



Low-Voltage Logic ALB, ALVC, LV, LVC, LVT, LVTZ, and GTL Families

Data Book

Low-Voltage Logic

ALB, ALVC, LV, LVC, LVT, LVTZ, and GTL Families

General Information	1
ALB Widebus™	2
ALVC Widebus™	3
LVT Octals	4
LVTZ Octals: Power Up and 3 State	5
LVT Widebus™	6
LVT JTAG/IEEE 1149.1	7
LVC MSI and Octals	8
LVC Widebus™	9
LV MSI and Octals	10
GTL Transceivers and Backplane Drivers	TE
Application Reports	12
Characteristics Information	13
Mechanical Data	14

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INTRODUCTION

The 3.3-V era has arrived! The combination of continuous advancement in semiconductor wafer fabrication technologies and the proliferation of battery-powered computing devices has changed system-design methodologies of the past, and indeed our entire industry. This new era brings a new set of possibilities for computing and hand-held instruments: products that run faster, consume less power, and use fewer total system components than ever before; products that are smaller and lighter, yet maintain interface compatibility with existing industry standard bus architectures; and products that will bring on the next era in the computer industry.

Welcome to the 1996 Texas Instruments Low-Voltage Logic Data Book. A single family of 3.3-V logic products could not possibly cover the diverse needs of all of the end-equipment segments. Products ranging from hand-held point-of-sale terminals, notebook and laptop personal computers, low-power environmentally conscious desktop computers and peripherals, and high-performance RISC and CISC workstation platforms share the need for low-voltage technology, but have radically different price, performance, and feature requirements for the logic they employ. As a response to these diverse needs, Texas Instruments has developed four independent logic families:

Advanced Low-Voltage CMOS (ALVC) Low-Voltage HCMOS (LV) Low-Voltage CMOS (LVC) Low-Voltage Technology (LVT)

These products span four generations of CMOS and BiCMOS process technologies and years of fine-pitch packaging and innovative circuit developments to deliver a set of products for each of these end-equipment segments. In addition to popular octal and Widebus™ bus-interface circuits, two of the families also include SSI and MSI logic functions to help streamline design and facilitate time to market.

Voltage translators are provided to bridge the gap between the 5-V and 3.3-V environments. In addition to the LVT family, the LVC family also is 5 V tolerant. This creates even more flexibility in the mixed-signal environments. Also new this year is the addition of the 2.5-V specification to the ALVC family. Designers of high-speed backplane applications will have great interest in the GTL family of transceivers.

Some of the information in this data book is in product-preview or advance-information form. For more information on these products including availability dates, pricing, and final timing specifications, please contact your local Texas Instruments field sales representative, authorized distributor, or call our Advanced System Logic hotline at (903) 868-5202.

We are sure you will agree that Texas Instruments has developed the most complete line of low-voltage logic products in the industry. We hope that these products will meet your system and design needs. Texas Instruments has been and will continue to be the logic leader for bus-interface products.

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General Information	1
ALB Widebus™	2
ALVC Widebus™	3
LVT Octals	4
LVTZ Octals: Power Up and 3 State	5
LVT Widebus™	6
LVT JTAG/IEEE 1149.1	7
LVC MSI and Octals	8
LVC Widebus™	9
LV MSI and Octals	10
GTL Transceivers and Backplane Drivers	11
Application Reports	12
Characteristics Information	13
Mechanical Data	14

Contents

	Page
Alphanumeric Index	1–3
Glossary	1–5
Explanation of Function Tables	1–9
D Flip-Flop and Latch Signal Conventions	1–11
Thermal Information	
Functional Index	1–15

ALPHANUMERIC INDEX

DEVICE	PAGE I	DEVICE	PAGE
ALB Widebus™		LV MSI and Octals (continued)	
SN74ALB16244		SN74LV32	10. 27
	2-5	SN74LV74	
ALVC Widebus™		SN74LV125	
SN74ALVC164245	j	SN74LV138	
SN74ALVCH16240		SN74LV164	
SN74ALVCH16244		SN74LV165	
SN74ALVCH16245		SN74LV174	
SN74ALVCH16260	l l	SN74LV240	
SN74ALVCH16269		SN74LV244	
SN74ALVCH16270		SN74LV245	
SN74ALVCH16271		SN74LV273	
SN74ALVCH16272		SN74LV373	
SN74ALVCH16344		SN74LV374	
SN74ALVCH16373		SN74LV573	10-87
SN74ALVOH46400		SN74LV574	10-91
SN74ALVOL46500	3	SN74LVU04	10-15
SN74ALVCH16500		LVO NOL d O-d-l-	
SN74ALVCH16501		LVC MSI and Octals	0.5
SN74ALVCH16525		SN74LVC00	
SN74ALVCH16543		SN74LVC02 SN74LVC04	
SN74ALVOU46646		SN74LVC08	
SN74ALVCH16646		SN74LVC10	
SN74ALVCH16052		SN74LVC32	
SN74ALVCH16820		SN74LVC74 SN74LVC86	
SN74ALVCH16821		SN74LVC86	
SN74ALVOH16825		SN74LVC112	
SN74ALVCH16827	1	SN74LVC126	
SN74ALVCH16827		SN74LVC126	
SN74ALVCH16841	1	SN74LVC138	
SN74ALVCH16843		SN74LVC138	
SN74ALVCH16901		SN74LVC157	
SN74ALVCH16952		SN74LVC158	
SN74ALVCH162268		SN74LVC240	
SN74ALVCH162525		SN74LVC241	
SN74ALVCH162601		SN74LVC244A	
SN74ALVCH162820		SN74LVC245A	
SN74ALVCH162827	1	SN74LVC257	
SN74ALVCHR162269	1	SN74LVC258	
SN74ALVCHR162409	1	SN74LVC373A	
	0 100	SN74LVC374A	
GTL Transceivers and Backplane Drivers		SN74LVC540	
SN54GTL16612 SN74GTL16612	i	SN74LVC541	
SN54GTL16616 SN74GTL16616	,	SN74LVC543	
SN54GTL16622 SN74GTL16622	1	SN74LVC544	
SN54GTL16921 SN74GTL16921	11–25	SN74LVC573A	
LV MSI and Octals	ļ	SN74LVC574A	
SN74LV00	. 10–3	SN74LVC646	
SN74LV02		SN74LVC652	
SN74LV04	10–11	SN74LVC821	
SN74LV08		SN74LVC823	
SN74LV14	10–23	SN74LVC827	



ALPHANUMERIC INDEX

DEVICE PAGE LVC MSI and Octals (continued) 8-195 SN74LVC828 8-199 SN74LVC841 8-199 SN74LVC843 8-203 SN74LVC861 8-207 SN74LVC863 8-211 SN74LVC2952 8-215 SN74LVC4245 8-109 SN74LVCH244 8-93 SN74LVCH245 8-103 SN74LVCH245 8-103 SN74LVCH6246 9-3 SN74LVC16240 9-3 SN74LVC16241 9-7 SN74LVC16244A 9-11 SN74LVC16245A 9-29 SN74LVC16373 9-47 SN74LVC16374 9-53 SN74LVC16540 9-59 SN74LVC16541 9-63 SN74LVC16540 9-59 SN74LVC16540 9-59 SN74LVC16540 9-59 SN74LVC16540 9-59 SN74LVC16540 9-63 SN74LVC16540 9-63 SN74LVC16540 9-75 SN74LVC16540 <t< th=""><th></th><th></th><th></th></t<>			
SN74LVC828 8-195 SN74LVC841 8-199 SN74LVC843 8-203 SN74LVC861 8-207 SN74LVC863 8-211 SN74LVC2952 8-215 SN74LVC4245 8-109 SN74LVCH244 8-93 SN74LVCH245 8-103 SN74LVCH245 8-103 SN74LVCH245 8-103 SN74LVCH244 9-3 SN74LVC16240 9-3 SN74LVC16241 9-7 SN74LVC16244A 9-11 SN74LVC16245A 9-29 SN74LVC16373 9-47 SN74LVC16540 9-53 SN74LVC16540 9-59 SN74LVC16541 9-63 SN74LVC16543 9-67 SN74LVC16543 9-67 SN74LVC16654 9-75 SN74LVC16952 9-83 SN74LVC16952 9-83 SN74LVC16952 9-93 SN74LVC16245 9-21 LVT JAG/IEEE 1149.1 SN54LVT18245 7-3 SN54LVT18640 SN74LVT18652 7-3 SN54LVT18666	DEVICE	•	PAGE
SN74LVC841 8-199 SN74LVC843 8-203 SN74LVC861 8-207 SN74LVC863 8-211 SN74LVC2952 8-215 SN74LVC4245 8-109 SN74LVCH244 8-93 SN74LVCH245 8-103 SN74LVCH245 8-103 SN74LVC16240 9-3 SN74LVC16241 9-7 SN74LVC16245A 9-11 SN74LVC16245A 9-29 SN74LVC16373 9-47 SN74LVC16540 9-53 SN74LVC16540 9-53 SN74LVC16540 9-53 SN74LVC16540 9-63 SN74LVC16540 9-67 SN74LVC16540 9-67 SN74LVC16540 9-75 SN74LVC16540 9-75 SN74LVC16	LVC MSI and Octals (continued)	
SN74LVC843 8-203 SN74LVC861 8-207 SN74LVC863 8-211 SN74LVC2952 8-215 SN74LVC4245 8-109 SN74LVCH244 8-93 SN74LVCH245 8-103 SN74LVCH245 8-103 SN74LVCH245 8-103 SN74LVC16240 9-3 SN74LVC16241 9-7 SN74LVC16245A 9-11 SN74LVC1624AA 9-11 SN74LVC16373 9-47 SN74LVC16374 9-59 SN74LVC16540 9-59 SN74LVC16541 9-63 SN74LVC16543 9-67 SN74LVC16544 9-67 SN74LVC16654 9-75 SN74LVC16654 9-75 SN74LVC16654 9-75 SN74LVC16952 9-83 SN74LVC16952 9-93 SN74LVC162244 9-23 SN74LVC162244 9-23 SN74LVT18245 N74LVT18502 SN54LVT18245 SN74LVT18504 7-3 SN54LVT18640 SN74LVT18504 7-3 SN54LVT18650	SN74LVC828		8-195
SN74LVC861 8-207 SN74LVC863 8-211 SN74LVC2952 8-215 SN74LVC4245 8-109 SN74LVCH244 8-93 SN74LVCH245 8-103 SN74LVCH245 8-103 SN74LVCH245 8-17 LVC Widebus™ SN74LVC16240 SN74LVC16241 9-7 SN74LVC16245A 9-11 SN74LVC16245A 9-29 SN74LVC16373 9-47 SN74LVC16374 9-53 SN74LVC16540 9-59 SN74LVC16541 9-63 SN74LVC16543 9-63 SN74LVC16654 9-75 SN74LVC16654 9-75 SN74LVC16654 9-75 SN74LVC16652 9-83 SN74LVC16952 9-93 SN74LVC16952 9-93 SN74LVC162244 9-23 SN74LVC162244 9-23 SN74LVC162244 9-23 SN74LVC162245 9-35 SN74LVT18244 9-1 LVT JAG/IEEE 1149.1 SN54LVT18245 7-3 SN54LVT18640 S	SN74LVC841		8-199
SN74LVC863 8-211 SN74LVC2952 8-215 SN74LVC4245 8-109 SN74LVCH244 8-93 SN74LVCH245 8-103 SN74LVCH245 8-103 SN74LVC16240 9-3 SN74LVC16241 9-7 SN74LVC1624A 9-11 SN74LVC16373 9-47 SN74LVC16540 9-59 SN74LVC16541 9-63 SN74LVC16543 9-63 SN74LVC16646 9-75 SN74LVC16652 9-83 SN74LVC16652 9-83 SN74LVC16652 9-93 SN74LVC16244A 9-17 SN74LVCH6245A 9-23 SN74LVCH6244A 9-17 SN74LVCH6245A 9-35 SN74LVCH6245A 9-35 SN74LVCH6245A 9-35 SN74LVCH6245A 9-35 SN74LVT18245 SN74LVT18260 SN74LVT18264 7-3 SN74LVT18264 7-3 SN54LVT18264 SN74LVT18264 SN54LVT182640 SN74LVT182640 7-3 SN54LVT182645	SN74LVC843		8-203
SN74LVC863 8-211 SN74LVC2952 8-215 SN74LVC4245 8-109 SN74LVCH244 8-93 SN74LVCH245 8-103 SN74LVCH245 8-103 SN74LVC16240 9-3 SN74LVC16241 9-7 SN74LVC1624A 9-11 SN74LVC16373 9-47 SN74LVC16540 9-59 SN74LVC16541 9-63 SN74LVC16543 9-63 SN74LVC16646 9-75 SN74LVC16652 9-83 SN74LVC16652 9-83 SN74LVC16652 9-93 SN74LVC16244A 9-17 SN74LVCH6245A 9-23 SN74LVCH6244A 9-17 SN74LVCH6245A 9-35 SN74LVCH6245A 9-35 SN74LVCH6245A 9-35 SN74LVCH6245A 9-35 SN74LVT18245 SN74LVT18260 SN74LVT18264 7-3 SN74LVT18264 7-3 SN54LVT18264 SN74LVT18264 SN54LVT182640 SN74LVT182640 7-3 SN54LVT182645	SN74LVC861		8-207
SN74LVC2952 8-215 SN74LVC4245 8-109 SN74LVCH244 8-93 SN74LVCH245 8-103 SN74LVCH246 8-17 LVC Widebus™ SN74LVC16240 SN74LVC16241 9-3 SN74LVC16245A 9-11 SN74LVC16373 9-47 SN74LVC16540 9-59 SN74LVC16541 9-59 SN74LVC16543 9-67 SN74LVC16646 9-75 SN74LVC16652 9-83 SN74LVC16652 9-83 SN74LVC16652 9-93 SN74LVC16652 9-93 SN74LVC162244 9-23 SN74LVC162245 9-35 SN74LVCH16244A 9-17 SN74LVCH16245A 9-35 SN74LVCH16245A 9-35 SN74LVT18265 7-3 SN74LVT18640 7-3 SN74LVT18640 7-3 SN54LVT18640 SN74LVT18640 7-3 SN54LVT182661 SN74LVT182640 7-3 SN54LVT182662 SN74LVT182640 7-3 SN54LVT182663 SN74LVT182640			
SN74LVC4245 8–109 SN74LVCH244 8–93 SN74LVCH245 8–103 SN74LVCU04 8–17 LVC Widebus™ SN74LVC16240 SN74LVC16241 9–3 SN74LVC16244A 9–11 SN74LVC16245A 9–29 SN74LVC16373 9–47 SN74LVC16540 9–59 SN74LVC16541 9–63 SN74LVC16543 9–67 SN74LVC16646 9–75 SN74LVC16652 9–83 SN74LVC16652 9–83 SN74LVC16652 9–83 SN74LVC166244 9–23 SN74LVC162244 9–23 SN74LVCH16245A 9–35 SN74LVCH16245A 9–35 SN74LVC162244 9–23 SN74LVC162245 9–31 LVT JTAG/IEEE 1149.1 NYALVT18604 7–3 SN54LVT18245 NYALVT18604 7–3 SN54LVT18646 SN74LVT18640 7–3 SN54LVT18646 SN74LVT18650 7–3 SN54LVT182640 SN74LVT182640 7–3 SN54LVT182640 SN74LVT182640			
SN74LVCH244 8-93 SN74LVCH245 8-103 SN74LVCU04 8-17 LVC Widebus™ SN74LVC16240 9-3 SN74LVC16241 9-7 SN74LVC16245A 9-11 SN74LVC16245A 9-11 SN74LVC16373 9-47 SN74LVC16540 9-59 SN74LVC16540 9-59 SN74LVC16540 9-63 SN74LVC16541 9-63 SN74LVC16543 9-67 SN74LVC166543 9-67 SN74LVC16652 9-83 SN74LVC16652 9-83 SN74LVC16652 9-93 SN74LVC165244 9-23 SN74LVC16244A 9-17 SN74LVC16244A 9-17 SN74LVCH16245A 9-35 SN74LVCH16245A 9-35 SN74LVCH16245A 9-35 SN74LVCH16245A 9-35 SN74LVCH16245A 9-35 SN74LVCH16245A 9-35 SN74LVT18245 SN74LVT18245 7-3 SN54LVT18245 SN74LVT18640 7-3 SN54LVT18646 SN74LVT18640 7-3 SN54LVT18652 SN74LVT18640 7-3 SN54LVT18652 SN74LVT18646 7-3 SN54LVT18245 SN74LVT18640 7-3 SN54LVT182640 SN74LVT18652 7-3 SN54LVT182640 SN74LVT182640 7-3 SN54LVT182652 SN74LVT182640 7-3 SN54LVT182652 SN74LVT182660 7-3 SN54LVT182652 SN74LVT182664 7-3 SN54LVT182653 SN74LVT182664 7-3 SN54LVT182654 SN74LVT182664 7-3 SN54LVT182655 SN74LVT182665 7-3 SN54LVT182650 SN74LVT182664 7-3 SN54LVT182650 SN74LVT182665 7-3 SN54LVT182650 SN74LVT182664 7-3 SN54LVT182650 SN74LVT182664 7-3 SN54LVT182650 SN74LVT182664 7-3 SN54LVT182650 SN74LVT182660 7-3 SN54LVT182650 SN74LVT182664 7-3 SN54LVT182650 SN74LVT182665 7-3 SN54LVT182650 SN74LVT182664 7-3 SN54LVT182650 SN74LVT182665 7-3 SN54LVT182650 SN74LVT182664 7-3 SN54LVT182650 SN74LVT182665 7-3 SN54LVT182660 SN74LVT182664 7-3 SN54LVT182660 SN74LVT182660 7-3			
SN74LVCH245 8–103 SN74LVCU04 8–17 LVC Widebus™ SN74LVC16240 9–3 SN74LVC16241 9–7 SN74LVC16245A 9–11 SN74LVC16373 9–47 SN74LVC16574 9–53 SN74LVC16540 9–59 SN74LVC16541 9–63 SN74LVC16543 9–67 SN74LVC16646 9–75 SN74LVC16652 9–83 SN74LVC16652 9–83 SN74LVC16652 9–83 SN74LVC162244 9–23 SN74LVCH162245 9–35 SN74LVCH162245 9–35 SN74LVCH162245 9–35 SN74LVCH162245 9–31 LVT JTAG/IEEE 1149.1 SN54LVT18245 7–3 SN54LVT18245 SN74LVT18245 7–3 SN74LVT18640 N74LVT182640 7–3 SN54LVT18662 SN74LVT182640 7–3 SN54LVT182640 SN74LVT182640 7–3 SN54LVT182640 SN74LVT182640 7–3 SN54LVT182640 SN74LVT182640 7–3 SN54LVT182640 SN74L			
SN74LVCU04 8-17 LVC Widebus™ SN74LVC16240 9-3 SN74LVC16241 9-7 SN74LVC16245A 9-11 SN74LVC16373 9-47 SN74LVC16540 9-53 SN74LVC16540 9-59 SN74LVC16541 9-63 SN74LVC16543 9-67 SN74LVC16646 9-75 SN74LVC16652 9-83 SN74LVC16652 9-83 SN74LVC16652 9-93 SN74LVC1662244 9-23 SN74LVCH16245A 9-17 SN74LVCH16245A 9-35 SN74LVCH16245 9-35 SN74LVCH16245 9-35 SN74LVT18245 7-3 SN74LVT18640 SN74LVT18502 7-3 SN54LVT18646 SN74LVT18640 7-3 SN54LVT18652 SN74LVT18652 7-3 SN54LVT18265 SN74LVT182502 7-3 SN54LVT182640 SN74LVT182504 7-3 SN54LVT182640 SN74LVT182640 7-3 SN54LVT182640 SN74LVT182640 7-3 SN54LVT182640 SN7			
LVC Widebus™ SN74LVC16240 9-3 SN74LVC16241 9-7 SN74LVC16244A 9-11 SN74LVC16245A 9-29 SN74LVC16373 9-47 SN74LVC16540 9-53 SN74LVC16541 9-63 SN74LVC16543 9-67 SN74LVC166543 9-67 SN74LVC16652 9-83 SN74LVC16652 9-83 SN74LVC16952 9-93 SN74LVC162244 9-23 SN74LVCH16244A 9-17 SN74LVCH16245A 9-35 SN74LVCH16245A 9-35 SN74LVT18245 SN74LVT18502 7-3 SN54LVT18245 SN74LVT18504 7-3 SN54LVT18640 SN74LVT18640 7-3 SN54LVT18652 SN74LVT18646 7-3 SN54LVT182504 SN74LVT182645 7-3 SN54LVT182640 SN74LVT182640 7-3 SN54LVT182640 SN74LVT182640 7-3 SN54LVT182646 SN74LVT182640 7-3 SN54LVT182646 SN74LVT182640 7-3 SN54LVT182646 SN74LVT182652			
SN74LVC16240 9-3 SN74LVC16241 9-7 SN74LVC16244A 9-11 SN74LVC16373 9-29 SN74LVC16374 9-53 SN74LVC16540 9-59 SN74LVC16541 9-63 SN74LVC16543 9-67 SN74LVC16646 9-75 SN74LVC16652 9-83 SN74LVC16652 9-83 SN74LVC162244 9-23 SN74LVCH16244A 9-17 SN74LVCH16245A 9-35 SN74LVCH16245 9-35 SN74LVT18245 SN74LVT18502 7-3 SN54LVT18640 SN74LVT18504 7-3 SN54LVT18640 SN74LVT18640 7-3 SN54LVT18652 SN74LVT18640 7-3 SN54LVT182245 SN74LVT182640 7-3 SN54LVT182640 SN74LVT182640 7-3 SN54LVT240 SN74LVT240 4	3N/4LVC004	• • • • • • • • • • • • • • • • • • • •	. 0-17
SN74LVC16241 9-7 SN74LVC16244A 9-11 SN74LVC16245A 9-29 SN74LVC16373 9-47 SN74LVC16540 9-53 SN74LVC16541 9-63 SN74LVC16543 9-67 SN74LVC16654 9-75 SN74LVC16652 9-83 SN74LVC16652 9-83 SN74LVC162244 9-23 SN74LVCH1624AA 9-17 SN74LVCH16245A 9-35 SN74LVCH16245A 9-35 SN74LVT18245 SN74LVT18502 7-3 SN54LVT18640 SN74LVT18640 7-3 SN54LVT18646 SN74LVT18640 7-3 SN54LVT18652 SN74LVT18652 7-3 SN54LVT18245 SN74LVT18652 7-3 SN54LVT182646 SN74LVT182504 7-3 SN54LVT182645 SN74LVT182640 7-3 SN54LVT182646 SN74LVT182640 7-3 SN54LVT182646 SN74LVT182646 7-3 SN54LVT182646 SN74LVT182646 7-3 SN54LVT182645 SN74LVT182646 7-3 SN54LVT182652	LVC Widebus™		
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LVT Octals SN54LVT125 SN74LVT125 4-3 SN54LVT240 SN74LVT240 4-9 SN54LVT241 SN74LVT241 4-15 SN54LVT244 SN74LVT244A 4-21 SN54LVT245 SN74LVT245A 4-27 SN54LVT273 SN74LVT273 4-33 SN54LVT543 SN74LVT543 4-39 SN54LVT573 SN74LVT573 4-47 SN54LVT574 SN74LVT574 4-53			
SN54LVT125 4-3 SN54LVT240 SN74LVT240 4-9 SN54LVT241 SN74LVT241 4-15 SN54LVT244 SN74LVT244A 4-21 SN54LVT245 SN74LVT245A 4-27 SN54LVT273 SN74LVT273 4-33 SN54LVT543 SN74LVT543 4-39 SN54LVT573 SN74LVT573 4-47 SN54LVT574 SN74LVT574 4-53	SIN34LV I 182032	SN/4LV1182002	/-3
SN54LVT240 \$N74LVT240 \$4-9\$ SN54LVT241 \$N74LVT241 \$4-15\$ SN54LVT244 \$N74LVT244A \$4-21\$ SN54LVT245 \$N74LVT245A \$4-27\$ SN54LVT273 \$N74LVT273 \$4-33\$ SN54LVT543 \$N74LVT543 \$4-39\$ SN54LVT573 \$N74LVT573 \$4-47\$ SN54LVT574 \$N74LVT574 \$4-53\$	LVT Octals		
SN54LVT241 \$N74LVT241 4-15 SN54LVT244 \$N74LVT244A 4-21 SN54LVT245 \$N74LVT245A 4-27 SN54LVT273 \$N74LVT273 4-33 SN54LVT543 \$N74LVT543 4-39 SN54LVT573 \$N74LVT573 4-47 SN54LVT574 \$N74LVT574 4-53	SN54LVT125	SN74LVT125	4–3
SN54LVT244 SN74LVT244A 4-21 SN54LVT245 SN74LVT245A 4-27 SN54LVT273 SN74LVT273 4-33 SN54LVT543 SN74LVT543 4-39 SN54LVT573 SN74LVT573 4-47 SN54LVT574 SN74LVT574 4-53	SN54LVT240	SN74LVT240	4–9
SN54LVT245 SN74LVT245A 4-27 SN54LVT273 SN74LVT273 4-33 SN54LVT543 SN74LVT543 4-39 SN54LVT573 SN74LVT573 4-47 SN54LVT574 SN74LVT574 4-53	SN54LVT241	SN74LVT241	. 4–15
SN54LVT245 SN74LVT245A 4–27 SN54LVT273 SN74LVT273 4–33 SN54LVT543 SN74LVT543 4–39 SN54LVT573 SN74LVT573 4–47 SN54LVT574 SN74LVT574 4–53	SN54LVT244	SN74LVT244A	. 4–21
SN54LVT273 4-33 SN54LVT543 SN74LVT543 4-39 SN54LVT573 SN74LVT573 4-47 SN54LVT574 SN74LVT574 4-53	SN54LVT245	SN74LVT245A	. 4–27
SN54LVT543 4-39 SN54LVT573 SN74LVT573 4-47 SN54LVT574 SN74LVT574 4-53	SN54LVT273		
SN54LVT573 SN74LVT573 4–47 SN54LVT574 SN74LVT574 4–53			
SN54LVT574 SN74LVT574 4–53			
O110 121 1010 O111 721 1010			
SN54LVT652 SN74LVT652 4–69			

DEVICE	PAGE
VT Octals (continue	d)
SN54LVT2952	SN74LVT2952 4–79
.VT Widebus™	
SN54LVT16244A	SN74LVT16244A 6-3
SN54LVT16245A	SN74LVT16245A 6–15
SN54LVT16373	SN74LVT16373 6–27
SN54LVT16374	SN74LVT16374 6-37
SN54LVT16500	SN74LVT16500 6-47
SN54LVT16501	SN74LVT16501 6-55
SN54LVT16543	SN74LVT16543 6-63
SN54LVT16600	SN74LVT16600 6-71
SN54LVT16601	SN74LVT16601 6-77
SN54LVT16646	SN74LVT16646 6-83
SN54LVT16652	SN74LVT16652 6–93
	SN74LVT16835 6-101
SN54LVT16952	SN74LVT16952 6-107
SN54LVT162244	SN74LVT162244 6-9
SN54LVT162245	SN74LVT162245 6-21
SN54LVT162373	SN74LVT162373 6–33
SN54LVT162374	SN74LVT162374 6-43
VTZ Octals	
SN54LVTZ240	SN74LVTZ240 5–3
SN54LVTZ244	SN74LVTZ244 5–9
SN54LVTZ245	SN74LVTZ245 5–15



INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

operating conditions and characteristics (in sequence by letter symbols)

C_i Input capacitance

The internal capacitance at an input of the device

Cio Input/output capacitance

Input-to-output internal capacitance; transcapacitance

Co Output capacitance

The internal capacitance at an output of the device

C_{pd} Power dissipation capacitance

Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $P_D = C_{\rm pd} \cdot V_{\rm CC}^2 + I_{\rm CC} \cdot V_{\rm CC}$

f_{max} Maximum clock frequency

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification

I_{CC} Supply current

The current into* the V_{CC} supply terminal of an integrated circuit

ΔI_{CC} Supply current change

The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or VCC

I_{CEX} Output high leakage current

The maximum leakage current into the collector of the pulldown output transistor when the output is high and the output forcing condition $V_O = 5.5 \text{ V}$

I_{I(hold)} Input hold current

Input current that holds the input at the previous state when the driving device goes to a high-impedance state

I_{IH} High-level input current

The current into* an input when a high-level voltage is applied to that input

I_{IL} Low-level input current

The current into* an input when a low-level voltage is applied to that input

Ioff Input/output power-off leakage current

The current into a circuit mode when the device or a portion of the device affecting that circuit node is in the off state

IOH High-level output current

The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output

^{*}Current out of a terminal is given as a negative value.



GLOSSARY SYMBOLS, TERMS, AND DEFINITIONS

Low-level output current loL

The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output

Off-state (high-impedance-state) output current (of a 3-state output) IOZPU/PD

The current flowing into* an output having 3-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output

Access time ta

The time interval between the application of a specified input pulse and the availability of valid signals at an output

Clock cycle time tc

Clock cycle time is 1/fmax

Disable time (of a 3-state or open-collector output) tdis

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state

For 3-state outputs, t_{dis} = t_{PHZ} or t_{PLZ}. Open-collector outputs will change only if they are low NOTE: at the time of disabling, so tdis = tpl H-

Enable time (of a 3-state or open-collector output) ten

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low)

NOTE: In the case of memories, this is the access time from an enable input (e.g., \overline{OE}). For 3-state outputs, ten = tpzH or tpzL. Open-collector outputs will change only if they are responding to data that would cause the output to go low, so $t_{en} = t_{PHL}$.

Hold time th

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is to be expected.

Propagation delay time tpd

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level (tpd = tpHL or tpLH)

Propagation delay time, high-to-low level output **tPHL**

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level

t_{PHZ} Disable time (of a 3-state output) from high level

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to the high-impedance (off) state

*Current out of a terminal is given as a negative value.



tpLH Propagation delay time, low-to-high level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level

tpl Z Disable time (of a 3-state output) from low level

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined low level to the high-impedance (off) state

tpzH Enable time (of a 3-state output) to high level

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined high leve

t_{PZL} Enable time (of a 3-state output) to low level

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined low level

t_{sk(o)} Output Skew

The difference between any two propagation delay times when a single switching input or multiple inputs switching simultaneously cause multiple outputs to switch, as observed across all switching output. This parameter is used to describe the fanout capability of a clock driver and is of concern when making decisions on clock buffering and distribution networks.

t_{su} Setup time

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value, in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

tw Pulse duration (width)

The time interval between specified reference points on the leading and trailing edges of the pulse waveform

V_{IH} High-level input voltage

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables

NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is to be expected.

V_{IL} Low-level input voltage

An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables

NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is to be expected.

V_{OH} High-level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output



GLOSSARY SYMBOLS, TERMS, AND DEFINITIONS

V_{OL} Low-level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output

V_{IT+} Positive-going input threshold level

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{IT}_

V_{IT} Negative-going input threshold level

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, $V_{\rm IT+}$



EXPLANATION OF FUNCTION TABLES

The following symbols are used in function tables on TI data sheets:

H = high level (steady state)
L = low level (steady state)

↑ = transition from low to high level
 ↓ = transition from high to low level

= value/level or resulting value/level is routed to indicated destination

= value/level is re-entered

X = irrelevant (any input, including transitions)
 Z = off (high-impedance) state of a 3-state output

a...h = the level of steady-state inputs A through H respectively

Q₀ = level of Q before the indicated steady-state input conditions were established

 \overline{Q}_0 = complement of Q_0 or level of \overline{Q} before the indicated steady-state input

conditions were established

 Q_n = level of Q before the most recent active transition indicated by \downarrow or \uparrow

= one high-level pulse = one low-level pulse

Toggle = each output changes to the complement of its previous level on each active

transition indicated by ↓ or ↑

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with \uparrow and/or \downarrow , this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q₀, or \overline{Q}_0), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, $\neg \neg \neg \neg \neg$, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)



EXPLANATION OF FUNCTION TABLES

Among the most complex function tables are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

FUNCTION TABLE

			OUTPUTS										
CLEAR	MO	DE	CLOCK	SEI	RIAL		PARA	LLEL		٥.	Ω-	0-	0-
CLEAR	S1	S0	CLOCK	LEFT	RIGHT	Α	В	С	D	QA	QB	ФС	QD
L	Х	Х	Х	Х	Х	Х	Х	Х	Х	L	L	L	L
н	Х	Χ	L	Х	Χ	Х	Х	Х	Χ	Q _{A0}	Q_{B0}	Q _{C0}	Q_{D0}
н	Н	Н	1	х	Х	а	b	С	d	a	b	С	d
н	L	Н	1	Х	Н	н	Н	Н	Н	н	Q_{An}	Q_{Bn}	\mathbf{Q}_{Cn}
н	L	Н	1	х	L	L	L	L	L	L	Q _{An}	Q_{Bn}	Q_{Cn}
н	Н	L	1	н	Χ	х	. X	Х	Х	QBn	QCn	Q_{Dn}	Н
н	Н	L	1	L	X	х	Х	Х	Х	QBn	Q_{Cn}	Q_{Dn}	L
Н	L	L	Х	х	X	Х	X	Χ	Χ	Q _{A0}	Q_{B0}	Q _{C0}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A , data entered at B will be at Q_B , and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B , the previous levels of Q_B and Q_C are now at Q_C and Q_D , respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A , the previous levels of Q_C and Q_D are now at Q_B and Q_C , respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

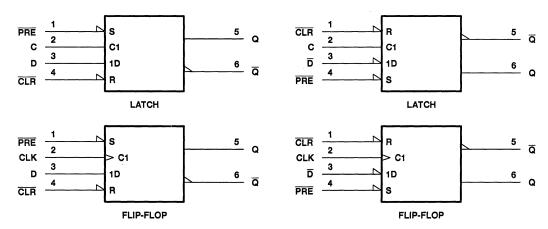
The function table functional tests do not reflect all possible combinations or sequential modes.

D FLIP-FLOP AND LATCH SIGNAL CONVENTIONS

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called \overline{Q} . An input that causes a Q output to go high or a \overline{Q} output to go low is called preset (PRE). An input that causes a \overline{Q} output to go high or a Q output to go low is called clear (CLR). Bars are used over these pin names (PRE and CLR) if they are active low.

The devices on several data sheets are second-source designs, and the pin name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits \overline{D} and Q.

In some applications, it may be advantageous to redesignate the data input from D to \overline{D} or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown.



The figures show that when Q and \overline{Q} exchange names, the preset and clear pins also exchange names. The polarity indicators (\square) on \overline{PRE} and \overline{CLR} remain, as these inputs are still active low, but the presence or absence of the polarity indicator changes at D (or \overline{D}), Q, and \overline{Q} . Pin 5 (Q or \overline{Q}) is still in phase with the data input (D or \overline{D}); their active levels change together.

THERMAL INFORMATION

In digital system design, consideration must be given to thermal management of components. The small size of the small-outline package makes this even more critical. Figure 1 shows the thermal resistance of these packages for various rates of air flow. Figures 2, 3, 4, and 5 are derating curves for the DB package.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures for the LVL family. In general, the junction temperature for any device can be calculated using the following equation.

$$T_J = R_{\Theta JA} \times P_T + T_A$$

Where:

T_J = virtual junction temperature

 $R_{\theta JA}$ = thermal resistance, junction to free air P_T = total power dissipation of the device

 T_{Δ} = free-air temperature

JUNCTION-TO-AMBIENT THERMAL RESISTANCE

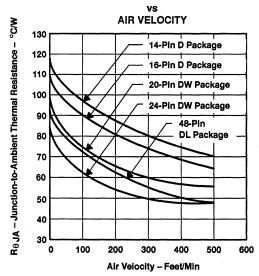
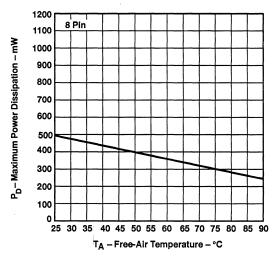


Figure 1

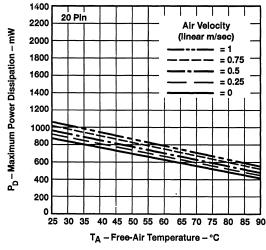
DERATING CURVES FOR 210-MIL SHRINK SMALL-OUTLINE PACKAGE (DB)



1200 16 Pin P_D- Maximum Power Dissipation – mW 1000 800 600 Air Velocity 400 (linear m/sec) = 0.75200 = 0.5= 0.2525 30 35 40 45 50 55 60 65 70 75 80 85 90 T_A - Free-Air Temperature - °C

Figure 2

Figure 3



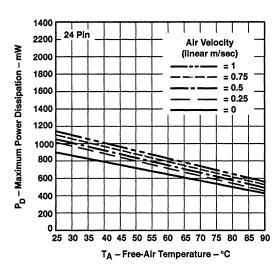


Figure 4

Figure 5

Current Texas Instruments Advanced Logic Publications

Listed below is the current collection of Texas Instruments logic technical documentation. The alphanumeric code is the literature number for each item listed. These documents can be ordered through a TI representative or authorized distributor by referencing the literature number.

	Document L	iterature Number
	Advanced BiCMOS Technology Data Book (1994)	SCBD002B
	Advanced Bus-Interface SPICE I/O Models Data Book (1995)	SCBD004A
	Advanced CMOS Logic Data Book (1993)	SCAD001C
	Advanced Logic and Bus-Interface Logic Data Book (1991)	SCYD001
	ALS/AS Logic Data Book (1995)	SDAD001C
	BCT BiCMOS Bus-Interface Logic Data Book (1994)	SCBD001B
	Boundary-Scan Logic, IEEE Std. 1149.1 (JTAG) 5-V and 3.3-V Bus-Interface and Scan-Support Products Data Book (1994)	SCTD002
	CBT Bus Switches Crossbar Technology Data Book (1995)	SCDD001
	CDC Clock-Distribution Circuits Data Book (1994)	SCAD004
	F Logic Data Book (1994)	SDFD001B
	High-Performance FIFO Memories Data Book (1996)	SCAD003C
	High-Performance FIFO Memories Designer's Handbook (1996)	SCAA012A
	High-Speed CMOS Logic Data Book (1989)	SCLD001C
	Low-Voltage Logic Data Book (1996)	SCBD003B
	TTL Logic Data Book (TTL, LS, S) (1988)	SDLD001A
	Semiconductor Group Package Outlines Reference Guide	SSYU001A
2	the books listed above, the following documents are available only in Eu	rope.

In addition to

Document	Literature Number
Advanced BiCMOS Technology Data Book (1994)	SCBDE08
CBT Crossbar Technology Data Book (1995)	SCDDE01
CDC Data and Applications Manual (1995)	SCBTE07B
Packaging Data Book (1995)	SCYDE04
ASL SCOPE™ Products Data and Applications Manual (1994)	SCBDE09



GATES

Positive-NAND Gates

DECODIDATION	OUTDUT	TYPE	TECHNOLOGY													
DESCRIPTION	OUTPUT	ITPE	ALS	AS	F	LS	S	∠ TTL	AC	ACT	AHC	AHCT	HC	HCT	LV	LVC
8 Input		'30	~	~	~	~	~	~								
13 Input		'133	~				~									
Dual 4 Input		'20	~	~	~	~	~						~			
Triple 3 Input		'10	~	~	~	~	~		~	~			~			~
		'00	~	~	~	~	~	V-	V.	~	~	~	V	~	~	V
		'37	~			~	~	~								
Quad 2 Input	OC	'38	~		~	~	1	~						-		
		'132				~	~	~					~			
		'1000		~		-										
		'804	~	~												
Hex 2 Input		'1804		~												
Quad 2 Input	OC	'03	~			~							~			
Dual 2 Input		'8003	~													

Positive-AND Gates

PEROPIPEION	ОИТРИТ	TVDE							TECHN	IOLOGY						
DESCRIPTION		TYPE	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	нс	HCT	LV	LVC
0 -1011	OC.	'09	~			~	~									
Quad 2 Input		'7001											~			
Dual 4 Input		'21	~	~	~	~							~			
Triple 3 Input		'11	~	~	~	~	~		~	~			~			
0 -101 - 1		'08	~	~	~	~	~		٧.	V.	~	~	~	~	~	~
Quad 2 Input		'1008		~												
Hex 2 Input		'808		~												
		'1808		~												

[✔] Product available in technology indicated

[•] Product available in reduced-noise advanced CMOS (11000 series)

⁺ New product planned in technology indicated

GATES

Positive-OR/NOR Gates

DESCRIPTION	OUTDUT	TVDE	TECHNOLOGY													
DESCRIPTION	OUTPUT	ITPE	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	HC	HCT	LV	LVC
Ouad 2 Input		'32	~	~	~	~	~	~	٧.	V.	~	~	~	~	~	V
Quad 2 Input		'1032		~												
Hex 2 Input		'832	~	~												
nex 2 input		'1832		~	:											
Dual 5 Input		'260			~		~									
Triple 3 Input		'27	~		~	~							~			
		'02	~	~	V.	~	~						~	~	~	~
Quad 2 Input	OC	'33				~										
		'7002											~			
		'805	~	V												
Hex 2 Input		'1805		~												

OR/NOR Gates

DESCRIPTION	OUTPUT	TYPE							JECHN	OLOGY						
DESCRIPTION	OUIPUI	ITPE	ALS	AS	F	LS	S	ΠL	AC	ACT	AHC	AHCT	HC	нст	LV	LVC
Quad 2-Input Exclusive-OR Gates With Totem-Pole Outputs		'86	~		~	v			v •	~	V	~	~			~
Quad 2-Input Exclusive-NOR Gates	OD	'266				~							V.			

[✔] Product available in technology indicated

Product available in reduced-noise advanced CMOS (11000 series)

⁺ New product planned in technology indicated

INVERTING/NONINVERTING BUFFERS

Hex Inverters/Noninverters

DESCRIPTION	OUTDUT	TVDE							TECHN	OLOGY				,		
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	LS	S	ΠL	AC	ACT	AHC	AHCT	HC	HCT	LV	LVC
		'04	~	~	~	~	~	~	V.	V.	~	~	V	~	~	~
		'U04									~		V		V	~
	OC	'05	~			~	~	~					V			
Hex Inverters		'06						V								
		'14				V		~	~	~	~	V	V		~	V
		'1004	~	V												
		'1005	~													
	ОС	'35	~													
Hex Noninverters		'1034	~	~												
	ОС	'1035	~													

BUFFERS/DRIVERS AND BUS TRANSCEIVERS

Buffers/Drivers

DECORIDED	OUTDUT	TVDE									T	ECHNO	LOGY								
DESCRIPTION	OUTPUT	TYPE	ABT	вст	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	OTHER
2-Bit Buffers	3S	'306		~																	
Quad Buffers/Drivers	38	'125	~	~	~			V	~					+	+		V	~	~	~	
Quad bullers/Drivers	33	'126	~	~				~	~					+	+		٧				
Hex Buffers	OC	'07									~										
Noninverting	3S	'365							~								1				
Hex Buffers/Drivers	3S	'367							~		~						~				_
Inverting Hex Buffers/Drivers	38	'368						,	~		~						~				

[✔] Product available in technology indicated

 Product available in reduced-noise advanced CMOS (11000 series)

⁺ New product planned in technology indicated

BUFFERS/DRIVERS AND BUS TRANSCEIVERS

Buffers/Drivers (Continued)

DESCRIPTION	ОИТРИТ	TYPE									Т	ECHNO	LOGY								
DESCRIPTION	OUIPUI	ITPE	ABT	ВСТ	LVT	ALS	AS	F	LS	S	ΠL	AC	ACT	AHC	AHCT	ALVC	НС	нст	LV	LVC	OTHER
		'241	~	~	~	~	~	V	V	~		V	V				V				
		'244	~	~	V	~	V	V	V	~		٧.	V.	~	~		V	~	V	~	+LVCH
	38	'1240				~															
Noninverting	35	'1244				~													-		
Octal Buffers/Drivers		'25244		V																	
		'541	V	~		~		~	~					~	~		V	~		~	
	oc	'757		•			~														
		'760		V		~	V														
	38	'240	~	V	V	~	~	V	~	V		٧.	V.	~	~		V	~	V	~	
Inverting Octal Buffers/Drivers	35	'540	~	~		~			~					~	~		V	~		~	
Octal bullers/blivers	OC	'756		~			~														
Inverting and Noninverting Octal Buffers/Drivers	38	'230					~														
Noninverting		'827	~																	1	
10-Bit Buffers/Drivers	3S	'29827		~		4															
Inverting		'828																		1	
10-Bit Buffers/Drivers	3S	'29828		V		~															
		'16241	~										V			~				V	
Noninverting 16-Bit Buffers/Drivers	38	'16244	V		~							~	~			V				~	
10-Dit Dullers/Drivers		'16541	V										~							~	
Inverting		'16240	V									V	~			~				~	
16-Bit Buffers/Drivers	3S	'16540	~										~							V	
Noninverting	00	'16825	V										V			~					
18-Bit Buffers/Drivers	3S	'16835			~											~					
Noninverting 20-Bit Buffers/Drivers	38	'16827	v										~			v					

[✔] Product available in technology indicated

[•] Product available in reduced-noise advanced CMOS (11000 series)

⁺ New product planned in technology indicated

Universal Bus Transceivers (UBT™)/Universal Bus Exchangers (UBE™)

DECORIDATION	OUTDUT	TVDE	İ		•	TECHNOLOG	Υ£		
DESCRIPTION	OUTPUT	TYPE	ABT	ВСТ	LVT	LV	LVC	ALVC	OTHER
Noninverting 9-Bit 4-Port UBE™	38	'16409						~	
Noninverting 17-Bit UBT™ With Buffered Clock Outputs and Output Edge Control (OEC™)	OD	'16616							✓GTL
		'16500	~		~			~	
Nacionatina 10 Di LIDTIN	38	'16501	~					~	
Noninverting 18-Bit UBT™	33	'16600	~					~	
	l	'16601	~					~	
Noninverting 18-Bit UBT™ With Output Edge Control (OEC™)	OD	'16612							✓GTL
Noninverting 18-Bit UBT™	OD	'16622							+GTL
Noninverting 36-Bit UBT™	38	'32501	~						
Noninverting 16-Bit Tri-Port UBE™	38	'32316	~						
Noninverting 18-Bit Tri-Port UBE™	38	'32318	~						
		'162500	~						
18-Bit UBT™ With Series Resistors on B Port	38	'162501	~						
		'162601	~					~	
Noninverting 18-Bit UBT™ With Parity Generators /Checkers	38	'16901						~	
SCOPE™ 18-Bit UBT™	38	'18502	~		~				
SCOPE™ 20-Bit UBT™	38	'18504	~		~				

[✔] Product available in technology indicated

Product available in reduced-noise advanced CMOS (11000 series)

⁺ New product planned in technology indicated

FUNCTIONAL INDEX

BUFFERS/DRIVERS AND BUS TRANSCEIVERS

Bus Transceivers

DESCRIPTION	OUTPUT	TYPE									Т	ECHNO	LOGY								
DESCRIPTION	OUIPUI	ITPE	ABT	BCT	LVT	ALS	AS	F	LS	S	ΠL	AC	ACT	AHC	AHCT	ALVC	НС	HCT	LV	LVC	OTHER
Inverting Quad Transceivers	ос	758		-		~															_
Noninverting Quad Transceivers	38	'243				~		~	~												
		'245	~	~	V	~	~	~	~			V.	V•	~	~		V	~	١	~	+LVCH
		'1245				~															
	38	'25245	~	V																	
Noninverting		'645				~	~		~								~	~			
Octal Transceivers		'1645				~															
	oc	'621				~															
		'641				~	~		~												
	OC/3S	'639				~	~														
		'620	~			~															
	38	'623	~	~		~		~	~								~	~			
Inverting	35	'640	~	~		~	~		~								~				
Octal Transceivers		'1640				~															
	oc	'642				~			~												
	OC/3S	'638				~	~														
Noninverting	38	'863	~																	~	
9-Bit Transceivers	33	29863		~		~															
Noninverting 10-Bit Transceivers	38	'861	~																	~	
Noninverting	00	'16245	~		~							~	~			~				~	✓ ABTE
16-Bit Transceivers	38	'16623	~										~								
Noninverting 16-Bit Transceivers, 3.3-V-to-5-V Level Shifter	38	'164245														~					
Inverting	200	'16640	~									V	~								
16-Bit Transceivers	3S	'16620										~	~								
Noninverting 18-Bit Transceivers	38	'16863	~										~			~					

[✔] Product available in technology indicated

Product available in reduced-noise advanced CMOS (11000 series)

⁺ New product planned in technology indicated

Bus Transceivers (Continued)

DESCRIPTION	OUTPUT	TYPE									T	ECHNO	LOGY								
DESCRIPTION	OUIPUI	ITPE	ABT	ВСТ	LVT	ALS	AS	F	LS	S	ΠL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	OTHE
Inverting 18-Bit Transceivers	3S	'16864											~		-		-				
Noninverting 20-Bit Transceivers	38	'16861											~								
		'543	~	~	~			~												~	
	38	'646	~	~	~	~	~		~								>	~		~	
Noninverting	35	'652	~	~	~	~	V		~			•	•				V	~		~	
Octal Registered Transceivers		'2952	~		~															~	
	OC/3S	'653				~															
	00/35	'654				~															
Inverting		'648				~	~		~												
Octal Registered	38	'651	~			~	~														
Transceivers		'2953		~																	
		'16470	~										~								
Noninverting		'16543	~		~							~	~			~				~	
16-Bit Registered	38	'16646	~		~							~	~			~				~	
Transceivers		'16652	~		~							~	~							~	
		'16952	~		~								~		-					+	
Inverting		'16544											~								
16-Bit Registered	38	'16648											~								
Transceivers		'16651											~								
		'16474											~								
Noninverting		'16500	~		٧											~	ļ	<u> </u>			<u> </u>
18-Bit Registered	38	'16501	~		٧											~					
Transceivers		'16600	~													~					
		'16601	~													~					
Noninverting 36-Bit Transceivers	38	'32245	~																		
Noninverting 36-Bit	3S	'32501	~																		
Registered Transceivers	35	'32543	V																		

[✔] Product available in technology indicated

 Product available in reduced-noise advanced CMOS (11000 series)

⁺ New product planned in technology indicated

BUFFERS/DRIVERS AND BUS TRANSCEIVERS

Bus Transceivers (Continued)

DESCRIPTION	OUTPUT	TYPE									Т	ECHNO	LOGY								
DESCRIPTION	OUIPUI	ITPE	ABT	вст	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	нс	нст	LV	LVC	OTHER
		'657	~																		
8-/9-Bit	38	'833	~																		
Bus Transceivers		'853	~																		
With Parity Checkers/ Generators	ĺ	'29833				~															
Generators	3S/OC	'29834		~																	
		'29854		~																	
Dual 8-/9-Bit Bus Transceivers		'16833	~										~								
With Parity Checkers/	3S	'16657	~										~								
Generators		'16853	~					<u></u>													
Noninverting 16-Bit Tri-Port Registered Bus Exchangers	38	'32316	-																		
Noninverting 18-Bit Tri-Port Registered Bus Exchangers	3S	'32318	~													-					
7-Bit TTL/BTL Transceivers	ос	'2041	-																		√ FB
8-Bit TTL/BTL Transceivers	ос	'2040																			√ FB
8-Bit TTL/BJL Registered Transceivers	ос	'2033																			✓ FB
9-Bit TTL/BTL Competition Transceivers	ос	'2032																			+FB
9-Bit TTL/BTL Address/ Data Transceivers	ос	'2031																			√ FB
17-Bit TTL/BTL Universal Storage Transceivers	ос	'1651																			√ FB
18-Bit TTL/BTL Universal Storage Transceivers	ос	'1650																			√ FB

[✔] Product available in technology indicated

 Product available in reduced-noise advanced CMOS (11000 series)
 + New product planned in technology indicated

MOS Memory Drivers/Transceivers

DESCRIPTION	OUTPUT	TYPE						TEC	HNOLO	GY				
DESCRIPTION	OUIPUI	ITPE	ABT	вст	LVT	ALS	AS	F	AC	ACT	ALVC	LV	LVC	OTHER
		'2240	V	~		~								
OLID Wall to NEW O. to Double on O. to I		'2241	~											
Octal Buffers/Drivers With Series Resistors on Output	38	'2244	~	~				~						
		'2541				~								
Octal Transceivers With Series Resistors on B Port	38	'2245	~	~				~						
AO D'I D. M. M. D. L. D. L.		'2827		~										
10-Bit Buffers/Drivers With Series Resistors	38	'2828		~										
10-Bit Flip-Flops With Dual Outputs and Series Resistors	38	'162820									V			
44 Pi P # - #P i Mrit O i P - i - i -		'5400	~											
11-Bit Buffers/Drivers With Series Resistors	38	'5401	~											
		'5402	~											
12-Bit Buffers/Drivers With Series Resistors	38	'5403	~											
16-Bit Buffers/Drivers With Series Resistors	38	'162244	~		V						~		V	
16-Bit Transceivers With Series Resistors	38	'162245	~		~						~			∠ LVTH
16-Bit D-Type Latches With Series Resistors	38	'162373			~									
16-Bit D-Type Flip-Flops With Series Resistors	38	'162374			V									
4-to-1 Multiplexed/Demultiplexed Registered Transceivers With Series Resistors	3S	'162460	~											
		'162500	V											
18-Bit UBT™ With Series Resistors on B Port	38	'162501	~											
		'162601	~								~			
18-Bit Bus-Interface Flip-Flops With Series Resistors	38	'162823	~											
18-Bit Buffers/Drivers With Series Resistors	38	'162825	~											
20-Bit Buffers/Drivers With Series Resistors	3S	'162827	~											
12-to-24 Multiplexed D-Type Latches With Series Resistors on B Port	38	162260	1											

[✔] Product available in technology indicated

Product available in reduced-noise advanced CMOS (11000 series)

⁺ New product planned in technology indicated

FUNCTIONAL INDE

TESTABILITY BUS-INTERFACE CIRCUITS

IEEE 1149.1 (JTAG) Boundary-Scan Logic

DECODIDETON	NO. OF	OUTPUT	TVDF					TECHN	OLOGY				
DESCRIPTION	BITS	COIPOI	TYPE	ABT	ВСТ	LVT	F	LS	S	TTL	AC	ACT	OTHER
D. How Drivers		00	'8240	+	~								
Buffers/Drivers	8	3S	'8244	+	~								
Transaciones	8	38	'8245	~	~								
Transceivers	18	3S	'18245	V		~							
Transparent Latches	8	38	'8373	+	~								
Flip-Flops	. 8	38	'8374	+	V								
			'8543										
	8	38	'8646	~									
	*	35	'8652	~		-							
Desistand Transactivers			'8952	V									
Registered Transceivers			'18502	~		~							
	18	38	'18646	~		~							
			'18652	~		~							
·	20	38	'18504	~		~							
Test Bus Controllers		38	'8990									V	

FLIP-FLOPS AND LATCHES

Flip-Flops

PECODIPTION	OUTDUT	TVDE									T'	ECHNOL	LOGY								
DESCRIPTION	OUTPUT	TYPE	ABT	BCT	LVT	ALS	AS	F	LS	S	ΠL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	OTHER
		'109				~	~	~	~								~				
Dual J-K Edge Triggered		'112				~		1	~	~							V			+	+CDC
Luge mygereu		'113				~															
Dual D-Type		'74				~	~	V	~	V	~	1.	V.	~	~		~	~	~	~	
Dual 4 Bit D-Type	00	'874				~	~														
Edge Triggered	3S	'876				~	~														
Quad D-Type		'175				~	~	V	V	~	~						V				
		'174				1	V	V	V	V							V		V		
Hex D-Type		'378						1													

[✔] Product available in technology indicated

Product available in reduced-noise advanced CMOS (11000 series)

⁺ New product planned in technology indicated

Flip-Flops (Continued)

DESCRIPTION	ОИТРИТ	TYPE									T	ECHNOL	.OGY								
DESCRIPTION	JUIFUI	IIFE	ABT	ВСТ	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	нс	HCT	LV	LVC	OTHE
Octal D-Type	38	'374	~	~		~	~	~	~	~		V•	V•	+	+		~	~	~	~	
True Data	33	'574	~		~	~	~	~				~	~	~	~		~	~	1	~	
Octal D-Type		'273	~		~	~			~								~	~	~		
True Data	38	'575				~	~														
With Clear	00	'874				~	~														
Octal D-Type True Data With Clock Enable	-	'377	,					,,	~									v ,			
		'534	~			~						V	~				~				
Octal D-Type Inverting	38	'564				~						~	~								
mirciang		'576				~	1											· ·			
Octal Dual Ranked True Data	38	'4374					-														
Octal Inverting With Clear	38	'577				~															
Octal Inverting With Preset	38	'876				v	~														
Octal True Data	38	'825					~														
9 Bit True Data	38	'823	~				~													~	
9 bit True Data	35	'29823		~																	
10 Bit Noninverting	3S	'16820														~					
10 Bit True Data	38	'821	~				~													+	
TO DIL TIUE Dala	30	'29821		~		~															
16 Bit Noninverting	3S	'16374	~		~							~	~			1				1	
18 Bit Noninverting	38	'16823	~									~	V			~					
20 Bit Noninverting	38	'16721														~					
20 Dit Normiverang	35	'16821	~										"			~			L		
20 Bit Noninverting With GTL I/O Levels	OD	'16921																			+GTL

[✔] Product available in technology indicated

 Product available in reduced-noise advanced CMOS (11000 series)
 → New product planned in technology indicated

FLIP-FLOPS AND LATCHES

Latches

DESCRIPTION	NO. OF	ОИТРИТ	TYPE									1	TECHNO	DLOGY								
DESCRIPTION	BITS	OUIPUI	IIFE	ABT	вст	LVT	ALS	AS	F	LS	s	ΠL	AC	ACT	AHC	AHCT	ALVC	нс	нст	LV	LVC	OTHER
D-Type Edge Triggered Inverting and Noninverting	8	3S	'996				~															
D-Type Transparent	8	3 S	'990				~															
Readback Latch,	9	3 S	'992				~															
True	10	38	'994				~															
D-Type Transparent With Clear, True Outputs	8	38	'666				v															
D-Type Transparent With Clear, Inverting Outputs	8	3 S	'667				v															
	8	38	'373	~	~	,	V	~	V	~	V		٧.	V.	+	+		~	~	~	~	
D-Type Transparent True	°	35	'573	V		~	~	~	~				V	V	~	~		~	~	~	~	
Transparent True	16	3 S	'16373	V		V							V	V			V				V	
D-Type Dual 4 Bit Transparent True	8	3 S	'873				V	~														
D-Type			'533	~			~	~					V	V								
Transparent	8	3 S	'563				~						V	V				~				
Inverting			'580				~															
Addressable	8	28	259				~			~								~				
	8	3 S	'845				~															
	9	3S	'843	~			~														+	
	9	33	29843		~																	
D-Type True Inputs	10	3 S	'841	~			~														~	
	10	30	29841		~		~															
	18	3 S	'16843	+										Ĺ			~					
	20	3 S	'16841	~										~			~					
D-Type Inverting Inputs	10	3 S	'842				~															

[✔] Product available in technology indicated

[•] Product available in reduced-noise advanced CMOS (11000 series)

⁺ New product planned in technology indicated

REGISTERS

Shift Registers

DESCRIPTION	NO. OF	ОИТРИТ	TYPE	TECHNOLOGY														
DESCRIPTION	BITS		IIFE	ABT	ВСТ	LVT	ALS	AS	F	LS	S	TTL	AHC	AHCT	HC	HCT	LV	
	4		'194					~		~	~							
Parallel In, Parallel Out, Bidirectional	8		'299				~		~	~	~							
	"		'323				~			~								
Parallel In, Parallel Out	4		'195							~	~							
Serial In, Parallel Out	8		'164				~			~					~		~	
Parallel In, Serial Out	8		'165				~			~					~			
Parallel In, Senai Out	•		'166				~			~					~			
Control to Described Control of the	8	38	'594				1			~					~			
Serial In, Parallel Out With Output Latches	°	33	'595							~					~			
	8	38	'299				~		4	~	~							
Noninverting	9	38	'29823		~													

Register Files

DESCRIPTION	оитрит	TYPE		TECHNOLOGY													
DESCRIPTION			ABT	BCT	LVT	ALS	AS	F	LS	S	ΠL	AC	ACT				
Dual 16 Word × 4 Bits	38	'870				~											

[✔] Product available in technology indicated

[•] Product available in reduced-noise advanced CMOS (11000 series)

⁺ New product planned in technology indicated

COUNTERS

Synchronous Counters – Positive Edge Triggered

DECODIDETON	PARALLEL LOAD	TYPE						TE	CHNOLO	GY					
DESCRIPTION		ITPE	ABT	ВСТ	LVT	ALS	AS	F	LS	S	ΠL	AHC	AHCT	нс	HCT
4 Bit Decade Up/Down	Sync	'568				~									
	Sync	'161				~	~	~	~					~	
4 Bit Binary		'163				~	~	~	~	~				~	
		'561				~									
		'169				~	~	~	~	~					
4 Dit Dinon Ho/Down		'569				~									
4 Bit Binary Up/Down	Sync	'191				~			~					V	
		'193				~			~		~			~	
o Dia Ha/Davia	Sync Clear	'869				~	~								
8 Bit Up/Down	Async Clear	'867				~	~								

Asynchronous Counters (Ripple Clock) – Negative Edge Triggered

DESCRIPTION	PARALLEL	TYPE	TECHNOLOGY														
DESCRIPTION	LOAD	IIFE	ABT	BCT	LVT	ALS	AS	F	LS	S	TTL	AHC	AHCT	HC	HCT		
Dual 4 Bit Binary	None	'393				-			~					~			
12 Bit Binary	Async	'4040												~			
14 Dit Dinon	A	'4020												~			
14 Bit Binary	Async	'4060												~			

8-Bit Binary Counters With Registers

DESCRIPTION	PARALLEL LOAD	ТҮРЕ	TECHNOLOGY														
DESCRIPTION			ABT	ВСТ	LVT	ALS	AS	F	LS	S	TTL	AHC	AHCT	HC	нст		
Parallel Register Outputs	38	'590							~					V			
Parallel Register Inputs	3S	'593							~								

[✔] Product available in technology indicated

Product available in reduced-noise advanced CMOS (11000 series)

⁺ New product planned in technology indicated

DECODERS, ENCODERS, DATA SELECTORS/MULTIPLEXERS

Encoders/Data Selectors/Multiplexers

DESCRIPTION	ОИТРИТ	TYPE									TECH	NOLOG	Υ							
DESCRIPTION	OUIPUI	ITPE	ABT	BCT	LVT	ALS	AS	F	LS	S	ΠL	AC	ACT	AHC	AHCT	ALVC	НС	HCT	LV	LVC
		'157				V	V	~	~	V	~			+	+		V	~		~
		'158				V	>	V	V	V				+	+		V			
Quad 2-to-1		298					~		~											
	3S	'257				~	~	~	~	~			•	+	+		V	~		~
	33	'258				~	>	~	~					+	+					
Hex 2-to-1 Universal Multiplexers	38	'857				~														
		'153				~	~	~	~	~							~			
Dual 4-to-1	3S	'253				~	١	~	~								~			
	33	'353					1													
4-to-1 Registered Transceivers	38	'16460	1																	
Cascadable Octals		'148							1		~						١			
8-to-1		'151				~	~	~	~	~							~			
8-10-1	3S	'251				~		~	~	~							~			
16-to-1	3S	'250					~													
12-to-24 Multiplexed D-Type Latches	3S	'16260	~													~				
12-to-24 Registered Bus Exchangers 3S	20	'16269														~				
	35	'16270						,								~				

Decoders/Demultiplexers

DESCRIPTION	ОИТРИТ	TYPE								TECH	HNOLOG	iΥ						
DESCRIPTION	OUIPUI	ITPE	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	НСТ	LV	LVC	OTHER
		'131		~														
Dual 2-to-4		'139	V			V	~		•	•	+	+		~	~			
	oc	'156	~			V		~										
Dual 2-to-4 for Battery Backed-Up Memories		2414																
3-to-8		'138	~	~	~	~	~		•		+	+		~	~	~	~	
3-to-8 With Address Registers		'137	~	~		V											+	
4-to-10 BCD-to-Decimal		'42				V			-					~				

[✔] Product available in technology indicated

[•] Product available in reduced-noise advanced CMOS (11000 series)

⁺ New product planned in technology indicated

COMPARATORS AND PARITY GENERATORS/CHECKERS

Comparators

			DESC	RIPTION				7/05				TECHN	OLOGY			
INPUT	P=Q	P=Q	P>Q	P>Q	P <q< th=""><th>OUTPUT</th><th>ENABLE</th><th>TYPE</th><th>ALS</th><th>AS</th><th>F</th><th>LS</th><th>AC</th><th>ACT</th><th>HC</th><th>HCT</th></q<>	OUTPUT	ENABLE	TYPE	ALS	AS	F	LS	AC	ACT	HC	HCT
8 Bit With 20-kΩ	No	Yes	No	No	No	28	Yes	'520	V				•			
Pullup	No	Yes	No	Yes	No	28	No	'682				~			~	
	No	Yes	Nọ	No	No	28	Yes	'521	~		~					
8 Bit Standard	No	Yes	No	Yes	No	28	No	'684				~			~	
Otalidaid	No	Yes	No	No	No	28	Yes	'688	~			~			~	
8 Bit Latched P	No	No	Yes	No	Yes	28	Yes	'885		V						

Parity Generators/Checkers

DESCRIPTION	NO. OF	TYPE					TECHN	OLOGY				
DESCRIPTION	BITS	IIFE	ALS	AS	F	LS	S	ΠL	AC	ACT	HC	HCT
Odd/Even	_	280	~	~	~	~	~					
	9	286		~						•		

[✔] Product available in technology indicated

Product available in reduced-noise advanced CMOS (11000 series)

⁺ New product planned in technology indicated

1-32

BUS SWITCHES AND 5-V/3-V VOLTAGE TRANSLATORS

Bus Switches

DECORPTION	TVDF		TECH	NOLOGY	
DESCRIPTION	TYPE	CBT	CBTS	CBTD	OTHER
Quad Bus Switches	'3125	~			
Dual 4-Bit Bus Switches With '244 Pinout	'3244	·			
8-Bit Bus Switches With '245 Pinout	'3245	~			~
Quad 2-to-1-Bit FET Multiplexers/Demultiplexers	'3257	~			
Dual Bus Switches	'3306	~	~	~	
8-Bit Bus Switches	'3345	~			
10-Bit Bus-Exchange Switches	'3383	~			
Dual 5-Bit Bus Switches	'3384	V	~	~	
10 Bit With Precharged Outputs for Live Insertion	'6800	~			
18-Bit Bus-Exchange Switches	'16209	~			
	'16211	~			
24-Bit Bus-Exchange Switches	'16212	V			
	'16213	~			
12-Bit 3-to-1 Bus Select	'16214	v .			`
Synchronous 16-Bit-to-32-Bit FET Multiplexers	'16232	V			
16-Bit-to-32-Bit FET Multiplexers/Demultiplexers	'16233	~			

ARITHMETIC CIRCUITS

Parallel Binary Adders

DESCRIPTION	OUTPUT	TYPE						TECHN	OLOGY					
DESCRIPTION	COIPUI	ITPE	ALS	AS	F	LS	S	TTL	HC	HCT	AC	ACT	LV	LVC
4 Bit		'283			>	~	>							

Arithmetic Logic Units

DESCRIPTION	OUTPUT	TYPE						TECHN	OLOGY					
DESCRIPTION	OUIFUI	ITPE	ALS	AS	F	LS	S	ΠL	НС	HCT	AC	ACT	LV	LVC
4-Bit Arithmetic Logic Units: Function Generator		'181		~										

[✔] Product available in technology indicated

[•] Product available in reduced-noise advanced CMOS (11000 series)

⁺ New product planned in technology indicated

FUNCTIONAL INDEX

FIFO MEMORIES

First-In, First-Out (FIFO) Memories

DESCRIPTION	·	OUTPUT	TYPE	1					TECH	NOLOGY					
SIZE	TYPET	OUIPUI	ITPE	ABT	BCT	LVT	ALS	AS	F	LS	S	ΠL	AC	ACT	ALVC
16 Words × 4 Bits	U	3S	'232				~								
16 Words × 5 Bits		38	'225								~				
16 Words × 5 Bits	U	33	'233				~								
32 Words × 9 Bits	В	38	'2238				~								
64 Words × 4 Bits	U	3S	'234				~								
64 Words × 4 Bits	U		'236				~								
64 Words × 5 Bits	U	3S	'235				~								
64 Words × 8 Bits	U	38	'2232				~								
64 Words × 9 Bits	U	38	'2233				~								
64 Words × 18 Bits	U, C	3S	7813											~	~
b4 Words x 10 bits	U	38	'7814											~	~
	B, C	38	'3612	~											
64 Words × 36 Bits	B , O	33	'3614	~											
04 Words x 30 Dits	U, C	38	'3611	~											
	0,0	30	'3613	~											
Dual 64×1	С	38	'2226											~	
Dual 04 X I		35	'2227											V	
Dual 256 × 1	С	38	'2228				'							~	
Dual 200 X 1		35	'2229											V	
256 Words × 9 Bits	U	38	'7200L											~	
256 Words × 18 Bits	U, C	38	'7805											~	
200 WUIUS X 10 DILS	U	38	'7806											~	V
256 × 36 × 2 Bits	B, C	3S	'3622											~	
512 Words × 9 Bits	U	38	'7201LA	·						T		T		~	

[✔] Product available in technology indicated

 Product available in reduced-noise advanced CMOS (11000 series)

⁺ New product planned in technology indicated

[†]U = Unidirectional B = Bidirectional

C = Clocked

S = Synchronized

First-In, First-Out (FIFO) Memories (Continued)

DESCRIPTION		OUTDIT.	7/25						TECHN	OLOGY					
SIZE	TYPET	OUTPUT	TYPE	ABT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	ALVC
	U, C	38	'7803											~	~
512 Words × 18 Bits	U	38	'7804											~	~
512 WOIQS X TO DILS	B, C	38	'7819	>											
	В	38	'7820	~											
512 Words × 32 Bits	B, C	38	'3638											~	
512 Words × 36 Bits	U, C	38	'3631											~	
512 WOIOS X 30 DILS	B, C	38	'3632											~	
	В	38	'2235											~	
1K Words × 9 Bits		30	'2236											~	
	U	3S	'7202LA											1	
	U, C	38	'7811											~	
1K Words × 18 Bits	0,0	30	'7881											~	
	U	3 S	'7802											~	
1K Words × 36 Bits	U, C	38	'3641											~	
1K×36×2 Bits	B, C	3S	'3642											+	
	U, C	3 S	'7807											~	
2K Words × 9 Bits	U	38	'7203L											~	
		33	'7808											~	
2K Words × 18 Bits	U, C	38	'7882											~	
2K Words × 36 Bits	U, C	3S	'3651			,								+	
4K Words × 9 Bits	U	38	'7204L											~	
4K Words × 18 Bits	U, C	38	'7884											~	

[✔] Product available in technology indicated

[•] Product available in reduced-noise advanced CMOS (11000 series)

⁺ New product planned in technology indicated

[†] U = Unidirectional

B = Bidirectional

C = Clocked

S = Synchronized

CLOCK-DISTRIBUTION CIRCUITS

3.3-V Clock-Distribution Circuits (CDC)

DESCRIPTION	VO LEVELS	TYPE		TECHN	IOLOGY	
DESCRIPTION	VOLEVELS	ITPE	AS	AC	ACT	ABT
3.3-V Hex Inverting Clock Drivers/Buffers	CMOS/CMOS	'203		~		
1-to-9 Differential LVPECL Buffers	LVPECL/LVPECL	'111				+
1-to-9 Differential LVPECL Buffers With Output Enable	LVPECL/LVPECL	'112				+
1-to-10 Buffers With Output Enable	TTL/TTL	'351				~
1-to-10 bullets with Output Enable	TIDITE	'2351				~
1-to-6 PLL Clock Drivers	TTL/TTL	'536				+
I-to-o PLL Clock Drivers	110116	'2536				+
	TTL/TTL	'586				~
1-to-12 PLL Clock Drivers	110/112	'2586				~
1-to-12 FLL Clock Drivers	LVPECL/TTL	'582				+
	LVPECDITE	'2582				+
Phase-Locked-Loop 1-to-16 Clock Drivers	SSTL/TTL	'587				+
Filase-Locked-Loop 1-to-10 Clock Dilvers	3310111	'2587				+
		'9841				V
P5 Motherboard Clock Synthesizers/Drivers	TTL/TTL	'9842				~
		'9843				~
P6 Motherboard Clock Synthesizers/Drivers	TTL/TTL	'916				+
PC Motherboard Clock Generators With Dual 1-to-4 Buffers	TTL/TTL	'913				+

FUNCTIONAL INDEX

[✔] Product available in technology indicated

 Product available in reduced-noise advanced CMOS (11000 series)

⁺ New product planned in technology indicated

5-V Clock-Distribution Circuits (CDC)

DESCRIPTION	VO LEVELS	TYPE		TECHI	NOLOGY	
DESCRIPTION	NO LEVELS	TYPE	AS	AC	ACT	ABT
Hay by codes	CMOSICMOS	204		~		
Hex Inverters	CMOS/CMOS	204-7		~		
1-to-6 Exclusive ORs	TTL/ITL	'328				V
1-to-6 Exclusive Ons	TTL/CMOS	'329				V .
4 to C Fushing ODs With Order & Esphia	TTL/ITL	'391				V
1-to-6 Exclusive ORs With Output Enable	TTL/CMOS	'392		-		>
	TTL/CMOS	208			~	
Dual 4 to 4 Buffers (Gianuta Gautanta)	TILIOMOS	208-7			~	
Dual 1-to-4 Buffers (2 inputs, 8 outputs)	CMOS/CMOS	209		V		
	CIMOS/CIMOS	209-7		V		
1-to-8 Divide-by-2 Flip-Flops (6 inverting, 2 noninverting)	TTL/TTL	'303	V			
1-to-8 Divide-by-2 Flip-Flops (8 noninverting)	TTL/TTL	'304	~			
1-to-8 Divide-by-2 Flip-Flops (4 inverting, 4 noninverting)	TTL/ITL	'305	~			
4 to 0 Ferrote (4 perimunities huffers 4 divide by 0 flip flore)	TTL/CMOS	'337				~
1-to-8 Fanouts (4 noninverting buffers, 4 divide-by-2 flip-flops)	TTL/TTL	'339				~
1-to-8 NANDs	TTL/ITL	'340			-	V
1-to-8 ANDs	TTL/TTL	'341				~
3-Way Fanout Buffers (dual 1-to-3 noninverting buffers, 1-to-4 divide-by-2 flip-flops)	TTL/TTL	'330				~

Product available in technology indicated.

[•] Product available in reduced-noise advanced CMOS (11000 series)

⁺ New product planned in technology indicated

General Information	11
ALB Widebus™	2
ALVC Widebus™	3
LVT Octals	4
LVTZ Octals: Power Up and 3 State	5
LVT Widebus™	6 ·
LVT JTAG/IEEE 1149.1	7
LVC MSI and Octals	8
LVC Widebus™	9
LV MSI and Octals	10
GTL Transceivers and Backplane Drivers	11
Application Reports	12
Characteristics Information	13
Mechanical Data	14

Contents

		Page
SN74ALB16244	16-Bit Buffer/Driver With 3-State Outputs	 2-3

 State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V 		DL PACK P VIEW)	AGE
Operation	1 0E [1	\mathcal{O}_{ω}	2 <u>0E</u>
 Members of the Texas Instruments Widebus™ Family 	1Y1 []2	47	[] 1A1
 Fastest Buffer/Driver: 2 ns Maximum Input to Output Time Delay 	1Y2 [] 3 GND [] 4	45	1A2 GND
Schottky Diodes on All Inputs to Eliminate	1Y3 []5 1Y4 []6		1A3 1A4
Overshoot and Undershoot	V _{CC} []7	42	v _{cc}
● Industry Standard '16244 Pinout	2Y1 🛮 8] 2A1
 Distributed V_{CC} and GND Pin Configuration 	2Y2 🛮 9	40	2A2
Minimizes High-Speed Switching Noise	GND [] 10	0 39	GND
Flow-Through Architecture Optimizes	2Y3 🛚 1	1 38	2A3
PCB Layout	2Y4 🛚 1:		2A4
Package Options Include Plastic 300-mil	3Y1 🛚 1		3A1
Shrink Small-Outline (DL) and Thin Shrink	3Y2 🛚 1		3A2
Small-Outline (DGG) Packages	GND [] 1		GND
(, 3	3Y3 🛚 1		3A3
description	3Y4 [] 1		3A4
The ONITABLE DAGGAA AG INTER Was and Para Albara	V _{CC} [] 1		V _{CC}
The SN74ALB16244 16-bit buffer and line driver	4Y1 [] 1		4A1
is designed for high-speed, low-voltage (3.3-V)	4Y2 2		4A2
V _{CC} operation. This device is intended to replace the conventional driver in any speed-critical path.	GND [] 2 4Y3 [] 2		GND
The propagation delay from input to output is 2 ns	4Y3 U2] 4A3] 4A4
maximum. The small propagation delay is	474 U2 40E U2		_
achieved using a unity gain amplifier on the input	405 42	4 20	30E
and feedback resistors from input to output,			

which allows the output to track the input with a small offset voltage (Voff). The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and symmetrical active-low output-enable (OE) inputs.

The SN74ALB16244 is characterized for operation from -40°C to 85°C.

applications

The SN74ALB16244 is particularly suitable for driving the system bus, which requires external drivers due to high capacitive loading caused by address multiplexing. The 25-mA drive capability and 2-ns delay is ideal for this application.

The SN74ALB16244 is ideal in cache memory (SRAM) or main memory (DRAM and EDO DRAM) interface; it can also be used in high-speed graphics and multimedia applications.

FUNCTION TABLE (each buffer)

INPL	JTS	OUTPUT
ŌĒ	Α	, Y
L	Н	Н
L	L	L
Н	Х	Z

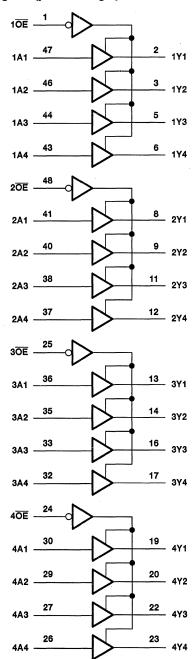
Widebus is a trademark of Texas Instruments Incorporated



SCBS647 - AUGUST 1995 logic symbol†

10E EN₁ 48 2OE EN2 25 3OE EN3 24 4OE EN4 47 2 1 🗸 1Y1 1A1 3 46 1A2 1Y2 44 5 1A3 1Y3 43 6 1A4 1Y4 8 41 2∇ 2A1 2Y1 40 2A2 2Y2 38 11 2A3 2Y3 37 12 2A4 2Y4 36 13 3A1 3 ▽ 3Y1 35 14 3A2 3Y2 33 16 **3Y3** 3A3 32 17 3Y4 3A4 30 19 4 ▽ 4A1 1 4Y1 29 20 4A2 **4Y2** 27 22 4A3 4Y3 26 23 4A4 **4Y4**

logic diagram (positive logic)



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V ₁ : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{ K }(V_1 < 0)$	
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	± 50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	± 50 mA
Continuous current through each V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	
DL package	1.4 W
Storage temperature range, T _{stg}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. The input and output positive-voltage ratings may be exceeded up to 4.6 V if the input and output clamp-current ratings are observed.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		3	3.6	٧
V _{IH} ‡	High-level input voltage		2.2		٧
V _{IL} ‡	Low-level input voltage			0.6	٧
ЮН	High-level output current	9		-25	mA
loL	Low-level output current			25	mA ,
Δt/Δν	Input transition rise or fall rate	Outputs enabled		5	ns/V
TA	Operating free-air temperature		-40	85	°C

[‡] The outputs are warranted to be TTL compatible.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
VIK	V _{CC} = 3 V,	l _l = −18 mA				-1.2	٧
+	V _{CC} = 3 V	I _{OH} = 0		V _I -0.2			V
V _{OH} ‡	ACC = 2 A	I _{OH} = -25 mA		2			· ·
V +	V _{CC} = 3 V	I _{OL} = 0 mA			,	V _I +0.2	V
V _{OL} ‡	VCC = 2 V	I _{OL} = 25 mA				V _I +0.2) ^v
		V _I = V _{CC} or GND	Control inputs			±10	μΑ
lį	V _{CC} = 3.6 V	VI = VCC	Data pins			1	mA
		V _I = 0	Data pilis			-1.5	1117
^I OZH	$V_{CC} = 3.6 \text{ V},$	V _O = 3 V)		20	μА
lozl_	V _{CC} = 3.6 V,	V _O = 0.5 V				-20	μА
lcc	V _{CC} = 3.6 V,	i _O = 0,	Outputs high		5	9	mA
(per buffer)	V _I = V _{CC} or GND		Outputs low		5	9	ША
lcc	Entire device in the high-imped	Entire device in the high-impedance state				0.8	mA
ΔICC§	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or GND	One input at V _{CC} -0.6 V,				750	μА
Ci	V _I = 3 V or 0				4		pF
Co	V _O = 3 V or 0		7 13 10 10 10 10 10 10 10 10 10 10 10 10 10		10		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted)

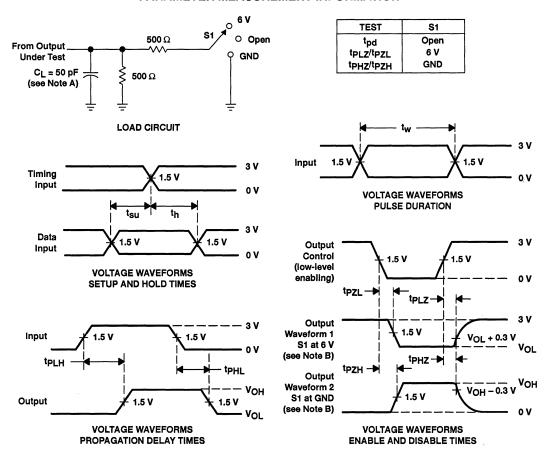
PARAMETER	FROM (INPUT)	1		V _{CC} = 3.3 V ± 0.3 V	UNIT
	(INPOT)	(OUTPUT)	MIN MAX	MIN TYPT MA	7
^t pd	A	Y			2 ns
^t en	ŌĒ	Υ			3
^t dis	ŌĒ	Υ.			ns 3

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] Limits are valid only if the buffer is in the linear region. In the nonlinear region, the output transistors are clamped at the output voltage margins.

^{\$} This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

General Information	1
ALB Widebus™	2
ALVC Widebus™	3
LVT Octals	4
LVTZ Octals: Power Up and 3 State	5
LVT Widebus™	6
LVT JTAG/IEEE 1149.1	7
LVC MSI and Octals	8
LVC Widebus™	9
LV MSI and Octals	10
GTL Transceivers and Backplane Drivers	11
Application Reports	12
Characteristics Information	13
Mechanical Data	14

Contents

		. ugc
SN74ALVCH16240	16-Bit Buffer/Driver With 3-State Outputs	3-3
SN74ALVCH16244	16-Bit Buffer/Driver With 3-State Outputs	3-9
SN74ALVCH16245	16-Bit Bus Transceiver With 3-State Outputs	3-15
SN74ALVC164245	16-Bit 3.3-V to 5-V Level Shifting Transceiver With 3-State Outputs	3-21
SN74ALVCH16260	12-Bit to 24-Bit Multiplexed D-Type Latch With 3-State Outputs	3-29
SN74ALVCH162268	12-Bit to 24-Bit Registered Bus Exchanger With 3-State Outputs	3-37
SN74ALVCH16269	12-Bit to 24-Bit Registered Bus Transceiver With 3-State Outputs	3-45
SN74ALVCHR162269	12-Bit to 24-Bit Registered Bus Exchanger With 3-State Outputs	3-53
SN74ALVCH16270	12-Bit to 24-Bit Registered Bus Exchanger With 3-State Outputs	3-61
SN74ALVCH16271	12-Bit to 24-Bit Multiplexed Bus Exchanger With 3-State Outputs	3-69
SN74ALVCH16272	12-Bit to 24-Bit Multiplexed Bus Exchanger With 3-State Outputs	3-73
SN74ALVCH16344	1-to-4 Address Driver With 3-State Outputs	3-79
SN74ALVCH16373	16-Bit Transparent D-Type Latch With 3-State Outputs	3-85
SN74ALVCH16374	16-Bit Edge-Triggered D-Type Flip-Flop With 3-State Outputs	3-93
SN74ALVCH16409	9-Bit, 4-Port Universal Bus Exchanger With 3-State Outputs	3-101
SN74ALVCHR162409	9-Bit, 4-Port Universal Bus Exchanger With 3-State Outputs	3-109
SN74ALVCH16500	18-Bit Universal Bus Transceiver With 3-State Outputs	3-117
SN74ALVCH16501	18-Bit Universal Bus Transceiver With 3-State Outputs	3-123
SN74ALVCH16525	18-Bit Registered Bus Transceiver With 3-State Outputs	3-131
SN74ALVCH162525	18-Bit Registered Bus Transceiver With 3-State Outputs	3-139
SN74ALVCH16543	18-Bit Registered Bus Transceiver With 3-State Outputs	3-147
SN74ALVCH16600	18-Bit Universal Bus Transceiver With 3-State Outputs	3-153
SN74ALVCH16601	18-Bit Universal Bus Transceiver With 3-State Outputs	3-161
SN74ALVCH162601	18-Bit Universal Bus Transceiver With 3-State Outputs	3-169
SN74ALVCH16646	16-Bit Bus Transceiver and Register With 3-State Outputs	3-177
SN74ALVCH16652	16-Bit Bus Transceiver and Register With 3-State Outputs	3-185
SN74ALVCH16721	3.3-V 20-Bit Flip-Flop With 3-State Outputs	3-193
SN74ALVCH16820	3.3-V 10-Bit Flip-Flop With Dual Outputs	3-199
SN74ALVCH162820	3.3-V 10-Bit Flip-Flop With Dual Outputs and 3-State Outputs	3-205
SN74ALVCH16821	3.3-V 20-Bit Bus-Interface Flip-Flop With 3-State Outputs	3-213
SN74ALVCH16823	18-Bit Bus-Interface Flip-Flop With 3-State Outputs	3-221
SN74ALVCH16825	18-Bit Buffer/Driver With 3-State Outputs	3-231
SN74ALVCH16827	20-Bit Buffer/Driver With 3-State Outputs	3-237
SN74ALVCH162827	20-Bit Buffer/Driver With 3-State Outputs	3-243
SN74ALVCH16835	18-Bit Universal Bus Driver With 3-State Outputs	3-249
SN74ALVCH16841	20-Bit Bus-Interface D-Type Latch With 3-State Outputs	3-257
SN74ALVCH16843	18-Bit Bus-Interface D-Type Latch With 3-State Outputs	3-265
SN74ALVCH16901	18-Bit Universal Bus Transceiver With Parity Generators/Checkers	3-269
SN74ALVCH16952	16-Bit Registered Transceiver With 3-State Outputs	3-277

SCES045 - JULY 1995

 Member of the Texas Instruments Widebus™ Family 			L PACI VIEW)	KAGE
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	10E [1		2 <u>OE</u>
 ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, 	1Y1 [1Y2 [GND [1Y3 [3 4	46 45] 1A1] 1A2] GND] 1A3
R = 0) ■ Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17	1Y4 [V _{CC} [2Y1 [6 7	43 42	1 1A4] 1A4] V _{CC}] 2A1
 Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors 	2Y2 [GND [2Y3 [9 10	40 39	2A2 GND 2A3
 Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages 	2Y4 [3Y1 [3Y2 [12 13	37 36	2A4 3A1 3A2
description	GND [3Y3 [15 16	34 33	GND 3A3
This 16-bit buffer/driver is designed for 2.3-V to 3.6-V V_{CC} operation.	3Y4 [V _{CC} [4Y1 [18	31] 3A4] V _{CC}] 4A1
The SN74ALVCH16240 is designed specifically to improve both the performance and density of	4Y2 [GND [20	29	4A2 GND

The SN74ALVCH16240 is available in Tl's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

4Y3 [22

4Y4 **1**23 40E 1 24

25 T 3 OE

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16240 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 4-bit buffer)

INPUTS		OUTPUT		
ŌĒ	Α	Y		
L	H	L		
L	L	Н		
Н	Χ	Z		

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3-state memory address drivers, clock drivers,

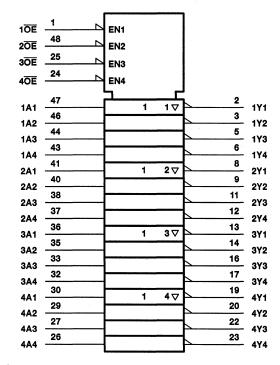
The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides inverting outputs and symmetrical active-low

and bus-oriented receivers and transmitters.

output-enable (OE) inputs.

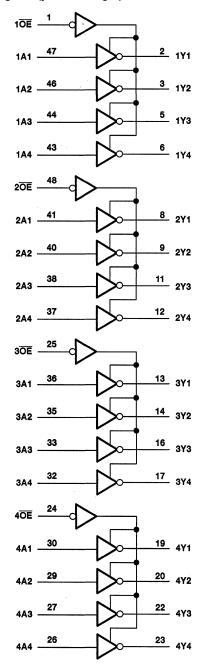
ISTRUMENTS

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{ K }(V_1 < 0)$	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, IO (VO = 0 to VCC)	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	je 0.85 W
DL package	1.2 W
Storage temperature range, T _{stg}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		2.3	3.6	٧
V	High level inner college	V _{CC} = 2.3 V to 2.7 V	1.7		٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V	Law layed input valtage	V _{CC} = 2.3 V to 2.7 V		0.7	٧
VIL	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	v
٧ _I	Input voltage		0	Vcc	٧
٧o	Output voltage		0	Vcc	٧
		V _{CC} = 2.3 V		-12	
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 2.3 V		12	
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SCES045 - JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CO	ONDITIONS	vcct	MIN	TYP‡	MAX	UNIT
		I _{OH} = -100 μA		MIN to MAX	VCC-C	.2		
		I _{OH} = -6 mA,	V _{IH} = 1.7 V	2.3 V	2			
			V _{IH} = 1.7 V	2.3 V	1.7			V
VOH		I _{OH} = -12 mA	V _{IH} = 2 V	2.7 V	2.2			V
			V _{IH} = 2 V	3 V	2.4			
		i _{OH} = -24 mA,	V _{IH} = 2 V	3 V	2		0.2 0.4 0.7 0.4 0.55 ±5 1500 ±10 40 750	
		I _{OL} = 100 μA		MIN to MAX			0.2	
v _{OL}		$I_{OL} = 6 \text{ mA},$	V _{IL} = 0.7 V	2.3 V			0.4	
		IOI = 12 mA	V _{IL} = 0.7 V	2.3 V			0.7	V
		IOC = 12 IIIA	V _{IL} = 0.8 V	2.7 V			0.4	
		I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V			0.55	
lį		V _I = V _{CC} or GND		3.6 V			±5	μА
		V _i = 0.7 V		2.3 V	45			
		V _i = 1.7 V	,	2.3 V	-45			
l(hold)		V _I = 0.8 V			75			μА
		V _I = 2 V		3 V	-75			
		V _I = 0 to 3.6 V		3.6 V			±500	
loz		VO = VCC or GND		3.6 V			±10	μА
Icc		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			40	μА
Δlcc		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА
C:	Control inputs	V. Vee or CND		221/		3		
Ci	Data inputs	VI = VCC or GND		3.3 V		6		pF
Со	Outputs	VO = VCC or GND		3.3 V		7		рF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	PARAMETER (INPUT) (OUTPUT)	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V V _{CC} = 3.3 V ± 0.3 V		UNIT	
		(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	
^t pd	, A	Υ	1	5.9		5.3	1	4.2	ns
^t en	ŌĒ	Y	1	6.9		6.1	1	5	ns
^t dis	ŌĒ	Υ	1.5	5.6		4.8	1	4.4	ns

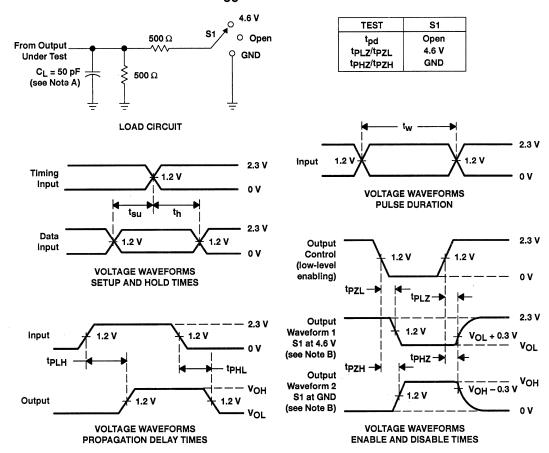
operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
			TYP	TYP		
Cpd	Power dissipation capacitance	Outputs enabled	Cı = 50 pF. f = 10 MHz	. 16	19	
Ора	rower dissipation capacitance	Outputs disabled	C _L = 50 pF, f = 10 MHz	4	5	pF

 $[\]ddagger$ Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

SCES045 - JULY 1995

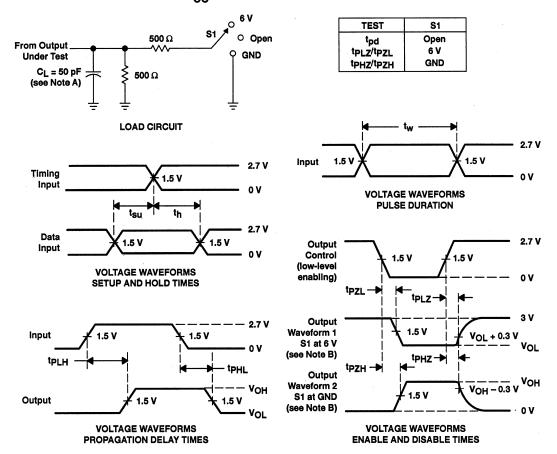
PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50$ Ω , $t_f \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tplz and tpHZ are the same as tdis.
 - F. tpy and tpyH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V } \pm 0.3 \text{ V}$



- NOTES: A. CL includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{\rm O}$ = 50 Ω , $t_{\rm f} \leq$ 2.5 ns, $t_{\rm f} \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

SCES014 - JULY 1995

 Member of the Texas Instruments Widebus™ Family 	DGG OR DL PACKAGE (TOP VIEW)
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	1 OE 1 48 2 OE
 ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0) 	1Y2
 Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17 	1Y4 [] 6 43 [] 1A4 V _{CC} [] 7 42 [] V _{CC} 2Y1 [] 8 41 [] 2A1
 Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors 	2Y2
 Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages 	2Y4
description	GND
This 16-bit buffer/driver is designed for 2.3-V to 3.6-V V_{CC} operation.	3Y4 [] 17 32 [] 3A4 V _{CC} [] 18 31 [] V _{CC} 4Y1 [] 19 30 [] 4A1
The SN74ALVCH16244 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.	4Y2
The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true	4 OE [24 25] 3 OE

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16244 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16244 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 4-bit buffer)

INP	JTS	OUTPUT
ŌĒ	Α	Y
L	Н	Н
L	L	L
Н	Х	Z

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outputs and symmetrical active-low output-

enable (OE) inputs.



SN74ALVCH16244 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

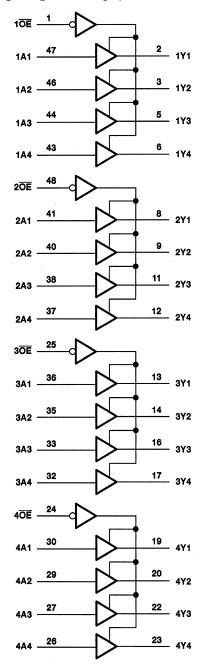
SCES014 - JULY 1995

logic symbol†

10E 20E 30E 40E	1 A8 A 25 A	EN1 EN2 EN3 EN4		,		
1A1	47	广	1	1 ▽	2	1Y1
1A2	46				3	1Y2
1A3	44		,		5	1Y3
1A4	43				6	1Y4
	41		1	2▽	8	
2A1	40			- Z V	. 9	2Y1
2A2	38				11	2Y2
2A3	37	 			12	2Y3
2A4	36				13	2Y4
3A1	35		1	3 ▽	14	3Y1
3A2	33				16	3Y2
3A3	32	·			17	3Y3
3A4	30	<u> </u>			19	3Y4
4A1	29	<u> </u>	1	4 ▽	20	4Y1
4A2	27				22	4Y2
4A3	26	<u> </u>			23	4Y3
4A4						4Y4

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SCES014 - JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Cupality voltage vange V	051/+0461/
Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	–0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{ K }(V_1 < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	e 0.85 W
DL package	1.2 W
Storage temperature range, T _{sto}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book. literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	V
V	Lieb level input veltage	V _{CC} = 2.3 V to 2.7 V	1.7		V
VIH	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		\ \
\/	Law level input veltage	V _{CC} = 2.3 V to 2.7 V		0.7	V
VIL	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	'
۷į	Input voltage		0	Vcc	V
Vo	Output voltage		0	VCC	V
		V _{CC} = 2.3 V		-12	
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 2.3 V		12	
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA
	V _{CC} = 3 V			24	
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TΑ	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN74ALVCH16244 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS SCES014 - JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P/	ARAMETER	TEST CO	ONDITIONS	vcct	MIN	TYP‡	MAX	UNIT
		I _{OH} = -100 μA		MIN to MAX	VCC-C).2		
		$I_{OH} = -6 \text{ mA},$	V _{IH} = 1.7 V	2.3 V	2			
$VOH \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$			v					
vон		I _{OH} = -12 mA	V _{IH} = 2 V	2.7 V	2.2			v
			V _{IH} = 2 V	3 V	2.4			
		I _{OH} = -24 mA,	V _{IH} = 2 V	3 V	2			
		I _{OL} = 100 μA		MIN to MAX			0.2	
		IOL = 6 mA,	V _{IL} = 0.7 V	2.3 V			0.4	
V _{OL}		l 10 mA	V _{IL} '= 0.7 V	2.3 V			0.7	V
	,	IOL = 12 MA	V _{IL} = 0.8 V	2.7 V			0.4	
		I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V			0.55	
l _I		V _I = V _{CC} or GND		3.6 V			±5	μА
		V _I = 0.7 V		0.21/	45			
		V _I = 1.7 V		2.3 V	-45			
I(hold)		V _I = 0.8 V		2.1/	75			μА
		V _I = 2 V		3 V	-75			
		V _I = 0 to 3.6 V	,	3.6 V			±500	
loz		VO = VCC or GND		3.6 V			±10	μA
		V _I = V _{CC} or GND,	IO = 0	3.6 V			40	μА
Δlcc		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА
	Control inputs	V. Voc or GND		3.3 V		3		nE
Cį	Data inputs	V _I = V _{CC} or GND		3.3 V		6		pF
Со	Outputs	VO = VCC or GND		3.3 V		7		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	PARAMETER FROM TO (OUTPUT)	V _{CC} =	2.5 V 2 V	V _{CC} = 2.7 V V _{CC} = 3.3 V ± 0.3 V			UNIT		
	(INPOT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	1	5		4	1	3.6	ns
t _{en}	ŌĒ	Υ	1	6.8		6	1	5	ns
^t dis	ŌĒ	Y	1	6		5.2	1	5	ns

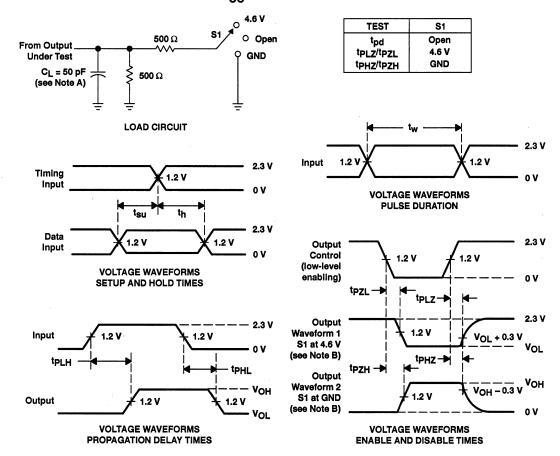
operating characteristics, T_A = 25°C

	PARAMETER		TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
			TYP			
C .	Power dissipation capacitance	Outputs enabled	C ₁ = 50 pF, f = 10 MHz	16	19	pF
C _{pd}	- ower dissipation capacitance	Outputs disabled	OL = 50 pr, 1 = 10 MHZ	4	5	pr _.

[‡] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

SCES014 - JULY 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

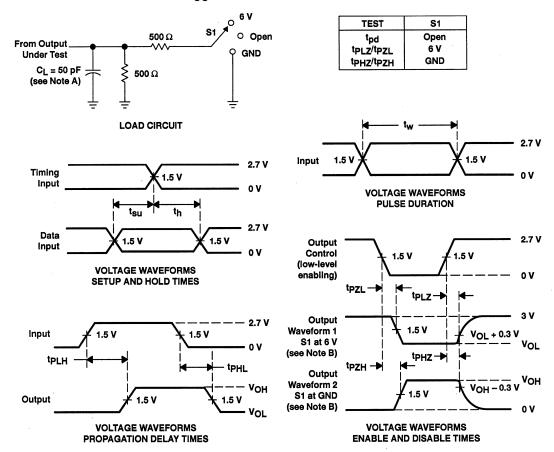


- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_f ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpl H and tpHI are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SCES014 - JULY 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{\rm O} = 50 \,\Omega$, $t_{\rm f} \leq$ 2.5 ns, $t_{\rm f} \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

SCES015 - JULY 1995

 Member of the Texas Instruments Widebus™ Family 	DGG OR DL (TOP \	
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	1DIR 1	48 1 0E
 ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0) Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17 	1B1 U 2 1B2 U 3 GND U 4 1B3 U 5 1B4 U 6 V _{CC} U 7	47 1 1A1 46 1 1A2 45 1 GND 44 1 1A3 43 1 1A4 42 1 V _{CC}
 Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages 	1B5 U 8 1B6 U 9 GND U 10 1B7 U 11 1B8 U 12 2B1 U 13 2B2 U 14 GND U 15	41] 1A5 40] 1A6 39] GND 38] 1A7 37] 1A8 36] 2A1 35] 2A2 34] GND
description	2B3 🛚 16	33 2A3
This 16-bit (dual-octal) noninverting bus transceiver is designed for 2.3-V to 3.6-V $V_{\hbox{\scriptsize CC}}$ operation.	2B4 17 V _{CC} 18 2B5 19 2B6 20	32 2 2A4 31 2V _{CC} 30 2A5 29 2A6
The SN74ALVCH16245 is designed for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.	2B0	28 GND 27 2A7 26 2A8 25 2OE

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data

transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16245 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16245 is characterized for operation from -40°C to 85°C.

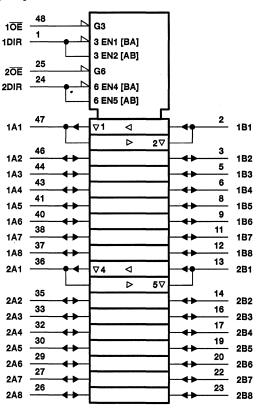
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FUNCTION TABLE (each 8-bit section)

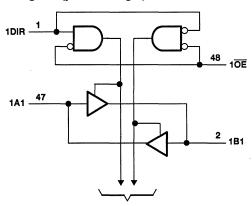
INPUTS		OPERATION
ŌĒ	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	Х	Isolation

logic symbol†

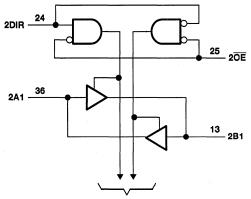


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels



To Seven Other Channels

SCES015 - JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-0.5 V to 4.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)	-0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	
Output voltage range, VO (see Notes 1 and 2)	V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	0.85 W
DL package	1.2 W
Storage temperature range, T _{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	V
V	V _{CC} = 2.3 V to 2.7 V		1.7		V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
1/	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V		0.7	V
VIL	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	v
VI	Input voltage		0	VCC	٧
٧o	Output voltage		0	VCC	٧
	High-level output current	V _{CC} = 2.3 V		-12	
ЮН		$V_{CC} = 2.7 \text{ V}$	-1		mA
		V _{CC} = 3 V	i i	-24	
		V _{CC} = 2.3 V		12	
lol	Low-level output current	V _{CC} = 2.7 V	12		mA
		V _{CC} = 3 V		24	
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN74ALVCH16245 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES015 - JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER	TEST CO	vcct	MIN	TYP‡	MAX	UNIT		
		I _{OH} = -100 μA		MIN to MAX	VCC-C	.2			
		I _{OH} = -6 mA,	V _{IH} = 1.7 V	2.3 V	2				
			V _{IH} = 1.7 V	2.3 V	1.7			v	
VOH		I _{OH} = -12 mA	V _{IH} = 2 V	2.7 V	2.2			, v	
			V _{IH} = 2 V	3 V	2.4				
		I _{OH} = -24 mA,	V _{IH} = 2 V	3 V	2				
		l _{OL} = 100 μA		MIN to MAX			0.2		
		I _{OL} = 6 mA,	V _{IL} = 0.7 V	2.3 V			0.4		
VOL		I _{OL} = 12 mA	V _{IL} = 0.7 V	2.3 V			0.7	٧	
			V _{IL} = 0.8 V	2.7 V			0.4	ı	
		I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V			0.55		
lį .		V _I = V _{CC} or GND	1	3.6 V			±5	μΑ	
		V _I = 0.7 V		2.3 V	45		,	μА	
		V _I = 1.7 V		2.5 V	-45				
I _{I(hold)}		V _I = 0.8 V	,	9.1/	75				
, ,		V _I = 2 V		3 ∨	-75				
		V _I = 0 to 3.6 V		3.6 V			±500		
I _{OZ} §		V _O = V _{CC} or GND		3.6 V			±10	μА	
Icc	•	V _I = V _{CC} or GND,	I _O = 0	3.6 V			40	μА	
Δlcc		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА	
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V		4		pF	
Cio	A or B ports	VO = VCC or GND		3.3 V		8		pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM	•		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V	
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	l
t _{pd}	A or B	B or A	1	5		4	1	3.6	ns
t _{en}	ŌĒ	B or A	1	6.8		6	1	5	ns
^t dis	ŌĒ	B or A	1	6		5.2	1	5	ns

operating characteristics, T_A = 25°C

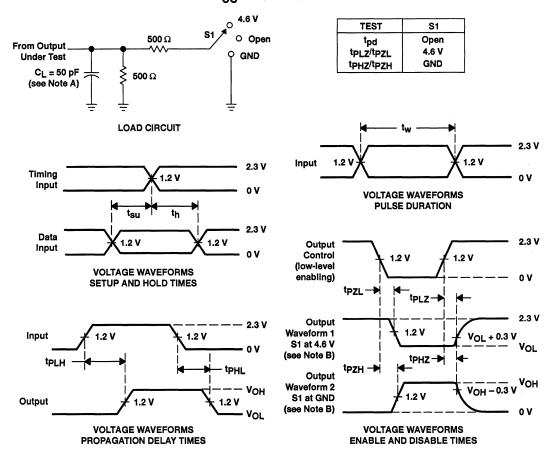
PARAMETER		TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V TYP	V _{CC} = 3.3 V ± 0.3 V TYP	UNIT		
<u> </u>	C . Bower dissination considers	Outputs enabled	O: F0 = F + 10 MU=	22	29	PΓ	
Cpd Power dissipation capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	4	5	рг		

[‡] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

[§] For I/O ports, the parameter IOZ includes the input leakage current.

SCES015 - JULY 1995

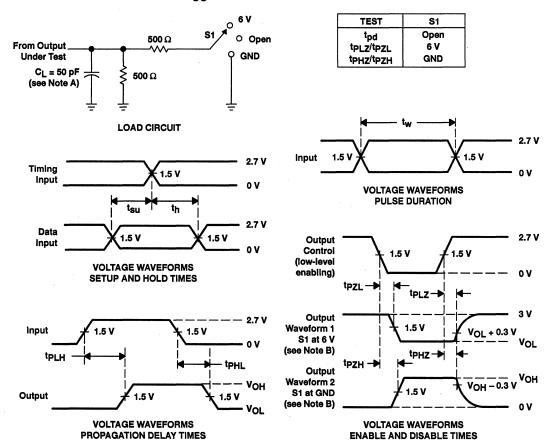
PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \Omega$, $t_{r} \leq 2.5 \text{ ns}$, $t_{f} \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHI are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

SN74ALVC164245 16-BIT 3.3-V TO 5-V LEVEL SHIFTING TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS416A - MARCH 1994 - REVISED DECEMBER 1995

- **Member of the Texas Instruments** Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit (dual-octal) noninverting bus transceiver contains two separate supply rails; B port has V_{CCB}, which is set at 5 V, and A port has V_{CCA}, which is set to operate at 3.3 V. This allows for translation from a 3.3-V to a 5-V environment and vice-versa.

SN74ALVC164245 is designed for asynchronous communication between data buses.

The SN74ALVC164245 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

To ensure the high-impedance state during power up or power down, OE should be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ALVC164245 is characterized for operation from -40°C to 85°C.

DGG OR DL PACKAGE (TOP VIEW)

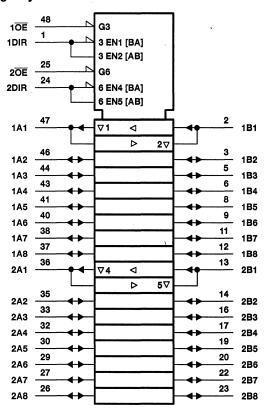
1DIR 🛭	1	48	10E
1B1 🛚			1A1
1B2			1A2
GND [GND
1B3 [] 1A3
1B4 🛚			1A4
(5 V) V _{CCB}	7	42	V _{CCA} (3.3 V)
1B5 L	8	41	1A5
1B6 🛚			1A6
GND [GND
1B7 🛚			1A7
1B8 🛚] 1A8
2B1 🛚			2A1
2B2 🛚] 2A2
GND [GND
2B3 🛚			2A3
2B4 🛚		32	2A4
(5 V) V _{CCB}	18	31	V _{CCA} (3.3 V)
2B5	1	30	2A5
2B6			2A6
GND [GND
2B7			2A7
2B8 🛚			2A8
2DIR	24	25	2 <u>0E</u>

FUNCTION TABLE (each 8-bit section)

,							
INPUTS		OPERATION					
ŌĒ	DIR	OPERATION					
L	L	B data to A bus					
L	Н	A data to B bus					
Н	Х	Isolation					

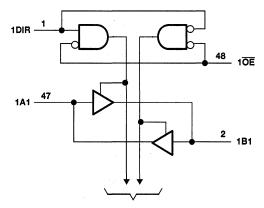
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logic symbol†

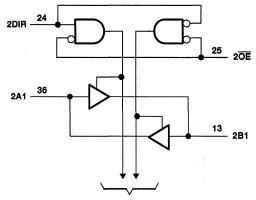


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels



To Seven Other Channels

SN74ALVC164245 16-BIT 3.3-V TO 5-V LEVEL SHIFTING TRANSCEIVER WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range for V_{CCB} at 5 V (unless otherwise noted)†

Supply voltage range, V _{CCB} 0.5 V to 6 V	
Input voltage range, V _I (see Note 1)	
Output voltage range, V _O (see Note 1)	
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CCB}$)	
Output clamp current, l_{OK} ($V_O < 0$ or $V_O > V_{CCB}$)	
Continuous output current, I _O (V _O = 0 to V _{CCB})	
Continuous current through each V _{CCB} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 2): DGG package	
DL package 1.2 W	
Storage temperature range, T _{stg} –65°C to 150°C	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. This value is limited to 6 V maximum.

2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

absolute maximum ratings over operating free-air temperature range for V_{CCA} at 3.3 V (unless otherwise noted)†

Supply voltage range, V _{CCA}	0.5 V to 4.6 V
Input voltage range, VI: Except I/O ports (see Note 3)	0.5 V to 4.6 V
I/O ports (see Note 3)	0.5 V to V _{CCA} + 0.5 V
Output voltage range, VO (see Note 3)	\dots -0.5 V to V _{CCA} + 0.5 V
Input clamp current, $I_{ K }(V_1 < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CCA})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CCA})	±50 mA
Continuous current through each V _{CCA} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 2): DGG package	0.85 W
DL package .	1.2 W
Storage temperature range, Teta	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

3. This value is limited to 4.6 V maximum.

SN74ALVC164245 16-BIT 3.3-V TO 5-V LEVEL SHIFTING TRANSCEIVER WITH 3-STATE OUTPUTS SCAS416A - MARCH 1994 - REVISED DECEMBER 1995

recommended operating conditions for V_{CCB} at 5 V (see Note 4)

		MIN	MAX	UNIT
Vccв	Supply voltage	4.5	5.5	٧
VIH	High-level input voltage	2		٧
V _{IL}	Low-level input voltage		8.0	٧
VIA	Input voltage	0	VCCB	V
VOB	Output voltage	0	VCCB	٧
ЮН	High-level output current		-24	mA
lol	Low-level output current		24	mA
Δt/Δν	Input transition rise or fall rate	0	10	ns/V
TA	Operating free-air temperature	-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

recommended operating conditions for $V_{\mbox{CCA}}$ at 3.3 V (see Note 4)

		*,	MIN	MAX	UNIT
VCCA	Supply voltage	·	2.7	3.6	٧
V _{IH}	High-level input voltage	V _{CCA} = 2.7 V to 3.6 V	2		٧
V _{IL}	Low-level input voltage	V _{CCA} = 2.7 V to 3.6 V		0.8	٧
V _{IB}	Input voltage		.0	VCCA	٧
VOA	Output voltage		0	VCCA	٧
lou	High-level output current	V _{CCA} = 2.7 V		-12	mA
ЮН	riigh-level output current	V _{CCA} = 3 V		-24	ША
lai	Low-level output current	V _{CCA} = 2.7 V		12	mA
lOL	Low-level output current	V _{CCA} = 3 V		24	ША
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TΑ	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

SN74ALVC164245 16-BIT 3.3-V TO 5-V LEVEL SHIFTING TRANSCEIVER WITH 3-STATE OUTPUTS SCAS416A - MARCH 1994 - REVISED DECEMBER 1995

electrical characteristics over recommended operating free-air temperature range for V_{CCB} = 5 V (unless otherwise noted) (see Note 5)

PA	RAMETER	TEST CONDITIONS	VCCB	MIN	TYPT	MAX	UNIT
		100	4.5 V	4.3			
V (A.	40 D)	IOH = -100 μA	5.5 V	5.3			ν
V _{OH} (A to B)		Jan. 04 m4	4.5 V	3.7			\ \ \
		IOH = -24 mA	5.5 V	4.7			
		100	4.5 V			0.2	
\/- /A	1- D)	I _{OL} = 100 μA	5.5 V			0.2	v
V _{OL} (A t	ю ы	I. 04 mA	4.5 V			0.55	٧
		I _{OL} = 24 mA	5.5 V			0.55	
lı	Control inputs	V _I = V _{CCB} or GND	5.5 V			±5	μА
loz‡	A or B ports	VO = VCCB or GND	5.5 V				μА
Icc		$V_I = V_{CCB}$ or GND, $I_O = 0$	5.5 V				μА
∆I _{CC} §		One input at 3.4 V, Other inputs at V _{CCB} or GN	D 4.5 V to 5.5 V				μА
Ci	Control inputs	V _I = V _{CCB} or GND	5 V		6.5		pF
Cio	A or B ports	V _O = V _{CCB} or GND	5 V		6.5		pF

[†] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range for V_{CCA} = 3.3 V (unless otherwise noted) (see Note 6)

PAI	RAMETER	TEST C	ONDITIONS	VCCA	MIN	TYPT	MAX	UNIT
		l _{OH} = -100 μA		MIN to MAX	V _{CC} -0	.2		
V (B.	۱۵ ۸۱	la 10 mA		2.7 V	2.2			v
VOH (B t	10 A)	IOH = -12 mA		3 V	2.4			٧
		I _{OH} = -24 mA		3 V	2			
		I _{OL} = 100 μA		MIN to MAX			0.2	
VOL (B t	o A)	I _{OL} = 12 mA		2.7 V			0.4	٧
		I _{OL} = 24 mA		3 V			0.55	
4	Control inputs	V _I = V _{CCA} or GND		3.6 V			±5	μA
loz‡		VO = VCCA or GND		3.6 V			±10	μA
Icc		V _I = V _{CCA} or GND,	I _O = 0	3.6 V			40	μА
ΔlCC§		One input at V _{CCA} - 0.6 V,	Other inputs at V _{CCA} or GND	3 V to 3.6 V			750	μA
Ci	Control inputs	V _I = V _{CCA} or GND		3.3 V		6.5		pF
Cio	A or B ports	VO = VCCA or GND		3.3 V		8.5		pF

[†] Typical values are measured at VCC = 3.3 V, TA = 25°C.

NOTE 6: $V_{CCB} = 5 V \pm .05 V$



For I/O ports, the parameter IOZ includes the input leakage current.

^{\$} This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather then at 0 V or VCCA. NOTE 5: V_{CCA} = 2.7 V to 3.6 V

For I/O ports, the parameter IOZ includes the input leakage current.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather then at 0 V or VCCA.

 $[\]P$ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

SN74ALVC164245 16-BIT 3.3-V TO 5-V LEVEL SHIFTING TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS416A - MARCH 1994 - REVISED DECEMBER 1995

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

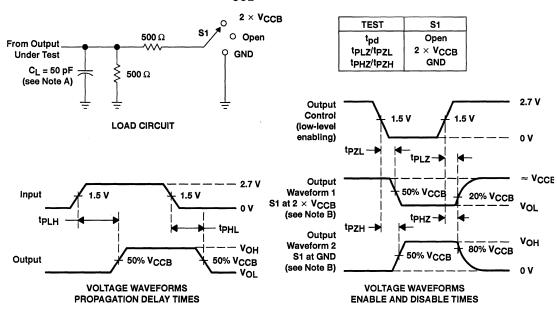
			VCCB = 5	V ± 0.5	٧	
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCA} = 2.7 V	VCCA ± 0	= 3.3 V .3 V	UNIT
		,	MIN MAXT	MINT	MAXT	
	A	В	5.9	1	5.8	ns
^t pd	В	Α	6.7	1.2	5.8	ns
t _{en}	ŌĒ	В	9.3	1	8.9	ns
^t dis	ŌĒ	В	9.2	2.1	9.5	ns
^t en	ŌĒ	A	10.2	2	9.1	ns
^t dis	ŌĒ	Α	9	2.9	8.6	ns

[†] This datasheet limit can vary among suppliers.

operating characteristics, T_A = 25°C

	PARAMETEI	3	TEST COM	NDITIONS	V _{CCA} = 3.3 V V _{CCB} = 5 V	UNIT
C .	Power dissipation especitance	Outputs enabled (A or B)	C. 50 pE	f = 10 MHz	56	nE
C _{pd}	Power dissipation capacitance	Outputs disabled (A or B)	C _L = 50 pF,	I = IU MITZ	6	pF

PARAMETER MEASUREMENT INFORMATION $V_{CCB} = 5 V \pm 0.5 V$

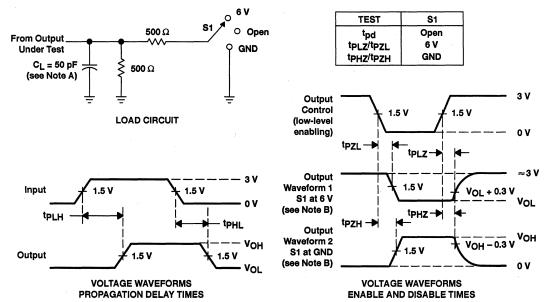


- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SCAS416A - MARCH 1994 - REVISED DECEMBER 1995

PARAMETER MEASUREMENT INFORMATION V_{CCA} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tplz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten. G. tplH and tpHL are the same as tod.

Figure 2. Load Circuit and Voltage Waveforms

SN74ALVCH16260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS

SEL 28

29 OE1B

SCES046 - JULY 1995

Member of the Texas Instruments Widebus™ Family	DGG OR DL (TOP \	
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	OEA 1 LE1B 1 2	56] OE2B 55] LEA2B
 ESD Protection Exceeds 2000 V Per 	2B3 []3	54 2B4
MIL-STD-883C, Method 3015; Exceeds	GND 🛮 4	53 GND
200 V Using Machine Model	2B2 🛮 5	52] 2B5
(C = 200 pF, R = 0)	2B1 🛮 6	51 2B6
Latch-Up Performance Exceeds 250 mA	V _{CC} [] 7	50 V _{CC}
Per JEDEC Standard JESD-17	A1 ∐ 8	49 2 2B7
Bus Hold on Data Inputs Eliminates	A2 ∏ 9	48 2B8
the Need for External Pullup/Pulldown Resistors	A3 🛮 10	47 2B9
1100101010	GND [] 11	46 GND
Package Options Include Plastic Shrink Package Options Include Plastic Shrink	A4 [] 12 A5 [] 13	45 2B10 44 2B11
Small-Outline (DL) and Thin Shrink	A6 [] 14	43 2B12
Small-Outline (DGG) Packages	A7 15	42 1 1B12
description	A8 [] 16	41 1B11
·	A9 II 17	40 1B10
This 12-bit to 24-bit multiplexed D-type latch is	GND 18	39 GND
designed for 2.3-V to 3.6-V _{CC} operation.	A10 19	38 [1B9
The SN74ALVCH16260 is used in applications	A11 🛮 20	37 🛭 1B8
where two separate datapaths must be	A12 🛛 21	36 🛘 1B7
multiplexed onto, or demultiplexed from, a	V _{CC} 🛮 22	35 🕽 V _{CC}
single datapath. Typical applications include	1B1 🛛 23	34 [] 1B6
multiplexing and/or demultiplexing address and	1B2 [] 24	33 🛮 1B5
data information in microprocessor or	GND 🛮 25	32 [GND
bus-interface applications. This device is also	1B3 🛮 26	31 [] 1B4
useful in memory-interleaving applications.	LE2B 🛮 27	30 🛮 LEA1B

Three 12-bit I/O ports (A1-A12, 1B1-1B12, and 2B1-2B12) are available for address and/or data

transfer. The output-enable (OE1B, OE2B, and OEA) inputs control the bus transceiver functions. The OE1B and OE2B control signals also allow bank control in the A-to-B direction.

Address and/or data information can be stored using the internal storage latches. The latch-enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch-enable input is high, the latch is transparent. When the latch-enable input goes low, the data present at the inputs is latched and remains latched until the latch-enable input is returned high.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16260 is available in Tl's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16260 is characterized for operation from -40°C to 85°C.

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Function Tables

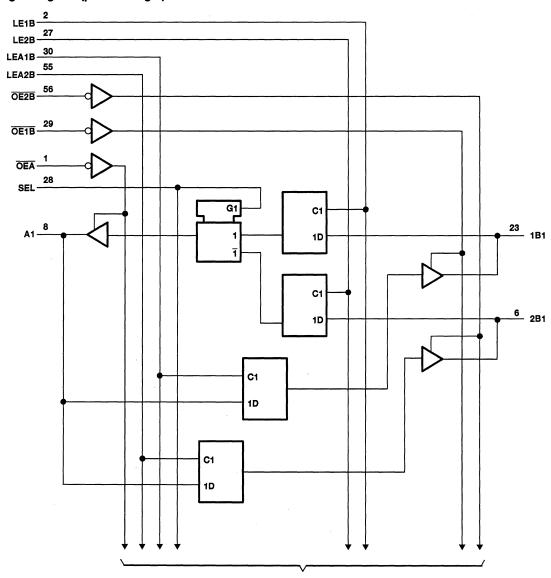
B TO A (OEB = H)

		INP	UTS			OUTPUT
1B	2B	SEL	LE1B	LE2B	OEA	A
Н	Х	Н	Н	Х	L	Н
L	Χ	Н	н	X	L	L
×	X	н	L	Х	L	A ₀
х	Н	L	X	Н	L	н
×	L	L	X	н	L	L
х	X	L	. X	L	L '	A ₀
Х	X	Χ	X	X	Н	Z

A TO B (OEA = H)

		INPUTS			OUT	PUTS
Α	LEA1B	LEA2B	OE1B	OE2B	1B	2B
Н	Н	Н	L	L	Н	Н
L	н	Н	L	L	L	L
н	н	L	L	L	н	2B ₀
L	Н	L	L	L	L	2B ₀
н	L	н	L	L	1B ₀	Н
L	L	Н	L	L	1B ₀	L
X	L	L	L	L	1B ₀	2B ₀
Х	Х	Х	н	н	Z	Z ^r
x	Х	X	L	Н	Active	Z
X	X	X	Н	L	Z	Active
Х	Х	Х	L	L	Active	Active

logic diagram (positive logic)



To 11 Other Channels

SN74ALVCH16260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS

SCES046 - JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}
$\begin{array}{llllllllllllllllllllllllllllllllllll$
$\begin{array}{llllllllllllllllllllllllllllllllllll$
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ± 50 mA Continuous output current, I_O (V_O = 0 to V_{CC}) ± 50 mA Continuous current through each V_{CC} or GND ± 100 mA Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package 1 W
Continuous output current, I_O (V_O = 0 to V_{CC})
Continuous current through each V_{CC} or GND
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package
DL package 1.4 W
Storage temperature range, T _{stq} –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		2.3	3.6	V
	High level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7		V
VIH	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		V
V.	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
VIL	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	V
VI	Input voltage		0	VCC	V
٧o	Output voltage		0	Vcc	V
		V _{CC} = 2.3 V		-12	
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		2.3 3.6 1.7 2 0.7 0.8 0 V _{CC} 0 V _{CC} -12	
		V _{CC} = 2.3 V		12	
loL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature	,	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN74ALVCH16260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS

SCES046 - JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	RAMETER	TEST C	ONDITIONS	v _{cc} t	MIN	TYP‡	MAX	UNIT
		I _{OH} = -100 μA		MIN to MAX	VCC-0	.2		
		I _{OH} = −6 mA,	V _{IH} = 1.7 V	2.3 V	2			
W			V _{IH} = 1.7 V	2.3 V	1.7			v
VOH		I _{OH} = -12 mA	V _{IH} = 2 V	2.7 V	2.2			V
			V _{IH} = 2 V	3 V	2.4			
		I _{OH} = -24 mA,	V _{IH} = 2 V	3 V	2			
		I _{OL} = 100 μA		MIN to MAX			0.2	
		I _{OL} = 6 mA,	V _{IL} = 0.7 V	2.3 V			0.4	
V _{OL}			V _{IL} = 0.7 V	2.3 V			0.7	V
		I _{OL} = 12 mA	V _{IL} = 0.8 V	2.7 V			0.4	
		I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V			0.55	
l _l		VI = VCC or GND		3.6 V			±5	μА
		V _J = 0.7 V			45			
		V _I = 1.7 V		2.3 V	-45			
(hold)		V _I = 0.8 V		1	75			μА
		V _I = 2 V		3 ٧	-75			
		V _I = 0 to 3.6 V		3.6 V			±500	
loz§		VO = VCC or GND		3.6 V			±10	μА
lcc		VI = VCC or GND,	I _O = 0	3.6 V			40	μА
ΔICC		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА
C _i	Control inputs	VI = VCC or GND		3.3 V		3.5		pF
Cio	A or B ports	VO = VCC or GND		3.3 V		9		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high	3.3		3.3		3.3		ns
tsu	Setup time, data before LE1B, LE2B, LEA1B, or LEA2B	1.4		1.1		1.1		ns
th	Hold time, data after LE1B, LE2B, LEA1B, or LEA2B	1.6		1.9		1.5		ns

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. § For I/O ports, the parameter I_{OZ} includes the input leakage current.

SN74ALVCH16260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS SCES046 - JULY 1995

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

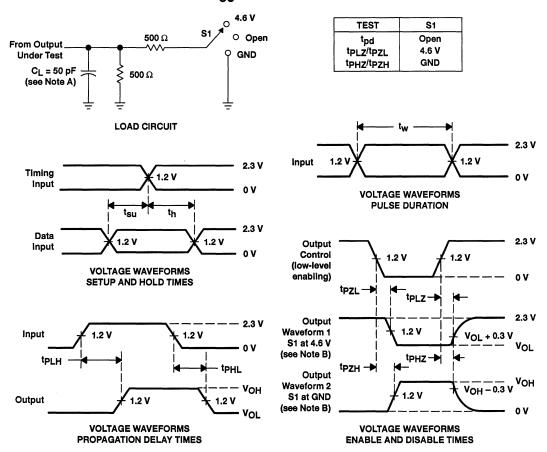
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} = ± 0.	3.3 V 3 V	UNIT
	(INFOT)	(001801)	MIN	MAX	MIN	MAX	MIN	MAX	
	A or B	B or A	1.2	6		5.1	1.2	4.3	
t _{pd}	LE	A or B	1	6.2		5.2	1	4.4	ns
	SEL	Α	1.2	7.5		6.6	1.1	5.6	
t _{en}	ŌĒ	A or B	1	7.2		6.4	1	5.4	ns
^t dis	ŌĒ	A or B	1.7	5.9		5	1.3	4.6	ns

operating characteristics, T_A = 25°C

	PARAMETER		TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT	
			TYP				
	Down dissination consistence	Outputs enabled	C _L = 50 pF, f = 10 MHz	87	120	ρF	
C _{pd}	Fower dissipation capacitance	wer dissipation capacitance Outputs disabled		80.5	118	ρг	

SCES046 - JULY 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

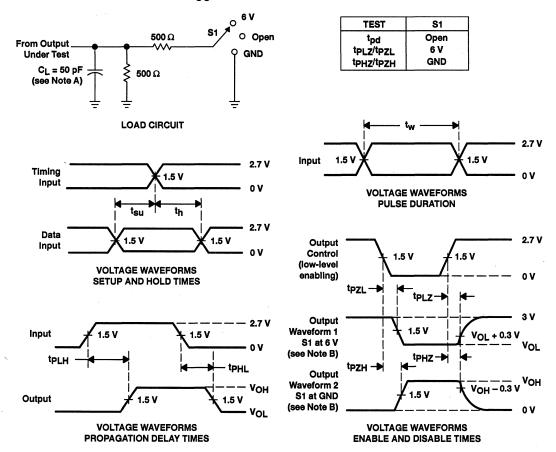


- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms

SCES046 - JULY 1995

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V } \pm 0.3 \text{ V}$



NOTES: A. C_L includes probe and jig capacitance.

- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_f ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

SN74ALVCH162268 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES018 - AUGUST 1995

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- B-Port Outputs Have Equivalent 26- Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 12-bit to 24-bit registered bus exchanger is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH162268 is used for applications where data must be transferred from a narrow high-speed bus to a wide, lower-frequency bus.

The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable (CLKEN) inputs are low. The select (SEL) line is synchronous with CLK and selects 1B or 2B input data for the A outputs.

DGG OR DL PACKAGE (TOP VIEW)

OEA [₁ O	56	OEB
CLKEN1B [2	55	CLKENA2
2B3 [2B4
GND [4	53	GND
2B2 [5	52	2B5
2B1 [6]2B6
v _{cc} [7	50]v _{cc}
A1 []	8	49] 2B7
A2 [9] 2B8
A3 [10] 2B9
GND []GND
A4 []2B10
A5 [2B11
A6 []2B12
A7 []1B12
A8 [41]1B11
A9 [40]1B10
GND [] GND
A10 🛚] 1B9
A11 [] 1B8
A12 🛚	21] 1B7
v _{cc} [22	35]∨ _{cc}
1B1 🛭] 1B6
1B2 [24] 1B5
GND [25		[] GND
1B3 [31] 1B4
CLKEN2B			CLKENAT
SEL [28	29]]CLK

For data transfer in the A-to-B direction, a two-stage pipeline is provided in the A-to-1B path with a single storage register in the A-to-2B path. Proper control of these inputs allows two sequential 12-bit words to be presented synchronously as a 24-bit word on the B port. Data flow is controlled by the active-low output enables (OEA, OEB). These control terminals are registered so bus direction changes are synchronous with CLK.

The B outputs, which are designed to sink up to 12 mA, include $26-\Omega$ resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162268 is characterized for operation from -40°C to 85°C.

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SCES018 - AUGUST 1995

Function Tables

OUTPUT ENABLE

	INPUTS		OUT	PUTS
CLK	OEA	OEB	Α	1B, 2B
1	Н	Н	Z	Z
1	Н	L	z i	Active
	L	Н	Active	Z
↑	L.	L	Active	Active

A-TO-B STORAGE (OEB = L)

				,	
	INPUTS			OUTI	PUTS
CLKENA1	CLKENA2	CLK	Α	1B	2B
Н	Н	Х	Χ	1B ₀ ‡	2B ₀ ‡
L	X	1	L	L†	х
L	Х	1	Н	н†	х
х	L	1	L	Х	L
X	L	↑	Н	х	. Н

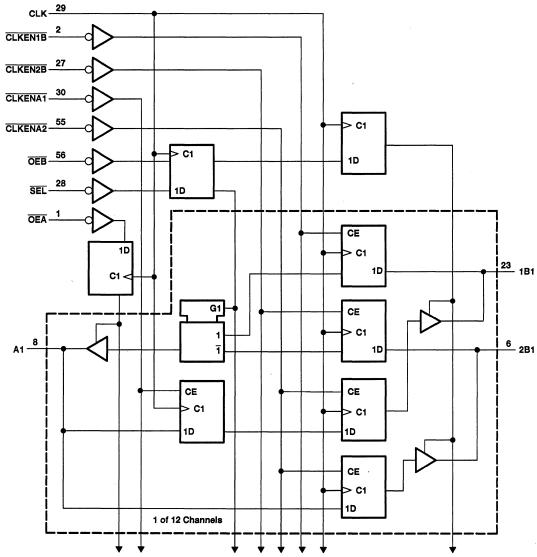
B-TO-A STORAGE (OEA = L)

	INPUTS						
CLKEN1B	CLKEN2B	CLK	SEL	1B	2B	Α	
Н	Х	Х	Н	Х	Х	A ₀ ‡	
Х	. н	Χ	, L	Χ	X	A ₀ ‡	
L	Χ	↑	Н	L	Х	L	
L	X	1	Н	Н	Χ	н	
X	L	1	L	X	L	L.	
Х	L	1	L	Х	Н	Н	

[‡]Output level before the indicated steady-state input conditions were established

[†] Two CLK edges are needed to propagate data. ‡ Output level before the indicated steady-state input conditions were established

logic diagram (positive logic) CLK-29



SN74ALVCH162268 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES018 - AUGUST 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} 0.5 V to 4.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)
1/O ports (see Notes 1 and 2)0.5 V to V _{CC} + 0.5 V
Output voltage range, V _O (see Notes 1 and 2)
Input clamp current, I _{IK} (V _I < 0)
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})
Continuous output current, I _O (V _O = 0 to V _{CC}) ±50 mA
Continuous current through each V _{CC} or GND
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package
DL package 1.4 W
Storage temperature range, T _{sto} –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	V
	Liliah laval innuk valkana	V _{CC} = 2.3 V to 2.7 V	1.7		v
ViH	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		V
V	Low lovel input veltage	V _{CC} = 2.3 V to 2.7 V		0.7	V
VIL	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	_ v
۷Į	Input voltage		0	VCC	V
Vο	Output voltage		0	٧cc	٧
		V _{CC} = 2.3 V		-6	
ЮН	High-level output current (B port)	V _{CC} = 2.7 V		-8	mA
		V _{CC} = 3 V		-12	
		V _{CC} = 2.3 V		6	
lOL	Low-level output current (B port)	rent (B port) V _{CC} = 2.7 V		8	mA
		V _{CC} = 3 V		12	
		V _{CC} = 2.3 V		-12	
IOH	High-level output current (A port)	$V_{CC} = 2.7 \text{ V}$		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 2.3 V		12	
lOL	Low-level output current (A port)	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	1
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



SN74ALVCH162268 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS SCES018 - AUGUST 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST C	ONDITIONS	v _{cc} t	MIN	TYP‡	MAX	UNIT
	I _{OH} = -100 μA		MIN to MAX	V _{CC} -0	.2		
	i _{OH} = -4 mA,	V _{IH} = 1.7 V	2.3 V	1.9			
VOH	$ \begin{array}{c} \text{OH} \\ \text{3 port)} \end{array} \begin{array}{c} \text{I}_{\text{OH}} = -6 \text{mA} \\ \end{array} \begin{array}{c} \text{I}_{\text{OH}} = -8 \text{mA}, & \text{V}_{\text{IH}} = 2 \text{V} \\ \end{array} \begin{array}{c} \text{3 V} \\ \text{2.7 V} \\ \end{array} \begin{array}{c} 2 \\ \text{3 V} \\ \end{array} \begin{array}{c} \text{2.2 V} \\ \end{array} \begin{array}{c} \text{2.2 V} \\ \end{array} \begin{array}{c} \text{2.2 V} \\ \text{3 V} \\ \text{3 V} \\ \end{array} \begin{array}{c} \text{2.2 V} \\ \text{3 V} \\ \text{3 V} \\ \end{array} \begin{array}{c} \text{2.2 V} \\ \text{3 V} \\ \text{3 V} \\ \end{array} \begin{array}{c} \text{2.2 V} \\ \text{3 V} \\ \end{array} \begin{array}{c} \text{2.2 V} \\ \text{3 V} \\ \text{3 V} \\ \end{array} \begin{array}{c} \text{2.2 V} \\ \text{3 V} \\ \text{3 V} \\ \end{array} \begin{array}{c} \text{2.2 V} \\ \text{3 V} \\ \text{4 Port)} \\ \text{4 Port)} \\ \text{4 Port)} \\ \text{4 Port} \\$	v					
(B port)	10H = -0 mA	V _{IH} = 2 V	3 V	2.4			V
	I _{OH} = -8 mA,	V _{IH} = 2 V	2.7 V	2			
	$I_{OH} = -12 \text{ mA},$	V _{IH} = 2 V	3 V	2			
	I _{OL} = 100 μA		MIN to MAX			0.2	
	IOL = 4 mA,	V _{IL} = 0.7 V	2.3 V			0.4	
VOL	In. 6 mA	V _{IL} = 0.7 V	2.3 V			0.55	v
(B port)	IOL = 0 IIIA	V _{IL} = 0.8 V	3 V			0.55	· •
	I _{OL} = 8 mA,	V _{IL} = 0.8 V	2.7 V			0.6	
	I _{OL} = 12 mA,	V _{IL} = 0.8 V	3 V			0.8	
	IOH = -100 μA		MIN to MAX	VCC-0	.2		
	IOH = −6 mA,	V _{IH} = 1.7 V	2.3 V	2			
Vон		V _{IH} = 1.7 V	2.3 V	1.7			v
(A port)	I _{OH} = -12 mA	V _{IH} = 2 V	2.7 V	2.2			. '
		V _{IH} = 2 V	3 V	2.4			
	I _{OH} = -24 mA,	V _{IH} = 2 V	3 V	2			
	I _{OL} = 100 μA		MIN to MAX			0.2	
	$I_{OL} = 6 \text{ mA},$	V _{IL} = 0.7 V	2.3 V			0.4	
VOL	In. 10 mA	V _{IL} = 0.7 V	2.3 V			0.7	٧
(A port)	IOL = 12 IIIA	V _{IL} = 0.8 V	2.7 V			0.4	
	I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V			0.55	
l _l	VI = VCC or GND		3.6 V			±5	μА
	V _I = 0.7 V		2.3 V	45			
	V _I = 1.7 V		2.3 V	-45			
I _I (hold)	V _I = 0.8 V		2.1/	75			μА
, ,	V _I = 2 V		3 V	-75			
	V _I = 0 to 3.6 V		3:6 V			±500	
I _{OZ} §	VO = VCC or GND		3.6 V			±10	μA
Icc	VI = VCC or GND,	I _O = 0	3.6 V			40	μА
ΔICC	One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА
C _i Control inputs	VI = VCC or GND		3.3 V		3.5		pF
Cio A or B ports	VO = VCC or GND		3.3 V		9		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. § For I/O ports, the parameter I_{OZ} includes the input-leakage current.

SN74ALVCH162268 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS SCES018 - AUGUST 1995

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V _{CC} =		V _{CC} =	2.7 V	V _{CC} = 3.3 V ± 0.3 V		UNIT
		·	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequenc	у	0	120	0	125	0	150	MHz
t _W	Pulse duration	CLK high or low	3.3		3.3		3.3		ns
		A data before CLK↑	4.5		4		3.4		
		B data before CLK↑	0.8		1.2		1		
	Catua tima	SEL before CLK↑	1.4		1.6		1.3		
^t su	Setup time	CLKENA1 or CLKENA2 before CLK↑	3.6		3.4		2.8		ns
		CLKENB1 or CLKENB2 before CLK↑	3.2		3		2.5		
		OE before CLK↑	4.2		3.9		3.2		
		A data after CLK↑	0		0		0.2		
		B data after CLK↑	1.3		1.2		1.3		
	11-1-14:	SEL after CLK↑	1		1		1		
th	Hold time	CLKENA1 or CLKENA2 after CLK↑	0.1		0.1		0.4		ns
		CLKENB1 or CLKENB2 after CLK↑	0.1		0		0.5		
		OE after CLK↑	0	-	0		0.2		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =	2.7 V	V _{CC} =		UNIT
	(INPOT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			120		125		150		MHz
^t pd	CLK	В	2.1	6.7		5.9	1.8	5.4	ns
t _{pd}	CLK	A (1B)	2.1	6.4		5.4	1.7	4.8	ns
t _{pd}	CLK	A (2B)	2.1	6.4		5.3	1.8	4.8	ns
t _{pd}	CLK	A (SEL)	3	7.9		6.5	2.4	5.8	ns
ten	CLK	В	2.8	7.7		6.8	2.6	6.1	ns
t _{dis}	CLK	В	3.5	7.4		6.1	2.5	5.9	ns
ten	CLK	Α	2.1	6.7		5.6	1.8	5.1	ns
^t dis	CLK	Α	2.7	6.7		5.4	2.1	5	ns

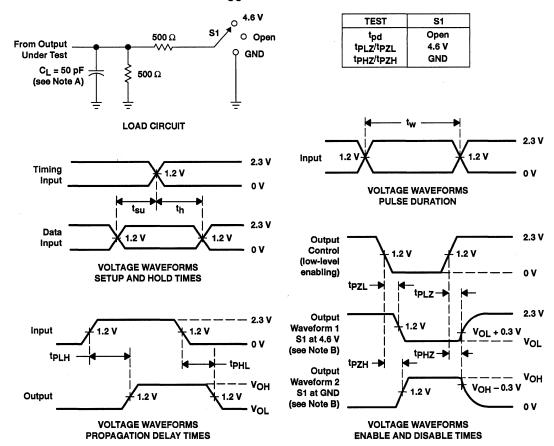
operating characteristics, $T_A = 25$ °C

PARAMETER			TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
			TYP	TYP		
Cpd	Power dissipation capacitance	Outputs enabled	C ₁ = 50 pF, f = 10 MHz	87	120	
Ора	r ower dissipation capacitance	Outputs disabled	C _L = 50 pF, f = 10 MHz	80.5	118	pF



SCES018 - AUGUST 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

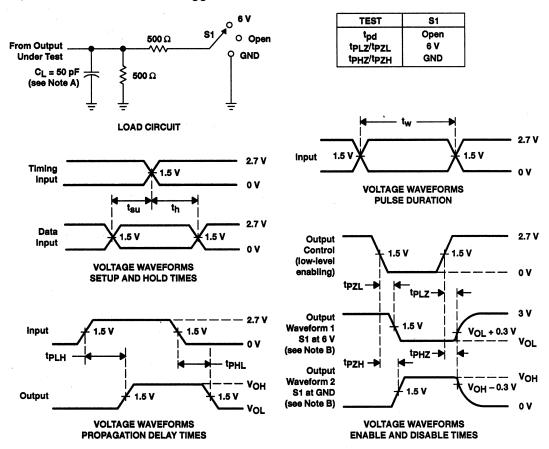


- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SCES018 - AUGUST 1995

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V } \pm 0.3 \text{ V}$



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tplz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

SCES019 - JULY 1995

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 12-bit to 24-bit registered bus transceiver is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16269 is used in applications where two separate ports must be multiplexed onto, or demultiplexed from, a single port. The device is particularly suitable as an interface between synchronous DRAMs and high-speed microprocessors.

Data is stored in the internal B-port registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable (CLKENA) inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B port. For data

DGG OR DL PACKAGE (TOP VIEW)

OEA [1	56	OEB2
OEB1 [2	55	CLKENA2
2B3 🛚	3	54] 2B4
GND [4	53	GND
2B2 [5	52] 2B5
2B1 [51] 2B6
v _{cc} [7	50] v _{cc}
A1 [8	49	2B7
A2 [48] 2B8
A3 [47] 2B9
GND [11	46	GND
A4 [45]2B10
A5 [44	2B11
A6 [43]2B12
A7 [42] 1B12
A8 [41] 1B11
A9 [40] 1B10
GND [] GND
A10 [19	38] 1B9
A11 [37] 1B8
A12 [36	
v _{cc} [22	35	Dv _{cc}
1B1 🛭		34] 1B6
1B2 🛚] 1B5
GND [GND
1B3 [] 1B4
NC [27	30	CLKENA1
SEL [28	29]]CLK
			-

NC - No internal connection

transfer in the B-to-A direction, a single storage register is provided. The select (SEL) line selects 1B or 2B data for the A outputs. The register on the A output permits the fastest possible data transfer, thus extending the period that the data is valid on the bus. The control terminals are registered so that all transactions are synchronous with CLK. Data flow is controlled by the active-low output enables (OEA, OEB1, OEB2).

To ensure the high-impedance state during power up or power down, $\overline{\sf OE}$ should be tied to ${\sf V}_{\sf CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16269 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16269 is characterized for operation from -40°C to 85°C.

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SCES019 - JULY 1995

Function Tables

OUTPUT ENABLE

	INPUTS		OUTPUTS			
CLK	OEA	OEB	Α	1B, 2B		
1	Н	Н	Z	Z		
1	Н	L	z	Active		
1	L	Н	Active	Z		
1	L	L	Active	Active		

A-TO-B STORAGE (OEB = L)

	INPUTS				
CLKENA1	CLKENA2	CLK	Α	1B	2B
Н	Н	X	Х	1B ₀ †	2B ₀ †
L	X	1	L	L	х
L	X	1	Н	н	х
x	L	1	L	Х	L
Х	L	1	Н	x	Н

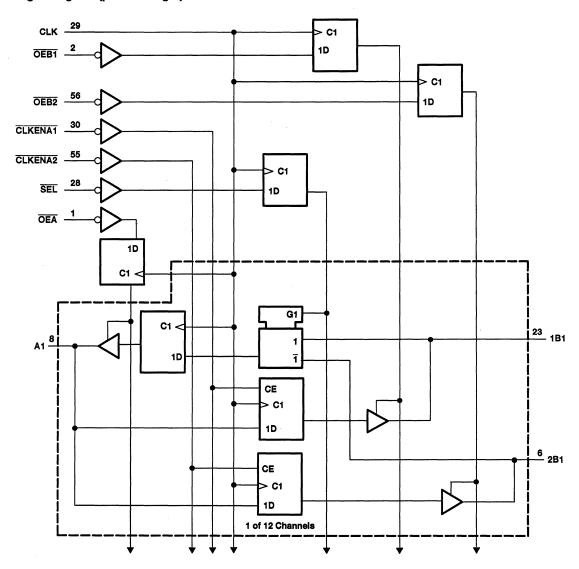
[†]Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE (OEA = L)

	INP	JTS		OUTPUT
CLK	SEL	1B	2B	A
Х	Н	Х	Х	A ₀ † A ₀ †
Х	L	Χ	X	A ₀ †
↑	н	L	Χ	L
1	н	Н	Х	н
1	L	X	L	L
1	L	Х	Н	Н

[†] Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)



SN74ALVCH16269 12-BIT TO 24-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES019 - JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)	
	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through each V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3)	: DGG package 1 W
	DL package 1.4 W
Storage temperature range, T _{stq}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage	7	2.3	3.6	٧
V	High level input veltage	V _{CC} = 2.3 V to 2.7 V	1.7		v
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V.,	Low level input veltage	V _{CC} = 2.3 V to 2.7 V		0.7	v
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
٧į	Input voltage		0	VCC	٧
Vo	Output voltage		0	VCC	٧
		V _{CC} = 2.3 V		-12	
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 2.3 V		12	
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

^{3.} The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

SCES019 - JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMET	ER	TEST CO	ONDITIONS	vcct	MIN	TYP‡	MAX	UNIT
	IOH = -	·100 μA		MIN to MAX	VCC-C	.2		
•	ioH = -	6 mA,	V _{IH} = 1.7 V	2.3 V	2			i
,			V _{IH} = 1.7 V	2.3 V	1.7			v
VOH	IOH = -	12 mA	V _{IH} = 2 V	2.7 V	2.2			V
	1		V _{IH} = 2 V	3 V 2.4				
	IOH = -	24 mA,	V _{IH} = 2 V	3 V	2			
	I _{OL} = 10	00 μΑ		MIN to MAX			0.2	
	I _{OL} = 6	mA,	V _{IL} = 0.7 V	2.3 V			0.4	
VOL	Jan. 46	0 4	V _{IL} = 0.7 V	2.3 V			0.7	V
	I _{OL} = 12	z ma	V _{IL} = 0.8 V	2.7 V			0.4	
	I _{OL} = 24	4 mA,	V _{IL} = 0.8 V	3 V			0.55	
11	VI = VC	C or GND		3.6 V			±5	μА
	V _I = 0.7	·V		221	45			
	$V_{ } = 1.7$	٧.		2.3 V	-45			
l(hold)	$V_{ } = 0.8$	V		3 V	75			μА
	V ₁ = 2 V	1] 3V	-75			
	$V_{\parallel} = 0 \text{ to}$	3.6 V		3.6 V			±500	
IOZ§	V _O = V ₀	CC or GND		3.6 V			±10	μА
ICC	VI = VC	C or GND,	IO = 0	3.6 V			40	μА
ΔICC	One inp	out at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА
C _i Contro	inputs V _I = V _C	C or GND		3.3 V		3.5		pF
Cio A or B	ports V _O = V ₀	CC or GND		3.3 V		9		рF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V _{CC} = 2.5 V ± 0.2 V		V _{CC} =	2.7 V	V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequen	cy .	0	135	0	135	0	135	MHz
tw	Pulse duration	n, CLK high or low	3.3		3.3		3.3		ns
		A data before CLK↑	2		2		1.7		
		B data before CLK↑	2.2		2.1		1.8		
t _{su}	Setup time	SEL before CLK↑	1.6		1.6		1.3		MHz
		CLKENA1 or CLKENA2 before CLK↑	1		1.2		0.9		
		OE before CLK↑	1.5		1.6		1.3		
		A data after CLK↑	0.7		0.6		0.6		
		B data after CLK↑	0.7		0.6		0.6		
th	Hold time	SEL after CLK↑	1.1		0.7		0.7		ns
		CLKENA1 or CLKENA2 after CLK1	1		0.8		1.1		
		OE after CLK↑	0.8		0.8		0.8		ĺ

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[§] For I/O ports, the parameter IOZ includes the input-leakage current.

SN74ALVCH16269 12-BIT TO 24-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCES019 – JULY 1995

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

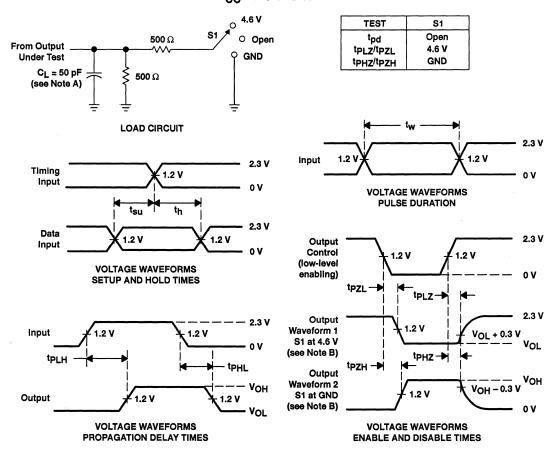
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INPUT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			135		135		135		MHz
	CLK	В	1	8.8		7.3	1	6.2	
^t pd	OLK	A	1	7		5.8	1	5	113
	OLK	В	1	8.4		6.7	1	6.1	ns
^t en	CLK	Α	1	8.1		6.2	1	5.9	115
^t dis	CLK	В	1.4	8.3		6.9	1	6.1	
	OLK	Α	1.5	7.7		6.8	1	5.6	ns

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
			TYP	TYP		
C .	Dower dissination consistence	Outputs enabled	C. FO. F. 4 40 MH-	87	120	pF
C _{pd}	Power dissipation capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	80.5	118	þΓ

SCES019 - JULY 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



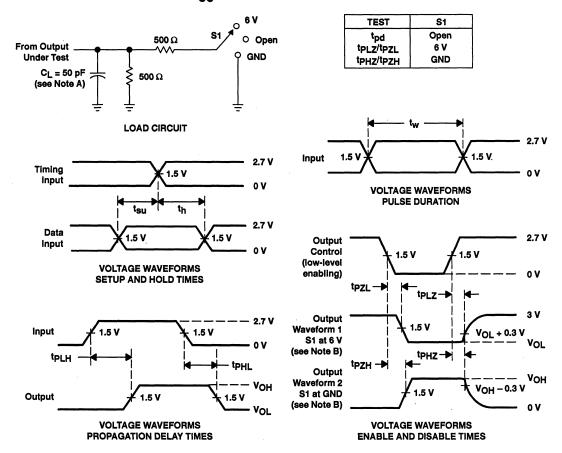
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SCES019 - JULY 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , $t_{\rm f} \leq$ 2.5 ns, $t_{\rm f} \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

SN74ALVCHR162269 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES050 - AUGUST 1995

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- All Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 12-bit to 24-bit registered bus exchanger is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCHR162269 is used in applications where two separate ports must be multiplexed onto, or demultiplexed from, a single port. It is particularly suitable as an interface between synchronous DRAMs and high-speed microprocessors.

Data is stored in the internal B-port registers on the low-to-high transition of the clock (CLK) input when the appropriate clock enable (CLKENA)

DGG OR DL PACKAGE (TOP VIEW)

			L
OEA]1 `	56	OEB2
OEB1	2	55	CLKENA2
2B3]з	54]] 2B4
GND]4	53	GND
2B2	5	52] 2B5
2B1	6] 2B6
Vcc	7	50]∨ _{cc}
A1] 8	49	2B7
A2		48] 2B8
A3	10	47] 2B9
GND			GND
A4		45	2B10
	13		2B11
	14		2B12
	15] 1B12
8A	16	41] 1B11
	17	40	1B10
GND		39	GND
A10		38] 1B9
A11	20] 1B8
A12		36] 1B7
Vcc		35] v _{cc}
1B1] 1B6
1B2	24] 1B5
GND	25] GND
1B3] 1B4
NC	27	30	CLKENAT
SEL	28	29]CLK
	-		-

NC - No internal connection

inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B port. For data transfer in the B-to-A direction, a single storage register is provided. The select (SEL) line selects 1B or 2B data for the A outputs. The register on the A output permits the fastest possible data transfer, thus extending the period that the data is valid on the bus. The control terminals are registered so that all transactions are synchronous with CLK. Data flow is controlled by the active-low output enables (OEA, OEB1, and OEB2).

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

All outputs are designed to sink up to 12 mA and include $26-\Omega$ resistors to reduce overshoot and undershoot.

The SN74ALVCHR162269 is characterized for operation from -40°C to 85°C.

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Function Tables

OUTPUT ENABLE

INPUTS			OUTPUTS		
CLK OEA OEB		Α	1B, 2B		
1	Н	Н	Z	Z	
1	Н	L,	Ż	Active	
1	L	Н	Active	Z `	
1	L	L	Active	Active	

A-TO-B STORAGE (OEB = L)

INPUTS				OUTPUTS		
CLKENA1	CLKENA2	CLK	Α	1B	2B	
L	Н	1	L	L	2B ₀ †	
L	Н	1	Н	Н	2B ₀ †	
L	L	1	L	L	L	
L	L	1	Н	н	н	
Н	L	1	L	1B ₀ †	L	
H	L	1	Н	1B ₀ †	н	
Н	н	Х	X	1B ₀ †	2B ₀ †	

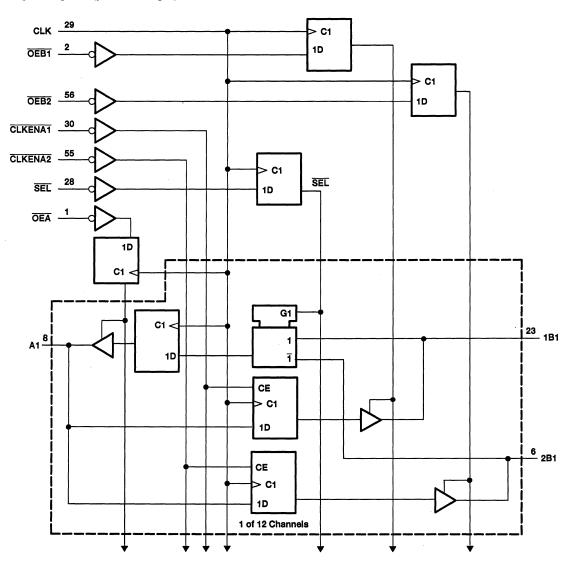
[†]Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE (OEA = L)

	OUTPUT			
CLK	SEL	1B	2B	Α
Х	Н	Х	Х	A ₀ † A ₀ †
Х	L	Χ	Χ	A ₀ †
1	Н	L	Х	L
1	Н	Н	Χ	н
1	L	Χ	L	L
1	L	Х	Н	Н

[†] Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)



SN74ALVCHR162269 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES050 - AUGUST 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, VI: Except I/O ports (see Note 1)	0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	
Continuous current through each V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (s	ee Note 3): DGG package 1 W
	DL package 1.4 W
Storage temperature range, T _{stg}	−65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		2.3	3.6	٧	
VIH	$V_{CC} = 2.3 \text{ V to } 2.3 \text{ V}$		1.7		V	
	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		·	
VIL		V _{CC} = 2.3 V to 2.7 V		0.7	V	
	Low-level input voltage V _{CC} = 2.7 V to			0.8	l	
٧١	Input voltage		0	VCC	V	
٧o	Output voltage		0	VCC	٧	
		V _{CC} = 2.3 V		-6	mA	
ЮН	High-level output current	V _{CC} = 2.7 V		-8		
		V _{CC} = 3 V		-12		
		V _{CC} = 2.3 V		6		
lOL	Low-level output current	V _{CC} = 2.7 V		8	mA	
	V _{CC} = 3 V			12		
Δt/Δν	Input transition rise or fall rate		0	10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN74ALVCHR162269 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARA	METER	TEST CONDITIONS		vcct	MIN	TYP‡	MAX	UNIT	
		l _{OH} = -100 μA		MIN to MAX	V _{CC} -0	.2			
		I _{OH} = -4 mA	V _{IH} = 1.7 V	2.3 V	1.9				
			V _{IH} = 2 V	2.7 V	2.2				
Vон		I _{OH} = -6 mA	V _{IH} = 1.7 V	2.3 V	1.7			V	
			V _{IH} = 2 V	3 V	2.4				
		IOH = -8 mA,	V _{IH} = 2 V	2.7 V	2				
		I _{OH} = -12 mA,	V _{IH} = 2 V	3 V	2				
		i _{OL} = 100 μA		MIN to MAX			0.2		
		le: 4 mA	V _{IL} = 0.7 V	2.3 V			0.4	· V	
		IOL = 4 mA	V _{IL} = 0.8 V	2.7 V			0.4		
VOL		I _{OL} = 6 mA	V _{IL} = 0.7 V	2.3 V			0.55		
			V _{IL} = 0.8 V	3 V			0.55		
		I _{OL} = 8 mA,	V _{IL} = 0.8 V	2.7 V			0.6	ļ	
		I _{OL} = 12 mA,	V _{IL} = 0.8 V	3 V			0.8		
1 ₁		V _I = V _{CC} or GND		3.6 V			±5	μА	
		V _I = 0.7 V		2.3 V	45			μΑ	
		V _I = 1.7 V		2.5 V	-4 5				
l(hold)		V _I = 0.8 V		3 V	75				
		V _I = 2 V		7 34	-75				
·		V _I = 0 to 3.6 V		3.6 V			±500		
loz§		VO = VCC or GND		3.6 V			±10	μА	
Icc		V _I = V _{CC} or GND,	I _O = 0	3.6 V			40	μА	
ΔlCC		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА	
	ontrol inputs	V _I = V _{CC} or GND		3.3 V		3.5		рF	
C _{io} A	or B ports	VO = VCC or GND		3.3 V		9		pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. § For I/O ports, the parameter I_{OZ} includes the input leakage current.

SN74ALVCHR162269 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS SCES050 - AUGUST 1995

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
l			MIN	MAX	MIN	MAX	MIN	MAX		
fclock	Clock frequency		0	135	0	135	0	135	MHz	
t _w			3.3	•	3.3		3.3		ns	
	Setup time	A data before CLK↑	2		2		1.7			
		B data before CLK↑	2.2		2.1		1.8		ns	
tsu		SEL before CLK↑	1.6		1.6		1.3			
		CLKENA1 or CLKENA2 before CLK↑	1		1.2		0.9			
		OE before CLK↑	1.5		1.6		1.3			
		A data after CLK↑	0.7		0.6		0.6			
		B data after CLK↑	0.7		0.6		0.6			
th	Hold time	SEL after CLK↑	1.1		0.7		0.7		ns	
		CLKENA1 or CLKENA2 after CLK↑	1		0.8		1.1			
		OE after CLK↑	0.8		0.8		0.8			

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

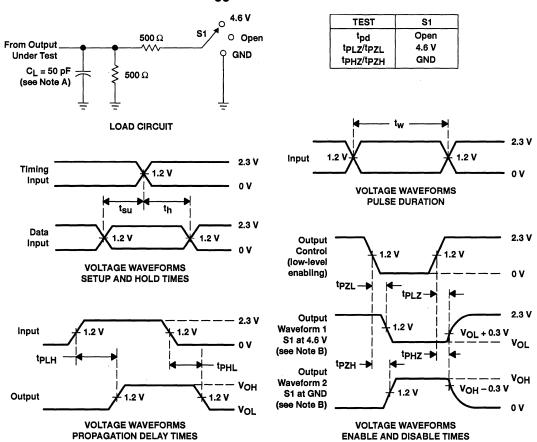
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INFOT)		MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			135		135		135		MHz
	CLK	В	1.5	9.2		7.9	1.6	6.7	ns
^t pd	OLK	A	1.5	7.4		6.4	1.6	5.5	115
	OLK	В	1.5	8.8		7.3	1.6	6.6	ns
^t en	CLK	Α	1.5	8.5		6.8	1.6	6.4	115
+ ,,	CLK	В	1.8	8.7		7.5	1.6	6.5	no
^t dis	OLN .	A	1.9	8.1		7.4	1.6	6	ns

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
			TYP	TYP		
C .	Power dissipation capacitance	Outputs enabled	C: 50 pF f 10 MH=	- 10 MHz 87		ρF
C _{pd}	rower dissipation capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	80.5	118] PF

SCES050 - AUGUST 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

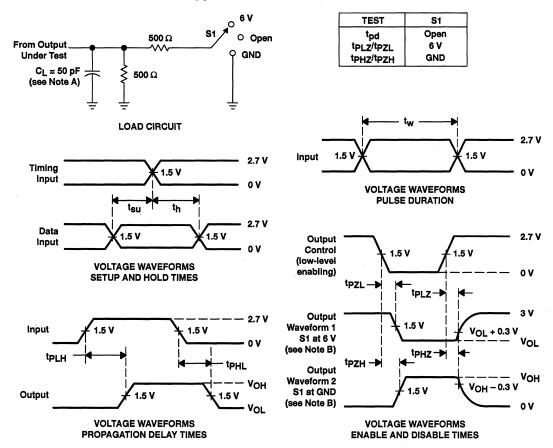


- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \, \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SCES050 - AUGUST 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement,
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

SN74ALVCH16270 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES028 - JULY 1995

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA
 Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 12-bit to 24-bit registered bus exchanger is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16270 is used in applications where data must be transferred from a narrow high-speed bus to a wide lower-frequency bus.

The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input when the appropriate CLKEN inputs are low. The select (SEL) line selects 1B or 2B data for the A outputs. For data transfer in the A-to-B direction, a two-stage pipeline is provided in the A-to-1B path,

DGG OR DL PACKAGE (TOP VIEW)

5=-	١.	U		h
OEA [OEB
CLKEN1B [CLKENA2
2B3 [54	2B4
GND [GND
2B2 [2B5
2B1 [51	2B6
v _{cc} [7			v _{cc}
A1 [8			2B7
A2 [9		48] 2B8
A3 [10		47	2B9
GND [46	GND
A4 [2B10
A5 [13			2B11
A6 [2B12
A7 [] 1B12
A8 [16		41] 1B11
A9 [] 1B10
GND [GND
A10 [19		38] 1B9
A11 [37] 1B8
A12 [36] 1B7
v _{cc} [22		35]v _{cc}
1B1 [] 1B6
1B2 [] 1B5
GND [32] GND
1B3 [26		31] 1B4
CLKEN2B [30	CLKENAT
SEL [28		29	CLK

with a single storage register in the A to 2B path. Proper control of the CLKENA inputs allows two sequential 12-bit words to be presented synchronously as a 24-bit word on the B port. Data flow is controlled by the active-low output enables (OEA, OEB). The control terminals are registered to synchronize the bus direction changes with CLK.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16270 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16270 is characterized for operation from -40°C to 85°C.

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SCES028 - JULY 1995

Function Tables

OUTPUT ENABLE

	INPUTS		OUTPUTS			
CLK	CLK OEA OEB		Α	1B, 2B		
1	Н	Н	Z	Z		
1	Н	L	z	Active		
1	L	н	Active	Z		
1	L	L	Active	Active		

A-TO-B STORAGE (OEB = L)

	INPUTS			OUT	PUTS
CLKENA1	CLKENA2	CLK	Α	1B	2B
L	Н	1	L	L†	2B ₀ ‡
L	Н	1	Н	н†	2B ₀ ‡
L	L	1	L	L†	L
L.	L	1	Н	н†	н
Н	L	1	L	1B ₀ ‡	L
Н	L	1	Н	1B ₀ ‡	н
н	Н	X	X	1B ₀ ‡	2B ₀ ‡

[†] Two CLK edges are needed to propagate data.

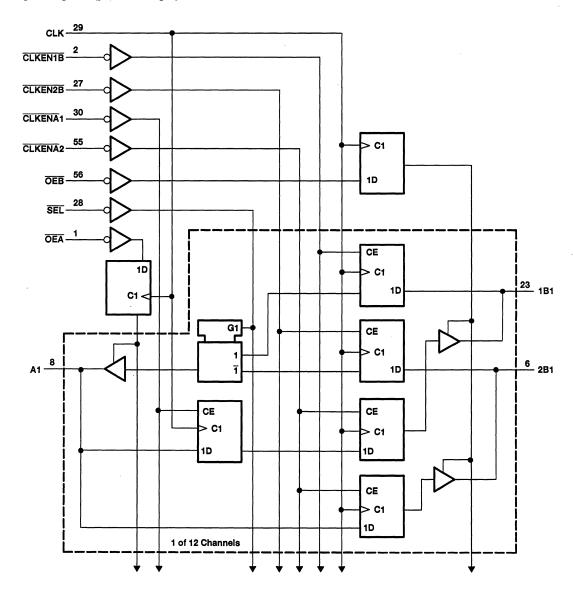
B-TO-A STORAGE (OEA = L)

	1	NPUTS				OUTPUT
CLKEN1B	CLKEN2B	CLK	SEL	1B	2B	A
Н	X	Х	Н	Х	X	A ₀ ‡
х	Н	Χ	L	X	Χ	A ₀ ∓ A ₀ ‡
L	Х	1	н	L	Χ	L
L	Х	1	н	Н	Χ	н
Х	L	1	L	Χ	L	L
X	L	1	L	Х	Н	Н

[‡]Output level before the indicated steady-state input conditions were established

[‡]Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)





SN74ALVCH16270 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES028 - JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, VI: Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	$5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{ K }(V_1 < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range, T _{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	٧
V	Link level incut valence	V _{CC} = 2.3 V to 2.7 V	1.7		V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
V.,	Low lovel input veltage	V _{CC} = 2.3 V to 2.7 V		0.7	V
VIL	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	· ·
V_{l}	Input voltage		0	Vcc	V
٧o	Output voltage		0	Vcc	. V
		V _{CC} = 2.3 V		-12	
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 2.3 V		12	
loL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN74ALVCH16270 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS SCES028 - JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST C	ONDITIONS	vcct	MIN	TYP‡	MAX	UNIT	
		I _{OH} = -100 μA		MIN to MAX	V _{CC} -0	.2			
		I _{OH} = -6 mA,	V _{IH} = 1.7 V	2.3 V	2				
			V _{IH} = 1.7 V	2.3 V	1.7			v	
VOH		I _{OH} = -12 mA	V _{IH} = 2 V	2.7 V	2.2			V	
			V _{IH} = 2 V	3 V	2.4				
		I _{OH} = -24 mA,	V _{IH} = 2 V	3 V	2				
		I _{OL} = 100 μA		MIN to MAX			0.2		
v _{OL}	I _{OL} = 6 mA,	V _{IL} = 0.7 V	2.3 V			0.4			
		l	V _{IL} = 0.7 V	2.3 V			0.7	V	
	I _{OL} = 12 mA	V _{IL} = 0.8 V	2.7 V			0.4			
		I _{OL} = 24 mA,	OL = 24 mA, V _{IL} = 0.8 V				0.55		
Ц		V _I = V _{CC} or GND		3.6 V			±5	μА	
		V _I = 0.7 V		001/	45				
		V _I = 1.7 V		2.3 V	-45				
l(hold)		V _I = 0.8 V		3 V	75			μА	
		V _I = 2 V]	<i>–</i> 75				
		V _I = 0 to 3.6 V		3.6 V			±500		
I _{OZ} §		VO = VCC or GND		3.6 V			±10	μА	
lcc		V _I = V _{CC} or GND,	IO = 0	3.6 V			40	μА	
ΔICC		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ	
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V		3.5		pF	
C _{io}	A or B ports	VO = VCC or GND		3.3 V		9		pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions. ‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. § For I/O ports, the parameter I_{OZ} includes the input leakage current.

SN74ALVCH16270 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES028 - JULY 1995

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		,	V _{CC} =		V _{CC} =	2.7 V	V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		- 0	150	0	150	0	150	MHz
t _W	Pulse duration, CLK high or low				3.3		3.3		ns
	Setup time	A data before CLK↑	4.1		3.8		3.1		
		B data before CLK↑	0.9		1.2		0.9		
tsu		CLKENA1 or CLKENA2 before CLK↑	3.5		3.2		2.7		ns
		CLKEN1B or CLKEN2B before CLK↑	3.4		. 3		2.6		
		OE data before CLK↑	4.4		3.9		3.2		
		A data after CLK↑	0		0		0.2		
		B data after CLK↑	1.4		1		1.7		1
th	Hold time	CLKENA1 or CLKENA2 after CLK↑	0		0.1		0.3		ns
		CLKEN1B or CLKEN2B after CLK↑	0		. 0		0.6		1
		OE after CLK↑	0		0		0.1		,

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

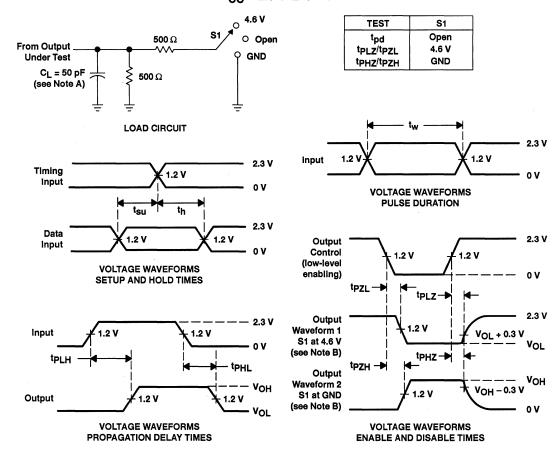
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	V _{CC} = 2.5 V ± 0.2 V		2.7 V	V _{CC} = 3.3 V ± 0.3 V		UNIT
	(1141-01)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			150		150		150		MHz
	CLK	В	2	6.5		5.8	1.1	5.1	
t _{pd}	CLK	Α	1.7	6		5.4	1	4.7	ns
	SEL	Α	1.9	6.8		6.4	1	5.5	
^t en	CLK	A or B	1.6	7.5		6.8	1	6	ns
^t dis	CLK	A or B	2.6	7.4		6.5	1.1	5.8	ns

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNÍT
<u> </u>	Power dissination conscitance	Outputs enabled	C: 50 pF 4 10 MH=	87	120	
C _{pd}	Power dissipation capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	80.5	118	pF

SCES028 - JULY 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

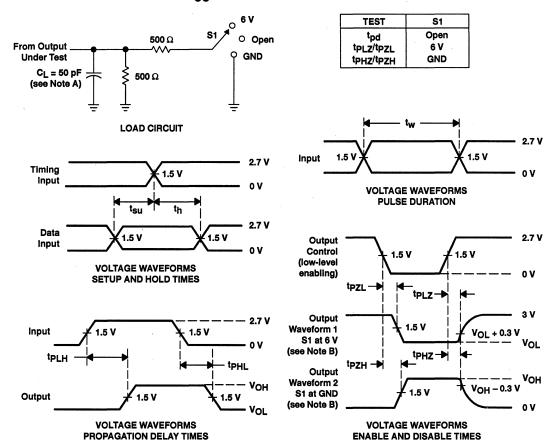


- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \, \Omega$, $t_f \leq 2.5 \, \text{ns}$, $t_f \leq 2.5 \, \text{ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpHL and tpLH are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SCES028 - JULY 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \, \Omega$, $t_f \leq 2.5 \, ns$, $t_f \leq 2.5 \, ns$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tplz and tpHz are the same as tdis.
 - F. tpZL and tpZH are the same as ten.
 - G. tpHL and tpLH are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

SN74ALVCH16271 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS

- **Member of the Texas Instruments** Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Packaged in Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) **Packages**

description

This 12-bit to 24-bit bus exchanger is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16271 is intended for applications where two separate datapaths must be multiplexed onto, or demultiplexed from, a single datapath. This device is particularly suitable as an interface between conventional DRAMs and high-speed microprocessors.

A data is stored in the internal A-to-B registers on the low-to-high transition of the clock (CLK) input, provided that the CLKENA inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B port.

Transparent latches in the B-to-A path allow asynchronous operation in order to maximize memory access throughput. These latches transfer data when the latch-enable (LE) inputs are low. The select (SEL) line selects 1B or 2B data for the A outputs. Data flow is controlled by the active-low output enables (OEA, OEB).

DGG OR DL PACKAGE (TOP VIEW)

C	l	U		h
OEA [_	56	OEB
LE1B				CLKENA2
2B3 [3		54] 2B4
GND [53	GND
2B2 [52] 2B5
2B1 [6		51	2B6
v _{cc} [7		50	v _{cc}
A1 [8		49	ll 2B7
A2 [9		48	D 2B8
A3 [10		47] 2B9
GND [11		46	II GND
A4 [12		45	2B10
A5 [A6 [13		44	2B11
A6 [14		43] 2B12
A7 [15		42] 1B12
A8 [16		41	T 1B11
A9 [17		40	1B10
GND [18		39	GND
A10 [19		38	1B9
A11 [37	1B8
A12 [21		36] 1B7
v _{cc} [22		35	v _{cc}
1B1 [23		34] 1B6
1B2 [33] 1B5
GND [25		32	GND
1B3 [31] 1B4
LE2B	27			CLKENA1
SEL [CLK

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16271 is available in Tl's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

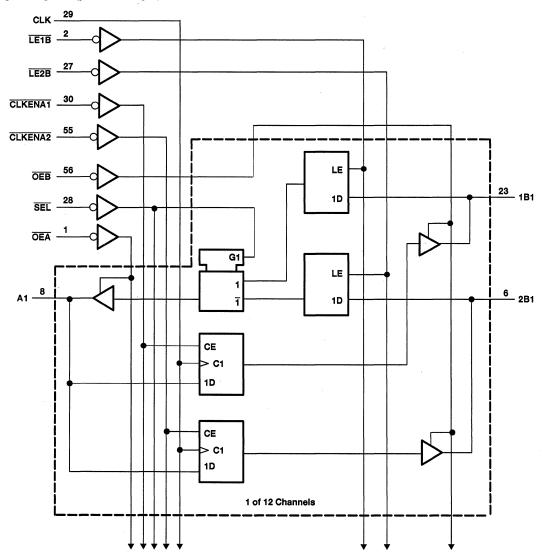
The SN74ALVCH16271 is characterized for operation from -40°C to 85°C.

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SN74ALVCH16271 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS SCES017 - JULY 1995

logic diagram (positive logic)





SN74ALVCH16271 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER **WITH 3-STATE OUTPUTS**

SCES017 - JULY 1995

Function Tables OUTPUT ENABLE

INP	UTS	OUTI	PUTS
OEA OEB		Α	1B, 2B
Н	Н	Z	Z
Н	L	Z	Active
L	Н	Active	Z
L	L	Active	Active

A-TO-B STORAGE (OEB = L)

	INPUTS				
CLKENA1	CLKENA2	CLK	Α	1B	2B
Н	Н	Х	Х	1B ₀ †	2B ₀ †
L	Х	1	L	L	Χ
L	Χ	1	Н	Н	Χ
х	L	1	L	Х	L
х	L	1	Н	A ₀	Н

B-TO-A STORAGE ($\overline{OEA} = L$)

	INPL	OUTPUT		
LE	SEL	1B	2B	Α
Н	Х	Х	Х	A ₀ † A ₀ †
Н	X	Χ	Χ	. A ₀ †
L	Н	L	X	L
L	Н	Н	X	н
L	L	Χ	L	L
L	L	Х	Н	н

[†] Output level before the indicated steady-state input conditions were established

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, VI: Except I/O ports (see Note 1)	0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, $I_{ K }(V_1 < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	: 1 W
DL package	1.4 W
Storage temperature range, Teta	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.



SN74ALVCH16271 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES017 - JULY 1995

recommended operating conditions (see Note 4)

	•	(MIN	MAX	UNIT	
Vcc	Supply voltage		2.3	3.6	V	
V	High level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7		v	
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	
V	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V		0.7	v	
VIL	VIL CON-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	ľ	
۷Į	Input voltage		0	VCC	V	
Vo	Output voltage		0	Vcc	٧	
		V _{CC} = 2.3 V		-12		
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA	
		V _{CC} = 3 V		-24		
		V _{CC} = 2.3 V		12		
lol	Low-level output current	V _{CC} = 2.7 V		12	mA	
		V _{CC} = 3 V		24	İ	
Δt/Δν	Input transition rise or fall rate		0	10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CO	v _{cc} †	MIN	TYP‡	MAX	UNIT	
		I _{OH} = -100 μA	*	MIN to MAX	V _{CC} -0	.2		
		I _{OH} = -6 mA,	V _{IH} = 1.7 V	2.3 V	2			
			V _{IH} = 1.7 V	2.3 V	1.7			v
VOH		I _{OH} = -12 mA	V _{IH} = 2 V	2.7 V	2.2			V
		1	V _{IH} = 2 V	3 V	2.4			
		I _{OH} = -24 mA,	V _{IH} = 2 V	3 V	2			
		I _{OL} = 100 μA		MIN to MAX			0.2	
		I _{OL} = 6 mA,	V _{IL} = 0.7 V	2.3 V			0.4	
VOL		la. 10 mA	V _{IL} = 0.7 V	2.3 V			0.7	v
		I _{OL} = 12 mA	V _{IL} = 0.8 V	2.7 V			0.4	
		I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V			0.55	
11		V _I = V _{CC} or GND		3.6 V			±5	μА
		V _I = 0.7 V V _I = 1.7 V		2.3 V	45			
				2.3 V	-45			
I(hold)		V _I = 0.8 V		0.1/	75			1 μΑ
		V _I = 2 V		3 V	-75			
		V _I = 0 to 3.6 V		3.6 V			±500	
I _{OZ} §		VO = VCC or GND		3.6 V			±10	μΑ
Icc		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			40	μА
Δlcc		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V		·		pF
Cio	A or B ports	VO = VCC or GND		3.3 V				pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[§] For I/O ports, the parameter IOZ includes the input leakage current.



[‡] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

SN74ALVCH16272 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS

DGG OR DL PACKAGE (TOP VIEW)

SCES057 - OCTOBER 1995

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- **Bus Hold on Data Inputs Eliminates** the Need for External Pullup/Pulldown Resistors
- Packaged in Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) **Packages**

description

This 12-bit to 24-bit bus exchanger is designed for 2.3-V to 3.3-V V_{CC} operation.

The SN74ALVCH16272 is intended for applications where two separate datapaths must be multiplexed onto, or demultiplexed from, a single datapath. This device is particularly suitable as an interface between conventional DRAMs and high-speed microprocessors.

Data from the A inputs is stored in the internal registers on the low-to-high transition of the clock (CLK) input, when the CLKENA inputs are low. A two-stage pipeline is provided in each of the A-to-1B and A-to-2B paths to serve as a shallow write buffer.

Transparent latches are provided in the B-to-A path to allow asynchronous operation to maximize memory access throughput. These latches transfer data when the latch-enable (LE) inputs are low. The select (SEL) line selects 1B or 2B data for the A outputs. Data flow is controlled by the active-low output enables (OEA, OEB).

d₁	\cup_{56}	OEB
2		CLKENA2
[]3	54	2B4
[]₄	53	GND
[[5	52	2B5
[]6	51	2B6
] 7		2 v _{cc}
] 8		2B7
		2B8
		GND
_	45	2B10
[] 13		2B11
] 14		2B12
15		P
_		
_	40] 1B10
_		GND
_] 1B9
3		E
21] 1B7
3		□ v _{cc}
<u>J</u> 23	34] 1B6
	2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 19 20	2 55 3 54 4 53 5 52 6 51 7 50 8 49 9 48 10 47 11 46 112 45 113 44 114 43 115 42 116 41 117 40 118 39 119 38 120 37 121 36 122 35

33 1B5

32 GND

29]] CLK

1B4

CLKENA1

1B2 []24

GND 1 25

1B3 [26

LE2B 127

SEL | 28

To ensure the high-impedance state during power up or power down, $\overline{\sf OE}$ should be tied to ${\sf V}_{\sf CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

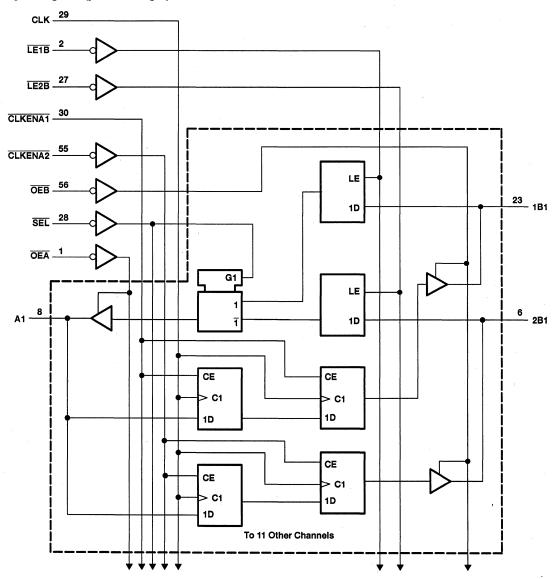
The SN74ALVCH16272 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16272 is characterized for operation from -40°C to 85°C.

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logic diagram (positive logic)





PRODUCT PREVIEW

PRODUCT PREVIEW

Function Tables

OUTPUT ENABLE

INP	UTS	OUT	PUTS
OEA OEB		Α	1B, 2B
Н	Н	Z	Z
Н	L	z	Active
L	Н	Active	Z
L	L	Active	Active

A-TO-B STORAGE (OEB = L)

	INPUTS					
CLKENA1	CLKENA2	CLK	Α	1B	2B	
Н	Н	Х	Х	1B ₀ †	2B ₀ †	
L	Χ	1	L	L†	X	
L	Χ	1	Н	H [†]	Χ	
x	L	1	L	х	L	
х	L	1	Н	A ₀	, H	

†Two CLK edges are needed to propagate data.

B-TO-A STORAGE (OEA = L)

	INP	OUTPUT		
LE	SEL	1B	2B	A
Н	Х	Х	Х	A ₀ ‡
Н	Х	X	Χ	A ₀ ‡
L	Н	L	Χ	L
L	Н	Н	Х	Н
L	L	Χ	L	L
L	L,	Χ	Н	н

‡ Output level before the indicated steady-state input conditions were established

SN74ALVCH16272 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES057 - OCTOBER 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, VI: Except I/O ports (see Note 1)	0.5 V to 4.6 V
I/O ports (see Notes 1 and 2) –	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2) –	0.5 V to V _{CC} + 0.5 V
Input clamp current, $I_{ K }(V_1 < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range, T _{stg}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		2.3	3.6	٧
	High level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7		V
VН	VIH High-level input voltage VIL Low-level input voltage VI Input voltage VO Output voltage OH High-level output current OL Low-level output current	V _{CC} = 2.7 V to 3.6 V	2		v
V.,	Low level input veltage	V _{CC} = 2.3 V to 2.7 V		0.7	v
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	\ \
VI	Input voltage		0	Vcc	٧
Vo	Output voltage		0	-V _C C	٧
		V _{CC} = 2.3 V		-12	
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 2.3 V		12	
IOL	Low-level output current	$V_{CC} = 2.7 \text{ V}$		12	mA
		V _{CC} = 3 V		24	
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

^{3.} The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

SN74ALVCH16272 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS

SCES057 - OCTOBER 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CO	ONDITIONS	vcct	MIN	TYP‡	MAX	UNIT
		IOH = -100 μA		MIN to MAX	V _{CC} -0.	2		
		I _{OH} = -6 mA,	V _{IH} = 1.7 V	2.3 V	2			
\ _{V=}			V _{IH} = 1.7 V	2.3 V	1.7			v
VOH		IOH = -12 mA	V _{IH} = 2 V	2.7 V	2.2			V
		,	V _{IH} = 2 V	3 V	2.4			
		I _{OH} = -24 mA,	V _{IH} = 2 V	3 V	2			
		I _{OL} = 100 μA		MIN to MAX			0.2	
İ		I _{OL} = 6 mA,	V _{IL} = 0.7 V	2.3 V			0.4	
VOL	IOL = 12 MA	V _{IL} = 0.7 V	2.3 V			0.7	V	
		V _{IL} = 0.8 V	2.7 V			0.4		
		I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V			0.55	
lj.		V _I = V _{CC} or GND		3.6 V			±5	μА
		V _I ≈ 0.7 V		0.01/	45			
		V _I = 1.7 V		2.3 V	-45			
l(hold)		V _I = 0.8 V		3 V	75			μА
		V _j = 2 V]	-75			
		V _I = 0 to 3.6 V		3.6 V			±500	
I _{OZ} §		VO = VCC or GND		3.6 V			±10	μА
Icc		$V_I = V_{CC}$ or GND,	IO = 0	3.6 V			40	μА
∆lcc		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V				pF
Cio	A or B ports	VO = VCC or GND		3.3 V				pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C. § For I/O ports, the parameter I_{OZ} includes the input leakage current.

ADVANCE INFORMATION

- **Member of the Texas Instruments** Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 1-bit-to-4-bit address driver is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16344 is used in applications where four separate memory locations must be addressed by a single address.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN74ALVCH16344 is packaged in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ALVCH16344 is characterized for operation from -40°C to 85°C.

DGG OR DL PACKAGE (TOP VIEW)

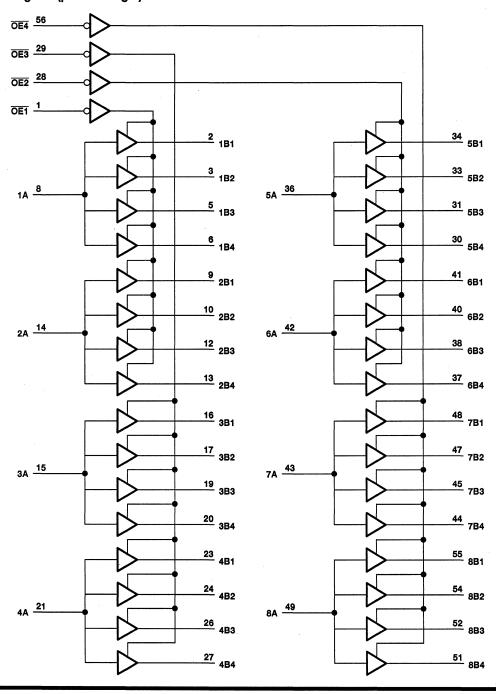
		$\tau \tau$,	
OE1	1	_	56	OE4
1B1 [2			8B1
1B2 [3			8B2
GND [4		53	GND
1B3 [5			BB3
1B4 [6		51	8B4
v _{cc} [7		50	v _{cc}
1A [8		49	П 8А
2B1 [48	7B1
2B2 [47	7B2
GND [11		46	GND 7B3
2B3 [45	7B3
2B4 [44	7B4 7A 6A
2A [43	7A
3А [42	[] 6A
	16		41	∐ 6B1
3B2 [40	6B2
GND [39	GND
звз [38	6B3
3B4 [20		37] 6B4
	21		36] 5A
v _{cc} [22		35	v _{cc}
	23		34	5B1
4B2 [33	5B2
GND [32	GNE
4B3 [31	5B3
	27		30	5B4
OE2	28		29	OE3

FUNCTION TABLE

INP	JTS	OUTPUT
OE	Α	Bn
L	Н	Н
L	L	L
Н	Н	Z

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logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}		-0.5 V to	4.6 V
Input voltage range, V _I (see Note 1)			
Output voltage range, Vo (see Notes 1 and 2)			
Input clamp current, I_{ik} ($V_i < 0$)			
Output clamp current, IOK (VO < 0 or VO > VCC)			
Continuous output current, I_O ($V_O = 0$ to V_{CC})			
Continuous current through each VCC or GND			
Maximum power dissipation at $T_{\Delta} = 55^{\circ}$ C (in still air) (see Note 3): DG			
, , , , , , , , , , , , , , , , , , , ,	package		
Storage temperature range, T _{sto}			

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	V
V	Lligh level input veltage	V _{CC} = 2.3 V to 2.7 V	1.7		V
VIH	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
V.,	Level level innet valte as	V _{CC} = 2.3 V to 2.7 V		0.7	V
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
٧١	Input voltage		0	Vcc	٧
Vo	Output voltage		0	Vcc	V
		V _{CC} = 2.3 V		-12	
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 2.3 V		12	
lol	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	•c

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

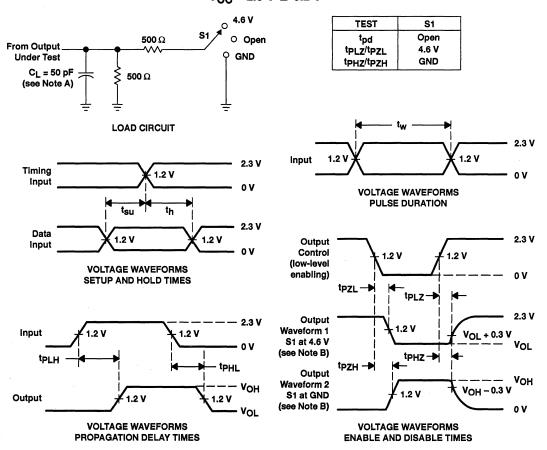
PA	RAMETER	TEST CO	ONDITIONS	vcct	MIN	TYP‡	MAX	UNIT	
		I _{OH} = -100 μA		MIN to MAX	VCC-0	.2			
		I _{OH} = -6 mA,	V _{IH} = 1.7 V	2.3 V	2				
,, .			V _{IH} = 1.7 V	2.3 V	1.7			V	
VOH	vOH	I _{OH} = -12 mA	V _{IH} = 2 V	2.7 V	2.2			V	
		V _{IH} = 2 V	3 V	2.4					
		I _{OH} = -24 mA,	V _{IH} = 2 V	3 V	2				
		I _{OL} = 100 μA		MIN to MAX			0.2	2	
		I _{OL} = 6 mA,	V _{IL} = 0.7 V	2.3 V			0.4		
VOL		1 10 4	V _{IL} = 0.7 V	2.3 V			0.7	7 V	
	I _{OL} = 12 mA	V _{IL} = 0.8 V	2.7 V			0.4			
		$I_{OL} = 24 \text{ mA},$ $V_{IL} = 0.8 \text{ V}$		3 V			0.55		
l _l		V _I = V _{CC} or GND		3.6 V			±5	μА	
		V _I = 0.7 V		2.3 V	45				
		V _i = 1.7 V		2.3 V	-45				
I(hold)		V _I = 0.8 V		3 V	75			μА	
		V _I = 2 V] 3 V	-75				
		V _I = 0 to 3.6 V		3.6 V			±500		
loz		VO = VCC or GND		3.6 V			±10	μА	
Icc		V _I = V _{CC} or GND,	IO = 0	3.6 V			40	μА	
Δlcc		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА	
<u></u>	Control inputs	V. Vaa er CND		3.3 V		3.5			
Ci	Data inputs	VI = VCC or GND		3.3 V		6		pF	
Co	Outputs	V _I = V _{CC} or GND		3.3 V		7		pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SCES054 - SEPTEMBER 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



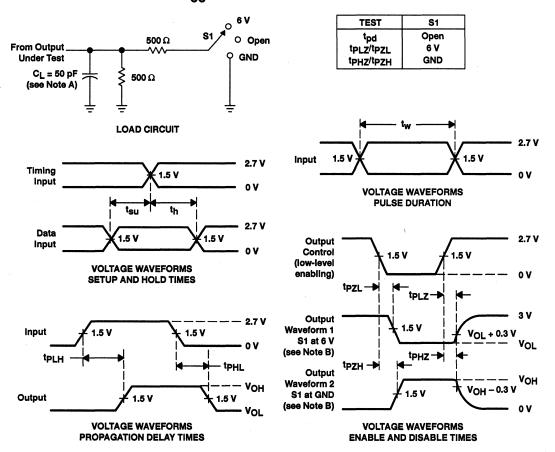
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_f \leq 2.5 \,\text{ns}$, $t_f \leq 2.5 \,\text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpHL and tpLH are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SCES054 - SEPTEMBER 1995

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V } \pm 0.3 \text{ V}$



- NOTES: A. C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpHL and tpLH are the same as tod.

Figure 2. Load Circuit and Voltage Waveforms

SN74ALVCH16373 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCES020 - JULY 1995

 Member of the Texas Instruments Widebus™ Family 		R DL PAC TOP VIEW	
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	1 <u>0E</u>		1LE
ESD Protection Exceeds 2000 V Per	1Q1 [] 1Q2 []		1D1 1D2
MIL-STD-833C, Method 3015; Exceeds	GND [GND
200 V Using Machine Model	1Q3 [1D3
(C = 200 pF, R = 0)	104		1D4
Latch-Up Performance Exceeds 250 mA	v _{cc}]		V _{CC}
Per JEDEC Standard JESD-17	105		1D5
Bus Hold on Data Inputs Eliminates the	1Q6 🛚	9 40	D 1D6
Need for External Pullup/Pulldown	GND 🛚		GND
Resistors	1Q7 🛭		D7 1D7
Package Options Include Plastic 300-mil	1Q8 🏻	12 37	1D8
Shrink Small-Outline (DL) and Thin Shrink	2Q1 🏻		2D1
Small-Outline (DGG) Packages	2Q2 L		2D2
description	GND [15 34	GND
description	2Q3 [2D3
This 16-bit transparent D-type latch is designed	2Q4 [2D4
for 2.3-V to 3.6-V V _{CC} operation.	v _{cc} [10 31	V _{CC} 2D5
The SN74ALVCH16373 is particularly suitable	2Q5 [2Q6 [2D6
for implementing buffer registers, I/O ports,	GND [GND
bidirectional bus drivers, and working registers.	2Q7 [2D7
This device can be used as two 8-bit latches or	2Q8 [2D8
one 16-bit latch. When the latch-enable (LE) input	2 0E []		2LE
is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched			Γ

A buffered output-enable (OE) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. OE does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16373 is available in Tl's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16373 is characterized for operation from -40°C to 85°C.

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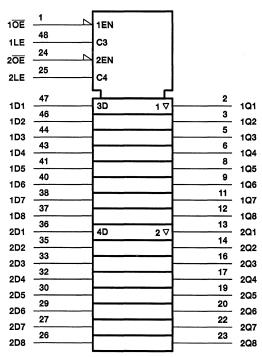
at the levels set up at the D inputs.

SCES020 - JULY 1995

FUNCTION TABLE (each 8-bit section)

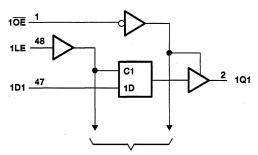
	INPUTS	OUTPUT	
0E	LE	D	Q
L	Н	Н	Η ,
L	Н	L	L
L	L	Χ	Q ₀
Н	X	Χ	Z

logic symbol†

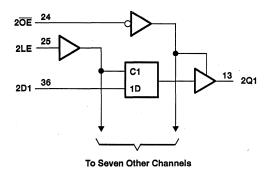


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels



SN74ALVCH16373 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCES020 - JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} Input voltage range, V _I (see Note 1) Output voltage range, V _O (see Notes 1 and 2) Input clamp current, I _{IK} (V _I < 0) Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC}) Continuous output current, I _O (V _O = 0 to V _{CC}) Continuous current through each V _{CC} or GND	-0.5 V to 4.6 V -0.5 V to V _{CC} + 0.5 V -50 mA ±50 mA ±50 mA ±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DG	G package 0.85 W package 1.2 W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	V
\ /	Ligh level input veltage	V _{CC} = 2.3 V to 2.7 V	1.7		V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		ľ
V	Low-level input voltage			0.7	V
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	L v
۷į	Input voltage		0	VCC	V
V _O	Output voltage		0	VCC	٧
		V _{CC} = 2.3 V		-12	
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 2.3 V		12	
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA
·OL		V _{CC} = 3 V		24	ĺ
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN74ALVCH16373 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCES020 - JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P/	RAMETER	TEST C	ONDITIONS	vcct	MIN	TYP‡	MAX	UNIT	
		I _{OH} = -100 μA		MIN to MAX	VCC-C).2		-	
		I _{OH} = -6 mA	V _{IH} = 1.7 V	2.3 V	2				
l.,			V _{IH} = 1.7 V	2.3 V	1.7			v	
VOH		I _{OH} = -12 mA	V _{IH} = 2 V	2.7 V	2.2			V	
			V _{IH} = 2 V	3 V	2.4				
		I _{OH} = -24 mA	V _{IH} = 2 V	3 V	2				
		I _{OL} = 100 μA		MIN to MAX			0.2		
		I _{OL} = 6 mA	V _{IL} = 0.7 V	2.3 V			0.4		
VOL		I _{OL} = 12 mA	V _{IL} = 0.7 V	2.3 V			0.7	٧	
		IOL = 12 mA	V _{IL} = 0.8 V	2.7 V			0.4		
		I _{OL} = 24 mA	V _{IL} = 0.8 V	3 V			0.55		
l _l		V _I = V _{CC} or GND	·	3.6 V			±5	μА	
		V _I = 0.7 V V _I = 1.7 V		2.3 V	45	* .			
				3 V	-45				
I _{I(hold)}		V _I = 0.8 V		3 V	75			μА	
		V _i = 2 V	*	3 V	-75				
		V _I = 0 to 3.6 V		3.6 V			±500	0	
loz		VO = VCC or GND		3.6 V			±10	μΑ	
Icc		V _I = V _{CC} or GND,	IO = 0	3.6 V			40	μА	
Δlcc		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА	
C.	Control inputs	Vi - Voo or GND		3.3 V		3		nE.	
Ci	Data inputs	V _I = V _{CC} or GND				6		pF	
Со	Outputs	VO = VCC or GND		3.3 V		7		pF	

[†] For conditions shown as MIN or MAX use the appropriate values under recommended operating conditions.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

		V _{CC} = 2.5 \ ± 0.2 V	/ vcc	V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V	
		MIN MA	X MIN	MAX	MIN	MAX	
t _W	Pulse duration, LE high or low	3.3	3.3		3.3		ns
t _{su}	Setup time, data before LE↓	1	1		1.1		ns
th	Hold time, data after LE↓	1.5	1.7		1.4		ns

[‡] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

SN74ALVCH16373 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS SCES020 - JULY 1995

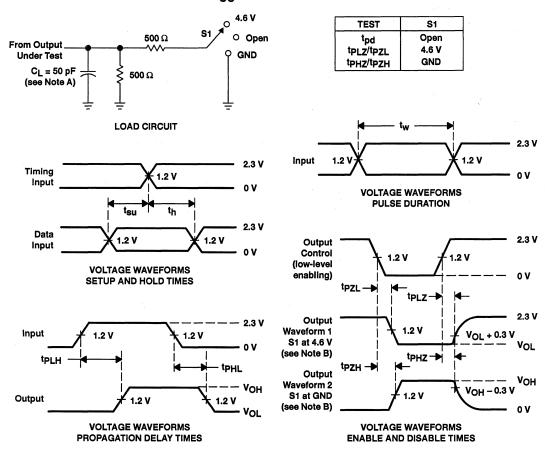
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM	TO	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
	(INPUT) (OUTPUT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	
	D	Q	1	5.1		4.3	1.1	3.6	
^t pd	LE	Q	1	5.5		4.6	1	3.9	ns
t _{en}	ŌĒ	Q	1	6.5		5.7	1	4.7	ns
^t dis	ŌĒ	Q	1.9	5.3		4.5	1.4	4.1	ns

operating characteristics, $T_A = 25$ °C

	PARAMETER		TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT	
				TYP	TYP		
C .	Power dissipation capacitance	Outputs enabled	C ₁ = 50 pF, f = 10 MHz	19	22	pF	
C _{pd}		Outputs disabled	C _L = 50 pF, f = 10 MHz	4	5	pr	

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$



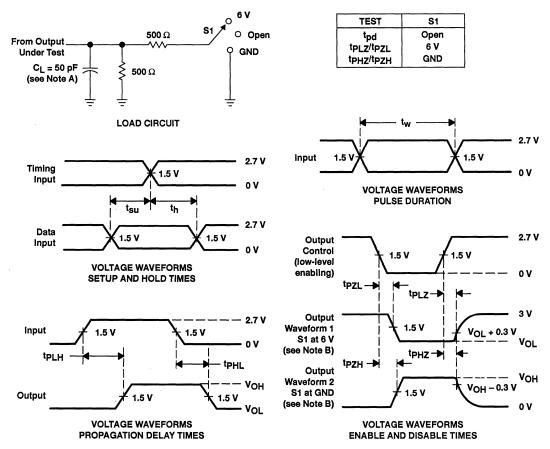
NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms

SCES020 - JULY 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \Omega$, $t_{f} \leq 2.5 \text{ ns.}$ tf $\leq 2.5 \text{ ns.}$
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

SN74ALVCH16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCES021 - JULY 1995

 Member of the Texas Instruments Widebus™ Family 	DGG OR DL PACKAGE (TOP VIEW)			
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	10E 1	48 1CLK		
 ESD Protection Exceeds 2000 V Per MIL-STD-833C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0) 	1Q1 [2 1Q2 [3 GND [4 1Q3 [5	47 1D1 46 1D2 45 GND 44 1D3		
 Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17 	1Q4 []6 V _{CC} []7 1Q5 []8	43 1 1D4 42 1 V _{CC} 41 1 1D5		
 Bus Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors 	1Q6 [9 GND [10 1Q7 [11	40 1 1D6 39 1 GND 38 1 1D7		
 Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages 	1Q8	37 1 1D8 36 2D1 35 2D2		
description	GND (15 2Q3 (16	34] GND 33] 2D3		
This 16-bit edge-triggered D-type flip-flop is designed for 2.3-V to 3.6-V $\rm V_{CC}$ operation.	2Q4 [] 17 V _{CC} [] 18 2Q5 [] 19	32 2D4 31 V _{CC} 30 2D5		
The SN74ALVCH16374 is particularly suitable for implementing buffer registers, I/O ports,	2Q6 [20 GND [21	29 2D6 28 GND		
bidirectional bus drivers, and working registers. It can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock	2Q7 [] 22 2Q8 [] 23 2 OE [] 24	27 2D7 26 2D8 25 2CLK		
(CLK) input, the Q outputs of the flip-flop take on	<u> </u>			

can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. \overline{OE} does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16374 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16374 is characterized for operation from -40°C to 85°C.

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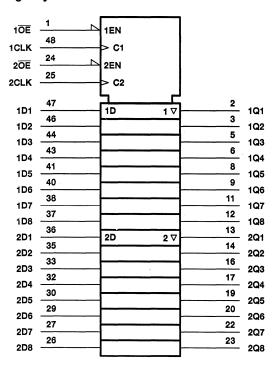
the logic levels set up at the data (D) inputs. OE)



FUNCTION TABLE (each flip-flop)

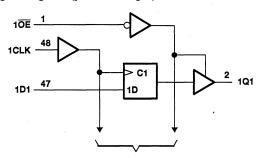
	INPUTS	OUTPUT	
ŌĒ	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	H or L	Х	Q ₀
Н	X	Х	z

logic symbol†

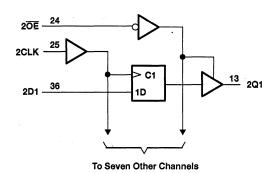


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels



SN74ALVCH16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCES021 - JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	
Continuous current through each V _{CC} or GND	
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): DGG pa	
DL pack	kage 1.2 W
Storage temperature range, Teta	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	V
V	High level input valence	V _{CC} = 2.3 V to 2.7 V	1.7		V
VIH VIL VI VO	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		V
Viii	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V		0.7	V
۷IL	Low-level input voitage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	v
٧١	Input voltage		0	VCC	٧
Vo	Output voltage		0	Vcc	V
		V _{CC} = 2.3 V		-12	
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 2.3 V		12	
loL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN74ALVCH16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCES021 - JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST C	ONDITIONS	v _{cc} †	MIN	TYP‡	MAX	UNIT
		I _{OH} = -100 μA		MIN to MAX	VCC-0).2		
		I _{OH} = -6 mA,	V _{IH} = 1.7 V	2.3 V	2			
			V _{IH} = 1.7 V	2.3 V	1.7			v
VOH		I _{OH} = -12 mA	V _{IH} = 2 V	2.7 V	2.2			V
		V _{IH} = 2 V	3 V	2.4				
	IOH = -24 mA,	V _{IH} = 2 V	3 V	2				
		I _{OL} = 100 μA		MIN to MAX			0.2	
		I _{OL} = 6 mA,	V _{IL} = 0.7 V	2.3 V			0.4	
VOL		I _{OL} = 12 mA,	V _{IL} = 0.7 V	2.3 V			0.7	v
	I _{OL} = 12 mA,	V _{IL} = 0.8 V	2.7 V			0.4		
		I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V			0.55	1
lį		V _I = V _{CC} or GND		3.6 V			±5	μА
		V _I = 0.7 V		2.3 V	45			
		V _I = 1.7 V		2.3 V	-45			
I(hold)		V _I = 0.8 V	·	3 V	75			μA
		V _I = 2 V		3 V	-75			
		V _I = 0 to 3.6 V		3.6 V			±500	
loz		VO = VCC or GND		3.6 V			±10	μА
Icc		V _I = V _{CC} or GND,	IO = 0	3.6 V			40	μΑ
∆lcc		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА
C.	Control inputs	VI = VCC or GND		3.3 V		3		. pF
Ci	Data Inputs	A1 = ACC OLGIAD		3.3 V		.6		þΓ
Co	Outputs	VO = VCC or GND		3.3 V		. 7		pF

[†] For conditions shown as MIN or MAX use the appropriate values under recommended operating conditions.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

		V _{CC} = ± 0.		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency	0	150	0	150	0	150	MHz
t _w	Pulse duration, CLK high or low	3.3		3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	2.1		2.2		1.9		ns
t _h	Hold time, data after CLK↑	0.6		0.5		0.5		ns

[‡] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

SN74ALVCH16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCES021 - JULY 1995

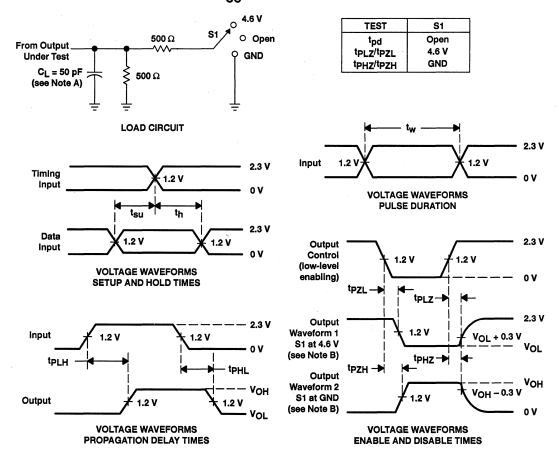
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO	V _{CC} =	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V	
	(INPO1)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			150		150		150		MHz
^t pd	CLK	Q	1	5.9		4.9	1	4.2	ns
^t en	CLK	Q	1	6.7		5.9	1	4.8	ns
^t dis	CLK	Q	1.7	5.5		4.7	1.2	4.3	ns

operating characteristics, T_A = 25°C

	PARAMETER		TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V TYP	V _{CC} = 3.3 V ± 0.3 V	UNIT	
	Power dissination especitance	Outputs enabled	C ₁ = 50 pF. f = 10 MHz	31	30	ρF	
□□pd	C _{pd} Power dissipation capacitance	Outputs disabled	C _L = 50 pF, f = 10 MHz	16	18	Pr	

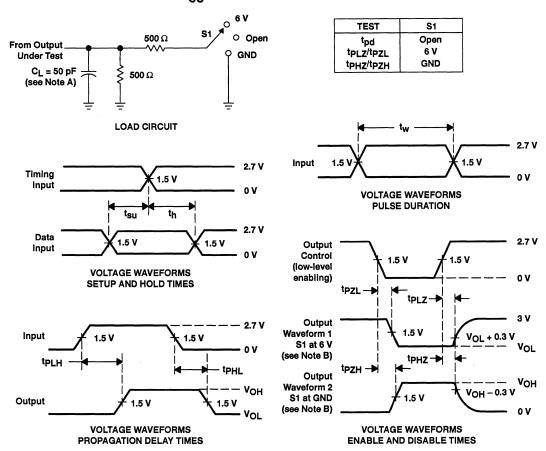
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - The outputs are measured one at a time with one transition per measurement.
 - E. tpl 7 and tpH7 are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V}$ AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns. $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tp71 and tp7H are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

2A9 🛮 26

SEL1 127

SEL2 28

31 2B9

30 N SEL4

29 SEL3

SCES022 - JULY 1995

 Member of the Texas Instruments Widebus+™ Family 	DGG OR DL PACKAGE (TOP VIEW)
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	PRE 1 56 CLK SELO 2 55 SELEN
 UBE™ (Universal Bus Exchanger) Allows Synchronous Data Exchange 	1A1 3 54 1B1 GND 4 53 1 GND
 ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model 	1A2 0 5 52 1 1B2 1A3 0 6 51 1 1B3
(C = 200 pF, R = 0)	V _{CC}
 Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17 	1A5 9 48 1 1B5 1A6 10 47 1 1B6
 Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors 	GND 111 46 GND 1A7 12 45 1B7 1A8 13 44 1B8
Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink	1A9 14 43 1B9 2A1 15 42 2B1
Small-Outline (DGG) Packages	2A2
description	GND [] 18 39 [] GND 2A4 [] 19 38 [] 2B4
This 9-bit, 4-port universal bus exchanger is designed for 2.3-V to 3.6-V V_{CC} operation.	2A5 [] 20 37 [] 2B5 2A6 [] 21 36 [] 2B6
The SN74ALVCH16409 allows synchronous data exchange between four different buses.	V _{CC} [22 35] V _{CC} 2A7 [23 34] 2B7
Data flow is controlled by the select (SEL0-SEL4)	2A8

The data-flow control logic is designed to allow glitch-free data transmission.

To ensure the high-impedance state during power up or power down, $\overline{\text{SELEN}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16409 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16409 is characterized for operation from -40°C to 85°C.

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inputs. A data-flow state is stored on the rising

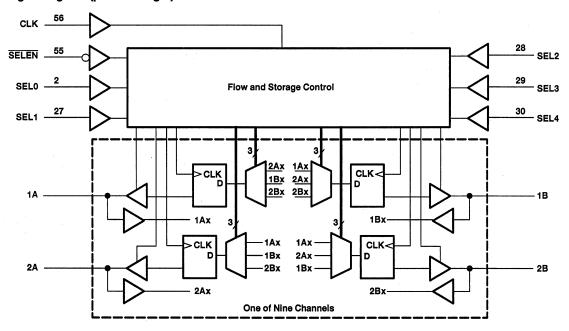
edge of the clock (CLK) input if the select-enable

(SELEN) input is low. Once a data-flow state has

been established, data is stored in the flip-flop on the rising edge of CLK if SELEN is high.



logic diagram (positive logic)



FUNCTION TABLE

INF	PUTS	OUTPUT
CLK	SEND PORT	RECEIVE PORT
Х	Х	В0 [†]
Х	L	L
Х	Н	н
1	L	L
1	Н	Н
Н	Х	в ₀ †
L	Х	В ₀ †

[†]Output level before the indicated steady-state input conditions were established

SN74ALVCH16409 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS SCES022 - JULY 1995

DATA-FLOW CONTROL FUNCTION TABLE

		ı	NPUTS		***************************************		
SELEN	CLK	SEL0	SEL1	SEL2	SEL3	SEL4	DATA FLOW
Н	1	Х	Х	Х	Х	X	No change
L	1	0	0	0	0	0	None, all I/Os off
L	1	0	0	0	0	1	Not used
L	1	0	0	0	1	0	Not used
L	1	0	0	0	1	1	Not used
L	1	0	0	1	0	0	Not used
L	1	0	0	1	0	1	Not used
L	1	0	0	1	1	0	Not used
L	1	0	0	1	1	1	Not used
L	1	0	1	0	0	0	2A to 1A and 1B to 2B
L	1	0	1	0	0	1	2A to 1A
L	1	0	1	0	1	0	2B to 1B
L	1	0	1	0	1	1	2A to 1A and 2B to 1B
L	1	0	1	1	0	0	1A to 2A and 1B to 2B
L	1	0	1	1	0	1	1A to 2A
L	<u>,</u> ↑	0	1	1	1	0	1B to 2B
L	1	0	1	1	1	1	1A to 2A and 2B to 1B
L	1	1	0	0	0	0	1A to 1B and 2B to 2A
L	1	1	0	0	0	1	1A to 1B
·L	1	1	0	0	1	0	2A to 2B
L	\uparrow	1	0	0	1	1	1A to 1B and 2A to 2B
L	1	1	0	1	0	0	1B to 1A and 2A to 2B
L	1	1	0	1	0	1	1B to 1A
L	1	1	0	1	1	0	2B to 2A
L	1	1	0	1	1	1	1B to 1A and 2B to 2A
L	1	1	1	0	0	0	2B to 1A and 2A to 1B
L	1	1	1	0	0	1	1B to 2A
L	1	1	1	0	1	0	2B to 1A
L	1	1	1	0	1	1	2B to 1A and 1B to 2A
L	↑	1	1	1	0	0	1A to 2B and 1B to 2A
L	1	1	1	1	0	1	1A to 2B
L	1	1	1	1	1	0	2A to 1B
L	1	1	1	1	1	1	1A to 2B and 2A to 1B

SCES022 - JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5 V to 4.6 V
Input voltage range, VI: Except I/O ports (see Note 1)
I/O ports (see Notes 1 and 2)0.5 V to V _{CC} + 0.5 V
Output voltage range, V _O (see Notes 1 and 2)
Input clamp current, I_{IK} ($V_I < 0$)
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)
Continuous output current, I _O (V _O = 0 to V _{CC}) ±50 mA
Continuous current through each V _{CC} or GND
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package
DL package 1.4 W
Storage temperature range, T _{sto}

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	٧
V	Ligh level input veltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIH	High-level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7		ν,
	Law level input veltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
VIL	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V .
٧ _I	Input voltage		0	VCC	٧
٧o	Output voltage		0	Vcc	V
		V _{CC} = 2.3 V		-12	
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA .
ЮН		V _{CC} = 3 V		-24	
		V _{CC} = 2.3 V		12	
loL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V			
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST	CONDITIONS	vcct	MIN	TYP‡	MAX	UNIT	
	I _{OH} = -100 μA		MIN to MAX	VCC-0	.2			
	I _{OH} = -6 mA,	V _{IH} = 1.7 V	2.3 V	2				
		V _{IH} = 1.7 V	2.3 V	1.7			v	
Voн	IOH = -12 mA	V _{IH} = 2 V		2.2			V	
		V _{IH} = 2 V	3 V 2.4]	
	IOH = -24 mA,	V _{IH} = 2 V	3 V	2				
	I _{OL} = 100 μA,		MIN to MAX			0.2		
	$i_{OL} = 6 \text{ mA},$	V _{IL} = 0.7 V	2.3 V			0.4		
VOL	In. 10 mA	V _{IL} = 0.7 V	2.3 V			0.7	v	
	I _{OL} = 12 mA	V _{IL} = 0.8 V	2.7 V			0.4		
	IOL = 24 mA,	$I_{OL} = 24 \text{ mA}, \qquad V_{IL} = 0.8 \text{ V}$			0.55			
l _l	V _I = V _{CC} or GND		3.6 V			±5	μА	
	V _i = 0.7 V			45				
	V _I = 1.7 V		2.3 V	-45				
I(hold)	V _i = 0.8 V		3 V	75			μА	
٠	V _I = 2 V		7	-75				
	V _I = 0 to 3.6 V		3.6 V			±500		
I _{OZ} §	VO = VCC or GND		3.6 V			±10	μА	
Icc	V _I = V _{CC} or GND,	IO = 0	3.6 V			40	μА	
ΔICC	One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА	
C _i Control inputs	VI = VCC or GND		3.3 V		4		pF	
Cio A or B ports	VO = VCC or GND		3.3 V		8		рF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V _{CC} = 2.5 V ± 0.2 V V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		0	120	0	120	0	120	MHz
t _W	Pulse duration, CLK high or low		4.2		4.2		3		ns
		A or B before CLK↑	1.9		1.9		1.4		
	Setup time	SEL before CLKT	5.1		4.2		3.5		ns
t _{su}	Setup time	SELEN before CLK1	2.5		2.5		1.8		
		PRE before CLK↑	1		1		0.7		
		A or B after CLKT	0.8		0.8		1		
th	th Hold time	SEL after CLKT	0		0		0		ns
		SELEN after CLK↑	0.5		0.5		0.8		

[‡] All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C. § For I/O ports, the parameter I_{OZ} includes the input leakage current.

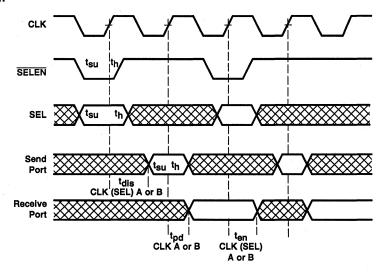
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V	
	(1147-01)		MIN	MAX	MIN	MAX	MIN	MAX	i l
f _{max}		·	120		120		120		MHz
t _{pd}	CLK (A or B)	B or A	2	6.6		5.7	1.5	5.1	ns
t _{en}	CLK (SEL)	A or B	2.5	7.4		6.3	2	5.7	ns
^t dis	CLK (SEL)	A or B	3	7.3		6	2	5.7	ns
t _{dis}	PRE	A or B	3.5	7.7		6.5	2.5	6.1	ns

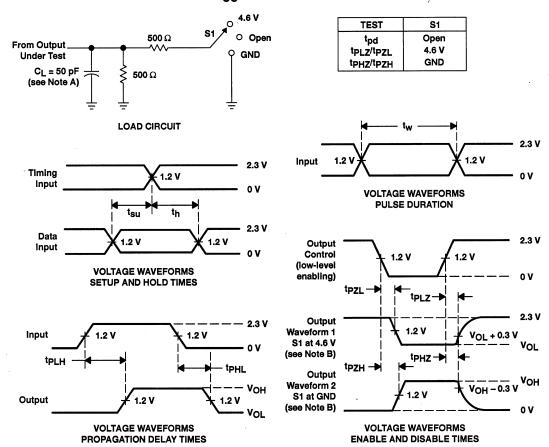
operating characteristics, T_A = 25°C

PARAMETER			TEST CO	NDITIONS	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
					TYP	TYP	
C .	Power dissipation capacitance	Outputs enabled	C: - 50 nE	f = 10 MHz	60	60	ρF
C _{pd}	rower dissipation capacitance	Outputs disabled	С _L = 50 pF,	1 = 10 MINZ	00	00	"

timing diagram



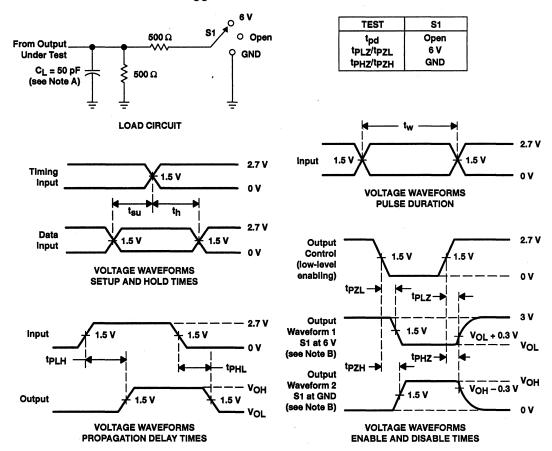
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpl 7 and tpH7 are the same as tdis.
 - F. tpzi and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{\rm O}$ = 50 Ω , $t_{\rm f} \leq$ 2.5 ns, $t_{\rm f} \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tod.

Figure 2. Load Circuit and Voltage Waveforms

SCES056 - SEPTEMBER 1995

 Member of the Texas Instruments Widebus+™ Family 	DGG OR DL P (TOP VII	
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	PRE 1 SELO 2	56 CLK 55 SELEN
 B-Port Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors are Required 	1A1 []3 GND []4	54] 1B1 53] GND 52] 1B2
 UBE™ (Universal Bus Exchanger) Allows Synchronous Data Exchange 	1A3 🛮 6	51 1B3 50 V _{CC}
 ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model 	1A4 🛮 8 1A5 🗓 9 1A6 🖟 10	49 1 1B4 48 1 1B5 47 1 1B6
(C = 200 pF, R = 0) ■ Latch-Up Performance Exceeds 250 mA	GND 🛚 11	46 GND 45 1B7
Per JEDEC Standard JESD-17 Bus Hold on Data Inputs Eliminates the		44] 1B8 43] 1B9
Need for External Pullup/Pulldown Resistors		42 2B1 41 2B2
Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small Outline (DCC) Packages	2A3 🛮 17 GND 🗓 18 2A4 🖟 19	40 2B3 39 GND 38 2B4
Small-Outline (DGG) Packages description	2A5 [] 20 2A6 [] 21	37 2B5 36 2B6
This 9-bit 4-port universal bus exchanger is designed for 2.3-V to 3.6-V V_{CC} operation.	V _{CC} [] 22 2A7 [] 23 2A8 [] 24	35 V _{CC} 34 2B7 33 2B8
The SN74ALVCHR162409 allows synchronous data exchange between four different buses. Data	GND □ 25 2A9 □ 26 SEL1 □ 27	32] GND 31] 2B9 30] SEL4
flow is controlled by the select (SEL0-SEL4)	CELO II 20	201 0512

select-enable (SELEN) input is low. Once a data-flow state is established, data is stored in the flip-flop on the rising edge of the CLK, provided SELEN is high.

SEL2 28

29 SEL3

The data-flow control logic is designed to allow glitch-free data transmission.

The B outputs, which are designed to sink up to 12 mA, include $26-\Omega$ resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{\text{SELEN}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCHR162409 is available in Tl's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

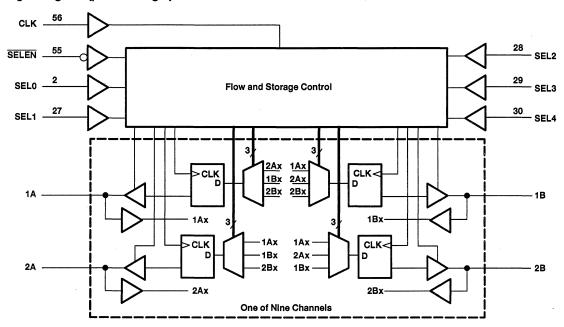
The SN74ALVCHR162409 is characterized for operation from -40°C to 85°C.

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inputs. A data-flow state is stored on the rising edge of the clock (CLK) input, provided the



logic diagram (positive logic)



FUNCTION TABLE

INF	PUTS	OUTPUT
CLK	SEND PORT	RECEIVE PORT
Х	Х	в ₀ †
Х	L	L
Х	Н	н
1	L	L
1	Н	н
Н	\mathbf{X}^{c}	в ₀ †
L	Х	В ₀ †

[†]Output level before the indicated steady-state input conditions were established

SN74ALVCHR162409 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS SCESSOSO - SEPTEMBER 1995

DATA-FLOW CONTROL FUNCTION TABLE

		ı	NPUTS				
SELEN	CLK	SEL0	SEL1	SEL2	SEL3	SEL4	DATA FLOW
Н	1	X	Х	Х	Х	. X	No change
L	1	0	0	0	0	0	None, all I/Os off
L	1	0	0	0	0	1	Not used
L	1	0	0	0	1	0	Not used
L	1	0	0	0	1	1	Not used
L	1	0	0	1	0	0	Not used
L	1	0	0	1	0	1	Not used
L	1	0	0	1	1	0	Not used
L	1	0	0	1	1	1	Not used
L	1	0	1	0	0	. 0	2A to 1A and 1B to 2B
L	1	0	1	0	0	1	2A to 1A
L	1	0	1	0	1	0	2B to 1B
L	1	0	1	0	1	1	2A to 1A and 2B to 1B
L	1	0	1	1	0	0	1A to 2A and 1B to 2B
L	↑	0	1	1	0	1	1A to 2A
L	1	0	1	1	1	0	1B to 2B
L	1	0	1	1	1	1	1A to 2A and 2B to 1B
L	1	1	0	0	0	0	1A to 1B and 2B to 2A
L	1	1	0	0	0	1	1A to 1B
L	1	1	0	0	1	0	2A to 2B
L	1	1	0	0	1	1	1A to 1B and 2A to 2B
L	1	1	0	1	0	0	1B to 1A and 2A to 2B
L	1	1	0	1	0	1	1B to 1A
L	1	1	0	1	1	0	2B to 2A
L	1	1	0	1	1	1	1B to 1A and 2B to 2A
L	1	1	1	0	0	0	2B to 1A and 2A to 1B
L	1	1	1	0	0	1	1B to 2A
L	1	1	1	0	1	0	2B to 1A
L	1	1	1	0	1	1	2B to 1A and 1B to 2A
L	↑	1	1	1	0	0	1A to 2B and 1B to 2A
L	1	1	1	1	0	1	1A to 2B
L	1	1	1	1	1	0	2A to 1B
L	1	1	1	1	1 .	. 1	1A to 2B and 2A to 1B

SCES056 - SEPTEMBER 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} 0.5 V to 4.6 V	.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)	.6 V
I/O ports (see Notes 1 and 2)	.5 V
Output voltage range, V _O (see Notes 1 and 2)	.5 V
Input clamp current, I _{IK} (V _I < 0)	mΑ
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	mΑ
Continuous output current, I _O (V _O = 0 to V _{CC}) ±50 mA	mΑ
Continuous current through each V _{CC} or GND ±100 mA	mΑ
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	1 W
DL package 1.4 W	4 W
Storage temperature range, T _{stg} –65°C to 150°C	0°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	٧
V	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		
VIH	nign-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		٧
· · · · · · · · · · · · · · · · · · ·	Low-level input voltage VCC = 2.7 V to 3.6 VCC = 2.3 V to 2.7 Input voltage Output voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
VIL	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	
۷Į	Input voltage		0	VCC	٧
۷o	Output voltage		0	VCC	٧
	V _{CC} = 2.3 V			-6	mA
ЮН	High-level output current	V _{CC} = 2.7 V		-8	mA
		V _{CC} = 3 V		-12	mA
		V _{CC} = 2.3 V		6	mA
lo _L	Low-level output current	V _{CC} = 2.7 V		8	Δ
		V _{CC} = 3 V		12	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SCES056 - SEPTEMBER 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST C	ONDITIONS	v _{cc} t	MIN	TYP‡	MAX	UNIT
	I _{OH} = -100 μA		MIN to MAX	V _{CC} -0	.2		
	I _{OH} = -4 mA,	V _{IH} = 1.7 V	2.3 V	1.9			
Vou	I _{OH} = -6 mA	V _{IH} = 1.7 V	2.3 V	1.7			v
Voн	10H = -0 IIIV	V _{IH} = 2 V	3 V	2.4			V
	I _{OH} = -8 mA,	V _{IH} = 2 V	2.7 V	2			
	IOH = -12 mA,	V _{IH} = 2 V	3 V	2			
	l _{OL} = 100 μA		MIN to MAX			0.2	
	I _{OL} = 4 mA,	V _{IL} = 0.7 V	2.3 V			0.4	
	In. 6 mA	V _{IL} = 0.7 V	2.3 V			0.55	l v l
VOL	IOL = 6 mA	V _{IL} = 0.8 V	3 V			0.55	V
	IOL = 8 mA,	V _{IL} = 0.8 V	2.7 V			0.6	
	$I_{OL} = 12 \text{ mA},$ $V_{IL} = 0.8 \text{ V}$		3 V			0.8	
1լ	VI = VCC or GND		3.6 V			±5	μА
	V _I = 0.7 V.		2.3 V	45			
	V _I = 1.7 V		2.3 V	-45			
I(hold)	V _I = 0.8 V		3 V	75			μА
	V _I = 2 V]	-75			
	V _I = 0 to 3.6 V		3.6 V			±500	
loz§	VO = VCC or GND		3.6 V			±10	μΑ
Icc	VI = VCC or GND,	IO = 0	3.6 V			40	μА
ΔICC	One input at V _{CC} - 0.6 V,	Other inputs at VCC or GND	3 V to 3.6 V			750	μA
C _i Control inputs	VI = VCC or GND		3.3 V		4		рF
Cio A or B ports	VO = VCC or GND		3.3 V		8		pF

[†] For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions. ‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	120	0	120	0	120	MHz
tw	Pulse duration	CLK high or low	4.2		4.2		3		ns
		A or B before CLK↑	1.9		1.9		1.4		
	Setup time	SEL before CLK↑	5.1		4.2		3.5		ns
^t su	Setup time	SELEN before CLK↑	2.5		2.5		1.8		
		PRE before CLK1	1		1		0.7		
		A or B after CLK↑	0.8		0.8		1		
th	Hold time	S after CLK↑	0		0		0		ns
		SELEN after CLK↑	0.5		0.5		0.8		1

[§] For I/O ports, the parameter IOZ includes the input leakage current.

SCES056 - SEPTEMBER 1995

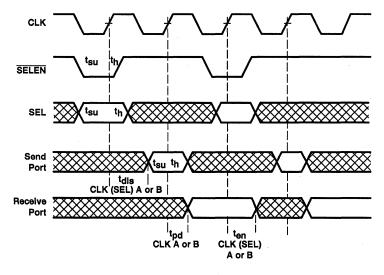
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	TER FROM (INPUT)	TO (OUTPUT)	V _{CC} =	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V	
			MIN	MAX	MIN	MAX	MIN	MAX	
fmax			120		120		120		MHz
t _{pd}	CLK (A or B)	B or A	2	7.5		7	1.5	6.2	ns
t _{en}	CLK (SEL)	A or B	2.5	8.3		7.6	2	6.8	ns
^t dis	CLK (SEL)	A or B	3	7.8		6.4	2	6.1	ns
^t dis	PRE	A or B	3.5	8.4		7	2.5	6.4	ns

operating characteristics, T_A = 25°C

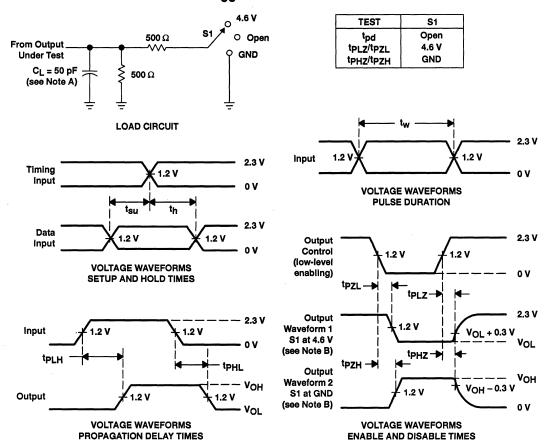
PARAMETER		TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT	
Cpd	Power dissipation capacitance	Outputs enabled	C _I = 50 pF, f = 10 MHz	60	60	pF
Ора	ower dissipation capacitance	Outputs disabled	OL = 30 pr , 1 = 10 Will2	"	00	Pi

timing diagram



SCES056 - SEPTEMBER 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

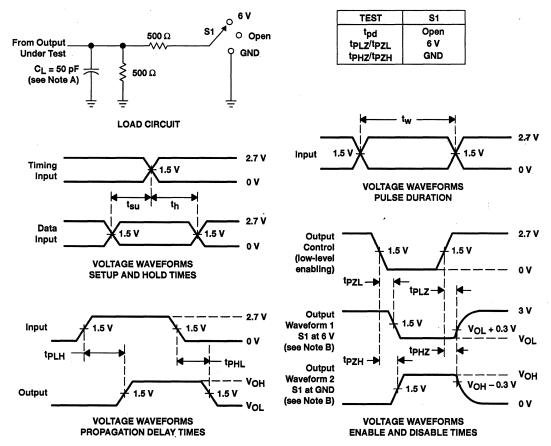


- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SCES056 - SEPTEMBER 1995

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V } \pm 0.3 \text{ V}$



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns.}$ tf \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

SN74ALVCH16500 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES023 - JULY 1995

•	Member of	the Texas	Instruments
	Widebus™	Family	

- UBT™ (Universal Bus Transceiver)
 Combines D-Type Latches and D-Type
 Flip-Flops for Operation in Transparent,
 Latched, or Clocked Mode
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit universal bus transceiver is designed for 2.3-V to 3.6-V V_{CC} operation.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output-enable OEAB is active high. When OEAB is low, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

DGG OR DL PACKAGE (TOP VIEW)

DEAB	1	_	56	GND
LEAB	2		55	CLKAB
A1	Дз		54	B1
GND				GND
A2	[]5		52	B2
А3	[]6] B3
Vcc] 7		50] v _{cc}
A4	8		49	B4
A5] 9		48	B5
A6	10			B6
GND A7	[] 11		46	GND
A7	12		45	
A8	13] B8
A9	14] B9
A10	15			B10
A11	16			B11
A12 GND	17			B12
GND	18		39	GND
A13				B13
A14	20		37	B14
A15	21		36	B15
Vcc	22		35] v _{cc}
A16	23		34	B16
A17	24		33	B17
GND] GND
A18			31	B18
DEBA	27			CLKBA
LEBA	28		29] GND

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, and CLKBA. The output enables are complementary (OEAB is active high, and OEBA is active low).

ō

To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to V_{CC} through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16500 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16500 is characterized for operation from -40°C to 85°C.

TEXAS INSTRUMENTS

SN74ALVCH16500 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCES023 - JULY 1995

FUNCTION TABLET

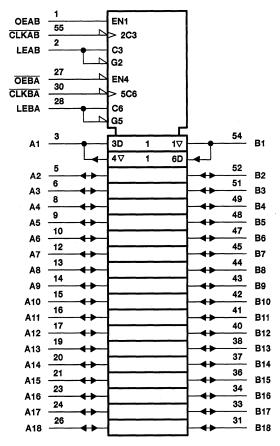
	INPUTS				
OEAB	LEAB	CLKAB	Α	В	
L	Х	X	Х	Z	
н	Н	X	L	L	
Н	Н	X	Н	н	
н	L	\downarrow	L	L	
Н	L	\downarrow	Н	н	
Н	L	Н	Χ	В ₀ ‡ В ₀ §	
Н	L_	L	Х	В ₀ §	

[†] A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

[‡] Output level before the indicated steady-state input conditions were established

[§] Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

logic symbolt



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, VI: Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	1 W
DL package	
Storage temperature range, T _{stq}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.



ADVANCE INFORMATION

SN74ALVCH16500 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCES023 - JULY 1995

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		2.3	3.6	٧	
V	Like laveline deserva	V _{CC} = 2.3 V to 2.7 V	1.7		V	
VIH	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
\/	I am I am I am I am I am I am I am I am	V _{CC} = 2.3 V to 2.7 V		0.7	V	
VIL	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	V	
VI	Input voltage		0	Vcc	٧	
Vo	Output voltage		0	Vcc	٧	
		V _{CC} = 2.3 V		-12		
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA	
Ì		V _{CC} = 3 V		-24		
		V _{CC} = 2.3 V		12		
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA	
		V _{CC} = 3 V		24		
Δt/Δν	Input transition rise or fall rate		0	10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: Unused control inputs must be held high or low to prevent the from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARA	AMETER	TEST CO	ONDITIONS	vcct	MIN	TYP‡	MAX	UNIT
		I _{OH} = -100 μA		MIN to MAX	VCC-0	.2		
		IOH = -6 mA,	V _{IH} = 1.7 V	2.3 V	2			
VOH			V _{IH} = 1.7 V	2.3 V	1.7			v
	I _{OH} = -12 mA	V _{IH} = 2 V	2.7 V	2.2			' '	
		V _{IH} = 2 V	3 V	2.4				
		IOH = -24 mA,	V _{IH} = 2 V	3 V	2			
		l _{OL} = 100 μA		MIN to MAX			0.2	
j		IOL = 6 mA,	V _{IL} = 0.7 V	2.3 V			0.4	V
V _{OL}		l _{Ol} = 12 mA	V _{IL} = 0.7 V	2.3 V			0.7	
		IOL = 12 IIIA	V _{JL} = 0.8 V	2.7 V			0.4	
		I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V			0.55	
lį		V _I = V _{CC} or GND		3.6 V			±5	μА
		V _I = 0.7 V		2.3 V	45			
		V _I = 1.7 V		2.5 V	-45			:
l(hold)		V _I = 0.8 V		3 V	75			μА
		V _I = 2 V		3 V	-75			
	6	V _I = 0 to 3.6.V		3.6 V			±500	
I _{OZ} §		VO = VCC or GND		3.6 V			±10	μА
Icc		$V_I = V_{CC}$ or GND,	lO = 0	3.6 V			40	μА
∆lCC		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА
C _i (Control inputs	V _I = V _{CC} or GND		3.3 V				pF
C _{io}	A or B ports	VO = VCC or GND	•	3.3 V				pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[§] For I/O ports, the parameter IOZ includes the input leakage current.



[‡] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

SN74ALVCH16501 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES024 - JULY 1995

•	Member of	the Texas	Instruments
	Widebus™	Family	

- EPIC™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- UBT[™] (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit universal bus transceiver is designed for 2.3-V to 3.6-V V_{CC} operation.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB

DGG OR DL PACKAGE (TOP VIEW)

OEAB			GND
LEAB	2		CLKAB
A1			B1
GND			GND
A2	5		B2
A3		51	B3
V _{CC}	7	50	V_{CC}
A4	8	49	B4
A5			B5
A6			B6
GND			GND
A7	12		B7
A8		44	B8
A9	14		B9
A10			B10
A11		41	B11
A12			B12
GND		39] GND
A13			B13
A14			B14
A15			B15
Vcc	22	35	V _{CC}
A16			B16
A17			B17
GND] GND
A18	26] B18
OEBA	27	30] CLKBA
LEBA	28	29] GND

is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, OEBA should be tied to V_{CC} through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and OEBA is active low).

The SN74ALVCH16501 is available in Tl's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16501 is characterized for operation from -40°C to 85°C.

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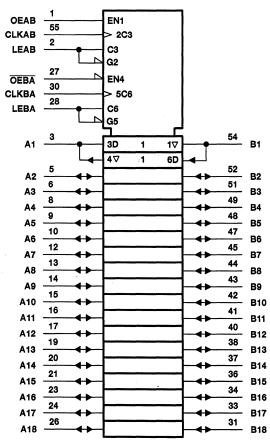


FUNCTION TABLET

	INPUTS				
OEAB	LEAB	CLKAB	Α	В	
L	Х	Х	Х	Z	
Н	Н	Х	L	L	
Н	Н	X	Н	Н	
Н	L	↑	L	L	
Н	L	↑	Н	н	
н	L	Н	Х	В ₀ ‡ В ₀ §	
Н	L	L	Х	B ₀ §	

TA-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

logic symbol†



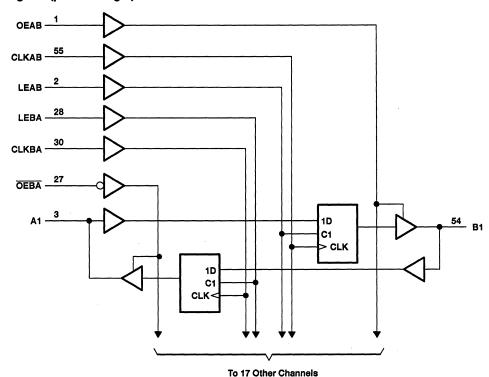
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



Output level before the indicated steady-state input conditions were established, provided that CLKAB is high before LEAB goes low

[§] Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC} 0.5 V to 4.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)
I/O ports (see Notes 1 and 2)
Output voltage range, V _O (see Notes 1 and 2)
Input clamp current, $I_{ K }(V_1 < 0)$ —50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)
Continuous output current, IO (VO = 0 to VCC) ±50 mA
Continuous current through each V _{CC} or GND
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package
DL package 1.4 W
Storage temperature range, T _{stg} –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.



SN74ALVCH16501 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCES024 - JULY 1995

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
Vcc	Supply voltage		2.3	3.6	٧	
1/	High levelines despite	V _{CC} = 2.3 V to 2.7 V	1.7		V	
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V	
	Lauria di anni di anti	$V_{GC} = 2.3 \text{ V to } 2.7 \text{ V}$, 0.7	V	
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	v	
٧١	Input voltage	:	0	Vcc	٧	
Vo	Output voltage		0	Vcc	٧	
	High-level output current	V _{CC} = 2.3 V		-12	2	
ЮН		$V_{CC} = 2.7 \text{ V}$		-12	mA	
		V _{CC} = 3 V		-24		
		V _{CC} = 2.3 V		12		
lOL	Low-level output current	$V_{CC} = 2.7 \text{ V}$		12	mA	
		V _{CC} = 3 V		24		
Δt/Δν	Input transition rise or fall rate		0	10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER	TEST C	ONDITIONS	v _{cc} †	MIN	TYP‡	MAX	UNIT	
VOН		I _{OH} = -100 μA		MIN to MAX	V _{CC} -0	.2			
		I _{OH} = -6 mA,	V _{IH} = 1.7 V	2.3 V	2				
		I _{OH} = -12 mA	V _{IH} = 1.7 V	2.3 V	1.7			v	
			V _{IH} = 2 V	2.7 V	2.2			V	
			V _{IH} = 2 V	3 V	2.4				
		I _{OH} = -24 mA,	V _{IH} = 2 V	3 V	2				
		I _{OL} = 100 μA		MIN to MAX			0.2		
		I _{OL} = 6 mA,	V _{IL} = 0.7 V	2.3 V			0.4		
VOL		la. 10 mA	V _{IL} = 0.7 V	2.3 V			0.7	V	
		I _{OL} = 12 mA	V _{IL} = 0.8 V	2.7 V			0.4		
		I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V			0.55		
11		V _I = V _{CC} or GND		3.6 V			±5	μА	
		V _I = 0.7 V		001/	45				
l(hold)		V _I = 1.7 V		2.3 V	-45			μА	
		V _I = 0.8 V		0.1/	75				
		V _I = 2 V		3 V	-75				
		V _I = 0 to 3.6 V		3.6 V			±500		
I _{OZ} §		VO = VCC or GND		3.6 V			±10	μА	
Icc		V _I = V _{CC} or GND,	IO = 0	3.6 V			40	μА	
ΔlCC		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА	
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V		4		pF	
Cio	A or B ports	VO = VCC or GND		3.3 V		8		pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V _{CC} =		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX		
fclock	Clock frequency		0	150	0	150	0	150	MHz	
	Pulse duration	LE high	3.3		3.3		3.3		ns	
t _w		CLK high or low	3.3		3.3		3.3		IIS	
	Setup time	Data before CLK↑	2.2		2.1		1.7		ns	
t _{su}		Data before LE↓, CLK high	1.9		1.6		1.5			
		Data before LE↓, CLK low	1.3		1.1		1			
th	Hold time	Data after CLK↑	0.6		0.6		0.7			
		Data after LE↓, CLK high or low	1.4		1.7		1.4		ns	

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. § For I/O ports, the parameter I_{OZ} includes the input leakage current.

SN74ALVCH16501 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCES024 - JULY 1995

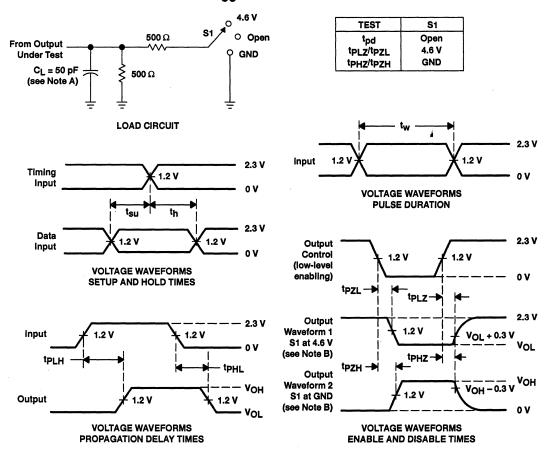
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V	
			MIN	MAX	MIN	MAX	MIN	MAX	
fmax			150		150		150		MHz
	A or B	B or A	1.2	5.4		4.5	1	3.9	
^t pd	LE	A or B	1.6	6.3		5.3	1.3	4.6	ns
	CLK	A or B	1.7	6.7		5.6	1.4	4.9	
^t en	OEAB	В	1.1	6.3		5.3	1	4.6	ns
^t dis	OEAB	В	2.2	6.4		5.7	1.4	5	ns
^t en	OEBA	Α	1.4	6.8		6	1.1	5	ns
^t dis	ŌĒBĀ	Α	2	5.5		4.6	1.3	4.2	ns

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V TYP	V _{CC} = 3.3 V ± 0.3 V TYP	UNIT	
<u> </u>	Power dissipation capacitance	Outputs enabled	C _L = 50 pF, f = 10 MHz	44	54	pF	
C _{pd}		Outputs disabled		6	6	pr	

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

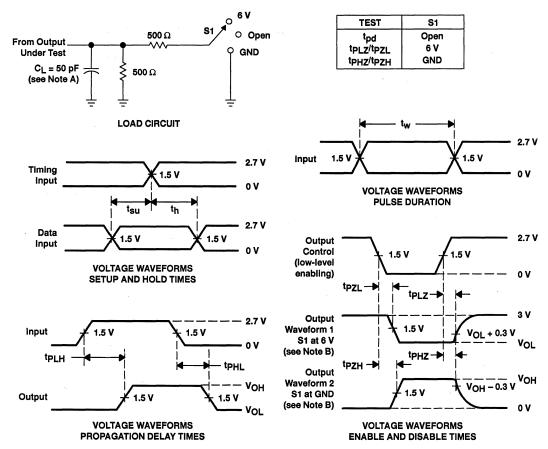


- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2.5$ ns. $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tplz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms

SCES024 - JULY 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

SN74ALVCH16525 18-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES059 - NOVEMBER 1995

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Option Includes Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit universal bus transceiver is designed for 2.3-V to 3.6-V V_{CC} operation.

Data flow in each direction is controlled by output-enable (OEAB and OEBA) and clock enable (CLKENAB and CLKENBA) inputs. For the A-to-B data flow, the data flows through a single register. The B-to-A data can flow through a four-stage pipeline register path, or through a single register path, depending on the state of SEL.

Data is stored in the internal registers on the low-to-high transition of the CLK input, provided that the appropriate CLKEN inputs are low. The A-to-B data transfer is synchronized to the CLKAB input, and B-to-A data transfer is synchronized with the CLK1BA and CLK2BA inputs.

DGG OR DL PACKAGE (TOP VIEW)

CLKENAB [1	\cup	56	SEL
OEAB	12		55] CLKAB
A 4 1	1.		54] B1
GND (14		53	GND
A2 [1 5		52] B2
A1 GND A2 A3 V _{CC} A4 A5	6		51] B3
v _{cc} (7		50] v _{cc}
A4]8		49] B4
A5 (9		48] B5
			47	B6
GND A7	11		46	GND
A7	12		45] B7
A8	13		44] B8
A9 A10 A11	14] B9
A10	15			B10
A11	16			B11
A12 GND	17		40	B12
GND	18			GND
A13	19			B13
A14	20		37	B14
A14 A15	21		36	B15
Vcc	22		35] v _{cc}
A16	23		34	B16
A16 A17 GND	24		33	B17
GND	25		32] GND
A18	26		31] B18
OEBA (27		30	[] CLK1BA
CLKENBA	28		29	CLK2BA
				-

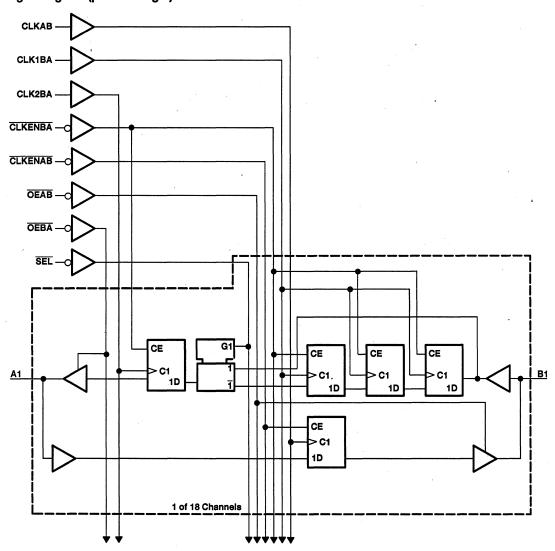
To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16525 is characterized for operation from -40°C to 85°C.

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logic diagram (positive logic)



SCES059 - NOVEMBER 1995

Function Tables

A-TO-B STORAGE (OEAB = L)

l l	INPUTS					
CLKENAB	KENAB CLKAB A		В			
Н	Х	Х	B ₀ †			
L	1	L	L			
L	1	Н	н			

[†] Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE (OEBA = L)

	OUTPUT				
CLKENBA	CLK2BA	CLK1BA	SEL	В	A
Н	Х	X	Х	Х	A ₀ †
L	1	X	н	L	L
L	1	X	н	Н	Н
L	1	1	L	L	L‡
L	1	1	L	Н	н‡

[†] Output level before the indicated steady-state input conditions were established

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output clamp current, IOK (VO < 0 or VO > VCC)	
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range, T _{stg}	65°C to 150°C

[§] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

[‡]Three CLK1BA edges and one CLK2BA edge are needed to propagate data from B-to-A when SEL is low.

SN74ALVCH16525 18-BIT REGISTERED BUS TRANSCEIVER **WITH 3-STATE OUTPUTS**

SCES059 - NOVEMBER 1995

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		2.3	3.6	٧
.,	High leveling decline	V _{CC} = 2.7 V to 3.6 V	2		V
VIH	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		ľ
	l and land land to the sec	V _{CC} = 2.7 V to 3.6 V		0.8	V
VIL	Low-level input voltage VCC = 2.3 V t			0.7	
VI	Input voltage		0	VCC	V
Vo	Output voltage		0	VCC	V
		V _{CC} = 2.3 V		-12	
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 2.3 V		12	
loL	Low-level output current	V _{CC} = 2.7 V		12	mA
	•	V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CO	ONDITIONS	v _{cc} †	MIN	TYP‡	MAX	UNIT
		I _{OH} = -100 μA	•	MIN to MAX	VCC-C).2		
		IOH = −6 mA,	V _{IH} = 1.7 V	2.3 V	2			
1/			V _{IH} = 1.7 V	2.3 V	1.7			v
Vон		I _{OH} = -12 mA	V _{IH} = 2 V	2.7 V	2.2			•
			V _{IH} = 2 V	3 V	2.4			
	,	IOH = −24 mA,	V _{IH} = 2 V	3 V	2			
		l _{OL} = 100 μA		MIN to MAX			0.2	
		I _{OL} = 6 mA,	V _{IL} = 0.7 V	2.3 V			0.4	
VOL		l- 10 4	V _{IL} = 0.7 V	2.3 V			0.7	V
		I _{OL} = 12 mA	V _{IL} = 0.8 V	2.7 V			0.4	
		I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V			0.55	
lį		V _I = V _{CC} or GND		3.6 V			±5	μА
		V _I = 0.7 V		2.3 V	45			
		V _I = 1.7 V] 2.3 V	-45			
Ihold		V _I = 0.8 V		0.1/	- 75			μΑ
		V _I = 2 V		3 V	-75			
		V _I = 0 to 3.6 V		3.6 V			±500	
IOZ§		VO = VCC or GND		3.6 V			±10	μΑ
Icc		V _I = V _{CC} or GND,	IO = 0	3.6 V			40	μА
Δlcc		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V		3		pF
Co	A or B ports	V _O = V _{CC} or GND		3.3 V		7		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

 $[\]ddagger$ All typical values are at VCC = 3.3, TA = 25°C. § For I/O ports, the parameter IOZ includes the input-leakage current.



SN74ALVCH16525 18-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCES059 - NOVEMBER 1995

timing requirements over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

						V _{CC} = 2.7 V		3.3 V 3 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	120	0	125	0	150	MHz
t _w	Pulse duration, CLK high or low		3.2		3.2		3		ns
		A data before CLKAB↑	1.3		1.3		1.3	-	
		B data before CLK2BA↑	2.1		1.8		1.7		
		B data before CLK1BA↑	1.3		1.2		1.1		
t _{su}	Setup time	SEL before CLK2BA↑	3.3		3.3		3.3		ns
		CLKENAB before CLKAB↑	2.1		1.9		1.6		
		CLKENBA before CLK1BA↑	2.7		2.5		2.1		
		CLKENBA before CLK2BA↑	2.7		2.5		2.2		
		A data after CLKAB↑	0.7		0.4		0.9		
		B data after CLK2BA↑	0.4		0		0.6		
		B data after CLK1BA↑	0.8		0.4		1		
th	Hold time	SEL after CLK2BA↑	0		0		0.1		ns
		CLKENAB after CLKAB↑	0.1		0.3		0.3		
		CLKENBA after CLK1BA↑	0		0		0.1		
		CLKENBA after CLK2BA↑	0	********	0		0		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

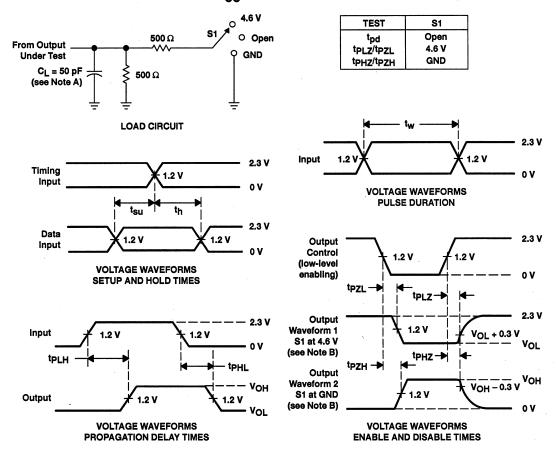
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.5 V ± 0.2 V		V _{CC} =	2.7 V	V _{CC} =		UNIT
	(INFO1)	(OUTFOT)	MIN	MAX	MIN	MAX	MIN	MAX	
fmax			120		125		150		MHz
^t pd	CLKAB or CLK2BA	A or B	1	5.1		4.4	1	4.2	ns
t _{en}	OEAB or OEBA	A or B	1	6.6		6.1	1	5.1	ns
^t dis	OEAB or OEBA	A or B	1	6.5		5.4	1	4.9	ns

operating characteristics, T_A = 25°C

	PARAMETER		TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
	Danier diagia di ancoralita di a	Outputs enabled	0 50-5 4 40 141-			
C _{pd}	Power dissipation capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	160	160	pF

SCES059 - NOVEMBER 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

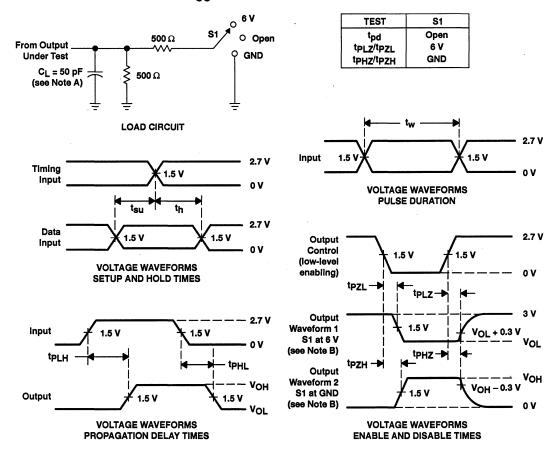


- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tplz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SCES059 - NOVEMBER 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - 8. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \, \Omega$, $t_f \leq 2.5 \, \text{ns}$, $t_f \leq 2.5 \, \text{ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

SN74ALVCH162525 18-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES058 - NOVEMBER 1995

- **Member of the Texas Instruments** Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted) **CMOS) Submicron Process**
- B-Port Outputs Have Equivalen 26-Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Option Includes Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit universal bus transceiver is designed for 2.3-V to 3.6-V V_{CC} operation.

Data flow in each direction is controlled by output-enable (OEAB and OEBA) and clock enable (CLKENAB and CLKENBA) inputs. For the A-to-B data flow, the data flows through a single register. The B-to-A data can flow through a four-stage pipeline register path, or through a single register path, depending on the state of SEL.

DGG OR DL PACKAGE (TOP VIEW)

	_	$\overline{}$		
CLKENAB [1	U	56	SEL
OEAB [2			CLKAB
A1 [54	
GND [4			GND
	5		52] B2
	6		51] B3
v _{cc} [7		50] v _{cc}
A4 [8		49] B4
A5 [9		48] B5
A6 [10] B6
GND [11	•		GND
A7 [] B7
	13] B8
A9 [] B9
	15] B10
A11 [B11
	17		40	B12
	18] GND
A13 [3] B13
A14 [B 14
	21			B15
	22			□ v _{cc}
A16 [] B16
	24			B17
	25] GND
	26		31	B18
OEBA	d ~ .			CLK1BA
CLKENBA [28		29	CLK2BA

Data is stored in the internal registers on the low-to-high transition of the CLK input, provided that the appropriate CLKEN inputs are low. The A-to-B data transfer is synchronized to the CLKAB input, and B-to-A data transfer is synchronized with the CLK1BA and CLK2BA inputs.

The B outputs, which are designed to sink up to 12 mA, include $26-\Omega$ resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

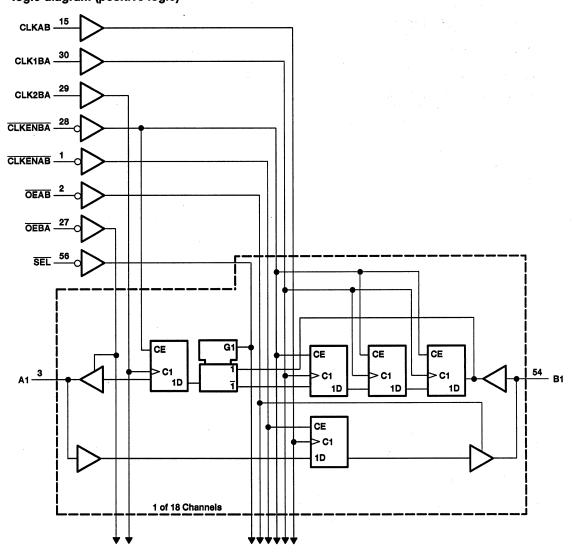
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162525 is characterized for operation from -40°C to 85°C.

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logic diagram (positive logic)



SCES058 - NOVEMBER 1995

Function Tables

A-TO-B STORAGE (OEAB = L)

1	INPUTS			
CLKENAB	CLKAB	Α	В	
Н	Х	Х	B ₀ †	
L	↑	L	L	
ĺ	1	Н	* н	

[†] Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE (OEBA = L)

	INPUTS							
CLKENBA	CLK2BA	CLK1BA	SEL	В	Α			
Н	X	Χ	X	X	A ₀ †			
L	1	X	Н	L	L			
L	1	X	Н	Н	н			
L	1	1	L	L	L‡			
L	1	1	L	Н	н‡			

[†]Output level before the indicated steady-state input conditions were established

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	. $-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): DGG package .	1 W
DL package	1.4 W
Storage temperature range, T _{sto}	

[§] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

[‡]Three CLK1BA edges and one CLK2BA edge are needed to propagate data from B-to-A when SEL is low.

SN74ALVCH162525 18-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCES058 - NOVEMBER 1995

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		2.3	3.6	V
V	V _{CC} = 2.7 V to 3.6 V		2		V
VIH	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		\ \
V.,	Low level input veltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
VIL	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	\ \
٧ı	Input voltage		0	Vcc	٧
Vο	Output voltage		0	Vcc	V
		V _{CC} = 2.3 V		-12	
ЮН	High-level output current (A port)	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V	\	-24	
		V _{CC} = 2.3 V		12	
lol	Low-level output current (A port)	ow-level output current (A port) V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
		V _{CC} = 2.3 V		-6	
ЮН	High-level output current (B port)	V _{CC} = 2.7 V		-8	mA
		V _{CC} = 3 V		-12	
		V _{CC} = 2.3 V		6	
loL	Low-level output current (B port)	V _{CC} = 2.7 V	2.7 V		mA
		V _{CC} = 3 V		12	
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SCES058 - NOVEMBER 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST C	ONDITIONS	v _{cc} t	MIN	TYP‡	MAX	UNIT	
	IOH = -100 μA		MIN to MAX	VCC-C).2			
	IOH = -6 mA,	V _{IH} = 1.7 V	2.3 V	2				
\/(A mant)		V _{IH} = 1.7 V	2.3 V	1.7			v	
V _{OH} (A port)	I _{OH} = -12 mA	V _{IH} = 2 V	2.7 V	2.2			V	
	ĺ	V _{IH} = 2 V	3 V	2.4				
	IOH = −24 mA,	V _{IH} = 2 V	3 V	2				
	IOH = -100 μA		MIN to MAX	VCC-C).2			
	IOH = -4 mA,	V _{IH} = 1.7 V	2.3 V	1.9				
Var. (B nort)	lau 6 mA	V _{IH} = 1.7 V	2.3 V	1.7			v	
V _{OH} (B port)	IOH = -6 mA	V _{IH} = 2 V	3 V	2.4			V	
	IOH = -8 mA,	V _{IH} = 2 V	2.7 V	2				
	IOH = -12 mA,	V _{IH} = 2 V	3 V	2				
	ΙΟL = 100 μΑ		MIN to MAX			0.2		
	IOL = 6 mA,	V _{IL} = 0.7 V	2.3 V			0.4		
VOL (A port)	la: 10 mA	V _{IL} = 0.7 V	2.3 V			0.7	V	
	I _{OL} = 12 mA	V _{IL} = 0.8 V	2.7 V			0.4		
	I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V			0.55		
	l _{OL} = 100 μA		MIN to MAX			0.2		
	I _{OL} = 4 mA,	V _{IL} = 0.7 V	2.3 V			0.4		
VOL (B port)	IOL = 6 mA	V _{IL} = 0.7 V	2.3 V			0.55	55 V	
	IOL = 0 IIIX	V _{IL} = 0.8 V	3 V			0.55	· •	
	I _{OL} = 8 mA,	V _{IL} = 0.8 V	2.7 V			0.6		
	I _{OL} = 12 mA,	V _{IL} = 0.8 V	3 V			0.8		
կ	V _I = V _{CC} or GND		3.6 V			±5	μА	
	V _I = 0.7 V		2.3 V	45				
	V _I = 1.7 V		2.5 V	-45				
lhold	V ₁ = 0.8 V		3 V	75			μA	
	V _I = 2 V]	-75				
	V _I = 0 to 3.6 V		3.6 V			±500		
loz§	VO = VCC or GND		3.6 V			±10	μΑ	
loc	$V_1 = V_{CC}$ or GND,	I _O = 0	3.6 V			40	μΑ	
ΔICC	One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μΑ	
C _i Control inputs	V _I = V _{CC} or GND		3.3 V		3		pF	
Co A or B ports	VO = VCC or GND		3.3 V		7		pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions. ‡ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. § For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

		VCC = 2.6 ±0.2 V				2.7 V	V _{CC} =		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
^f clock	Clock frequency		0	120	0	125	0	150	MHz
t _w	Pulse duration, CLK high or l	ow	3.2		3.2		3		ns
		A data before CLKAB↑	1.3		1.3		1.3		
l	•	B data before CLK2BA↑	2.1		1.8		1.7		
		B data before CLK1BA↑	1.3		1.2		1.1		
t _{su}	Setup time	SEL before CLK2BA↑	3.3		3.3		3.3		ns
		CLKENAB before CLKAB↑	2.1		1.9		1.6		
		CLKENBA before CLK1BA↑	2.7		2.5		2.1		
		CLKENBA before CLK2BA↑	2.7		2.5		2.2		
		A data after CLKAB↑	0.7		0.4		0.9		
		B data after CLK2BA↑	0.4		0		0.6		
		B data after CLK1BA↑	0.8		0.4		1		
th	Hold time	SEL after CLK2BA1	0		0		0.1		ns
		CLKENAB after CLKAB↑	0.1		0.3		0.3		
		CLKENBA after CLK1BA↑	0		0		0.1		
		CLKENBA after CLK2BA↑	0		0		0		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Vcc =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} = ± 0.	3.3 V 3 V	UNIT
	(INFOT)	(0011-01)	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			120		125		150		MHz
	CLKAB	В	1	6.1		5.4	1	4.7	
^t pd	CLK2BA	Α	1	5.1		4.4	1	4.2	ns
	OEBA	Α	1	6.6		6.1	1	5.1	
t _{en}	OEAB	В	1	7.2		6.8	1	5.7	ns
	ŌĒBĀ	Α	1	6.5	,	5.4	1	4.9	
^t dis	OEAB	В	1	6.5		5.4	1	4.9	ns

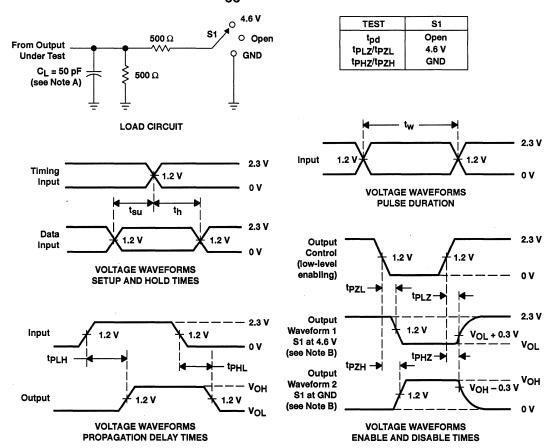
operating characteristics, T_A = 25°C

	PARAMETER		TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
C .	Power dissipation capacitance	Outputs enabled	C ₁ = 50 pF, f = 10 MHz	160	160	pF
C _{pd}	r ower dissipation capacitance	Outputs disabled	- ο[= 50 pr, 1= 10 Mmz	160	100	PΓ



SCES058 - NOVEMBER 1995

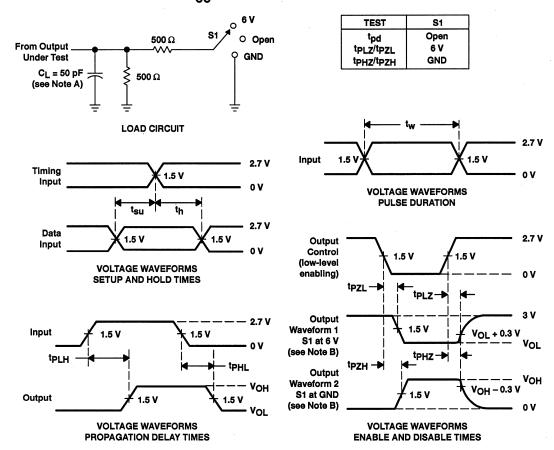
PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten-
 - G. tplH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpl H and tpHI are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

SN74ALVCH16543 16-BIT REGISTERED TRANSCEIV WITH 3-STATE OUTPUTS

SCES025 - JULY 1995

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit registered transceiver is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16543 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (CEAB) input must be low in order to enter data from A or to output data from B. If CEAB is low and LEAB is low, the A-to-B latches are transparent; a subsequent low-to-high transition of LEAB puts the A latches in the storage mode. With CEAB and OEAB both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using CEBA, LEBA, and OEBA.

DGG OR DL PACKAGE (TOP VIEW)

	П		1
1	<u> </u>		1OEBA
2			1LEBA
		54	1CEBA
4		53] GND
		52	
		51] 1B2
7] v _{cc}
] 1B3
9] 1B4
] 1B5
] GND
12		45] 1B6
] 1B7
] 1B8
] 2B1
			2B2
] 2B3
18			GND
] 2B4
] 2B5
21] 2B6
22		35	
		34] 2B7
		32	GND
26		31	2CEBA
27		30	2LEBA
28		29	2OEBA
	2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27	2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27	2 55 3 54 4 53 5 52 6 51 7 50 8 49 9 48 10 47 11 46 12 45 13 44 14 43 15 42 16 41 17 40 18 39 19 38 20 37 21 36 22 35 23 34 24 33 25 32 26 31 27 30

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16543 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16543 is characterized for operation from -40°C to 85°C.

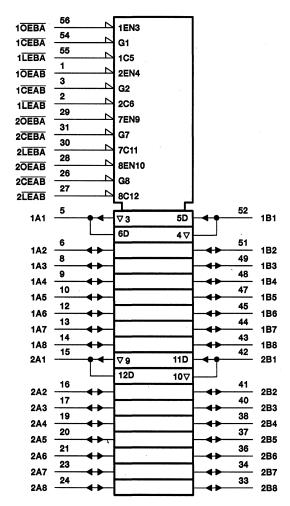
ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

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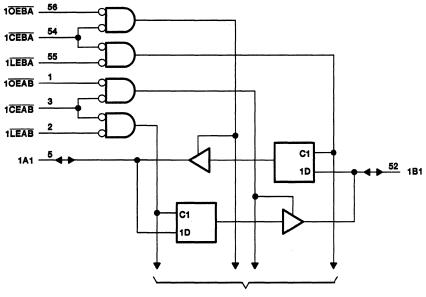
3-147

logic symbol†

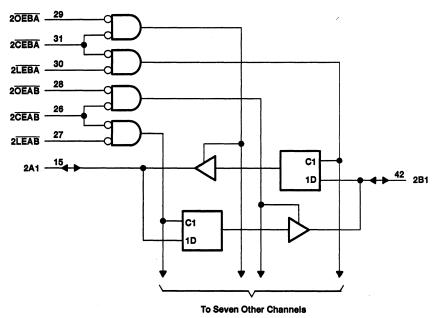


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels



SN74ALVCH16543 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCES025 - JULY 1995

FUNCTION TABLET (each 8-bit section)

	INPUTS							
CEAB	LEAB	OEAB	Α	В				
Н	Х	Х	Х	Z				
×	Х	н	Χ	z				
L	Н	L	X	B ₀ ‡				
L	L	L	L'	L				
L	L	L	Н	Н				

[†] A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, VI: Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range, T _{stg}	65°C to 150°C

[§] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

[‡] Output level before the indicated steady-state input conditions were established

SN74ALVCH16543 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCES025 - JULY 1995

recommended operating conditions (see Note 4)

i			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	V
	High level input veltage	V _{CC} = 2.3 V to 2.7 V	1.7		V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		_ v
V	t ave lavel input valtage	V _{CC} = 2.3 V to 2.7 V		0.7	v
VIL	V _{IL} Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	v
Vj	Input voltage		0	Vcc	V
Vο	Output voltage		0	VCC	٧
		V _{CC} = 2.3 V		-12	
ЮН	High-level output current	$V_{CC} = 2.7 \text{ V}$		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 2.3 V		12	
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CO	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
		I _{OH} = -100 μA		MIN to MAX	V _{CC} -0	.2		
		I _{OH} = -6 mA,	V _{IH} = 1.7 V	2.3 V	2			
V			V _{IH} = 1.7 V	2.3 V	1.7			v
VOH		I _{OH} = -12 mA	V _{IH} = 2 V	2.7 V	2.2			V
			V _{IH} = 2 V	3 V	2.4			
		I _{OH} = −24 mA,	V _{IH} = 2 V	3 V	2			
		I _{OL} = 100 μA		MIN to MAX			0.2	
		I _{OL} = 6 mA,	V _{IL} = 0.7 V	2.3 V			0.4	
VOL		I _{OL} = 12 mA	V _{IL} = 0.7 V	2.3 V			0.7	·V
		IOL = 12 IIIA	V _{IL} = 0.8 V	2.7 V			0.4	
		I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V			0.55	
կ		VI = VCC or GND		3.6 V			±5	μΑ
		V _I = 0.7 V		2.3 V	45			
		V _I = 1.7 V		2.5 V	-45			
l(hold)		V _I = 0.8 V		3 V	75			μA
		V _I = 2 V]	-75			
		V _I = 0 to 3.6 V		3.6 V			±500	
I _{OZ} §		VO = VCC or GND		3.6 V			±10	μА
Icc		V _I = V _{CC} or GND,	I _O = 0	3.6 V			40	μА
∆lcc		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V				pF
Cio	A or B ports	VO = VCC or GND		3.3 V				pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[§] For I/O ports, the parameter IOZ includes the input leakage current.



 $[\]ddagger$ Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

SCES030 - JULY 1995

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance implanted **CMOS) Submicron Process**
- UBT™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit universal bus transceiver is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16600 combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and

DGG OR DL PACKAGE (TOP VIEW)

OEAB [1	U	56	CLKENAB
LEAB [CLKAB
A1 [<u>Б</u> В1
GND [GND
A2 [5			B2
A3 [6		51] B3
v _{cc} [7		50	₫ v _{cc}
Ã4 [8		49] в4
A5 [Ī B5
A6 [<u>Б</u> В6
GND [GND
A7 [₫ B7
A8 [44] B8
A9 [] в9
A10 [15		42	B10
A11 [16		41	B11
A12 [17		40	B12
GND [18		39] GND
A13 [38] B13
A14 [20		37] B14
A15 [21] B15
v _{cc} [22		35] v _{cc}
A16 [23		34] B16
A17 [24] B17
GND [25] GND
A18 [26] B18
OEBA [27			CLKBA
LEBA [28		29	CLKENBA

CLKBA) inputs. The clock can be controlled by the clock-enable (CLKENAB and CLKENBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output enable OEAB is active low. When OEAB is low, the outputs are active. When OEAB is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, CLKBA, and CLKENBA.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16600 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16600 is characterized for operation from -40°C to 85°C.

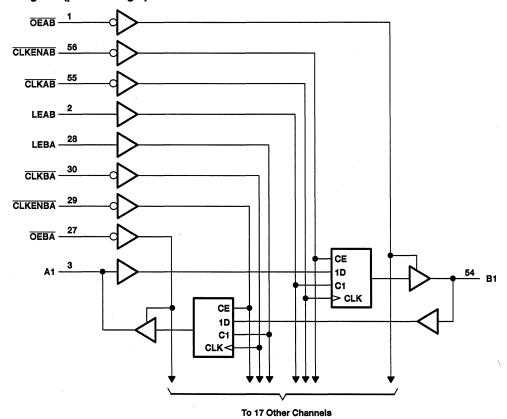
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							E†
E	IN	СТ	n	uт	Δ	RI	FI

	1	NPUTS			OUTPUT
CLKENAB	OEAB	LEAB	CLKAB	Α	В
X	Н	Х	Х	Х	Z
х	L	Н	X	L	L
Х	L	Н	Х	Н	Н
Н	L	L	Х	Χ	В ₀ ‡ В ₀ ‡
Н	L	L	X	Χ	в ₀ ‡
L	L	L	\downarrow	L	L
L	L	L	\downarrow	Н	н
L	L	L	Н	Χ	В ₀ ‡ В ₀ §
L	L	L	L	X	В ₀ §

[†] A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.

logic diagram (positive logic)





[‡] Output level before the indicated steady-state input conditions were established

[§] Output level before the indicated steady-state input conditions were established, provided that OLKAB was low before LEAB went low

SN74ALVCH16600 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES030 - JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Oural walters was V	051/4-461/
Supply voltage range, V _{CC}	– U.5 V to 4.6 V
Input voltage range, VI: Except I/O ports (see Note 1)	0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3)): DGG package 1 W
	DL package 1.4 W
Storage temperature range, Teta	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		2.3	3.6	V
	Lligh lovel input veltage	V _{CC} = 2.3 V to 2.7 V	1.7		v
VIH	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		_ v
V.	Levy level input veltage	V _{CC} = 2.3 V to 2.7 V		0.7	V
۷ĮL	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	V
VI	Input voltage		0	Vcc	٧
Vo	Output voltage		0	Vcc	٧
*		V _{CC} = 2.3 V		-12	
ЮН	High-level output current	$V_{CC} = 2.7 \text{ V}$		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 2.3 V		12	
lol	Low-level output current	$V_{CC} = 2.7 \text{ V}$		12	mA
		V _{CC} = 3 V		24	
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SCES030 - JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST Co	ONDITIONS	v _{cc} †	MIN	TYP‡	MAX	UNIT	
		I _{OH} = -100 μA		MIN to MAX	VCC-C).2			
		I _{OH} = -6 mA,	V _{IH} = 1.7 V	2.3 V	2				
		I _{OH} = -12 mA	V _{IH} = 1.7 V	2.3 V	1,7			V	
VOH			V _{IH} = 2 V	2.7 V	2.2			V	
			V _{IH} = 2 V	3 V	2.4				
		IOH = -24 mA,	V _{IH} = 2 V	3 V	2				
		I _{OL} = 100 μA		MIN to MAX			0.2		
		I _{OL} = 6 mA,	V _{IL} = 0.7 V	2.3 V			0.4		
VOL		I 40 mA	V _{IL} = 0.7 V	2.3 V			0.7	ν	
		I _{OL} = 12 mA	V _{IL} = 0.8 V	2.7 V			0.4		
		I _{OL} = 24 mA,	V _{IL} = 0.8 V	. 3 V			0.55		
lį	,	VI = VCC or GND	,	3.6 V			±5	μА	
		V _I = 0.7 V		2.3 V	45				
		V _I = 1.7 V		2.3 V	-45				
l(hold)		V _I = 0.8 V		3 V	75			μА	
		V _I = 2 V]	-75				
	*	V _I = 0 to 3.6 V	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	3.6 V			±500		
l _{OZ} §		VO = VCC or GND	,	3.6 V			±10	μА	
ICC	-	V _I = V _{CC} or GND,	IO = 0	3.6 V			40	μА	
Δlcc		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА	
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V		4		рF	
Cio	A or B ports	VO = VCC or GND		3.3 V		8		pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		y	V _{CC} =		V _{CC} =	2.7 V	V _{CC} =		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	150	0	150	0	150	MHz
tw	Pulse duration	LE↑	3.3		3.3		3.3		ns
w	ruise duration	<u>CLK</u> ↑	3.3		3.3		3.3		118
		Data before CLK↑	1.3		1.3		1.2		
	Setup time	Data before LE↓, CLK↑	1.2		1.1		1.1		ns
t _{su}	Setup time	Data before LE↓, CLK↓	1.8		1.5		1.5		
		CLKEN before CLK↑	0.7		0.7		0.8		
		Data after CLK↑	1.5		1.8		1.5		
th	Hold time	Data after LE↓, CLK↑	1.6		1.9		1.6		ns
เท	riold time	Data after LE↓, CLK↓	1.2		1.6		1.3		
,		CLKEN after CLK↑	1.4		1.7		1.4		

[†] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C. § For I/O ports, the parameter I_{OZ} includes the input leakage current.

SN74ALVCH16600 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS SCES030 - JULY 1995

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

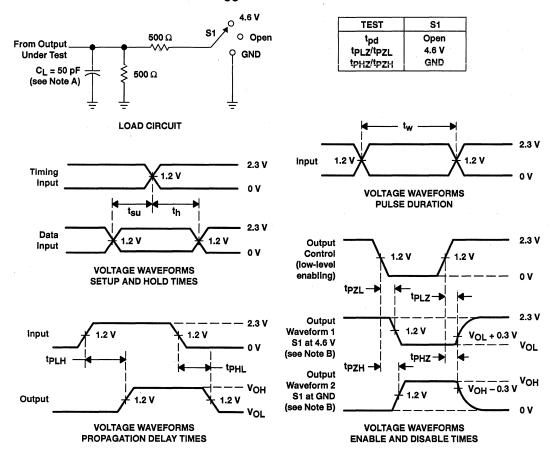
PARAMETER	PARAMETER	FROM	TO (OUTPUT)					2.5 V 2 V	Vcc=	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INPUT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX					
^f max			150		150		150		MHz				
	A or B	B or A	1	5.7		4.7	1	4					
^t pd	LEAB or LEBA	A or B	1	6.5		5.5	1	4.8	ns				
•	CLKAB or CLKBA	A or B	1.4	7.9		6.8	1.3	5.7	İ				
t _{en}	OEAB	В	1.1	7.1		6.3	1.1	5.2	ns				
t _{dis}	OEAB	В	1.7	5.7		4.7	1.2	4.4	ns				

operating characteristics, $T_A = 25$ °C

	PARAMETER		TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V TYP	V _{CC} = 3.3 V ± 0.3 V TYP	UNIT
<u> </u>	Power dissipation capacitance	Outputs enabled	C ₁ = 50 pF, f = 10 MHz	43	56	ρF
C _{pd}	Fower dissipation capacitance	Outputs disabled	CL = 50 pr, T = 10 MHZ	6	6	Pr

SCES030 - JULY 1995

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$

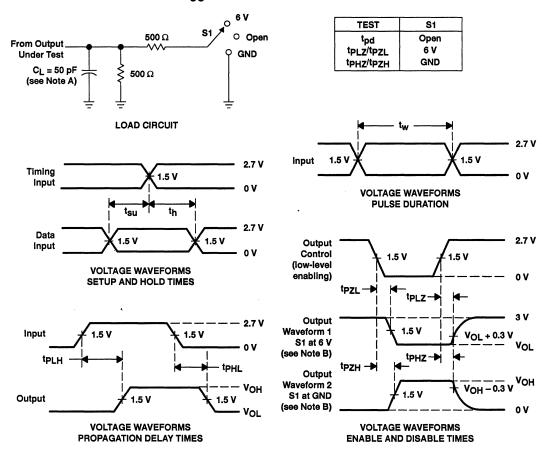


- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \Omega$, $t_{f} \leq 2.5 \text{ ns}$, $t_{f} \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms

SCES030 - JULY 1995

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V AND } 3.3 \text{ V } \pm 0.3 \text{ V}$



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tod.

Figure 2. Load Circuit and Voltage Waveforms

SCES027 - JULY 1995

- Member of the Texas Instruments Widebus™ Family
- UBT™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode
- EPIC™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF. R = 0
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit universal bus transceiver is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16601 combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and

DGG OR DL PACKAGE (TOP VIEW)

	\Box		1
OEAB [CLKENAB
LEAB [CLKAB
A1 [] B1
GND [53] GND
A2 [52] B2
A3 [] B3
v _{cc} [7	50] v _{cc}
A4 [8	49	□ B4
A5 [] B5
A6 [10] B6
GND [11		GND
A7 [12] B7
	13	44] B8
A9 [14	43] B9
A10 [] B10
A11 [16]B11
A12 [17		B12
GND [18] GND
A13 [19] B13
A14 [20		B14
A15 [36	B15
v _{cc} [22	35] v _{cc}
A16 [B16
A17 [B17
GND [] GND
A18 [26] B18
OEBA [30] CLKBA
LEBA [28	29	CLKENBA

CLKBA) inputs. The clock can be controlled by the clock-enable (CLKENAB and CLKENBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Output enable \overline{OEAB} is active low. When \overline{OEAB} is low, the outputs are active. When OEAB is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, CLKBA, and CLKENBA.

To ensure the high-impedance state during power up or power down, $\overline{\sf OE}$ should be tied to $\sf V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16601 is available in Tl's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16601 is characterized for operation from -40°C to 85°C.

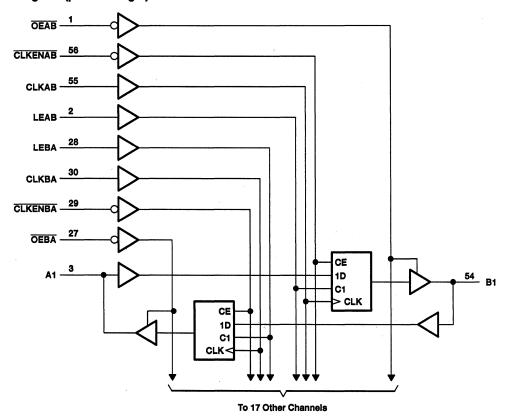
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FUN	ICT		TA	DI	Ϡ
rur	401	IUN	IIA	Ю	-61

	ı	NPUTS			OUTPUT		
CLKENAB	OEAB	LEAB	CLKAB	Α	В		
X	Н	Х	Х	Х	Z		
X	L	Н	X	L	L		
x	. L	Н	X	Н	н		
н	L.	L	X	X	В ₀ ‡ В ₀ ‡		
н	L	L	X	X	в ₀ ‡		
L	L	L	1	L	L		
L	L	L	1	Н	н		
L	L	L	L	X	В ₀ ‡ В ₀ \$		
L	L	L	Н	×	B ₀ §		

TA-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.

logic diagram (positive logic)





[‡] Output level before the indicated steady-state input conditions were established

[§] Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

SN74ALVCH16601 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES027 - JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} 0.5 V to 4.6 V
Input voltage range, VI: Except I/O ports (see Note 1)
I/O ports (see Notes 1 and 2)
Output voltage range, V _O (see Notes 1 and 2)
Input clamp current, I_{IK} ($V_I < 0$)
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)
Continuous output current, I _O (V _O = 0 to V _{CC}) ±50 mA
Continuous current through each V _{CC} or GND
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package
DL package 1.4 W
Storage temperature range, T _{stg} –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
Vcc	Supply voltage		2.3	3.6	V	
V	V _{CC} = 2.3 V to 2.7 V V _{CC} = 2.7 V to 3.6 V		1.7		V	
VIH			2		_ v	
V.,	Law law line wheels	V _{CC} = 2.3 V to 2.7 V		0.7	v	
VIL	Low-level input voltage V _{CC} = 2.7 V to 3.6 V			0.8	٧	
VI	Input voltage		0	Vcc	V	
٧o	Output voltage	,	0	VCC	٧	
	High-level output current	V _{CC} = 2.3 V		-12		
ЮН		V _{CC} = 2.7 V		-12	mA	
		V _{CC} = 3 V		-24		
	$ V_{CC} = 2.3 \text{ V} $ Low-level output current $ V_{CC} = 2.7 \text{ V} $	V _{CC} = 2.3 V	12			
lOL		V _{CC} = 2.7 V		12	mA	
		V _{CC} = 3 V		24		
Δt/Δv	Input transition rise or fall rate		0	10	ns/V	
T _A	Operating free-air temperature		-40	85	°C	

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN74ALVCH16601 **18-BIT UNIVERSAL BUS TRANSCEIVER** WITH 3-STATE OUTPUTS

SCES027 - JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		vcct	MIN	TYP‡	MAX	UNIT
Vон		I _{OH} = -100 μA		MIN to MAX	VCC-0	.2		
		I _{OH} = -6 mA,	V _{IH} = 1.7 V	2.3 V	2			
			V _{IH} = 1.7 V	2.3 V	1.7			v
	I _{OH} = -12 mA	V _{IH} = 2 V	2.7 V	2.2			V	
			V _{IH} = 2 V	3 V	2.4			
		I _{OH} = -24 mA,	V _{IH} = 2 V	3 V	2			
		I _{OL} = 100 μA		MIN to MAX			0.2	
		I _{OL} = 6 mA,	V _{IL} = 0.7 V	2.3 V			0.4	
VOL		10 1	V _{IL} = 0.7 V	2.3 V			0.7	V
		I _{OL} = 12 mA	V _{IL} = 0.8 V	2.7 V			0.4	
		I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V			0.55	
lį		V _I = V _{CC} or GND		3.6 V			±5	μА
		V _I = 0.7 V		0.01/	45		,	μА
		V _I = 1.7 V		2.3 V	-45			
li(hold)		V _I = 0.8 V		9.1/	75			
		V _I = 2 V		3 ∨	-75			
		V _I = 0 to 3.6 V		3.6 V			±500	
loz§		VO = VCC or GND		3.6 V			±10	μА
Icc		V _I = V _{CC} or GND,	I _O = 0	3.6 V			40	μА
ΔICC		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V		4		pF
Cio	A or B ports	VO = VCC or GND		3.3 V		8		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V	
				MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	150	0	150	0	150	MHz
	Pulse duration	LE↑	3.3		3.3		3.3		ns
t _w	ruise duration	CLK high or low	3.3		3.3		3.3		
	Setup time	Data before CLK↑	2.3		2.4		2.1		ns
١.		Data before LE↓, CLK↑	2		1.6		1.6		
t _{su}		Data before LE↓, CLK↓	1.3		1.2		1.1		
		, CLKEN before CLK↑	2		2		1.7		
	Hold time	Data after CLK↑	0.7	,	0.7		0.8		
		Data after LE↓, CLK↑	1.3		1.6		1.4		
th ,		Data after LE↓, CLK↓	1.7		2		1.7		ns
		CLKEN after CLK1	0.3		0.5		0.6		

[‡] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C. § For I/O ports, the parameter I_{OZ} includes the input leakage current.

SN74ALVCH16601 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES027 - JULY 1995

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

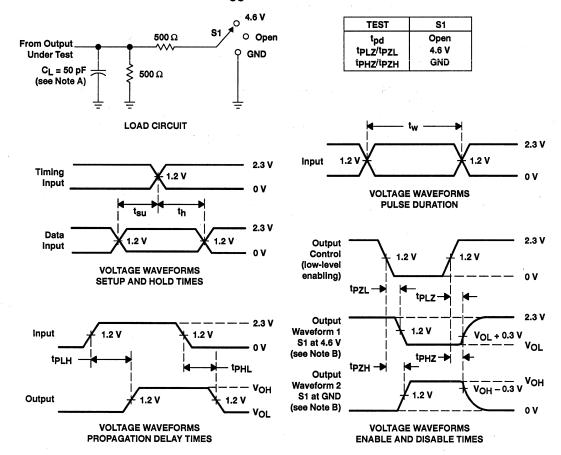
PARAMETER	FROM (INPUT)	TO (OUTPUT)		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V	
			MIN	MAX	MIN	MAX	MIN .	MAX	
fmax			150		150		150		MHz
	A or B	B or A	1.3	4.9		4.6	,	4.1	
^t pd	LEAB or LEBA	A or B	1.2	5.6	1.	5.3		4.7	ns
·	CLKAB or CLKBA	A or B	1.7	6.2		5,8		5	
t _{en}	OEAB or OEBA	B or A	1.2	6.1		6.1		5.2	ns
t _{dis}	OEAB or OEBA	B or A	2.1	5.4		4.8		4.4	ns

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
	Danier dia da Alamana da Alamana	Outputs enabled	C _L = 50 pF, f = 10 MHz	41	52	pF
C _{pd}	Power dissipation capacitance	Outputs disabled		` 6	6	

SCES027 - JULY 1995

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$



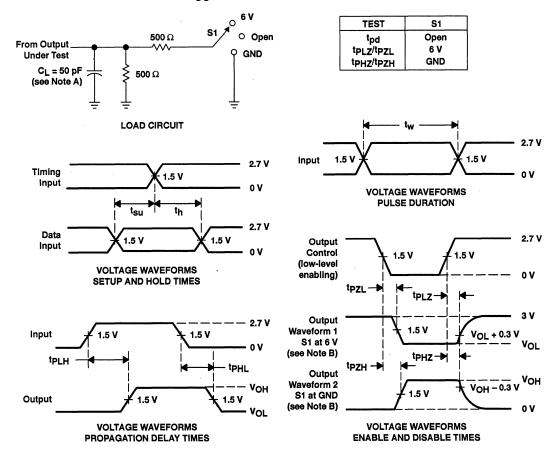
- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms



SCES027 - JULY 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 - Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tod.

Figure 2. Load Circuit and Voltage Waveforms

SCES026 - JULY 1995

- Member of the Texas Instruments Widebus™ Family
- EPIC ™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- UBT™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode
- Output Ports Have Equivalent 26-Ω Series Resisters, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit universal bus transceiver is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH162601 combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

DGG OR DL PACKAGE (TOP VIEW)

		TT		l .
OEAB [1	O	56	CLKENAB
LEAB[2		55	CLKAB
A1 [54]B1
GND [4		53	GND
A2 [5		52] B2
A3 [6		51] B3
v _{cc} []7		50] v _{cc}
A4 [8		49] B4
A5 [9		48] B5
A6 [] B6
GND [11		46] GND
A7 [45] B7
A8 [] B8
A9 [] B9
A10 [15		42] B10
A11 [16			B11
A12			40	B12
GND [39	GND
A13 [] B13
A14 [] B14
A15 [21		36	B15
v _{cc} [22]v _{cc}
A16	23			B16
A17 [33	B17
GND [GND
A18 [B18
OEBA [] CLKBA
LEBA [28		29	CLKENBA

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable (CLKENAB and CLKENBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. When OEAB is low, the outputs are active. When OEAB is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, CLKBA, and CLKENBA.

The B-port outputs include $26-\Omega$ series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

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SCES026 - JULY 1995

description (continued)

The SN74ALVCH162601 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH162601 is characterized for operation from -40°C to 85°C.

FUNCTION TABLET

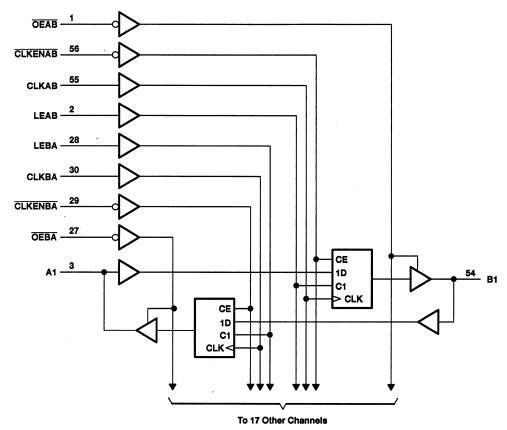
	ı	NPUTS			OUTPUT
CLKENAB	OEAB	LEAB	CLKAB	Α	В
Х	Н	Х	Х	Х	Z
х	L	Н	X	L	L
х	L	Н	Х	Н	Н
н	L	L	Х	Х	в ₀ ‡
н	L	L	X	Χ	В ₀ ‡ В ₀ ‡
L	L	L	↑	L	L
L	L	L	1	Н	н
L	L	L	L	Х	в ₀ ‡
L	L	L	Н	Х	В ₀ ‡ В ₀ §

[†] A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.

[‡] Output level before the indicated steady-state input conditions were established

[§] Output level before the indicated steady-state input conditions were established, provided that CLKAB is low before LEAB goes low

logic diagram (positive logic)



SN74ALVCH162601 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES026 - JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)	0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): I	DGG package 1 W
	DL package 1.4 W
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	٧
V	High level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
VIH	High-level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7		٧
V.,	Lour level input veltere	V _{CC} = 2.7 V to 3.6 V		0.8	V
VIL	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V		0.7	· ·
VI	Input voltage		0	VCC	V
Vo	Output voltage		0	Vcc	V
		V _{CC} = 2.3 V		-12	
ЮН	High-level output current (A port)	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 2.3 V		12	
lOL	Low-level output current (A port)	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
	·	V _{CC} = 2.3 V		-6	
ЮН	High-level output current (B port)	V _{CC} = 2.7 V		-8	mA
		V _{CC} = 3 V		-12	
		V _{CC} = 2.3 V		6	
loL	Low-level output current (B port)	V _{CC} = 2.7 V		8	mA
		V _{CC} = 3 V		12	
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SCES026 - JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER	TEST C	ONDITIONS	vcct	MIN	TYP‡	MAX	UNIT	
		I _{OH} = -100 μA		MIN to MAX	V _{CC} -0	.2			
		I _{OH} = -4 mA,	V _{IH} = 1.7 V	2.3 V	1.9				
V (D-		Jan. 6 mA	V _{IH} = 1.7 V	2.3 V	1.7			V	
VOH (B	port)	IOH = -6 mA	V _{IH} = 2 V	3 V	2.4			V	
		I _{OH} = -8 mA,	V _{IH} = 2 V	2.7 V	2				
		I _{OH} = -12 mA,	V _{IH} = 2 V	3 V	2				
		I _{OH} = -100 μA		MIN to MAX	V _{CC} -0	.2			
		I _{OH} = -6 mA,	V _{IH} = 1.7 V	2.3 V	2				
V (A -			V _{IH} = 1.7 V	2.3 V	1.7			V	
VOH (A I	OH (A port)	I _{OH} = −12 mA	V _{IH} = 2 V	2.7 V	2.2			v	
		V _{IH} = 2 V	3 V	2.4					
		I _{OH} = -24 mA,	V _{IH} = 2 V	3 V	2				
		I _{OL} = 100 μA		MIN to MAX			0.2		
V _{OL} (B port)	I _{OL} = 4 mA,	V _{IL} = 0.7 V	2.3 V			0.4			
	oot)	I _{OL} = 6 mA	V _{IL} = 0.7 V	2.3 V			0.55	v	
	borty	IOL = VIIIA	V _{IL} = 0.8 V	3 V			0.55		
		I _{OL} = 8 mA,	V _{IL} = 0.8 V	2.7 V			0.6		
		I _{OL} = 12 mA,	V _{IL} = 0.8 V	3 V			0.8		
		I _{OL} = 100 μA		MIN to MAX			0.2		
		IOL = 6 mA,	V _{IL} = 0.7 V	2.3 V			0.4		
VOL (A p	oort)	I _{OL} = 12 mA	V _{IL} = 0.7 V	2.3 V			0.7	٧	
		IOL = 12 IIIA	V _{IL} = 0.8 V	2.7 V			0.4		
		I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V			0.55		
l _l		V _I = V _{CC} or GND		3.6 V			±5	μA	
	-	V ₁ = 0.7 V		2.3 V	45				
		V _I = 1.7 V		2.5 V	-4 5				
I _I (hold)		V _I = 0.8 V		3 V	75			μА	
	V _I = 2 V]	-75					
		V _I = 0 to 3.6 V		3.6 V			±500		
loz§		VO = VCC or GND		3.6 V			±10	μΑ	
Icc		V _I = V _{CC} or GND,	1O = 0	3.6 V ·			40	μΑ	
ΔICC		One input at V _{CC} - 0.6 V,	Other inputs at VCC or GND	3 V to 3.6 V			750	μΑ	
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V		4		рF	
Cio	A or B ports	VO = VCC or GND		3.3 V		8		pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions. ‡ All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C. § For I/O ports, the parameter I_{OZ} includes the input leakage current.

SN74ALVCH162601 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES026 - JULY 1995

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V _{CC} = 2.5 V ± 0.2 V				V _{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX		
fclock	Clock frequency		. 0	140	0	150	0	150	MHz	
	v Pulse duration	LE high	3.3		3.3		3.3			
t _w Pulse duration	CLK high or low	3.3		3.3		3.3		ns		
		Data before CLK high	2.3		2.4		2.1			
		Data before LE low, CLK high	2		1.6		1.6			
t _{su}	Setup time	Data before LE low, CLK low	1.3		1.2		1.1		ns	
		CLKEN before CLK high	2		2		1.7			
		Data after CLK high	0.7		0.7		0.8			
	Data after LE low, CLK high	1.3		1.6		1.4				
чh	t _h Hold time	Data after LE low, CLK low	1.7		2		1.7		ns	
		CLKEN after CLK high	0.3		0.5		0.6			

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

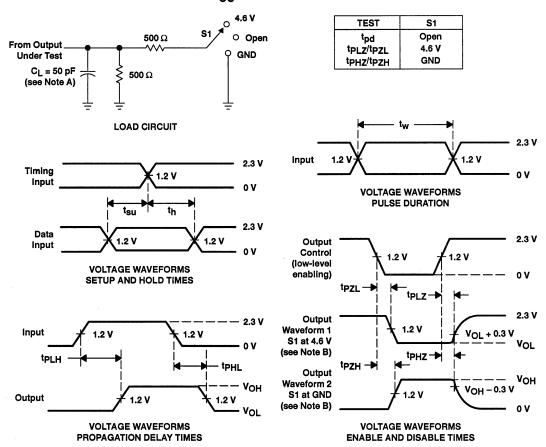
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} =	UNIT	
	(INPOT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			140		150		150		MHz
t _{pd}	Α	В	1.8	5.4		5.2	1.6	4.5	ns
^t pd	В	Α	1.3	4.9		4.6	1	4.1	ns
t _{pd}	LEAB	В	1.5	6.1		5.9	1.5	5.1	ns
^t pd	LEBA	Α	1.4	5.6		5.3	1	4.7	ns
^t pd	CLKAB	В	2	6.7		6.3	1.6	5.5	ns
t _{pd}	CLKBA	Α	1.8	6.2		5.8	1.4	5	ns
t _{en}	OEAB	. В	1.7	6.6		6.7	1.6	5.7	ns
^t dis	OEAB	В	2.5	5.9		5.3	1.8	4.8	ns
t _{en}	ŌĒBĀ	Α	1.2	6		6.1	1.1	5.2	ns
^t dis	ŌĒBĀ	Α	2.1	5.4		4.8	1.6	4.4	ns

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V TYP	V _{CC} = 3.3 V ± 0.3 V	UNIT	
<u> </u>	Power dissipation capacitance	Outputs enabled	O. 50 aE 4 10 MH-	41	50	ρF
C _{pd}	rowei dissipation capacitance	Outputs disabled	C _L = 50 pF, f = 10 MHz	6	. 6	pr

SCES026 - JULY 1995

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$

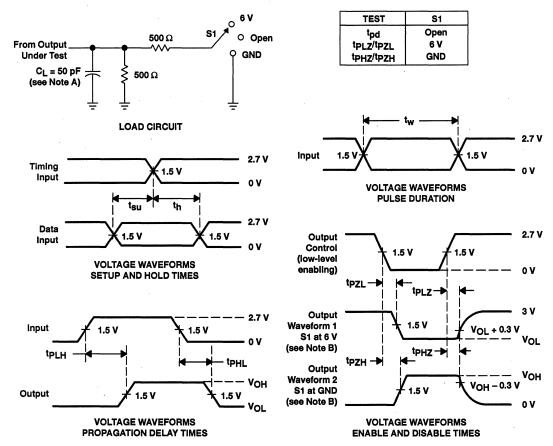


- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpl 7 and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms

SCES026 - JULY 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

SN74ALVCH16646 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCES032-JULY 1995

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit bus transceiver and register is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16646 can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74ALVCH16646.

Output-enable (\overline{OE}) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data.

DGG OR DL PACKAGE (TOP VIEW)

		_	_	ì
1DIR	1	U	56	10E
ICLKAB] 1CLKBA
1SAB			54] 1SBA
GND [4		53	GND
1A1 [5] 1B1
1A2 [1B2
V _{CC} [7] v _{cc}
1A3 [8		49] 1B3
1A4 [9		48] 1B4
1A5 [10] 1B5
GND [] GND
1A6 [12] 1B6
1A7 [13		44] 1B7
1A8 [] 1B8
2A1 [15		42] 2B1
2A2 [16		41	2B2
2A3 [17] 2B3
GND [18] GND
2A4 [19] 2B4
2A5 [20		37	2B5
2A6 [36] 2B6
v _{cc} [22		35	ī v _{cc}
2A7 [23		34] 2B7
2A8 [24] 2B8
GND [25] GND
2SAB [] 2SBA
2CLKAB [] 2CLKBA
2DIR	28		29] 2 <u>OE</u>
				•

DIR determines which bus receives data when \overline{OE} is low. In the isolation mode (\overline{OE} high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16646 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16646 is characterized for operation from -40°C to 85°C.

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SN74ALVCH16646 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS SCES032-JULY 1995

FUNCTION TABLE

INPUTS						DATA	A I/Os	OPERATION OR FUNCTION
ŌĒ	DIR	CLKAB	CLKBA	SAB	SBA	A1 – A8	B1 - B8	OPERATION OR FUNCTION
Х	Х	1	Х	X	Х	Input	Unspecified†	Store A, B unspecified†
Χ	X	Х	1	X	Х	Unspecified†	Input	Store B, A unspecified†
Н	Х	↑	1	Х	Х	Input	Input	Store A and B data
Н	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	Х	Х	Х	L	Output	Input	Real-time B data to A bus
L	L	Х	H or L	Χ	Н	Output	Input	Stored B data to A bus
L	Н	Х	Х	L	Х	Input	Output	Real-time A data to B bus
·L	Н	H or L	X	Н	Х	Input	Output	Stored A data to B bus

[†] The data output functions may be enabled or disabled by various signals at the \overline{OE} and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition of the clock inputs.



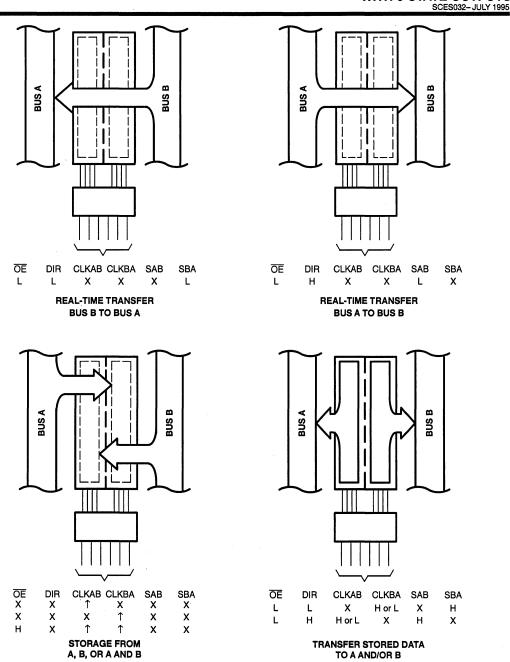
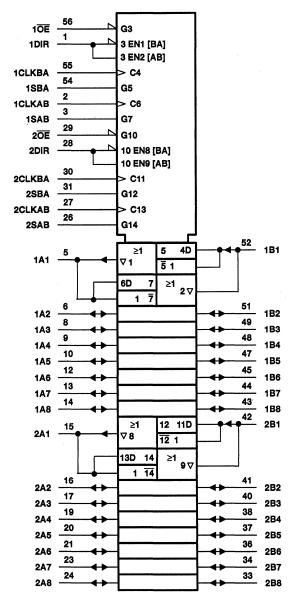


Figure 1. Bus-Management Functions



logic symbol†

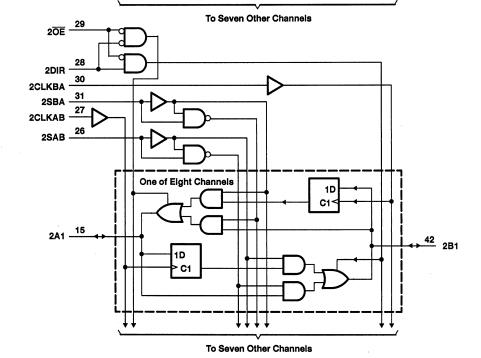


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

52 1B1

C1

logic diagram (positive logic) 10E 1DIR 1CLKBA 1SBA 1SAB 1SAB 1SAB 1SAB





SN74ALVCH16646 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCES032-JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Overhouselters respective	051144 4611
Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)	0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	
Output voltage range, VO (see Notes 1 and 2)	V to V _{CC} + 0.5 V
input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range, T _{sto}	

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		2.3	3.6	٧
V	Link level inner trailing	V _{CC} = 2.3 V to 2.7 V	1.7		V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		ı v
V	Law level input veltage	V _{CC} = 2.3 V to 2.7 V		0.7	v
VIL	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	v
VI	Input voltage		0	VCC	٧
VO	Output voltage		0	Vcc	٧
		V _{CC} = 2.3 V		-12	
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 2.3 V		12	
loL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	1
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN74ALVCH16646 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCES032-JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAME	TER	TEST CO	ONDITIONS	vcct	MIN	TYP‡	MAX	UNIT
		I _{OH} = -100 μA		MIN to MAX	VCC-C).2		
		I _{OH} = −6 mA,	V _{IH} = 1.7 V	2.3 V	2			
V			V _{IH} = 1.7 V	2.3 V	1.7			٧
VOH		IOH = -12 mA	V _{IH} = 2 V	2.7 V	2.2			V
			V _{IH} = 2 V	3 V	2.4			
		I _{OH} = -24 mA,	V _{IH} = 2 V	3 V	2			
		I _{OL} = 100 μA		MIN to MAX			0.2	
		$I_{OL} = 6 \text{ mA},$	V _{IL} = 0.7 V	2.3 V			0.4	
VOL		In. 10 mA	V _{IL} = 0.7 V	2.3 V			0.7	٧
		I _{OL} = 12 mA	V _{IL} = 0.8 V	2.7 V			0.4	
		I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V		0.55		İ
l _l		VI = VCC or GND		3.6 V			±5	μА
		V _I = 0.7 V		2.3 V	45	-		
		V _i = 1.7 V		2.5 V	-45			
I(hold)		V _I = 0.8 V		3 V	75			μА
		V _I = 2 V		3 V	-75			
		V _I = 0 to 3.6 V		3.6 V			±500	
I _{OZ} §		VO = VCC or GND		3.6 V			±10	μА
Icc		VI = VCC or GND,	IO = 0	3.6 V			40	μА
ΔICC		One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА
C _i Cont	trol inputs	VI = VCC or GND		3.3 V				pF
C _{io} A or	B ports	VO = VCC or GND		3.3 V				pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C. § For I/O ports, the parameter I_{OZ} includes the input leakage current.

SN74ALVCH16652 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCES034 - JULY 1995

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit bus transceiver and register is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16652 consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary output-enable (OEAB OEBA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74ALVCH16652.

DGG OR DL PACKAGE (TOP VIEW)

10EAB	1	U	56	h	1 OEBA
1CLKAB					1CLKBA
1SAB					1SBA
GND [53	ĸ	GND
1A1 [50	ĸ	1B1
1A2 [51	ĸ	1B2
v _{cc}					V _{CC}
1A3 [Ω		10	ĸ	1B3
1A4	0		49	ĸ	1B4
1A5 [40	ĸ	1B5
GND [46	ĸ	GND
1A6	12		45	ĸ	1B6
1A7 [12				1B7
1A8 [14				1B8
2A1 [15				2B1
2A2 [41	K	2B2
2A3 [17		40	K	2B3
GND [12		30	ĸ	GND
2A4					2B4
2A4 L					2B5
2A5 [36	K	2B6
v _{cc} [35	ĸ	V _{CC}
2A7	22		34	K	VCC 2B7
2A7 L					2B8
GND [20	ĸ	GND
2SAB			21	K	2SBA
ZSAB [] 2CLKAB []					2CLKBA
20EAB					20EBA
ZOEAB II	20		29	ш	ZUEBA

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it also is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus line are in the high-impedance state, each set of bus lines remains at its last level configuration.

Active bus-hold circuitry is provided to hold unused for floating inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to V_{CC} through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking current-sourcing capability of the driver.

The SN74ALVCH16652 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16652 is characterized for operation from -40°C to 85°C.

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SN74ALVCH16652 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS SCES034 - JULY 1995

FUNCTION TABLE

		INPU'	rs			DATA	A VOT	OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 – A8	B1 – B8	OPERATION OR FUNCTION
L	Н	H or L	H or L	Х	Х	Input	Input	Isolation
L	н	1	1	X	x	Input	Input	Store A and B data
x	Н	1	H or L	X	x	Input	Unspecified [‡]	Store A, hold B
Н	Н	1	1	x‡	x	Input	Output	Store A in both registers
L	X	H or L	1	X	x	Unspecified [‡]	Input	Hold A, store B
L	L	1	1	X	x‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input ^e	Real-time B data to A bus
L	L	X	H or L	X	н	Output	Input	Stored B data to A bus
н	Н	X	X	L	×	Input	Output	Real-time A data to B bus
н	Н	H or L	X	н	×	Input	Output	Stored A data to B bus
Н	L	H or L	H or L	Н	н	Output	Output	Stored A data to B bus and stored B data to A bus

[†] The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition of the clock inputs.

[‡] Select control = L; clocks can occur simultaneously

Select control = H; clocks must be staggered in order to load both registers

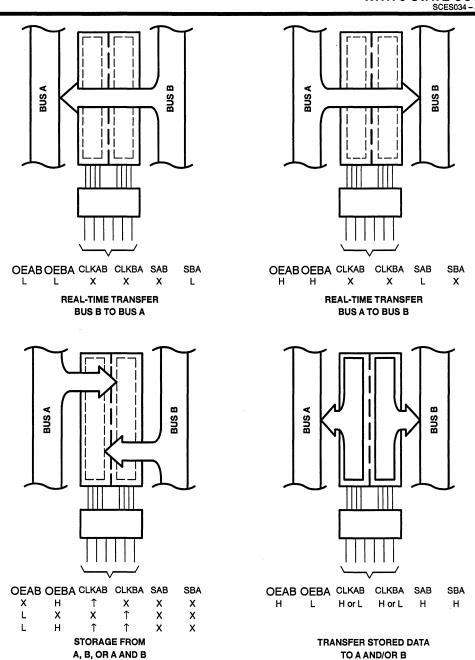
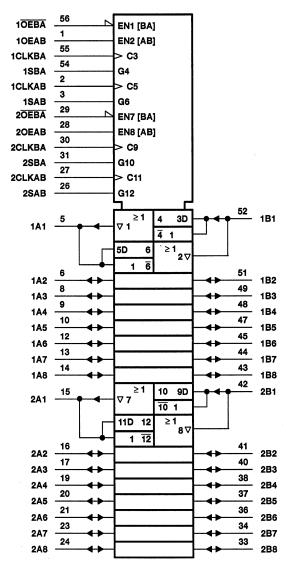


Figure 1. Bus-Management Functions

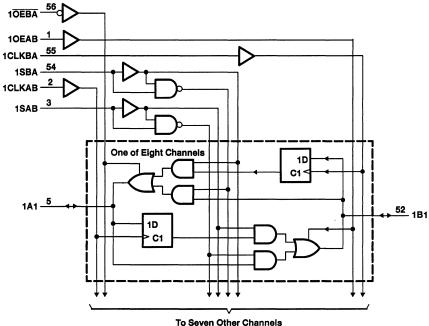


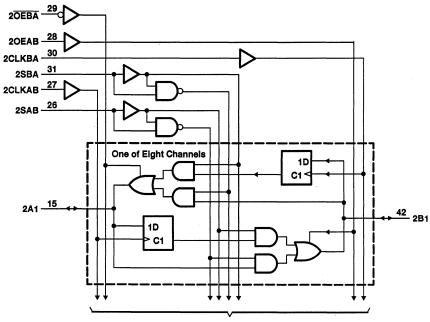
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





To Seven Other Channels



SN74ALVCH16652 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCES034 - JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, VI: Except I/O ports (see Note 1)	0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)0.	5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range, T _{stg}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

	4		MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	٧
	I link level innot value	V _{CC} = 2.3 V to 2.7 V	1.7		V
VIH	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		V
V	Low level input voltage	V _{CC} = 2.3 V to 2.7 V	0.7 V		V
V_{IL}	Low-level input voltage		0.8	'	
٧ı	Input voltage		0	Vcc	٧
٧o	Output voltage		0	Vcc	٧
		V _{CC} = 2.3 V		-12	
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 2.3 V		12	
loL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate	-	0	10	ns/V
TA	Operating free-air temperature		-40	85	•€

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SCES034 - JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER	TEST CO	ONDITIONS	vcct	MIN	TYP‡	MAX	UNIT
		I _{OH} = -100 μA		MIN to MAX	V _{CC} -0	.2		
		I _{OH} = -6 mA,	V _{IH} = 1.7 V	2.3 V	2			
V			V _{IH} = 1.7 V	2.3 V	1.7			v
VOH		I _{OH} = -12 mA	V _{IH} = 2 V	2.7 V	2.2	_		, v
			V _{IH} = 2 V	3 V	2.4			
		I _{OH} = -24 mA,	V _{IH} = 2 V	3 V	2			
		I _{OL} = 100 μA		MIN to MAX			0.2	
		I _{OL} = 6 mA,	V _{IL} = 0.7 V	2.3 V			0.4	
VOL		I _{OL} = 12 mA	V _{IL} = 0.7 V	2.3 V			0.7	٧
		IOL = 12 IIIA	V _{IL} = 0.8 V	2.7 V			0.4	
		I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V			0.55	
lj		VI = VCC or GND		3.6 V			±5	μA
		V _j = 0.7 V		2.3 V	45			
		V _I = 1.7 V		2.5 V	-45			
I _I (hold)		V _I = 0.8 V		3 V	75			μA
		V _I = 2 V		3 V	-75			
		V _I = 0 to 3.6 V		3.6 V			±500	
I _{OZ} §		VO = VCC or GND		3.6 V			±10	μА
Icc		$V_I = V_{CC}$ or GND,	IO = 0	3.6 V			40	μА
Δlcc		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V				pF
Cio	A or B ports	VO = VCC or GND		3.3 V				pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



[‡] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C. § For I/O ports, the parameter I_{OZ} includes the input leakage current.

SCES052 - JULY 1995

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 20-bit flip-flop is designed specifically for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16721 20 flip-flops are edgetriggered D-type flip-flops with qualified clock storage. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs if the clock-enable (CLKEN) input is low. If CLKEN is high, no data is stored.

A buffered output-enable (OE) input places the 20 outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive

DGG OR DL PACKAGE (TOP VIEW)

ŌĒ			CLK
Q1]D1
Q2] D2
GND]GND
Q3] D3
Q4		51] D4
Vcc	7]v _{cc}
Q5	8] D5
Q6	9	48] D6
Q7		47] D7
GND		46] GND
Q8	12	45] D8
	13] D9
Q10	14	43	D10
Q11	15		D11
Q12	16	41	D12
Q13		40	D13
GND	18	39	GND
Q14		38	D14
Q15			D15
Q16		36	D16
Vcc	22	35]v _{cc}
Q17		34	D17
Q18	24		D18
GND		32]GND
Q19		31	D19
Q20	27	30	D20
NC	28	29	CLKEN

NC - No internal connection

provide the capability to drive bus lines without need for interface or pullup components. OE does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16721 is available in Tl's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16721 is characterized for operation from -40°C to 85°C.

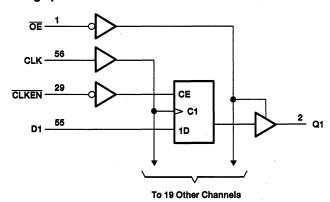
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SCES052 - JULY 1995

FUNCTION TABLE (each flip-flop)

	INPU	ITS		OUTPUT
ŌĒ	CLKEN	CLK	D	a
L	Н	Х	Х	QO
L	L	1	Н	Н
l L	L	1	L	L
L	L	L or H	Х	Q ₀
Н	Χ .	×	Х	Z ·

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, V _O (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through each V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DG	
	package 1.4 W
Storage temperature range, Teta	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	V
.,	High leveling Avelone	V _{CC} = 2.3 V to 2.7 V	1.7		V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		1 °
	Law lavel input veltage	V _{CC} = 2.3 V to 2.7 V		0.7	V
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	
VI	Input voltage		0	Vcc	V
٧ _O	Output voltage		0	VCC	٧
		V _{CC} = 2.3 V		-12	
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	1
		V _{CC} = 2.3 V		12	
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P.	ARAMETER	TEST CO	NDITIONS	v _{cc} †	MIN	TYP‡	MAX	UNIT	
		I _{OH} = -100 μA		MIN to MAX	V _{CC} -0	.2			
		I _{OH} = −6 mA,	V _{IH} = 1.7 V	2.3 V	2				
		I _{OH} = -12 mA,	V _{IH} = 1.7 V	2.3 V	1.7			.,	
VOH		I _{OH} = -12 mA,	V _{IH} = 2 V	2.7 V	2.2			V	
		I _{OH} = −12 mA,	V _{IH} = 2 V	3 V	2.4				
		I _{OH} = -24 mA,	V _{IH} = 2 V	3 V	2				
		I _{OL} = 100 μA		MIN to MAX			0.2		
		I _{OL} = 6 mA,	V _{IL} = 0.7 V	2.3 V			0.4		
VOL		I _{OL} = 12 mA,	V _{IL} = 0.7 V	2.3 V			0.7	7 . V	
		I _{OL} = 12 mA,	V _{IL} = 0.8 V	2.7 V			0.4	0.4	
		I _{OL} = 24 mA,	$OL = 24 \text{ mA}, \qquad V_{ L} = 0.8 \text{ V}$ 3 V				0.55		
lį .		VI = VCC or GND		3.6 V			±5	μА	
		V _I = 0.7 V			45				
		V _I = 1.7 V		2.3 V	-45				
I)(hold)	V _I = 0.8 V		9.1/	75			μА	
		V ₁ = 2 V		3 V	-75		-		
		V _I = 0 to 3.6 V		3.6 V			±500		
loz		VO = VCC or GND		3.6 V			±10	μА	
Icc		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			40	μA	
Δlcc		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА	
	Control inputs					3.5			
Ci	Data inputs	V _I = V _{CC} or GND		3.3 V		6		pF	
Cio	Data inputs	V _O = V _{CC} or GND		3.3 V		7		pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.



SCES052 - JULY 1995

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figures 1 and 2)

			V _{CC} =		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX		
fclock	Clock frequency		0	150	0	150	0	150	MHz	
t _w	Pulse duration, CLK high or low		3.3		3.3		3.3		ns	
		Data before CLK↑	4		3.6		3.1			
t _{su}	Setup time	CLKEN before CLKT	3.4		3.1		2.7		ns	
	Hold time	Data after CLK↑	0		0		0			
^t h	noid time	CLKEN after CLK1	0		0		0		ns	

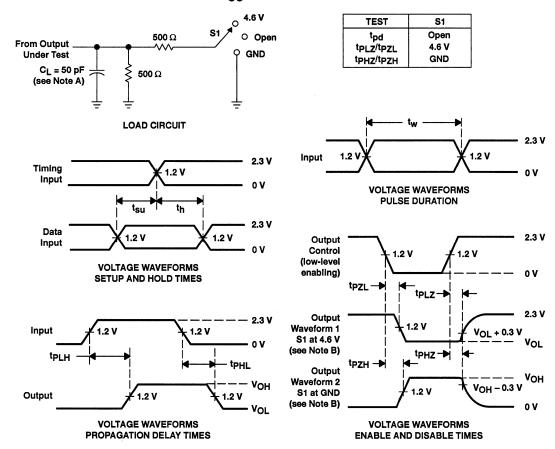
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
	(INPOT)		MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			150		150		150		MHz
t _{pd}	CLK	Q	1	7	1	5.7	1	4.9	ns
t _{en}	ŌĒ	Q .	1	7.4	1	6.5	1	5.4	ns
^t dis	ŌĒ	Q	1	6.2	1	5.1	1	4.8	ns

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
			TYP	TYP		
C .	Power dissipation capacitance	Outputs enabled	Cı = 50 pF. f = 10 MHz	55	59	ρF
C _{pd}	rower dissipation capacitance	Outputs disabled	C _L = 50 pF, f = 10 MHz	46	49	PF

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$

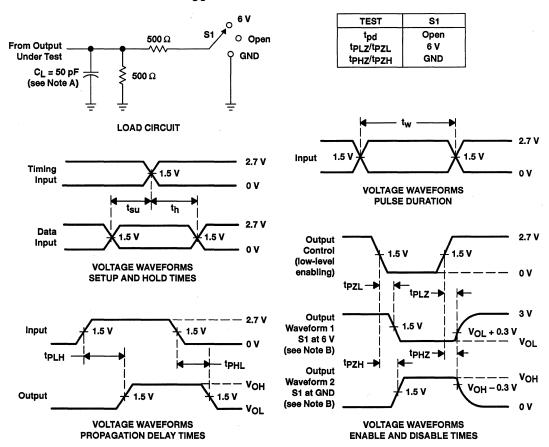


- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzl and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \Omega$, $t_{f} \leq 2.5 \text{ ns}$, $t_{f} \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tod.

Figure 2. Load Circuit and Voltage Waveforms

SCES035 - JULY 1995

- Member of the Texas Instruments
 Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 10-bit flip-flop is designed for 2.3-V to 3.6-V V_{CC} operation.

The flip-flops of the SN74ALVCH16820 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable (\overline{OE}) input can be used to place the ten outputs in either a normal logic state (high or low logic level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

DGG OR DL PACKAGE (TOP VIEW)

10E	1	O	56	CLK
1Q1] D1
1Q2			54	NC
GND			53] GND
2Q1			52	D2
2Q2			51	NC
v_{cc}] 7		50] v _{cc}
3Q1				D3
3Q2			48]NC
4Q1			47	D4
GND	11		46	GND
4Q2			45	NC
5Q1] D5
5Q2			43	NC
6Q1			42	D6
6Q2	16		41	NC
7Q1			40	D7
GND	18		39] GND
7Q2			38	NC
8Q1	20		37] D8
8Q2			36	NC
V_{CC}	22] v _{cc}
9Q1] D9
9Q2	24			NC
GND	25] GND
10Q1	26			D10
10Q2	_		30]NC
2 0E	[28		29	NC
				•

NC - No internal connection

OE input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16820 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16820 is characterized for operation from -40°C to 85°C.

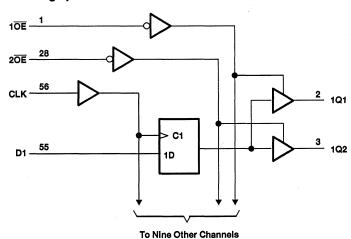
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FUNCTION TABLE (each flip-flop)

INPUTS			OUTPUT
OE _n t	CLK	D	Q _n †
L	1	Н	·H
L	↑	L	L
L	L	Х	Q ₀
Н	X	Х	Z

†n = 1.2

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range, T _{stq}	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.



recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage		2.3	3.6	V	
	High level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7		V	
VIH	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			
V.,	Low level input veltage	V _{CC} = 2.3 V to 2.7 V		0.7	V	
VIL	Low-level input voltage VCC = 2.7 V to 3.6 V			0.8	v	
VI	Input voltage		0	VCC	V	
٧o	Output voltage		0	VCC	٧	
		V _{CC} = 2.3 V		-12	?	
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA	
		V _{CC} = 3 V		-24		
		V _{CC} = 2.3 V		12		
loL	Low-level output current	V _{CC} = 2.7 V		12	mA	
	V _{CC} = 3 V			24		
Δt/Δν	Input transition rise or fall rate		0	10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS		v _{cc} t	MIN	TYP‡	MAX	UNIT	
		I _{OH} = -100 μA		MIN to MAX	V _{CC} -0	.2			
		I _{OH} = -6 mA,	V _{IH} = 1.7 V	2.3 V	2				
V			V _{IH} = 1.7 V	2.3 V	1.7			· v	
VOH		I _{OH} = -12 mA	V _{IH} = 2 V	2.7 V	2.2			V	
			V _{IH} = 2 V	3 V	2.4				
		I _{OH} = -24 mA,	V _{IH} = 2 V	3 V	2				
	· · · · · · · · · · · · · · · · · · ·	I _{OL} = 100 μA		MIN to MAX			0.2		
		I _{OL} = 6 mA,	V _{IL} = 0.7 V	2.3 V			0.4	v	
VOL		10 4	V _{IL} = 0.7 V	2.3 V			0.7		
		I _{OL} = 12 mA	V _{IL} = 0.8 V	2.7 V			0.4		
		I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V			0.55		
lj		V _I = V _{CC} or GND		3.6 V			±5	μA	
		$V_{I} = 0.7 \text{ V}$ $V_{I} = 1.7 \text{ V}$ $V_{I} = 0.8 \text{ V}$		0.01/	45				
				2.3 V	-45				
I(hold)				274	75			μА	
		V _I = 2 V		3 V	-75				
		V _I = 0 to 3.6 V		3.6 V			±500	1	
loz		VO = VCC or GND		3.6 V			±10	μА	
Icc		V _I = V _{CC} or GND,	I _O = 0	3.6 V	Ī		40	μА	
Δlcc		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА	
Cor	Control inputs			1		3.5			
Ci	Data inputs	V _I = V _{CC} or GND		3.3 V		6		рF	
Со	Outputs	VO = VCC or GND		3.3 V		7		pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions. \ddagger All typical values are at V_{CC} = 3.3 V, T_A = 25°C.



SN74ALVCH16820 3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS

SCES035 - JULY 1995

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		V _{CC} = ± 0.	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
		MIN	MAX	MIN	MAX	MIN	MAX		
fclock	Clock frequency	0	150	0	150	0	150	MHz	
t _w	Pulse duration, CLK high or low	3.3		3.3		3.3		ns	
tsu	Setup time, data before CLK↑	1.7		1.8		1.4		ns	
th	Hold time, data after CLK↑	1.1		1.1		1		ns	

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

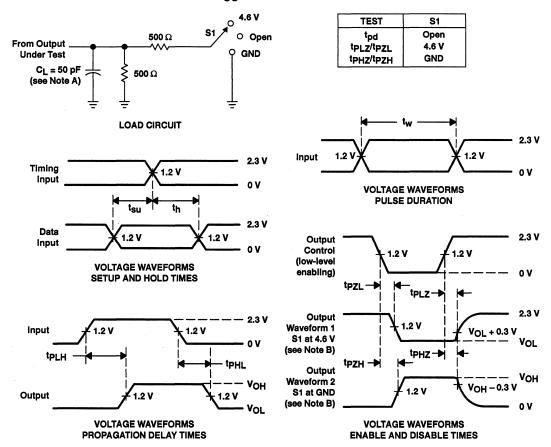
PARAMETER	FROM	TO	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	1 1
f _{max}			150		150		150		MHz
t _{pd}	CLK	Q	1	6.5		5.5	. 1	4.8	ns
t _{en}	ŌĒ	Q	1	6.9		6.1	1	5	ns
^t dis	ŌĒ	Q	1.3	5.9		5	1	4.5	ns

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT	
				TYP	TYP	
	Dayyar dissination consultance	Outputs enabled	C: 50 pF f 10 MHz	60	63	pF
C _{pd}	Power dissipation capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	38	46	l br

SCES035 - JULY 1995

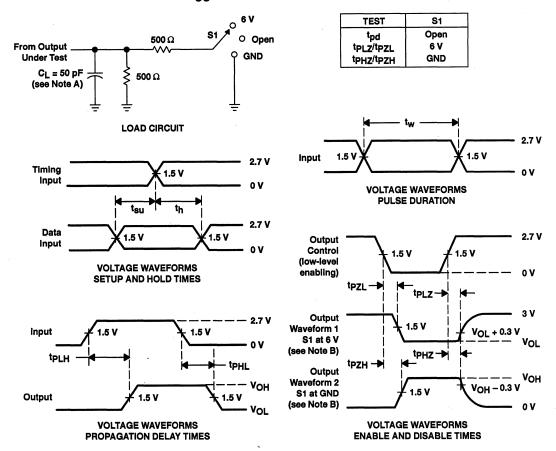
PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$



- NOTES: A. C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \Omega$, $t_{f} \leq 2.5 \text{ ns}$, $t_{f} \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tod.

Figure 2. Load Circuit and Voltage Waveforms

SN74ALVCH162820 3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS AND 3-STATE OUTPUTS

SCES012 - JULY 1995

DGG OR DL PACKAGE Member of the Texas Instruments (TOP VIEW) Widebus™ Family EPIC™ (Enhanced-Performance Implanted 10E [] 1 56 CLK **CMOS) Submicron Process** 1Q1 **[**]2 55 D1 Output Ports Have Equivalent 26- Ω Series 54 NC 1Q2 **[**]3 Resistors, So No External Resistors Are GND []4 53 GND Required. 2Q1 **[**]5 52 N D2 ESD Protection Exceeds 2000 V Per 51 NC 2Q2 **[**]6 MIL-STD-883C, Method 3015; Exceeds V_{CC} []7 50 V_{CC} 200 V Using Machine Model 49 D3 3Q1 🛮 8 (C = 200 pF, R = 0)3Q2 🛮 9 48 NC Latch-Up Performance Exceeds 250 mA 4Q1 **∏**10 47 D4 Per JEDEC Standard JESD-17 GND [] 11 46 GND 4Q2 12 45 NC Bus Hold on Data Inputs Eliminates 5Q1 13 44 D5 the Need for External Pullup/Pulldown Resistors 5Q2 **∏**14 43 NC 42 D6 6Q1 **1**15 Package Options Include Plastic Shrink 6Q2 116 41 NC Small-Outline (DL) and Thin Shrink 7Q1 🛮 17 40 D7 Small-Outline (DGG) Packages GND 118 39 GND 7Q2 **[** 19 38 NC description 8Q1 []20 37 T D8 This 10-bit flip-flop is designed for 2.3-V to 3.6-V 8Q2 []21 36 NC V_{CC} operation. V_{CC} [] 22 9Q1 [] 23 35 V_{CC} 34 🛛 D9 The SN74ALVCH162820 flip-flops are edge-9Q2 **[**] 24 triggered D-type flip-flops. On the positive 33 NC GND II 25 32 | GND transition of the clock (CLK) input, the device 10Q1 **[**]26 31 D10 provides true data at the Q outputs. 10Q2 1 27 30 NC A buffered output-enable (OE) input can be used

NC - No internal connection

29 NC

20E 28

impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to sink up to 12 mA, include $26-\Omega$ resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

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to place the eight outputs in either a normal logic state (high or low logic levels) or a highSCES012 - JULY 1995

description (continued)

The SN74ALVCH162820 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

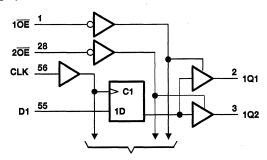
The SN74ALVCH162820 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each flip-flop)

	INPUTS	OUTPUT	
0E _n t	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	L	X	Q ₀
Н	×	Х	Z

†n = 1, 2

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

To Nine Other Channels

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, $I_{ K }(V_1 < 0)$	–50 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3)	: DGG package 1 W
	DL package 1.4 W
Storage temperature range, T _{stg}	–65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

^{2.} This value is limited to 4.6 V maximum.

SN74ALVCH162820 3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS AND 3-STATE OUTPUTS SCES012 - JULY 1995

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
Vcc	Supply voltage					
V	High level input veltage	V _{CC} = 2.3 V to 2.7 V	1.7		V	
VIH	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		٧	
17	Law level input veltage	V _{CC} = 2.3 V to 2.7 V		0.7	V	
VIL	Low-level input voltage VCC = 2.7 V to 3.6 V			0.8	v	
VI	Input voltage	0	Vcc	٧		
VO	Output voltage		0	Vcc	٧	
	High-level output current	V _{CC} = 2.3 V		-6		
ЮН		V _{CC} = 2.7 V		-8	mA	
		V _{CC} = 3 V		-12		
		V _{CC} = 2.3 V		6		
lOL	Low-level output current	V _{CC} = 2.7 V		8	mA	
	•	V _{CC} = 3 V		12		
Δt/Δν	Input transition rise or fall rate		0	10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SCES012 - JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CO	NDITIONS	v _{cc} t	MIN	TYP‡	MAX	UNIT	
		IOH = -100 μA		MIN to MAX	V _{CC} -C).2			
		I _{OH} = -4 mA,	V _{IH} = 1.7 V	2.3 V	1.9				
V		1 CA	V _{IH} = 1.7 V	2.3 V	1.7			v	
VOH		IOH = -6 mA	V _{IH} = 2 V	3 V	2.4			V V	
		IOH = -8 mA,	V _{IH} = 2 V	2.7 V	2				
		I _{OH} = -12 mA,	V _{IH} = 2 V	3 V	2				
		IOL = 100 μA	Αμ 00				0.2		
		IOL = 4 mA,	V _{IL} = 0.7 V	2.3 V			0.4		
		In. 6mA	V _{IL} = 0.7 V	2.3 V			0.55	v	
VOL		IOL = 6 mA	V _{IL} = 0.8 V	3 V			0.55	v	
		I _{OL} = 8 mA,	V _{IL} = 0.8 V	2.7 V			0.6		
		I _{OL} = 12 mA,	$I_{OL} = 12 \text{ mA},$ $V_{IL} = 0.8 \text{ V}$				0.8		
l _l		V _I = V _{CC} or GND		3.6 V			±5	μА	
		V _I = 0.7 V		2.3 V	45				
		V _I = 1.7 V			-45				
l(hold)	V _I = 0.8 V	V _I = 0.8 V		75			μА	
		V _I = 2 V		3 V	-75				
		V _I = 0 to 3.6 V		3.6 V			±500		
loz		VO = VCC or GND		3.6 V		•	±10	μА	
Icc		$V_I = V_{CC}$ or GND,	I _O = 0	3.6 V			40	μА	
ΔICC		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА	
<u> </u>	Control inputs	V ₁ = V _{CC} or GND		3.3 V		3.5		pF	
Ci	Data inputs	V _I ≈ V _{CC} or GND		3.3 V		6		pF	
Co	Outputs	V _I = V _{CC} or GND		3.3 V		7		pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		V _{CC} :	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V	
		MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency	0	150	0	150	0	150	MHz
t _W	Pulse duration, CLK high or low	3.3		3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	1.7		1.8		1.4		ns
th	Hold time, data after CLK↑	1.1		1.1		1		ns

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SN74ALVCH162820 3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS AND 3-STATE OUTPUTS

SCES012 - JULY 1995

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

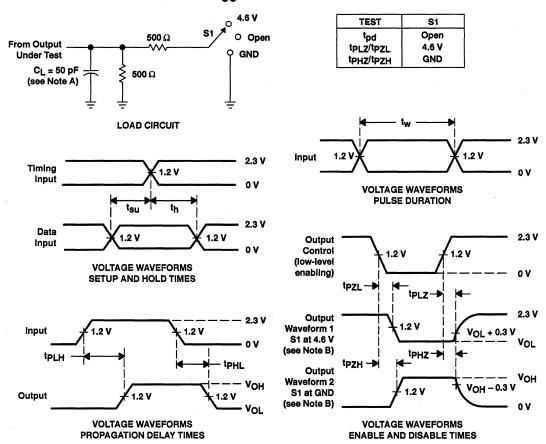
PARAMETER	FROM	TO (OUTPUT)	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INPUT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	
fmax			150		150		150		MHz
^t pd	CLK	œ	1	7		6.2	1	5.4	ns
t _{en}	ŌĒ	Q	1	7.4		6.8	1	5.6	ns
tdis	ŌĒ	Q	1.3	6.4		5.5	1	5	ns

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT	
			TYP	TYP			
	Dower dissination consistence	Outputs enabled	C: 50 = 5 4 10 MU-	68	66	ρF	
C _{pd}	Power dissipation capacitance	Outputs disabled	C _L = 50 pF, f = 10 MHz	39	47	Pr	

SCES012 - JULY 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

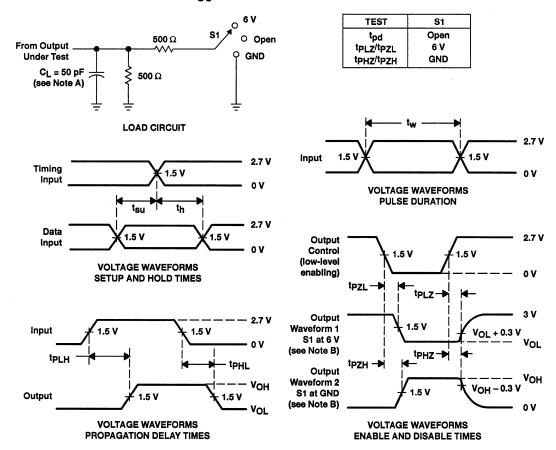


- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpHL and tpLH are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SCES012 - JULY 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \, \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 G. tpHL and tpLH are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

SN74ALVCH16821 3.3-V 20-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

SCES037 - JULY 1995

•	Member of	the Texas	Instruments
	Widebus™	Family	

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 20-bit bus-interface flip-flop is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16821 can be used as two 10-bit flip-flops or one 20-bit flip-flop. The 20 flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable (\overline{OE}) input can be used to place the ten outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

DGG OR DL PACKAGE (TOP VIEW)

10E [₁ ∪	56]1CLK
1Q1 [2	55] 1D1
1Q2 [3	54	1D2
GND [4	53	GND
1Q3 [5	52] 1D3
1Q4 [6		1D4
v _{cc} [7	50] v _{cc}
1Q5 [8] 1D5
1Q6 [9	48] 1D6
1Q7 [10	47] 1D7
GND [11	46] GND
1Q8 [12] 1D8
1Q9 [13] 1D9
1Q10[43] 1D10
2Q1 [15	42	2D1
2Q2 [16	41	2D2
2Q3 [2D3
GND [18] GND
2Q4 [19	38	2D4
2Q5 [20	37] 2D5
2Q6 [36	2D6
v _{cc} [] v _{cc}
2Q7 [23	34	2D7
2Q8 [24	33	2D8
GND [] GND
2Q9 [2D9
2Q10[30	2D10
20E [28	29]2CLK

OE does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16821 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16821 is characterized for operation from -40°C to 85°C.

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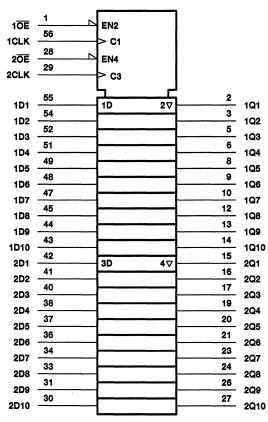


SCES037 - JULY 1995

FUNCTION TABLE (each 10-bit flip-flop)

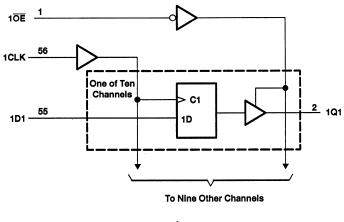
	INPUTS	OUTPUT	
ŌĒ	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	H or L	X	Q ₀
Н	X	Х	Z

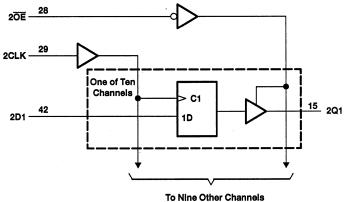
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





SN74ALVCH16821 3.3-V 20-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

SCES037 - JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through each V _{CC} or GND	
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): DG	
DL	package 1.4 W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

		·	MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	V
V	Ligh level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7		v
VIH	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		V
V.,	Low level input voltage	V _{CC} = 2.3 V to 2.7 V		0.7	v
VIL	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	l
VĮ	Input voltage		0	Vcc	V
٧o	Output voltage		0	VCC	٧
		V _{CC} = 2.3 V		-12	
Іон	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 2.3 V		12	
loL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	l
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN74ALVCH16821 3.3-V 20-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS SCES037 - JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P	ARAMETER	TEST (CONDITIONS	vcct	MIN	TYP‡	MAX	UNIT	
		I _{OH} = -100 μA		MIN to MAX	V _{CC} -0	.2			
		I _{OH} = -6 mA,	V _{IH} = 1.7 V	2.3 V	2				
V			V _{IH} = 1.7 V	2.3 V	1.7			v	
VOH		I _{OH} = -12 mA	V _{IH} = 2 V	2.7 V	2.2			v	
			V _{IH} = 2 V	3 V	2.4				
	I _{OH} = -24 mA,	V _{IH} = 2 V	3 V	2					
		l _{OL} = 100 μA		MIN to MAX			0.2		
		I _{OL} = 6 mA,	V _{IL} = 0.7 V	2.3 V			0.4		
V _{OL}	101	V _{IL} = 0.7 V	2.3 V			0.7	V		
		I _{OL} = 12 mA	V _{IL} = 0.8 V	2.7.V			0.4		
		I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V			0.55		
lį .		VI = VCC or GND		3.6 V			±5	μА	
		V _I = 0.7 V		2.3 V	45				
		V _I = 1.7 V		7 2.3 V	-45				
l _l (hold)	V _I = 0.8 V		0.1/	75			μΑ	
•	,	V _I = 2 V		- 3 V	-75				
		V _I = 0 to 3.6 V		3.6 V			±500		
loz		V _O = V _{CC} or GND		3.6 V			±10	μА	
Icc		V _I = V _{CC} or GND,	I _O = 0	3.6 V			40	μА	
Δlcc		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА	
<u> </u>	Control inputs	V. Van au CND		0.01/		3.5			
Ci	Data inputs	V _I = V _{CC} or GND		3.3 V		6		pF	
Со	Outputs	VO = VCC or GND		3.3 V		7		pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		V _{CC} = ± 0.5	2.5 V 2 V	V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency	0	150	0	150	0	150	MHz
t _W	Pulse duration, CLK high or low	3.3		3.3		3.3		ns
tsu	Setup time, data before CLK↑	4.4		3.9		3.4		ns
th	Hold time, data after CLK↑	0		0		0		ns

[‡] All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

SN74ALVCH16821 3.3-V 20-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS SCES037 - JULY 1995

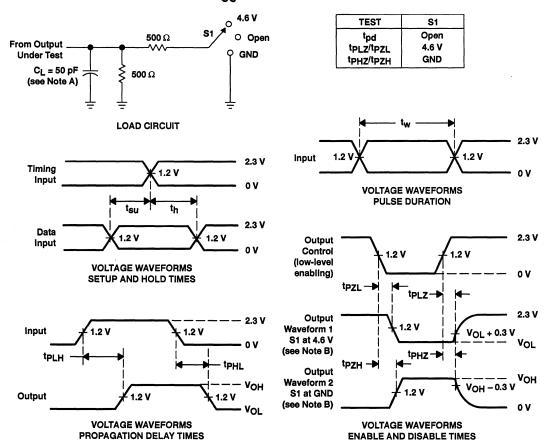
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM	TO (OUTPUT)	V _{CC} = ± 0.	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INPUT)		MIN	MAX	MIN	MAX	MIN	MAX	
fmax			150		150		150		MHz
t _{pd}	CLK	Q	1	6.4		5.3	1	4.5	ns
t _{en}	ŌĒ	Q	1	7.1		6.2	1	5.1	ns
^t dis	. <u>OE</u>	Q	1.4	5.9		5	1	4.6	ns

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
O Bourse dissipation considers		Outputs enabled	C: E0 nE : 10 MHz	36	40	pF
□ ⊃pd	Cpd Power dissipation capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	22	24	pr

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.5 V \pm 0.2 V$

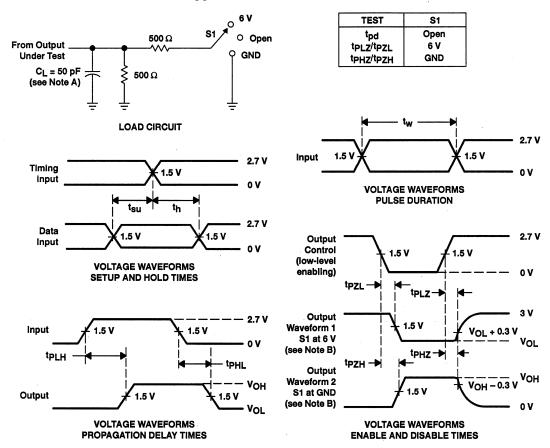


- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns.}$ tf $\leq 2.5 \text{ ns.}$
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpl and tpHI are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SCES037 - JULY 1995

PARAMETER MEASUREMENT INFORMATION $V_{CC} = 2.7 \text{ V}$ AND 3.3 V $\pm 0.3 \text{ V}$



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

SCES038 - JULY 1995

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit bus-interface flip-flop is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16823 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The SN74ALVCH16823 can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable (CLKEN) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking CLKEN high disables the clock buffer, thus latching the outputs. Taking the clear (CLR) input low causes the Q outputs to go low independently of the clock.

DGG OR DL PACKAGE (TOP VIEW)

		U		L
ICLR []1CLK
10E	2		55	1CLKEN
1Q1 [3		54] 1D1
GND [4		53	GND
1Q2 [5		52] 1D2
1Q3 [6		51	1D3
V _{CC} [7		50]v _{cc}
1Q4 [49] 1D4
1Q5 [9		48] 1D5
1Q6 [10		47] 1D6
GND [46] GND
1Q7 [12		45] 1D7
1Q8 [13		44] 1D8
1Q9 [14		43] 1D9
2Q1 [15		42]2D1
2Q2 [16]2D2
2Q3 [17		40	2D3
GND [18		39] GND
2Q4 [19		38	2D4
2Q5 [20		37	2D5
2Q6 [21		36] 2D6
v _{cc} [22		35]∨ _{cc}
2Q7 [23		34] 2D7
2Q8 [24] 2D8
GND [25		32] GND
2Q9 [26		31] 2D9
2OE [27		30	2CLKEN
CLR [28		29]2CLK
			_	

A buffered output-enable (\overline{OE}) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

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SN74ALVCH16823 18-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

SCES038 - JULY 1995

description (continued)

The SN74ALVCH16823 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16823 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 9-bit flip-flop)

	OUTPUT				
ŌĒ	CLR	CLKEN	CLK	D	Q
L	L	Х	Х	Х	L
L	Н	L	1	н	Н
L	Н	L	1	L	L
L	Н	L	L	Χ	Q ₀
L	Н	Н	X	X	Q ₀
Н	Х	X	Х	X	Z .

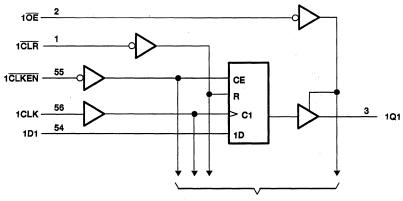
logic symbol†

1OE	2	EN1		
1CLR	1	R2		
1CLKEN	55	G3		
1CLKEN	56	> 3C4		
2OE	27	EN5		
2CLR	28	R6		
2CLKEN	30	G7		
	29	i		
2CLK	-	≥ 7C8	لے	
1D1	54	4D 1, 2	3	1Q1
1D2	52	1,2	<u>`</u> 5	
	51		- 6	1Q2
1D3	49		- 8	1Q3
1D4	48		9	1Q4
1D5	47		10	1Q5
1D6	45		12	1Q6
1D7	44		13	1Q7
1D8	43		14	1Q8
1D9	42		15	1Q9
2D1	41	8D 5, 6	7 16	2Q1
2D2	40	ļ	17	2Q2
2D3	38		19	2Q3
2D4	37		20	2Q4
2D5	36		21	2Q5
2D6	34		23	2Q6
2D7	33		24	2Q7
2D8	31		26	2Q8
2D9				2Q9

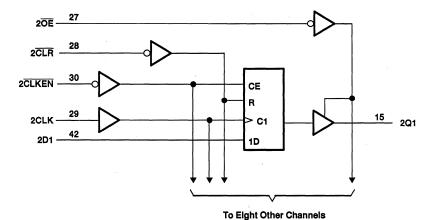
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SCES038 - JULY 1995

logic diagram (positive logic)



To Eight Other Channels



SN74ALVCH16823 18-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

SCES038 - JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} Input voltage range, V_I (see Note 1) Output voltage range, V_O (see Notes 1 and 2) Input clamp current, I_{IK} ($V_I < 0$) Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) Continuous output current, I_O ($V_O = 0$ to V_{CC})	-0.5 V to 4.6 V -0.5 V to V _{CC} + 0.5 V -50 mA -50 mA -50 mA
Continuous current through each V_{CC} or GND	±100 mA
DL pack	age 1.4 W
Storage temperature range, T _{stg}	65°C 10 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage	·	2.3	3.6	٧
V	High level incodes allows	V _{CC} = 2.3 V to 2.7 V	1.7		٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V	Levelevelinevelveltere	V _{CC} = 2.3 V to 2.7 V		0.7	٧
VIL	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	V
VI	Input voltage		0	VCC	٧
۷o	Output voltage		0	Vcc	٧
	High-level output current	V _{CC} = 2.3 V		-12	
ЮН		V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 2.3 V		12	
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SCES038 - JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CO	ONDITIONS	vcct	MIN	TYP‡	MAX	UNIT	
		I _{OH} = -100 μA	`	MIN to MAX	VCC-C).2			
		I _{OH} = -6 mA,	V _{IH} = 1.7 V	2.3 V	2				
V			V _{IH} = 1.7 V	2.3 V	1.7			v	
VOH		I _{OH} = -12 mA	V _{IH} = 2 V	2.7 V	2.2			7 ' I	
	•		V _{IH} = 2 V	3 V	2.4				
		I _{OH} = -24 mA,	V _{IH} = 2 V	3 V	2				
		I _{OL} = 100 μA		MIN to MAX			0.2		
		I _{OL} = 6 mA,	V _{IL} = 0.7 V	2.3 V			0.4		
VOL		la. 10 mA	V _{IL} = 0.7 V	2.3 V			0.7	V	
		I _{OL} = 12 mA	V _{IL} = 0.8 V	2.7 V			0.4		
		I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V			0.55		
I _L		V _I = V _{CC} or GND		3.6 V			±5	μA	
		√ _I = 0.7 V		2.3 V	45				
		V _I = 1.7 V	*	2.5 V	-45				
l(hold)		V _I = 0.8 V	V _I = 0.8 V		75			μA	
		V _I = 2 V		3 V	-75			·	
		V _I = 0 to 3.6 V		3.6 V			±500		
loz		VO = VCC or GND		3.6 V			±10	μА	
ICC		V _I = V _{CC} or GND,	IO = 0	3.6 V			40	μA	
ΔlCC		One input at V _{CC} - 0.6 V,	Other inputs at VCC or GND	3 V to 3.6 V			750	μΑ	
	Control inputs	V V 010		3.3 V	4.5		nE		
Ci	Data inputs	AI = ACC OL GIAD	/I = V _{CC} or GND 3.3			6.5		рF	
Co	Outputs	VO = VCC or GND		3.3 V		7		pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		· ·	VCC =		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	150	0	150	0	150	MHz
tw Pulse duration		CLR low	3.3		3.3		3.3		
t _W Pulse duration	CLK high or low	CLK high or low	3.3		3.3		3.3		ns
	Setup time	CLR low	0.7		0.7		0.8		ns
•.		Data low	1.4		1.6		1.3		
tsu	Setup time	Data high	1.1		1.1		1		
		CLKEN low	1.8		1.9		1.5		
		Data low	0.4		0.5		0.5		
th	Hold time	Data high	0.7		0.1		0.8		ns
		CLKEN low	0.2		0.3		0.4		

[‡] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

SN74ALVCH16823 18-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS SCES038 - JULY 1995

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

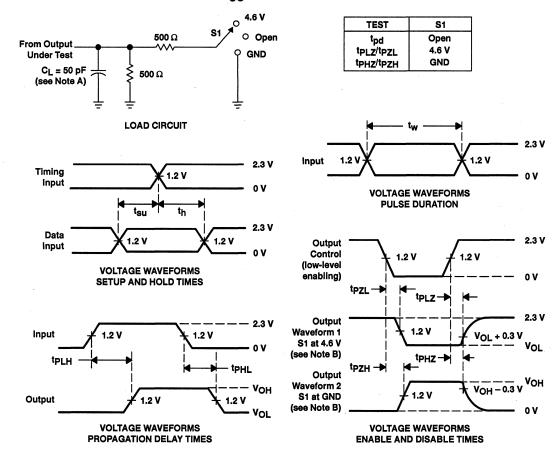
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		3.3 V 3 V	UNIT
	(INPOT)	(OUTPUT)		MAX	MIN	MAX	MIN	MAX	
f _{max}			150		150		150		MHz
	CLK	Q	1	6.4		5.2	1	4.5	
^t pd	CLR	Q	1.4	6		5.2	1.2	4.6	ns
^t en	ŌĒ	Q	1	6.5		5.7	1	4.8	ns
^t dis	ŌĒ	Q	1.8	5.6		4.7	1.3	4.5	ns

operating characteristics, T_A = 25°C

	PARAMETER		TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V TYP	V _{CC} = 3.3 V ± 0.3 V TYP	UNIT
	Davis dissination and sites	Outputs enabled	O: 50 -5 4 40 MH-	27	30	
C _{pd}	Opt Power dissipation capacitance Outputs disab		C _L = 50 pF, f = 10 MHz	16	18	pF

SCES038 - JULY 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

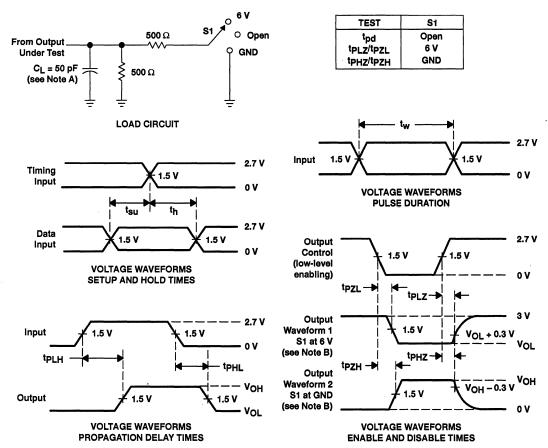


- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \Omega$, $t_{r} \leq 2.5 \text{ ns}$, $t_{f} \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SCES038 - JULY 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis-
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tod.

Figure 2. Load Circuit and Voltage Waveforms

SCES039 - JULY 1995

 Member of the Texas Instruments Widebus™ Family 	DGG OR DL PACKAGE (TOP VIEW)
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	1 OE1 1 56 1 OE2
 Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17 	1Y1
 ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 	1Y3 5 52 1A3 1Y4 6 51 1A4
200 V Using Machine Model (C = 200 pF, R = 0)	V _{CC} [7 50] V _{CC} 1Y5 [8 49] 1A5
 Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors 	1Y6 0 9 48 11A6 1Y7 0 10 47 11A7 GND 0 11 46 0 GND
Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink	1Y8 12 45 1A8 1Y9 13 44 1A9
Small-Outline (DGG) Packages	GND 1 14 43 GND GND 1 15 42 GND
description This 18-bit buffer and line driver is designed for	2Y1
2.3-V to 3.6-V V _{CC} operation.	GND [18 39
This SN74ALVCH16825 improves the perform- ance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers	2Y4 [] 20 37 [] 2A4 2Y5 [] 21 36 [] 2A5 V _{CC} [] 22 35 [] V _{CC}

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

2Y6 23

2Y7 **[**] 24

GND 1 25

2Y8 **[**] 26

2Y9 1 27

20E1 🛮 28

34**[**] 2A6 33 2A7

32 | GND

31 2A8

30 2A9

29 20E2

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN74ALVCH16825 is available in Tl's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16825 is characterized for operation from -40°C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

The device can be used as two 9-bit buffers or one

The 3-state control gate is a 2-input AND gate with

active-low inputs so that if either output-enable

(OE1 or OE2) input is high, all nine affected outputs are in the high-impedance state.

18-bit buffer. It provides true data.



and transmitters.

FUNCTION TABLE (each 9-bit section)

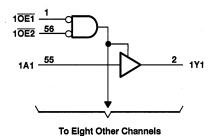
	INPUTS	OUTPUT	
OE1	OE2	Α	Y
L	L	L	L
L	L	Н	Н
Н	X	Х	z
Х	Н	Х	Z

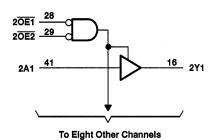
logic symbolt

10E1 EN1 56 10E2 28 20E1 & EN2 29 20E2 55 2 1A1 1Y1 1 🗸 3 54 1A2 1Y2 52 5 1A3 1Y3 6 51 1A4 **1Y4** 49 8 1A5 1Y5 48 9 1A6 1Y6 47 10 1A7 1Y7 45 12 1A8 1Y8 44 13 1A9 1Y9 41 16 2A1 2 🗸 2Y1 17 40 2A2 2Y2 38 19 2A3 2Y3 37 20 2Y4 2A4 36 21 2A5 2Y5 34 23 2A6 2Y6 33 24 2A7 2Y7 31 26 2A8 2Y8 30 2A9 2Y9

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





CES039 - JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{ K }(V_1 < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range, T _{stg}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		2.3	3.6	V
V	Lich level innut value	V _{CC} = 2.3 V to 2.7 V	1.7		V
ViH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V	Low level input veltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
VIL	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	V
۷Į	Input voltage		0	VCC	V
٧o	Output voltage		0	VCC	٧
		V _{CC} = 2.3 V		-12	
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 2.3 V		12	
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SCES039 - JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CO	ONDITIONS	vcct	MIN	TYP‡	MAX	UNIT	
		I _{OH} = -100 μA		MIN to MAX	V _{CC} -C).2			
		I _{OH} = -6 mA,	V _{IH} = 1.7 V	2.3 V	2				
\ _V			V _{IH} = 1.7 V	2.3 V	1.7			v	
Vон		I _{OH} = -12 mA	V _{IH} = 2 V	2.7 V	2.2] '	
			V _{IH} = 2 V	3 V	2.4				
		I _{OH} = -24 mA,	V _{IH} = 2 V	3 V	2				
		I _{OL} = 100 μA		MIN to MAX			0.2		
		I _{OL} = 6 mA,	V _{IL} = 0.7 V	2.3 V		,	0.4		
VOL		l 10 mA	V _{IL} = 0.7 V	2.3 V			0.7	V	
]		I _{OL} = 12 mA	V _{IL} = 0.8 V	2.7 V			0.4		
		I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V			0.55		
l _l		V _I = V _{CC} or GND		3.6 V			±5	μА	
		V _I = 0.7 V		2.3 V	45				
		V _I = 1.7 V		2.5 V	-45				
I _I (hold)		V _I = 0.8 V		3 V	75			μА .	
		V _I = 2 V]	-75				
		V _I = 0 to 3.6 V		3.6 V			±500		
loz		VO = VCC or GND		3.6 V			±10	μА	
Icc		V _I = V _{CC} or GND,	IO = 0	3.6 V			40	μА	
Δlcc		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА	
<u></u>	Control inputs	V _I = V _{CC} or GND		221		3.5		pF	
Ci	Data inputs			3.3 V		6			
Co	Outputs	VO = VCC or GND		3.3 V		7.5		pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	2.5 V 2 V	V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		ÚNIT
	(INPOT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	Α	Y	1	4.7		3.9	1	3.4	ns
ten	ŌĒ	Υ	1	6.5		5.7	1	4.7	ns
^t dis	ŌE	Υ	1.9	5.8		4.9	1.3	4.5	ns

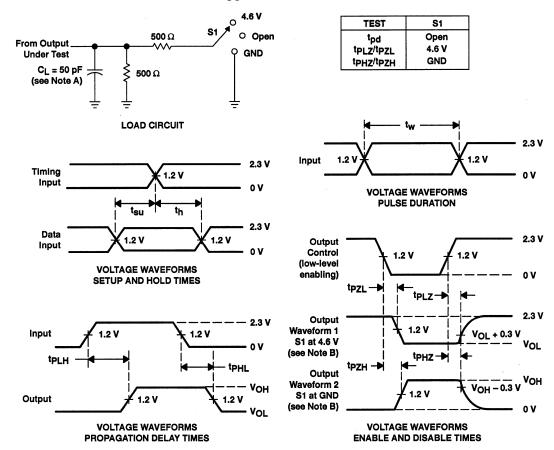
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT		
				TYP	TYP		
C	Power dissipation capacitance	Outputs enabled	Cı = 50 pF. f = 10 MHz	16	18	-F	
C _{pd}		Outputs disabled	C _L = 50 pF, f = 10 MHz	4	6	pF	

[‡] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

SCES039 - JULY 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

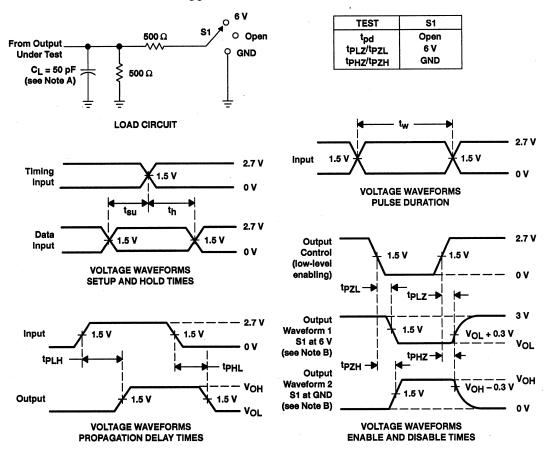


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_r \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpl 7 and tpH7 are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2.5$ ns. $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - tpl 7 and tpH7 are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tod.

Figure 2. Load Circuit and Voltage Waveforms

SCES041 - JULY 1995

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 20-bit non-inverting buffer/driver is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16827 is composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable (1OE1 and 1OE2 or 2OE1 and 2OE2) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

DGG OR DL PACKAGE (TOP VIEW)

10E1	1₁ ິ		10E2
1Y1 [2	55] 1A1
1Y2] 3	54] 1A2
GND		53	GND
1Y3 [5	52	1A3
	6] 1A4
]7	50	□ v _{cc}
1Y5	8	49	1A5
1Y6	9] 1A6
1Y7 [] 1A7
GND		46	GND
1Y8			1A8
1Y9 [13		1A9
1Y10	14	43	1A10
2Y1			2A1
2Y2 [16	41	2A2
2Y3 [2A3
GND	18	39	GND
2Y4		38] 2A4
2Y5		37	2A5
	21		2A6
	22	35] v _{cc}
2Y7		34	2A7
2Y8 [2A8
GND	25		GND
2Y9 [2A9
	27	30	2A10
20E1	28	29	2 0E 2

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16827 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16827 is characterized for operation from -40°C to 85°C.

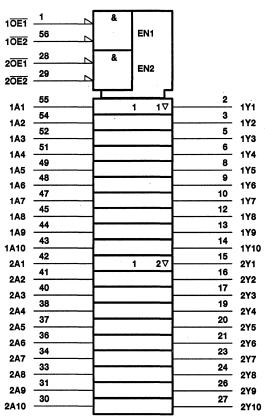
EPIC and Widebus are trademarks of Texas Instruments Incorporated.

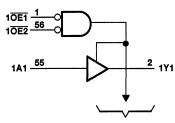
FUNCTION TABLE (each 10-bit section)

	INPUTS	OUTPUT	
OE1	OE2	Α	Y
L	L	L	L
L	L	Н	н
Н	X	X	Z
Х	Н	X	Z

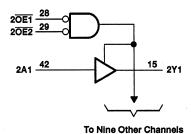
logic symbol†

logic diagram (positive logic)





To Nine Other Channels



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SCES041 - JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG p	ackage 1 W
DL pac	kage 1.4 W
Storage temperature range, T _{stq}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		2.3	3.6	V
V	High level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		v
VIH	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		ľ
V	Low level input veltage	V _{CC} = 2.3 V to 2.7 V		0.7	V
VIL	Low-level input voltage V _{CC} = 2.7 V to 3.6 V			8.0	V
VI	Input voltage		0	VCC	٧
Vo	Output voltage		0	VCC	٧
		V _{CC} = 2.3 V		-12	
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 2.3 V		12	
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V		24	
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN74ALVCH16827 20-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCES041 - JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CO	ONDITIONS	vcct	MIN	TYP‡	MAX	UNIT	
		I _{OH} = -100 μA		MIN to MAX	VCC-C	0.2			
Vou		$I_{OH} = -6 \text{ mA},$	V _{IH} = 1.7 V	2.3 V	2				
	•		V _{IH} = 1.7 V	2.3 V	1.7			v	
VOH		I _{OH} = -12 mA	V _{IH} = 2 V	2.7 V	2.2			V	
			V _{IH} = 2 V	3 V	2.4				
		I _{OH} = -24 mA,	V _{IH} = 2 V	3 V	2				
		I _{OL} = 100 μA		MIN to MAX			0.2		
		I _{OL} = 6 mA,	V _{IL} = 0.7 V	2.3 V			0.4		
VOL		I _{OL} = 12 mA	V _{IL} = 0.7 V	2.3 V			0.7	٧	
		IOL = 12 IIIA	V _{IL} = 0.8 V	2.7 V			0.4		
		I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V			0.55		
l _l		V _I = V _{CC} or GND		3.6 V			±5	μA	
		V _I = 0.7 V		2.3 V	45				
		V _I = 1.7 V		2.3 V	-45				
l _{l(hold)}		V _I = 0.8 V		0.1/	75			μА	
		V _I = 2 V		3 V	-75				
		V _I = 0 to 3.6 V		3.6 V			±500		
loz		VO = VCC or GND		3.6 V			±10	μΑ	
Icc		V _I = V _{CC} or GND,	IO = 0	3.6 V			40	μА	
ΔICC		One input at V _{CC} - 0.6 V,	Other inputs at VCC or GND	3 V to 3.6 V			750	μА	
C:	Control inputs	VI - Voc or GND		3.3 V		3.5		nE	
Ci	Data inputs	VI = VCC or GND		3.3 V		6		pF	
Co	Outputs	VO = VCC or GND		3.3 V		7.5		pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(IMFOT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	Α	Y	1	4.7		3.9	1	3.4	ns
^t en	ŌĒ	Y	1	6.5		5.7	1	4.7	ns
^t dis	ŌĒ	Y	1.9	5.8		4.9	1.3	4.5	ns

operating characteristics, T_A = 25°C

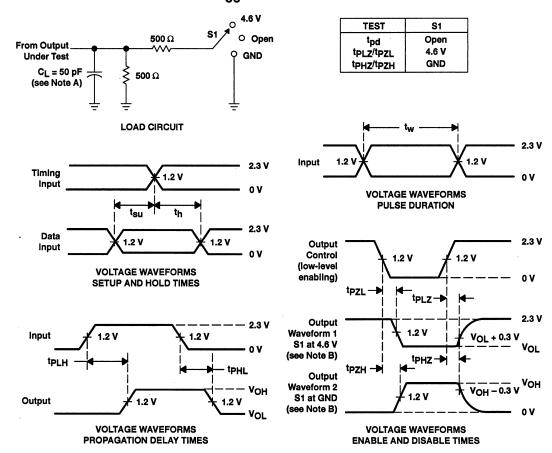
PARAMETER			TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
C	Power dissipation capacitance	Outputs enabled	Cı = 50 pF. f = 10 MHz	16	18	
C _{pd}	Fower dissipation capacitance	Outputs disabled	C _L = 50 pF, f = 10 MHz	4	6	pF



[‡] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

SCES041 - JULY 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

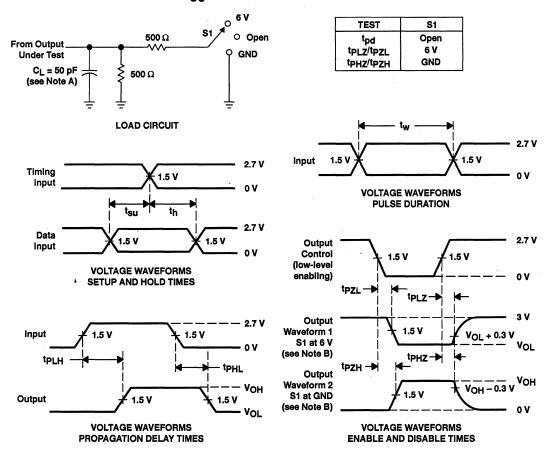


NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tplz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \Omega$, $t_{r} \leq 2.5 \text{ ns}$, $t_{f} \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

SCES013 - JULY 1995

•	Member of	the Texas	Instruments
	Widebus™	Family	

- EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 20-bit noninverting buffer/driver is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH162827 is composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable (10E1 and 10E2 or 20E1 and 20E2) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

DGG OR DL PACKAGE (TOP VIEW)

10E1			10E2
1Y1	2] 1A1
1Y2] 1A2
GND	4	53] GND
1Y3	5] 1A3
1Y4		51] 1A4
Vcc	7] v _{cc}
1Y5] 1A5
1Y6] 1A6
1Y7] 1A7
GND			GND
1Y8] 1A8
1Y9] 1A9
1Y10] 1A10
2Y1		42]2A1
2Y2			2A2
2Y3	17] 2A3
GND	18] GND
2Y4]2A4
2Y5			2A5
2Y6			2A6
VCC		35	V _{CC}
2Y7			2A7
2Y8			2A8
GND] GND
2Y9			2A9
2Y10			2A10
2 OE 1	28	29	20E2

The outputs, which are designed to sink up to 12 mA, include $26-\Omega$ resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162827 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH162827 is characterized for operation from -40°C to 85°C.

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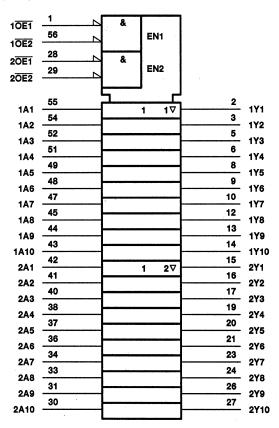
SN74ALVCH162827 **20-BIT BUFFER/DRIVER** WITH 3-STATE OUTPUTS SCES013 - JULY 1995

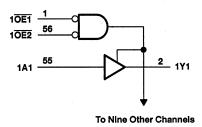
FUNCTION TABLE (each 10-bit section)

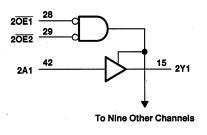
	INPUTS	V	OUTPUT
OE1	ŌE2	Α	Υ
L	L	L	L
L	L	Н	н
Н	X	X	z
Х	Н	Χ	z

logic symbolt

logic diagram (positive logic)







[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55$ °C (in still air): DGG package	1 W
DL package	
Storage temperature range, Teta	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
Vcc	Supply voltage		2.3	3.6	٧	
Viii	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
VIH	r light-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		•	
V _{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	>	
۷IL	V _{CC} = 2.7 V to 3.6 V			8.0	· ·	
۷j	Input voltage		0	Vcc	>	
۷o	Output voltage		0	VCC	>	
		V _{CC} = 2.3 V		-6		
ЮН	High-level output current	V _{CC} = 2.7 V		-8	-8 mA	
		V _{CC} = 3 V		-12		
		V _{CC} = 2.3 V		6		
lOL	Low-level output current V _{CC} = 2.7 V			8	mA	
		V _{CC} = 3 V		12		
Δt/Δν	Input transition rise or fall rate		0	10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN74ALVCH162827 20-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCES013 - JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST C	ONDITIONS	vcct	MIN	TYP‡	MAX	UNIT
		I _{OH} = -100 μA		MIN to MAX	Vcc-C).2		
	-	IOH = -4 mA,	V _{IH} = 1.7 V	2.3 V	1.9			
Van		IOH = -6 mA	V _{IH} = 1.7 V	2.3 V	1.7	* -		v
VOH		IOH = -6 IIIA	V _{IH} = 2 V	3 V	2.4			v
		$I_{OH} = -8 \text{ mA},$	V _{IH} = 2 V	2.7 V	2			
		I _{OH} = -12 mA,	V _{IH} = 2 V	3 V	2			
		I _{OL} = 100 μA		MIN to MAX			0.2	
		$I_{OL} = 4 \text{ mA},$	V _{IL} = 0.7 V	2.3 V			0.4	
Voi		.I _{OL} = 6 mA	V _{IL} = 0.7 V	2.3 V			0.55	v
VOL		·IOL = 0 IIIA	V _{IL} = 0.8 V	3 V			0.55	•
		$I_{OL} = 8 \text{ mA},$	V _{IL} = 0.8 V	2.7 V			0.6	
		I _{OL} = 12 mA,	V _{IL} = 0.8 V	3 V			0.8	
l _l		V _I = V _{CC} or GND		3.6 V			±5	μA
		V _I = 0.7 V		2.3 V	45			
		V _I = 1.7 V		2.5 V	-45			μА
l(hold)	V _I = 0.8 V		3 V	75			
		V _I = 2 V		1 ° ′	-75			
		V _I = 0 to 3.6 V		3.6 V			±500	
loz		VO = VCC or GND		3.6 V			±10	μА
Icc		VI = VCC or GND,	IO = 0	3.6 V			40	μА
Δlcc		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА
	Control inputs	V _I = V _{CC} or GND		3.3 V		3.5		pF
Ci	Data inputs	VI = VCC or GND		3.3 V		6		pF
Со	Outputs	V _I = V _{CC} or GND		3.3 V		7		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INFOT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	Α	Υ	1.3	5.2		4.6	1.5	4	ns
ten	ŌĒ	Υ	1.5	7		6.4	1.6	5.3	ns
^t dis	ŌĒ	Y	2.4	6.3		5.4	1.8	4.9	ns

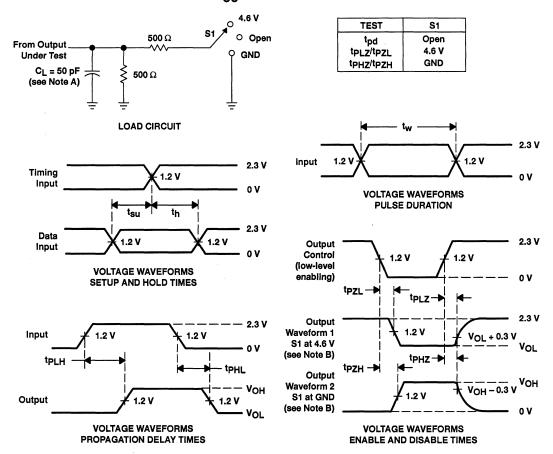
operating characteristics, T_A = 25°C

	PARAMETER	TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT	
			ITP	TYP		
C-4	C _{pd} Power dissispation capacitance	Outputs enabled	C _L = 50 pF, f = 10 MHz	16	18	pF
- pa		Outputs disabled	O[= 30 pr, 1 = 10 MΠ2	4	6	pr

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SCES013 - JULY 1995

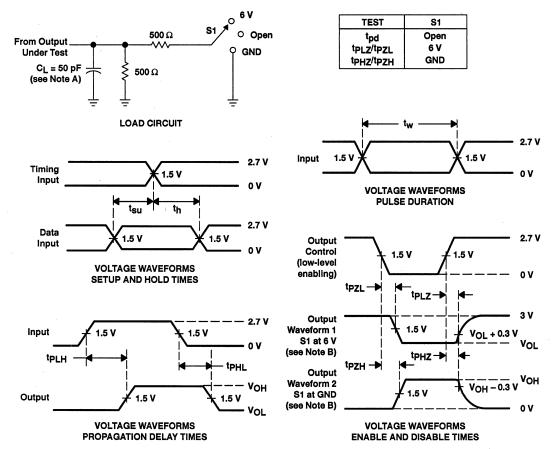
PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpZL and tpZH are the same as ten.
 - G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \Omega$, $t_{r} \leq 2.5$ ns. $t_{f} \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzi and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tod.

Figure 2. Load Circuit and Voltage Waveforms

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit universal bus driver is designed for 2.3-V to 3.6-V V_{CC} operation.

Data flow from A to Y is controlled by the output-enable $\overline{(OE)}$. The device operates in the transparent mode when LE is high. The A data is latched if CLK is held at a high or low logic level. If LE is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLK. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

DGG OR DL PACKAGE (TOP VIEW)

NC	[]1		GND
NC		55]NC
Y1	Дз] A1
GND	4]GND
Y2] A2
Y3] A3
V_{CC}	7] V _{CC}
Y4] A4
Y5	9	48	A5
	10	47] A6
GND] GND
	12		A 7
	13		8A [
	14] A9
Y10			A10
Y11] A11
Y12	17		A12
GND] GND
Y13] A13
Y14	20] A14
Y15] A15
V_{CC}			Vcc
Y16			A16
Y17	24] A17
GND	25		GND
Y18		31] A18
ŌĒ	27]CLK
LE	28	29	GND
			•

NC - No internal connection

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16835 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

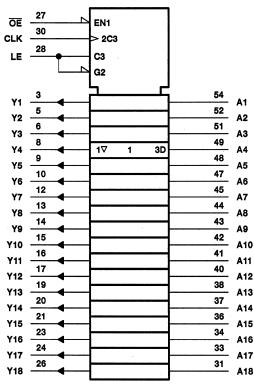
The SN74ALVCH16835 is characterized for operation from -40°C to 85°C.

NCT		

	INP		OUTPUT	
ŌĒ	LE	CLK	Α	Y
Н	Х	X	Х	Z
L	Н	Х	L	L
L	Н	X	Н	Н
, L	L	1	L	L
L	L	1	Н	Н
L	L	Н	Х	Y ₀ †
L	L	L	Х	Y ₀ ‡

[†] Output level before the indicated steady-state input conditions were established, provided that CLK is high before LE goes low

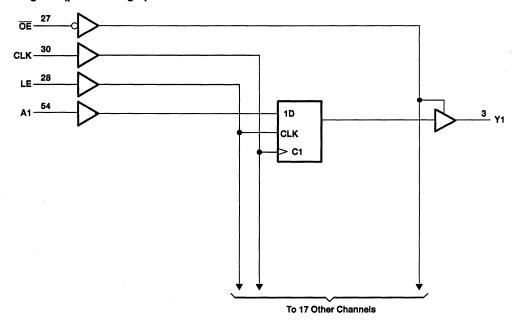
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

[‡] Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through each V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	
DL package	1.4 W
Storage temperature range, T _{stq}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

SCES053 - SEPTEMBER 1995

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage	2.3	3.6	٧	
V	V _{CC} = 2.3 V to 2.7 V		1.7		V
VIH	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		. •
V	Levy level input veltage	V _{CC} = 2.3 V to 2.7 V		0.7	v
VIL	Low-level input voltage V _{CC} = 2.7 V to 3.6 V			0.8	V .
٧Į	Input voltage		0	٧cc	V
٧o	Output voltage		0	Vcc	٧
		V _{CC} = 2.3 V		-12	
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 2.3 V	ł	12	
IOL	Low-level output current	V _{CC} = 2.7 V		12	mA
	V _{CC} = 3 V			24	İ
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	AMETER	TEST CONDITIONS		vcct	MIN	TYP‡	MAX	UNIT	
		I _{OH} = -100 μA		MIN to MAX	VCC-0	.2			
		i _{OH} = -6 mA,	V _{IH} = 1.7 V	2.3 V	2				
V			V _{IH} = 1.7 V	2.3 V	1.7			v	
Vон		I _{OH} = -12 mA	V _{IH} = 2 V	2.7 V	2.2			V	
			V _{IH} = 2 V	3 V	2.4	2.4			
		I _{OH} = -24 mA,	V _{IH} = 2 V	3 V	2				
		I _{OL} = 100 μA		MIN to MAX			0.2		
	V _{OL}	IOL = 6 mA,	V _{IL} = 0.7 V	2.3 V			0.4		
VOL		I _{OL} = 12 mA	V _{IL} = 0.7 V	2.3 V			0.7	٧	
	IOL = 12 IIIA	V _{IL} = 0.8 V	2.7 V			0.4			
		I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V			0.55		
- II		V _I = V _{CC} or GND		3.6 V			±5	μA	
		V _I = 0.7 V		2.3 V	45				
		V _I = 1.7 V		2.5 V	-45				
I(hold)		V _i = 0.8 V		3 V	75			μA.	
		V _I = 2 V]	-75				
		V _I = 0 to 3.6 V		3.6 V			±500		
loz		VO = VCC or GND		3.6 V			±10	μA	
Icc		$V_I = V_{CC}$ or GND,	l _O = 0	3.6 V			40	μА	
Δlcc		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА	
Ci	Control inputs	VI - Voc or GND		3.3 V		3.5			
	Data inputs	V _I = V _{CC} or GND		3.3 V		6		pF	
C _{io}	Outputs	VO = VCC or GND		3.3 V		7		pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.



SCES053 - SEPTEMBER 1995

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V _{CC} = 2.5 V ± 0.2 V		2.7 V	V _{CC} = 3.3 V ± 0.3 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX		
fclock	Clock frequency		0	150	0	150	0	150	MHz	
t _w	Pulse duration	LE high	3.3		3.3		3.3			
		CLK high or low	3.3		3.3		3.3		ns	
	Setup time	Data before CLK↑	2.2		2.1		1.7		ns	
t _{su}		Data before LE↓, CLK high	1.9		1.6		1.5			
		Data before LE↓, CLK low	1.3		1.1		1			
th		Data after CLK↑	0.6		0.6		0.7		ns	
	Hold time	Data after LE↓, CLK high or low	1.4		1.7		1.4			

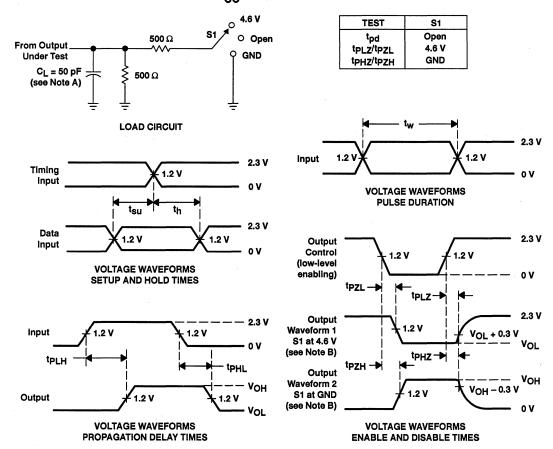
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM TO (OUTPUT)	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT	
		(001701)	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}	·		150		150		150		MHz
·	Α	Y	1.3	5.4		4.5	1	3.9	
t _{pd}	LE	Y	1.8	6.3		5.3	1.3	4.6	ns
,	CLK	Y	1.9	6.7		5.6	1.4	4.9	
^t en	ŌĒ	Y	1.5	6.8		6	1.1	5	ns
^t dis	ŌĒ	Y	2.1	5.5		4.6	1.3	4.2	ns

operating characteristics, T_A = 25°C

	PARAMETER	TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT	
			TYP	TYP	TYP	
C	C _{pd} Power dissipation capacitance	Outputs enabled		26	31	рF
Ора		Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	12	14	pr

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



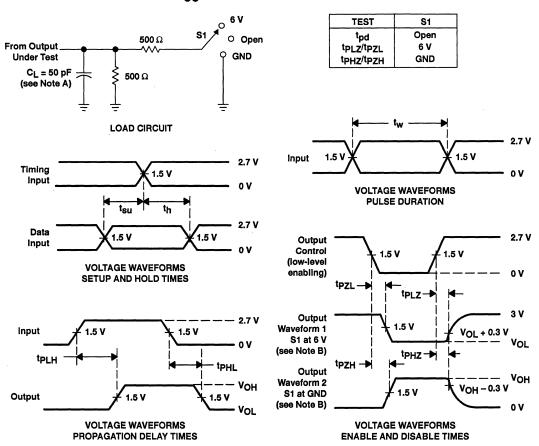
NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms

SCES053 - SEPTEMBER 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH andtpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

20-BIT BUS-INTERFACE D-TYPE LA WITH 3-STATE OUTPUTS

 Member of the Texas Instruments Widebus™ Family 	DGG OR DL PACKAGE (TOP VIEW)	
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	1 OE 1 56 1LE 1Q1 2 55 1D1	
 Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17 	1Q2 3 54 1 1D2 GND 4 53 1 GND	
 ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 	1Q3	
200 V Using Machine Model (C = 200 pF, R = 0)	V _{CC}	
 Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors 	1Q6 9 48 1 1D6 1Q7 1 10 47 1 1D7 GND 1 11 46 1 GND	
 Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink 	1Q8 0 12 45 0 1D8 1Q9 0 13 44 0 1D9	
Small-Outline (DGG) Packages description	1Q10 14 43 1D10 2Q1 15 42 2D1	
·	2Q2	
This 20-bit bus-interface D-type latch is designed for 2.3-V to 3.6-V V _{CC} operation.	GND 118 39 GND 2Q4 119 38 2D4	
The SN74ALVCH16841 features 3-state outputs designed specifically for driving highly capacitive	2Q5 20 37 2D5 2Q6 21 36 2D6	
or relatively low-impedance loads. This device is particularly suitable for implementing buffer	V _{CC} 22 35 V _{CC} 2Q7 23 34 2D7	
registers, unidirectional bus drivers, and working registers.	2Q8	
The SN74ALVCH16841 can be used as two 10-bit latches or one 20-bit latch, The 20 latches are transparent D-type latches. The device has	2Q9 26 31 2D9 2Q10 27 30 2D10 2OE 28 29 2LE	

data at its outputs. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the D inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (1OE or 2OE) input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

The output-enable (\overline{OE}) input does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN74ALVCH16841 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16841 is characterized for operation from -40°C to 85°C.

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noninverting data (D) inputs and provides true

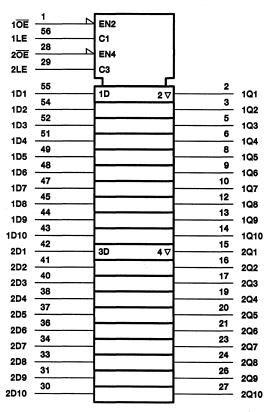


FUNCTION TABLE (each 10-bit latch)

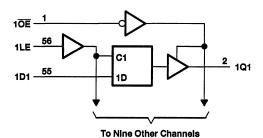
	INPUTS		OUTPUT
ŌĒ	LE	D	Q
L	Н	Н	Η.
L	Н	L	Ľ
L	L	X	Q ₀
Н	X	X	· Z

logic symbol†

SCES043 - JULY 1995



logic diagram (positive logic)



2DE 28

2LE 29

2D1 42

To Nine Other Channels

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74ALVCH16841 20-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I _{IK} (V ₁ < 0)	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	
Continuous current through each V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	
DL package	1.4 W
Storage temperature range, T _{sto}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The Input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	V
V	Link level innut valtage	V _{CC} = 2.3 V to 2.7 V	1.7		v
VIΗ	nigri-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		\ \ \
V	Supply voltage High-level input voltage Low-level input voltage Input voltage Output voltage High-level output current	V _{CC} = 2.3 V to 2.7 V		0.7	V
۷IL	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	, v
۷į	Input voltage		0	VCC	V
Vo	Output voltage		0	VCC	٧
		V _{CC} = 2.3 V		-12	
ЮН	High-level output current	$V_{CC} = 2.7 \text{ V}$		-12	mA
VIH VIL VI VO IOH LOL Δt/Δv		V _{CC} = 3 V		-24	
		V _{CC} = 2.3 V		12	
lOL	Low-level output current	$V_{CC} = 2.7 \text{ V}$		12	mA
			24		
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN74ALVCH16841 20-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SCES043 - JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CO	ONDITIONS	vcct	MIN	TYP‡	MAX	UNIT	
		I _{OH} = -100 μA		MIN to MAX	VCC-C).2			
		I _{OH} = -6 mA,	V _{IH} = 1.7 V	2.3 V	2				
			V _{IH} = 1.7 V	2.3 V	1.7			v	
VOH		I _{OH} = -12 mA	V _{IH} = 2 V	2.7 V	2.2			٧	
			V _{IH} = 2 V	3 V	2.4				
		I _{OH} = -24 mA,	V _{IH} = 2 V	3 V	2				
		I _{OL} = 100 μA		MIN to MAX			0.2		
		I _{OL} = 6 mA,	V _{IL} = 0.7 V	2.3 V			0.4		
VOL		la. 10 mA	V _{IL} = 0.7 V	2.3 V			0.7	V	
-		I _{OL} = 12 mA	V _{IL} = 0.8 V	2.7 V			0.4		
		I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V			0.55		
ΙĮ		VI = VCC or GND		3.6 V			±5	μА	
		V _I = 0.7 V		2.3 V	45				
		V _I = 1.7 V] 2.3 V	-45				
I _I (hold)		V _I = 0.8 V		0.1/	75			μА	
		V _I = 2 V		3 V	-75				
		V _I = 0 to 3.6 V		3.6 V			±500		
loz		VO = VCC or GND		3.6 V			±10	μА	
Icc		V _I = V _{CC} or GND,	I _O = 0	3.6 V			40	μА	
ΔlCC		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА	
	Control inputs	V VOND		201/		3			
Ci	Data inputs	VI = VCC or GND		3.3 V		6		pF	
Со	Outputs	VO = VCC or GND		3.3 V		7		pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature, (unless otherwise noted) (see Figures 1 and 2)

PARAMETER		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _W	Pulse duration, LE high or low	3.3		3.3		3.3		ns
t _{su}	Setup time, data before LE↑	0.9		0.7		1.1		ns
th	Hold time, data after LE↑	1.2		1.5		1.1		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =	3.3 V 3 V	UNIT
	(INTOT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	ŀ
• ,	. D	Q	1.1	5.6		4.7	1.2	3.9	
^t pd	LE .	Q	1	6.2		5.1	1	4.3	ns
t _{en}	ŌĒ	Q	1	6.7		6	1	4.9	ns
^t dis	ŌĒ	Q	1.8	5.5		4.3	1.3	4.1	ns



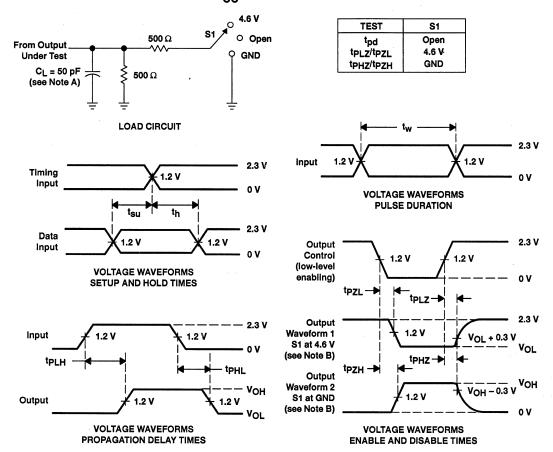
[‡] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

SN74ALVCH16841 20-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS SCES043 - JULY 1995

operating characteristics, $T_A = 25$ °C

PARAMETER			TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
	Power dissipation capacitance	Outputs enabled	C _L = 50 pF, f = 10 MHz	12	20	pF
C _{pd}	Power dissipation capacitance	Outputs disabled	C[= 50 pr, 1= 10 MHZ	1	3	pr

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V

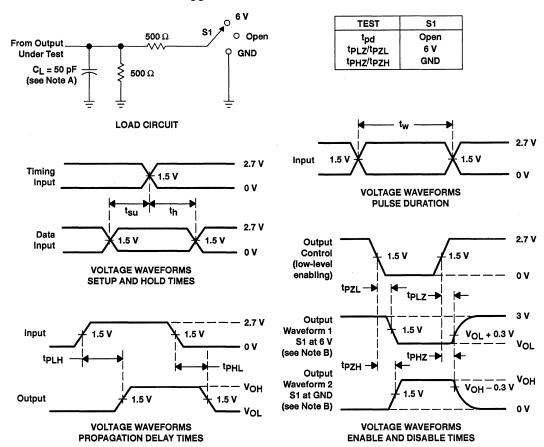


- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_f ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SCES043 - JULY 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \, \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns,
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tod.

Figure 2. Load Circuit and Voltage Waveforms

SN74ALVCH16843 18-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 18-bit bus-interface D-type latch is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16843 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, unidirectional bus drivers, and working registers.

The SN74ALVCH16843 can be used as two 9-bit latches or one 18-bit latch. The 18 latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

A buffered output-enable (\overline{OE}) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or a high-impedance state. The outputs also are in the high-impedance during power-up and power-down

conditions. The outputs remain in the high-impedance state while the device is powered down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN74ALVCH16843 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16843 is characterized for operation from -40°C to 85°C.

DGG OR DL PACKAGE (TOP VIEW)

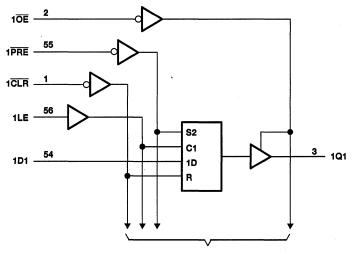
		_	
CLR [1	56] 1LE
10E [2	55	1PRE
1Q1 [3	54] 1D1
GND [4	53	GND
1Q2 [5		1D2
1Q3 [6	51] 1D3
v _{cc} [7	50] v _{cc}
1Q4 [8] 1D4
1Q5 [9] 1D5
1Q6 [10] 1D6
GND [46	GND
1Q7 [] 1D7
1Q8 [] 1D8
1Q9 [D9 1D9
2Q1 [15		2D1
2Q2 [16		2D2
2Q3 [40	2D3
GND [] GND
2Q4 [19		2D4
2Q5 [20	37	2D5
2Q6 [2D6
v _{cc} [22	35] v _{cc}
2Q7 [2D7
2Q8 [2D8
GND [25] GND
2Q9 [31	
20E [2PRE
CLR [28	29	2LE
			•

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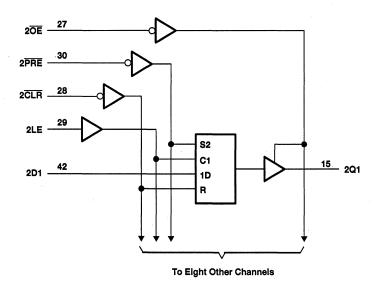


SN74ALVCH16843 18-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS SCES044 - JULY 1995

logic diagram (positive logic)



To Eight Other Channels



SN74ALVCH16843 18-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SCES044 - JULY 1995

FUNCTION TABLE (each 9-bit latch)

	INPUTS						
PRE	CLR	ŌĒ	LE	D	Q		
L	Х	L	Х	Х	н		
Н	L	L	X	Χ	L		
Н	н	L	н	L	L		
н	H	L	Н	Н	н		
н	н	L	L	Χ	Q ₀		
x	X	Н	X	X	Z		

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-05 V to 46 V
Input voltage range, V _I (see Note 1)	0.5 V to 4.6 V
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	
	1.4 W
Storage temperature range, Teta	65°C to 150°C

- † Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	٧
V	High-level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7		٧
VIH	nigri-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
V	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
VIL	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	٧
٧Į	Input voltage		0	VCC	٧
٧o	Output voltage		0	VCC	٧
		V _{CC} = 2.3 V		-12	
ЮН	High-level output current	V _{CC} = 2.7 V		-12	mA
		V _{CC} = 3 V		-24	
		V _{CC} = 2.3 V		12	
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA
			24		
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



SN74ALVCH16843 18-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS SCES044 – JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER	TEST CO	ONDITIONS	vcct	MIN	TYP‡	MAX	UNIT
		I _{OH} = -100 μA		MIN to MAX	VCC-C).2		
Voh	I _{OH} = -6 mA,	V _{IH} = 1.7 V	2.3 V	2				
		V _{IH} = 1.7 V	2.3 V	1.7			ν	
VOH		I _{OH} = -12 mA	V _{IH} = 2 V	2.7 V	2.2			V .
			V _{IH} = 2 V	3 V	2.4			·
	I _{OH} = -24 mA,	V _{IH} = 2 V	3 V	2				
		I _{OL} = 100 μA		MIN to MAX			0.2	
		I _{OL} = 6 mA,	V _{IL} = 0.7 V	2.3 V			0.4	
VOL		In. 10 mA	V _{IL} = 0.7 V	2.3 V			0.7	٧
, voc	I _{OL} = 12 mA	V _{IL} = 0.8 V	2.7 V			0.4		
		I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V			0.55	
l _l		V _I = V _{CC} or GND		3.6 V			±5	μА
		V _I = 0.7 V		2.3 V	45			
		V _I = 1.7 V		2.3 V	-45			
I(hold)		V _I = 0.8 V		3 V	75			μА
		V _I = 2 V] 3	-75			
		V _I = 0 to 3.6 V		3.6 V			±500	
loz		VO = VCC or GND		3.6 V			±10	μА
Icc		$V_I = V_{CC}$ or GND,	i _O = 0	3.6 V			40	μА
Δlcc		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μА
Control inputs		V. Von as CND		227				
Ci	Data inputs	VI = VCC or GND		3.3 V				pF
Co	Outputs	VO = VCC or GND		3.3 V				pF

TFor conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

SCES010 - JULY 1995

- Member of the Texas Instruments Widebus+™ Family
- EPIC™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- UBT™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Simultaneously Generates and Checks Parity
- Option to Select Generate Parity and Check or Feed-Through Data/Parity in A-to-B or **B-to-A Directions**
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Packaged in Thin Shrink Small-Outline (DGG) Package

description

This 18-bit (dual-octal) noninverting registered transceiver is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16901 is a dual 9-bit to dual 9-bit parity transceiver with registers. The device can operate as a feed-through transceiver or it can generate/check parity from the two 8-bit data buses in either direction.

DGG PACKAGE (TOP VIEW)

		$\overline{}$	
1CLKENAB	₁	64	1CLKENBA
LEAB [2] LEBA
CLKAB [3	62] CLKBA
1ERRA [4	61] 1ERRB
1APAR [5] 1BPAR
GND [59] GND
1A1 [58] 1B1
1A2 [8	57] 1B2
1A3 [] 1B3
v _{cc} [10	55] v _{cc}
1A4 [] 1B4
1A5 [12	53] 1B5
1A6 [13	52] 1B6
GND [] GND
1A7 [50] 1B7
1A8 [16	49] 1B8
2A1 [17] 2B1
2A2 [] 2B2
GND [] GND
2A3 [45] 2B3
2A4 [44	2B4
2A5 [1] 2B5
v _{cc} [42] v _{cc}
	24] 2B6
	25] 2B7
2A8 [] 2B8
GND [27	38] GND
	28] 2BPAR
2ERRA			2ERRB
OEAB [30		OEBA
SEL [31	34	ODD/EVEN
2CLKENAB	32	33	2CLKENBA

The SN74ALVCH16901 features independent clock (CLKAB or CLKBA), latch-enable (LEAB or LEBA), and dual 9-bit clock-enable (CLKENAB or CLKENBA) inputs. It also provides parity-enable (SEL) and parity-select (ODD/EVEN) inputs and separate error-signal (ERRA or ERRB) outputs for checking parity. The direction of data flow is controlled by OEAB and OEBA. When SEL is low, the parity functions are enabled. When SEL is high, the parity functions are disabled and the device acts as an 18-bit registered transceiver.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

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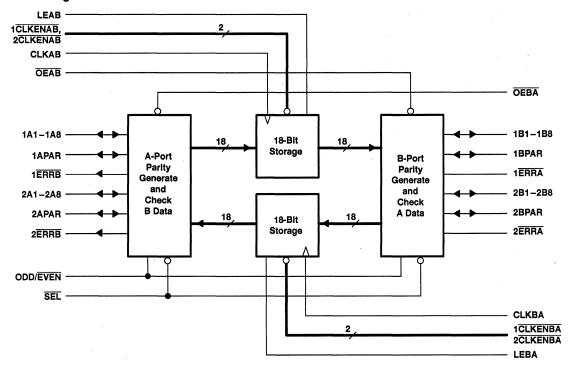
SCES010 - JULY 1995

description (continued)

The SN74ALVCH16901 is available in Tl's thin shrink small-outline (DGG) package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16901 is characterized for operation from -40°C to 85°C.

block diagram



FUNCTION TABLET

	INPUTS								
CLKENAB	OEAB	LEAB	CLKAB	Α	В				
X	Н	Х	Х	Х	Z				
х	L	Н	X	L	L				
х	L	Н	X	Н	Н				
н	L	L	X	Χ	в ₀ ‡				
L	L	L	1	L	L				
L	L	L	1	Н	Н				
L	L	L	L	Χ	В ₀ ‡				
L	L	L	Н	Χ	в ₀ §				

[†] A-to-B data flow is shown: B-to-A flow is similar, but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKENBA}}$.

[§] Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low



[‡] Output level before the indicated steady-state input conditions were established

PARITY-ENABLE FUNCTION TABLE

INPUTS			OPERATION OR FUNCTION						
SEL	OEBA	OEAB	OPERATION	OR FUNCTION					
L	Н	L	Parity is checked on port A a	Parity is checked on port A and is generated on port B.					
L	L	Н	Parity is checked on port B and is generated on port A.						
L	Н	Н	Parity is checked on port B and port A.						
L	L	L	Parity is generated on port A and B if device is in FF mode						
Н	L	L	Parity functions are	Q _A data to B, Q _B data to A					
Н	L	Н	disabled; device acts as a	QB data to A					
н	Н	L		Q _A data to B					
Н	Н	Н .	transceiver.	Isolation					

PARITY FUNCTION TABLE

	INPUTS							OUT	PUTS		
SEL	OEBA	OEAB	ODD/EVEN	Σ OF INPUTS A1-A8 = H	Σ OF INPUTS B1-B8 = H	APAR	BPAR	APAR	ERRA	BPAR	ERRB
L	Н	L	L	0, 2, 4, 6, 8	N/A	L	N/A	N/A	Н	L	Z
L.	Н	L	L	1, 3, 5, 7	N/A	L	N/A	N/A	L	Н	Z
L	Н	L	L	0, 2, 4, 6, 8	N/A	н	N/A	N/A	L	L	Z
L	Н	L	L	1, 3, 5, 7	N/A	Н	N/A	N/A	Н	Н	Z
L	L	Н	L	N/A	0, 2, 4, 6, 8	N/A	L	L	Z	N/A	Н
L	L	Н	L	N/A	1, 3, 5, 7	N/A	L	н	Z	N/A	L
L	L	Н	L	N/A	0, 2, 4, 6, 8	N/A	Н	L	Z	N/A	L
L	L	Н	L	N/A	1, 3, 5, 7	N/A	н	н	Z	N/A	Н
L	Н	L	Н	0, 2, 4, 6, 8	N/A	L	N/A	N/A	L	Н	Z
L	Н	L	Н	1, 3, 5, 7	N/A	Ľ	N/A	N/A	Н	L	Z
L	Н	L	Н	0, 2, 4, 6, 8	N/A	н	N/A	N/A	Н	Н	Z
L	Н	L	Н	1, 3, 5, 7	N/A	Н	N/A	N/A	L	L	Z
L	Ĺ	Н	Н	N/A	0, 2, 4, 6, 8	N/A	L	Н	Z	N/A	L
L	L	Н	Н	N/A	1, 3, 5, 7	N/A	L	L	Z	N/A	Н
L	L	Н	Ħ	N/A	0, 2, 4, 6, 8	N/A	н	Н	Z	N/A	Н
L	L	Н	Н	N/A	1, 3, 5, 7	N/A	Н	L	Z	N/A	L
L	Н	Н	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	L	L	Z	Н	Z	Н
L	Н	Н	L	1, 3, 5, 7	1, 3, 5, 7	L	L	z	L	Z	L
L	Н	Н	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	Н	Н	z	L	Z	L
L	н	Н	L	1, 3, 5, 7	1, 3, 5, 7	Н	Н	z	, H	Z	Н
L	Н	Н	Н	0, 2, 4, 6, 8	0, 2, 4, 6, 8	L	L	Z	L	Z	L
L	н	н	Н	1, 3, 5, 7	1, 3, 5, 7	L	L	z	н	z	Н
L	Н	Н	Н	0, 2, 4, 6, 8	0, 2, 4, 6, 8	н	н	z	Н	Z	Н
L	Н	Н	Н	1, 3, 5, 7	1, 3, 5, 7	Н	Н	z	L	Z	L
L	L	L	L	N/A	N/A	N/A	N/A	PE†	Z	PE†	Z
L	L	L	Н	N/A	N/A	N/A	N/A	PO‡	z	PO‡	Z

[†] Parity output is set to the level so that the specific bus side is set to even parity. ‡ Parity output is set to the level so that the specific bus side is set to odd parity.



SN74ALVCH16901 18-BIT UNIVERSAL BUS TRANSCEIVER WITH PARITY GENERATORS/CHECKERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)	0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, $I_{ K }(V_{ I } < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3)	1 W
Storage temperature range, T _{stq}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 4)

		. ,	MIN	MAX	UNIT
VCC	Supply voltage		2.3	3.6	٧
V	V _{CC} = 2.3 V to 2.7 V		1.7		V
VIH	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		٧.
	Low level input veltage	V _{CC} = 2.3 V to 2.7 V		0.7	V
VIL	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	V
VI	Input voltage		0	VCC	٧
VO	Output voltage		0	VCC	V
	•	V _{CC} = 2.3 V		-12	
Юн	High-level output current	V _{CC} = 2.7 V		-12	, mA
		V _{CC} = 3 V	1	-24	
		V _{CC} = 2.3 V		12	
lOL	Low-level output current	V _{CC} = 2.7 V		12	mA
		V _{CC} = 3 V	T	24	
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

^{3.} The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

SCES010 - JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARA	AMETER	TEST C	ONDITIONS	v _{cc} t	MIN	TYP‡	MAX	UNIT
		l _{OH} = -100 μA		MIN to MAX	VCC-0	.2		
		I _{OH} = −6 mA,	V _{IH} = 1.7 V	2.3 V	2			
VOH		V _{IH} = 1.7 V	2.3 V	1.7			V	
VOH		I _{OH} = -12 mA	V _{IH} = 2 V	2.7 V	2.2			V
I		V _{IH} = 2 V	3 V	2.4				
	I _{OH} = -24 mA,	V _{IH} = 2 V	3 V	2				
		I _{OL} = 100 μA		MIN to MAX			0.2	
		$I_{OL} = 6 \text{ mA},$	V _{IL} = 0.7 V	2.3 V			0.4	
VoL	In. 10 mA	V _{IL} = 0.7 V	2.3 V			0.7	V	
	I _{OL} = 12 mA	V _{IL} = 0.8 V	2.7 V			0.4		
		I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V			0.55	
11		V _I = V _{CC} or GND		3.6 V			±5	μА
		V _I = 0.7 V		2.3 V	45			
		V _I = 1.7 V		7 2.3 V	-45			μА
l(hold)		V _I = 0.8 V		3 V	75			
, ,		V _I = 2 V] 3	-75			1
		V _I = 0 to 3.6 V		3.6 V			±500	
I _{OZ} §		VO = VCC or GND		3.6 V			±10	μА
		V _I = V _{CC} or GND,	I _O = 0	3.6 V			40	μА
		One input at V _{CC} - 0.6 V,	Other inputs at VCC or GND	3 V to 3.6 V			750	μА
	Control inputs	VI = VCC or GND		3.3 V		.3		рF
	or B ports	VO = VCC or GND		3.3 V		7.5		рF
	RR ports	VO = VCC or GND		3.3 V		6		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

				V _{CC} = 2.5 V ± 0.2 V		2.7 V	V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
^f clock	Clock frequency		0	125	0	125	0	125	MHz
t _W Pulse duration	CLK↑	3		3		3			
	Pulse duration	LE high	3		3		3		ns
		APAR or BPAR before CLK↑	1.9		2		1.7		
t _{su}	Setup time	CLKEN before CLK↑	2.1		2.1		1.7		ns
		APAR or BPAR before LE↓	1.4		1.3		1.2		
		APAR or BPAR after CLK↑	0.4	!	0.4		0.5		
th	Hold time	CLKEN after CLK↑	0.5		0.5		0.7		ns
		APAR or BPAR after LE↓	0.9		1.1		0.9		

[‡] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

[§] For I/O ports, the parameter IOZ includes the input leakage current.

SN74ALVCH16901 18-BIT UNIVERSAL BUS TRANSCEIVER WITH PARITY GENERATORS/CHECKERS

SCES010 - JULY 1995

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

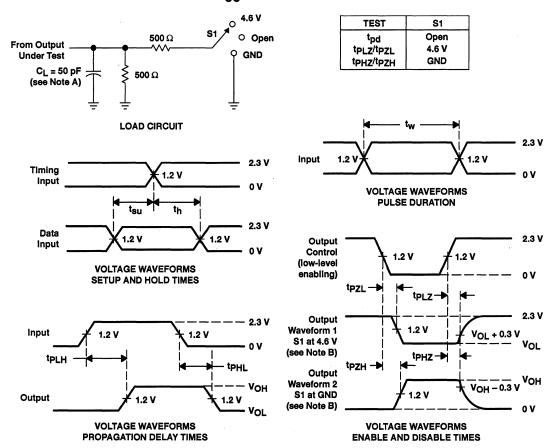
PARAMETER	FROM (INPUT)	TO (OUTPUT)		2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} =		UNIT
	(IMPOT)	(OUTPOT)	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}		4	125		125		125		MHz
	A or B	B or A	1.5	5.8		4.8	1	4.4	
	A or B	BPAR or APAR	2.5	9.5		7.6	2	6.7	
	APAR or BPAR	BPAR or APAR	1.5	6.3		5.2	1	4.7	
	APAR or BPAR	ERRA or ERRB	2.5	10.3		8.7	2	7.5	
	ODD/EVEN	ERRA or ERRB	2	9.3		7.9	1.5	6.8	
	ODD/EVEN	BPAR or APAR	2	8.9		7.6	1.5	6.5	
	SEL	BPAR or APAR	1.5	6.7		5.9	1	5.1	
	CLKAB or CLKBA	A or B	1.5	7		5.8	1	5.1	
t _{pd}	CLKAB or CLKBA	BPAR or APAR parity feedthrough	2	7.7		6.3	1.5	5.6	ns
	CLKAB or CLKBA	BPAR or APAR parity generated	3	10.8		8.7	2	7.7	
	CLKAB or CLKBA	ERRA or ERRB	3	11.1		8.9	2	7.9	
	LEAB or LEBA	A or B	1.5	6.6		5.5	1	4.8	
	LEAB or LEBA	BPAR or APAR parity feedthrough	2	7.3		6	1.5	5.3	
	LEAB or LEBA	BPAR or APAR parity generated	3	10.4		8.3	2	7.4	
	LEAB or LEBA	ERRA or ERRB	3	10.5		8.5	2	7.5	
t _{en}	OEAB or OEBA	B, BPAR or A, APAR	1.5	6.8		6.1	1	5.3	ns
t _{dis}	OEAB or OEBA	B, BPAR or A, APAR	2	6.3		5.2	1.5	4.9	ns
ten	OEAB or OEBA	ERRA or ERRB	1.5	6.7		5.5	1	4.9	ns
t _{dis}	OEAB or OEBA	ERRA or ERRB	2	7.5		6.5	1	5.7	ns
ten	SEL	ERRA or ERRB	1.5	7.2		6.5	1	5.5	ns
t _{dis}	SEL	ERRA or ERRB	2	6.6		5.4	1.5	4.9	ns

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	UNIT	
	Davis disclosition acceptance	Outputs enabled	0 50.5 / 40141	22	27	
C _{pd} Power dissipation capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	5	8	pF	

SCES010 - JULY 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



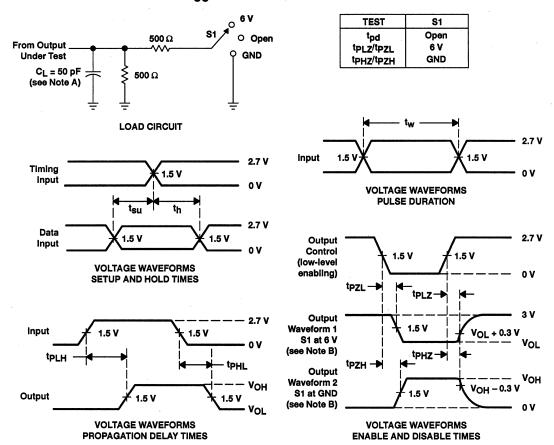
NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms

SCES010 - JULY 1995

PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7 V AND 3.3 V \pm 0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpl 7 and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

SN74ALVCH16952 **16-BIT REGISTERED TRANSCEIVER** WITH 3-STATE OUTPUTS

- **Member of the Texas Instruments** Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted) CMOS) Submicron Process
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit registered transceiver is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16952 contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. This device can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable (CEAB or CEBA) input is low. Taking the output-enable (OEAB or OEBA) input low accesses the data on either port.

To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16952 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16952 is characterized for operation from -40°C to 85°C.

DGG OR DL PACKAGE (TOP VIEW)

		_	
10EAB	₁ ∪		1 OEBA
1CLKAB	2 .	55	1CLKBA
1CEAB			1CEBA
GND [4] GND
1A1 [5] 1B1
1A2 [51] 1B2
v _{cc} [7	50] v _{cc}
1A3 L	8	49] 1B3
1A4 [] 1B4
1A5 🛚		47] 1B5
GND [46	GND
1A6 [12	45	1B6
1A7 [] 1B7
1A8 [14] 1B8
2A1 [2B1
2A2 [16	41	2B2
2A3 [17		2B3
GND [GND
2A4 [2B4
2A5 [2B5
2A6 [] 2B6
v _{cc} [22	35] v _{cc}
2A7 [34	2B7
2A8 [2B8
GND [GND
2CEAB	26		2CEBA
2CLKAB	27	30	2CLKBA
2 OEAB	28	29	2 0EBA

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SN74ALVCH16952 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS SCES011 - JULY 1995

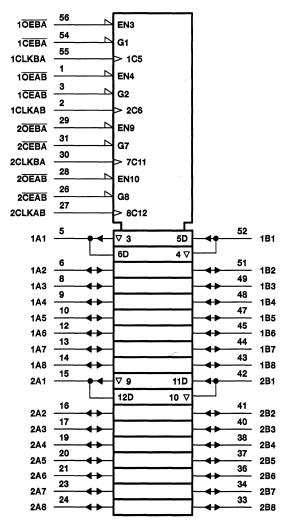
FUNCTION TABLET

	INPUTS				
CLKENAB	CLKAB	OEAB	Α	В	
Н	Х	L	Х	В ₀ ‡ В ₀ ‡	
х	L	L	X	В ₀ ‡	
L	1	L	L	L	
L	1	L	Н	н	
х	Х	Н	Х	Z	

[†] A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENBA, CLKBA, and OEBA.

[‡]Level of B before the indicated steady-state input conditions were established

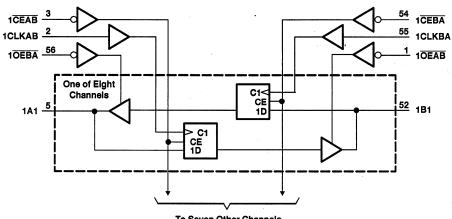
logic symbol†



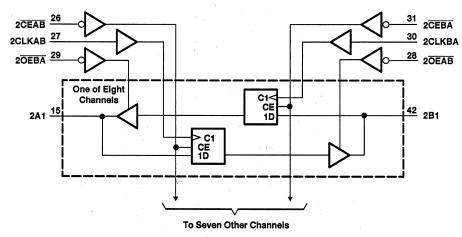
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74ALVCH16952 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS SCES011 - JULY 1995

logic diagram (positive logic)



To Seven Other Channels



SN74ALVCH16952 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCES011 - ILII V 1006

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)	0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through each V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): DGG package	
DL package	1.4 W
Storage temperature range, T _{stg}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.3	3.6	٧
V	V _{CC} = 2.3 V to 2.7 V		1.7		V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V			V
V	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	0.8
۷۱	Input voltage		0	VCC	٧
Vo	Output voltage		0	VCC	٧
		V _{CC} = 2.3 V		-12	2 mA
ЮН	High-level output current	V _{CC} = 2.7 V		-12	
		V _{CC} = 3 V		-24	
		V _{CC} = 2.3 V		12	
loL	Low-level output current	V _{CC} = 2.7 V		12	mA
	V _{CC} = 3 V			24	
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



SN74ALVCH16952 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCES011 - JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER	TEST CO	NDITIONS	vcct	MIN	TYP‡	MAX	UNIT	
		I _{OH} = -100 μA		MIN to MAX	V _{CC} -0	.2			
		$I_{OH} = -6 \text{ mA},$	V _{IH} = 1.7 V	2.3 V	2				
V			V _{IH} = 1.7 V	2.3 V	1.7			v	
VOH		I _{OH} = -12 mA	V _{IH} = 2 V	2.7 V	2.2			V	
			V _{IH} = 2 V	3 V	2.4				
		I _{OH} = -24 mA,	V _{IH} = 2 V	3 V	2				
		I _{OL} = 100 μA		MIN to MAX			0.2		
		I _{OL} = 6 mA,	V _{IL} = 0.7 V	2.3 V			0.4		
VOL		I 40 m A	V _{IL} = 0.7 V	2.3 V			0.7	v	
		I _{OL} = 12 mA	V _{IL} = 0.8 V	2.7 V			0.4		
		I _{OL} = 24 mA,	V _{IL} = 0.8 V	3 V			0.55		
lį		V _I = V _{CC} or GND		3.6 V			±5	μА	
		V _I = 0.7 V		001/	45				
		V _I = 1.7 V		2.3 V	-45				
I _{I(hold)}		V _I = 0.8 V		3 V	75			μА	
		V _I = 2 V		3 V	-75				
		V _I = 0 to 3.6 V		3.6 V		. 1	±500		
I _{OZ} §		VO = VCC or GND		3.6 V			±10	μА	
Icc		VI = VCC or GND,	IO = 0	3.6 V			40	μА	
ΔlCC		One input at V _{CC} - 0.6 V,	Other inputs at VCC or GND	3 V to 3.6 V			750	μА	
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V				pF	
Cio	A or B ports	VO = VCC or GND		3.3 V				pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

[§] For I/O ports, the parameter IOZ includes the input leakage current.

General Information	1
ALB Widebus™	2
ALVC Widebus™	3
LVT Octals	4
LVTZ Octals: Power Up and 3 State	5
LVT Widebus™	6
LVT JTAG/IEEE 1149.1	7
LVC MSI and Octals	8
LVC Widebus™	9
LV MSI and Octals	10
GTL Transceivers and Backplane Drivers	11
Application Reports	12
Characteristics Information	13
Mechanical Data	14

Contents

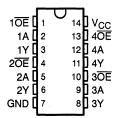
		Page
SN54/74LVT125	3.3-V ABT Quadruple Bus Buffers With 3-State Outputs	4-3
SN54/74LVT240	3.3-V ABT Octal Buffers/Drivers With 3-State Outputs	4-9
SN54/74LVT241	3.3-V ABT Octal Buffers/Drivers With 3-State Outputs	4-15
SN54LVT244	3.3-V ABT Octal Buffers/Drivers With 3-State Outputs	4-21
SN74LVT244A	3.3-V ABT Octal Buffers/Drivers With 3-State Outputs	4-21
SN54LVT245	3.3-V ABT Octal Bus Transceivers With 3-State Outputs	4-27
SN74LVT245A	3.3-V ABT Octal Bus Transceivers With 3-State Outputs	4-27
SN54/74LVT273	3.3-V ABT Octal D-Type Flip-Flops With Clear	4-33
SN54/74LVT543	3.3-V ABT Octal Registered Transceivers With 3-State Outputs	4-39
SN54/74LVT573	3.3-V ABT Octal Transparent D-Type Latches With 3-State Outputs	4-47
SN54/74LVT574	3.3-V ABT Octal Edge-Triggered D-Type Flip-Flops With 3-State Outputs	4-53
SN54/74LVT646	3.3-V ABT Octal Bus Transceivers and Registers With 3-State Outputs	4-59
SN54/74LVT652	3.3-V ABT Octal Bus Transceivers and Registers With 3-State Outputs	4-69
SN54/74LVT2952	3.3-V ABT Octal Bus Transceivers and Registers With 3-State Outputs	4-79

SN54LVT125, SN74LVT125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

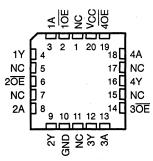
SCBS133D - MAY 1992 - REVISED JULY 1995

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) DIPs

SN54LVT125...J PACKAGE SN74LVT125...D, DB, OR PW PACKAGE (TOP VIEW)



SN54LVT125...FK PACKAGE (TOP VIEW)



NC - No internal connection

description

These bus buffers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT125 feature independent line drivers with 3-state outputs. Each output is in the high-impedance state when the associated output-enable (\overline{OE}) input is high.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT125 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

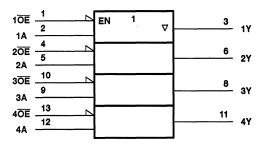
The SN54LVT125 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT125 is characterized for operation from -40°C to 85°C.

SCBS133D - MAY 1992 - REVISED JULY 1995

FUNCTION TABLE (each buffer)

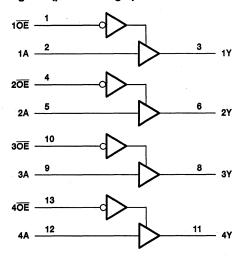
INPUTS		OUTPUT
ŌĒ	Α	Y
L	Н	Н
L	L	L
Н	X '	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, and PW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1) .	0.5 V to 7 V
Current into any output in the low state, Io: SN54LVT125	96 mA
SN74LVT125	128 mA
Current into any output in the high state, IO (see Note 2): SN54LVT125	48 mA
SN74LVT125	64 mA
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): D package	1.25 W
DB or PW package	0.5 W
Storage temperature range, T _{stq}	-65°C to 150°C

^{\$} Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

This current flows only when the output is in the high state and VO > VCC.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.



SCBS133D - MAY 1992 - REVISED JULY 1995

recommended operating conditions (see Note 4)

			SN54L	VT125	5 SN74LVT125		UNIT	
			MIN	MAX	MIN	MAX	UNII	
VCC	Supply voltage		2.7	3,6	2.7	3.6	٧	
V _{IH}	High-level input voltage		2	Æ,	2		٧	
VIL	Low-level input voltage			0.8		0.8	٧	
٧ _I	Input voltage			2 5.5		5.5	٧	
ЮН	High-level output current		1 3	-24		-32	mA	
lOL	Low-level output current		ŞĨ	48		64	mA	
Δt/Δν	Input transition rise or fall rate	Outputs enabled	8	10		10	ns/V	
TA	Operating free-air temperature	,	-55	125	-40	85	°C	

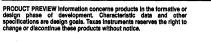
NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN	154LVT1:	25	SN	74LVT1	25	UNIT	
PARAMETER	 	ESI CONDITIONS		MIN	TYP	MAX	MIN	TYPT	MAX	UNIT	
V _{IK}	$V_{CC} = 2.7 \text{ V},$	i = -18 mA				-1.2			-1.2	٧	
	$V_{CC} = MIN \text{ to MAX}^{\ddagger},$	l _{OH} = -100 μA		VCC-C	.2		V _{CC} -0	.2			
V	$V_{CC} = 2.7 \text{ V},$	I _{OH} = -8 mA		2.4			2.4			v	
VOH	V _{CC} = 3 V	IOH = - 24 mA		2							
	ACC = 2 A	I _{OH} = -32 mA					2				
	V _{CC} = 2.7 V	l _{OL} = 100 μA				0.2			0.2		
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5		
Voi		I _{OL} = 16 mA			0.4			0.4	V		
V _{OL}	V _{CC} = 3 V	I _{OL} = 32 mA				0.5			0.5	. *	
	ACC = 2 A	I _{OL} = 48 mA		0.55							
		I _{OL} = 64 mA				42.			0.55		
	$V_{CC} = 0$ or MAX^{\ddagger} ,	′V _I = 5.5 V	Š	10			10				
lį.		V _I = V _{CC} or GND	Control inputs		1	±1			±1	μА	
"	V _{CC} = 3.6 V	V _I = V _{CC}	Data inputs		/\\\	1			1	μΛ.	
		V _I = 0	Data Inputs		Š	-5			-5		
loff	$V_{CC} = 0$,	V _I or V _O = 0 to 4.5	V	Š	3				±100	μА	
lia - i s	V _{CC} = 3 V	V _I = 0.8 V	Data inputs	7.5			75			μА	
l(hold)	VCC = 3 V	V ₁ = 2 V	Data inputs	-75			-75			μΛ	
^I OZH	$V_{CC} = 3.6 \text{ V},$	V _O = 3 V				5			5	μΑ	
^I OZL	$V_{CC} = 3.6 \text{ V},$	V _O = 0.5 V				-5			-5	μΑ	
			Outputs high		0.12	0.19		0.12	0.19		
lcc	$V_{CC} = 3.6 \text{ V},$	$I_{O}=0$,	Outputs low		4.5	. 7		4.5	7	mA	
.00	V _I = V _{CC} or GND		Outputs disabled		0.12	0.19		0.12	0.19	,,,,,	
ΔICC§	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} o	One input at V _{CC} – r GND	0.6 V,			0.3			0.2	mA	
Ci	V _I = 3 V or 0				4			. 4		pF	
Co	V _O = 3 V or 0			1	8			8		pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.



[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN54LVT125, SN74LVT125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

SCBS133D - MAY 1992 - REVISED JULY 1995

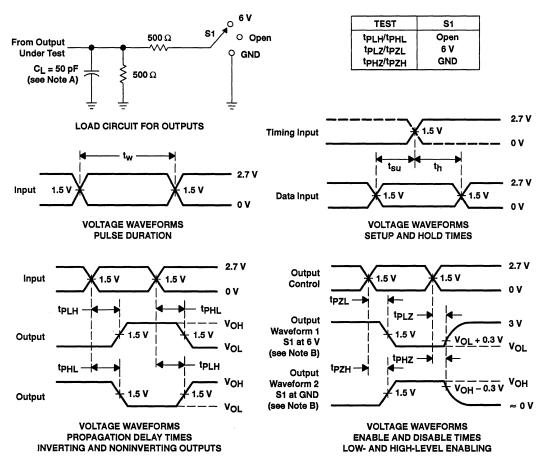
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

		SN54LVT125										
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =	2.7 V		± 0.3 V	V	V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
tPLH	Α	V	1	4.2	,37	4.7	1	2.7	4		4.5	no
tPHL	^	_ ·	1	4.1	Æ.	5.1	1	2.9	3.9		4.9	ns
tPZH	ŌĒ		1	4.9	Ž.	6.2	1	3.4	4.7		6	ns
t _{PZL}		Y	1.1	4,9	*	6.7	1.1	3.4	4.7		6.5	115
tPHZ	ŌĒ	v	1.8	,5 33		5.9	1.8	3.7	5.1		5.7	ns
tPLZ	OE .		1.3	Q4.7		4.2	1.3	2.6	4.5		4	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SCBS133D - MAY 1992 - REVISED JULY 1995

PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{\Omega} = 50 \Omega$, $t_r \leq 2.5$ ns, $t_r \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

8-1

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SCBS134F - SEPTEMBER 1992 - REVISED JULY 1995

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V) Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) DIPs

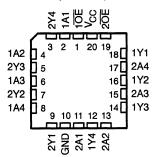
description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

SN54LVT240 . . . J PACKAGE SN74LVT240 . . . DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVT240 . . . FK PACKAGE (TOP VIEW)



These devices are organized as two 4-bit buffer/line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the devices pass data from the A inputs to the Y outputs. When OE is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{\sf OE}$ should be tied to $V_{\sf CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT240 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT240 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT240 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each buffer)

INP	JTS	OUTPUT
OE	Α	Y
L	Н	L
L	L	н
Н	Χ	z

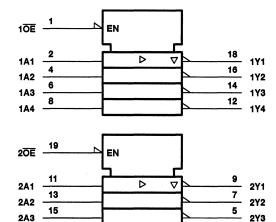
3

2Y4

logic symbol†

17

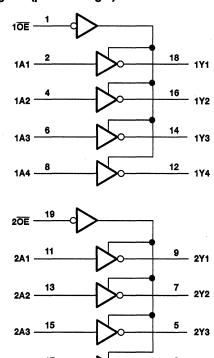
2A4



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

2A4 -



- 2Y4

SCBS134F - SEPTEMBER 1992 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	–0.5 V	to 4.6 V
Input voltage range, V _I (see Note 1)		
Voltage range applied to any output in the high state or power-off s		
Current into any output in the low state, Io: SN54LVT240		. 96 mA
SN74LVT240		128 mA
Current into any output in the high state, IO (see Note 2): SN54LVT	240	. 48 mA
SN74LVT	240	. 64 mA
Input clamp current, I _{IK} (V _I < 0)		-50 mA
Output clamp current, I_{OK} ($V_O < 0$)		
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): I	DB package	0.6 W
	DW package	1.6 W
· ·	PW package	0.7 W
Storage temperature range, T _{stg}		to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and VO > VCC.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			SN54L	VT240	SN74LVT240		UNUT
			MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage		2	Ü	2		V
VIL	Low-level input voltage			<i>⊘</i>)0.8		0.8	٧
VI	Input voltage			Q ^{4,5} 5.5		5.5	V
ЮН	High-level output current		S	-24		-32	mA
lOL	Low-level output current		Ş	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	J.S.	10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SCBS134F - SEPTEMBER 1992 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	_	FOT COMPLETIONS		IS I	154LVT2	40	SN	74LVT2	40	UNIT	
PARAMETER	11	EST CONDITIONS		MIN	TYPT	MAX	MIN	TYP	MAX	UNII	
VIK	V _{CC} = 2.7 V,	I _I = -18 mA			-	-1.2			-1.2	V	
	V _{CC} = MIN to MAX [‡] ,	IOH = -100 μA		V _{CC} -0).2		VCC-C).2			
Vari	$V_{CC} = 2.7 \text{ V},$	IOH = - 8 mA		2.4			2.4			v	
VOH	V _{CC} = 3 V	IOH = - 24 mA		2						٧	
	VCC = 2 V	I _{OH} = -32 mA	I _{OH} = -32 mA				2				
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2		
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5		
VOL		I _{OL} = 16 mA				0.4			0.4	v	
VOL	V _{CC} = 3 V	I _{OL} = 32 mA			0.5			0.5	. •		
	1000=30	IOL = 48 mA				0.55					
		I _{OL} = 64 mA				Ø.		-	0.55		
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V			4	ž 10			10		
1.	V _{CC} = 3.6 V	$V_I = V_{CC}$ or GND	Control inputs			±1			±1	μА	
lj		VI = VCC	Data inputs		.ζ.\.	1			1]	
		V _I = 0	Data inputs		8	-5			-5		
loff	$V_{CC} = 0$,	V_{I} or $V_{O} = 0$ to 4.5	/	Q	<u> </u>				±100	μА	
den en	V _{CC} = 3 V	V _I = 0.8 V	Data inputs	75			75			μА	
II(hold)	ACC = 2 A	V _I = 2 V	Data inputs	-75			-75			μА	
lozh	V _{CC} = 3.6 V,	V _O = 3 V				5			5	μА	
lozl	$V_{CC} = 3.6 \text{ V},$	V _O = 0.5 V				-5			-5	μА	
			Outputs high		0.12	0.19		0.12	0.19		
Icc	V _{CC} = 3.6 V,	$I_{O} = 0$,	Outputs low		8.6	12		8.6	12	mA	
100	V _I = V _{CC} or GND		Outputs disabled		0.12	0.19		0.12	0.19	, ,	
ΔlCC§	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} o	One input at V _{CC} – r GND	0.6 V,			0.2			0.2	mA	
Ci	V _I = 3 V or 0				4			4		pF	
Co	V _O = 3 V or 0				8			8		pF	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

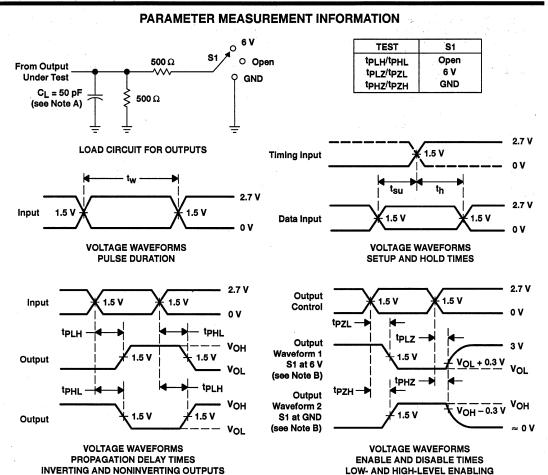
SCBS134F - SEPTEMBER 1992 - REVISED JULY 1995

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

		TO (OUTPUT)	SN54LVT240										
PARAMETER	FROM (INPUT)		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX		
t _{PLH}	^	A		1	4.2	.38	5.2	1	2.9	4.1		5.2	ns
^t PHL	^	ļ t	1.3	3.7	Ž.	4.1	1.3	2.5	3.5		4	115	
^t PZH	ŌĒ		1.2	4.7		5.7	1.2	3.2	4.6		5.6	ns	
^t PZL	OE	1	1.5	4,8		5.9	1.4	3.5	4.7		5.8	113	
t _{PHZ}	ŌĒ ·		2	(5 .3		5.7	2	3.6	5.2		5.5	20	
tPLZ				1.9	4.6		4.6	1.9	3.2	4.4		4.4	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SCBS134F - SEPTEMBER 1992 - REVISED JULY 1995



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCAS352C - MARCH 1994 - REVISED JULY 1995

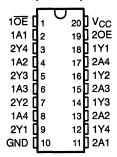
- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) DIPs

description

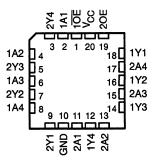
These octal buffers/drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT241 are organized as two 4-bit line drivers with separate output-enable ($1\overline{OE}$, 2OE) inputs. When $1\overline{OE}$ is low or 2OE is high, the devices pass data from the A inputs to the Y outputs. When $1\overline{OE}$ is high or 2OE is low, the outputs are in the high-impedance state.

SN54LVT241 ... J PACKAGE SN74LVT241 ... DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVT241 . . . FK PACKAGE (TOP VIEW)



Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The \$N74LVT241 is available in Tl's shrink small-outline package (DB), which provides the same input/output (I/O) pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT241 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT241 is characterized for operation from -40°C to 85°C.

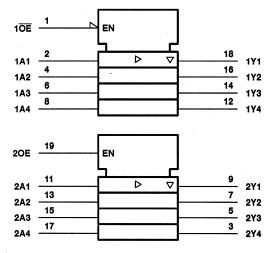
FUNCTION TABLES

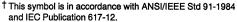
INP	JTS	OUTPUT
10E	1A	1Y
L	Н	Н
L	L	L
Н	Х	z

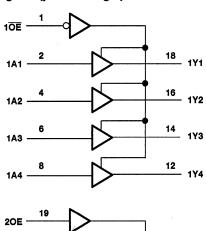
INP	JTS	OUTPUT
20E	2A	2Y
Н	Н	Н
Н	L	L
L	Х	Z

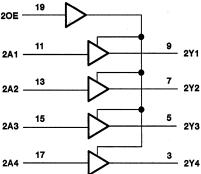
logic symbol†

logic diagram (positive logic)









SCAS352C - MARCH 1994 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, VO (see Note 1)	0.5 V to / V
Current into any output in the low state, Io: SN54LVT241	96 mA
SN74LVT241	
Current into any output in the high state, IO (see Note 2): SN54LVT241	48 mA
SN74LVT241	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB package	0.6 W
DW package	
PW package	_' 0.7 W
Operating free-air temperature range, T _A : SN54LVT241	
SN74LVT241	
Storage temperature range, Teta	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and VO > VCC.

3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			SN54L	VT241	SN74L	/T241	UNIT
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3,6	2.7	3.6	V
VIH	High-level input voltage		2	Ü	2		٧
VIL	Low-level input voltage			© 0.8		0.8	٧
VI	Input voltage			३ 5.5		5.5	٧
ЮН	High-level output current		S	-24		-32	mA
lOL	Low-level output current		Ş	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	S. C.	10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	င့

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SCAS352C - MARCH 1994 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	TEST CONDITIONS			SN	154LVT24	11	SN	74LVT24	11	
PARAMETER	'=	ST CONDITIONS		MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK	V _{CC} = 2.7 V,	l = −18 mA				-1.2			-1.2	٧
	V _{CC} = MIN to MAX [‡] ,	l _{OH} = -100 μA		V _{CC} -0	.2		V _{CC} -0	.2		
	V _{CC} = 2.7 V,	I _{OH} = -8 mA		2.4			2.4			v
VOH		IOH = -24 mA		2						V
	V _{CC} = 3 V	I _{OH} = -32 mA					2			
	V _{CC} = 2.7 V	I _{OL} = 100 μA		ł		0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
V		I _{OL} = 16 mA				0.4			0.4	v
VOL	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	I _{OL} = 32 mA			0.5			0.5	V	
	V _{CC} = 3 V	I _{OL} = 48 mA				0.55				
		I _{OL} = 64 mA			Ö	<i>i</i>			0.55	
	$V_{CC} = 0$ or MAX ‡ ,	V _I = 5.5 V			Ţ,Š	10			10	
	V _{CC} = 3.6 V	$V_I = V_{CC}$ or GND	Control inputs		~	±1			±1	μА
И.,		VI = VCC	Data inputs		~	1			1	μА
		$V_1 = 0$ Data	V _I = 0		8	-5			-5	
l _{off}	V _{CC} = 0,	V _I or V _O = 0 to 4.5	V	- 4					±100	μА
len en		V _I = 0.8 V	Data inputs	75			75			μА
[[] I(hold)	V _{CC} = 3 V	V _I = 2 V	Data inputs	-75			-75			μА
lozh	V _{CC} = 3.6 V,	V _O = 3 V				5			5	μΑ
IOZL	V _{CC} = 3.6 V,	V _O = 0.5 V				-5			-5	μА
			Outputs high		0.12	0.5		0.12	0.19	
loo	$V_{CC} = 3.6 \text{ V},$	$I_{O} = 0$,	Outputs low		8.6	15		8.6	15	mA
ICC .	V _I = V _{CC} or GND		Outputs disabled		0.12	0.5		0.12	0.19	IIIA
Δl _{CC} §	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} o	One input at V _{CC} – 0.6 V,				0.3			0.2	mA
Ci	V _I = 3 V or 0				4			4		рF
Co	V _O = 3 V or 0				8			8		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER		TO (OUTPUT)	SN54LVT241				SN74LVT241					
	FROM (INPUT)		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V		v vcc =		2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
tPLH .	Α	Υ	1	4.7	34	5.2	1	2.2	4.3		5	ns
^t PHL			1	4.4	24	5.4	1	2.3	4.2		5.2	
^t PZH	OE or OE	Υ	1.3	5.4	7,	6.5	1.4	2.8	5.2		6.3	
^t PZL		1	1.5	5.4		7.6	1.6	2.8	5.2		6.7	ns
^t PHZ	OE or OE		1.8	_003		8.3	1.9	3.2	6.6		7.7	no
^t PLZ			1.9	₡6.2		7.4	2	3.1	6		7.1	ns

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

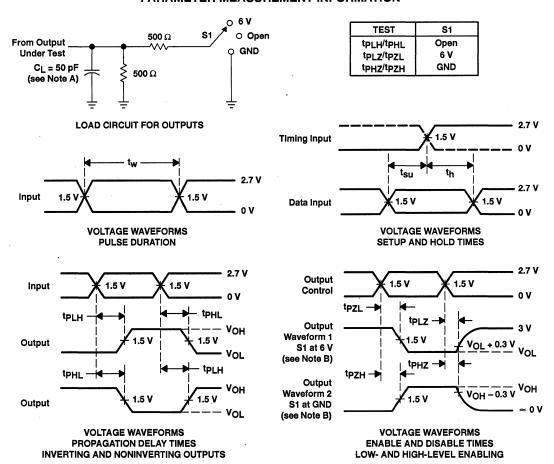


 $[\]uparrow$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. \uparrow For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

^{\$} This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SCAS352C - MARCH 1994 - REVISED JULY 1995

PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

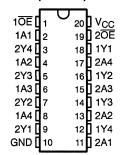
SCAS354B - FEBRUARY 1994 - REVISED JULY 1995

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Packages, and Ceramic (J) DIPs

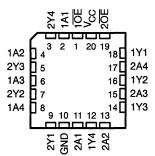
description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

SN54LVT244 . . . J OR W PACKAGE SN74LVT244A . . . DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVT244 . . . FK PACKAGE (TOP VIEW)



The SN54LVT244 and SN74LVT244A are organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

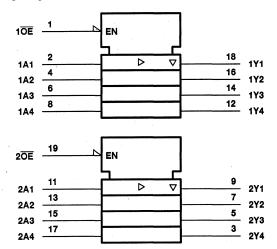
The SN74LVT244A is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT244 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT244A is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each buffer)

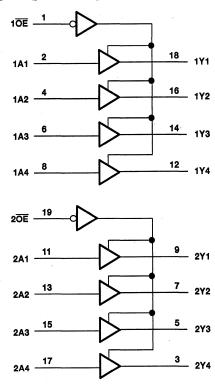
INP	JTS	OUTPUT
ŌĒ	Α	Y
L	Н	Н
L	L	L ·
Н	Х	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SCAS354B - FEBRUARY 1994 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high state or power-off state, Vo (see Note 1)0.5 V to 7 V
Current into any output in the low state, Io: SN54LVT244	
SN74LVT244A	
Current into any output in the high state, IO (see Note 2): SN54LVT244	48 mA
SN74LVT244A	64 mA
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB package	0.6 W
DW package	1.6 W
	0.7 W
Storage temperature range, T _{stg}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	2.7	3.6	2.7	3.6	٧	
VIH	High-level input voltage		2		2		٧
VIL	Low-level input voltage		0.8		0.8	٧	
VI	Input voltage			5.5		5.5	٧
ЮН	High-level output current			-24		-32	mA
lol	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	္င

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SCAS354B - FEBRUARY 1994 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

D4 D444ETED		SI	54LVT2	14	SN	74LVT24	4A	UNIT			
PARAMETER	1!	TEST CONDITIONS					MIN	TYPT	MAX	UNII	
VIK	V _{CC} = 2.7 V,	I _I = -18 mA			-1.2			-1.2	· V		
	V _{CC} = MIN to MAX [‡] ,	V _{CC} -0).2		VCC-C).2					
V	V _{CC} = 2.7 V,	2.4			2.4			٧			
VOH	V _{CC} = 3 V	I _{OH} = -8 mA								•	
	ACC = 2 A	IOH = -32 mA		1		2					
	V _{CC} = 2.7 V	I _{OL} = 100 μA			-	0.2			0.2		
	VCC = 2.7 V	I _{OL} = 24 mA			0.5			0.5			
Voi		IOL = 16 mA				0.4			0.4	V	
VOL	V _{CC} = 3 V	I _{OL} = 32 mA			0.5	0.5			,		
	ACC = 2 A	I _{OL} = 48 mA	0.55								
		I _{OL} = 64 mA				0.55					
	$V_{CC} = 0$ or MAX ‡ ,				50			10			
6	V _{CC} = 3.6 V	$V_I = V_{CC}$ or GND	Control inputs			±1			±1	μА	
lį		V _I = V _{CC}	Data inputs		1	1			1	,	
		V _I = 0	Data inputs		-5		-5				
l _{off}	$V_{CC} = 0$,	$V_{ }$ or $V_{ } = 0$ to 4.5	<i>'</i>						±100	μА	
lia in	V _{CC} = 3 V	V _I = 0.8 V	A inputs	75			75			μΑ	
l(hold)	ACC = 2 A	V _I = 2 V		-75			–75			μ^	
lozh	V _{CC} = 3.6 V,	VO = 3 V	•			5			5	μА	
lozl	V _{CC} = 3.6 V,	V _O = 0.5 V				-5			-5	μА	
			Outputs high		0.12	0.39		0.12	0.19		
lcc	V _{CC} = 3.6 V,	$I_{O} = 0$,	Outputs low		8.6	14		8.6	12	mA	
	V _I = V _{CC} or GND	Outputs disabled		0.12	0.39		0.12	0.19			
ΔICC§	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} o	One input at V _{CC} – r GND	0.6 V,			0.3			0.2	mA	
Ci	V _I = 3 V or 0				4			4		pF	
Co	V _O = 3 V or 0				8			8		pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER		SN54LVT244				SN74LVT244A							
	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		± 0.3 V			V _{CC} = 2.7 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX		
tPLH	A	_		0.5	4.7		5.2	1	2.5	4.1		-5	ns
t _{PHL}		'	0.5	4.4		5.4	1	2.5	4.1		5.2	115	
tPZH .	ŌĒ	v	0.8	5.4		6.5	1	2.7	5.2		6.3	ns	
tPZL		'	0.8	5.4		7.6	1.1	3.1	5.2		6.7	115	
t _{PHZ}	ŌĒ	V	1.5	6.2		6.9	1.9	3.9	5.6		6.3	ns	
t _{PLZ}		'	1.2	5.5		6	1.8	3.2	5.1		5.6	118	

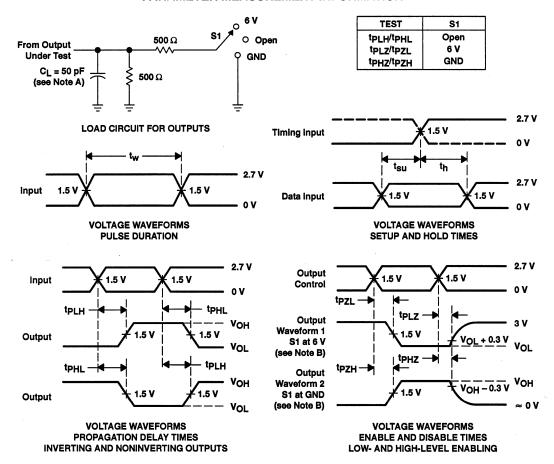


[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SCAS354B - FEBRUARY 1994 - REVISED JULY 1995

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \, \Omega$, $t_{r} \leq 2.5 \, \text{ns}$, $t_{f} \leq 2.5 \, \text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVT245, SN74LVT245A 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

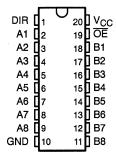
SCBS130G - MAY 1992 - REVISED JANUARY 1996

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V) Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OI P} (Output Ground Bounce) $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Packages, and Ceramic (J) DIPs

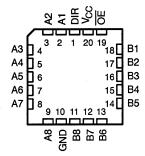
description

These octal bus transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

SN54LVT245...J OR W PACKAGE SN74LVT245A . . . DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVT245 . . . FK PACKAGE (TOP VIEW)



These devices are designed for asynchronous communication between data buses. They transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the devices so the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT245A is available in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

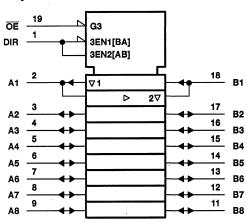
The SN54LVT245 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT245A is characterized for operation from -40°C to 85°C.

SCBS130G - MAY 1992 - REVISED JANUARY 1996

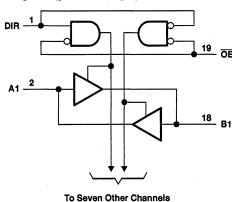
FUNCTION TABLE

INP	UTS	OPERATION				
ŌĒ	DIR	OPERATION				
L	L	B data to A bus				
L	Н	A data to B bus				
Н	Х	Isolation				

logic symbol†



logic diagram (positive logic)



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1)	0.5 V to 7 V
Current into any output in the low state, IO: SN54LVT245	96 mA
SN74LVT245A	128 mA
Current into any output in the high state, IO (see Note 2): SN54LVT245	48 mA
SN74LVT245A	64 mA
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0)	
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): DB package	0.6 W
DW package	1.6 W
PW package	
Storage temperature range, T _{stq}	

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and VO > VCC.



^{3.} The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

SN54LVT245, SN74LVT245A 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS130G - MAY 1992 - REVISED JANUARY 1996

recommended operating conditions (see Note 4)

	1		SN54L	VT245	SN74LV	UNIT	
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	V
VI	Input voltage			5.5		5.5	V
ЮН	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN54LVT245, SN74LVT245A 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS130G - MAY 1992 - REVISED JANUARY 1996

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		EST CONDITIONS		AS.	54LVT2	45	SN	74LVT24	5A	UNIT
PARAMETER		EST CONDITIONS		MIN	TYP	MAX	MIN	TYPT	MAX	ÜNII
ViK	V _{CC} = 2.7 V,	l _l = −18 mA	,			-1.2			-1.2	V
	V _{CC} = MIN to MAX [‡] ,	IOH = -100 μA	, , , , , , , , , , , , , , , , , , , ,	V _{CC} -0).2		Vcc-0	0.2		
Vari	V _{CC} = 2.7 V,	l _{OH} = – 8 mA		2.4	•		2.4			v
VOH	V _{CC} = 3 V	IOH = -24 mA		2						\ \ \
	ACC = 2 A	I _{OH} = -32 mA					2			
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
VOL		I _{OL} = 16 mA				0.4	5		0.4	V
VOL	V _{CC} = 3 V	I _{OL} = 32 mA				0.5			0.5	\ \ \
	VCC = 3 V	I _{OL} = 48 mA				0.55				
		I _{OL} = 64 mA							0.55	
	$V_{CC} = 3.6 \text{ V},$	V _I = V _{CC} or GND Control input				±1			±1	
	$V_{CC} = 0$ or MAX‡,	V _I = 5.5 V	Control inputs			10			10	
Iį		V _I = 5.5 V				100			20	μΑ
	V _{CC} = 3.6 V	V _I = V _{CC}	A or B ports§			5			5	
		V _I = 0		-10		-10		-10		
loff	$V_{CC} = 0$,	$V_1 \text{ or } V_0 = 0 \text{ to } 4.5 \text{ V}$	V						±100	μΑ
lia - i n	V _{CC} = 3 V	V _I = 0.8 V	A or B ports	75			75			μА
l(hold)	VCC = 3 V	V _I = 2 V	A or B ports -75				-75			μΛ
lozh	·V _{CC} = 3.6 V,	V _O = 3 V				1			1	μΑ
lozL	$V_{CC} = 3.6 \text{ V},$	V _O = 0.5 V				-1			-1	μΑ
			Outputs high		0.13	0.39		0.13	0.19	
lcc	V _{CC} = 3.6 V,	$I_{O} = 0$,	Outputs low		8.8	14		8.8	12	mA
	V _I = V _{CC} or GND		Outputs disabled		0.13	0.39		0.13	0.19	IIIA
ΔICC¶	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} o			0.3			0.2	mA		
Ci	V _I = 3 V or 0	/ = 3 V or 0						4		pF
Cio	V _O = 3 V or 0				10			10		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused terminals at V_{CC} or GND.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

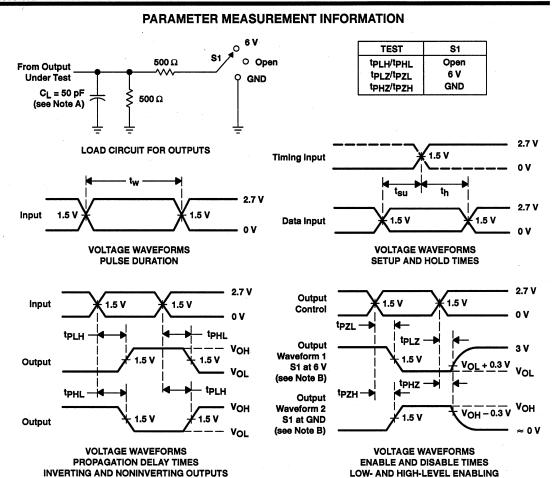
SN54LVT245, SN74LVT245A 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS130G - MAY 1992 - REVISED JANUARY 1996

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

			T	SN54L	VT245			SN	174LVT2	45										
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V				V _{CC} = 2.7 V		V _{CC} = 2.7 V		V _{CC} = 2.7 V V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX									
tPLH	A or B	B or A	0.5	4.4		5.2	1	2.5	4		5.2	ns								
t _{PHL}	AOIB	L BOYA	0.5	4.2		4.8	1	2.5	4		5.5	113								
^t PZH	ŌĒ	A or B	0.8	5.9		7.3	1.1	3.3	5.9		7.1									
t _{PZL}	OE		1	5.9		7.2	1.5	3.8	6.5		7.9	ns								
t _{PHZ}	ŌĒ .	A or B	1.5	6.5		7.2	2.2	4.3	5.9		6.5	no								
t _{PLZ}		AorB	1.5	6.1		6.5	2	3.9	5.5		5.6	ns								

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

SCBS130G - MAY 1992 - REVISED JANUARY 1996



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.

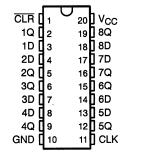
Figure 1. Load Circuit and Voltage Waveforms

SN54LVT273, SN74LVT273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

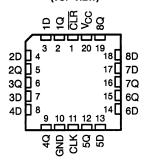
SCBS136E - MAY 1992 - REVISED JULY 1995

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V **Operation and Low-Static Power** Dissipation
- Support Mixed-Mode Signal Operation (5-V) Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Typical V_{OLP} (Output Ground Bounce) $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) DIPs

SN54LVT273...J PACKAGE SN74LVT273 . . . DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVT273 . . . FK PACKAGE (TOP VIEW)



description

These octal D-type flip-flops are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT273 are positive-edge-triggered flip-flops with a direct clear input. Information at the data (D) inputs meeting the setup-time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVT273 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

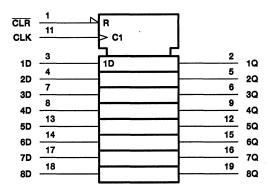
The SN54LVT273 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT273 is characterized for operation from -40°C to 85°C.

SCBS136E - MAY 1992 - REVISED JULY 1995

FUNCTION TABLE (each flip-flop)

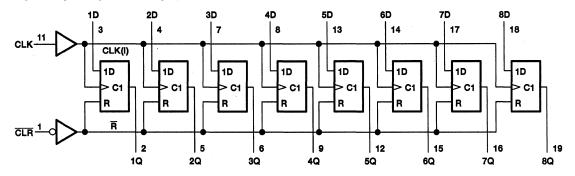
	INPUTS OUTPU						
CLR	CLK	D	Q				
L	Х	Х	L				
Н	1	Н	н				
Н	1	L	L				
Н	H or L	X	Q ₀				

logic symbolt



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVT273, SN74LVT273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

SCBS136E - MAY 1992 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo (see Note 1) .	
Current into any output in the low state, IO: SN54LVT273	., 96 mA
SN74LVT273	
Current into any output in the high state, IO (see Note 2): SN54LVT273	48 mA
SN74LVT273	64 mA
Input clamp current, $I_{IK}(V_1 < 0)$	
Output clamp current, I _{OK} (V _O < 0)	50 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3): DB package	
DW package	1.6 W
PW package	0.7 W
Storage temperature range, Teta	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

		SN54L	VT273	SN74L	UNIT	
		MIN	MAX	MIN	MAX	UNII
VCC	Supply voltage	2.7	3,6	2.7	3.6	٧
VIH	High-level input voltage	2	Ž,	2		V
VIL	Low-level input voltage		0.8		0.8	V
VI	Input voltage	1	% 5.5		5.5	٧
ЮН	High-level output current	(i)	-24		-32	mA
IOL	Low-level output current	,S	48		64	mA
Δt/Δν	Input transition rise or fall rate	S.	10		10	ns/V
TA	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SCBS136E - MAY 1992 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DA DAMETED	-	FOT CONDITIONS		SN	54LVT2	73	SN	174LVT2	73	UNIT
PARAMETER		EST CONDITIONS		MIN	TYPT	MAX	MIN	TYPT	MAX	UNII
VIK	V _{CC} = 2.7 V,	I _I = -18 mA				-1.2			-1.2	V
	V _{CC} = MIN to MAX [‡] ,	IOH = -100 μA		V _{CC} -C	.2		VCC-C).2		
Vari	$V_{CC} = 2.7 \text{ V},$	IOH = - 8 mA		2.4			2.4			V
VOH	V _{CC} = 3 V	IOH = - 24 mA		2						V
	ACC = 2 A	I _{OH} = -32 mA					2			
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA	`			0.5			0.5	
Voi		I _{OL} = 16 mA				0.4			0.4	٧
VOL	V _{CC} = 3 V	I _{OL} = 32 mA				∜ 0.5			0.5	
	VCC = 3 V	I _{OL} = 48 mA			84	0.55				
		I _{OL} = 64 mA			Α.				0.55	
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V			Š	10			10	
lj		$V_I = V_{CC}$ or GND	Control inputs		<u> </u>	±1			±1	μА
'4	V _{CC} = 3.6 V	V _I = V _{CC}	Data inputs	Q.		1			1	μΛ
		V _I = 0	Data Inputs			-5			-5	
1175-1-0	V _{CC} = 3 V	V _I = 0.8 V	Data inputs	75			75			μА
I(hold)	100-01	V _I = 2 V	Data Inputo	-75			-75			μ,
Icc	V _{CC} = 3.6 V,	$I_{O} = 0$,	Outputs high		0.12	0.19		0.12	0.19	mA
100	V _I = V _{CC} or GND		Outputs low		8.6	12	<u> </u>	8.6	12	11171
Δl _{CC} §	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} o	One input at V _{CC} – r GND	0.6 V,	Ì		0.2			0.2	mA
Ci	V _I = 3 V or 0						*	4		pF
Co	V _O = 3 V or 0							8		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54LVT273			SN74LVT273				
		. V _{CC} =		Vcc	= 2.7 V	V _{CC} =		V _{CC} :	= 2.7 V	UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency			,		0	150			MHz
t _W	Pulse duration			10.U		3.3		3.3		ns
	Setup time, data high or low before CLK↑		~ 0	116		2.3		2.7		
t _{su}	Setup time, CLR high before CLK↑		4%	Y		2.7		3.2		ns
th .	Hold time, data high or low after CLK↑					0		0		ns

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SN54LVT273, SN74LVT273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

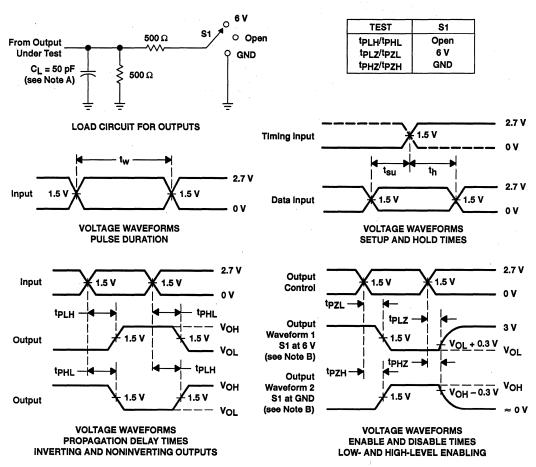
SCBS136E - MAY 1992 - REVISED JULY 1995

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

				SN54LVT273								
PARAMETER	FROM (INPUT)	TO (OUTPUT)		V _{CC} = 3.3 V ± 0.3 V V _{CC} = 2.7 V				٧	V _{CC} = 2.7 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
f _{max}					.A.		150					MHz
tPLH	CLK	Any Q		- N	% "		1.7	3.5	5.5		6.3	ns
tPHL	OLK	Arry C		₹ ⁰	7		1.9	3.5	5.5		5.9	115
t _{PHL}	CLR	Any Q		4.			1.3	3.2	5.1		6.2	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCBS137D - MAY 1992 - REVISED JULY 1995

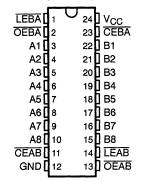
- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (JT) DIPs

description

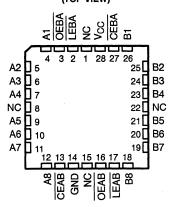
These octal transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT543 contain two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either direction of data flow.

SN54LVT543 . . . JT PACKAGE SN74LVT543 . . . DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVT543...FK PACKAGE (TOP VIEW)



NC - No internal connection

The A-to-B enable (CEAB) input must be low in order to enter data from A or to output data from B. If CEAB is low and LEAB is low, the A-to-B latches are transparent; a subsequent low-to-high transition of LEAB puts the A latches in the storage mode. With CEAB and OEAB both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the CEBA, LEBA, and OEBA inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

SN54LVT543, SN74LVT543 3.3-V ABT OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS137D - MAY 1992 - REVISED JULY 1995

description (continued)

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT543 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

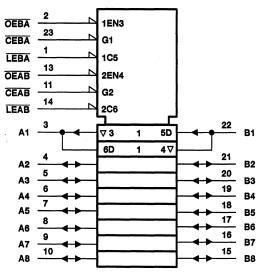
The SN54LVT543 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74LVT543 is characterized for operation from -40° C to 85°C.

FUNCTION TABLET

	INPUTS									
CEAB	LEAB	OEAB	Α	В						
Н	Х	Х	. X	Z						
Х	Х	Н	χ	z						
L	H ·	L	X	в ₀ ‡						
L	L	L	L	L						
L	L	L	Н	Н						

[†] A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

logic symbol§



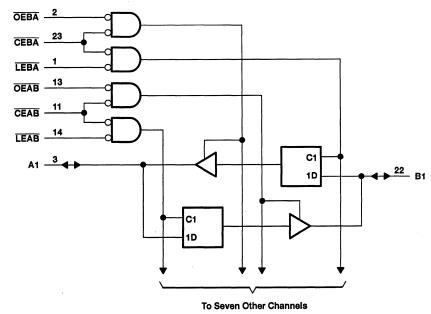
[§] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, and PW packages.



[‡] Output level before the indicated steady-state input conditions were established

SCBS137D - MAY 1992 - REVISED JULY 1995

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and PW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-0.5 V to 4.6 V -0.5 V to 7 V
Voltage range applied to any output in the high state or power-or	
Current into any output in the low state, Io: SN54LVT543	96 mA
SN74LVT543	128 mA
Current into any output in the high state, IO (see Note 2): SN54	LVT543 48 mA
SN74	ILVT543 64 mA
input clamp current, $I_{IK}(V_I < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0)	
Maximum power dissipation at T _A = 55°C (in still air) (see Note	
, , , , , , , , , , , , , , , , , , , ,	DW package 1.7 W
	PW package 0.7 W
Storage temperature range, T _{stq}	–65°C to 150°C
- ·	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.



SN54LVT543, SN74LVT543 3.3-V ABT OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS137D - MAY 1992 - REVISED JULY 1995

recommended operating conditions (see Note 4)

			SN54L	VT543	SN74L	VT543	UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2.7	3,6	2.7	3.6	٧
VIH	High-level input voltage		2	4	2		٧
VIL	Low-level input voltage			Ø.0.8		0.8	. V
٧ _I	Input voltage		٠. ﴿	5.5		5.5	٧
ЮН	High-level output current		<u> </u>	-24		-32	mA
lOL	Low-level output current		Ş	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	SE	10		10	ns/V
TA	Operating free-air temperature		~55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN54LVT543, SN74LVT543 3.3-V ABT OCTAL REGISTERED TRANSCEIVERS **WITH 3-STATE OUTPUTS**

SCBS137D - MAY 1992 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	-	EST CONDITIONS		SN	I54LVT5	43	SN	74LVT5	43	UNIT
PARAMETER	<u>'</u>	EST CONDITIONS		MIN	TYPT	MAX	MIN	TYP	MAX	UNII
VIK	$V_{CC} = 2.7 \text{ V},$	I _I = -18 mA				-1.2			-1.2	٧
	V_{CC} = MIN to MAX ‡ ,	I _{OH} = -100 μA		VCC-C).2		VCC-0	.2		
Vou	$V_{CC} = 2.7 \text{ V},$	I _{OH} = – 8 mA	I _{OH} = - 8 mA				2.4			v
VOH	V _{CC} = 3 V	I _{OH} = - 24 mA		2						, v
	VCC = 3 V	I _{OH} = -32 mA					2			
	V _{CC} = 2.7 V	i _{OL} = 100 μA				0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
Voi		I _{OL} = 16 mA				0.4			0.4	v
VOL	V _{CC} = 3 V	I _{OL} = 32 mA				0.5			0.5	'
	VCC = 3 V	IOL = 48 mA				0.55				
		IOL = 64 mA				liz.			0.55	
	$V_{CC} = 3.6 \text{ V},$	V _I = V _{CC} or GND	Control			∜ ±1			±1	
	$V_{CC} = 0$ or MAX ‡ ,	V _I = 5.5 V	inputs		S.	10			10	
lj.		V _I = 5.5 V			*** **********************************	20			20	μA
	V _{CC} = 3.6 V	V _I = V _{CC}	A or B ports§		Š	5			5	
		V _I = 0			ď	-10			-10	
l _{off}	$V_{CC} = 0$,	V_1 or $V_0 = 0$ to 4.5 V		Q.					±100	μА
lias - i-is	V _{CC} = 3 V	V _I = 0.8 V	A or B ports	75			75			μА
l(hold)		V _I = 2 V	A OF B ports	-75			-75			μΛ
lozh	$V_{CC} = 3.6 \text{ V},$	V _O = 3 V				1			.1	μА
lozl	V _{CC} = 3.6 V,	V _O = 0.5 V				-1			-1	μА
		,	Outputs high		0.13	0.19		0.13	0.19	
Icc	$V_{CC} = 3.6 \text{ V},$	$I_{O}=0$,	Outputs low		8.8	12		8.8	12	mA
	V _I = V _{CC} or GND		Outputs disabled		0.13	0.19		0.13	0.19	
∆ICC [¶]	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND					0.2			0.2	mA
Ci	V _I = 3 V or 0				4.5			4.5		pF
Cio	V _O = 3 V or 0				11			11		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused terminals at V_{CC} or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				T T	SN54L	VT543			SN74L	VT543		
				V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V			3.3 V 3 V	V _{CC} = 2.7 V		UNIT
				MIN	MAX	MĬN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration,	LEAB or LEBA low		3.3		<i>8</i> ,3		3.3		3.3		ns
		A or B before LEAB or	Data high	0		<i>₽</i> 0		0		0		
	Catum tima	LEBA↑	Data low	8.0		₹ 1.1		0.8		1.1		ns
tsu	Setup time	A or B before CEAB or	Data high	0	é	~ 0		0		0		115
	•	<u>CEBA</u> ↑	Data low	0.9	25	1.2		0.9		1.2		
	I I a lal kina a	A or B after LEAB or LE	BA↑	1.7	Ş	1.7		1.7		1.7		
th	Hold time	A or B after CEAB or CE	BA↑	1.8	4	1.8		1.8		1.8		ns

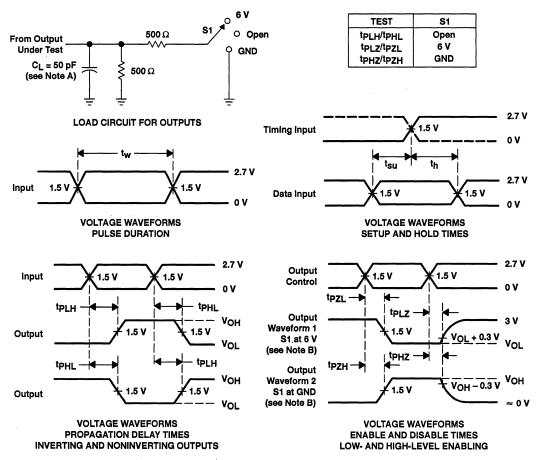
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

				SN54L	VT543			SN	74LVT5	43		
PARAMETER	FROM (INPUT)			V _{CC} = 3.3 V ± 0.3 V V _{CC} = 2.7 V		2.7 V		± 0.3 V	٧ .	V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
tPLH	A or B	B or A	1	4.9		5.7	1	2.9	4.7		5.5	ns
t _{PHL}	Z OI B	DOIA	1	4.8	4.	6	1	3.3	4.6		5.8	113
t _{PLH}	ΙĒ	A or B	1	6.1	Ţ,	7.5	1	4	5.9		7.3	ns
^t PHL	LE	AOIB	1	5.9	<i>[ii</i>]	7.5	1	4.1	5.7		7.3	115
tPZH	ŌĒ	A or B	1	6,	<u> </u>	7.8	1-	4.1	5.8		7.6	ns
tPZL	OE	AOIB	1.1	6.6	*	8.4	1.1	4.5	6.4		8.2	115
t _{PHZ}	ŌĒ	A or B	2.4	67		7.3	2.4	4.8	6.5		7.1	
tPLZ	OE	AOIB	2	<i>§</i> ₹ 6		6.1	2	4	5.8		5.9	ns
^t PZH	CE	A or B	1	6.2		7.8	1	4.2	6		7.6	
t _{PZL}	GE .	AUIB	1.4	6.9		8.5	1.4	4.7	6.7		8.3	ns
^t PHZ	CE	A or B	2.3	6.6		7.3	2.3	4.7	6.4		7.1	
^t PLZ	OE.	AUFB	2	5.6		5.8	2	3.8	5.4		5.6	ns

 $[\]dagger$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SCBS137D - MAY 1992 - REVISED JULY 1995

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \, \Omega$, $t_r \leq 2.5 \, \text{ns}$, $t_f \leq 2.5 \, \text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

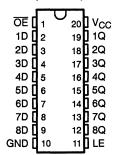
Figure 1. Load Circuit and Voltage Waveforms

SN54LVT573, SN74LVT573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

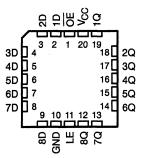
SCBS138D - MAY 1992 - REVISED JULY 1995

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Packages, and Ceramic (J) DIPs

SN54LVT573 . . . J OR W PACKAGE SN74LVT573 . . . DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVT573...FK PACKAGE (TOP VIEW)



description

These octal latches are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight latches of the 'LVT573 are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components. \overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT573 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

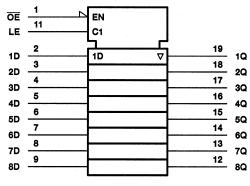
The SN54LVT573 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT573 is characterized for operation from -40°C to 85°C.

SCBS138D - MAY 1992 - REVISED JULY 1995

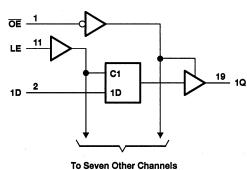
FUNCTION TABLE (each latch)

-	INPUTS	OUTPUT	
ŌĒ	LE	D	Q
L	Н	Н	Н -
L	н	L	L
L	L	Х	Q ₀
Н	X	Χ	z

logic symbol†



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo (see Note 1) .	0.5 V to 7 V
Current into any output in the low state, Io: SN54LVT573	96 mA
SN74LVT573	
Current into any output in the high state, IO (see Note 2): SN54LVT573	
SN74LVT573	
Input clamp current, $I_{ K }(V_{ } < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0)	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB package	0.6 W
DW package	
PW package	
Storage temperature range, T _{stg}	

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and $V_O > V_{CC}$.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

SN54LVT573, SN74LVT573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS SCBS138D - MAY 1992 - REVISED JULY 1995

recommended operating conditions (see Note 4)

			SN54L	VT573	SN74L	VT573	UNIT
			MIN	MAX	MIN	MAX	UNII
VCC	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage		2		2		٧
VIL	Low-level input voltage			0.8		0.8	٧
Vį	Input voltage			5.5		5.5	٧
ЮН	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN54LVT573, SN74LVT573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS138D - MAY 1992 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED		TEST CONDITIONS —			54LVT5	73	SN	74LVT5	73	UNIT
PARAMETER	<u>'</u>			MIN	TYP	MAX	MIN	TYPT	MAX	UNIT
VIK	V _{CC} = 2.7 V,	I _I = -18 mA			-1.2			-1.2	٧	
	V _{CC} = MIN to MAX‡,	I _{OH} = -100 μA	VCC-0	.2		VCC-0	.2			
M	V _{CC} = 2.7 V,	I _{OH} = – 8 mA	I _{OH} = -8 mA				2.4			v
VOH	V _{CC} = 3 V	IOH = - 24 mA		2						٧
	VCC = 2 V	I _{OH} = -32 mA					2			
	V _{CC} = 2.7 V	I _{OL} = 100 μA		·		0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
Va		I _{OL} = 16 mA				0.4			0.4	V
VOL	V _{CC} = 3 V	I _{OL} = 32 mA				0.5			0.5	V
	1000-30	I _{OL} = 48 mA				0.55				
		IOL = 64 mA					•		0.55	
	$V_{CC} = 0$ or MAX ‡ ,	V _I = 5.5 V				50			10	
		VI = VCC or GND	Control inputs			±1			±1	μА
	V _{CC} = 3.6 V	V _I = V _{CC}	Data innuts			1			1	
		V ₁ = 0	Data inputs			-5			-5	
loff	V _{CC} = 0,	V _I or V _O = 0 to 4.5 V							±100	μΑ
lea en	V _{CC} = 3 V	V _I = 0.8 V	Data inputs	75			75			μА
li(hold)	VCC = 3 V	V ₁ = 2 V	Data inputs	-75			-75			μζ
^l ozh	$V_{CC} = 3.6 \text{ V},$	V _O = 3 V				1			1	μΑ
^l OZL	$V_{CC} = 3.6 \text{ V},$	V _O = 0.5 V				-1			-1	μΑ
			Outputs high		0.13	0.39		0.13	0.19	
lcc	V _{CC} = 3.6 V,	$I_{O} = 0$,	Outputs low		8.6	14		8.6	12	mA
,00	V _I = V _{CC} or GND		Outputs disabled		0.13	0.39		0.13	0.19	IIIA
ΔI _{CC} §	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND					0.3			0.2	mA
Ci	V _I = 3 V or 0				4			4		pF
Co	V _O = 3 V or 0	V _O = 3 V or 0			8			8		pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN	54LVT573			SN74L	VT573		
		V _{CC} = 3.3 V	v _{cc}	= 2.7 V	V _{CC} =	3.3 V 3 V	V _{CC} =	2.7 V	UNIT
L		MIN MA	X MIN	MAX	MIN	MAX	MIN	MAX	1
t _W	Pulse duration, LE high	3.3	3.3		3.3		3.3		ns
t _{su}	Setup time, data before LE↓	1	0.9		0.7		0.6		ns
th	Hold time, data after LE↓	1.8	2		1.6		1.8		ns



[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SN54LVT573, SN74LVT573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

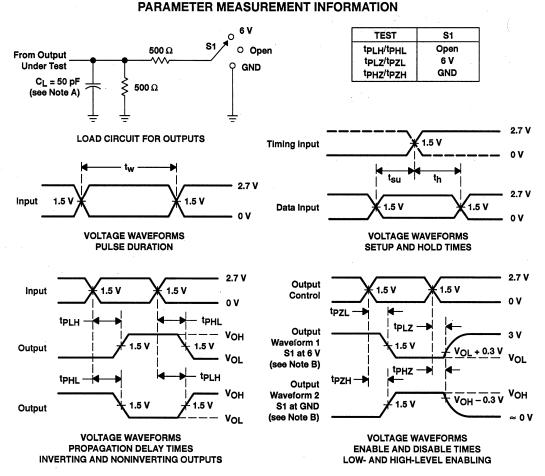
SCBS138D - MAY 1992 - REVISED JULY 1995

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

		,		SN54L	VT573			SN	74LVT5	73		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V				V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
^t PLH	D	Q	0.5	4.7		4.9	1	2.5	4.2		4.7	ns
t _{PHL}	U	ď	0.5	4.9		5.4	1	2.7	4.3		5.2	10
t _{PLH}	LE	Q	1	6		6.9	1.6	3.5	5.6		6.3	ns
t _{PHL}	LL	ď	1.4	6.9		7.6	2.5	4.3	6.5		7.2	120
t _{PZH}	ŌĒ	Q	0.5	5.3		6.4	1	2.8	5.1		6.2	ns
tPZL	OE	ď	0.7	5.7		7.2	1.3	3.3	5.5		6.6	10
tPHZ	ŌĒ	Q	1.2	5.9		6.9	2	3.7	5.7		6.7	200
tPLZ	06	ď	1	5.4		5.5	1.5	3	4.6		5.1	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SCBS138D - MAY 1992 - REVISED JULY 1995



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

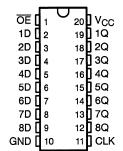
Figure 1. Load Circuit and Voltage Waveforms

SN54LVT574, SN74LVT574 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

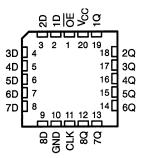
SCBS139D - MAY 1992 - REVISED JULY 1995

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Packages, and Ceramic (J) DIPs

SN54LVT574 . . . J OR W PACKAGE SN74LVT574 . . . DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVT574 . . . FK PACKAGE (TOP VIEW)



description

These octal flip-flops are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight flip-flops of the 'LVT574 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components. \overline{OE} does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT574 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

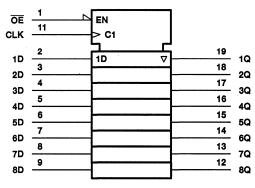
The SN54LVT574 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74LVT574 is characterized for operation from -40° C to 85°C.

SCBS139D - MAY 1992 - REVISED JULY 1995

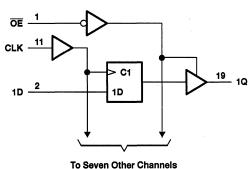
FUNCTION TABLE (each flip-flop)

	INPUTS	OUTPUT	
ŌĒ	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	H or L	Х	Q ₀
Н	Х	Х	z

logic symbolt



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo (see Note 1)	0.5 V to 7 V
Current into any output in the low state, IO: SN54LVT574	96 mA
SN74LVT574	128 mA
Current into any output in the high state, IO (see Note 2): SN54LVT574	48 mA
SN74LVT574	64 mA
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): DB package	0.6 W
DW package	
PW package	0.7 W
Storage temperature range, T _{stg}	

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current flows only when the output is in the high state and VO > VCC.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54LVT574, SN74LVT574 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS SCBS139D - MAY 1992 - REVISED JULY 1995

recommended operating conditions (see Note 4)

			SN54L	VT574	T574 SN74LVT574		UNIT
			MIN	MAX	MIN	MAX	UNII
VCC	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage		2		2		٧
VIL	Low-level input voltage			0.8		0.8	٧
VI	Input voltage			5.5		5.5	٧
ЮН	High-level output current			-24		-32	mA .
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN54LVT574, SN74LVT574 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS139D - MAY 1992 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		SN	I54LVT5	74	SN	174LVT5	74	UNIT			
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNI	
VIK	$V_{CC} = 2.7 \text{ V},$	l _l = –18 mA				-1.2			-1.2	>	
	V _{CC} = MIN to MAX‡,	l _{OH} = -100 μA		VCC-C).2		VCC-C).2			
Vou	V _{CC} = 2.7 V,	2.4			2.4			v			
VOH	V _{CC} = 3 V	IOH = - 24 mA		2						•	
	VCC=5 V	IOH = -32 mA					2		,		
	V _{CC} = 2.7 V					0.2			0.2		
	VGC = 2.7 V	I _{OL} = 24 mA				0.5			0.5		
VOL		I _{OL} = 16 mA				0.4			0.4	V	
VOL	V _{CC} = 3 V	I _{OL} = 32 mA				0.5			0.5	•	
	VCC = 3 V	I _{OL} = 48 mA				0.55					
		IOL = 64 mA						0.55			
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V				50			10		
lį	V _{CC} = 3.6 V	VI = VCC or GND	Control inputs			±1			±1	μА	
•		V _I = V _{CC}	Doto inputo			1			1		
		V ₁ = 0	Data inputs			-5			-5		
loff	V _{CC} = 0,	V _I or V _O = 0 to 4.5 V							±100	μА	
l	V 0V	V _I = 0.8 V	Data inputs	75			75				
li(hold)	V _{CC} = 3 V	V _I = 2 V	Data inputs	-75			-75			μА	
lozh	$V_{CC} = 3.6 \text{ V},$	V _O = 3 V				1			1	μА	
lozL	$V_{CC} = 3.6 \text{ V},$	V _O = 0.5 V				-1			-1	μA	
			Outputs high		0.13	0.39		0.13	0.19		
loo	$V_{CC} = 3.6 \text{ V},$	$I_{O} = 0$,	Outputs low	utputs low 8.7		14		8.7	12	mA	
lcc	V _I = V _{CC} or GND	Outputs disabled		0.13	0.39		0.13	0.19	mA		
ΔI _{CC} §	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND					0.3			0.2	mA	
Ci	V _I = 3 V or 0	1			4			4		pF	
Co	V _O = 3 V or 0				8			8		pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54L	VT574	574 SN74L			VT574			
		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	1	
fclock	Clock frequency	0	150	0	150	0	150	0	150	MHz	
tw	Pulse duration, CLK high or low	3.3		3.3		3.3		3.3		ns	
t _{su}	Setup time, data before CLK↑	2		2.4		2		2.4		ns	
th	Hold time, data after CLK↑	0.9		0.9		0.3		0		ns	



For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

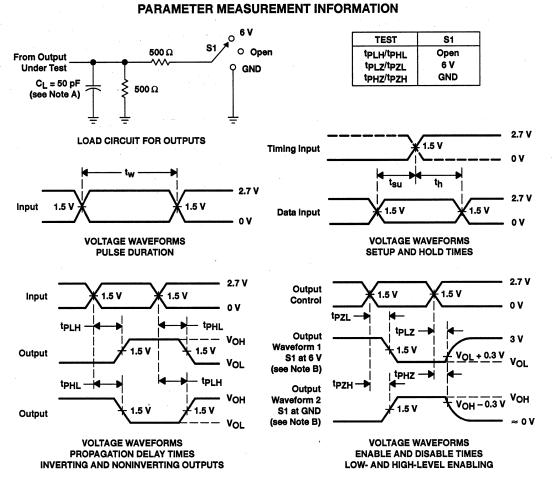
SN54LVT574, SN74LVT574 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS SCBS139D - MAY 1992 - REVISED JULY 1995

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

			SN54LVT574									
PARAMETER	FROM (INPUT)			100		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V	
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
fmax	į		150		150		150			150		MHz
tPLH	CLK	Q	1	5.9		6.6	1.7	3.6	5.4		6.2	ns
^t PHL	OLK	٩	1	6.1		6.8	2.4	4.3	5.9		6.6	115
^t PZH	ŌĒ	Q	0.5	5.9		7.1	1	2.9	4.8		5.9	
t _{PZL}) OE	~	0.5	5.3		6.4	1.3	3.4	5.1		6.2	ns
^t PHZ	ŌĒ	Q	0.7	5.9		6.6	1.9	4	5.5		5.9	
t _{PLZ}]	I	0.5	5.1		5.1	1.7	3.2	4.5		4.5	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SCBS139D - MAY 1992 - REVISED JULY 1995



NOTES: A. C₁ includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_t \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVT646, SN74LVT646 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS140D - MAY 1992 - REVISED JULY 1995

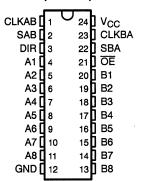
- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Packages, and Ceramic (JT) DIPs

description

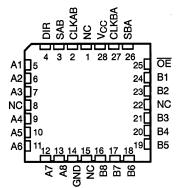
These bus transceivers and registers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT646 consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the

SN54LVT646 . . . JT OR W PACKAGE SN74LVT646 . . . DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVT646 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT646.

Output-enable (OE) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus receives data when \overline{OE} is low. In the isolation mode (\overline{OE} high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

SN54LVT646, SN74LVT646 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS140D - MAY 1992 - REVISED JULY 1995

description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT646 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT646 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT646 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

		INP	UTS			DATA	A I/Os	OPERATION OR FUNCTION
ŌĒ	DIR	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8	OPERATION OR FUNCTION
Х	Х	1	Х	Х	Х	Input	Unspecified [†]	Store A, B unspecified†
Χ	Х	Х	1	X	Х	Unspecified [†]	Input	Store B, A unspecified†
Н	Х	1	1	Х	Х	Input	Input	Store A and B data
Н	X	H or L	H or L	Х	Х	Input disabled	Input disabled	Isolation, hold storage
L	L	Х	X	Х	L	Output	Input	Real-time B data to A bus
L	· L	X	H or L	Х	Н	Output	Input	Stored B data to A bus
L	Н	Х	X	L	Х	Input	Output	Real-time A data to B bus
L	Н	H or L	X	Н	X	Input	Output	Stored A data to B bus

[†] The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition of the clock inputs.



SCBS140D - MAY 1992 - REVISED JULY 1995

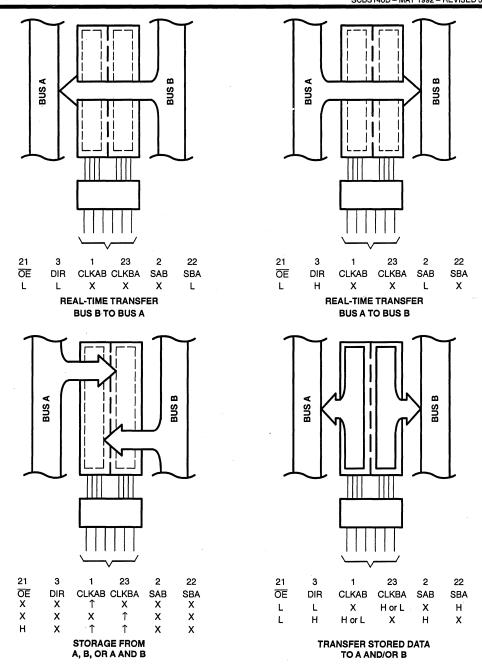


Figure 1. Bus-Management Functions

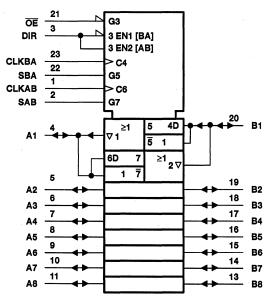
Pin numbers shown are for the DB, DW, JT, PW, and W packages.



SN54LVT646, SN74LVT646 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

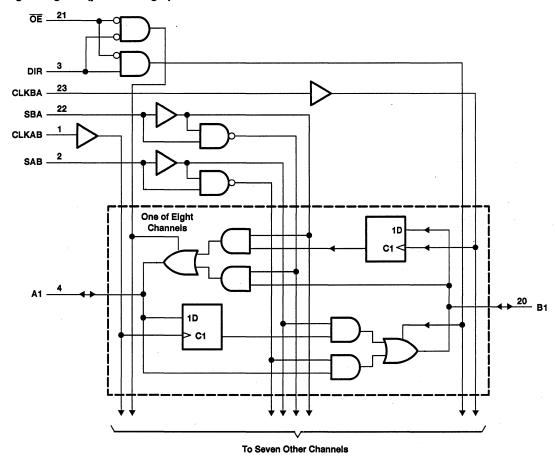
SCBS140D - MAY 1992 - REVISED JULY 1995

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, PW, and W packages.

SCBS140D - MAY 1992 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, VO (see Note 1)	0.5 V to 7 V
Current into any output in the low state, IO: SN54LVT646	96 mA
SN74LVT646	128 mA
Current into any output in the high state, IO (see Note 2): SN54LVT646	48 mA
SN74LVT646	64 mA
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB package	0.65 W
DW package	1.7 W
PW package	0.7 W
Storage temperature range, T _{stg}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and $V_O > V_{CC}$.

 The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			SN54L	VT646	SN74L	VT646	UNIT
1	•		MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage	1.	2		2		٧
VIL	Low-level input voltage			0.8		0.8	٧
VI	Input voltage			5.5		5.5	٧
ЮН	High-level output current			-24		-32	mA
lol	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN54LVT646, SN74LVT646 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS SCBS140D - MAY 1992 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	-	TET COMPITIONS		SN	54LVT64	16	SN	74LVT64	16	UNIT
PARAMETER	11	EST CONDITIONS		MIN	TYP	MAX	MIN	TYPT	MAX	UNII
V _{IK}	$V_{CC} = 2.7 \text{ V},$	l _l = −18 mA				-1.2			-1.2	>
	V _{CC} = MIN to MAX‡,	lOH = -100 μA		VCC-C	.2		VCC-0	.2		
Vou	$V_{CC} = 2.7 \text{ V},$	I _{OH} = -8 mA		2.4			2.4			v
VOH	V _{CC} = 3 V	I _{OH} = - 24 mA		2						٧
	ACC = 2 A	I _{OH} = -32 mA					2			
	V _{CC} = 2.7 V	I _{OL} = 100 μA			0.2			0.2		
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
Voi		I _{OL} = 16 mA				0.4			0.4	v
V _{OL}	V _{CC} = 3 V	I _{OL} = 32 mA				0.5			0.5	, v
	VCC = 3 V	I _{OL} = 48 mA			0.55					
		I _{OL} = 64 mA						0.55		
	$V_{CC} = 3.6 \text{ V},$	$V_I = V_{CC}$ or GND	Control			±1			±1	
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V	inputs			10			10	
l _l		V _I = 5.5 V				100			20	μA
	V _{CC} = 3.6 V	V _I = V _{CC}	A or B ports§			1			1	
		V _I = 0				-5			-5	
loff	$V_{CC} = 0$,	V_{I} or $V_{O} = 0$ to 4.5 V					ł		±100	μΑ
lun - i-n	V _{CC} = 3 V	V _I = 0.8 V	A or B ports	75			75			μА
l(hold)	VCC = 3 V	V _I = 2 V	A OI B POIG	-75			- 75			μΛ
^I OZH	V _{CC} = 3.6 V,	V _O = 3 V				1			1	μА
lozl	V _{CC} = 3.6 V,	V _O = 0.5 V				-1			-1	μA
			Outputs high	<u> </u>	0.13	0.39	<u> </u>	0.13	0.19	
Icc	V _{CC} = 3.6 V,	IO = 0,	Outputs low		8.8	14		8.8	12	mA
.00	V _I = V _{CC} or GND		Outputs disabled		0.13	0.39		0.13	0.19	»·
ΔICC¶	V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND					0.3			0.2	mA
Ci	V _I = 3 V or 0				4.5			4.5		pF
C _{io}	V _O = 3 V or 0) = 3 V or 0			11			11		pF

 $^{^{\}dagger}$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused terminals at V_{CC} or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SCBS140D - MAY 1992 - REVISED JULY 1995

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

		· ·		SN54L	VT646			SN74L	VT646		
			V _{CC} =		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
^f clock	ock Clock frequency		0	150	0	150	0	150	0	150	MHz
tw	Pulse duration, CLK high or low		3.3		3.3	• • •	3.3		3.3		ns
	Setup time, A or B before CLKAB↑ or	Data high	1.5		1.5		1.3		1.3		
^t su	CLKBA [↑]	Data low	2.5		3.0		2		2.4		ns
^t h	Hold time, A or B after CLKAB↑ or CLKBA↑		0.9		0.9		0.4		0.4		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

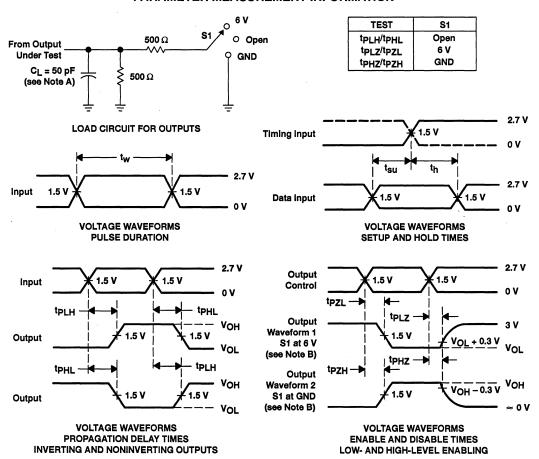
				SN54L	VT646			SN	74LVT6	46		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =	2.7 V	V	± 0.3 V			2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
fmax	,		150				150					MHz
t _{PLH}	CLKBA or	A or B	1.2	5.9		6.9	1.8	3.8	5.7		6.7	ns
^t PHL	CLKAB	AOIB	1.2	5.9		6.6	2.1	3.8	5.7		6.4	115
tPLH .	A or B	B or A	0.8	4.9		5.6	1.3	2.8	4.7		5.4	ns
tPHL		BOIA	0.6	4.8		5.5	1	2.7	4.6		5.3	118
^t PLH	0D4 04D‡	A or B	1	6.4		7.4	1.4	3.7	6.2		7.2	ns
^t PHL	SBA or SAB‡	AOIB	1	6.4	į	7	1.4	3.8	6.2		6.8	118
t _{PZH}	ŌĒ	A or B	0.6	6		7.4	1	3	5.8		7.2	
tPZL.	OE .	AOID	0.6	6.2		7.5	1	3.2	6		7.3	ns
^t PHZ	ŌĒ	A or B	1.4	6.7		7.1	2.3	4.3	6.5		6.9	ns
^t PLZ	OE .	AUID	1.4	6.4		6.5	2.2	3.8	5.8		5.9	118
tPZH	DIR	A or B	0.6	6.7		7.7	1	3.4	6.5		7.5	
^t PZL	אוט	A or B	0.8	6.5		7.3	1.2	3.4	6.3		7.1	ns
t _{PHZ}	DIR	A or B	0.8	7.4		8.3	1.7	4.1	7.2		8.1	
t _{PLZ}		DIR	AUID	1	6.7		7	1.5	3.5	5.8		6.3

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

SCBS140D - MAY 1992 - REVISED JULY 1995

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \, \Omega$, $t_{r} \leq 2.5 \, \text{ns}$, $t_{f} \leq 2.5 \, \text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

SCBS141E - MAY 1992 - REVISED JULY 1995

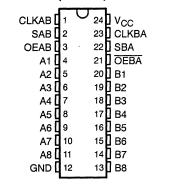
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW)
 Packages, Ceramic Chip Carriers (FK), and Ceramic (JT) DIPs

description

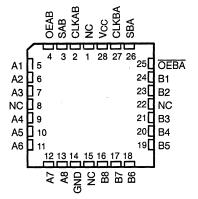
These bus transceivers and registers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT652 consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

SN54LVT652 . . . JT PACKAGE SN74LVT652 . . . DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVT652...FK PACKAGE (TOP VIEW)



NC - No internal connection

Output-enable (OEAB and OEBA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input selects real-time data and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT652.

SCBS141E - MAY 1992 - REVISED JULY 1995

description (continued)

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration, each output reinforces its input; therefore, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74LVT652 is available in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT652 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT652 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

		INPU	rs			DATA	A 1/0†	OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8	OPERATION OR FUNCTION
L	Н	H or L	H or L	Х	Х	Input	Input	Isolation
L	н	1	1	Х	X	Input	Input	Store A and B data
X	Н	1	H or L	Х	х	Input	Unspecified [‡]	Store A, hold B
н	Н	1	1	X‡	Х	Input	Output	Store A in both registers
L	X	H or L	1	Х	Х	Unspecified [‡]	Input	Hold A, store B
L	L	1	1	X	x‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	Χ	H or L	Х	, н	Output	Input	Stored B data to A bus
н	Н	X	Χ	L	Х	Input	Output	Real-time A data to B bus
н	н	H or L	X	н	Х	Input	Output	Stored A data to B bus
н	L	H or L	H or L	н	н	Output	Output	Stored A data to B bus and stored B data to A bus

[†] The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition of the clock inputs.

[‡] Select control = L; clocks can occur simultaneously

Select control = H; clocks must be staggered in order to load both registers

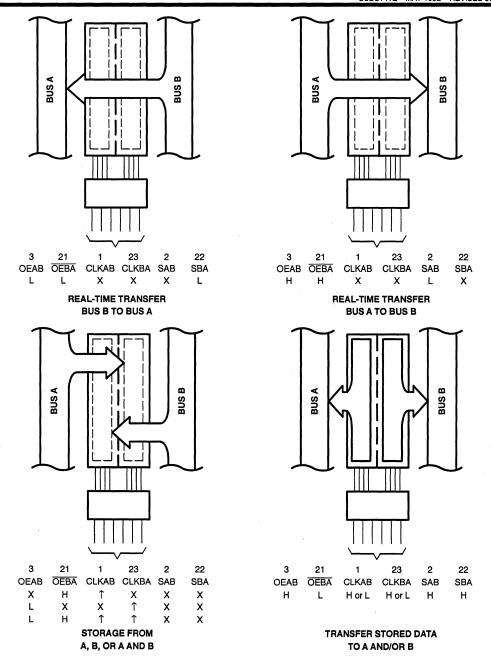


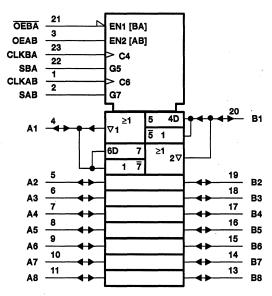
Figure 1. Bus-Management Functions

Pin numbers shown are for the DB, DW, JT, and PW packages.



SCBS141E - MAY 1992 - REVISED JULY 1998

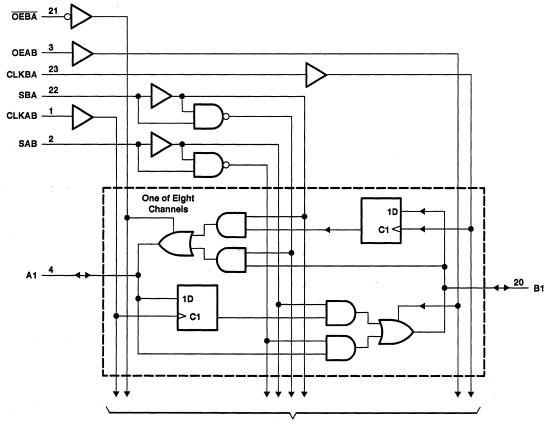
logic symbolt



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, and PW packages.



logic diagram (positive logic)



To Seven Other Channels

Pin numbers shown are for the DB, DW, JT, and PW packages.

SCBS141E - MAY 1992 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-o	ff state, V_O (see Note 1)0.5 V to 7 V
Current into any output in the low state, Io: SN54LVT652	
SN74LVT652	
Current into any output in the high state, IO (see Note 2): SN54I	LVT652
SN74I	LVT652 64 mA
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3	
, , , , , , , , , , , , , , , , , , , ,	DW package 1.7 W
	PW package 0.7 W
Storage temperature range, T _{stq}	
- · · · · · · · · · · · · · · · · · · ·	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			SN54L	VT652	SN74L	VT652	LINUT
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3,6	2.7	3.6	· V
VIH	High-level input voltage		2	Ü	2		V
VIL	Low-level input voltage			8.0		0.8	٧
VI	Input voltage		,4	\$ 5.5		5.5	٧
ЮН	High-level output current		\$	* –2 4		-32	mA _.
lOL	Low-level output current		ŞĬ	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	S. S.	10		10	ns/V
TA	Operating free-air temperature		~55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SCBS141E - MAY 1992 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER		OT CONDITIONS		SN	154LVT6	52	SN	74LVT65	52	LINUT
PARAMETER	11	ST CONDITIONS		MIN	TYP	MAX	MIN	TYPT	MAX	UNIT
VIK	V _{CC} = 2.7 V,	I _I = -18 mA				-1.2			-1.2	٧
	V _{CC} ≈ MIN to MAX‡,	I _{OH} = -100 μA		Vcc-0).2		VCC-0	.2		
	V _{CC} = 2.7 V,	I _{OH} = -8 mA		2.4			2.4			v
VOH	Van 2V	I _{OH} = -24 mA		2		_				V
	V _{CC} = 3 V	I _{OH} = -32 mA					2			
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
\ \v		I _{OL} = 16 mA				0.4			0.4	V
VOL	Van 2V	I _{OL} = 32 mA				0.5			0.5	V
	V _{CC} = 3 V	I _{OL} = 48 mA				0.55				
		I _{OL} = 64 mA							0.55	
	V _{CC} = 3.6 V,	$V_I = V_{CC}$ or GND	Control inputs		Z.S.	* ±1			±1	
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V	Control inputs		824	10			10	
l ₁		V _I = 5.5 V			1	20			20	μА
	V _{CC} = 3.6 V	V _I = V _{CC}	A or B ports§		8	5			5	
		V _I = 0		-	>	-10			-10	
loff	V _{CC} = 0,	V_1 or $V_0 = 0$ to 4.5	S V	-					±100	μΑ
harris	V _{CC} = 3 V	V _I = 0.8 V	A or B ports	75			75			μА
l(hold)	ACC = 2 A	V _I = 2 V	A OF B POFES	-75			-75			μζ
lozh	V _{CC} = 3.6 V,	V _O = 3 V				1			1	μA
lozl	V _{CC} = 3.6 V,	V _O = 0.5 V				-1			-1	μA
			Outputs high		0.13	0.19		0.13	0.19	
Icc	$V_{CC} = 3.6 \text{ V},$	$I_{O} = 0$,	Outputs low		8.8	12		8.8	12	mA
,00	V _I = V _{CC} or GND		Outputs disabled		0.13	0.19		0.13	0.19	
ΔICC¶	V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND					0.2			0.2	mA
Ci	V _I = 3 V or 0				4.5			4.5		pF
C _{io}	V _O = 3 V or 0				11			11		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused terminals at V_{CC} or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SCBS141E - MAY 1992 - REVISED JULY 1995

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

			SN54LVT652 SN74LVT652								
			V _{CC} = ± 0.		Vcc=	2.7 V	V _{CC} =		Vcc=	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
[†] clock	Clock frequency		0	150	, 0	150	0	150	0	150	MHz ³
tw	Pulse duration, CLK high or lov	<i>i</i>			25.91		3.3		3.3		ns
	Setup time, A or B before	Data high		<i>"</i> ⊘			1.2		1.2		
^t su	CLKAB↑ or CLKBA↑	Data low		4,94			. 2		2.5		ns
th	Hold time, A or B after CLKAB↑ or CLKBA↑						0.5		0.5		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

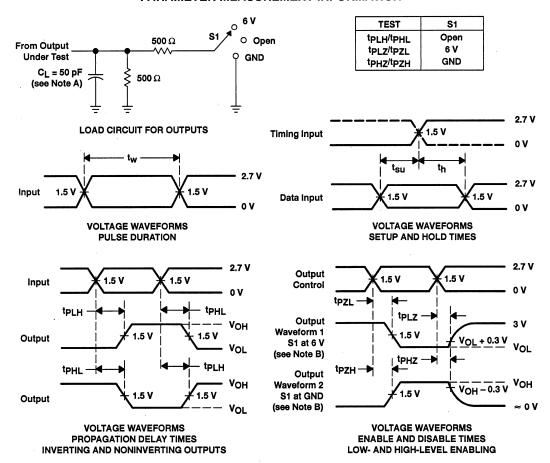
				SN54L	VT652			SN	74LVT6	52		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =	2.7 V	V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
fmax							150			150		MHz
t _{PLH}	CLKBA or	A or B					1.8	3.7	6		6.9	ns
tPHL	CLKAB	A or B					2	3.7	5.7		6.4	110
tPLH	A or B	B or A					1.2	2.8	4.7		5.5	ns
tPHL	AUIB	BUIA			ZÎ.		1	2.6	4.6		5.3	IIS
t _{PLH}	SBA or SAB‡	A or B			§*		1.4	3.7	6.4		7.6	ns
t _{PHL}	SBA or SAB+	AOFB		ث.	*		1.4	4	6.2		6.8	115
^t PZH	OEBA	А		<u> </u>			1	2.9	5.8		7.2	ns
tPZL	OEBA	^		Æ			1	3	6		7.3	118
^t PHZ	OEBA	Α					2.2	3.9	6.5		6.9	ns
tPLZ	OEBA	^					1.8	3.2	5.8		5.9	HS
^t PZH	OEAB	В					1	3.3	6.5		7.5	ns
^t PZL] CEAB	В					1.2	3.4	6.3		7.1	IIS
^t PHZ	OEAR	В					1.7	4.5	7.2		8.1	
tPLZ	OEAB						1.5	3.8	5.8		6.3	ns

[†] All typical values are at VCC = 3.3 V, TA = 25°C.

[‡] These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

SCBS141E - MAY 1992 - REVISED JULY 1995

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_f \leq 2.5 \,\text{ns}$, $t_f \leq 2.5 \,\text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

SCBS152E - MAY 1992 - REVISED JULY 1995

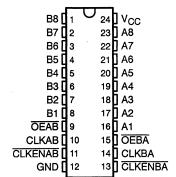
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW)
 Packages, Ceramic Chip Carriers (FK), and Ceramic (JT) DIPs

description

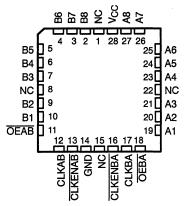
These octal bus transceivers and registers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT2952 consist of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high

SN54LVT2952 . . . JT PACKAGE SN74LVT2952 . . . DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVT2952 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

transition of the clock (CLKAB or CLKBA) input provided that the clock-enable (CLKENAB or CLKENBA) input is low. Taking the output-enable (OEAB or OEBA) input low accesses the data on either port.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT2952 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT2952 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT2952 is characterized for operation from -40°C to 85°C.



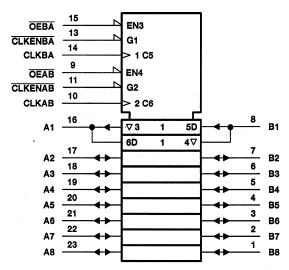
SCBS152E - MAY 1992 - REVISED JULY 1995

FUNCTION TABLET

	INPUTS										
CLKENAB	CLKAB	OEAB	Α	В							
Н	X	L	Х	в ₀ ‡							
х	H or L	L	Х	В ₀ ‡ В ₀ ‡							
L	1	L	L	L							
L	1	L	Н	н							
X	X	Н	Х	z							

[†] A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENBA, CLKBA, and OEBA.

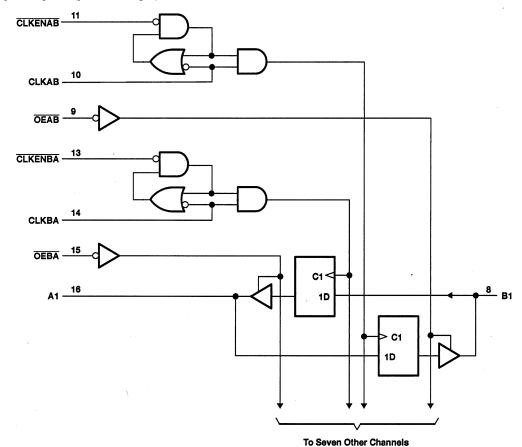
logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, and PW packages.

[‡]Level of B before the indicated steady-state input conditions were established

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and PW packages.

SCBS152E - MAY 1992 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Voltage range applied to any output in the high state or power-off state, VO (see Note 1)	0.5 V to 7 V
Current into any output in the low state, Io: SN54LVT2952	96 mA
SN74LVT2952	128 mA
Current into any output in the high state, Io (see Note 2): SN54LVT2952	48 mA
SN74LVT2952	64 mA
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I_{OK} ($V_O < 0$)	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB package	
DW package	1.7 W
PW package	0.7 W
Storage temperature range, T _{stq}	
3 3-, -3tg	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions (see Note 4)

			SN54LV	T2952	SN74LV	UNIT	
	:		MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3,6	2.7	3.6	٧
VIH	High-level input voltage		2	Ţ,	2		٧
VIL	Low-level input voltage			0.8		0.8	٧
٧ _I	Input voltage		. <	₹ 5.5		5.5	٧
ЮН	High-level output current		<u>(</u>)	-24		-32	mA
loL	Low-level output current		رَيْ	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	F	10		10	ns/V
TA	Operating free-air temperature		~55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

SCBS152E - MAY 1992 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	-	FOT CONDITIONS		SN	54LVT29	52	SN	74LVT29	52	UNIT
PARAMETER		EST CONDITIONS		MIN	TYPT	MAX	MIN	TYP	MAX	UNII
VIK	$V_{CC} = 2.7 \text{ V},$	l = −18 mA				-1.2			-1.2	٧
	$V_{CC} = MIN \text{ to } MAX^{\ddagger},$	l _{OH} = -100 μA		VCC-C).2		VCC-0).2		
1/	$V_{CC} = 2.7 \text{ V},$	I _{OH} = -8 mA		2.4			2.4			v
VOH	V _{CC} = 3 V	IOH = - 24 mA		2						, v
	, ACC = 2 A	I _{OH} = -32 mA					2			
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5	İ
V		I _{OL} = 16 mA				0.4			0.4	l v
VOL	Vac. 2 V	I _{OL} = 32 mA				0.5			0.5	V
	V _{CC} = 3 V	I _{OL} = 48 mA				0.55				
		I _{OL} = 64 mA				Ø			0.55	
	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	Combrelianute		ŢĴ.	±1			±1	
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V	Control inputs		,4"	10			10	
lį	$V_{CC} = 3.6 \text{ V}$ $V_{I} = 5.5 \text{ V}$ $V_{I} = V_{CC}$			Ų.	20			20	μА	
		$V_1 = V_{CC}$ A or B ports§	A or B ports§	Ŕ	Q"	5			5	
	,	V _I = 0]	S		-10			-10	
loff	$V_{CC} = 0$,	V _I or V _O = 0 to 4.5	V						±100	μА
lun in	V _{CC} = 3 V	V _I = 0.8 V	A or B ports	75			75			
[[] I(hold)	ACC = 2 A	V _I = 2 V	A or B ports	-75			-75			μА
^I OZH	$V_{CC} = 3.6 \text{ V},$	V _O = 3 V				1			1	μА
lozL	$V_{CC} = 3.6 \text{ V},$	V _O = 0.5 V				-1			-1	μA
,			Outputs high		0.13	0.19		0.13	0.19	
Icc	V _{CC} = 3.6 V, V _I = V _{CC} or GND	$I_{O}=0,$	Outputs low		8.8	12		8.8	12	mA
	11-100 01 0115		Outputs disabled		0.13	0.19		0.13	0.19	
ΔICC¶	$V_{CC} = 3 \text{ V to } 3.6 \text{ V,}$ Other inputs at V_{CC} o	One input at V _{CC} or GND	– 0.6 V,			0.2			0.2	mA
Ci	V _I = 3 V or 0				4.5			4.5		pF
C _{io}	V _O = 3 V or 0				11.5			11.5		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused terminals at V_{CC} or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SCBS152E - MAY 1992 - REVISED JULY 1995

timing requirement over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

					SN54LVT2952				/T2952		
			V _{CC} = 3 ± 0.3		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency						150		150	MHz	
t _w	Pulse duration H	CLK high			42.		3.3		3.3		ns
		CLK low			/S		3.3		3.3		
		Data high	2.6		2.9		2.5		2.8		ns
	Setup time, A or B before CLK↑	Data low	2.6	/.	3.1		2.5		3		
t _{su}		Data high	0.9	22	0.8		0.9		0.8		
	Setup time, CE before CLK↑	Data low	2.5	80	2.7		2.4		2.7		i i
1.	Hold time, A or B after CLK↑		1.5	Q	0.7		1.5		0.7		
th	Hold time, CE after CLK↑	2.6		2.6		2.5		2.6		ns	

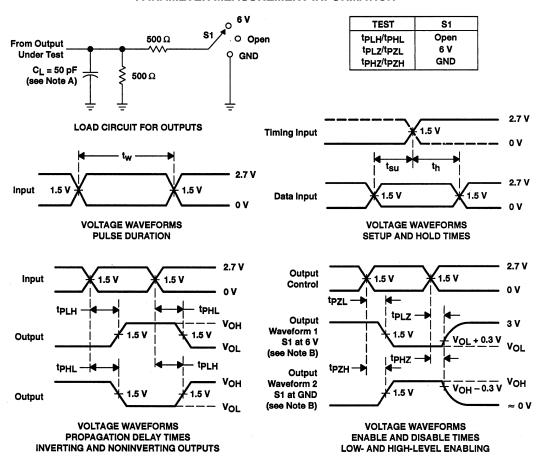
switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

				SN54L	/T2952			SN	74LVT29	52			
PARAMETER	FROM (INPUT)		TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT
r			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX		
fmax							150			150		MHz	
t _{PLH}	CLKBA or	A or B	1.3	6.4	2,7	7.4	1.3	3.6	6.1	2.7	7.1	ns	
^t PHL	CLKAB	AOIB	1.8	6.1	£2.7	7	1.8	3.7	6	2.7	6.9		
t _{PZH}	OEBA or	A or B	1	6.3	2.6	7.3	1	3.2	5.6	2.6	6.7	ns	
^t PZL	OEAB	A OI B	1.1	6, 6	2.9	8.2	1.2	3.2	6.5	2.9	8	115	
t _{PHZ}	OEBA or	A or B	1	ুণ	2.7	7.6	1	4.1	6.3	2.7	6.9	ns	
^t PLZ	OEAB OF	AVIB	1.6	₹5.8	1.7	6	1.6	3.3	5.1	1.8	5.3	115	

 $[\]dagger$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SCBS152E - MAY 1992 - REVISED JULY 1995

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \,\Omega$, $t_{r} \leq 2.5 \,\text{ns}$, $t_{f} \leq 2.5 \,\text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

General Information	1
ALB Widebus™	2 °
ALVC Widebus™	3
LVT Octals	4
LVTZ Octals: Power Up and 3 State	5
LVT Widebus™	6
LVT JTAG/IEEE 1149.1	7
LVC MSI and Octals	8
LVC Widebus™	9
LV MSI and Octals	10
GTL Transceivers and Backplane Drivers	11
Application Reports	12
Characteristics Information	13
Mechanical Data	14

Contents

		Page
SN54/74LVTZ240	3.3-V ABT Octal Buffers/Drivers With 3-State Outputs	5-3
SN54/74LVTZ244	3.3-V ABT Octal Buffers/Drivers With 3-State Outputs	5-9
SN54/74LVTZ245	3.3-V ABT Octal Bus Transceivers With 3-State Outputs	5-15

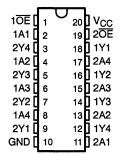
SCBS301B - SEPTEMBER 1993 - REVISED JULY 1995

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) DIPs

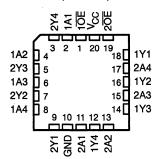
description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

SN54LVTZ240 . . . J PACKAGE SN74LVTZ240 . . . DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVTZ240....FK PACKAGE (TOP VIEW)



These devices are organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVTZ240 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

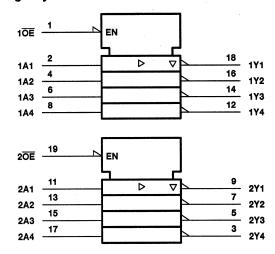
The SN54LVTZ240 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVTZ240 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each buffer)

١	INP	JTS	OUTPUT
	ŌĒ	Α	Y
	L	Н	L
1	L	L	н
	Н	Х	Z

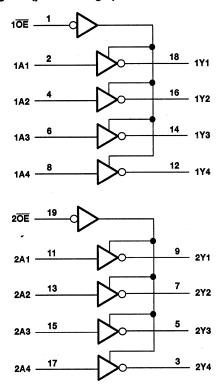
SN54LVTZ240, SN74LVTZ240 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SCBS301B - SEPTEMBER 1993 - REVISED JULY 1995

logic symbol[†]



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SCBS301B - SEPTEMBER 1993 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} —0.5 V to 4.6 V Input voltage range, V_{I} (see Note 1) —0.5 V to 7 V Voltage range applied to any output in the high state or power-off state, V_{O} (see Note 1) —0.5 V to 7 V Current into any output in the low state, I_{O} : SN54LVTZ240 —96 mA SN74LVTZ240 —128 mA Current into any output in the high state, I_{O} (see Note 2): SN54LVTZ240 —48 mA SN74LVTZ240 —64 mA Input clamp current, I_{IK} (V_{I} < 0) —50 mA Output clamp current, I_{OK} (V_{O} < 0) —50 mA Maximum power dissipation at T_{A} = 55°C (in still air) (see Note 3): DB package —0.6 W DW package —0.6 W

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and $V_O > V_{CC}$.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

		,	SN54LV	TZ240	SN74LV	TZ240	UNIT
		·	MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage		2	42.			٧
V _{IL} _	Low-level input voltage			0.8		0.8	٧
VI	Input voltage			5.5		5.5	٧
ЮН	High-level output current			ື −24		-32	mA
loL	Low-level output current		,3	48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled	/ς)"	10		10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate		₹ 200		200		μs/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	-	FOT COMPLETIONS		SN	54LVTZ2	40	SN	74LVTZ2	240				
PARAMETER	'	EST CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNIT			
VIK	$V_{CC} = 2.7 \text{ V},$	l = −18 mA			-	-1.2			-1.2	٧			
	V _{CC} = MIN to MAX [‡] ,	IOH = -100 μA		Vcc-0).2		VCC-C).2					
V	V _{CC} = 2.7 V,	IOH = - 8 mA		2.4			2.4			v			
VOH	V _{CC} = 3 V	IOH = - 24 mA		2						٧			
	VCC = 3 V	IOH = -32 mA					2						
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2				
	VCC = 2.7 V	I _{OL} = 24 mA			0.5			0.5					
VOL		I _{OL} = 16 mA				0.4			0.4	l _v			
VOL	V _{CC} = 3 V	I _{OL} = 32 mA				0.5			0.5	٧			
	VCC = 3 V	I _{OL} = 48 mA			0.55								
		I _{OL} = 64 mA							0.55				
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V				10			10				
l _l		$V_I = V_{CC}$ or GND	Control inputs		±1				±1	μΑ			
4	V _{CC} = 0 to 3.6 V	V _I = V _{CC}	Data inputs		64	1			1	μΛ			
		V ₁ = 0	Data inputs		~~	-5			-5				
loff	V _{CC} = 0 V,	V_{I} or $V_{O} = 0$ to 4.5 \	,		Ž Ž				±100	μА			
IOZPU [§]	$V_{CC} = 0$ to 1.5 V,	$V_O = 0.5 \text{ V to 3 V},$	OE = X		Š'				±50	μА			
IOZPD\$	$V_{CC} = 1.5 \text{ V to 0},$	$V_O = 0.5 \text{ V to 3 V},$	OE = X	å					±50	μA			
la in	V _{CC} = 3 V	V _I = 0.8 V	A inputs	75			75						
[[] l(hold)	ACC = 2 A	V _I = 2 V	Ainputs	-75			-75		-1.2 0.2 0.5 0.4 0.5 10 ±1 1 -5 ±100 ±50 ±50 -5 0.225 12 0.225	μА			
lozh	V _{CC} = 3.6 V,	V _O = 3 V				5			5	μA			
^I OZL	V _{CC} = 3.6 V,	V _O = 0.5 V				-5			-5	μA			
			Outputs high		0.12	0.5		0.12	0.225				
lcc	V _{CC} = 3.6 V,	$I_{O} = 0$,	Outputs low		8.6	14		8.6	12	mA			
100	V _I = V _{CC} or GND		Outputs disabled		0.12	0.5		0.12	0.225	IIIA			
ΔICC¶	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} o		0.6 V,			0.3			0.2	mA ⁻			
Ci	V _I = 3 V or 0				4			4		pF			
Co	V _O = 3 V or 0				8			8		pF			

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] This parameter is specified by characterization.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SN54LVTZ240, SN74LVTZ240 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SCBS301B - SEPTEMBER 1993 - REVISED JULY 1995

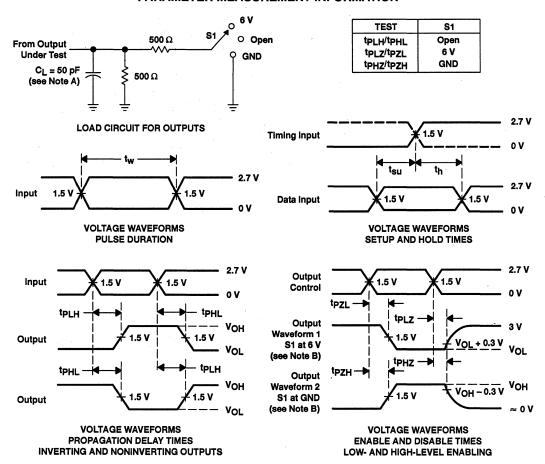
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

				SN54L	/TZ240			SN	74LVTZ2	240			
PARAMETER	FROM (INPUT)		TO (OUTPUT)	V _{CC} =		V _{CC} =	2.7 V	V	± 0.3 V	٧	V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX		
tPLH	Α		1	4.5	3	5.4	1	2.5	4.3		5.2	ns	
^t PHL		1	<u>'</u>	1	4.5	&'	5.2	1	2.5	4.3		5	115
^t PZH	<u> </u>	V	1	5.4	*	6.5	1	2.7	5.2		6.3	ns	
^t PZL	ŌĒ	'	1	5¥		7.4	1	3.1	5.2		6.7	115	
^t PHZ	ŌĒ	v	2	_C 5.8		6.5	2	3.9	5.6		6.3	ns	
^t PLZ		OE Y	1.6	₹ 5.3		5.8	1.6	3.2	5.1		5.6	HS	

 $[\]dagger$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SCBS301B - SEPTEMBER 1993 - REVISED JULY 1995

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control,
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\hat{\Omega}$, $t_r \leq 2.5 \,\text{ns}$, $t_f \leq 2.5 \,\text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

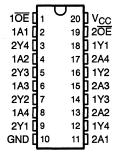
SCBS302C - SEPTEMBER 1993 - REVISED JULY 1995

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) DIPs

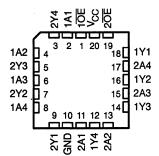
description

These octal buffers/drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation with the capability to provide a TTL interface to a 5-V system environment.

SN54LVTZ244 . . . J PACKAGE SN74LVTZ244 . . . DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVTZ244 . . . FK PACKAGE (TOP VIEW)



These devices are organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

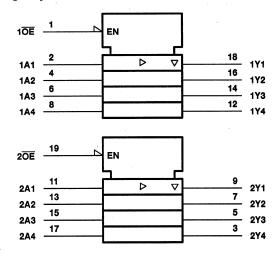
The SN74LVTZ244 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVTZ244 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVTZ244 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each buffer)

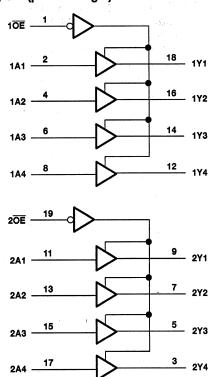
INP	JTS	OUTPUT
ŌĒ	Α	Y
L	Н	Н
L	L	L
Н	Х	Z

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SCBS302C - SEPTEMBER 1993 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1)	
Current into any output in the low state, Io: SN54LVTZ244	
SN74LVTZ244	128 mA
Current into any output in the high state, IO (see Note 2): SN54LVTZ244	48 mA
SN74LVTZ244	64 mA
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB package	0.6 W
DW package	1.6 W
PW package	
Operating free-air temperature range, T _A : SN54LVTZ244	
SN74LVTZ244	40°C to 85°C
Storage temperature range, T _{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and $V_O > V_{CC}$.

 The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			SN54LV	TZ244	SN74LV	TZ244	UNIT
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage	-	2	42	2		٧
VIL	Low-level input voltage			.0 .8		0.8	٧
VĮ	Input voltage			₹ 5.5		5.5	٧
ЮН	High-level output current			ື −24		-32	mA
IOL	Low-level output current			48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled	ΛΟ,	10		10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate		₹ 200		200		μs/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SCBS302C - SEPTEMBER 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST COMPLIANCE			SN	54LVTZ2	44	SN74LVTZ244			UNIT	
PARAMETER	TEST CONDITIONS				TYPT	MAX	MIN	TYPT	MAX	UNII	
VIK	$V_{CC} = 2.7 \text{ V},$	l _l = –18 mA			-1.2			-1.2	٧		
VOH	V _{CC} = MIN to MAX [‡] ,	Vcc-0).2		VCC-C).2					
	$V_{CC} = 2.7 \text{ V},$	2.4			2.4			.,			
	V 0.V	I _{OH} = -24 mA	2						٧		
	V _{CC} = 3 V	I _{OH} = -32 mA				2					
	V _{CC} = 2.7 V	l _{OL} = 100 μA				0.2			0.2		
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5		
V		I _{OL} = 16 mA				0.4			0.4	v	
VOL	V 2V	I _{OL} = 32 mA			0.5				.5		
	VCC = 3 V	I _{OL} = 48 mA		0.55							
		IOL = 64 mA						0.55			
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V				10			10		
1.	V _{CC} = 0 to 3.6 V	VI = VCC or GND	Control inputs		, S	/ ±1			±1		
lį		V _I = V _{CC}	Data lassata		64	1			1	μA	
		V _I = 0 Data inputs			Z ^N	-5			-5	L	
l _{off}	V _{CC} = 0 V,	V _I or V _O = 0 to 4.5 \	<i>,</i>		\$				±100	μА	
I _{OZPU} §	$V_{CC} = 0 V \text{ to } 1.5 V,$	$V_O = 0.5 \text{ V to 3 V},$	OE = X	ۇ. ا	7			,	±50	μА	
IOZPD§	V _{CC} = 1.5 V to 0,	V _O = 0.5 V to 3 V,	OE = X	4,	,				±50	μА	
		V _I = 0.8 V	A :	75			75				
l (hold)	V _{CC} = 3 V	V ₁ = 2 V	A inputs	-75			-75			μA	
lozh	V _{CC} = 3.6 V,	V _O = 3 V				5			5	μА	
lozl	V _{CC} = 3.6 V,	V _O = 0.5 V	,			-5			-5	μА	
		I _O = 0,	Outputs high		0.12	0.5		0.12	0.225		
laa	$V_{CC} = 3.6 \text{ V},$		Outputs low		8.6	15		8.6	15	mA	
Icc	V _I = V _{CC} or GND		Outputs disabled		0.12	0.5		0.12	0.225	IIIA	
ΔICC¶	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND					0.3			0.2	mA	
Ci	V _I = 3 V or 0				4			4		pF	
Со	V _O = 3 V or 0				8			8		pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] This parameter is specified by characterization.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SCBS302C - SEPTEMBER 1993 - REVISED JULY 1995

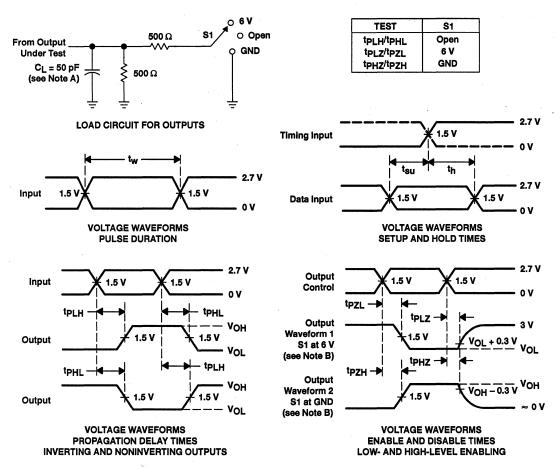
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

		TO (OUTPUT)	SN54LVTZ244				SN74LVTZ244							
PARAMETER	FROM (INPUT)		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT		
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX			
tPLH	Α	Y	1	4.7	,5,5	5.2	1	2.5	4.1		5	ns		
tPHL			1	4.4	Ž.	5.4	1	2.5	4.1		5.2			
^t PZH	ŌĒ	OF.	ŌĒ	· ·	1	5.4	14.	6.5	1	2.7	5.2		6.3	ns
^t PZL		OE '	1.1	5,43	•	7.6	1.1	3.1	5.2		6.7	113		
t _{PHZ}	ŌĒ	V	1.9	χŽ		6.9	1.9	3.9	5.6		6.3	ne		
tPLZ		'	1.8	Q 5.5		6	1.8	3.2	5.1		5.6	ns		

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SCBS302C - SEPTEMBER 1993 - REVISED JULY 1995

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_r \leq 2.5 \,ns$, $t_f \leq 2.5 \,ns$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



SN54LVTZ245, SN74LVTZ245 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

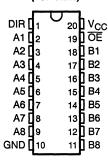
SCBS303B - DECEMBER 1993 - REVISED JULY 1995

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V **Operation and Low-Static Power** Dissipation
- **High-Impedance State During Power Up** and Power Down
- Support Mixed-Mode Signal Operation (5-V) Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) DIPs

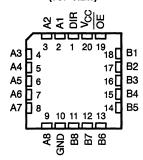
description

These octal bus transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

SN54LVTZ245 . . . J PACKAGE SN74LVTZ245...DB, DW, OR PW PACKAGE (TOP VIEW)



SN54LVTZ245...FK PACKAGE (TOP VIEW)



These devices are designed for asynchronous communication between data buses. They transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the devices so the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVTZ245 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVTZ245 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVTZ245 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

INP	UTS	OPERATION
ŌĒ	DIR	OPERATION
L	L	B data to A bus
L	н	A data to B bus
Н	X	Isolation



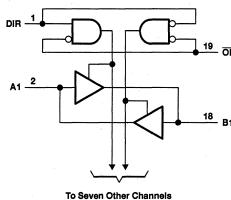
SN54LVTZ245, SN74LVTZ245 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS303B - DECEMBER 1993 - REVISED JULY 1995

logic symbol†

ŌĒ G3 3EN1[BA] 3EN2[AB] 18 В1 2∇ **D** 17 A2 16 АЗ **B3** 15 5 A4 **B**4 6 14 **B**5 Α5 7 13 A6 **B6** R 12 Α7 **B7** 9 11 **A8 B8**

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1) .	0.5 V to 7 V
Current into any output in the low state, IO: SN54LVTZ245	96 mA
SN74LVTZ245	128 mA
Current into any output in the high state, IO (see Note 2): SN54LVTZ245	48 mA
SN74LVTZ245	64 mA
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB package	
DW package	1.6 W
PW package	0.7 W
Storage temperature range, T _{stq}	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54LVTZ245, SN74LVTZ245 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS303B - DECEMBER 1993 - REVISED JULY 1995

recommended operating conditions (see Note 4)

			SN54LV	TZ245	SN74LV	UNIT	
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧
ViH	High-level input voltage		2		2		V
VIL	Low-level input voltage			0.8		0.8	V
VI	Input voltage			5.5		5.5	٧
ЮН	High-level output current			-24		-32	mA
lOL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate		200		200		μs/V
TA	Operating free-air temperature		-55	125	-40	85	့

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



SN54LVTZ245, SN74LVTZ245 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS303B - DECEMBER 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		EST CONDITIONS		SN	54LVTZ2	45	SN	74LVTZ2	45	UNIT
PARAMETER	"	EST CONDITIONS	·	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
VIK	$V_{CC} = 2.7 \text{ V},$	lj = -18 mA				-1.2			-1.2	٧
V _{CC} = MIN to MAX‡,		lOH = -100 μA		V _{CC} -C).2		VCC-C).2		
V _{OH} V _{CC} = 2.7 V _{CC} = 3 V	V _{CC} = 2.7 V,		2.4			2.4			v	
	V 2V	I _{OH} = -8 mA		2						V
•	ACC = 2 A	IOH = -32 mA					2			
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2	
		I _{OL} = 24 mA				0.5			0.5	
V		I _{OL} = 16 mA				0.4			0.4	v
VOL	V 0.V	IOL = 32 mA				0.5			0.5	v
	VCC = 3 V	I _{OL} = 48 mA				0.55				
		IOL = 64 mA							0.55	
	$V_{CC} = 3.6 \text{ V},$	V _I = V _{CC} or GND	Comband Samuels			±1			±1	
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V	Control inputs			10			10	μΑ
ij	V _{CC} = 3.6 V	V _I = 5.5 V	A or B ports§			100			20	
		V _I = V _{CC}				5			5	
		V ₁ = 0				-10			-10	
l _{off}	$V_{CC} = 0$,	V _I or V _O = 0 to 4.5	V						±100	μА
lozpu [¶]	V _{CC} = 0 to 1.5 V,	$V_O = 0.5 \text{ V to 3 V},$	OE = X						±50	μА
lozpd [¶]	V _{CC} = 1.5 V to 0,	V _O = 0.5 V to 3 V,	ŌĒ = X						±50	μА
	V 0V	V _I = 0.8 V	A B d.	75			75			
ⁱ l(hold)	V _{CC} = 3 V	V _I = 2 V	A or B ports	-75			-75			μА
lozh	$V_{CC} = 3.6 \text{ V},$	V _O = 3 V				1			1	μА
IOZL	V _{CC} = 3.6 V,	V _O = 0.5 V				-1			-1	μА .
			Outputs high		0.13	0.5		0.13	0.19	
loo	V _{CC} = 3.6 V,	$I_{O} = 0$,	Outputs low		8.8	14		8.8	12	mA
loc	V _I = V _{CC} or GND		Outputs disabled		0.13	0.5		0.13	0.19	IIIA
Δlcc#	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or		- 0.6 V,		-	0.3			0.2	mA
Ci	V _I = 3 V or 0				4			4		pF
Cio	V _O = 3 V or 0				10			10		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused terminals at V_{CC} or GND

This parameter is specified by characterization but is not tested.

[#] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54LVTZ245, SN74LVTZ245 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS303B - DECEMBER 1993 - REVISED JULY 1995

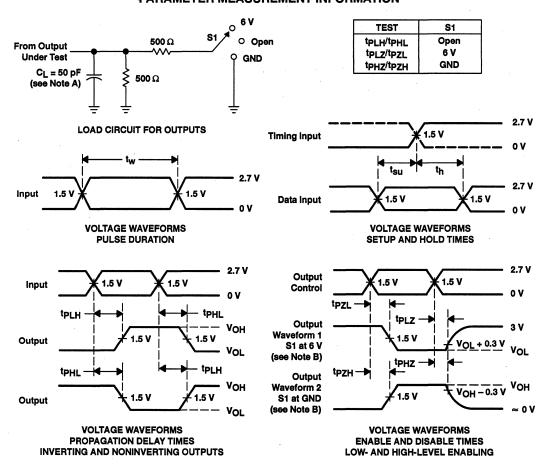
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

				SN54L	/TZ245			SN	74LVTZ2	245				
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	3.3 V 3 V	V _{CC} =	2.7 V	V	± 0.3 V	٧	V _{CC} =	2.7 V	UNIT		
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX			
^t PLH	A or B	B or A	1	4.6		5.3	1	2.5	4		5.2	ns		
tPHL	AOID	AOID	AGIB	BULA	1	4.1		5.7	1	2.5	4		5.5	115
^t PZH	ŌĒ	A or B	1.1	6.1		7.2	1.1	3.3	5.9		7.1	ns		
^t PZL	OE.	7015	1.5	6.6		8	1.5	3.8	6.5		7.9	113		
t _{PHZ}	ŌĒ	A or B	2.2	6.2		7	2.2	4.3	5.9		6.5	ns		
tPLZ	OE	AOIB	2	6.3		5.9	2	3.9	5.5		5.6	118		

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.



PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

General Information	1
ALB Widebus™	2
ALVC Widebus™	3
LVT Octals	4
LVTZ Octals: Power Up and 3 State	5
LVT Widebus™	6
LVT JTAG/IEEE 1149.1	7
LVC MSI and Octals	8
LVC Widebus™	9
LV MSI and Octals	10
GTL Transceivers and Backplane Drivers	11
Application Reports	12
Characteristics Information	13
Mechanical Data	14

Contents

		rage
SN54/74LVT16244A	3.3-V ABT 16-Bit Buffers/Drivers With 3-State Outputs	6-3
SN54/74LVT162244	3.3-V ABT 16-Bit Buffers/Drivers With 3-State Outputs	6-9
SN54/74LVT16245A	3.3-V ABT 16-Bit Bus Transceivers With 3-State Outputs	6-15
SN54/74LVT162245	3.3-V ABT 16-Bit Bus Transceivers With 3-State Outputs	6-21
SN54/74LVT16373	3.3-V ABT 16-Bit Transparent D-Type Latches With 3-State Outputs	6-27
SN54/74LVT162373	3.3-V ABT 16-Bit Transparent D-Type Latches With 3-State Outputs	6-33
SN54/74LVT16374	3.3-V ABT 16-Bit Edge-Triggered D-Type Flip-Flops With 3-State Outputs	6-37
SN54/74LVT162374	3.3-V ABT 16-Bit Edge-Triggered D-Type Flip-Flops With 3-State Outputs	
SN54/74LVT16500	3.3-V ABT 18-Bit Universal Bus Transceivers With 3-State Outputs	6-47
SN54/74LVT16501	3.3-V ABT 18-Bit Universal Bus Transceivers With 3-State Outputs	6-55
SN54/74LVT16543	3.3-V ABT 16-Bit Registered Transceivers With 3-State Outputs	6-63
SN54/74LVT16600	3.3-V ABT 18-Bit Universal Bus Transceivers With 3-State Outputs	6-71
SN54/74LVT16601	3.3-V ABT 18-Bit Universal Bus Transceivers With 3-State Outputs	6-77
SN54/74LVT16646	3.3-V ABT 16-Bit Bus Transceivers With 3-State Outputs	6-83
SN54/74LVT16652	3.3-V ABT 16-Bit Bus Transceivers and Registers With 3-State Outputs	6-93
SN74LVT16835	3.3-V ABT 18-Bit Universal Bus Driver With 3-State Outputs	6-101
SN54/74LVT16952	3.3-V ABT 16-Bit Registered Transceivers With 3-State Outputs	6-107

SN54LVT16244A, SN74LVT16244A 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SN54LVT16244A . . . WD PACKAGE

SCBS142E - MAY 1992 - REVISED JANUARY 1996

Technology (ABT) Design for 3.3-V Operation and Low-Static Power	SN74LVT16244A DGG OR DL PACKAGE (TOP VIEW)
 Dissipation Members of the Texas Instruments Widebus™ Family 	1OE [1 48] 2OE 1Y1 [2 47] 1A1 1Y2 [3 46] 1A2
 Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC}) 	GND
 Support Unregulated Battery Operation Down to 2.7 V 	1Y4
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	2Y1
ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds	GND [] 10 39 [] GND 2Y3 [] 11 38 [] 2A3 2Y4 [] 12 37 [] 2A4
200 V Using Machine Model (C = 200 pF, R = 0)	3Y1 13 36 3A1 3Y2 114 35 3A2
 Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17 	GND 115 34 GND

Support Live Insertion

Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise

Bus-Hold Data Inputs Eliminate the Need

for External Pullup Resistors

• Flow-Through Architecture Optimizes **PCB Layout**

State-of-the-Art Advanced BiCMOS

 Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

GIAD I	44	45 H GIVD
1Y3 [5	44 🛮 1A3
	6	43] 1A4
V _{CC}	7	42 V _{CC}
2Y1 [41 2A1
2Y2 [9	40 2A2
GND [10	39 GND
2Y3 []11	38 🛮 2A3
2Y4 [12	37 🛮 2A4
3Y1 [13	36 🛮 3A1
3Y2 [14	35 3A2
GND [15	34 🛮 GND
3Y3 [16	33 🛮 3A3
3Y4 [32 🛭 3A4
v _{cc} l] 18	31 V _{CC}
4Y1	19	30 🛮 4A1
4Y2	20	29 🛮 4A2
GND	21	28 GND
4Y3 [22	27 🛮 4A3
4Y4	23	26 🛮 4A4
4 0E	24	25 3OE

description

The 'LVT16244A are 16-bit buffers and line drivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable (OE) inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16244A is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

Widebus is a trademark of Texas Instruments Incorporated



SCBS142E - MAY 1992 - REVISED JANUARY 1996

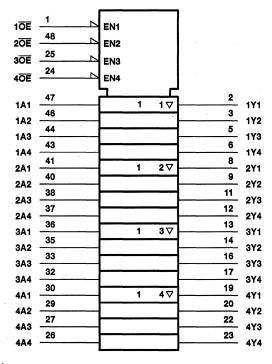
description (continued)

The SN54LVT16244A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16244A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (each buffer)

INP	JTS	OUTPUT
ŌĒ	Α	Y
L	Н	Н
L	L	L
Н	Χ	z

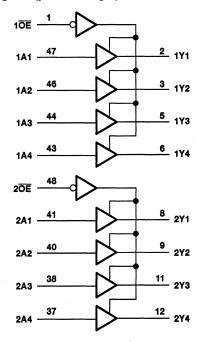
logic symbol†

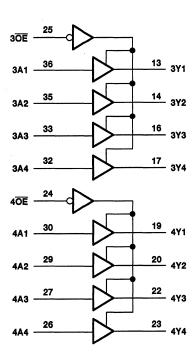


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SCBS142E - MAY 1992 - REVISED JANUARY 1996

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC} –C	.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high state or power-off state, VO (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, Io: SN54LVT16244A	96 mA
SN74LVT16244A	128 mA
Current into any output in the high state, IO (see Note 2): SN54LVT16244A	48 mA
SN74LVT16244A	64 mA
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	0.85 W
DL package	1.2 W
Storage temperature range, T _{stg}	5°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current flows only when the output is in the high state and VO > VCC.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.



SN54LVT16244A, SN74LVT16244A 3.3-V ABT 16-BIT BUFFERS/DRIVERS **WITH 3-STATE OUTPUTS**

SCBS142E - MAY 1992 - REVISED JANUARY 1996

recommended operating conditions (see Note 4)

	,			T16244A	SN74LV	UNIT	
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	V _{IH} High-level input voltage		2		2		- V
VIL	V _{IL} Low-level input voltage			0.8		0.8	٧
VI	V _I Input voltage			5.5		5.5	٧
ЮН	High-level output current			-24		-32	mA
loL	OL Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS			SN54LV	Г16244А	SN74	LVT162	44A	UNIT
PARAMETER		TEST CONDITIONS		MIN	MAX	MIN	TYP	MAX	UNII
VIK	$V_{CC} = 2.7 \text{ V},$	lj = -18 mA			-1.2			-1.2	٧
	$V_{CC} = MIN \text{ to MAX}^{\ddagger}$,	i _{OH} = -100 μA		V _{CC} -0.	2	VCC-0	.2		
Vou	$V_{CC} = 2.7 \text{ V},$	I _{OH} = – 8 mA		2.4		2.4			V
VOH	V _{CC} = 3 V	IOH = - 24 mA		2					V
	VCC = 3 V	I _{OH} = -32 mA				2			
	V _{CC} = 2.7 V	l _{OL} = 100 μA			0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA			0.5			0.5	
V _{OL}		I _{OL} = 16 mA			0.4			0.4	V
, AOF	V _{CC} = 3 V	I _{OL} = 32 mA			0.5			0.5	٧
	\vCC = 3 v	I _{OL} = 48 mA	,		0.55]
		I _{OL} = 64 mA						0.55	
	$V_{CC} = 0$ or MAX ‡ ,	V _I = 5.5 V			50			10	
· 1 ₁	,	V _I = V _{CC} or GND	Control inputs		±1			±1	μА
"	V _{CC} = 3.6 V	V _I = V _{CC}	Data inputs		1			1	μΑ
		V _I = 0	Data inputs		-5			-5	
l _{off}	$V_{CC} = 0$,	V_I or $V_O = 0$ to 4.5 V						±100	μА
liza . i .n	V _{CC} = 3 V	V _I = 0.8 V	A inputs	75		75			μА
l(hold)	VCC = 3 V	V _I = 2 V] A inputs	-75		-75			μΑ
lozh	$V_{CC} = 3.6 \text{ V},$	V _O = 3 V			5			5	μА
lozl	$V_{CC} = 3.6 \text{ V},$	V _O = 0.5 V			-5			-5	μΑ
			Outputs high		0.19			0.09	
ICC	V _{CC} = 3.6 V, V _I = V _{CC} or GND	IO = 0,	Outputs low		5			5	mA
	11-100 31 3115		Outputs disabled		0.19		-	0.09	
Δl _{CC} §	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} o	One input at V _{CC} – 0.6 r GND	V,		0.2			0.2	mA
Ci	V _I = 3 V or 0						4		pF
Co	V _O = 3 V or 0						10		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.



[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

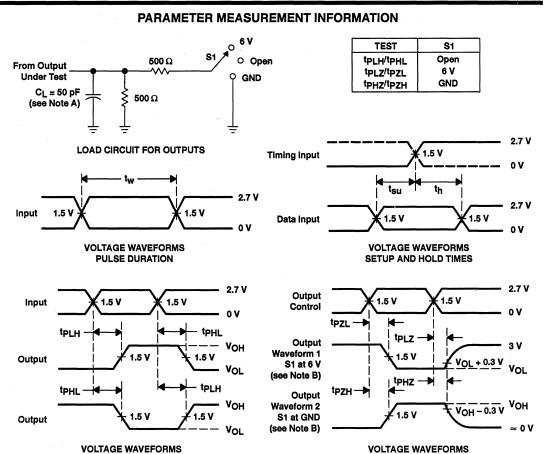
SN54LVT16244A, SN74LVT16244A 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SCBS142E - MAY 1992 - REVISED JANUARY 1996

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

				SN54LVT16244A			SN74LVT16244A					
PARAMETER	FROM (INPUT)			3.3 V 3 V	V _{CC} =	2.7 V		± 0.3 V	٧	V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
^t PLH	Α	v	1	4.4		5.1	1	2.3	4.1		5	ns
^t PHL	^	ī	1	4.5		5.3	1	2.3	4.1		5.2	115
tPZH	ŌĒ		1	5.3		6.4	1	2.6	5.2		6.3	ns
tPZL	OE	1	1	5.3		6.8	1	2.6	5.2		6.7	113
tPHZ	ŌĒ	v	2.1	7		7.7	2.2	3.9	5.7		6.3	ns
t _{PLZ}	OE .	1	1.9	5.9		5.9	2	3.7	5.1		5.6	10

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SCBS142E - MAY 1992 - REVISED JANUARY 1996



NOTES: A. C_L includes probe and jig capacitance.

PROPAGATION DELAY TIMES

INVERTING AND NONINVERTING OUTPUTS

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \Omega$ tr \leq 2.5 ns, tr \leq 2.5 ns,

ENABLE AND DISABLE TIMES

LOW- AND HIGH-LEVEL ENABLING

D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVT162244, SN74LVT162244 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS258D - JUNE 1993 - REVISED JULY 1995

- Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments Widebus™ Family
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes
 PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVT162244 . . . WD PACKAGE SN74LVT162244 . . . DGG OR DL PACKAGE (TOP VIEW)

		_	1
10E [$ _{1}$	48	2 <u>0E</u>
1Y1 [2	47] 1A1
1Y2 [3	46	1A2
GND [GND
1Y3 [] 1A3
1Y4 [1] 1A4
v _{cc} [□ v _{cc}
2Y1 [2A1
2Y2 [2A2
GND [10] GND
2Y3 [] 2A3
2Y4 [12	37] 2A4
3Y1 [] 3A1
3Y2 [35	3A2
GND [15	34	GND
3Y3 [16		3A3
3Y4 [] 3A4
v _{cc} [18	31] v _{cc}
4Y1 [30] 4A1
4Y2 [20	29] 4A2
GND [21	28] GND
4Y3 [22	27] 4A3
4Y4 [23	26] 4A4
4 0E [24	25] 3 <u>0E</u>
	i		1

description

The 'LVT162244 are 16-bit buffers and line drivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable $\overline{(OE)}$ inputs.

The outputs, which are designed to source or sink up to 12 mA, include $22-\Omega$ series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Widebus is a trademark of Texas Instruments Incorporated.

SN54LVT162244, SN74LVT162244 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS258D - JUNE 1993 - REVISED JULY 1995

description (continued)

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT162244 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT162244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT162244 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (each 4-bit buffer)

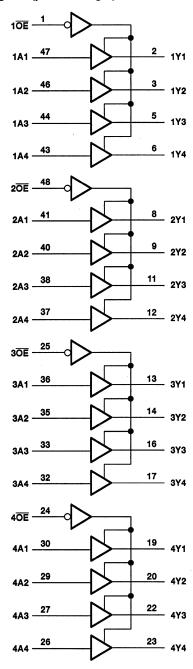
INP	JTS	OUTPUT
ŌĒ	Α	Y
L	Н	Н
L	L	L
н	Χ	Z

logic symbol†

10E 1 EN1		
48		
20E 25		
30E ————————————————————————————————————		
4 0E 24 EN4		
1A1 47 1 1 ∇	1	Y1
1A2 46	3	Y2
1A3 44	5	
43	6	Y3
1A4 41	8	Y4
2A1 1 2 ∇	9	Y1
2A2 38	11	Y2
2A3 37	12	Y3
2A4 36	13	Y4
3A1 35 1 3 ∇	14	Y1
3A2 33	—— 3 16	Y2
3A3 32	 3	SY3
3A4 30	——— 3 19	Y4
4A1		Y1
4A2 ————————————————————————————————————	4	Y2
4A3 27	22 4	ΥЗ
4A4 <u>26</u>	4	Y4

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVT162244, SN74LVT162244 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS258D - JUNE 1993 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .	
Current into any output in the low state, Io	
Current into any output in the high state, IO (see Note 2)	30 mA
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	
DL package	1.2 W
Storage temperature range, Teta	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			SN54LV	T162244	SN74LV	T162244	UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2	Zi.	2		٧
VIL	Low-level input voltage			⊘ 0.8		0.8	٧
VI	Input voltage			% 5.5		5.5	V
ЮН	High-level output current		\ \ \ \ \ \ \ \ \	〗−12		-12	mA
loL	Low-level output current		Ş	12		12	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	Š	10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SCBS258D - JUNE 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	AMETER TEST CONDITIONS			SN54LVT162244			SN7	UNIT			
PARAMETER				MIN	TYPT	MAX	MIN	TYPT	MAX	UNII	
VIK	V _{CC} = 2.7 V,	I _I = -18 mA				-1.2			-1.2	V	
Voн	V _{CC} = 3 V,	I _{OH} = - 12 mA		2			2			٧	
V _{OL}	V _{CC} = 3 V,	I _{OL} = 12 mA				0.8			0.8	٧	
	$V_{CC} = 0$ or MAX‡,	V _I = 5.5 V				10			10		
6.		V _I = V _{CC} or GND	Control pins			±1			±1		
lį	V _{CC} = 3.6 V	V _I = V _{CC}	Data ains			1			1	μА	
		V _I = 0	Data pins			<i>∰</i> −5			-5		
loff	V _{CC} = 0,	V _I or V _O = 0 to 4.5 V			<u> Q</u>	,			±100	μΑ	
1	V 0V	V _I = 0.8 V			75		75	75			
^I I(hold)	V _{CC} = 3 V	V _I = 2 V	A inputs	-75 Ç			–7 5			μА	
IOZH	V _{CC} = 3.6 V,	V _O = 3 V		Ś	Q"	5			5	μА	
lozL	V _{CC} = 3.6 V,	V _O = 0.5 V		S	*	-5			-5	μА	
			Outputs high			0.19		***	0.09		
Icc	V _{CC} = 3.6 V, V _I = V _{CC} or GND	$I_{O}=0$,	Outputs low			5			5	mA	
	AL = ACC OLGIND	Outputs disabled		Outputs disabled			0.19			0.09	
ΔlCC§	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC}	One input at V _{CC} – or GND	0.6 V,			0.2			0.2	mA	
Ci	V _I = 3 V or 0				4			4		pF	
Co	V _O = 3 V or 0				10			10		pF	

 $[\]dagger$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

					SN54LVT162244			SN74LVT162244				
PARAMETER	FROM (INPUT)			3.3 V 3 V	Vcc =	2.7 V	V	c = 3.3 ± 0.3 V	٧	V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
tPLH	Α		1.4	5.2	140	6.1	1.4	3.2	4.9		5.8	
t _{PHL}	_ ^	I	1.1	5.1	£9	6.3	1.1	3.1	5		6.1	ns
^t PZH	ŌĒ	V	1	6.6	ķ."	7.3	1	4.7	6.4		7.1	
t _{PZL}	UE UE	'	1.4	5.7		7.4	1.4	3.4	5.6		7.3	ns
^t PHZ	ŌĒ	_	2.6	. 05.9		7.6	2.6	4.5	6.6		7.3	
tPLZ		ľ	2.6	6.1		6.8	2.6	3.6	5.8		6.5	ns

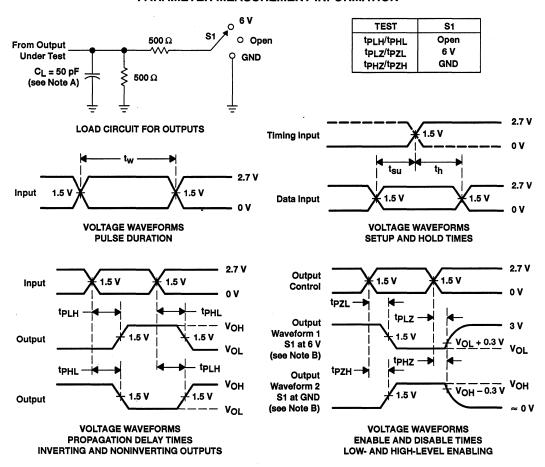
 $^{^{\}dagger}$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SCBS258D - JUNE 1993 - REVISED JULY 1995

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCBS143E - MAY 1992 - REVISED JANUARY 1996

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments
 Widebus™ Family
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Distributed V_{CC} and GND Pin Configuration
 Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes
 PCB Layout
- Packaged in Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVT16245A . . . WD PACKAGE SN74LVT16245A . . . DGG OR DL PACKAGE (TOP VIEW)

	_	_	_	1
1DIR[1	U		10E
1B1 [2] 1A1
1B2 [46	1A2
GND [4			GND
1B3 [1		44] 1A3
1B4 [1A4
v _{cc} [□ v _{cc}
1B5				1A5
1B6				1A6
GND [GND
1B7				1A7
1B8				1A8
2B1				2A1
2B2 [2A2
GND [GND
2B3 [2A3
2B4				2A4
v _{cc} [18		31	□ v _{cc}
2B5 [2A5
2B6	1			2A6
GND [GND
2B7				2A7
2B8				2A8
2DIR[24		25	20E
	L			

description

The 'LVT16245A are 16-bit (dual-octal) noninverting 3-state transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so that the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Widebus is a trademark of Texas Instruments Incorporated.

SCBS143E - MAY 1992 - REVISED JANUARY 1996

description (continued)

The SN74LVT16245A is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16245A is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT16245A is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 8-bit section)

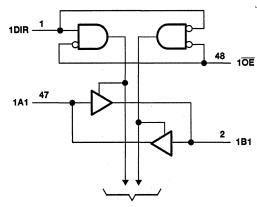
INP	UTS	OPERATION				
ŌĒ	DIR	OPERATION				
L	L	B data to A bus				
L	н	A data to B bus				
н	X	Isolation				

logic symbolt

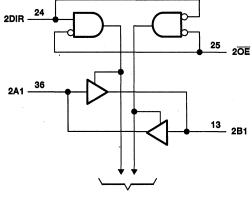
10E G3 1 1DIR 3 EN1 [BA] 3 EN2 [AB] G6 2OE 24 2DIR 6 EN4 [BA] 6 EN5 [AB] 1B1 1A1 ٥ Þ 2∇ 46 1A2 1**B**2 5 44 **1A3** 1**B**3 43 6 1**B**4 **1A4** 41 8 1A5 1**B**5 40 1A6 1**B**6 38 11 1A7 1**B**7 37 12 1A8 1**B**8 36 13 2A1 ۵ 2B1 5▽ 35 14 2A2 2B2 33 16 2A3 2B3 32 17 2B4 2A4 30 19 2A5 2B5 29 20 2A6 2**B**6 27 22 2A7 2B7 23 26 2A8 2B8

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels



To Seven Other Channels



SCBS143E - MAY 1992 - REVISED JANUARY 1996

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Input voltage range, V _I (see Note 1)	0.5 V to 7 V
Current into any output in the low state, IO: SN54LVT16245A	96 mA
Current into any output in the high state, IO (see Note 2): SN54LVT16245A	48 mA
SN74LVT16245A	64 mA
Input clamp current, $I_{ K }(V_1 < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): DGG package	0.85 W
DL package	1.2 W
Storage temperature range, Teta	-65°C to 150°C
	Supply voltage range, V_{CC} Input voltage range, V_{I} (see Note 1) Voltage range applied to any output in the high state or power-off state, V_{O} (see Note 1) Current into any output in the low state, I_{O} : SN54LVT16245A SN74LVT16245A Current into any output in the high state, I_{O} (see Note 2): SN54LVT16245A Input clamp current, I_{IK} ($V_{I} < 0$) Output clamp current, I_{OK} ($V_{O} < 0$) Maximum power dissipation at $T_{A} = 55^{\circ}$ C (in still air) (see Note 3): DGG package Storage temperature range, T_{Sto}

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and VO > VCC.

3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			SN54LV	T16245A	SN74LV	UNIT	
			MIN	MAX	MIN	MAX	UNII
V _{CC} Supply voltage				3.6	2.7	3.6	V
VIH	High-level input voltage				2		V
VIL	Low-level input voltage			0.8		0.8	٧
VI	Input voltage			5.5		5.5	V
ЮН	High-level output current			-24		-32	mA
lOL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SCBS143E - MAY 1992 - REVISED JANUARY 1996

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS				SN54LVT16245A			SN74LVT16245A			
PARAMETER	•	EST CONDITIONS		MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT	
VIK	V _{CC} = 2.7 V,	lj = -18 mA			-1.2			-1.2	٧		
	$V_{CC} = MIN \text{ to MAX}^{\ddagger},$	IOH = -100 μA	l _{OH} = -100 μA				VCC-C).2			
Vari	V _{CC} = 2.7 V,	IOH = - 8 mA		2.4			2.4			V	
VOH	V _{CC} = 3 V	IOH = - 24 mA		2						٧	
	VCC = 3 V	IOH = -32 mA				2					
	V _{CC} = 2.7 V	l _{OL} = 100 μA				0.2			0.2		
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5		
		I _{OL} = 16 mA				0.4			0.4	1 _v 1	
VOL	V 2V	I _{OL} = 32 mA			0.5	0.5			v		
	VCC = 3 V	I _{OL} = 48 mA	0.55								
		I _{OL} = 64 mA						0.55			
	V _{CC} = 3.6 V,	VI = VCC or GND	Control inputs			±1	,		±1.		
	V _{CC} = 0 or MAX [‡] ,	V _i = 5.5 V	Control inputs			10			-10		
lį		V _I = 5.5 V				100			20	μА	
	V _{CC} = 3.6 V	VI = VCC	A or B ports§	1				1			
	1	V _j = 0				-5			-5		
loff	V _{CC} = 0,	V _I or V _O = 0 to 4.5	V						±100	μΑ	
1		V _I = 0.8 V	A or B ports	75			75				
l(hold)	V _{CC} = 3 V	V _I = 2 V	A or B ports	-75			-75			μА	
lozh	$V_{CC} = 3.6 \text{ V},$	V _O = 3 V				5			1	μА	
lozL	$V_{CC} = 3.6 \text{ V},$	V _O = 0.5 V		i		-5			-1	μА	
			Outputs high			0.09			0.09		
Icc	V _{CC} = 3.6 V, V _I = V _{CC} or GND	$I_{O}=0,$	Outputs low		5				5	mA	
	11-10001010		Outputs disabled	0.09		0.09					
ΔICC¶	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND					0.2			0.2	mA	
Ci	V _I = 3 V or 0				4			4		pF	
Cio	V _O = 3 V or 0				11			11		pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ Unused pins at V_{CC} or GND
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

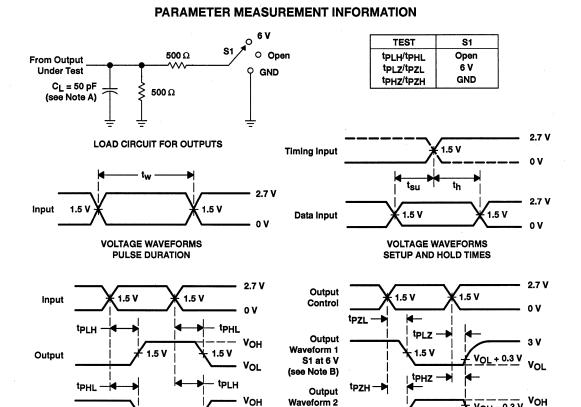
SN54LVT16245A, SN74LVT16245A 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS143E - MAY 1992 - REVISED JANUARY 1996

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

		TO (OUTPUT)	SN54LVT16245A			SN74LVT16245A						
PARAMETER	FROM (INPUT)		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
^t PLH	A or B	B or A	0.5	4.4		5.3	1	2.4	4.1		5	ns
t _{PHL}		BULA	0.5	4.7		5.5	1	2.3	4.1		5.2	113
t _{PZH}	ŌĒ	A or B	0.5	7		7.7	1	3	5.3		6.3	ns
tPZL	OE	Aorb	0.5	5.8		7.2	1	3.1	5.2		6.7	115
tPHZ	ŌĒ	A or B	1	7.2		7.7	2.7	4.6	6.4		7.2	
t _{PLZ}			1	6.3		6.5	2.6	4.3	5.8		6.1	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SCBS143E - MAY 1992 - REVISED JANUARY 1996



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES **INVERTING AND NONINVERTING OUTPUTS**

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

1.5 V

V_{OH} - 0.3 V

≈ 0 V

NOTES: A. C_L includes probe and jig capacitance.

Output

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

S1 at GND

(see Note B)

D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

Vон

VOL

1.5 V

SCBS260E - JUNE 1993 - REVISED NOVEMBER 1995

- A-Port Outputs Have Equivalent 22-Ω
 Series Resistors, So No External Resistors
 Are Required
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments Widebus™ Family
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes
 PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVT162245...WD PACKAGE SN74LVT162245...DGG OR DL PACKAGE (TOP VIEW)

		T 1		ì
1DIR[1	U	48] 10E
1B1 [2		47] 1A1
1B2 [3		46] 1A2
GND [4		45] GND
1B3 [] 1A3
1B4	6] 1A4
V _{CC} [] v _{cc}
1B5 [] 1A5
1B6				1A6
GND [GND
1B7] 1A7
1B8] 1A8
2B1				2A1
2B2 [2A2
GND [] GND
2B3 [] 2A3
2B4[] 2A4
V _{CC} [18			V _{CC}
2B5 [2A5
2B6 [2A6
GND [GND
2B7 [•			2A7
2B8	1			2A8
2DIR[24		25	20E

description

The 'LVT162245 are 16-bit (dual-octal) noninverting 3-state transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

The A-port outputs, which are designed to source or sink up to 8 mA, include 22-Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

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SCBS260E - JUNE 1993 - REVISED NOVEMBER 1995

description (continued)

The SN74LVT162245 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the input/output (I/O) pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT162245 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT162245 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 8-bit section)

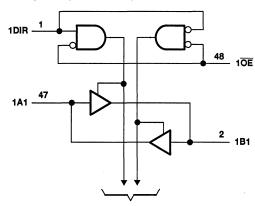
INP	UTS	ODERATION				
OE	DIR	OPERATION				
L	L	B data to A bus				
L	Н	A data to B bus				
н	X	Isolation				

logic symbol†

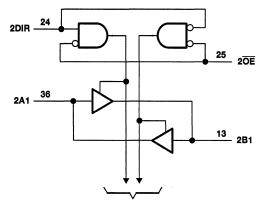
48 GЗ 10E 1 1DIR 3 EN1 [BA] 3 EN2 [AB] 25 2OE G6 24 2DIR 6 EN4 [BA] 6 EN5 [AB] **∇**1 1B1 ۵ \triangleright 2∇ 46 3 1A2 1**B**2 44 5 1**B**3 1A3 43 6 1**B**4 **1A4** 41 8 1**B**5 1A5 40 9 1A6 **1B6** 38 11 1A7 1**B**7 37 12 1A8 1**B**8 36 13 2A1 2B1 \triangleright 5∇ 35 14 2A2 2B2 33 16 2A3 2B3 32 17 2A4 2B4 30 19 2A5 2B5 29 20 2A6 2B6 27 22 2A7 2**B**7 26 2B8

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels



To Seven Other Channels

SCBS260E - JUNE 1993 - REVISED NOVEMBER 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} —0.5 V to 4.6 V Input voltage range, V _I (see Note 1) —0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1)0.5 V to 7 V
Current into any output in the low state, I _O : SN54LVT162245 (B port)
SN74LVT162245 (B port)
A port
Current into any output in the high state, Io (see Note 2): SN54LVT162245 (B port)
SN74LVT162245 (B port)
A port
Input clamp current, $I_{ K }(V_1 < 0)$
Output clamp current, $l_{OK}(V_O < 0)$ 50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package
DL package
Storage temperature range. Teta

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and VO > VCC.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			SN54LV	T162245	SN74LV	UNIT	
}			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage	2.7	3.6	2.7	3.6	٧	
VIH	High-level input voltage		2		2		٧
VIL	Low-level input voltage		0.8		0.8	٧	
VI	Input voltage			/5 :5		5.5	٧
	High-level output current	B port		ૂં≎24	-32		mA
ЮН	High-level output current	A port	1 3	ີງ −8		-8	, "IA
lai	Low level output ourrent	A port	ŞŠ	8		8	^
lOL	Low-level output current	B port	1	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	*	10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SCBS260E - JUNE 1993 - REVISED NOVEMBER 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			SN54LVT162245			SN74LVT162245			UNIT	
		. I O O O O O O O O O O O O O O O O O O				TYP	MAX	MIN	TYPT	MAX	ONI	
٧ _{IK}		$V_{CC} = 2.7 \text{ V},$	l _l = -18 mA				-1.2			-1.2	٧	
	A port	V _{CC} = 3 V,	I _{OH} = -8 mA		2			2				
		V _{CC} = MIN to MAX‡,	IOH = -100 μA	VCC-C).2		VCC-0	.2				
Vон	B port	V _{CC} = 2.7 V,	IOH = - 8 mA	I _{OH} = – 8 mA				2.4			٧	
	B port	V _{CC} = 3 V	Ιου = - 24 mΔ		2							
		ACC = 2 A	$I_{OH} = -32 \text{ mA}$					2				
	A port	V _{CC} = 3 V,	I _{OL} = 8 mA	I _{OL} = 8 mA			0.8			0.8		
		V _{CC} = 2.7 V	l _{OL} = 100 μA				0.2			0.2		
		VCC = 2.7 V	I _{OL} = 24 mA			0.5			0.5			
VOL	B port		I _{OL} = 16 mA			0.4			0.4	٧		
S port	V _{CC} = 3 V	$I_{OL} = 32 \text{ mA}$		-	0.5			0.5				
		1,000-0,4	I _{OL} = 48 mA				0.55				-	
			I _{OL} = 64 mA			42.			0.55			
	Control pins	V _{CC} = 3.6 V,	V _I = V _{CC} or GI	ND	<u> </u>	کہ	¥ ±1			±1		
I _I	Control pins	$V_{CC} = 0$ or MAX^{\ddagger} ,	[‡] , V _I = 5.5 V				10			10		
	1		V _I = 5.5 V		<u> </u>	<u> </u>	20			20	μΑ	
	A or B ports	V _{CC} = 3.6 V	VI = VCC		· .	3	5			5		
			V _I = 0			3"	-10			-10		
loff		$V_{CC} = 0$,	V_I or $V_O = 0$ to	4.5 V	Q*					±100	μΑ	
		V _{CC} = 3 V			75			75				
I(hold)	A or B ports	VCC-0 V	V _I = 2 V	V _I = 2 V				-75			μА	
	1	$V_{CC} = 3.6 \text{ V},$	V _I = 0 to 3.6 V		<u> </u>		±500			±500		
lozh		V _{CC} = 3.6 V,	V _O = 3 V		<u> </u>		1			1	μA	
lozl		$V_{CC} = 3.6 \text{ V},$	V _O = 0.5 V				-1			-1	μΑ	
				Outputs high			0.09			0.09		
		V _{CC} = 3.6 V,	$I_{O}=0$,	Outputs low	<u> </u>	5			5	mA		
		V _I = V _{CC} or GND		Outputs disabled			0.09			0.09	,,,,,	
$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6$ Other inputs at V_{CC} or GND		CC - 0.6 V,			0.2			0.2	mA			
Ci		V _I = 3 V or 0				4			4		pF	
C _{io} V _O = 3 V or 0			10.5			10.5		pF				

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

 $[\]S$ This is the increase in supply current for each input that is at the specified TTL voltage level rather than \bar{V}_{CC} or GND.

SCBS260E - JUNE 1993 - REVISED NOVEMBER 1995

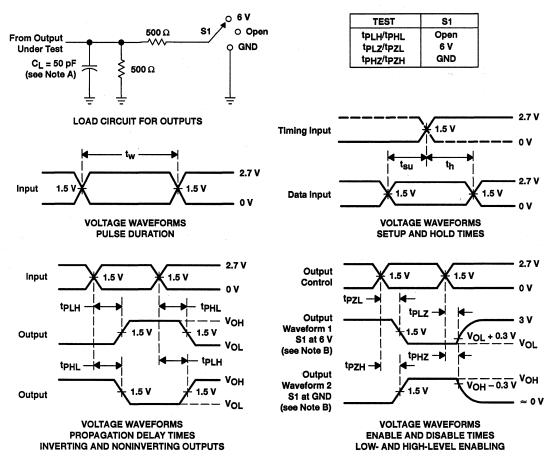
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

		TO (OUTPUT)		SN54LV	T162245			SN7	4LVT162	245			
PARAMETER	FROM (INPUT)		V _{CC} =		V _{CC} =	2.7 V		± 0.3 V	V	V _{CC} =	2.7 V	UNIT	
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX		
^t PLH	Α	В	1	4.3		5.2	1	2.4	4.1		5	ne	
t _{PHL}	*		1	4.3		5.3	1	2.3	4.1		5.2	ns	
t _{PLH}	В	Α	2	5.7		7.1	2	3.5	5.5		6.9	ns	
t _{PHL}	В	^	1.9	4.8	ŢĠ,	5.7	1.9	3.3	4.7		5.6	113	
^t PZH	OF.	ŌĒ	В	1	5.5	Li'	6.9	1	3	5.3		6.8	ns
^t PZL	OE L		1	5.4,	Z.,	6.8	1	3.1	5.2		6.7	115	
^t PZH	ŌĒ	Α	2.3	7.5		9.6	2.3	4.5	7.2		9.4		
^t PZL	OE	_ ^	2.4	,6 79		8.4	2.4	4.1	6.6		8.2	ns	
^t PHZ	ŌĒ	В	2.7	€6.7		7.4	2.7	4.6	6.4		7.2		
tPLZ	OE .		2.6	6		6.3	2.6	4.3	5.8		6.1	ns	
^t PHZ	ŌĒ	^	3.3	7.6		8.3	3.3	5	7.3		8		
^t PLZ	OE .	Α Α	3.4	6.9		7.5	3.4	5	6.7		7.1	ns	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SCBS260E - JUNE 1993 - REVISED NOVEMBER 1995

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_f ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVT16373, SN74LVT16373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS144E - MAY 1992 - REVISED JANUARY 1996

State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V	SN54LVT16373 WD PACKAGE SN74LVT16373 DGG OR DL PACKAGE (TOP VIEW)
Operation and Low-Static Power Dissipation	10E 1 48 1LE
 Members of the Texas Instruments Widebus™ Family 	1Q1
 Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC}) 	GND 04 45 GND 1Q3 05 44 1 1D3
Support Unregulated Battery Operation Down to 2.7 V	1Q4 0 6 43 1D4 V _{CC} 0 7 42 V _{CC}
 Typical V_{OLP} (Output Ground Bounce) 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1Q5 0 8 41 1 1D5 1Q6 0 9 40 1 1D6
 ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model 	GND 1 ₁₀ 39 GND 1Q7 1 11 38 1D7 1Q8 1 12 37 1D8
(C = 200 pF, R = 0) ■ Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17	2Q1
 Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors 	2Q3 [] 16 33 [] 2D3 2Q4 [] 17 32 [] 2D4 V _{CC} [] 18 31 [] V _{CC}
Support Live Insertion	2Q5 🛛 19 30 🗍 2D5
 Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise 	2Q6 [] 20 29 [] 2D6 GND [] 21 28 [] GND
 Flow-Through Architecture Optimizes PCB Layout 	2Q7 [] 22 27 [] 2D7 2Q8 [] 23 26 [] 2D8
 Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings 	2 0E [[24 25]] 2LE

description

The 'LVT16373 are 16-bit transparent D-type latches with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

OE does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

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SN54LVT16373, SN74LVT16373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS144E - MAY 1992 - REVISED JANUARY 1996

description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16373 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16373 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT16373 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 8-bit section)

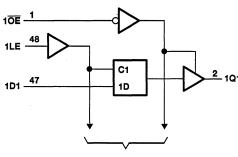
	•					
	INPUTS	OUTPUT				
ŌĒ	LE	D	Q			
L	Н	Н	Н			
L	Н	L	L			
L	L	Х	Q ₀			
Н	X	Х	z			

logic symbol†

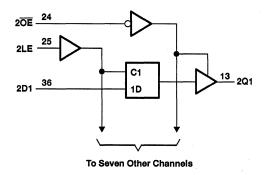
10E 1EN 48 1LE СЗ 24 20E 2EN 25 2LE C4 47 2 1D1 3D 1Q1 1∇ 3 46 1D2 1Q2 5 44 1D3 1Q3 43 6 1Q4 1D4 41 8 1D5 1Q5 40 9 1D6 1Q6 38 11 1D7 **1Q7** 37 12 1D8 1Q8 36 13 2D1 4D 2∇ 2Q1 35 14 2D2 2Q2 33 16 2D3 2Q3 32 17 2D4 2Q4 30 19 2D5 2Q5 29 20 2D6 2Q6 27 22 2D7 2Q7 26 23 2D8 2Q8

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels



SN54LVT16373, SN74LVT16373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS144E - MAY 1992 - REVISED JANUARY 1996

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, VO (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, IO: SN54LVT16373	96 mA
SN74LVT16373	128 mA
Current into any output in the high state, IO (see Note 2): SN54LVT16373	48 mA
SN74LVT16373	64 mA
Input clamp current, I _{IK} (V _I < 0)	50 mA
Output clamp current, I _{OK} (V _O < 0)	50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	0.85 W
DL package	1.2 W
Storage temperature range, T _{stq} – (65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and VO > VCC.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			SN54LV		SN74LVT16373		UNIT
			MIN	MAX	MIN	MAX	ONII
VCC	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage		2		2		٧
VIL	Low-level input voltage			0.8		0.8	٧
VI	Input voltage			5.5		5.5	٧
ЮН	High-level output current			-24		-32	mA
lOL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		∸55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SCBS144E - MAY 1992 - REVISED JANUARY 1996

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		7507.00	ONDITIONS	SN	54LVT16	373	SN7	4LVT16	373	UNIT		
,	ARAMETER	IESI C	ONDITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	UNII		
VIK		V _{CC} = 2.7 V,	I _I = -18 mA			-1.2			-1.2	٧		
		V _{CC} = MIN to MAX [‡] ,	I _{OH} = -100 μA	Vcc-0).2		VCC-C).2				
V		V _{CC} = 2.7 V,	I _{OH} = – 8 mA	2.4			2.4			v		
VOH		V _{CC} = 3 V	IOH = - 24 mA	2						٧		
		ACC = 2 A	I _{OH} = -32 mA				2					
		V _{CC} = 2.7 V	I _{OL} = 100 μA			0.2			0.2			
		VCC = 2.7 V	I _{OL} = 24 mA			0.5			0.5			
V			I _{OL} = 16 mA			0.4			0.4	V		
VOL		V _{CC} = 3 V	I _{OL} = 32 mA			0.5			0.5	v		
		VCC = 3 V	IOL = 48 mA			0.55						
			I _{OL} = 64 mA						0.55	İ		
		V _{CC} = 0 or MAX [‡] ,	V _I = 5.5 V			40			10			
1.	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND			±1			±1	μА		
Ŋ	Data insute	V 00V	VI = VCC			1			1	μΑ		
	Data inputs	V _{CC} = 3.6 V	V _I = 0			-5			-5			
loff		V _{CC} = 0,	V _I or V _O = 0 to 4.5 V			±100			±100	μА		
1	Data innute	Vac. 2.V	V _I = 0.8 V	75			75					
l(hold)	Data inputs	V _{CC} = 3 V	V _I = 2 V	-75			-75			μА		
lozh		V _{CC} = 3.6 V,	V _O = 3 V			5			5	μΑ		
lozL		V _{CC} = 3.6 V,	V _O = 0.5 V			-5			-5	μА		
	Outputs high					0.09			0.09			
Icc	Outputs low $V_{CC} = 3.6 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$		$I_{O}=0$,			5			5	mA		
Outputs disabled		A AL = ACC OL GIAD				0.09			0.09	1 1		
ΔlCC§		$V_{CC} = 3 \text{ V to } 3.6 \text{ V},$ One input at $V_{CC} = 0.0$ Other inputs at $V_{CC} = 0.0$				0.2			0.2	mA		
Ci		V _I = 3 V or 0			5			5		pF		
Со		V _O = 3 V or 0			9.5			9.5		pF		

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54LVT16373			SN74LVT16373				
		V _{CC} = ± 0.	3.3 V 3 V	V _{CC} =	2.7 V	V _{CC} =	: 3.3 V .3 V	V _{CC} =	2.7 V	UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _W	Pulse duration, LE high	3.3		3.3		3.3		3.3		ns
t _{su}	Setup time, data before LE↓	1		1		0.5		0.5		ns
th	Hold time, data after LE↓	2.6		2.9		1.8		2		ns

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than \tilde{V}_{CC} or GND.

SCBS144E - MAY 1992 - REVISED JANUARY 1996

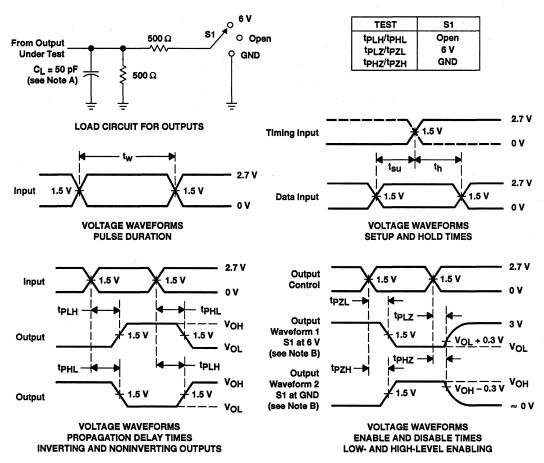
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

				SN54LV			SN74LVT16373					
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =	2.7 V		cc = 3.3 ± 0.3 V	٧	V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
tPLH	D	q	0.5	5.1		5.8	1.3	2.7	5		5.7	ns
tPHL		ď	0.5	5		5.8	1.4	2.9	4.9		5.7	113
t _{PLH}	LE	Q	1	6.8		7.3	2.1	3.6	6		6.8	ns
t _{PHL}	LE	y	1	7.8		8.9	3	4.7	6.9		8.8	115
t _{PZH}	ŌĒ	Q	0.5	5.6		6.4	1	2.9	5.3		6.3	
tPZL	OE .	ď	0.5	5.5		6	1.3	3	5.1		5.9	ns
tPHZ	ŌĒ	Q	1	7.2		8	2.7	4.3	6.8		7.6	200
tPLZ	OE .	.	1	6.1		6.2	2.6	4	5.8		5.9	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SCBS144E - MAY 1992 - REVISED JANUARY 1996





NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_f ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCBS261D - JULY 1993 - REVISED NOVEMBER 1995

	$^{\circ}$ Output Ports Have Equivalent 22- Ω Serie:
	Resistors, So No External Resistors Are
	Required
•	State-of-the-Art Advanced BiCMOS
	Technology (ART) Design for 3.3-V

- **Operation and Low-Static Power** Dissipation
- Members of the Texas Instruments Widebus™ Family
- Support Mixed-Mode Signal Operation (5-V) Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes **PCB Layout**
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package **Using 25-mil Center-to-Center Spacings**

SN54LVT162373 . . . WD PACKAGE SN74LVT162373... DGG OR DL PACKAGE (TOP VIEW)

	_	_		١
10E [1	U	48	1LE
1Q1 [2		47] 1D1
1Q2 [3		46	1D2
GND [45] GND
1Q3 [44] 1D3
1Q4 [43] 1D4
V _{CC}			42] v _{cc}
1Q5 [41] 1D5
1Q6 [] 1D6
GND [39	GND
1Q7 [38] 1D7
1Q8 [] 1D8
2Q1	13			2D1
2Q2				2D2
GND [] GND
2Q3 [] 2D3
2Q4 [32	2D4
v _{cc} [18		31	V _{CC}
2Q5			30	2D5
2Q6 [_			2D6
GND				GND
2Q7	3			2D7
2Q8	_			2D8
20E	24		25	J 2LE

description

The 'LVT162373 are 16-bit transparent D-type latches with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 'LVT162373 can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

Widebus is a trademark of Texas Instruments Incorporated



SCBS261D - JULY 1993 - REVISED NOVEMBER 1995

description (continued)

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

OE does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include $22-\Omega$ series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT162373 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT162373 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT162373 is characterized for operation from -40°C to 85°C.

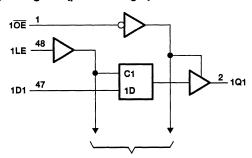
FUNCTION TABLE (each 8-bit section)

	INPUTS	OUTPUT	
ŌĒ	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Х	Q ₀
н	Х	Х	z

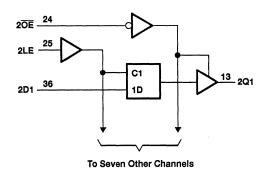
SCBS261D - JULY 1993 - REVISED NOVEMBER 1995

logic	symbol†			
	1			
10E	48	1EN		
1LE	24	СЗ		
2OE	25	2EN		
2LE		C4		
	47	<u> </u>	2	404
1D1	46	3D 1∇	3	1Q1
1D2	44		5	1Q2
1D3	43		6	1Q3
1D4	41		8	1Q4
1D5	40		9	105
1D6	38		11	1Q6
1D7	37		12	1Q7
1D8	36		13	1Q8
2D1	35	4D 2▽	14	2Q1
2D2	33		16	2Q2
2D3	32		17	2Q3
2D4	30	 	19	2Q4
2D5	29		20	2Q5
2D6	27		22	2Q6
2D7	26		23	2Q7
2D8		1		2Q8

logic diagram (positive logic)



To Seven Other Channels



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	-0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo (see Note 1)	0.5 V to 7 V
Current into any output in the low state, IO	30 mA
Current into any output in the high state, IO (see Note 2)	30 mA
Input clamp current, $I_{IK}(V_1 < 0)$	
Output clamp current, I _{OK} (V _O < 0)	50 mA
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): DGG package	0.85 W
DL package	1.2 W
Storage temperature range. Teta	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and $V_O > V_{CC}$.



[†] This symbol is in accordance with ANSI/JEEE Std 91-1984 and IEC Publication 617-12.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

SCBS261D - JULY 1993 - REVISED NOVEMBER 1995

recommended operating conditions (see Note 4)

			SN54LV	T162373	SN74LV	UNIT	
			MIN	MAX	MIN	MAX	UNIT
V _{CC} Supply voltage			2.7	3.6	2.7	3.6	٧
VIH	IH High-level input voltage				2		٧
VIL	Low-level input voltage			0.8		0.8	٧
Vi	Input voltage			5.5		5.5	٧
ЮН	High-level output current			-12		-12	mA
lOL	Low-level output current			12		12	mA
Δt/Δν	Input transition rise or fall rate Outputs enabled			10		10	ns/V
TA	Operating free-air temperature			125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED		TEST COMPLETIONS	-	SN54LV	Γ162373	SN74LV	Г162373	LINUT	
PARAMETER		TEST CONDITIONS	TEST CONDITIONS		MAX	MIN	MAX	UNIT	
VIK	V _{CC} = 2.7 V,	l _l = −18 mA	I _I = -18 mA		-1.2		-1.2	٧	
Voн	V _{CC} = 3 V,	I _{OH} = - 12 mA		2		2		٧	
VOL	V _{CC} = 3 V,	I _{OL} = 12 mA			0.8		0.8	٧	
	$V_{CC} = 0$ or MAX^{\dagger} ,	V _I = 5.5 V			10		10		
I.	,	V _I = V _{CC} or GND	V _I = V _{CC} or GND Control pins		±1		±1		
lį	V _{CC} = 3.6 V	V _I = V _{CC}	Data sina		1		1	μΑ	
		V ₁ = 0	Data pins		-5		-5	1	
loff	$V_{CC} = 0$,	V _I or V _O = 0 to 4.5 V	V _I or V _O = 0 to 4.5 V				±100	μА	
la	V 2V	V _I = 0.8 V	A innute	75	75				
l(hold)	V _{CC} = 3 V	V _I = 2 V	A inputs	-75		-75		μА	
lozh	V _{CC} = 3.6 V,	V _O = 3 V			1		1	μА	
lozL	V _{CC} = 3.6 V,	V _O = 0.5 V			-1		-1	μА	
			Outputs high		0.19		0.1		
Icc	V _{CC} = 3.6 V, V _I = V _{CC} or GND	$I_{O}=0$,	Outputs low		5		5	mA	
	AL = ACC OL GIAD		Outputs disabled		0.19		0.1	1	
∆lCC [‡]	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC}	/, One input at V _{CC} – 0.6 V, _C or GND			0.2		0.2	mA	
Ci	V _I = 3 V or 0			_			pF		
Co	V _O = 3 V or 0			1				pF	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SCBS145E - MAY 1992 - REVISED JANUARY 1996

 State-of-the-Art Advanced BiCMOS 		374 WD	
Technology (ABT) Design for 3.3-V	SN74LVT16374	DGG OI (TOP VIEW)	R DL PACKAGE
Operation and Low-Static Power		(,	ı
Dissipation	10E [$_{1}$ \cup $_{48}$] 1CLK
Members of the Texas Instruments	1Q1 [2 47	1D1
<i>Widebus</i> ™ Family	1Q2 [] 1D2
 Support Mixed-Mode Signal Operation (5-V 	GND [4 45] GND
Input and Output Voltages With 3.3-V V _{CC})	1Q3 [5 44] 1D3
 Support Unregulated Battery Operation 	1Q4 [] 1D4
Down to 2.7 V	v _{cc} [7 42] v _{cc}
 Typical V_{OLP} (Output Ground Bounce) 	1Q5 L	8 41	1D5
< 0.8 V at V_{CC} = 3.3 V, T_A = 25°C	1Q6 [9 40	1D6
 ESD Protection Exceeds 2000 V Per 	GND [GND
MIL-STD-883C, Method 3015; Exceeds	1Q7 [1D7
200 V Using Machine Model	1Q8 [1D8
(C = 200 pF, R = 0)	2Q1 [2D1
 Latch-Up Performance Exceeds 500 mA 	202		2D2
Per JEDEC Standard JESD-17	GND [GND
Bus-Hold Data Inputs Eliminate the Need	2Q3 [2D3
for External Pullup Resistors	2Q4 [2D4
Support Live Insertion	V _{CC} [2Q5 [10 31] V _{CC}] 2D5
Distributed V _{CC} and GND Pin Configuration	2Q6 [2D5 2D6
Minimizes High-Speed Switching Noise	GND [GND
• .	2Q7 [2D7
Flow-Through Architecture Optimizes PCB Leveut	2Q8 [2D8
PCB Layout	2 0E [2CLK
Package Options Include Plastic 300-mil Challes County Options (DL) and This Obtains	2021	<u> </u>	
Shrink Small-Outline (DL) and Thin Shrink			
Small-Outline (DGG) Packages and 380-mil			

description

The 'LVT16374 are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Widebus is a trademark of Texas Instruments Incorporated.

Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings



SCBS145E - MAY 1992 - REVISED JANUARY 1996

description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16374 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16374 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT16374 is characterized for operation from -40°C to 85°C.

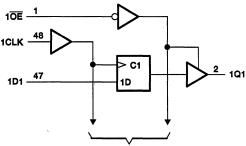
FUNCTION TABLE (each flip-flop)

	INPUTS	OUTPUT	
OE	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	H or L	X	Q ₀
Н	Х	Х	z

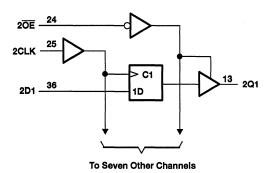
logic symbol†

10E 1EN 48 1CLK C1 24 2OE 2EN 25 C2 2CLK 47 2 1D 1 🗸 1D1 1Q1 46 3 1D2 1Q2 5 44 1D3 1Q3 43 6 1D4 1Q4 41 8 1D5 1Q5 40 9 1D6 1Q6 38 11 1D7 1Q7 37 12 1D8 1Q8 36 13 2D1 2D 2 ▽ 2Q1 35 14 2D2 2Q2 33 16 2D3 2Q3 32 17 2D4 2Q4 30 19 2D5 2Q5 29 20 2D6 2Q6 27 22 2D7 2Q7 26 23 2D8 208

logic diagram (positive logic)



To Seven Other Channels



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



SCBS145E - MAY 1992 - REVISED JANUARY 1996

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1)	
Current into any output in the low state, IO: SN54LVT16374	96 mA
SN74LVT16374	128 mA
Current into any output in the high state, I _O (see Note 2): SN54LVT16374	48 mA
SN74LVT16374	64 mA
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	
DL package	1.2 W
Storage temperature range, T _{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current flows only when the output is in the high state and VO > VCC.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

					SN74LVT16374		UNIT
			MIN	MAX	MIN	MAX	CINIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2		2		٧
VIL	Low-level input voltage			0.8		0.8	٧
VĮ	Input voltage			5.5		5.5	٧
ЮН	High-level output current			-24		-32	mA
lOL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SCBS145E - MAY 1992 - REVISED JANUARY 1996

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

_		7707.04	011DITIONS	SNS	4LVT16	374	SN7	4LVT16	374		
Р	ARAMETER	IESI CO	ONDITIONS	MIN	TYP	MAX	MIN	TYPT	MAX	UNIT	
VIK		$V_{CC} = 2.7 \text{ V},$	I _I = -18 mA			-1.2			-1.2	٧	
	•	V _{CC} = MIN to MAX [‡] ,	I _{OH} = -100 μA	Vcc-0).2		VCC-0	.2			
V		V _{CC} = 2.7 V,	I _{OH} = - 8 mA	2.4	,		2.4			v	
VOH		V 0V	I _{OH} = - 24 mA	2						v	
		V _{CC} = 3 V	I _{OH} = -32 mA				2				
		V 07V	I _{OL} = 100 μA		4	0.2			0.2		
		V _{CC} = 2.7 V	I _{OL} = 24 mA			0.5			0.5		
V			I _{OL} = 16 mA			0.4			0.4	V	
VOL		Vac. 2.V	I _{OL} = 32 mA			0.5			0.5	V	
		V _{CC} = 3 V	I _{OL} = 48 mA			0.55					
			IOL = 64 mA						0.55		
		$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V			10			10		
1.	Control inputs	V _{CC} = 3.6 V,	VI = VCC or GND			±1			±1	μА	
l _l	Data innuts	V _{CC} = 3.6 V	VI = VCC			1			1		
•	Data inputs	ACC = 2.0 A	V _I = 0			-5			-5		
loff		$V_{CC} = 0$,	V_{I} or $V_{O} = 0$ to 4.5 V			±100			±100	μА	
lia in	Data inputs	Vac. 2 V	V _I = 0.8 V	75			75			^	
I(hold)	Data Inputs	VCC = 3 V	V _I = 2 V	-75			-75			μА	
lozh		V _{CC} = 3.6 V,	V _O = 2.7 V			5			5	μА	
lozL		V _{CC} = 3.6 V,	V _O = 0.5 V			-5			-5	μΑ	
	Outputs high					0.1			0.1		
Icc	Outputs low	V _{CC} = 3.6 V, V _I = V _{CC} or GND	$I_{O}=0$,			5			5	mA	
	Outputs disabled	AL = ACC OLGIND			.,,,	0.1			0.1		
ΔICC§		V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.0 Other inputs at V _{CC} or				0.2			0.2	mA	
Ci		V _I = 3 V or 0			5			5		pF	
Co	:	V _O = 3 V or 0			9.5			9.5		pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				SN54LV	T16374			SN74LV	T16374		
			V _{CC} =		V _{CC} =	2.7 V	VCC =		V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	150	0	150	0	150	0	150	MHz
t _W	Pulse duration, CLK high or low		3.3		3.3		3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	High or low	2.8		3.3		2.2		2.6		ns
th	Hold time, data after CLK↑	High or low	0.6		0.5		0.6		0		ns



[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54LVT16374, SN74LVT16374 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS SCBS145E - MAY 1992 - REVISED JANUARY 1996

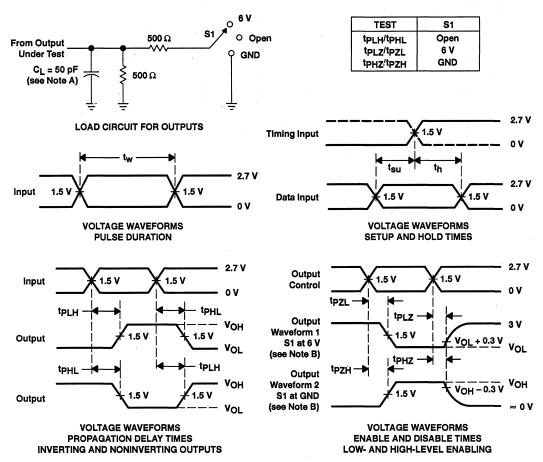
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

	SN54LVT16374				SN74LVT16374							
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _C C = ± 0.		V _{CC} =	2.7 V		CC = 3.3 ± 0.3 V	V	V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	TYPŤ	MAX	MIN	MAX	
fmax			150		150		150			150		MHz
^t PLH	CLK	Q	1.9	6.6		7.4	1.9	3.6	6.3		7	ns
^t PHL	OLK	<u> </u>	2.3	6.9		7.5	2.3	4.1	6.6		7.2	113
^t PZH	ŌĒ	Q	1	5.6		6.4	1	2.7	5.3		6.3	
[†] PZL) OE	<u> </u>	1.3	5.3		6	1.3	2.8	5.1		5.9	ns
t _{PHZ}	ŌĒ	Q	1	7.2		8.2	2.7	4.3	6.8		7.6	ns
^t PLZ	02	ų ,	2.6	6.1		8.2	2.6	3.9	5.8		5.9	115

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SCBS145E - MAY 1992 - REVISED JANUARY 1996

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCBS262C - JULY 1993 - REVISED JULY 1995

 Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required 	SN54LVT162374 WD PACKAGE SN74LVT162374 DGG OR DL PACKAGE (TOP VIEW)
 State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation 	1OE 1 48 1CLK 1Q1 2 47 1D1 1Q2 3 46 1D2
 Members of the Texas Instruments Widebus™ Family 	GND
 Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC}) 	V _{CC}
 Support Unregulated Battery Operation Down to 2.7 V 	1Q6 []9 40 [] 1D6 GND [] 10 39 [] GND
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1Q7 [] 11 38 [] 1D7 1Q8 [] 12 37 [] 1D8 2Q1 [] 13 36 [] 2D1
 ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0) 	2Q2
Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17	2Q4 [] 17 32 [] 2D4 V _{CC} [] 18 31 [] V _{CC} 2Q5 [] 19 30 [] 2D5
 Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors 	2Q6
 Support Live Insertion Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise 	2Q7
Flow-Through Architecture Optimizes PCB Layout	1
 Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package 	

description

The 'LVT162374 are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 'LVT162374 can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the D inputs.

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Using 25-mil Center-to-Center Spacings



SCBS262C - JULY 1993 - REVISED JULY 1995

description (continued)

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include $22-\Omega$ series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT162374 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT162374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT162374 is characterized for operation from –40°C to 85°C.

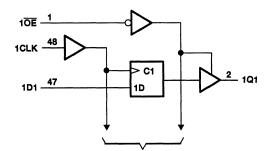
FUNCTION TABLE (each flip-flop)

	INPUTS	OUTPUT	
OE	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	L	Х	Q ₀
Н	X	Х	Z

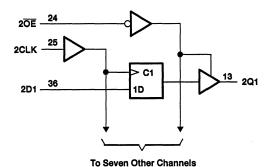
SCBS262C - JULY 1993 - REVISED JULY 1995

logic symbol[†] 10E 1EN 48 1CLK - C1 24 2OE 2EN 25 2CLK 47 1D1 1D 1Q1 1 V 46 3 1Q2 1D2 44 5 1Q3 1D3 43 6 1Q4 1D4 41 8 1D5 1Q5 9 40 1D6 **1Q6** 38 11 1D7 1Q7 37 12 1Q8 1D8 13 36 2D1 2D 2 ▽ 2Q1 35 14 2Q2 2D2 33 16 2D3 2Q3 32 17 2D4 2Q4 19 30 2D5 2Q5 29 20 2Q6 2D6 27 22 2Q7 2D7 26 23 2D8 2Q8

logic diagram (positive logic)



To Seven Other Channels



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Current into any output in the low state, Io	
Current into any output in the high state, IO (see Note 2)	30 mA
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): DGG package	0.85 W
DL package	
Storage temperature range, T _{stg}	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current flows only when the output is in the high state and VO > VCC.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SCBS262C - JULY 1993 - REVISED JULY 1995

recommended operating conditions (see Note 4)

					SN74LV	UNIT	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage		2		2		٧
VIL	Low-level input voltage			0.8		0.8	٧
VI	Input voltage			5.5		5.5	٧
ЮН	High-level output current			-12		-12	mA
loL	Low-level output current			12		12	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED		TEST COMPLETONS	·	SN54LV	T162374	SN74LV	T162374	UNIT
PARAMETER	·	TEST CONDITIONS	MIN	MAX	MIN	MAX	CIVIT	
VIK	$V_{CC} = 2.7 \text{ V},$	l _l = −18 mA			-1.2		-1.2	٧
VOH	V _{CC} = 3 V,	I _{OH} = - 12 mA		2		2		V
VOL	V _{CC} = 3 V,	I _{OL} = 12 mA			0.8		0.8	V
	V _{CC} = 0 or MAX [†] ,	V _I = 5.5 V			10		10	
1.		V _I = V _{CC} or GND	Control inputs		±1		±1	
lį	V _{CC} = 3.6 V	V _I = V _{CC}	Data insute		1		1	μА
		V _I = 0	Data inputs		. –5		-5]
loff	$V_{CC} = 0$,	V _I or V _O = 0 to 4.5 V					±100	μА
1	V 0V	V _I = 0.8 V	A :	75		75		
l(hold)	V _{CC} = 3 V	V _I = 2 V A inputs		-75		-75		μА
lozh	V _{CC} = 3.6 V,	V _O = 3 V			1		1	μА
^l OZL	V _{CC} = 3.6 V,	V _O = 0.5 V			-1		-1	μА
			Outputs high		0.19		0.1	
lcc	V _{CC} = 3.6 V, V _I = V _{CC} or GND	$I_{O}=0$,	Outputs low		5		5	mA
	AL = ACC OLGIAD		Outputs disabled		0.19		0.1	
Δl _{CC} ‡	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC}	One input at $V_{CC} = 0$. or GND	6 V,		0.2		0.2	mA
C _i	V _I = 3 V or 0							pF
Co	V _O = 3 V or 0							pF

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SCBS146C - MAY 1992 - REVISED JULY 1995

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V **Operation and Low-Static Power** Dissipation
- **Members of the Texas Instruments** Widebus™ Family
- Support Mixed-Mode Signal Operation (5-V) Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- UBT™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Typical V_{OLP} (Output Ground Bounce) $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes **PCB Layout**
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package **Using 25-mil Center-to-Center Spacings**

SN54LVT16500 . . . WD PACKAGE SN74LVT16500 . . . DGG OR DL PACKAGE (TOP VIEW)

		_	
OEAB	1	56	GND
LEAB [2	55	CLKAB
A1 [3	54	B1
GND [4	53	GND
A2 [52	B2
АЗ [51	B3
v _{cc} [7	50	V _{CC}
A4 🛛	8	49	B4
A5 🛚	9	48	B5
A6 [47	
GND [46	GND
A7 [45	B7
A8 [13	44]	B8
A9 🛛			B9
A10 [15		B10
A11 [16	41	B11
A12 🛛	17	40	B12
GND [GND
A13 🛛	19	38]	B13
A14 [20	37	B14
A15 🛛	ı	36	
v _{cc} [22	35	V _{CC}
A16 🛛			B16
A17 🛚			B17
GND [32	
A18 🛛			B18
OEBA [30	CLKBA
LEBA [28	29	GND
`			

description

The 'LVT16500 are 18-bit universal bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output-enable OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

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SCBS146C - MAY 1992 - REVISED JULY 1995

description (continued)

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and OEBA is active low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74LVT16500 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16500 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT16500 is characterized for operation from -40°C to 85°C.

FUNCTION TABLET

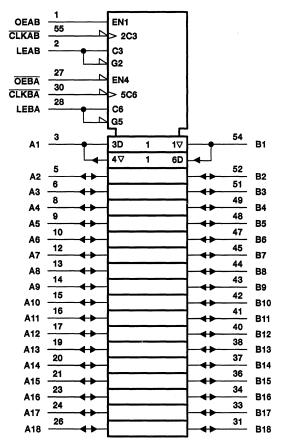
	INPUTS						
OEAB	LEAB	CLKAB	Α	В			
L	Х	Х	Х	Z			
Н	Н	X	L	L			
н	Н	X	Н	н .			
н	L	1	L	L			
н	L	\downarrow	Н	Н			
н	L	Н	X	в ₀ ‡ в ₀ §			
Н	L	L	X	B ₀ §			

[†] A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

[‡]Output level before the indicated steady-state input conditions were established

[§] Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

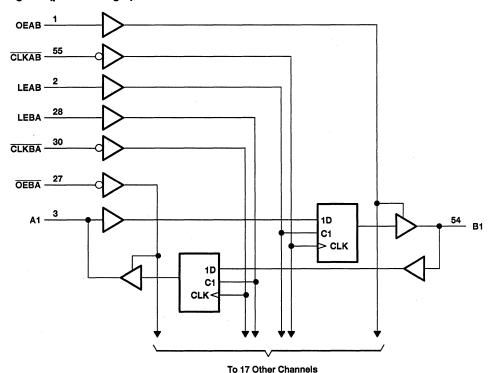
logic symbolt



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} 0.5 V	
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1)0.5 \	/ to 7 V
Current into any output in the low state, Io: SN54LVT16500	96 mA
SN74LVT16500	128 mA
Current into any output in the high state, I _O (see Note 2): SN54LVT16500	48 mA
SN74LVT16500	64 mA
Input clamp current, I _{IK} (V _I < 0)	-50 mA
Output clamp current, I_{OK} (V _O < 0)	-50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	
DL package	. 1.4 W
Storage temperature range, T _{stq} –65°C to	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and VO > VCC.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.



SN54LVT16500, SN74LVT16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS146C - MAY 1992 - REVISED JULY 1995

recommended operating conditions (see Note 4)

			SN54LV	T16500	SN74LV	/T16500	UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage		2	L.	2		V
VIL	Low-level input voltage			Ø .8		0.8	V
VI	Input voltage		8	₹ 5.5		5.5	٧
ЮН	High-level output current		Ų, Ç	-24		-32	mA
loL	Low-level output current		Ş	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	8	10		10	ns/V
TΑ	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SCBS146C - MAY 1992 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

24244555	-	FOT COMPLETIONS		SNS	4LVT16	500	SN7	4LVT16	500	
PARAMETER	!!	EST CONDITIONS		MIN	TYPT	MAX	MIN	TYP	MAX	UNIT
VIK	V _{CC} = 2.7 V,	l _l = −18 mA				-1.2			-1.2	٧
	V _{CC} = MIN to MAX [‡] ,	lOH = -100 μA	•	VCC-C	.2		VCC-0	.2		
V	$V_{CC} = 2.7 \text{ V},$	I _{OH} = -8 mA		2.4			2.4			v
VOH	V _{CC} = 3 V	I _{OH} = -24 mA		2						V
	VCC = 3 V	I _{OH} = -32 mA					2			
	V _{CC} = 2.7 V	l _{OL} = 100 μA				0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
V		I _{OL} = 16 mA				0.4			0.4	V
V _{OL}	V 0.V	I _{OL} = 32 mA				0.5			0.5	V
	V _{CC} = 3 V	IOL = 48 mA				0.55				
		I _{OL} = 64 mA				ly.			0.55	:
	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	Control		Ś				±1	
	V _{CC} = 0 or MAX [‡] ,	V _I = 5.5 V	inputs		\$	10			10	
lį		V _I = 5.5 V			Z.	20			20	μА
	V _{CC} = 3.6 V	V _I = V _{CC}	A or B ports§		3	5			5	
		V _I = 0		٠, ٥	3	-10			-10	
l _{off}	$V_{CC} = 0$,	V _I or V _O = 0 to 4.5 V		Q.					±100	μА
lia - i-s	V _{CC} = 3 V	V _I = 0.8 V	A or B ports	75			75			μА
l(hold)	VCC = 3 V	V _I = 2 V	A or B ports	-75			- 75			μΛ
^l OZH	V _{CC} = 3.6 V,	V _O = 3 V				1			1	μΑ
lozl	$V_{CC} = 3.6 \text{ V},$	V _O = 0.5 V				-1			-1	μА
			Outputs high			0.12			0.12	
Icc	V _{CC} = 3.6 V,	$I_{O} = 0$,	Outputs low			5	1		5	mA
.00	V _I = V _{CC} or GND		Outputs disabled			0.12			0.12	
ΔICC¶	$V_{CC} = 3 \text{ V to } 3.6 \text{ V,}$ Other inputs at V_{CC} o	One input at V _{CC} – 0.6 r GND	V,			0.2			0.2	mA
Ci	V _i = 3 V or 0				3.5			3.5		pF
C _{io}	V _O = 3 V or 0				12			12		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at VCC or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SCBS146C - MAY 1992 - REVISED JULY 1995

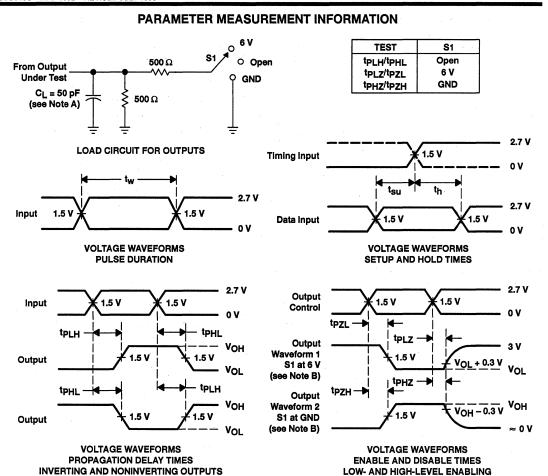
timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				SN54LV	T16500			SN74LV	T16500		
			V _{CC} =		Vcc=	2.7 V	V _{CC} =		V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	150	0	125	0	150	0	125	MHz
	Pulse duration	LE high	3.3		3.3		3.3		3.3		
tw	Pulse duration	CLK high or low	3.3		3.3		3.3		3.3		ns
		A before CLKAB↓	1.8		£€1.1		1.8		1.1		
	0.1	B before CLKBA↓	1.9		Q 1.2		1.9		1.2		
^t su	Setup time	A or B before LE↓, CLK high	2.2	Š	1.3		2.2		1.3		ns
	Hold time	A or B before LE↓, CLK low	2.7	్టర్	1.9		2.7		1.9		
		A or B after CLK↓	1.2	Q.	1.2		1.2		1.2		
th		A or B after LE↓	0.9		1.1		0.9		1.1		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

				SN54LV	T16500			SN7	4LVT16	500		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		Vcc =	2.7 V	V	C = 3.3 ± 0.3 V	٧	V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
f _{max}			150		125		150			125		MHz
^t PLH	D an A	A or B	1.7	5.8		7	1.7	3	5.4		6.8	ns
^t PHL	BorA	AOID	1.6	6		7.8	1.6	3.2	5.9		7.7	115
^t PLH	LEDALEAD	A or B	2.3	7.3		8.9	2.3	4	7		8.5	
^t PHL	LEBA or LEAB	AOIB	2.7	8.2		9.8	2.7	4.3	7.9		9.7	ns
^t PLH	CLKBA or	A or B	2	7.4		8.8	2	4.1	7		8.3	
^t PHL	CLKAB	AOrb	2.4	83		10	2.4	4.4	7.9		9.9	ns
^t PZH	OEBA or	A or B	1.2	€ 3.2		6.1	1.2	3	5		5.9	
^t PZL	OEAB	AULD	1.5	[≪] 5.9		7	1.5	.3	5.8		6.9	ns
^t PHZ	OEBA or	A or B	2.7	7.7		8.6	2.7	4.6	7.4		8.3	
^t PLZ	OEAB	AUFB	2.8	7.3		7.7	2.8	4.7	6.7		7.2	ns

 $[\]dagger$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCBS147D - MAY 1992 - REVISED JULY 1995

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments Widebus™ Family
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- UBT[™] (Universal Bus Transceiver)
 Combines D-Type Latches and D-Type
 Flip-Flops for Operation in Transparent,
 Latched, or Clocked Mode
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes
 PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVT16501 . . . WD PACKAGE SN74LVT16501 . . . DGG OR DL PACKAGE (TOP VIEW)

OEAB	┨╸└	56 GND
LEAB		55 CLKAB
A1] 3	54 🕽 B1
GND	[] 4	53 🛮 GND
A2		52 🕽 B2
А3		51 🛛 B3
Vcc	7	50] V _{CC}
A4	8	49 🛮 B4
A5] 9	48 🕽 B5
A6	10	47 🕽 B6
GND	11	46] GND
	12	45 🛮 B7
A8	13	44 🛛 B8
A9	14	43 B9
A10		42]] B10
A11	16	41 B11
A12		40 B12
GND		39 🛚 GND
A13		38 🛮 B13
A14	20	37 🛭 B14
A15		36 🛮 B15
v _{cc} l	22	35 🛘 V _{CC}
A16	23	34 🛭 B16
A17	24	33 🛭 B17
GND		32 🛛 GND
A18	26	31 🛛 B18
OEBA		30 CLKBA
LEBA	28	29] GND

description

The 'LVT16501 are 18-bit universal bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

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SCBS147D - MAY 1992 - REVISED JULY 1995

description (continued)

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and OEBA is active low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, OE should be tied to VCC through a pullup resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74LVT16501 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the input/output (I/O) pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16501 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT16501 is characterized for operation from -40°C to 85°C.

FUNCTION TABLET

	INP	UTS		OUTPUT
OEAB	LEAB	CLKAB	Α	В
L	X	Х	Х	Z
Н.	Н	X	L	L
н	Н	Х	Н	н
Н	L	1	L	L
н	L	1	Н	н
н	L	Н	Х	в _о ‡
н	L	L	Х	В ₀ ‡ В ₀ §

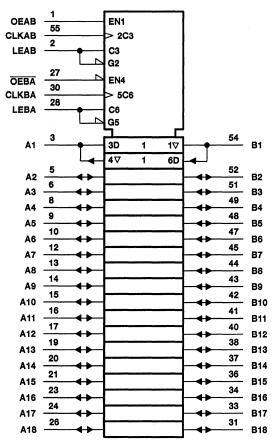
[†] A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

[‡] Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

[§] Output level before the indicated steady-state input conditions were established

SCBS147D - MAY 1992 - REVISED JULY 1995

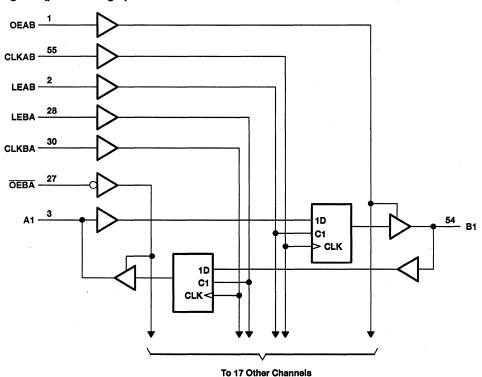
logic symbolt



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54LVT16501, SN74LVT16501 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS147D - MAY 1992 - REVISED JULY 1995

logic diagram (positive logic)



SCBS147D - MAY 1992 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.	
Input voltage range, V _I (see Note 1) – Voltage range applied to any output in the high state or power-off state, V _O (see Note 1) –	
Current into any output in the low state, Io: SN54LVT16501	
SN74LVT16501	128 mA
Current into any output in the high state, IO (see Note 2): SN54LVT16501	48 mA
SN74LVT16501	
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I _{OK} (V _O <0)	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	
DL package	1.4 W
Operating free-air temperature range, T _A : SN54LVT16501 –55	°C to 125°C
SN74LVT165014	0°C to 85°C
Storage temperature range, T _{stq} –65	°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

l			SN54LV	T16501	SN74LV	T16501	UNIT
			MIN	MAX	MIN	MAX	UNII
VCC	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage		2	Ø	2		٧
VIL	Low-level input voltage			8.00		0.8	٧
VI	Input voltage			₹ 5.5		5.5	٧
ЮН	High-level output current		, Ç	~ –2 4		-32	mA
loL	Low-level output current		S.	48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled	8	10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SCBS147D - MAY 1992 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DAMETED	7507	CONDITIO	210	SNS	4LVT16	501	SN7	4LVT16	501	LIAUT
PA	RAMETER	IESI	CONDITIO	JN5	MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK		V _{CC} = 2.7 V,	I _I = -18	mA	[-1.2			-1.2	٧
		V _{CC} = MIN to MAX [‡] ,	IOH = -	100 μΑ	VCC-C).2		Vcc-C).2		
V		$V_{CC} = 2.7 \text{ V},$	IOH = -	8 mA	2.4			2.4			v
VOH		V 2V	loH = -		2						V
		VCC = 3 V	IOH = -:	32 mA				2			
		V _{CC} = 2.7 V	I _{OL} = 10	00 μΑ			0.2			0.2	
		VCC = 2.7 V	I _{OL} = 24	l mA			0.5			0.5	
V			I _{OL} = 16	i mA			0.4			0.4	v
VOL		V 0V	I _{OL} = 32	2 mA			0.5			0.5	v
		VCC = 3 V	I _{OL} = 48	3 mA			0.55				
			IOL = 64	l mA			A.			0.55	
	Control pins	$V_{CC} = 3.6 \text{ V},$	VI = VC	or GND		75	* ±1			±1	
	Control pins	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5	V		S.	10			10	1
Ŋ			V _I = 5.5	V		6	20			20	μA
	A or B ports§	V _{CC} = 3.6 V	VI = VC	0		3	1			1	
			V _I = 0			?	-5			-5	
loff		V _{CC} = 0,	V _I or V _C	= 0 to 4.5 V	~					±100	μА
I.a	A or B ports	V _{CC} = 3 V	V _I = 0.8	٧	75			75			μА
I(hold)	A of B poils	ACC = 2 A	V _I = 2 V		-75			-75			μΛ
lozh		$V_{CC} = 3.6 \text{ V},$	V _O = 3 \	/			1			1	μА
lozL		V _{CC} = 3.6 V,	$V_{O} = 0.5$	5 V			-1			-1	μA
				Outputs high			0.12			0.12	
ICC		V _{CC} = 3.6 V, V _I = V _{CC} or GND	$I_{O} = 0$,	Outputs low			5			5	mA
		11 - 100 or arts		Outputs disabled			0.12			0.12	
ΔICC¶		V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} o		ut at V _{CC} – 0.6 V,			0.2			0.2	mA
Ci		V _I = 3 V or 0				3.5			3.5		pF
Cio		V _O = 3 V or 0				12			12		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at VCC or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SCBS147D - MAY 1992 - REVISED JULY 1995

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

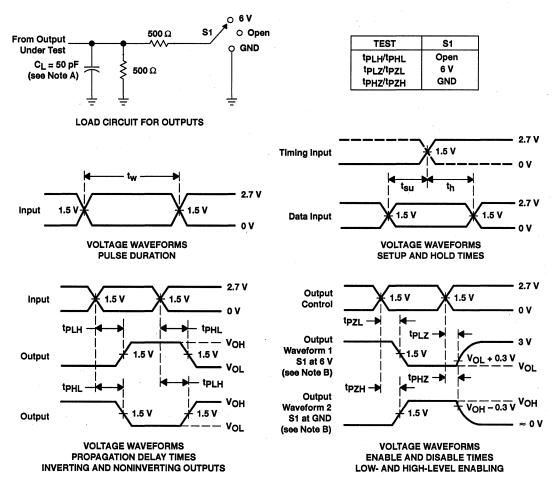
				SN54LV	T16501			SN74LV	T16501		
			V _{CC} = 3.3 V ± 0.3 V		Vcc =	2.7 V	V V _{CC} = 3.3 ± 0.3 V		V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	150	0	125	0	150	0	125	MHz
	Bules duration	LE high	3.3		3.3		3.3		3.3		ns
tw	Pulse duration	CLK high or low	3.3		3.3		3.3		3.3		115
		A before CLKAB↑	1.6		%2.1		1.6		2.1		
		B before CLKBA↑	1.6		2.1		1.6		2.1		
^t su	Setup time	A or B before LE↓, CLK high	2.6	Š	1.9		2.6		1.9		ns
	Hold time	A or B before LE↓, CLK low	2		1.3		2		1.3		
. .		A or B after CLK↑	2	Q"	2.1		2		2.1		ns
^t h		A or B after LE↓	0.9		1.2		0.9		1.2		115

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

				SN54LV	T16501			SN7	4LVT16	501		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =	2.7 V	V	CC = 3.3 ± 0.3 V	V	V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
fmax			150		125		150			125		MHz
tPLH	B or A	A or B	1.7	5.4		5.8	1.7	3	5.4		6.8	ns
tPHL	BOLA	AUID	1.6	6		7.8	1.6	3.2	5.9		7.7	115
^t PLH	LEBA or LEAB	A or B	2.3	7.3	75	9	2.3	4	7		8.5	ns
^t PHL		AUIB	2.7	8.2	8.	9.8	2.7	4.3	7.9		9.7	115
^t PLH	CLKBA or	A or B	2.5	8.3	*	9.7	2.5	4.1	7.9		9.2	
tPHL	CLKAB	AOIB	3.5	9.4		10.7	3.5	5.4	8.9		10.4	ns
^t PZH	<u> </u>	A or B	1.2	⊘ 5.1		6.1	1.2	3	5		5.9	
tPZL	OEBA or OEAB	AUIB	1.5	[≪] 5.9		7	1.5	3	5.8		6.9	ns
^t PHZ	OEBA or OEAB	A or B	2.7	7.5		8.5	2.7	4.6	7.4		8.3	
tPLZ	OLDA OF OEAD	AUID	2.8	6.8		7.5	2.8	4.7	6.7		7.2	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_r \leq 2.5 \,\text{ns}$, $t_f \leq 2.5 \,\text{ns}$.

D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVT16543, SN74LVT16543 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS148C - MAY 1992 - REVISED JULY 1995

 State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power 	SN54LVT16543WD PACKAGE SN74LVT16543DGG OR DL PACKAGE (TOP VIEW)	
Dissipation	10EAB I	56 1 1 OEBA
Members of the Texas Instruments	1LEAB []2	55 1 1 LEBA
<i>Widebus</i> ™ Family	1CEAB II3	54 1 1 CEBA
Support Mixed-Mode Signal Operation (5-V)	GND []4	53 GND
Input and Output Voltages With 3.3-V V _{CC})	1A1 05	52 1B1
Support Unregulated Battery Operation	1A2 []6	51 1B2
Down to 2.7 V	V _{CC} 🗓 7	50 V _{CC}
Typical V _{OLP} (Output Ground Bounce)	1Ă3 🛮 8	49 1 1 B3
< 0.8 V at V _{CC} = 3.3 V, T _A = 25°C	1A4 🗓 9	48 🛘 1B4
ESD Protection Exceeds 2000 V Per	1A5 🛚 10	47 🛘 1B5
MIL-STD-883C, Method 3015; Exceeds	GND 🛚 11	46 🛛 GND
200 V Using Machine Model	1A6 [] 12	45 [] 1B6
(C = 200 pF, R = 0)	1A7 []13	44 🛛 1B7
Latch-Up Performance Exceeds 500 mA	1A8 []14	43 🛛 1B8
Per JEDEC Standard JESD-17	2A1 []15	42 2B1
Bus-Hold Data Inputs Eliminate the Need	2A2 🛮 16	41 2B2
for External Pullup Resistors	2A3 🛮 17	40 2B3
•	GND [] 18	39 GND
Support Live Insertion	2A4 [] 19	38
Distributed V _{CC} and GND Pin Configuration	2A5 []20 2A6 []21	37 J 285 36 J 286
Minimizes High-Speed Switching Noise	3	35 D V _{CC}
Flow-Through Architecture Optimizes	V _{CC} U22 2A7 [23	34 1 2B7
PCB Layout	2A8 1 24	33 2B8
 Package Options Include Plastic 300-mil 	GND 1 25	32 GND
Shrink Small-Outline (DL) and Thin Shrink	2CEAB 1 26	31 2 <u>CEBA</u>
Small-Outline (DGG) Packages and 380-mil	2 <u>LEAB</u> 127	30 2 2 LEBA
Fine-Pitch Ceramic Flat (WD) Package	20EAB []28	29 20EBA
Using 25-mil Center-to-Center Spacings	1	

description

The 'LVT16543 are 16-bit registered transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (CEAB) input must be low in order to enter data from A or to output data from B. If CEAB is low and LEAB is low, the A-to-B latches are transparent; a subsequent low-to-high transition of LEAB puts the A latches in the storage mode. With CEAB and OEAB both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the CEBA, LEBA, and OEBA inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

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SCBS148C - MAY 1992 - REVISED JULY 1995

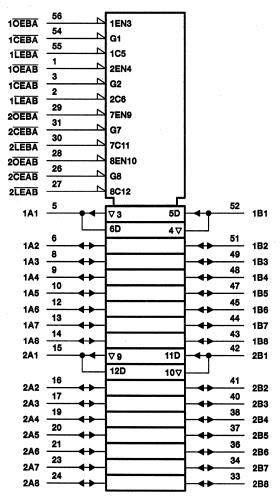
description (continued)

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16543 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16543 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16543 is characterized for operation from –40°C to 85°C.

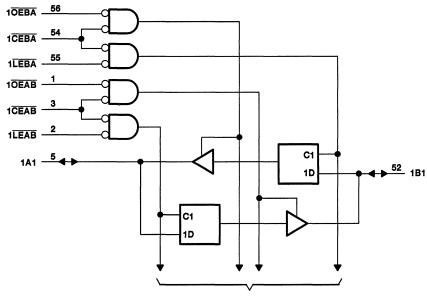
logic symbol[†]



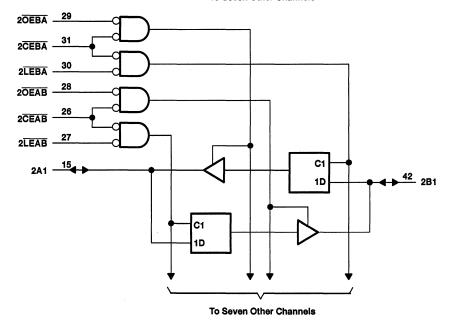
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



To Seven Other Channels



SCBS148C - MAY 1992 - REVISED JULY 1995

FUNCTION TABLET (each 8-bit section)

	INPUTS							
CEAB	LEAB	OEAB	Α	В				
Н	Х	Х	Х	Z				
x	X	Н	Χ	Z				
L	Н	L	Х	в ₀ ‡				
L	L	L	L	L				
L	L	L	Н	н				

[†] A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1)	
Current into any output in the low state, Io: SN54LVT16543	
SN74LVT16543	
Current into any output in the high state, IO (see Note 2): SN54LVT16543	
SN74LVT16543	
Input clamp current, I_{IK} ($V_1 < 0$)	–50 mA
Output clamp current, $I_{OK}(V_O < 0)$	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	
DL package	
Storage temperature range, T _{stg}	65°C to 150°C

[§] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current flows only when the output is in the high state and VO > VCC.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			SN54LV	T16543	SN74LV	T16543	UNIT
			MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage		2	- A	2		٧
VIL	Low-level input voltage			/0.8		0.8	٧
VI	Input voltage			₹ [©] 5.5		5.5	٧
Іон	High-level output current		T Ó	~ –24		-32	mA
loL	Low-level output current		Š	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	ŢĶ.	10		10	ns/V
TA	Operating free-air temperature			125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



[‡] Output level before the indicated steady-state input conditions were established

SN54LVT16543, SN74LVT16543 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS148C - MAY 1992 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	-	FOT COMPLETIONS		SNS	54LVT165	543	SN7	'4LVT16	543	UNIT
PARAMETER		EST CONDITIONS		MIN	TYPT	MAX	MIN	TYPT	MAX	UNII
VIK	$V_{CC} = 2.7 \text{ V},$	I _I = -18 mA				-1.2			-1.2	V
	$V_{CC} = MIN \text{ to } MAX^{\ddagger},$	I _{OH} = -100 μA		V _{CC} -C).2		VCC-0).2		
Vou	$V_{CC} = 2.7 \text{ V},$	I _{OH} = -8 mA		2.4			2.4			v
VOH	V _{CC} = 3 V	I _{OH} = - 24 mA		2						V
	ACC = 2 A	IOH = -32 mA					2			
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
Va		I _{OL} = 16 mA				0.4			0.4	v
VOL	V _{CC} = 3 V	I _{OL} = 32 mA				0.5			0.5	V
	\ \CC = 2 \	I _{OL} = 48 mA				0.55	5			
		I _{OL} = 64 mA		18			0.55			
	$V_{CC} = 3.6 \text{ V},$	V _I = V _{CC} or GND	V _I = V _{CC} or GND Control inputs		1/2	° ±1			±1	
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V	Control inputs		8	10			10	
ļl _i		V _I = 5.5 V			8	20			20	μА
	V _{CC} = 3.6 V	V _I = V _{CC}	A or B ports§		ð	5			5	
		V ₁ = 0		<i>&</i>		-10			-10	
l _{off}	$V_{CC} = 0$,	$V_1 \text{ or } V_0 = 0 \text{ to } 4.5$	V	~					±100	μА
lia in	V _{CC} = 3 V	V _I = 0.8 V	A or B ports	75			75			^
l(hold)	ACC = 2 A	V ₁ = 2 V	A of B ports	-75			-75			μА
lozh	V _{CC} = 3.6 V,	V _O = 3 V				1			1	μΑ
lozL	V _{CC} = 3.6 V,	V _O = 0.5 V				-1			-1	μΑ
	V 00V	I _O = 0,	Outputs high			0.12			0.12	
Icc	$V_{CC} = 3.6 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$		Outputs low			5			5	mA
	11 - 100 or arts		Outputs disabled			0.12			0.12	:
ΔICC¶	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND					0.2			0.2	mA
Ci	V _I = 3 V or 0				4			4		pF
C _{io}	V _O = 3 V or 0				13			13		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at V_{CC} or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SN54LVT16543, SN74LVT16543 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS148C - MAY 1992 - REVISED JULY 1995

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

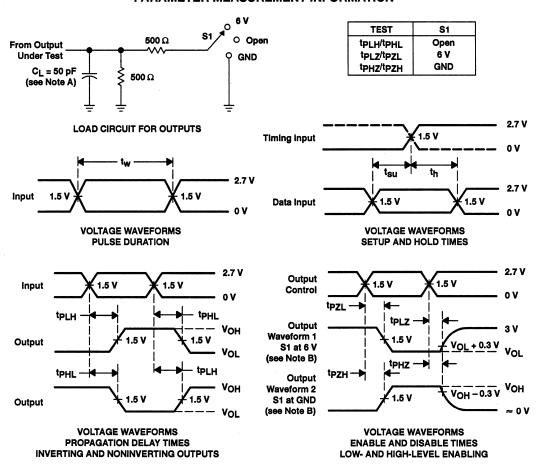
					SN54LVT16543			SN74LVT16543					
				V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT	
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t _w	Pulse durati	on, LEAB or LEBA low		3.3		3.3		3.3		3.3		ns	
	A or B before LEAB↑ or		Data high	0.8		0.5		0.8		0.5		ns	
١.	LEBA↑	Data low	1.5		199		1.5		1.9		118		
tsu	Setup time	A or B before CEAB↑ or	Data high	0.7		\$0.4		0.7		0.4			
		CEBA↑	Data low	1.6		<u>ڳ</u> 1.9		1.6		1.9		ns	
		A or B after LEAB↑ or	Data high	0.8	å	0		0.8		0			
	Hold time	Data low	1.2	ΔÇ.	1.3		1.2		1.3		ns		
th	noia time	A or B after CEAB↑ or	Data high	0.8	4	0		0.8		0			
	CEBA1		Data low	1.3		1.4		1.3		1.4		ns	

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

				SN54LV	T16543			SN7	4LVT16	543		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	1.4	5		5.8	1.4	2.7	4.6		5.5	ns
^t PHL	AUID	BUIA	1.3	4.7		5.9	1.3	2.9	4.6		5.8	115
t _{PLH}	ĪĒ	A or B	1.3	6.8		8.5	1.7	3.7	6.3		8.1	ns
t _{PHL}	LE	AOIB	1.5	6.5	/S	8.3	1.9	3.7	6		7.8	110
tPZH_	ŌĒ	A or B	1.4		Ş.	7.7	1.5	3.3	5.8		7.6	ns
^t PZL	OE	AOIB	1.6	6.3	•	8.4	1.6	3.3	6.2		8.2	115
t _{PHZ}	ŌĒ	A or B	2	63		7.3	2	4.1	6.5		7.1	ns
t _{PLZ}	OE .	AOIB	2.7	₹2 6		6.2	2.7	3.9	5.8		5.9	115
^t PZH	CE	A or B	1.4	[≪] 6.2		7.7	1.5	3.3	6		7.6	
tPZL	CE	AVIB	1.6	6.6		8.5	1.7	3.3	6.4		8.3	ns
t _{PHZ}	CE	A or B	2	6.6		7.2	2	4.1	6.4		7.1	ns
^t PLZ	J	AVIB	2.6	5.6		5.9	2.6	4	5.4		5.6	118

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVT16600, SN74LVT16600 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCES001A - JULY 1994 - REVISED JULY 1995

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V **Operation and Low-Static Power** Dissipation
- **Members of the Texas Instruments** Widebus™ Family
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- UBT™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Typical V_{OLP} (Output Ground Bounce) $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C. Method 3015: Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Distributed V_{CC} and GND Pin Configuration **Minimizes High-Speed Switching Noise**
- Flow-Through Architecture Optimizes **PCB Layout**
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package **Using 25-mil Center-to-Center Spacings**

SN54LVT16600 . . . WD PACKAGE SN74LVT16600 . . . DGG OR DL PACKAGE (TOP VIEW)

4	_	_	_	1
OEAB [1	U	56	CLKENAB
LEAB [CLKAB
A1 [54] B1
GND [53	GND
A2 [52	B2
АЗ [51] B3
v _{cc} [7		50	l v _{cc}
A4 🛚	8		49	B4
A5 [A6 [9		48] B5
A6 🛚	10		47] B6
GND [46	GND
A7 [12		45] B7
A8 [44	B7 B8
A9 [43	∐ B9
A10 🛚	15		42	B10
A11 🛚			41	B11
A12 🛭	17		40	B12
GND [18		39	GND
A13 🛚	19		38	B13
A14 🛚	20		37	B14
A15 🛚			36	B15
v _{cc} [22		35	v _{cc}
A16	23		34	B16
A17	24		33	B17
GND [25		32	GND
A18	26		31	B18
OEBA [2/		30	CLKBA
LEBA [28		29	CLKENBA

description

The 'LVT16600 are 18-bit universal bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

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SN54LVT16600, SN74LVT16600 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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description (continued)

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable (CLKENAB and CLKENBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output enable OEAB is active low. When OEAB is low, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, CLKBA, and CLKENBA.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16600 is available in Tl's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16600 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT16600 is characterized for operation from -40°C to 85°C.

FUNCTION TABLET

	INPUTS								
CLKENAB	OEAB	LEAB	CLKAB	Α	В				
Х	Н	Х	Х	Х	Z				
Х	L	Н	Χ	L	L				
x .	Ĺ	Н	X	Н	-⁄ H				
Н	L	L	X	Х	В ₀ ‡ В ₀ ‡				
н	L	L	X	Χ	в ₀ ‡				
L	L	L	1	L	L				
L	L	L	\downarrow	Н	н				
L	L	L	Н	X	в ₀ ‡				
L	L	L	L	Х	В ₀ ‡ В ₀ §				

[†] A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.

[‡] Output level before the indicated steady-state input conditions were established

[§] Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

Iogic diagram (positive logic) OEAB CLKENAB CLKENAB CLKENAB CLKENBA C

To 17 Other Channels



SN54LVT16600, SN74LVT16600 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-0.5 V to 4.6 V
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1)	
Current into any output in the low state, I _O : SN54LVT16600	
SN74LVT16600	
Current into any output in the high state, I _O (see Note 2): SN54LVT16600	48 mA
SN74LVT16600	64 mA
Input clamp current, I _{IK} (V _I < 0)	50 mA
Output clamp current, I_{OK} ($V_O < 0$)	~50 mA
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): DGG package	1 W
DL package	
Storage temperature range, T _{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current flows only when the output is in the high state and VO > VCC.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

İ			SN54LV	T16600	SN74LV	T16600	UNIT
			MIN	MAX	MIN	MAX	ONIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧
v_{IH}	High-level input voltage	2		2		٧	
VIL	Low-level input voltage		0.8		0.8	٧	
VI	Input voltage			5.5		5.5	V
loн	High-level output current		•	-24		-32	mA
IOL	Low-level output current		48		64	mA	
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN54LVT16600, SN74LVT16600 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

		TOT COMPLETIONS		SNS	4LVT16	600	SN7	4LVT16	600	UNIT
PARAMETER		EST CONDITIONS		MIN	TYPT	MAX	MIN	TYPT	MAX	UNII
VIK	$V_{CC} = 2.7 \text{ V},$	l _l = -18 mA				-1.2			-1.2	V
	V _{CC} = MIN to MAX‡,	l _{OH} = -100 μA		VCC-C).2		V _{CC} -0.2			
Vari	V _{CC} = 2.7 V,	IOH = -8 mA		2.4			2.4			v
VOH	V _{CC} = 3 V	IOH = - 24 mA		2						V
	ACC = 2 A	I _{OH} = -32 mA					2			
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
VOL		I _{OL} = 16 mA				0.4			0.4	V
VOL	V _{CC} = 3 V	IOL = 32 mA				0.5			0.5	V
	ACC = 2 A	I _{OL} = 48 mA				0.55				1
		I _{OL} = 64 mA							0.55	
	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	Control			±1			±1	
	$V_{CC} = 0$ or MAX [‡] ,	V _I = 5.5 V	inputs			10	10 1			
lj .		V _I = 5.5 V				20			20	μА
	V _{CC} = 3.6 V	VI = VCC	A or B ports§			5			5	
		V _I = 0	1	-10			-10			
loff	$V_{CC} = 0$,	$V_{ }$ or $V_{ } = 0$ to 4.5 V			-				±100	μА
len en	V _{CC} = 3 V	V _I = 0.8 V	A or B ports	75			75			μА
li(hold)	^CC = 2 v	V _I = 2 V	A or B ports	-75			-75			μА
lozh	V _{CC} = 3.6 V,	V _O = 3 V				1			1	μА
lozL	V _{CC} = 3.6 V,	V _O = 0.5 V				-1			-1	μА
			Outputs high			0.12			0.12	
lcc	V _{CC} = 3.6 V,	IO = 0,	Outputs low			5			5	mA
100	V _I = V _{CC} or GND	/i = V _{CC} or GND				0.12			0.12	ША
∆lcc¶	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND					0.2			0.2	mA
Ci	V _I = 3 V or 0				3.5			3.5		pF
C _{io}	V _O = 3 V or 0				12			12		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at V_{CC} or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54LVT16601, SN74LVT16601 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCES002A - JULY 1994 - REVISED JULY 1995

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments Widebus™ Family
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- UBT™ (Universal Bus Transceiver)
 Combines D-Type Latches and D-Type
 Flip-Flops for Operation in Transparent,
 Latched, or Clocked Mode
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVT16601 ... WD PACKAGE SN74LVT16601 ... DGG OR DL PACKAGE (TOP VIEW)

OEAB [₁ , ∪	56	CLKENAB
LEAB [2	55	CLKAB
A1 [54	B1
GND [53	GND
A2 [52	B2
A3 [51] B3
Vcc [7	50	V _{CC}
A4 [49	B4
A5 [9	48	B5
A6 [10	47] B6
GND [11	46	GND
A7 [12	45] B7
A8 [13	44] B8
A9 [14	43] B9
A10 [15		B10
A11 [16	41	B11
A12 [40] B12
GND [39	GND
A13 [38] B13
A14 [20		B14
A15	21		B15
V _{CC} [22	35] V _{CC}
A16	23	34]B16
A17 [33	B17
GND [GND
A18 [31	B18
OEBA [30	CLKBA
LEBA [28	29	CLKENBA

description

The 'LVT16601 are 18-bit universal bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

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SN54LVT16601, SN74LVT16601 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCES002A - JULY 1994 - REVISED JULY 1995

description (continued)

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable (CLKENAB and CLKENBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Output enable OEAB is active low. When OEAB is low, the outputs are active. When OEAB is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, CLKBA, and CLKENBA.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16601 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16601 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT16601 is characterized for operation from -40°C to 85°C.

FUNCTION TABLET

	ı	NPUTS			OUTPUT
CLKENAB	OEAB	LEAB	CLKAB	Α	В
Х	Н	Х	Х	Х	Z
х	L	Н	Χ	L	Ĺ
х	L	Н	X	Н	н
Н	L ·	L	X	Χ	В ₀ ‡ В ₀ ‡
н	L	L	X	Χ	в ₀ ‡
L	L	L	1	L	L
L	L	L	1	· H	: Н
L	L	L	L	Х	в ₀ ‡
L	L	L	Н	X	В ₀ ‡ В ₀ §

[†] A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.

[‡] Output level before the indicated steady-state input conditions were established

[§] Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

logic diagram (positive logic) OEAB ____1 CLKENAB __56 CLKAB 55 LEAB 2 LEBA —28 CLKBA -CLKENBA _____29 CE 1D C1 > CLK CE 1D C1

To 17 Other Channels



SN54LVT16601, SN74LVT16601 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCES002A - JULY 1994 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-05Vto46V
Supply voltage range, VCC	0.5 1/4- 7 1/
Input voltage range, V _I (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo (see Note 1)	
Current into any output in the low state, Io: SN54LVT16601	96 mA
SN74LVT16601	128 mA
Current into any output in the high state, IO (see Note 2): SN54LVT16601	48 mA
SN74LVT16601	64 mA
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range, T _{stg}	65°C to 150°C
and the state of t	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			SN54LV	T16601	SN74LV	UNIT	
			MIN	MAX	MIN	MAX	ONII
VCC	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage		2		2		٧
VIL	Low-level input voltage			0.8		0.8	٧
٧ _I	Input voltage			5.5		5.5	٧.
ЮН	High-level output current	·		-24		-32	mA
loL	Low-level output current		r	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	•€

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN54LVT16601, SN74LVT16601 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCES002A - JULY 1994 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	-	SNS	4LVT16	601	SN74LVT16601			UNIT			
PARAMETER	1	EST CONDITIONS		MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT	
VIK	V _{CC} = 2.7 V,	l _l = -18 mA				-1.2			-1.2	٧	
	V _{CC} = MIN to MAX [‡] ,	I _{OH} = -100 μA		VCC-C	.2		V _{CC} -0	.2			
V	V _{CC} = 2.7 V,	IOH = - 8 mA		2.4			2.4			v	
VOH		I _{OH} = -24 mA		2						٧	
	V _{CC} = 3 V	IOH = -32 mA					2				
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2		
	VCC = 2.7 V	I _{OL} = 24 mA			0.5			0.5			
Va. [I _{OL} = 16 mA		i .		0.4			0.4	v	
VOL	V _{CC} = 3 V	I _{OL} = 32 mA				0.5			0.5	V	
	ACC = 2 A	I _{OL} = 48 mA				0.55					
		I _{OL} = 64 mA							0.55		
	$V_{CC} = 3.6 \text{ V},$	V _I = V _{CC} or GND	Control			±1			±1		
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V	inputs			10			10		
łį		V _I = 5.5 V				20			20	20 μΑ	
	V _{CC} = 3.6 V	V _I = V _{CC}	A or B ports§			5			5		
		V _I = 0	1			-10			-10	1	
l _{off}	$V_{CC} = 0$,	V_I or $V_O = 0$ to 4.5 V							±100	μΑ	
11/1-1-11	V _{CC} = 3 V	V _I = 0.8 V	A or B ports	75			75			μА	
l(hold)	VCC = 0 V	V _I = 2 V	A OI B ports	-75			– 75			μΛ	
lozh	$V_{CC} = 3.6 \text{ V},$	V _O = 3 V				1			1	μΑ	
lozl	$V_{CC} = 3.6 \text{ V},$	V _O = 0.5 V				-1			-1	μΑ	
			Outputs high			0.12			0.12		
lcc	V _{CC} = 3.6 V,	$l_{O}=0$,	Outputs low			5			5	mA	
	$V_I = V_{CC}$ or GND		Outputs disabled				0.12	111/4			
ΔICC [¶]	V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				0.2			0.2	mA		
Ci	V _I = 3 V or 0				3.5			3.5		pF	
Cio	V _O = 3 V or 0				12			12		pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at VCC or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

CBS149C - JULY 1994 - REVISED JULY 1995

 State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power 	SN54LVT16646 WD PACKA SN74LVT16646 DGG OR DL PA (TOP VIEW)				
Dissipation Members of the Texas Instruments	1DIR [] 1	56 10E			
Widebus™ Family	1CLKAB	55 11 1CLKBA 54 11 1SBA			
Support Mixed-Mode Signal Operation (5-V	GND []4	53 I GND			
Input and Output Voltages With 3.3-V V _{CC})	1A1 [5	52 1B1			
Support Unregulated Battery Operation	1A2 ∐ 6	51 1B2			
Down to 2.7 V	V _{CC} []7	50 V _{CC}			
 Typical V_{OLP} (Output Ground Bounce) 	1A3 [] 8 1A4 [] 9	49 🛛 1B3 48 🖟 1B4			
< 0.8 V at V_{CC} = 3.3 V, T_A = 25°C	1A4 U 9 1A5 🛘 10	47 1 1B5			
ESD Protection Exceeds 2000 V Per NUL OTB 2000 Method 2015: Exceeds	GND [] 11	46 GND			
MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model	1A6 🛚 12	45 1B6			
(C = 200 pF, R = 0)	1A7 🛚 13	44 🛛 1B7			
Latch-Up Performance Exceeds 500 mA	1A8 🛮 14	43 1 1B8			
Per JEDEC Standard JESD-17	2A1 🛭 15 2A2 🖟 16	42 2B1 41 2B2			
Bus-Hold Data Inputs Eliminate the Need	2A3 17	40 2B3			
for External Pullup Resistors	GND [] 18	39 GND			
Support Live Insertion	2A4 🛚 19	38] 2B4			
 Distributed V_{CC} and GND Pin Configuration 	2A5 🛮 20	37 2B5			
Minimizes High-Speed Switching Noise	2A6 []21	36 2B6			
Flow-Through Architecture Optimizes	V _{CC} [] 22 2A7 [] 23	35 V _{CC} 34 2B7			
PCB Layout	2A7 1 23 2A8 1 24	33 2B8			
Package Options Include Plastic 300-mil	GND [] 25	32 GND			
Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil	2SAB 🛚 26	31] 2SBA			
Fine-Pitch Ceramic Flat (WD) Package	2CLKAB [] 27	30 2CLKBA			
Using 25-mil Center-to-Center Spacings	2DIR [28	29 2OE			

description

The 'LVT16646 are 16-bit bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT16646.

Output-enable (\overline{OE}) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. The direction control (DIR) determines which bus receives data when \overline{OE} is low. In the isolation mode $(\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

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SCBS149C - JULY 1994 - REVISED JULY 1995

description (continued)

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16646 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16646 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT16646 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

		INPUTS DATA I/Os				OPERATION OR FUNCTION		
ŌĒ	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	·
Х	Х	1	Х	Х	Х	Input	Unspecified [†]	Store A, B unspecified†
, X.	X	X	1	X	X	Unspecified [†]	Input	Store B, A unspecified†
н	Х	1	1	Х	Х	Input	Input	Store A and B data
н	X	H or L	H or L	Х	X	Input disabled	Input disabled	Isolation, hold storage
L	L	Х	X	Х	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	Х	Н	Output	Input	Stored B data to A bus
L	Н	Х	Х	L	Х	Input -	Output	Real-time A data to B bus
L	Н	H or L	X	Н	- X	Input	Output	Stored A data to B bus

[†] The data output functions may be enabled or disabled by various signals at $\overline{\sf OE}$ and DIR. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

SCBS149C - JULY 1994 - REVISED JULY 1995

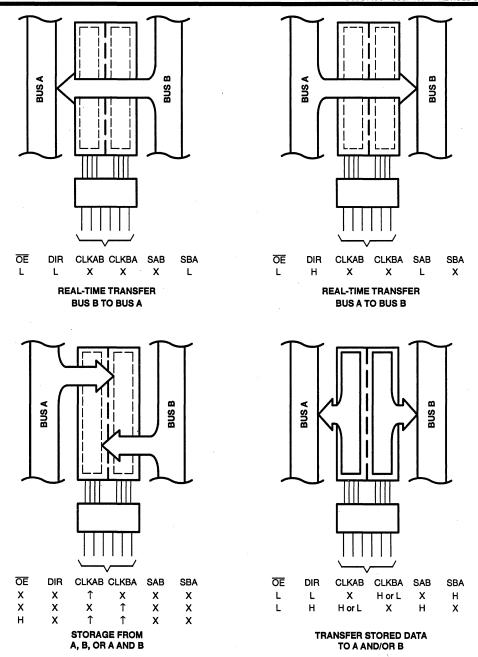
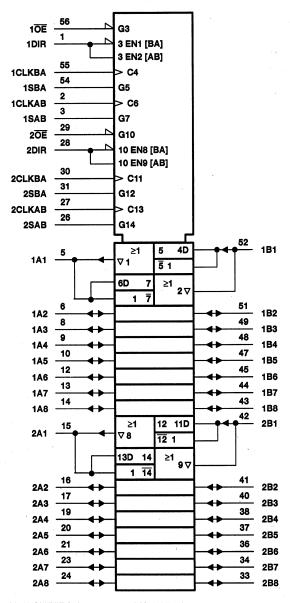


Figure 1. Bus-Management Functions



SCBS149C - JULY 1994 - REVISED JULY 1995

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic) 10E _56 1DIR -1 1CLKBA -1SBA ______ 1CLKAB _2 1SAB ______ One of Eight Channels 1D 1A1 ____ <u>52</u> 1B1 1D - C1 To Seven Other Channels 2DIR -30 2CLKBA 31 2SBA -26 2SAB -One of Eight Channels 1D 42 2B1 1D > C1 To Seven Other Channels



SCBS149C - JULY 1994 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0	
Input voltage range, V _I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, VO (see Note 1)	–0.5 V to 7 V
Current into any output in the low state, Io: SN54LVT16646	96 mA
SN74LVT16646	
Current into any output in the high state, IO (see Note 2): SN54LVT16646	48 mA
SN74LVT16646	64 mA
Input clamp current, I _{IK} (V _I < 0)	50 mA
Output clamp current, I _{OK} (V _O < 0)	50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	
DL package	1.4 W
Storage temperature range, T _{stg} –6	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			SN54LV	T16646	SN74LV	/T16646	UNIT
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	٧
VIH	High-level input voltage		2		2		٧
VIL	Low-level input voltage			0.8		0.8	٧
VI	Input voltage			^{్ట్ 5.5}		5.5	٧
ЮН	High-level output current		۵.	* –24		-32	mA .
lOL	Low-level output current		Š	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	I &	10		10	ns/V
TA	Operating free-air temperature		ື−55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SCBS149C - JULY 1994 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS				4LVT16	546	SN74LVT16646			UNIT
PANAMETER	'	EST CONDITIONS		MIN	TYPT	MAX	MIN	TYP	MAX	ONII
VIK	$V_{CC} = 2.7 \text{ V},$	l _l = -18 mA				-1.2			-1.2	٧
	$V_{CC} = MIN \text{ to MAX}^{\ddagger}$,	I _{OH} = -100 μA		VCC-C	.2		VCC-C).2		
V	$V_{CC} = 2.7 \text{ V},$	I _{OH} = -8 mA		2.4			2.4			v
VOH	V _{CC} = 3 V	I _{OH} = - 24 mA		2						'
	ACC = 2 A	I _{OH} = -32 mA					2			
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
\ \v		I _{OL} = 16 mA				0.4			0.4	ν
VOL	V 2V	I _{OL} = 32 mA			0.5			0.5	l v	
	V _{CC} = 3 V	I _{OL} = 48 mA			0.55					
		I _{OL} = 64 mA						0.55		
	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	Control innuts		7.5	* ±1			±1	
	$V_{CC} = 0$ or MAX ‡ ,	V _I = 5.5 V	Control inputs		8	10			10	
l ₁		V _I = 5.5 V			35	20			20	μА
	V _{CC} = 3.6 V	V _I = V _{CC}	A or B ports§		ð	5			5	
		V _I = 0		2	<u> </u>	-10			-10	
loff	$V_{CC} = 0$,	$V_1 \text{ or } V_0 = 0 \text{ to } 4.5$	V	~					±100	μА
lia i n	V _{CC} = 3 V	V _I = 0.8 V	A or B ports	75			75			μА
l(hold)	ACC = 2 A	V _I = 2 V	A or B ports	-75			-75			μА
lozh	V _{CC} = 3.6 V,	V _O = 3 V				1			1	μA
IOZL	V _{CC} = 3.6 V,	V _O = 0.5 V				-1			-1	μА
	V 00V		Outputs high			0.12			0.12	
Icc	V _{CC} = 3.6 V, V _I = V _{CC} or GND	$I_{O}=0,$	Outputs low			5			5	mA
			Outputs disabled			0.12			0.12	
∆lcc¶	V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or		- 0.6 V,			0.2			0.2	mA
Ci	V _I = 3 V or 0				3.5			3.5		рF
C _{io}	V _O = 3 V or 0				12			12		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. § Unused pins at V_{CC} or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SCBS149C - JULY 1994 - REVISED JULY 1995

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

			SN54LVT16646 SN74LVT16646					UNIT			
			V _{CC} = 3.3 V ± 0.3 V V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V				
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	150	,S0	150	0	150	0	150	MHz
tw	Pulse duration, CLK high or low		3.3		<i>Д</i> ₹ 3.3		3.3		3.3		ns
	Setup time,	Data high	1.3	É	1.4		1.3		1.4		
^t su	A or B before CLKABT or CLKBAT	Data low	2.4	72,	3		2.4		3		ns
Hold time,		Data high	0.5	ŶĊ.	0		0.5		0		
^t h	A or B after CLKABT or CLKBAT Data low	Data low	0.6	Q.	0.5		0.5		0.5		ns

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 2)

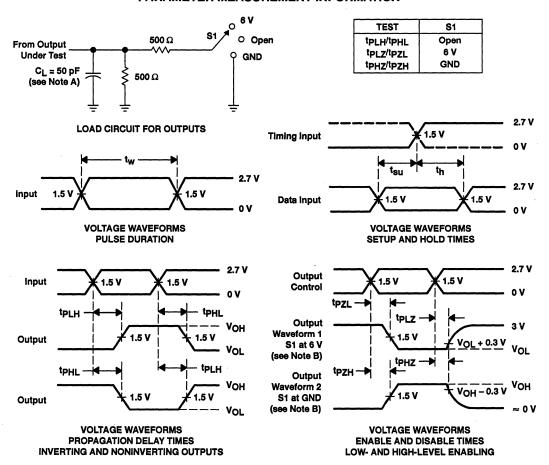
			SN54LV	T16646			SN7	4LVT16	646			
PARAMETER	FROM (INPUT)		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V			± 0.3 V	V	V _{CC} =	2.7 V	UNIT
		,	MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
f _{max}			150				150					MHz
^t PLH	CLKBA or	A or B	1.8	6		6.9	1.8	3.8	5.7		6.7	ns
t _{PHL}	CLKAB	ζ σ σ	2.1	5.9		6.6	2.1	3.9	5.7		6.5	115
^t PLH	A or B	B or A	1.3	4.9	44.	5.6	1.3	3	4.7		5.4	ns
tPHL	AUID	B 01 X	1	4.8	34	5.8	1	3.1	4.7		5.6	. 115
^t PLH	SBA or SAB‡	A or B	1.4	6.4	29	7.4	1.4	4	6.2		7.2	ns
^t PHL	SDA OF SABT	7015	1.4	6.4	٧,	7.4	1.4	4.3	6.2		7.2	113
^t PZH	ŌĒ	A or B	1	5.7	,	7.4	1	3	5.4		6.4	ns
tPZL	OE	AUIB	1	,6 }6		7.5	1	3.1	5.6		6.5	118
tPHZ	ŌĒ	A or B	2.3	₡6.7		7.1	2.3	4.6	6.5		6.9	ns
tPLZ	OE .	AUID	2.2	6		6.5	2.2	4.5	5.8		5.9	115
^t PZH	DIR	A or B	1	5.9		7.7	1	3.3	5.7		6.7	20
^t PZL	DIR	AUID	. 1.2	5.9		7.3	1.2	3.5	5.8		6.7	ns
tPHZ	DIR	A or B	1.7	7.3		8.5	1.7	4.7	7.2		8.3	no
[†] PLZ	DIR	AUIB	1.5	7.8		7.4	1.5	4.9	6.6		7.2	ns

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[‡] These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

SCBS149C - JULY 1994 - REVISED JULY 1995

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

SCBS150D - JULY 1994 - REVISED FEBRUARY 1996

 State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power 	SN54LVT16652 WD PACKAG SN74LVT16652 DGG OR DL PAC (TOP VIEW)				
Dissipation	10EAB [1	56 1 0EBA			
 Members of the Texas Instruments 	1CLKAB []2	55 1 1CLKBA			
<i>Widebus</i> ™ Family	1SAB [] 3	54 1 1SBA			
 Support Mixed-Mode Signal Operation (5-V 	GND II4	53 GND			
Input and Output Voltages With 3.3-V V _{CC})	1A1 []5	52 1 1B1			
Support Unregulated Battery Operation	1A2 1 6	51 1B2			
Down to 2.7 V	V _{CC} 17	50 V _{CC}			
Typical V _{OLP} (Output Ground Bounce)	1A3 [] 8	49 1 1B3			
$< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V}, T_A = 25^{\circ}\text{C}$	1A4 []9	48 1B4			
	1A5 [] 10	47 1 1B5			
ESD Protection Exceeds 2000 V Per MIL STD 9930 Method 2015; Exceeds	GND [] 11	46 ND			
MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model	1A6 🛮 12	45 [] 1B6			
(C = 200 pF, R = 0)	1A7 🛮 13	44 [] 1B7			
	1A8 🛮 14	43 [] 1B8			
 Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17 	2A1 🚺 15	42 2B1			
	2A2 🛚 16	41 2B2			
Bus-Hold Data Inputs Eliminate the Need	2A3 🛛 17	40 🛘 2B3			
for External Pullup Resistors	GND [] 18	39] GND			
Support Live Insertion	2A4 🛚 19	38 🛘 2B4			
 Distributed V_{CC} and GND Pin Configuration 	2A5 🛚 20	37] 2B5			
Minimizes High-Speed Switching Noise	2A6 🛚 21	36 [] 2B6			
Flow-Through Architecture Optimizes	V _{CC}] ²²	35 V _{CC}			
PCB Layout	2A7 []23	34] 2B7			
Package Options Include Plastic 300-mil	2A8 []24	33] 2B8			
Shrink Small-Outline (DL) and Thin Shrink	GND [] 25	32] GND			
Small-Outline (DGG) Packages and 380-mil	2SAB [26	31 2SBA			
Fine-Pitch Ceramic Flat (WD) Package	2CLKAB [27	30 2 2CLKBA			
Using 25-mil Center-to-Center Spacings	20EAB [28	29 20EBA			

description

The 'LVT16652 are 16-bit bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary output-enable (OEAB and OEBA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT16652.

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SCBS150D - JULY 1994 - REVISED FEBRUARY 1996

description (continued)

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration, each output reinforces its input. When all other data sources to the two sets of bus line are at high impedance, each set of bus lines remains at its last level configuration.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN74LVT16652 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16652 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVT16652 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

INPUTS						DATA	\	OPERATION OR FUNCTION		
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION		
L	Н	H or L	H or L	Х	Х	Input	Input	Isolation		
L	н	1	1	X	X	Input	input	Store A and B data		
×	Н	1	H or L	Х	X	Input	Unspecified [‡]	Store A, hold B		
н	Н	1	1	x ‡	X	Input	Output	Store A in both registers		
L	X	H or L	1	х	Х	Unspecified [‡]	Input	Hold A, store B		
L	L	1	1	Х	X ‡	Output	Input	Store B in both registers		
L	L	X	X	. X	L	Output	Input	Real-time B data to A bus		
L	L	X	H or L	X	Н	Output	Input	Stored B data to A bus		
н	н	X	Х	L	X	Input	Output	Real-time A data to B bus		
Н	Н	H or L	X	Н	X	Input	Output	Stored A data to B bus		
н	L	H or L	H or L	Н	Н	Output	Output	Stored A data to B bus and stored B data to A bus		

[†] The data output functions may be enabled or disabled by a variety of level combinations at OEAB or OEBA. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

Select control = H; clocks must be staggered in order to load both registers.

[‡] Select control = L; clocks can occur simultaneously.

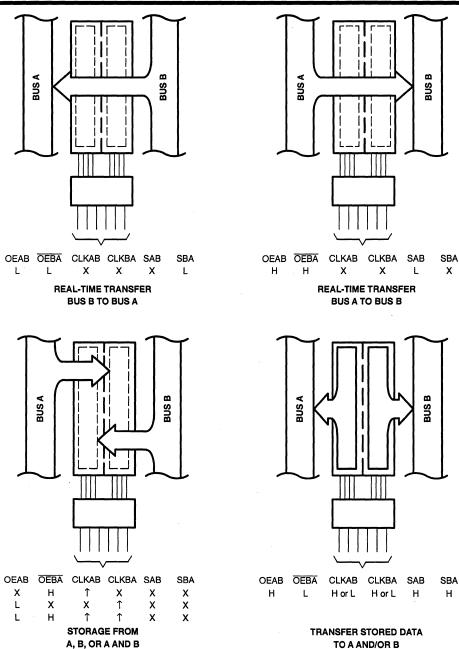
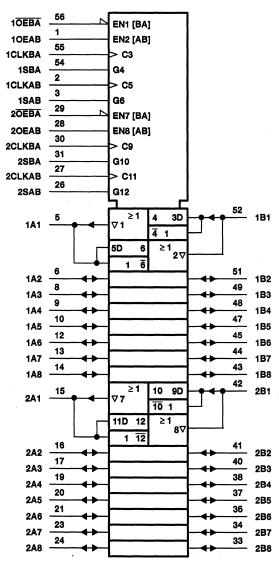


Figure 1. Bus-Management Functions



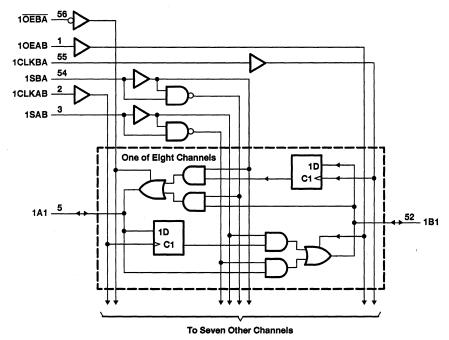
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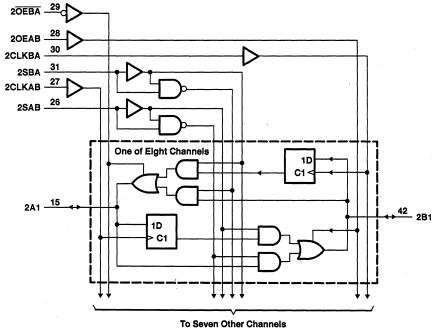
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)







SCBS150D - JULY 1994 - REVISED FEBRUARY 1996

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5 \	/ to 4.6 V
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1)0.5	
Current into any output in the low state, Io: SN54LVT16652	
SN74LVT16652	120 IIIA
Current into any output in the high state, IO (see Note 2): SN54LVT16652	. 48 mA
SN74LVT16652	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, $I_{OK}(V_O < 0)$	-50 mA
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): DGG package	
DL package	
Storage temperature range. Teta ——65°C	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			SN54LV	T16652	SN74LV	UNIT	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2		2		٧
VIL	Low-level input voltage			0.8		0.8	٧
VI	Input voltage			5.5		5.5	٧
ЮН	High-level output current			-24		-32	mA
lOL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



SCBS150D - JULY 1994 - REVISED FEBRUARY 1996

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS				SN54LVT16652			SN74LVT16652			
PARAMETER					TYPT	MAX	MIN	TYPT	MAX	UNIT	
VIK	V _{CC} = 2.7 V,	l _j = -18 mA				-1.2			-1.2	V	
,	$V_{CC} = MIN \text{ to } MAX^{\ddagger},$	V _{CC} -C).2		V _{CC} -0	.2					
	$V_{CC} = 2.7 \text{ V},$	$C = 2.7 \text{ V}, \qquad I_{OH} = -8 \text{ mA}$					2.4			V	
VOH	V _{CC} = 3 V	I _{OH} = -24 mA		2						V	
		I _{OH} = -32 mA					2				
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2	٧	
	VCC = 2.7 V	I _{OL} = 24 mA			0.5			0.5			
VOL		I _{OL} = 16 mA				0.4			0.4		
VOL	V00 2 V	I _{OL} = 32 mA				0.5			0.5		
	V _{CC} = 3 V	I _{OL} = 48 mA				0.55					
		I _{OL} = 64 mA				-			0.55	1	
	$V_{CC} = 3.6 \text{ V},$	V _I = V _{CC} or GND	Control innuts			±1			±1	μА	
	$V_{CC} = 0$ or MAX^{\ddagger} ,	V _I = 5.5 V	Control inputs			10			10		
11	V _{CC} = 3.6 V	V _I = 5.5 V				20			20		
		VI = VCC	A or B ports§			5			5		
		V _I = 0	<u>.</u>			-10			-10		
loff	$V_{CC} = 0$,	$V_1 \text{ or } V_0 = 0 \text{ to } 4.5$	V						±100	μА	
II(hold)	V _{CC} = 3 V	V _I = 0.8 V	A or B ports	75			. 75			μА	
		V _I = 2 V		-75			-75				
lozh	$V_{CC} = 3.6 \text{ V},$	V _O = 3 V				1			1	μΑ	
lozL	V _{CC} = 3.6 V,	V _O = 0.5 V				-1			-1	μΑ	
Icc	V _{CC} = 3.6 V, V _I = V _{CC} or GND			Outputs high			0.1			0.1	
			Outputs low			5			5	mA	
	11 - 100 or and		Outputs disabled			0.1			0.1		
∆ICC [¶]	V_{CC} = 3 V to 3.6 V, One input at V_{CC} - 0.6 V, Other inputs at V_{CC} or GND				0.2			0.2	mA		
C _i	V _I = 3 V or 0				3.5			3.5		pF	
Cio	V _O = 3 V or 0				12			12		pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. § Unused pins at VCC or GND

 $[\]P$ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN74LVT16835 3.3-V ABT 18-BIT UNIVERSAL BUS DRIV WITH 3-STATE OUTPUTS

SCBS309C - MARCH 1994 - REVISED JULY 1995

 State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V 	DGG OR DL PACKAGE (TOP VIEW)				
Operation and Low-Static Power Dissipation	NC[1	56] GND			
Member of the Texas Instruments	NC 2 Y1 3	55 NC 54 A1			
<i>Widebus</i> ™ Family	GND 4	53 GND			
 Supports Mixed-Mode Signal Operation 	Y2 5	52 A2			
(5-V Input and Output Voltages With 3.3-V V _{CC})	Y3 🛮 6	51 🛚 A3			
	V _{CC} ∏ 7	50 V _{CC}			
Supports Unregulated Battery Operation	Y4 	49 🛛 A4			
Down to 2.7 V	Y5 ∐ 9	48 [] A5			
 Typical V_{OLP} (Output Ground Bounce) 	Y6 ☐ 10	47 🛮 A6			
< 0.8 V at V _{CC} = 3.3 V, T _A = 25°C	GND 11	46 GND			
Bus-Hold Data Inputs Eliminate the Need	Y7 🛮 12 Y8 🖟 13	45 A7 44 A8			
for External Pullup Resistors	Y8U 13 Y9U 14	44 JI A8 43 II A9			
Supports Live Insertion	Y10 15	43 J A9 42 J A10			
 Distributed V_{CC} and GND Pin Configuration 	Y11 16	41 A11			
Minimizes High-Speed Switching Noise	Y12 17	40 A12			
Flow-Through Architecture Optimizes	GND 1 18	39 GND			
PCB Layout	Y13 19	38 A13			
 Package Options Include Plastic 300-mil 	Y14 20	37 A14			
Shrink Small-Outline (DL) and Thin Shrink	Y15 21	36 🛚 A15			
Small-Outline (DGG) Packages Using 25-mil	V _{CC} []22	35 🛚 V _{CC}			
Center-to-Center Spacings	Y16 23	34 🛮 A16			
	Y17 🛮 24	33 🛭 A17			
description	GND 🛮 25	32]] GND			
The SN74LVT16835 is an 18-bit universal bus	Y18[]26	31 🛛 A18			
driver designed for low-voltage (3.3-V) V _{CC}	ŌĒ [] 27	30 CLK			
operation, but with the capability to provide a TTL	LE[[28	29]] GND			

NC - No internal connection

Data flow from A to Y is controlled by the output-enable (OE) input. This device operates in the transparent mode when the latch-enable (LE)

interface to a 5-V system environment.

input is high. The A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of the clock. When $\overline{\sf OE}$ is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16835 is available in Tl's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the input/output (I/O) pins and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74LVT16835 is characterized for operation from -40°C to 85°C.

Widebus is a trademark of Texas Instruments Incorporated.



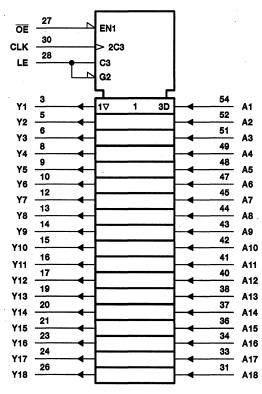
SCBS309C -		

IN	CT	10	м	TA	01	=

	OUTPUT			
ŌĒ	LE	CLK	Α	Υ
Н	Х	Х	Х	Z
L	Н	Х	L	L, '
L	Н	X	Н	н
L	L	1	L	L
L	L	1	Н	н
L	L	Н	Х	Y ₀ †
L	L	L	Χ	Y ₀ ‡

[†] Output level before the indicated steady-state input conditions were established, provided that CLK was high before LE went low

logic symbol§

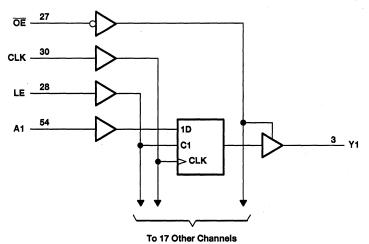


[§] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

[‡] Output level before the indicated steady-state input conditions were established

SCBS309C - MARCH 1994 - REVISED JULY 1995

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V _O (see Note 1)	0.5 V to 7 V
Current into any output in the low state, IO	128 mA
Current into any output in the high state, I _O (see Note 2)	64 mA
Input clamp current, $I_{ K }(V_{ I } < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Operating free-air temperature range, T _A	40°C to 85°C
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

SN74LVT16835 3.3-V ABT 18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

SCBS309C - MARCH 1994 - REVISED JULY 1995

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage		2		٧
VIL	Low-level input voltage			0.8	٧
VI	Input voltage			5.5	٧
ЮН	High-level output current			-32	mA
loL	Low-level output current	. `		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	7	EST CONDITIONS		MIN	TYP†	MAX	UNIT
v_{iK}		$V_{CC} = 2.7 \text{ V},$	lj = -18 mA				-1.2	V
		V _{CC} = MIN to MAX [‡] ,	I _{OH} = -100 μA		VCC-C	.2		
Vон		V _{CC} = 2.7 V,	IOH = - 8 mA		2.4			V
	5.	V _{CC} = 3 V	I _{OH} = -32 mA		2	,		
		V _{CC} = 2.7 V	I _{OL} = 100 μA	,			0.2	
		VCC = 2.7 V	I _{OL} = 24 mA				0.5	
VOL			I _{OL} = 16 mA				0.4	V
		V _{CC} = 3 V	I _{OL} = 32 mA				0.5	
			I _{OL} = 64 mA				0.55	
		$V_{CC} = 0$ or MAX ‡ ,	V _I = 5.5 V				10	
	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND				±1	
11			VI = VCC				1	→ '‴`
	A inputs	V _{CC} = 3.6 V	V _I = 5.5 V				20	
			V _I = 0			-5		
loff		V _{CC} = 0,	V _I or V _O = 0 to 4.5 V				±100	μА
1.0	A inpute	V _{CC} = 3 V	V _I = 0.8 V		75			
l(hold)	A inputs	ACC = 2 A	V _I = 2 V		-75			μΑ
lozh		V _{CC} = 3.6 V,	V _O = 3 V				1	μА
lozL		V _{CC} = 3.6 V,	V _O = 0.5 V				-1	μА
				Outputs high			0.12	
Icc .		V _{CC} = 3.6 V, V _I = V _{CC} or GND	$I_{O}=0$,	Outputs low		5		mA
ľ		AL = ACC OLGIAD		Outputs disabled	0		0.12	1
ΔICC§		V _{CC} = 3 V to 3.6 V, Other inputs at V _{CC} or GND	One input at V _{CC} – 0.6 V,				0.2	mA
Ci	Control inputs	V _I = 3 V or 0				3.5		nE
٩	Data pins	41 = 0 4 01 0				4.5		pF
Co		V _O = 3 V or 0				11		pF

 $^{^{\}dagger}$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.



[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

3.3-V ABT 18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS SCBS309C - MARCH 1994 - REVISED JULY 1995

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	İ
fclock	Clock frequency		0	150	0	125	MHz
Poles done	LE high	3.3		3.3			
١w	t _w Pulse duration	CLK high or low	3.3		3.3		ns
		Data before CLK↑	1.6		2.1		
t _{su}	Setup time	Data before LE↓, CLK high	2.6		1.9		ns
		Data before LE↓, CLK low	2		1.3		ĺ
		Data after CLK↑	2		2.1		
^t h	t _h Hold time	Data after LE↓	0.9		1.2		ns

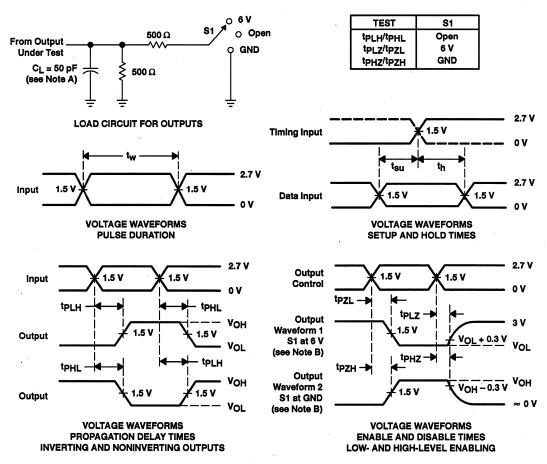
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM TO	то	то Усс		V _{CC} = 3.3 V ± 0.3 V			UNIT	
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYPT	MAX	MIN	MAX	UNII	
fmax			150			150		MHz	
^t PLH	A	V	1.7	3	5.4		6.8	ne	
^t PHL	1 ^		1.6	3.2	5.9		7.7	ns	
tPLH	LE	Y	2.3	4	7		8.5	ns	
^t PHL			2.7	4.3	7.9		9.7	115	
^t PLH	0114	Y	2.5	4.1	7.9		9.2	ns	
^t PHL	CLK	-K	3.5	5.4	8.9		10.4	115	
^t PZH	. OE	Y	1.2	3	5		5.9	ns	
^t PZL	OE	1 1	1.5	3	5.8		6.9	115	
^t PHZ	ŌĒ	OF V	Y	2.7	4.6	7.4		8.3	ns
^t PLZ		T	2.8	4.7	6.7		7.2	118	

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

SCBS309C - MARCH 1994 - REVISED JULY 1995

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVT16952, SN74LVT16952 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS151C - MAY 1992 - REVISED JULY 1995

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
 Members of the Toyon Instruments
- Members of the Texas Instruments
 Widebus™ Family
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes
 PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVT1695	2 WD PAG	CKAGE			
SN74LVT16952	DGG OR DL	PACKAGE			
(TOP VIEW)					

Г	$-\tau\tau$	\neg	
1OEAB	1	56	1 OEBA
1CLKAB 🛛			1CLKBA
1CLKENAB	3	54	1CLKENBA
GND 🗓	4	53	GND
1A1 []		52] 1B1
1A2 🗓	6	51] 1B2
v _{cc} 🗓	7	50] v _{cc}
1A3 🔲	8	49] 1B3
1A4 🗓] 1B4
1A5 🛛] 1B5
GND 🛛] GND
1A6 🛛] 1B6
1A7 🗓] 1B7
1A8 🛛] 1B8
2A1 🚺] 2B1
2A2 🛛		41] 2B2
2A3 🛛			2B3
GND 🗓] GND
2A4 🛛] 2B4
2A5 🛛			2B5
2A6 🛭	21	36] 2B6
v _{cc} 🗓	22] v _{cc}
2A7 🗓	23] 2B7
2A8 🗓] 2B8
GND []		32	GND
2CLKENAB	26	31	2CLKENBA
2CLKAB []		30	2CLKBA
2 OEAB [28	29	2 OEBA

description

The 'LVT16952 are 16-bit registered transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable (CLKENAB or CLKENBA) input is low. Taking the output-enable (OEAB or OEBA) input low accesses the data on either port.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16952 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

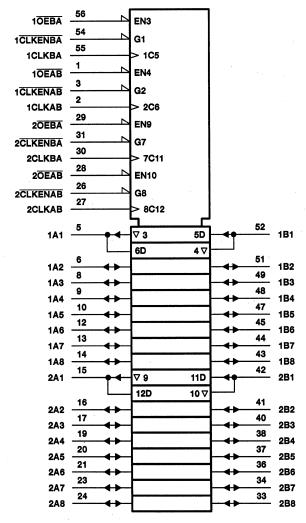
Widebus is a trademark of Texas Instruments Incorporated.

SCBS151C - MAY 1992 - REVISED JULY 1995

description (continued)

The SN54LVT16952 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16952 is characterized for operation from –40°C to 85°C.

logic symbolt



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



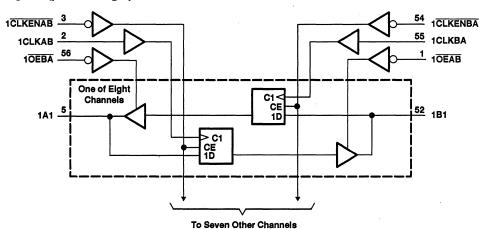
SCBS151C - MAY 1992 - REVISED JULY 1995

FUNCTION TABLET

	OUTPUT					
CLKENAB	CLKAB	OEAB	Α	В		
Н	Х	L	X	B ₀ ‡		
х	L	L	Х	В ₀ ‡ В ₀ ‡		
L	1	L	L	L		
L	1	L	Н	н		
Х	X	н	Χ	z		

[†] A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENBA, CLKBA, and OEBA.

logic diagram (positive logic)



2CLKENAB
2CLKAB
2OEBA
2OEBA
2OEBA
2OEBA
2OEBA
2OEBA
2OEBA
2OEBA
2OEBBA
2OEBBA
2OEBBA
2OEBBA
2OEBBA
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[‡]Level of B before the indicated steady-state input conditions were established

SN54LVT16952, SN74LVT16952 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS151C - MAY 1992 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, Vo (see Note 1)	
Current into any output in the low state, Io: SN54LVT16952	96 mA
SN74LVT16952	128 mA
Current into any output in the high state, IO (see Note 2): SN54LVT16952	48 mA
SN74LVT16952	64 mA
Input clamp current, I _{IK} (V _I < 0)	50 mA
Output clamp current, I_{OK} ($V_O < 0$)	50 mA
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current flows only when the output is in the high state and VO > VCC.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

	·		SN54LV	T16952	SN74LV	UNIT	
			MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	2.7	3.6	V
٧ _{IH}	High-level input voltage		2	<i>Ĉ</i>	2		٧
V _{IL}	Low-level input voltage			€ 0.8		0.8	٧
VI	Input voltage			رُ ^{2,5} 5.5		5.5	V
ЮН	High-level output current		٥.	<u>~ -24</u>		-32	mA
loL	Low-level output current		Ŝ	48		. 64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	J.S.	10		10	ns/V
TA	Operating free-air temperature		~55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN54LVT16952, SN74LVT16952 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS SCBS151C - MAY 1992 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS			SNS	54L VT 16	952	SN7	4L V T16	952	LINUT
PARAMETER	11	EST CONDITIONS		MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
VIK	V _{CC} = 2.7 V,	l _l = –18 mA				-1.2			-1.2	٧
	V _{CC} = MIN to MAX [‡] ,	I _{OH} = -100 μA		VCC-C).2		VCC-0	.2		
V	V _{CC} = 2.7 V,	IOH = - 8 mA	2.4			2.4			l v	
VOH	V _{CC} = 3 V	IOH = - 24 mA		2						,
	ACC = 2 A	IOH = -32 mA					2			
	V _{CC} = 2.7 V	I _{OL} = 100 μA				0.2			0.2	
	VCC = 2.7 V	I _{OL} = 24 mA				0.5			0.5	
Vo		I _{OL} = 16 mA				0.4			0.4	ν
VOL	V _{CC} = 3 V	I _{OL} = 32 mA				0.5			0.5	'
	ACC = 2 A	I _{OL} = 48 mA				0.55				
		IOL = 64 mA				0.55		0.55		
	$V_{CC} = 3.6 \text{ V},$	V _I = V _{CC} or GND	Control			∜ ±1			±1	
	$V_{CC} = 0$ or MAX [‡] ,	V _I = 5.5 V	inputs		K.	10			10	
lj .	V _{CC} = 3.6 V	V _I = 5.5 V	A or B ports§		Z.	20			20	μА
		V _I = V _{CC}			S	1			1	
		V _i = 0			გა	- 5			- 5	
l _{off}	$V_{CC} = 0$,	V _I or V _O = 0 to 4.5 V		Q ^N					±100	μΑ
lia in	V _{CC} = 3 V	V _I = 0.8 V	A or B ports	75			75			μА
l(hold)	vCC = 3 v	V ₁ = 2 V	A of B ports	-75			-75			μζ
lozh	V _{CC} = 3.6 V,	V _O = 3 V				1			1	μА
lozl	$V_{CC} = 3.6 \text{ V},$	V _O = 0.5 V				-1			-1	μΑ
			Outputs high			0.12			0.12	
lcc	$V_{CC} = 3.6 \text{ V},$	$I_{O} = 0$,	Outputs low			5			5	mA
100	V _I = V _{CC} or GND		Outputs disabled			0.12			0.12	III/A
ΔlCC¶	V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND					0.2			0.2	mA
Ci	V _I = 3 V or 0				4			4		pF
Cio	V _O = 3 V or 0				13			13		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at VCC or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SN54LVT16952, SN74LVT16952 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS151C - MAY 1992 - REVISED JULY 1995

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				SN54LVT16952			SN74LVT16952				
				V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		3.3 V 3 V	V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	150	.0	150	0	150	0	150	MHz
	Pulse duration	CLKEN high	3.3		_3\$:3		3.3		3.3		ns
tw		CLK high or low	3.3		₹ 3.3		3.3		3.3		
	Oakum tima	A or B before CLK	2.1		2.9		2.1		2.9		
^t su ³	Setup time	CLKEN before CLK	1.2		1.6		1.2		1.6		ns
. .	Hold time	A or B after CLK	0.7	\O_1	0.7		0.7		0.7		
^t h		CLKEN after CLK	1.4	Q.	1.5		1.4		1.5		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

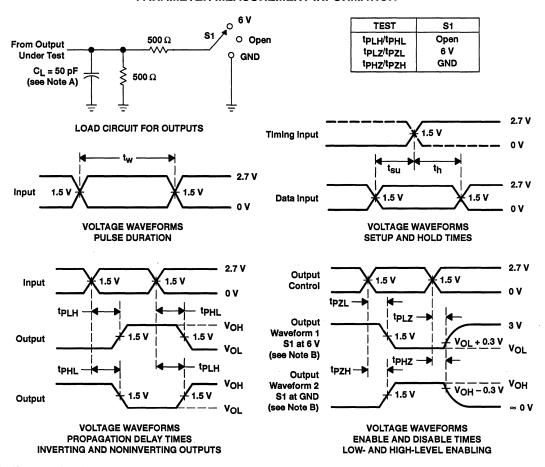
				SN54LV	T16952			SN7	4LVT16	952		
PARAMETER	FROM (INPUT)	TO (OUTPUT)	1 -00		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V	V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	TYPT	MAX	MIN	MAX	
fmax		ı	150		1,60		150			150		MHz
^t PLH	CLKBA or CLKAB	A or B	2	5.9	12	7.4	2	3.4	5.8		7.1	
t _{PHL}			2	6	ŞE.	7	2	3.4	5.8		6.9	ns
^t PZH	OEBA or	A or B	1	6.3	•	7.3	1	2.7	5.6		6.7	no
tPZL	ŌĒĀB	AUID	1.2	કહે	,	8.2	1.2	2.7	6.5		8	ns
tPHZ t	OEBA or	A or B	2.3	Ø ⁰ 7		7.6	2.3	3.9	6.3		6.9	20
^t PLZ	OEAB .	7016	2.2	≪ 5.8		6	2.2	3.9	5.1		5.3	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6-112

SCBS151C - MAY 1992 - REVISED JULY 1995

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

General Information	1
ALB Widebus™	2
ALVC Widebus™	3
LVT Octals	4
LVTZ Octals: Power Up and 3 State	5
LVT Widebus™	6
LVT JTAG/IEEE 1149.1	7
LVC MSI and Octals	8
LVC Widebus™	9
LV MSI and Octals	10
GTL Transceivers and Backplane Drivers	11
Application Reports	12
Characteristics Information	13
Mechanical Data	14

LVT JTAG/IEEE 1149.1

Features

- Compatibility with IEEE Standard 1149.1-1990 (JTAG) test access port (TAP) and boundary-scan architecture
- Effectively place a unique digital test probe on each signal pin
- TI extensions beyond 1149.1 required instructions.
 - Parallel Signature Analysis (PSA)
 - Pseudo-Random Pattern Generation (PRPG)
- EPIC-IIB™ submicron process with special low-voltage enhancements
- Expanded V_{CC} range from 2.7 V to 3.6 V
- 18-bit and 20-bit UBT™ architectures
- Widebus[™] functions available in space-saving EIAJ TSSOP, JEDEC SSOP, and EIAJ TQFP fine-pitch surface-mount packaging
- Maximum propagation delays < 6 ns
- Bus-hold circuitry at I/O signal pins
- Series-resistor options on B-port ('LVT182 series)
- Members of a broad family of Texas Instruments boundary-scan logic

Benefits

- Adherence to well-established industry standard, ensuring access to a board range of supporting software and test equipment
- Improved test access into complex circuit board assemblies for board manufacturing test and design verification/debug
- Built-in self-test features provide near-at-speed test capability for improved test flexibility, throughput, and effectiveness
- High-performance, low-power, high-drive, low-noise equivalents of standard LVT buffers/drivers/transceivers offering system and test designers flexible integration options
- Advanced integration, as one UBT™ can replace most common bus-interface logic
- Increased functional and component density supporting tight board space budgets
- Speed equivalency to standard LVT product, resulting in minimal performance penalty for boundary-scan implementation
- Reduced component count by eliminating need for external tie-off resistors
- Reduce component count by eliminating need for external line-termination resistors
- Compatibility with a full line of scan-support functions, including test bus controllers and addressable-scan ports, providing a complete solution for boundary-scan-based system testing

Today's designs are based on evermore complex ICs, fine-pitch packaging, and denser board layouts. These factors limit test access and greatly complicate traditional methods of functional and in-circuit manufacturing test and design verification/debug. The IEEE 1149.1 (JTAG) boundary-scan test standard was created to address these issues. TI has taken a leading role in the industry in supplying logic that integrates IEEE 1149.1 (JTAG) test methods.

Features and benefits of TI LVT boundary-scan logic products are on the facing page and a list of available LVT scannable bus-interface devices is presented below. Data sheets for the entire family are in the 1994 Boundary-Scan Logic/IEEE 1149.1 (JTAG) Data Book, lit# SCTD002. Please contact your local TI sales representative or TI authorized distributor for copies.

The following table lists LVT IEEE 1149.1 (JTAG) devices currently available or planned. Customers interested in learning more about TI's plans for these devices should contact the Advanced System Logic Marketing hotline at (903) 868-5202.

DEVICE		PIN COUNT	DESCRIPTION
SN54LVT18245	SN74LVT18245	56	18-bit bus transceiver
SN54LVT182245	SN74LVT182245	56	18-bit bus transceiver with series resistor option
	SN74LVT18502	64	18-bit universal bus transceiver
	SN74LVT182502	64	18-bit universal bus transceiver with series resistor option
	SN74LVT18504	64	20-bit universal bus transceiver
SN54LVT182504	SN74LVT182504	64	20-bit universal bus transceiver with series resistor option
SN54LVT18640	SN74LVT18640	56	18-bit inverting bus transceiver
SN54LVT182640	SN74LVT182640	56	18-bit inverting bus transceiver with series resistor option
SN54LVT18646	SN74LVT18646	64	18-bit transceiver and register
SN54LVT182646	SN74LVT182646	64	18-bit transceiver and register with series resistor option
SN54LVT18652	SN74LVT18652	64	18-bit transceiver and register
SN54LVT182652	SN74LVT182652	64	18-bit transceiver and register with series resistor option

General Information	1
ALB Widebus™	2
ALVC Widebus™	3
LVT Octals	4
LVTZ Octals: Power Up and 3 State	5
LVT Widebus™	6
LVT JTAG/IEEE 1149.1	7
LVC MSI and Octals	8
LVC Widebus™	9
LV MSI and Octals	10
GTL Transceivers and Backplane Drivers	11
Application Reports	12
Characteristics Information	13
Mechanical Data	14

Contents

		Page
SN74LVC00	Quadruple 2-Input Positive-NAND Gate	8-5
SN74LVC02	Quadruple 2-Input Positive-NOR Gate	8-9
SN74LVC04	Hex Inverter	8-13
SN74LVCU04	Hex Inverter	8-17
SN74LVC08	Quadruple 2-Input Positive-AND Gate	8-21
SN74LVC10	Triple 3-Input Positive-NAND Gate	8-25
SN74LVC14	Hex Schmitt-Trigger Inverter	8-29
SN74LVC32	Quadruple 2-Input Positive-OR Gate	
SN74LVC74	Dual Positive-Edge-Triggered D-Type Flip-Flop With Clear and Preset	8-37
SN74LVC86	Quadruple 2-Input Exclusive-OR Gate	8-43
SN74LVC112	Dual Negative-Edge-Triggered J-K Flip-Flop With Clear and Preset	8-47
SN74LVC125	Quadruple Bus Buffer Gate With 3-State Outputs	8-51
SN74LVC126	Quadruple Bus Buffer Gate With 3-State Outputs	8-55
SN74LVC137	3-Line to 8-Line Decoder/Demultiplexer With Address Latches	8-59
SN74LVC138	3-Line to 8-Line Decoder/Demultiplexer	8-63
SN74LVC139	Dual 2-Line to 4-Line Decoder/Demultiplexer	8-69
SN74LVC157	Quadruple 2-Line to 1-Line Data Selector/Multiplexer	8-73
SN74LVC158	Quadruple 2-Line to 1-Line Data Selector/Multiplexer	8-77
SN74LVC240	Octal Buffer/Driver With 3-State Outputs	8-81
SN74LVC241	Octal Buffer/Driver With 3-State Outputs	
SN74LVC244A	Octal Buffer/Driver With 3-State Outputs	8-89
SN74LVCH244	Octal Buffer/Driver With 3-State Outputs	
SN74LVC245A	Octal Bus Transceiver With 3-State Outputs	8-99
SN74LVCH245	Octal Bus Transceiver With 3-State Outputs	8-103
SN74LVC4245	Octal Bus Transceiver and 3.3-V to 5-V Shifter With 3-State Outputs	8-109
SN74LVC257	Quadruple 2-Line to 1-Line Data Selector/Multiplexer With 3-State Outputs	8-113
SN74LVC258	Quadruple 2-Line to 1-Line Data Selector/Multiplexer With 3-State Outputs	8-119
SN74LVC373A	Octal Transparent D-Type Latch With 3-State Outputs	8-123
SN74LVC374A	Octal Edge-Triggered D-Type Flip-Flop With 3-State Outputs	8-129
SN74LVC540	Octal Buffer/Driver With 3-State Outputs	8-135
SN74LVC541	Octal Buffer/Driver With 3-State Outputs	8-139
SN74LVC543	Octal Registered Transceiver With 3-State Outputs	8-143
SN74LVC544	Octal Registered Transceiver With 3-State Outputs	8-149
SN74LVC573A	Octal Transparent D-Type Latch With 3-State Outputs	8-153
SN74LVC574A	Octal Edge-Triggered D-Type Flip-Flop With 3-State Outputs	8-159
SN74LVC646	Octal Bus Transceiver and Register With 3-State Outputs	8-165
SN74LVC652	Octal Bus Transceiver and Register With 3-State Outputs	8-173
SN74LVC821	10-Bit Bus-Interface Flip-Flop With 3-State Outputs	8-181
SN74LVC823	9-Bit Bus-Interface Flip-Flop With 3-State Outputs	8-185

Contents

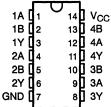
		Page
SN74LVC827	10-Bit Buffer/Driver With 3-State Outputs	8-191
SN74LVC828	10-Bit Buffer/Driver With 3-State Outputs	8-195
SN74LVC841	10-Bit Bus-Interface D-Type Latch With 3-State Outputs	8-199
SN74LVC843	9-Bit Bus-Interface D-Type Latch With 3-State Outputs	8-203
SN74LVC861	10-Bit Bus Transceiver With 3-State Outputs	8-207
SN74LVC863	9-Bit Bus Transceiver With 3-State Outputs	8-211
SN74LVC2952	Octal Bus Transceiver and Register With 3-State Outputs	8-215

SN74LVC00 QUADRUPLE 2-INPUT POSITIVE-NAND GATE

SCAS279B - JANUARY 1993 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per Mil-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE (TOP VIEW)



description

This quadruple 2-input positive-NAND gate is designed for 2.7-V to 3.6-V V_{CC} operation. The SN74LVC00 performs the Boolean functions $Y = \overline{A} \cdot \overline{B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

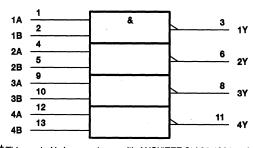
The SN74LVC00 is characterized for operation from -40°C to 85°C.

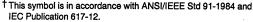
FUNCTION TABLE (each gate)

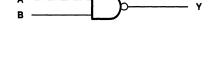
INP	UTS	OUTPUT
Α	В	Y
Н	Н	L
L	X	н
x	L	н

logic symbolt

logic diagram, each gate (positive logic)







EPIC is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS

SCAS279B - JANUARY 1993 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)	0.5 V to 6.5 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): D pa	
	or PW package 0.5 W
Storage temperature range, T _{stg}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V	Cumpliciality	Operating	2	3.6	V
VCC	Supply voltage	Data retention only	1.5		V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
VI	Input voltage		0	5.5	٧
۷o	Output voltage		0	VCC	٧
lau	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН	nigh-level output current	V _{CC} = 3 V		-24	MA
loi	Low-level output current	V _{CC} = 2.7 V		12	mA
IOL	Low-level output current	V _{CC} = 3 V		24	ША
T_A	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

SCAS279B - JANUARY 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} t	MIN TYP#	MAX	UNIT	
	l _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			
Vali	Jan. 10 mA	2.7 V	2.2		- v	
VOH	IOH = - 12 mA	3 V	2.4			
	I _{OH} = -24 mA	3 V	2.2			
	I _{OL} = 100 μA	MIN to MAX		0.2		
VOL	IOL = 12 mA	2.7 V		0.4	V	
	I _{OL} = 24 mA	3 V		0.55		
l ₁	V _I = 5.5 V or GND	3.6 V		±5	μА	
lcc	$V_1 = V_{CC}$ or GND, $I_0 = 0$	3.6 V		10	μА	
ΔlCC	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μА	
Ci	V _I = V _{CC} or GND	3.3 V	5		рF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	3.3 V 3 V	V _{CC} =	2.7 V	UNIT
		(114FO1)	(OUTPOT)	MIN	MAX	MIN	MAX	
I	^t pd	A or B	Y	• 1	6		7	ns
ſ	t _{sk(o)} §				1			ns

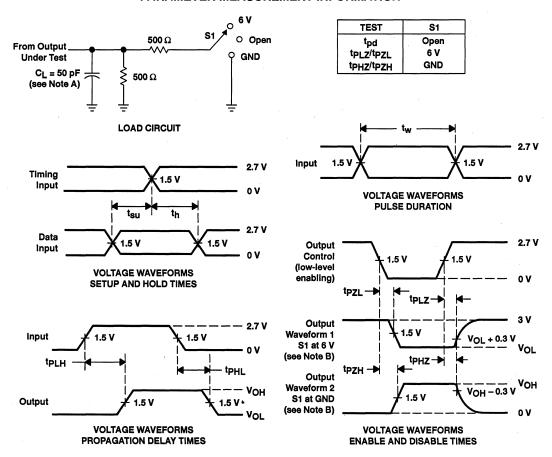
Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CO	TYP	UNIT		
Cpd	Power dissipation capacitance per gate		C _L = 50 pF,	f = 10 MHz	9.5	pF

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SN74LVC02 QUADRUPLE 2-INPUT POSITIVE-NOR GATE

SCAS280B - JANUARY 1993 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE (TOP VIEW)

1Y [1A [1B [2Y [2A [2B [2 3 4 5	U	12 11	V _C , 4Y 4B 4A 3Y 3B	2
2A [2B [3ND [6			3B 3A	

description

This quadruple 2-input positive-NOR gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC02 performs the Boolean functions $Y = \overline{A + B}$ or $Y = \overline{A} \bullet \overline{B}$ in positive logic.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

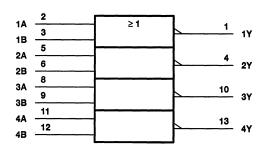
The SN74LVC02 is characterized for operation from -40°C to 85°C.

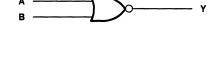
FUNCTION TABLE (each gate)

INP	UTS	OUTPUT			
Α	В	Y			
Н	Х	L			
×	Н	L			
L	L	Н			

logic symbolt

logic diagram, each gate (positive logic)





† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)	0.5 V to 6.5 V
Output voltage range, VO (see Notes 1 and 2)	. $-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): D package	1.25 W
DB or PW packa	ge 0.5 W
Storage temperature range, T _{stg}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V	Cumplicialtage	Operating	2	3.6	V
vcc	Supply voltage	Data retention only	1.5		٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
۷ _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
Vį	Input voltage		0	5.5	٧
Vo	Output voltage		0	VCC	٧
10	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН	migri-level output current	V _{CC} = 3 V		-24	IIIA
la.	Low-level output current	V _{CC} = 2.7 V		12	mA -
ŌL	Low-level output outrent	V _{CC} = 3 V		24	III/A
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

SN74LVC02 **QUADRUPLE 2-INPUT POSITIVE-NOR GATE**

SCAS280B - JANUARY 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} t	MIN TYP‡ MAX	UNIT
	IOH = -100 μA	MIN to MAX	V _{CC} -0.2	
V	la 10 mA	2.7 V	2.2] ,
VOH	I _{OH} = - 12 mA	3 V	2.4] '
	IOH = -24 mA	3 V	2.2]]
	I _{OL} = 100 μA	MIN to MAX	0.2	_ v .
v_{OL}	I _{OL} = 12 mA	2.7 V	0.4	
	I _{OL} = 24 mA	3 V	0.55	
11	V _I ≈ 5.5 V or GND	3.6 V	±5	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	10	μА
ΔlCC	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or Gi	ND 2.7 V to 3.6 V	500	μА
Ci	V _I = V _{CC} or GND	3.3 V	5	pF

Ter conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	3.3 V 3 V	V _{CC} =	2.7 _. V	UNIT
	(INPO1)	(001701)	MIN	MAX	MIN	MAX	1
t _{pd}	A or B	Y	1	6		7	ns
t _{sk(o)} §				1			ns

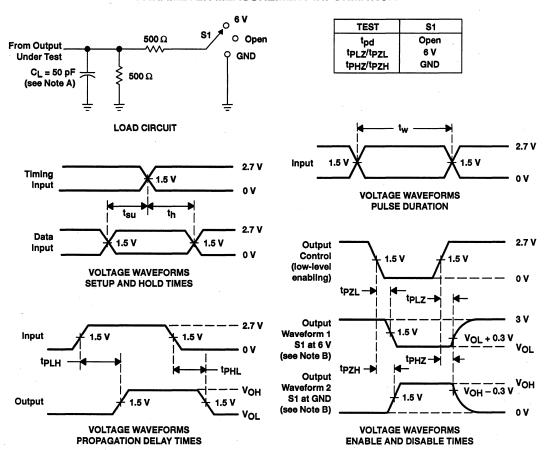
[§] Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
Cpd	Power dissipation capacitance per gate	C _L = 50 pF, f = 10 MHz	9.5	pF

 $[\]ddagger$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



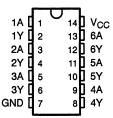
NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE (TOP VIEW)



description

This hex inverter contains six independent inverters designed for 2.7-V to 3.6-V V_{CC} operation. The SN74LVC04 performs the Boolean function $Y = \overline{A}$.

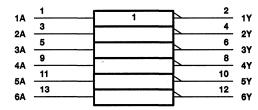
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC04 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each inverter)

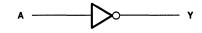
	100001111			
ı	INPUT	JT OUTPUT		
	A	Y		
	Н	L		
	L	Н		

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each inverter (positive logic)



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TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): D package
Storage temperature range, T _{stg} –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V	Supply voltage Operating Data retention only	Operating	2	3.6	V
VCC		Data retention only	1.5		V
٧ _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
۷ _I	Input voltage		0	5.5	٧
۷o	Output voltage		0	VCC	٧
lou	High-level output current	V _{CC} = 2.7 V		-12	mA
IOH	nigir-level output current	V _{CC} = 3 V		-24	IIIA
lo	Low-level output current	V _{CC} = 2.7 V		12	mA
lor	Low-level output current	V _{CC} = 3 V		24	IIIA.
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} t	MIN TYP‡	MAX	UNIT
	l _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
V	In., 10 mA	2.7 V	2.2		v
VOH	IOH = - 12 mA	3 V	2.4		v
	I _{OH} = -24 mA	3 V	2.2]
	I _{OL} = 100 μA	MIN to MAX		0.2	
VOL	I _{OL} = 12 mA	2.7 V		0.4	٧
	I _{OL} = 24 mA	3 V		0.55	
lμ	V _I = 5.5 V or GND	3.6 V		±5	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		10	μА
ΔlCC	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μА
Ci	V _I = V _{CC} or GND	3.3 V	5		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	3.3 V 3 V	V _{CC} =	2.7 V	UNIT
	(INPOT)	(001701)	MIN	MAX	MIN	MAX	
^t pd	A	Y	1	6		7	ns
tsk(o) [§]				1			ns

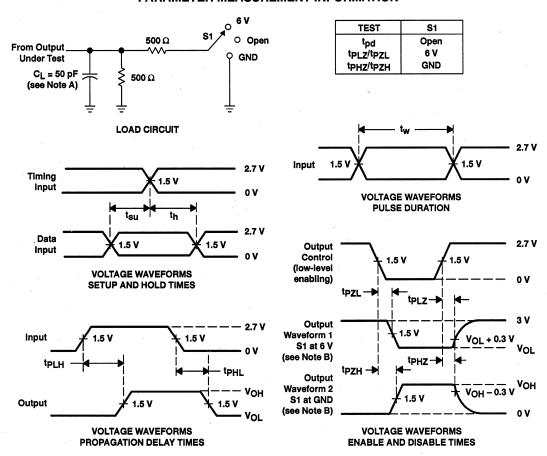
[§] Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C	od Power dissipation capacitance per inverter	C _L = 50 pF, f = 10 MHz	8	pF

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SCAS282B - JANUARY 1993 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883C. Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) **Packages**

D,	DB,	OR	P١	N	PΑ	CK.	AG
		πο	P١	VII	ΞW	0	

1A [1Y [1 2	U	14	þ	V _{CC}	
2A [3		12		6Y	
2Y [3A [4 5				5A 5Y	
3Y [GND [6 7		9 8	6	4A 4Y	

description

This hex inverter is designed for 2.7-V to 3.6-V VCC operation. The SN74LVCU04 contains six independent inverters with unbuffered outputs. The device performs the Boolean function $Y = \overline{A}$.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVCU04 is characterized for operation from -40°C to 85°C.

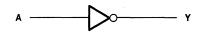
FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
Н	L
L	н

logic symbol†

1A **1Y** 4 2Y 2A 5 6 ЗА **3Y** 8 4Y 4A 10 11 5Δ **5**Y 13 12 6A

logic diagram, each inverter (positive logic)



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[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)	0.5 V to 6.5 V
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	
Continuous output current, I_{O} ($V_{O} = 0$ to V_{CC})	
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3):	
•	DB or PW package 0.5 W
Storage temperature range, Teta	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

		,	MIN	MAX	UNIT	
V	Complexediage	Operating	2	3.6	V	
VCC	Supply voltage	Data retention only	1.5		V	
	,	V _{CC} = 2.7 V	2.16			
VIH	High-level input voltage	V _{CC} = 3 V	2.4		٧	
		V _{CC} = 3.6 V	2.88			
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.65	٧	
٧ _I	Input voltage		0	5.5	٧	
٧o	Output voltage		0	Vcc	٧	
la	I Political and a services	V _{CC} = 2.7 V	,	-12	mA	
ЮН	High-level output current	V _{CC} = 3 V		-24	IIIA	
la.	Love lovel output aurent	V _{CC} = 2.7 V		12	A	
lOL	Low-level output current	V _{CC} = 3 V		24	mA	
Δt/Δv	Input transition rise or fall rate		0	10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST C	CONDITIONS	vcct	MIN TYP‡	MAX	UNIT
,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	I _{OH} = -100 μA		.MIN to MAX	V _{CC} -0.2		
Vari	10 mA		2.7 V	2.2		v
VOH	10H = - 12 IIIA	I _{OH} = - 12 mA		2.4		\ \
	I _{OH} = -24 mA		3 V	2.2		
	I _{OL} = 100 μA,	V _{IH} = 2.16 V	2.7 V		0.2	v
Voi	$I_{OL} \approx 100 \mu A$,	V _{IH} = 2.88 V	3.6 V		0.2	
VOL	I _{OL} = 12 mA,	V _{IH} = 2.16 V	2.7 V		0.4	
	$I_{OL} \approx 24 \text{ mA},$	V _{IH} = 2.4 V	3 V		0.55	
lį	V _I = 5.5 V or GND		3.6 V		±5	μА
lcc	$V_I = V_{CC}$ or GND,	IO = 0	3.6 V		10	μА
ΔlCC	One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μА
Ci	V _I = V _{CC} or GND		3.3 V	5		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	3.3 V 3 V	V _{CC} =	2.7 V	UNIT
	(INPOT)		MIN	MAX	MIN	MAX	Ì
^t pd	A	Υ	1	5		6	ns
t _{sk(o)} §				1			ns

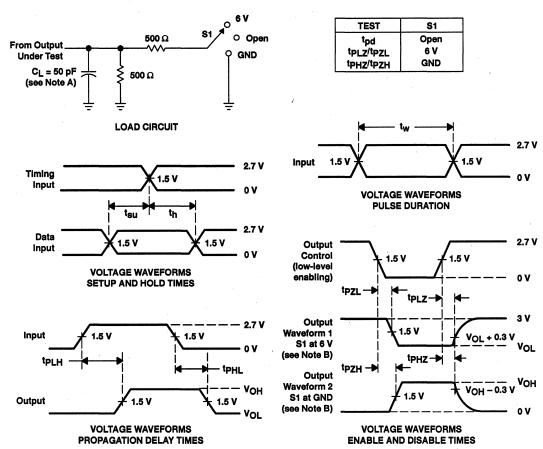
[§] Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per inverter	C _L = 50 pF, f = 10 MHz	5	рF

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \,\Omega$, $t_f \leq 2.5 \,ns$, $t_f \leq 2.5 \,ns$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SN74LVC08 QUADRUPLE 2-INPUT POSITIVE-AND GATE

SCAS283B - JANUARY 1993 - REVISED JULY 1995

- EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per Mil-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Inputs Accept Voltages to 5.5 V
- Package Options include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D,	DB,	OR PW PACKAG	Ε
		(TOP VIEW)	

1A		U	14] V _C (] 4B
1B	2		13	4B
1Y	3		12] 4A
2A	4		11] 4Y
2B	5		10] 3B
2Y	6		9] 3A
GND	7		8] 3Y
				i

description

This quadruple 2-input positive-AND gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC08 performs the Boolean functions $Y = A \bullet B$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-/5-V system environment.

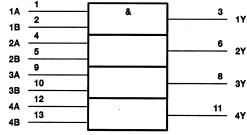
The SN74LVC08 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A B		Υ
Н	Н	Н
-L	Χ	L
Х	L	L

logic symbol†

logic diagram, each gate (positive logic)



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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TEXAS INSTRUMENTS SCAS283B - JANUARY 1993 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5 ^v	V to 6.5 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	C + 0.5 V
Input clamp current, $I_{ K }(V_{ } < 0)$	-50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): D package	
DB or PW package	0.5 W
Storage temperature range, T _{stg} –65°C	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V	Cumplus allege	Operating	2	3.6	V
VCC	Supply voltage	Data retention only	1.5		V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
٧į	Input voltage		0	5.5	٧
VO	Output voltage	put voltage		VCC	٧
lau	High-level output current	V _{CC} = 2.7 V		-12	m A
ЮН	nigh-level output current	V _{CC} = 3 V		-24	mA
la.	Low level output ourrent	V _{CC} = 2.7 V		12	mA
l _O L	Low-level output current VCC = 3 V			24	IIIA
Δt/Δv	Input transition rise or fall rate		0	8	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

SN74LVC08 QUADRUPLE 2-INPUT POSITIVE-AND GATE

SCAS283B - JANUARY 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} †	MIN TYP‡	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Vou	IOH = - 12 mA	2.7 V	2.2		0.2 0.4 0.55 ±5 μΑ 10 μΑ 500 μΑ
VOH	IOH = - 12 IIIA	3 V	2.4		
	I _{OH} = -24 mA	3 V	2.2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
V _{OL}	I _{OL} = 12 mA	2.7 V		0.4	V
	I _{OL} = 24 mA	3 V		0.55	
l _l	V _I = 5.5 V or GND	3.6 V		±5	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		10	μА
ΔlCC	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μА
Ci	V _I = V _{CC} or GND	3.3 V	5		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	3.3 V 3 V	V _{CC} = 2.7 V		UNIT
	(MFOI)	(001701)	MIN	MAX	MIN	MAX	
^t pd	A or B	Υ	1	6		7	ns
tsk(o) [§]				1			ns

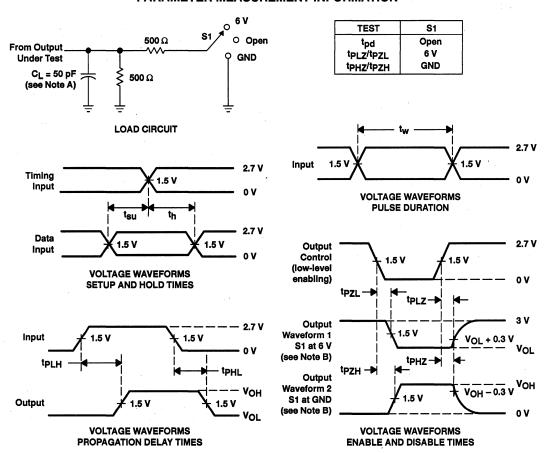
[§] Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

[PARAMETER		TEST CONDITIONS		TYP	UNIT	
I	C _{pd}	Power dissipation capacitance per gate	C _L = 50 pF,	f = 10 MHz	10	pF	

 $[\]ddagger$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tod.

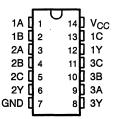
Figure 1. Load Circuit and Voltage Waveforms

SN74LVC10 TRIPLE 3-INPUT POSITIVE-NAND GATE

SCAS284B - JANUARY 1993 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- ESD Protection Exceeds 2000 V Per MIL-STD-883C. Method 3015: Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) **Packages**

D, DB, OR PW PACKAGE (TOP VIEW)



description

This triple 3-input positive-NAND gate is designed for 2.7-V to 3.6-V V_{CC} operation. The SN74LVC10 performs the Boolean functions $Y = \overline{A} \cdot \overline{B} \cdot \overline{C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC10 is characterized for operation from -40°C to 85°C.

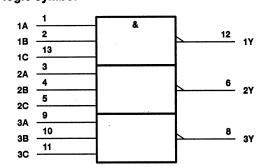
FUNCTION TABLE (each gate)

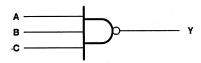
	INPUTS		OUTPUT
Α	В	С	1 Y
Н	Н	Н	L
L	Х	Х	Н
×	L	Χ	Н
Х	Χ	L	Н

SCAS284B - JANUARY 1993 - REVISED JULY 1995

logic symbol†

logic diagram, each gate (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)	0.5 V to 6.5 V
Output voltage range, VO (see Notes 1 and 2)	-0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): D package	1.25 W
	0.5 W
Storage temperature range, T _{stq}	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
	Complexed	Operating	2	3.6	V
VCC	Supply voltage	Data retention only	1.5		V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
VI	Input voltage		0	5.5	٧
Vο	Output voltage		0	VCC	٧
1	Lieb level evitevit evitent	V _{CC} = 2.7 V		-12	mA
ЮН	High-level output current VCC = 3 V			-24	IIIA
la.	V _{CC} = 2.7 V			12	mA
lOL	Low-level output current	V _{CC} = 3 V		24	IIIA
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SCAS284B - JANUARY 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} t	MIN TYP‡	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Mari	In., 10 mA	2.7 V 2.2	, ,		
VOH	IOH = - 12 mA	3 V	2.4		V дА дА дА
	I _{OH} = -24 mA	3 V	2.2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
v_{OL}	i _{OL} = 12 mA	2.7 V		0.4	V
	I _{OL} = 24 mA	3 V		0.55	
lį	V _I = 5.5 V or GND	3.6 V		±5	μА
loc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		10	μА
Δlcc	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μА
Ci	V _I = V _{CC} or GND	3.3 V	5		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

ſ	PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	3.3 V 3 V	V _{CC} =	2.7 V	UNIT
1		(INPOT) (OUTPO	(001701)	MIN	MAX	MIN	MAX	
	^t pd	Α	Y	1	6		7	ns
ſ	t _{sk(o)} §				1			ns

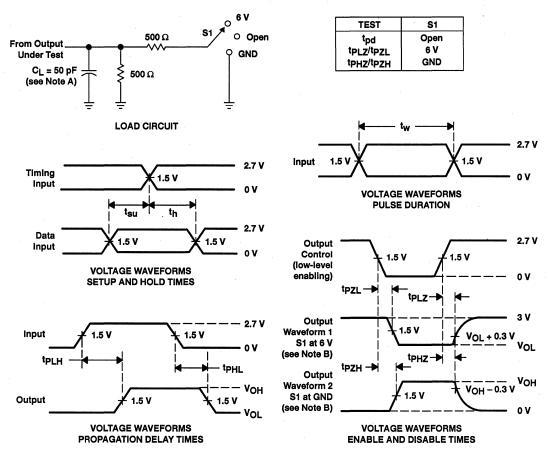
[§] Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per gate	C _L = 50 pF, f = 10 MHz	11	pF

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms

SN74LVC14 HEX SCHMITT-TRIGGER INVERTER

SCAS285B - MARCH 1993 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2 V at V_{CC} = 3.3 V, T_A = 25 °C$
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) **Packages**

D,	DB,	OR	PW	PACKAGE	
		ση	P VI	EW)	

1A [1Y [2	14 13	V _{CC} 6A
2A [12	6Y
2Y [4	11	5A
3A [5	10	5Y
3Y [6	9] 4A
GND [[7	8	4Y

description

This hex Schmitt-trigger inverter is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC14 contains six independent inverters. The device performs the Boolean function $Y = \overline{A}$.

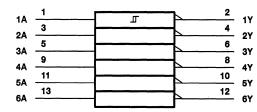
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC14 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each inverter)

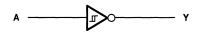
(0000111111011011								
INPUT	OUTPUT							
A	Y							
Н	L							
L	Н							

logic symbolt



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each inverter (positive logic)



SCAS285B - MARCH 1993 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)	0.5 V to 6.5 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	
Continuous output current, I _O (V _O = 0 to V _{CC})	
Continuous current through V _{CC} or GND	
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): D package	
DB or PW package	0.5 W
Storage temperature range, T _{sto}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V	Supply voltage	Operating		3.6	V
vcc	Supply voltage	Data retention only	1.5		· ·
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
٧ı	Input voltage			5.5	٧
VO	Output voltage		0	VCC	٧
lou	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН	riigh-level output current	V _{CC} = 3 V		-24	ША
lai	Low-level output current VCC = 2.7 V VCC = 3 V			12	mA
lOL				24	IIIA
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature			85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

SCAS285B - MARCH 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAME- TER	TEST CONDITIONS	vcct	MIN TYP‡	MAX	UNIT
V _{T+}		2.7 V	0.8	2	
Positive-going	· ·	3 V	0.8	2	v
threshold		3.6 V	0.8	2	
V _T _		2.7 V	0.4	1.4	
Negative-going		3 V	0.6	1.5	V
threshold		3.6 V	0.8	1.8	
ΔV _T		2.7 V	0.3	1.1	
Hysteresis		3 V	0.3	1.2	V
(V _{T+} - V _{T-})		3.6 V	0.3	1.2	
	l _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
V	Jan. 10 mA	2.7 V	2.2		V
VOH	IOH = - 12 mA	3 V	2.4		- v
	i _{OH} = -24 mA	3 V	2.2		
	l _{OL} = 100 μA	MIN to MAX		0.2	
VOL	I _{OL} = 12 mA	2.7 V		0.4	V 0.2 0.4 V
	I _{OL} = 24 mA	3 V		0.55	
l _l	V _I = 5.5 V or GND	3.6 V		±5	μA
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		10	μА
ΔlCC	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μА
Ci	V _I = V _{CC} or GND	3.3 V	5		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V	V _{CC} = 2.7 V	UNIT
	(114-01)	(001701)	MIN MAX	MIN MAX	
t _{pd}	A	Υ .	1 7	7.5	ns
t _{sk(o)} §			1		ns

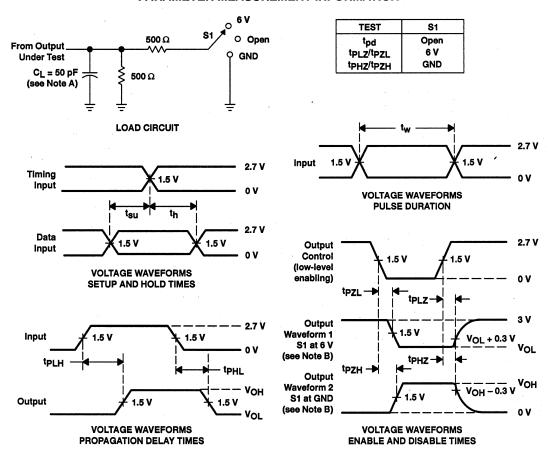
[§] Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CO	TYP	UNIT	
C _{pd}	Power dissipation capacitance per inverter	C _L = 50 pF,	f = 10 MHz	7	pF

[‡]Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \, \Omega$, $t_f \leq 2.5 \, ns$, $t_f \leq 2.5 \, ns$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SN74LVC32 QUADRUPLE 2-INPUT POSITIVE-OR GATE

SCAS286B - JANUARY 1993 - REVISED JULY 1995

 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process

- ESD Protection Exceeds 2000 V Per Mil-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE (TOP VIEW)					
1A [1B [1 2	U 14	, 	V _{CC} 4B	

1A [1 1	\cup	14	l vcc
1B			13] V _{CC}] 4B
1Y	3			
2A	14			5 4Y
2B	5		10] 3B
2Y	6		9	<u>.</u> ЗА
3ND İ				3Y
•	1			7

description

This quadruple 2-input positive-OR gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC32 performs the Boolean functions Y = A + B or $Y = \overline{A \cdot B}$ in positive logic.

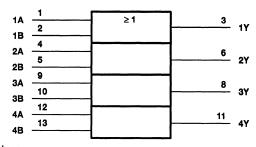
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC32 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each gate)

INP	UTS	OUTPUT
Α	В	Y
Н	Х	Н
X	Н	н
L	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each gate (positive logic)



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SCAS286B - JANUARY 1993 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	V to V_{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): D package	1.25 W
DB or PW package	0.5 W
Storage temperature range, T _{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Voc	Supply voltage	Operating	2	3.6	V
vcc	Supply voltage	Data retention only	1.5		V.
٧ _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
VI	Input voltage			5.5	٧
VΟ	Output voltage		0	VCC	٧
lavi	I Bala Jarrel andre de coment	V _{CC} = 2.7 V		-12	mA
ЮН	High-level output current	V _{CC} = 3 V		-24	IIIA
1	Low-level output current	V _{CC} = 2.7 V		12	
lOL	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate		0	7	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

SCAS286B - JANUARY 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} t	MIN TYP‡	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
V	10 mA	2.7 V	2.2		v
VOH	IOH = - 12 mA	3 V	2.4		\ \
1	I _{OH} = -24 mA	3 V	2.2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
V _{OL}	I _{OL} = 12 mA	2.7 V		0.4	V
	I _{OL} = 24 mA	3 V		0.55	
l _l	V _I = 5.5 V or GND	3.6 V		±5	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		10	μА
ΔlCC	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μА
Ci	V _I = V _{CC} or GND	3.3 V	5		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	FROM TO (OUTPUT)	V _{CC} =	3.3 V 3 V	V _{CC} =	2.7 V	UNIT
	(INFO1)		MIN	MAX	MIN	MAX	
^t pd	A or B	Y	1.5	6		7	ns
t _{sk(o)} §	·			1			ns

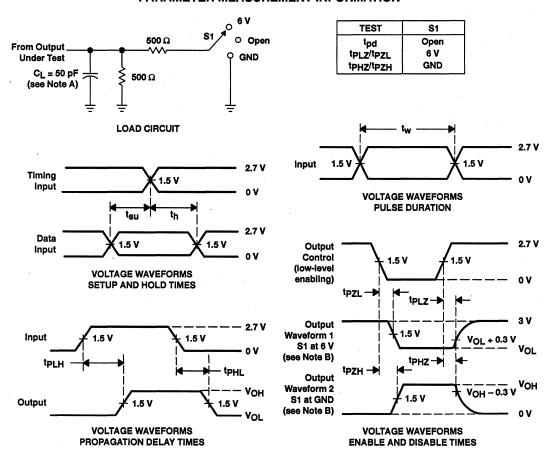
[§] Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$

PARAMETER		TEST CO	TYP	UNIT	
C _{pd} Power dis	sipation capacitance per gate	CL = 50 pF,	f = 10 MHz	12.5	pF

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

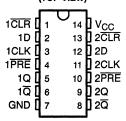
Figure 1. Load Circuit and Voltage Waveforms

SN74LVC74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

SCAS287B - JANUARY 1993 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE (TOP VIEW)



description

This dual positive-edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC74 is characterized for operation from -40°C to 85°C.

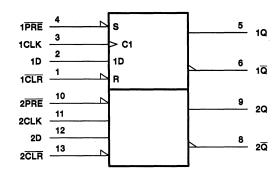
FUNCTION TABLE

INPUTS				OUT	PUTS
PRE	CLR	CLK	D	Q	Q
L	Н	Х	Х	Н	L
н	L	X	Х	L	н
L	L	X	X	Ht	H [†]
н	Н	1	Н	Н	L
Н	Н	1	L	L	н
Н	Н	L	X	Q ₀	\overline{Q}_0

[†] This configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

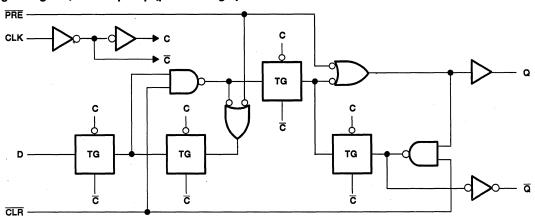
SCAS287B - JANUARY 1993 - REVISED JULY 1995

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	-0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)	
Output voltage range, V _O (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	
Continuous output current, I _O (V _O = 0 to V _{CC})	
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): D package	
DB or PW packa	ge 0.5 W
Storage temperature range, T _{stq}	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.



SN74LVC74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

SCAS287B - JANUARY 1993 - REVISED JULY 1995

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
14	O. and L. and L. and	Operating	2	3.6	V
VCC	Supply voltage	Data retention only	1.5		· ·
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
٧ _I	Input voltage			5.5	V
Vo	Output voltage		0	VCC	٧
	I limb lavel a short a summer	V _{CC} = 2.7 V		-12	
IOH	High-level output current	V _{CC} = 3 V		-24	mA
1	Low-level output current	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current	V _{CC} = 3 V		24	- III
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcct	MIN TYP‡	MAX	UNIT
	l _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
V	10 mA	2.7 V	2.2		v
VOH	IOH = - 12 mA	3 V	2.4		'
	I _{OH} = -24 mA	3 V	2.2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
VOL	I _{OL} = 12 mA	2.7 V		0.4	V
	I _{OL} = 24 mA	3 V		0.55	
lį	V _I = 5.5 V or GND	3.6 V		±5	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		10	μА
ΔlCC	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μА
Ci	V _I = V _{CC} or GND	3.3 V	5		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			VCC =		V _{CC} = 2.7 V		UNIT	
			MIN	MIN MAX MIN MAX				
fclock	Clock frequency		0	100	0	83	MHz	
A Dul	Pulse duration	PRE or CLR low	4		5			
t _w	ruise duration	CLK high or low	5		6		ns	
	0-4	Data	3		4		ns	
t _{su}	Setup time before CLK↑	PRE or CLR inactive	2		3			
th	Hold time, data after CLK↑		1		2		ns	

 $[\]ddagger$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SN74LVC74 **DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP** WITH CLEAR AND PRESET SCAS287B - JANUARY 1993 - REVISED JULY 1995

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO	V _{CC} =	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	
		(OUTPUT)	MIN	MAX	MIN	MAX	
f _{max}			100		83		MHz
	CLK	Q or Q	1	6.5		7	
^t pd	PRE or CLR		1	8		9	ns
t _{sk(o)} †				1			ns

[†] Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

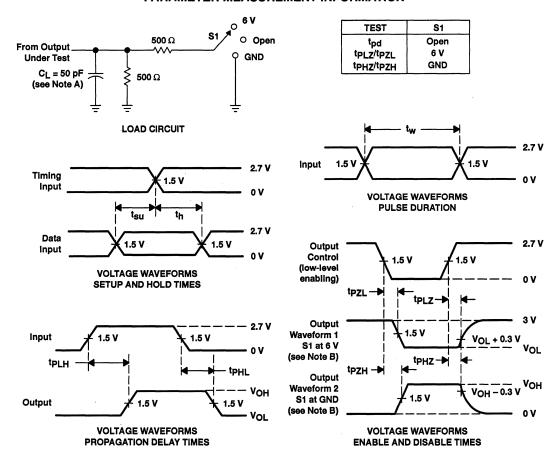
operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CO	TYP	UNIT	
C _{pd}	Power dissipation capacitance per flip-flop	C _L = 50 pF,	f = 10 MHz	27	pF



SCAS287B - JANUARY 1993 - REVISED JULY 1995

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

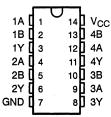
SN74LVC86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

SCAS288B - JANUARY 1993 - REVISED JULY 1995

 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process

- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE (TOP VIEW)



description

This quadruple 2-input exclusive-OR gate is designed for 2.7-V to 3.6-V V_{CC} operation. The SN74LVC86 performs the Boolean functions $Y = A \oplus B$ or $Y = \overline{AB} + A\overline{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

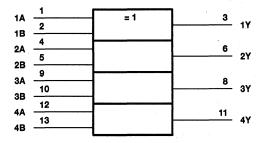
The SN74LVC86 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each gate)

(eacii gate)						
INP	UTS	OUTPUT				
Α	В	Y				
L	L	L				
L	Н	н				
Н	L	н				
Н	н	L				

SCAS288B - JANUARY 1993 - REVISED JULY 1995

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



These five equivalent exclusive-OR symbols are valid for an SN74LVC86 gate in positive logic; negation may be shown at any two ports.

The output is active (low) if all inputs stand at the same logic level (i.e., A = B). EVEN-PARITY ELEMENT ODD-PARITY ELEMENT The output is active (low) if an even number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)	0.5 V to 6.5 V
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): D package	1.25 W
DB or PW packag	e 0.5 W
Storage temperature range, T _{sto}	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

^{2.} This value is limited to 4.6 V maximum.

SCAS288B - JANUARY 1993 - REVISED JULY 1995

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V	Cumplicustage	Operating	2	3.6	V
VCC	Supply voltage	Data retention only	1.5		v
ViΗ	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
٧ _l	Input voltage		0	5.5	٧
Vο	Output voltage		0	VCC	٧
1	I Pale I and a day to see	V _{CC} = 2.7 V		-12	mA
ЮН	High-level output current	V _{CC} = 3 V		-24	ША
1	Law lavel autout august	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current	V _{CC} = 3 V		24	MA
Δt/Δν	Input transition rise or fall rate		0	9	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} t	MIN TYP‡	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Vall	I _{OH} = - 12 mA	2.7 V	2.2		v
VOH	IOH = - 12 IIIA	3 V	2.4		V
	I _{OH} = -24 mA	3 V	2.2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
VOL	I _{OL} = 12 mA	2.7 V		0.4	V
	I _{OL} = 24 mA	3 V		0.55	
l _l	V _I = 5.5 V or GND	3.6 V		±5	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		10	μА
ΔICC	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μА
Ci	V _I = V _{CC} or GND	3.3 V	5		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	
L			(001701)	MIN	MAX	MIN	MAX	
	^t pd	Α	Y	1	6.5	,	7.5	ns
ſ	t _{sk(o)} §				1			ns

[§] Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

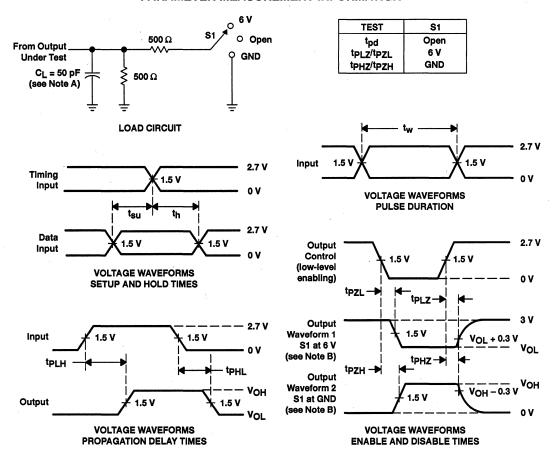
operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CO	TYP	UNIT	
C _{pd}	Power dissipation capacitance per gate	C _L = 50 pF,	f = 10 MHz	8.5	pF



[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP WITH CLEAR AND PRESET

GND

SCAS289A - JANUARY 1993 - REVISED JULY 1995

9[] 2Q

- D, DB, OR PW PACKAGE EPIC™ (Enhanced-Performance Implanted (TOP VIEW) **CMOS) Submicron Process** Typical V_{OLP} (Output Ground Bounce) 16 VCC 1CLK II 1 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 1K 🛮 2 15 1 1 CLR Typical V_{OHV} (Output V_{OH} Undershoot) 14 2 2 CLR 1J Π 3 > 2 V at V_{CC} = 3.3 V, T_A = 25°C 1PRE [] 4 13 2CLK Inputs Accept Voltages to 5.5 V 12 1 2K 1Q [] 5 Package Options Include Plastic 10 [6 11 2J 20 17 10 2PRE
- Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) **Packages**

description

This dual negative-edge-triggered J-K flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the J and K inputs meeting the setup time requirements is transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the J and K inputs can be changed without affecting the levels at the outputs. The SN74LVC112 can perform as a toggle flip-flop by tying J and K high.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices in a mixed 3.3-V/5-V system environment.

The SN74LVC112 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

		INPUTS			OUTI	PUTS
PRE	CLR	CLK	J	K	Q	Ø
L	Н	Х	Х	Х	Н	L
н	L	X	Х	X	L	н
L	L	X	Х	X	H†	нt
н	Н	1	L	L	Q ₀	\overline{Q}_{0}
Н	Н	1	Н	L	н	L
Н	Н	1	L	Н	L	н
н	Н	1	Н	Н	Toggle	
н	Н	Н	Х	X	Q ₀	\overline{Q}_0

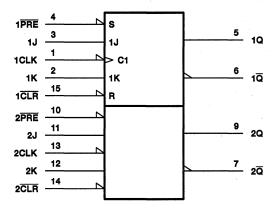
[†]The output levels in this configuration may not meet the minimum levels for VOH. Furthermore, this configuration is nonstable; that is, it does not persist when either PRE or CLR returns to its inactive (high) level.



SN74LVC112 DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP WITH CLEAR AND PRESET

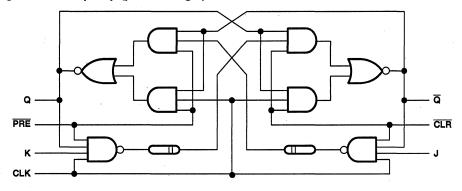
SCAS289A - JANUARY 1993 - REVISED JULY 1995

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each flip-flop (positive logic)



SN74LVC112 DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP WITH CLEAR AND PRESET

SCAS289A - JANUARY 1993 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5	V to 6.5 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	C + 0.5 V
Input clamp current, $I_{ K }(V_1 < 0)$	-50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): D package	1.3 W
DB package	. 0.55 W
PW package	0.5 W
Storage temperature range, T _{stq} –65°C	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
۷į	Input voltage		0	5.5	٧
٧o	Output voltage		0	VCC	>
lou	High-level output current $\frac{V_{CC} = 2.7 \text{ V}}{V_{CC} = 3 \text{ V}}$	V _{CC} = 2.7 V		-12	mA
ЮН		V _{CC} = 3 V		-24	111
lai	Low level output ourrant	V _{CC} = 2.7 V		12	mA
loL	Low-level output current	v _{CC} = 3 V		24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.



SN74LVC112 DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP WITH CLEAR AND PRESET SCAS289A - JANUARY 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcct	MIN TYP‡	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Vou	lou - 12 mA	2.7 V	2.2		v
VOH	I _{OH} = - 12 mA	3 V	2.4		. •
	$I_{OH} = -24 \text{ mA}$	3 V	2.2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
VOL	I _{OL} = 12 mA	2.7 V		0.4	V
	I _{OL} = 24 mA	3 V		0.55	
l ₁	V _I = 5.5 V or GND	3.6 V		±5	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		10	μА
ΔlCC	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μА
Ci	V _I = V _{CC} or GND	3.3 V			pF
Co	V _O = V _{CC} or GND	3.3 V			pF

TFor conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

SN74LVC125 QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

SCAS290B - JANUARY 1993 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE (TOP VIEW)

20E [2A [2 3 4 5	O	12 11 10		V _{CC} 4OE 4A 4Y 3OE 3A
	6 7			5	3A 3Y

description

This quadruple bus buffer gate is designed for 2.7-V to 3.6-V V_{CC} operation. The SN74LVC125 features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (\overline{OE}) input is high.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC125 is characterized for operation from -40°C to 85°C.

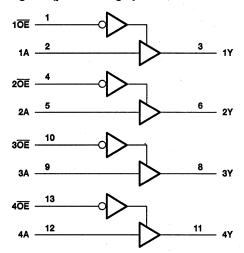
FUNCTION TABLE (each buffer)

(odon banor)				
INPUTS		OUTPUT		
OE	Α	Y		
L	Н	Н		
L	L	L		
Н	Х	z		

SCAS290B - JANUARY 1993 - REVISED JULY 1995

logic symbol†

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 6.5 V 0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at $\overline{T}_A = 55^{\circ}C$ (in still air) (see Note 3): D package	
	e 0.5 W
Storage temperature range, T _{stg}	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
Vcc	Supply voltage	Operating	2	3.6	3.6	
		Data retention only	1.5		٧	
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V	
VIL	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	٧	
٧į	Input voltage		0	5.5	٧	
Vo	Output voltage		0	VCC	٧	
	High-level output current	V _{CC} = 2.7 V		-12	mA	
IOH	High-level output current	V _{CC} = 3 V		-24	IIIA	
1	Law law Law Law Law Law Law Law Law Law Law L	V _{CC} = 2.7 V		12	mA	
lOL	Low-level output current	V _{CC} = 3 V		24	IIIA	
Δt/Δv	Input transition rise or fall rate		0	8	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} †	MIN TYP‡	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
V	lau 10 mA	2.7 V	2.2		٧
VOH	I _{OH} = - 12 mA	3 V	2.4		
	I _{OH} = -24 mA	3 V	2.2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
VOL	I _{OL} = 12 mA	2.7 V		0.4	V
	I _{OL} = 24 mA	3 V		0.55	
lį	V _I = 5.5 V or GND .	3.6 V		±5	μА
loz	V _O = V _{CC} or GND	3.6 V		±10	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		10	μА
ΔlCC	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μА
Ci	V _I = V _{CC} or GND	3.3 V	5		pF
Co	V _O = V _{CC} or GND	3.3 V	5		pF

For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)		VCC =	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	
	(INFOT)	(001701)	MIN	MAX	MIN	MAX	
^t pd	Α	Y	1	6.5		7	ns
t _{en}	ŌĒ	Y	1	7		8	ns
^t dis	ŌĒ	Y	1	5.5		6.5	ns
t _{sk(o)} §				1			ns

[§] Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

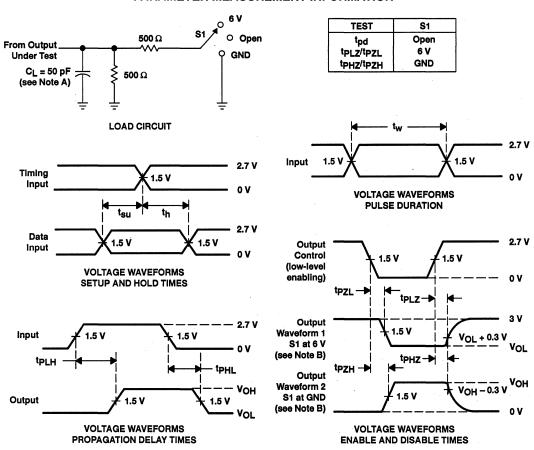


[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per gate	C _L = 50 pF, f = 10 MHz	15	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms

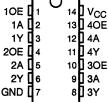


SN74LVC126 QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

SCAS339A - MARCH 1994 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE (TOP VIEW)



description

This quadruple bus buffer gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC126 features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC126 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each buffer)

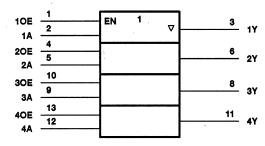
INPUTS		OUTPUT
OE	Α	Y
Н	Н	Н
Н	L	L
L	Х	Z .



SN74LVC126 QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

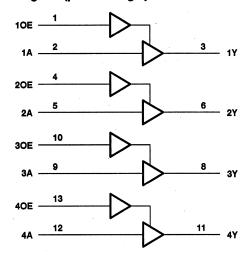
SCAS339A - MARCH 1994 - REVISED JULY 1995

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): D package	1.25 W
DB or PW package .	
Storage temperature range, T _{stq}	

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

SN74LVC126 QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS SCAS339A - MARCH 1994 - REVISED JULY 1995

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage V _{CC} = 2.7 V	/ to 3.6 V	2		٧
VIL	Low-level input voltage V _{CC} = 2.7 V	/ to 3.6 V		0.8	٧
٧ _I	Input voltage		0	5.5	٧
٧o	Output voltage		0	Vcc	٧
lau	High-level output current	/		-12	mA
ЮН	V _{CC} = 3 V			-24	ША
1	V _{CC} = 2.7 V	/		12	mA
lOL	Low-level output current VCC = 3 V			24	1111
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcct	MIN TYP‡	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Vari	10 mA	2.7 V	2.2		v
VOH	IOH = - 12 mA	3 V	2.4		٧
	I _{OH} = -24 mA	3 V	2.2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
v_{OL}	I _{OL} = 12 mA	2.7 V		0.4	٧
	I _{OL} = 24 mA	3 V		0.55	
lj	V _I = 5.5 V or GND	3.6 V		±5	μА
loz	V _O = V _{CC} or GND	3.6 V		±10	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		10	μА
ΔlCC	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μА
Ci	V _I = V _{CC} or GND	3.3 V			pF
Co	V _O = V _{CC} or GND	3.3 V		-	pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



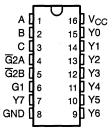
[‡] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

SN74LVC137 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCHES

SCAS340A - MARCH 1994 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) **Packages**

D, DB, OR PW PACKAGE (TOP VIEW)



description

This 3-line to 8-line decoder/demultiplexer with latches on three address inputs is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC137 is designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

When the latch-enable ($\overline{G}2A$) input is low, the SN74LVC137 acts as a decoder/demultiplexer. When $\overline{G}2A$ transitions from low to high, the address present at the inputs (A, B, and C) is stored in the latches. Further address changes are ignored provided $\overline{G}2A$ remains high. The output-enable (G1 and $\overline{G}2B$) inputs control the outputs independently of the select or latch-enable inputs. All of the outputs are forced high if G1 is low or $\overline{\sf G2B}$ is high.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices in a mixed 3.3-V/5-V system environment.

The SN74LVC137 is characterized for operation from -40°C to 85°C.

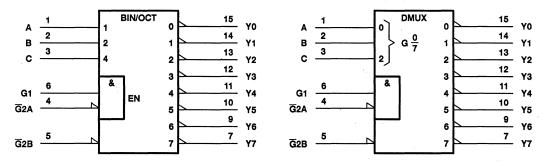
FUNCTION TABLE

LATCH ENABLE		PUT- ABLE	SEL	ECT INF	PUTS				OUTF	PUTS			
G2A	G1	G ₂ B	С	В	Α	YO	Y1	Y2	Y3	Y4	Y5	Y6	Y7
· X	Х	Н	Х	Х	Х	Н	Н	Н	Н	Н	Н	Н	Н
X	L	x	Х	Χ	Χ	н	Н	Н	Н	Н	Н	Н	н
L	Н	L	L	L	L	L	Н	Н	Н	Н	Н	Н	н
L	Н	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	н
L	Н	L	L	Н	L	Н	Н	L	Н	Н	Н	Н	н
L	Н	L	L	Н	н	н	Н	Н	L	Н	Н	Н	н
L	Н	L	Н	L	L	Н	н	Н	Н	L	Н	Н	Н
L	Н	L	Н	L	Н	Н	Н	Н	н	Н	L	Н	н
L	Н	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	н
L	Н	L	Н	Н	Н	н	H	Н	Н	Н	Н	Н	L
н	н	L	х	Χ	X	Outputs	corresp	onding to	stored a	address	= L; all of	ther outp	uts = H

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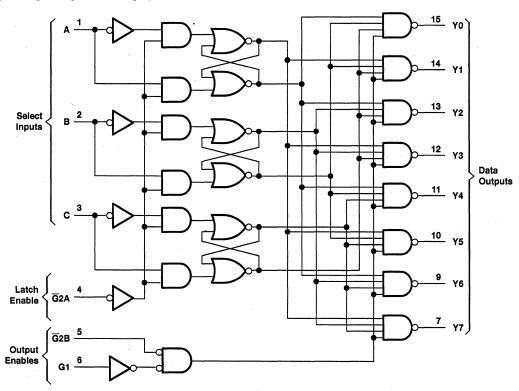


logic symbols (alternatives)†



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN74LVC137 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCHES

SCAS340A - MARCH 1994 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I_{IK} ($V_I < 0$)	
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3)	: D package 1.3 W
	DB package 0.55 W
	PW package 0.5 W
Storage temperature range, T _{sto}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	٧
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
۷ _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		8.0	٧
۷Į	Input voltage		0	5.5	٧
۷o	Output voltage		0	VCC	٧
10	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН	High-level output current	V _{CC} = 3 V		-24	ША
lo	Low-level output current	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current	V _{CC} = 3 V		24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.



SN74LVC137 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCHES SCAS340A - MARCH 1994 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} †	MIN TYP‡	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Vari	I _{OH} = – 12 mA	2.7 V	2.2		v
Voн	IOH = - 12111A	- 3 V	2.4		\ \
	I _{OH} = -24 mA	3 V	2.2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
VOL	I _{OL} = 12 mA	2.7 V		0.4	٧
	I _{OL} = 24 mA	3 V		0.55	
Ŋ	V _I = 5.5 V or GND	3.6 V		±5	μА
loz	V _O = V _{CC} or GND	3.6 V		±10	μА
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		10	μА
ΔICC	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μА
Ci	V _I = V _{CC} or GND	3.3 V			pF
Co	V _O = V _{CC} or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

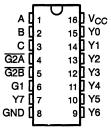
SN74LVC138 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

SCAS291B - MARCH 1993 - REVISED JULY 1995

 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process

- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D,	DB,	OR	PW	PAG	CKA	GΕ
		mο	P VI	EW))	



description

This 3-line to 8-line decoder/demultiplexer is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC138 is designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder minimizes the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight input lines. Two active-low enable inputs and one active-high enable input reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC138 is characterized for operation from -40°C to 85°C.

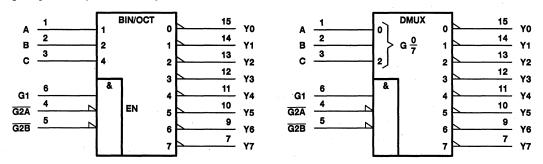
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SCAS291B - MARCH 1993 - REVISED JULY 1995

				-	-
FU	NCT	ION	TA	ВL	Æ

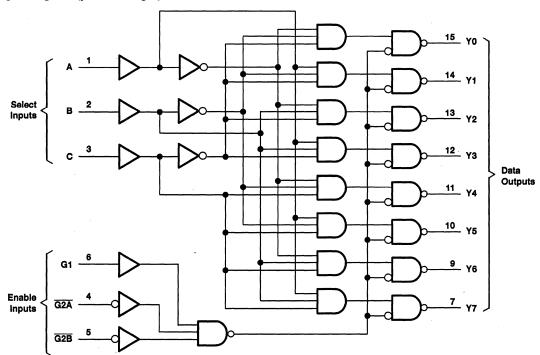
ENA	BLE INF	PUTS	SEL	ECT INP	UTS	OUTPUTS							
G1	G2A	G2B	C	В	Α	Y0	Y1	Y2	Y3 .	Y4	Y5	Y6	Y7
Х	Н	Х	Х	Х	Х	Н	Н	Н	Н	Н	Н	Н	Н
X	X	Н	х	Χ	Χ	Н	Н	Н	Н	Н	Н	н	н
L	X	X	Х	X	X	Н	Н	Н	Н	Н	Н	Н	н
н	L	L	L	L	L	L	Н	Н	Н	Н	Н	Н	H·
Н	L	L	L	L	Н	Н	L	Н	Н	Η .	Ή	. н	н
н	. L	L	L	Н	L	Н	Н	L	Н	Н	H	Н	н.
н	L	L	L	Н	H	Н	Н	Н	L	Н	Н	Н	н
Н	L	L	Н	L	L	Н	Н	Н	H	L	Н	Н	н
н	· L	L	н	L	Н	Н	Н	Н	Н	Н	· L	Н	н
н	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	н
н	L	L	н	Н	Н	н	н	Н	Н	· H	′ H	н	L

logic symbols (alternatives)†



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SCAS291B - MARCH 1993 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)		
Output voltage range, VO (see Notes 1 and 2)		5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)		–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})		±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})		±50 mA
Continuous current through V _{CC} or GND		±100 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air): (see Note 3)	D package	1.3 W
	DB package	0.55 W
	PW package	
Storage temperature range, T _{stg}		65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V	Cumply valtage	Operating	2	3.6	V
VCC	Data retention	Data retention only	1.5		٧
٧ _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
٧ _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
۷ _I	Input voltage		0	5.5	٧
۷o	Output voltage		0	VCC	٧
lau	High level entruit current	V _{CC} = 2.7 V		-12	A
ЮН	night-level output current	V _{CC} = 3 V		-24	mA
lo	Low lovel output ourrent	V _{CC} = 2.7 V		12	mA
loL	Low-level output current	V _{CC} = 3 V		24	IIIA
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C
	- Pro				

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

SCAS291B - MARCH 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} †	MIN TYP‡	MAX	UNIT
	IOH = -100 μA	MIN to MAX	V _{CC} -0.2		
Vari	10 mA	2.7 V	2.2		v
Voн	I _{OH} = - 12 mA	3 V	2.4		v
	I _{OH} = -24 mA	3 V	2.2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
V _{OL}	I _{OL} = 12 mA	2.7 V		0.4	V
	I _{OL} = 24 mA	3 V		0.55	
l ₁	V _I = 5.5 V or GND	3.6 V		±5	μΑ
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		10	μΑ
ΔlCC	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μА
Co	VO = VCC or GND	3.3 V	5		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)			V _{CC} = 2.7 V		UNIT
	(INPO1)		MIN	MAX	MIN	MAX	
A or B or C		1	6.7		7.9		
t _{pd}	G2A or G2B	Y	1	6.5		7.4	ns
	G1		1	5.8		6.4	1
t _{sk(o)} §				1			ns

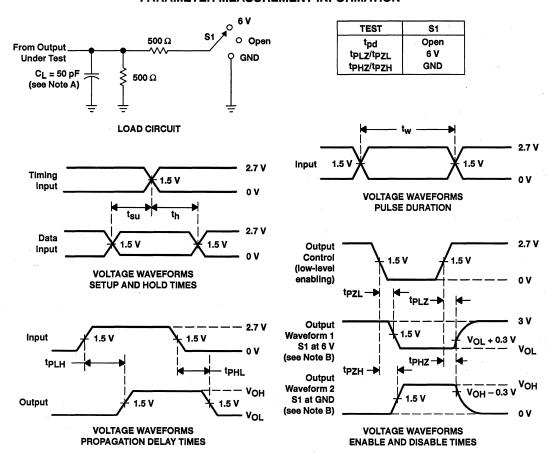
[§] Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER		TEST CONDITIONS		
Cpc	d Power dissipation capacitance	C _L = 50 pF,	f = 10 MHz	27	pF

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SN74LVC139 DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

SCAS341A - MARCH 1994 - REVISED JULY 1995

 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	D, DB, OR PW PACKAGE (TOP VIEW)
 Typical V_{OLP} (Output Ground Bounce) 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	10E 1 16 V _{CC}
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1A [2 15] 2OE 1B [3 14] 2A 1Y0 [4 13] 2B
 Inputs Accept Voltages to 5.5 V 	1Y1 5 12 2Y0
Package Options Include Plastic	1Y2 [6 11] 2Y1
Small-Outline (D), Shrink Small-Outline	1Y3 🛛 7 10 🗍 2Y2
(DB), and Thin Shrink Small-Outline (PW) Packages	GND [8 9] 2Y3

description

This dual 2-line to 4-line decoder/demultiplexer is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC139 is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The device comprises two individual 2-line to 4-line decoders in a single package. The active-low output-enable (\overline{OE}) input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices in a mixed 3.3-V/5-V system environment.

The SN74LVC139 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

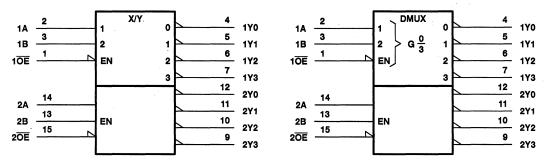
	INPUTS			OUTPUTS			
ŌĒ	SEL	SELECT		0017015			
OE	В	Α	Y0	Y1	Y2	Y3	
Н	Х	Х	Н	Н	Н	Н	
L	L	L	L	н	Н	н	
L	L	Н	Н	L	Н	н	
L	Н	L	Н	Н	L	н	
L	Н	н	н	Н	н	L	

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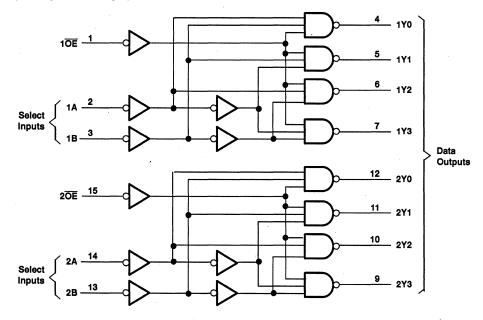
SCAS341A - MARCH 1994 - REVISED JULY 1995

logic symbols (alternatives)†



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN74LVC139 DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

SCAS341A - MARCH 1994 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 6.5 V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	
Continuous current through V _{CC} or GND	
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3)	: D package 1.3 W
, , , , , , , , , , , , , , , , , , , ,	DB package 0.55 W
	PW package 0.5 W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

		,	MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	٧
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
VI	Input voltage		0	5.5	٧
Vo	Output voltage		0	VCC	٧
1	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН		.V _{CC} = 3 V		-24	IIIA
la.	Lave lavel authorit auswant	V _{CC} = 2.7 V		12	mA
IOL Low-level output current		V _{CC} = 3 V		24	MA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.



SCAS341A - MARCH 1994 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST C	ONDITIONS	vcct	MIN	TYP‡	MAX	UNIT
	iOH = -100 μA		MIN to MAX	V _{CC} -0.2			
V	10 m 4		2.7 V	2.2			ν
VOH	IOH = - 12 mA		3 V	2.4			'
	I _{OH} = -24 mA		3 V	2.2			
	I _{OL} = 100 μA		MIN to MAX			0.2	
VOL	I _{OL} = 12 mA		2.7 V			0.4	٧
	I _{OL} = 24 mA		3 V			0.55	
ίι	V _I = 5.5 V or GND		3.6 V			±5	μА
loz	VO = VCC or GND		3.6 V			±10	μА
Icc	V _I = V _{CC} or GND,	I _O = 0	3.6 V			10	μА
ΔlCC	One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	μА
Ci	V _I = V _{CC} or GND		3.3 V				pF
Co	VO = VCC or GND		3.3 V		٠.		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions. ‡ Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

SCAS292B - JANUARY 1993 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance implanted **CMOS) Submicron Process**
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) **Packages**

D, DB,	OR	PW	PAC	KAGE
	(TO	P VI	EW)	

	_		_	
Ā/B [1	U	16	v _{cc}
1A [2		15] G
1B [] з] 4A
1Y [4		13] 4B
2A (5		12] 4Y
2B (6		11] 3A
2Y [7		10] 3B
GND	8		9	3Y
_				

description

This quadruple 2-line to 1-line data selector/multiplexer is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC157 features a common strobe (G) input. When the strobe is high, all outputs are low. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The device provides true data.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC157 is characterized for operation from -40°C to 85°C.

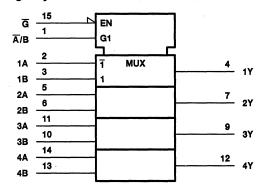
FUNCTION TABLE

	INPL	OUTPUT		
G	Ā/B	Α	В	Y
Н	Х	Х	Х	L
L	L	L	X	L
L	L	Н	Χ	Н
L	Н	Χ	L	L
L	Н	Х	н	Н

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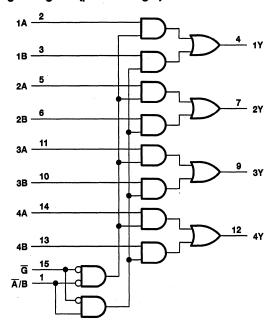
SCAS292B - JANUARY 1993 - REVISED JULY 1995

logic symbol[†]



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)	0.5 V to 6.5 V
Output voltage range, VO (see Notes 1 and 2)	. -0.5 V to $V_{CC} + 0.5 \text{ V}$
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): D package	1.3 W
DB package	0.55 W
PW package	0.5 W
Storage temperature range, T _{sto}	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

SCAS292B - JANUARY 1993 - REVISED JULY 1995

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V	Cumply voltage	Operating	2	3.6	V
VCC	Supply voltage	Data retention only	1.5		V
V_{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
VI	Input voltage		0	5.5	V
٧o	Output voltage		0	VCC	V
1	High-level output current	V _{CC} = 2.7 V	1	-12	mA
ЮН	High-level output current	V _{CC} = 3 V		-24	IIIA
1	Law law law and a ware at	V _{CC} = 2.7 V		12	^
IOL	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
T _A Operating free-air temperature		-40	85	°C ·	

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcct	MIN TYP	MAX	UNIT
	l _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Vau	I _{OH} = – 12 mA	2.7 V	2.2		v
VOH	10H = - 12 IIIA	3 V	2.4		•
	I _{OH} = -24 mA	3 V	2.2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
VOL	I _{OL} = 12 mA	2.7 V		0.4	V
	I _{OL} = 24 mA	3 V		0.55	
· - I	V _I = 5.5 V or GND	3.6 V		±5	μΑ
-cc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		10	μΑ
ΔlCC	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μΑ
C _i	V _I = V _{CC} or GND	3.3 V	5		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C₁ = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	3.3 V 3 V	V _{CC} =	2.7 V	UNIT
	(IIIFO1)	(001701)	MIN	MAX	MIN	MAX	
	A or B	,	1	5.8		6.3	
^t pd	Ā/B	. Y	1	7.5		8.5	ns
	G		1	7.5		8.5	
t _{sk(o)} §				1			ns

[§] Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.



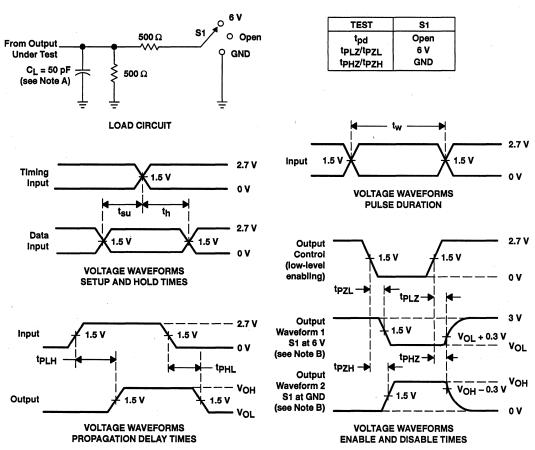
[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SCAS292B - JANUARY 1993 - REVISED JULY 1995

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST COND	TYP	UNIT	
C _{pd}	Power dissipation capacitance	C _L = 50 pF,	f = 10 MHz	16	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \, \Omega$, $t_f \leq 2.5 \, ns$, $t_f \leq 2.5 \, ns$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SN74LVC158 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

SCAS342A - MARCH 1994 - REVISED JULY 1995

 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	D, I
 Typical V_{OLP} (Output Ground Bounce) 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	Ā
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1 1

- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D,	DB,	OR	PW	PACKAGE
		(TO	P VI	EW)

Ā/B [1	U	16] v _{cc}
1A [2		15] ច
1B (3		14] 4A
1Y (4		13] 4B
2A (5		12] 4Y
2B [6		11] 3A
2Y [17		10] 3B
GND [8		9] 3Y
				,

description

This quadruple 2-line to 1-line data selector/multiplexer is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC158 features a direct strobe ($\overline{\mathbf{G}}$) input. When the strobe is high, all outputs are high. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The SN74LVC158 provides inverted data.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices in a mixed 3.3-V/5-V system environment.

The SN74LVC158 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

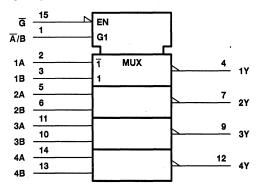
	INPL	OUTPUT		
G	Ā/B	Α	В	Y
Н	Х	Х	Х	Н
L	L	L	Х	Н
L	L	Н	Х	L
L	Н	X	L	Н
L	Н	Χ	Н	L

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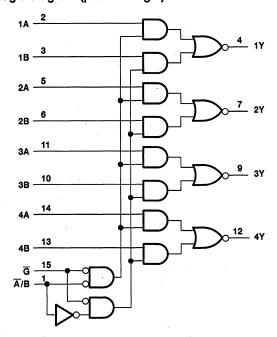
SCAS342A - MARCH 1994 - REVISED JULY 1995

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)	0.5 V to 6.5 V
Output voltage range, V _O (see Notes 1 and 2)	5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): D package	1.3 W
DB package	0.55 W
PW package	0.5 W
Storage temperature range, T _{stq}	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

SN74LVC158 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

SCAS342A - MARCH 1994 - REVISED JULY 1995

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
VI	Input voltage		0	5.5	٧
Vo	Output voltage		0	VCC	٧
1	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН	nigri-level output current	V _{CC} = 3 V		-24	IIIA
1	Low-level output current	V _{CC} = 2.7 V		12	mA
IOL	Low-level output current	V _{CC} = 3 V		24	ША
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcct	MIN TYP‡	MAX	UNIT	
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			
Vall	IOH = - 12 mA	2.7 V	2.2		v	
Voн	IOH = - 12 IIIA	3 V 2.4				
	I _{OH} = -24 mA	3 V	2.2			
	I _{OL} = 100 μA	MIN to MAX		0.2		
VOL	I _{OL} = 12 mA	2.7 V		0.4	٧	
	I _{OL} = 24 mA	3 V		0.55		
lj	V _I = 5.5 V or GND	3.6 V		±5	μА	
loz	$V_O = V_{CC}$ or GND	3.6 V		±10	μА	
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		10	μА	
ΔICC	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μA	
Ci	V _I = V _{CC} or GND	3.3 V			pF	
Co	$V_O = V_{CC}$ or GND	3.3 V			pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

SN74LVC240 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS293A - JANUARY 1993 - REVISED JULY 1995

 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	DB, DW, OR PW PACKAGE (TOP VIEW)
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1 OE 1 20 V _{CC} 1A1 2 19 2 OE
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	2Y4 [3 18] 1Y1 1A2 [4 17] 2A4
 Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17 	2Y3 [5 16] 1Y2 1A3 [6 15] 2A3
Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline	2Y2 07 14 0 1Y3 1A4 08 13 0 2A2
(DB), and Thin Shrink Small-Outline (PW) Packages	2Y1 0 12 1 1Y4 GND 0 10 11 2A1

description

This octal buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC240 is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN74LVC240 is organized as two 4-bit buffers/drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

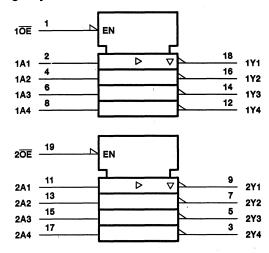
The SN74LVC240 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each buffer)

	<u> </u>	
INPL	JTS	OUTPUT
OE	Α	Y
L	Н	L
L	L	н
н	Х	Z

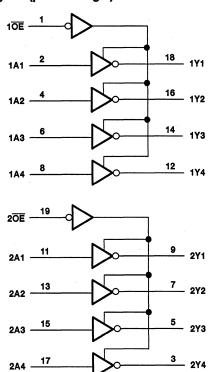
EPIC is a trademark of Texas Instruments Incorporated.

logic symbolt



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I _{IK} (V ₁ < 0)	
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB pack	
DW pack	kage 1.6 W
PW pack	kage 0.7 W
Operating free-air temperature range, T _A	40°C to 85°C
Storage temperature range, T _{stq}	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.



recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
٧į	Input voltage		0	5.5	V
Vο	Output voltage		0	VCC	V
la	High-level output current $ \frac{V_{CC} = 2.7 \text{ V}}{V_{CC} = 3 \text{ V}} $		-12	mA	
ЮН		V _{CC} = 3 V		-24	IIIA
la.	Low-level output current	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current	V _{CC} = 3 V		24	111/4
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST COND	TEST CONDITIONS			TYP‡	MAX	UNIT	
	I _{OH} = -100 μA		MIN to MAX	V _{CC} -0.2	2			
Vou	lau 10 mA		2.7 V	2.2			v	
Voн	IOH = - 12 IIIA	IOH = - 12 mA		2.4			V	
	I _{OH} = -24 mA		3 V	2			j	
	I _{OL} = 100 μA		MIN to MAX			0.2		
VOL	I _{OL} = 12 mA		2.7 V			0.4	v	
	I _{OL} = 24 mA		3 V			0.55		
lj.	V _I = 5.5 V or GND		3.6 V			±5	μА	
loz	VO = VCC or GND		3.6 V			±10	μА	
lcc	V _I = V _{CC} or GND,	IO = 0	3.6 V			20	μА	
ΔlCC	One input at V _{CC} - 0.6 V,	Other inputs at VCC or GND	3 V to 3.6 V			500	μА	
Ci	VI = VCC or GND		3.3 V		5.5		pF	
Со	VO = VCC or GND		3.3 V		5.8		pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	3.3 V 3 V	V _{CC} =	2.7 V	UNIT
	(114-01)	(001701)	MIN	MAX	MIN	MAX	
^t pd	Α	Ý	1.5	7.5		8.5	ns
^t en	ŌĒ	Y	1.5	8		9	ns
^t dis	ŌĒ	Y	1.5	7.5		8.5	ns

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SCAS293A - JANUARY 1993 - REVISED JULY 1995

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT	
	Dower discinction conscitones nor buffer/driver	Outputs enabled	C ₁ = 50 pF, f = 10 MHz	24	ρF
C _{pd}	Power dissipation capacitance per buffer/driver	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	2.5	рі

PARAMETER MEASUREMENT INFORMATION O 6 V **TEST** S1 500 Ω O Open From Output Open tpd **Under Test** GND 6 V tPLZ/tPZL GND tPHZ/tPZH CL = 50 pF **500** Ω (see Note A) 2.7 V LOAD CIRCUIT FOR OUTPUTS 1.5 V **Timing Input** tsu 2.7 V 1.5 V Input 1.5 V 1.5 V **Data Input** 0 V **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS PULSE DURATION** SETUP AND HOLD TIMES 2.7 V 2.7 V Output 1.5 V Input 1.5 V 1.5 V Control o v 0 V tpzL ^tPHL **tPLZ** Output VOH Waveform 1 1.5 V 1.5 V Output S1 at 6 V VOL (see Note B) tPHZ **tPLH** tPHL . Output Vон V_{OH} - 0.3 V Waveform 2 1.5 V Output S1 at GND - VOL (see Note B) **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS** PROPAGATION DELAY TIMES **ENABLE AND DISABLE TIMES INVERTING AND NONINVERTING OUTPUTS** LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



 EPIC™ (Enhanced-Performance Implanted **DB, DW, OR PW PACKAGE** (TOP VIEW) **CMOS) Submicron Process** Typical V_{OLP} (Output Ground Bounce) 10E [20 D VCC < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 1A1 🛮 2 19 20E Typical V_{OHV} (Output V_{OH} Undershoot) 2Y4 🛛 3 18 1Y1 > 2 V at V_{CC} = 3.3 V, T_A = 25°C 1A2 **[**]4 17**∏** 2A4 Supports Mixed-Mode Signal Operation on 2Y3 [5 16 1Y2 All Ports (5-V Input/Output Voltage With 1A3 🛮 6 15 2A3 3.3-V V_{CC}) 2Y2 [7 14 1 1Y3 Package Options Include Plastic 1A4 **[**8 13 2A2 Small-Outline (DW), Shrink Small-Outline 2Y1 ∏9 12 1Y4 (DB), and Thin Shrink Small-Outline (PW) GND 1 10 11 1 2A1

description

Packages

This octal buffer/line driver is designed for 2.7-V to 3.6-V V_{CC} operation; it can interface to a 5-V system environment.

The SN74LVC241 is designed specifically to improve both the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'LVC240 and 'LVC244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical \overline{OE} (active-low output-enable) inputs, and complementary OE and \overline{OE} inputs.

The SN74LVC241 is organized as two 4-bit line drivers with separate output-enable $(1\overline{OE}, 2OE)$ inputs. When $1\overline{OE}$ is low or 2OE is high, the device passes data from the A inputs to the Y outputs. When $1\overline{OE}$ is high or 2OE is low, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking or the current-sourcing capability of the driver.

The SN74LVC241 is characterized for operation from -40°C to 85°C.

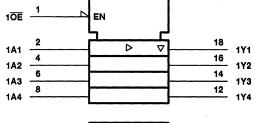
FUNCTION TABLES

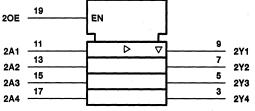
INP	JTS	OUTPUT
10E	1A	1Y
L	Н	Н
L	L	L
Н	Х	Z

INP	JTS	OUTPUT
20E	2A	2Y
Н	Н	Н
Н	L	L
L	Х	z

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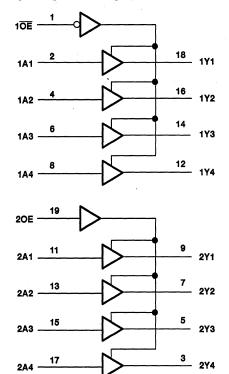
logic symbolt





[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

PW package 0.7 W

 3
Supply voltage range, V _{CC} –0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)
Voltage range applied to any output in the high-impedance state
or power-off state, V _O (see Note 1)
Voltage range applied to any output in the high
or low state, V _O (see Notes 1 and 2)
Input clamp current, $I_{ K }(V_1 < 0)$ —50 mA
Output clamp current, I_{OK} ($V_O < 0$)
Continuous output current, I _O (V _O = 0 to V _{CC}) ±50 mA
Continuous current through VCC or GND
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB package
DW package 1.6 W

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Storage temperature range, T_{stg} -65°C to 150°C

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Voc	Cumply voltage	Operating	2	3.6	V
VCC	Supply voltage	Data retention only	1.5		٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
VI	Input voltage		0	5.5	V
V-	Output voltage	High or low state	0	VCC	v
Vo		3 state	0	5.5	v
lou	High-level output current	V _{CC} = 2.7 V		-12	-m A
ЮН		V _{CC} = 3 V		-24	mA
lo:	Low-level output current	V _{CC} = 2.7 V		12	mA
lor 	V _{CC} = 3 V			24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.



SN74LVC241 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS SCAS343A - MARCH 1994 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CO	TEST CONDITIONS			TYP‡	MAX	UNIT
	I _{OH} = -100 μA		MIN to MAX	V _{CC} -0.	.2		
V	la 10 mA	I _{OH} = - 12 mA		2.2			v
VOH	IOH = - 12 MA			2.4			V
	I _{OH} = -24 mA		3 V	2.2			
	I _{OL} = 100 μA		MIN to MAX			0.2	
VOL	I _{OL} = 12 mA		2.7 V			0.4	V
	I _{OL} = 24 mA		3 V			0.55	
ΙΙ	V _I = 5.5 V or GND		3.6 V			±5	ιμΑ
loz	V _O = 5.5 V or GND		3.6 V			±10	μА
lcc	V _I = V _{CC} or GND,	I _O = 0	3.6 V			20	μА
ΔlCC	One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			500	μА
Ci	V _I = V _{CC} or GND		3.3 V				pF
Co	V _O = V _{CC} or GND		3.3 V				pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

SCAS414C - NOVEMBER 1992 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE (TOP VIEW)

. == [Γ.	U		h.,
10E [1		20	Vcc
1A1 [2		19	20E
2Y4 [3		18] 1Y1
1A2 [4			2A4
2Y3 [5			1Y2
1A3 [6		15	2A3
2Y2 [7		14] 1Y3
1A4 [8		13	2A2
2Y1 [9		12] 1Y4
GND [10		11	2A1

description

This octal buffer/line driver is designed for 2.7-V to 3.6-V V_{CC} operation; it can interface to a 5-V system environment.

The SN74LVC244A is organized as two 4-bit line drivers with separate output-enable \overline{OE} inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC244A is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each buffer)

INPUTS		OUTPUT				
ŌĒ	Α	Y				
	Н	Н				
L	L	L				
Н	Χ	Z				

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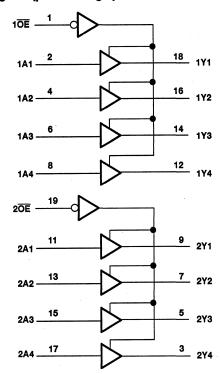
Products conform to specification standard warranty. Production pro

logic symbolt

1OE ΕN 2 18 16 1A2 6 14 1Y3 1A3 12 8 174 1A4 2OE ΕN 11 D 2A1 7 13 2Y2 5 15 **2A3** 17 3 2Y4 2A4

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	-0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)	-0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance state	
or power-off state, VO (see Note 1)	-0.5 V to 6.5 V
Voltage range applied to any output in the high	
or low state, V _O (see Notes 1 and 2)	to $V_{CC} + 0.5 V$
Input clamp current, I_{IK} ($V_I < 0$)	
Output clamp current, I_{OK} ($V_O < 0$)	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	
Continuous current through V _{CC} or GND	
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): DB package	
DW package	1.6 W
PW package	0.7 W
Storage temperature range, T _{stg}	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

^{2.} This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V	Supply voltage	Operating	2	3.6	, ,
VCC		Data retention only	1.5		V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
٧ _I	Input voltage	Input voltage		5.5	V
V _O Ou	Output voltage	High or low state	0	Vcc	c v
		3 state	0	5.5	, v
		V _{CC} = 2.7 V	-12		A
ЮН	High-level output current	V _{CC} = 3 V		-24	mA
1		V _{CC} = 2.7 V		12	
IOL	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcct	MIN TYP‡	MAX	UNIT	
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			
Vari	I _{OH} = - 12 mA	2.7 V	2.2		٧	
VOH	IOH = - 12 IIIA	3 V	2.4			
	$I_{OH} = -24 \text{ mA}$	3 V	2.2			
	I _{OL} = 100 μA	MIN to MAX		0.2	2	
v_{OL}	I _{OL} = 12 mA	2.7 V		0.4	٧	
	I _{OL} = 24 mA	3 V		0.55		
l _l	V _I = 5.5 V or GND	3.6 V		±5	μΑ	
lo-	$V_O = 5.5 \text{ V or GND}$	3.6 V		±10	μА	
loz	V _O = 3.6 V or 5.5 V	MIN to MAX		±50	μΛ	
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		10	μА	
ΔlCC	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μА	
Ci	V _I = V _{CC} or GND	3.3 V	3.1		рF	
Co	V _O = V _{CC} or GND	3.3 V	5		pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	
			MIN	MAX	MIN	MAX	
^t pd	A	Y	1.5	6.5		7.5	ns
ten	ŌĒ	Y	1.5	8		9	ns
^t dis	ŌĒ	Υ	1.5	7		8	ns
t _{sk(o)} §				1			ns

[§] Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.



[‡] All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per buffer/driver	Outputs enabled	O. 50 -5 4 40 MH-	30	
	Power dissipation capacitance per buffer/driver	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	2

PARAMETER MEASUREMENT INFORMATION 6 V TEST S1 500 Ω O Open Open ^tpd From Output 6 V tpLZ/tpZL **GND Under Test GND** tPHZ/tPZH CL = 50 pF 500 Ω (see Note A) 2.7 V LOAD CIRCUIT FOR OUTPUTS 1.5 V **Timing Input** tsu 2.7 V 1.5 V Input 1.5 V **Data Input** 1.5 V 0 V **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS PULSE DURATION** SETUP AND HOLD TIMES 2.7 V 2.7 V Output 1.5 V 1.5 V 1.5 V Input Control n v t_{PZL} ^tPLH **tPHL tPLZ** Output ۷он Waveform 1 1.5 V Output 1.5 V S1 at 6 V VOL (see Note B) tPHZ**tPLH** tPHL ─ tpzH -Output VOH Waveform 2 V_{OH} - 0.3 V Output 1.5 V S1 at GND ≈ 0 V (see Note B) **VOLTAGE WAVEFORMS** VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES **ENABLE AND DISABLE TIMES INVERTING AND NONINVERTING OUTPUTS** LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms



SCES009 - JULY 1995

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-833C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Shrink Small-Outline (DB), Plastic Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE (TOP VIEW)



description

This octal buffer/line driver is designed for 2.7-V to 3.6-V V_{CC} operation; it can interface to a 5-V system environment.

The SN74LVCH244 is organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

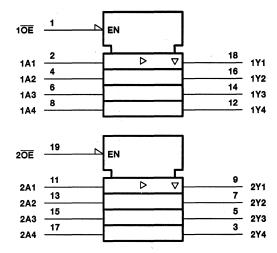
The SN74LVCH244 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each buffer)

INP	JTS	OUTPUT
ŌĒ	Α	Y
L	Н	Н
L.	L	L
Н	Х	Z

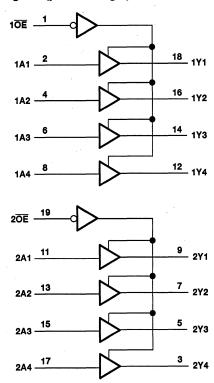
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



 † This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SCES009 - JULY 1995

absolute maximum ratings over operating free-air temperature range (u	ınless otherwise noted)†
Supply voltage range, V _{CC}	–0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high-impedance	
or power-off state, V _O (see Note 1)	0.5 V to 6.5 V
Voltage range applied to any output in the high	
or low state, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I _{IK} (V _I < 0)	– 50 mA
Output clamp current, I _{OK} (V _O < 0)	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB package	9 0.6 W
DW packag	e 1.6 W
PW package	e 0.7 W

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Storage temperature range, T_{stg} –65°C to 150°C

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V	Supply voltage Operating Data retention	Operating	2	3.6	v
VCC		Data retention only	1.5		v
ViH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
V _{JL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
٧į	Input voltage data inputs		0	5.5	٧
	Output voltage	High or low state	0 V _{CC}		v
Vo		3 state	0	5.5	, v
1	High-level output current	V _{CC} = 2.7 V		-12	4
ЮН		V _{CC} = 3 V		-24	mA
1	Low lovel cultural current	V _{CC} = 2.7 V		12	4
lOL	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcct	MIN TYP‡	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
V	la., 10 mA	2.7 V	2.2		v
VOH	I _{OH} = - 12 mA	3 V	2.4		v
	I _{OH} = -24 mA	3 V	2.2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
v _{OL}	I _{OL} = 12 mA	2.7 V		0.4	V
	I _{OL} = 24 mA	3 V		0.55	1
11	V _I = 5.5 V or GND	3.6 V		±5	μА
	V _I = 0.8 V	3 V	75		
l(hold)	V _I = 2 V	3 V	-75		μА
, ,	$V_{I} = 0 \text{ to } 3.6 \text{ V}$	3.6 V		±500	
	V _O = V _{CC} or GND	MIN to MAX		±10	4
loz	V _O = 3.6 V or 5.5 V	MIN to MAX		±50	μΑ
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		10	μA
Δlcc	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μА
Ci	V _I = V _{CC} or GND	3.3 V	3.1		pF
Co	V _O = V _{CC} or GND	3.3 V	5		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

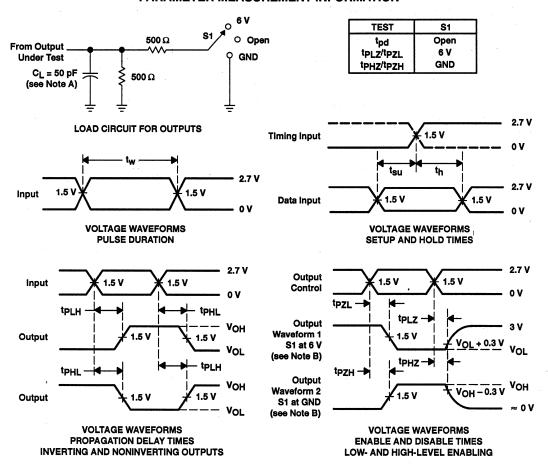
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	
			MIN	MAX	MIN	MAX	
t _{pd}	A or B	Υ	1.5	6.5		7.5	ns
t _{en}	ŌĒ	Υ	1.5	8		9	ns
^t dis	ŌĒ	Υ	1.5	7		8	ns
t _{sk(o)} †				1			ns

T Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$

PARAMETER		TEST CON	TYP	UNIT	
C _{pd} Power dissipation capacitance per buffer/driver	Outputs enabled	C ₁ = 50 pF.	f = 10 MHz	33	pF
	rower dissipation capacitance per buller/driver	Outputs disabled	CL = 50 pr,	1 = 10 WITZ	2

PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

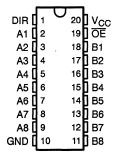
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_f ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpzL and tpzH are the same as ten.
- F. tpLZ and tpHZ are the same as tdis.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SCAS218D - JANUARY 1993 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- ESD Protection Exceeds 2000 V Per MIL-STD-883C. Method 3015: Exceeds 200 V Using Machine Model (C = 200 pF, R = 0
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) **Packages**

DB, DW, OR PW PACKAGE (TOP VIEW)



description

This octal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation; it can interface to a 5-V system environment.

The SN74LVC245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC245A is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

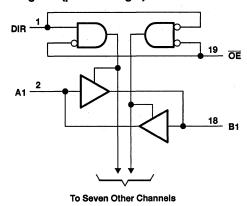
INP	UTS	OPERATION					
Œ	DIR	OPERATION					
L	L	B data to A bus					
L	н	A data to B bus					
Н	х	Isolation					

EPIC is a trademark of Texas Instruments Incorporated

logic symbol[†]

G3 3EN1[BA] 3EN2[AB] ⊽ 1 В1 2∇ 17 **B2** 16 **B3** 15 **B4** 14 **B**5 13 **A6 B6** 8 12 **B7 B8**

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high-impedance state	
or power-off state, V _O (see Note 1)	0.5 V to 6.5 V
Voltage range applied to any output in the high	
or low state, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I _{OK} (V _O < 0)	
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3)	
, , , , , , , , , , , , , , , , , , , ,	DW package 1.6 W
	PW package 0.7 W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book. literature number SCBD002B.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V	Cumply walkage	Operating	2	3.6	V
VCC	Supply voltage	Data retention only	1.5		V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
۷ _I	Input voltage		0	5.5	V
.,	Output voltage	High or low state	0	Vcc	V
v _O		3 state	0	5.5	· •
1	High-level output current	V _{CC} = 2.7 V		-12	
ЮН		V _{CC} = 3 V		-24	mA
1	l and land and and an entered	V _{CC} = 2.7 V		12	4
lOL	Low-level output current	V _{CC} = 3 V	1	24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	vcct	MIN	TYP‡	MAX	UNIT
		I _{OH} = -100 μA	MIN to MAX	VCC-0.2	2		
\/~		la., 10 mA	2.7 V	2.2			v
МОН		IOH = - 12 mA	3 V	2.4			٧
		I _{OH} = -24 mA	3 V	2.2			
VOL		I _{OL} = 100 μA	MIN to MAX			0.2	
		I _{OL} = 12 mA	2.7 V			0.4	٧
		I _{OL} = 24 mA	3 V			0.55	
lį		V _I = 5.5 V or GND	3.6 V			±5	μА
1. 8		V _O = 5.5 V or GND	3.6 V			±10	
loz§		V _O = 3.6 V or 5.5 V	MIN to MAX			±50	μА
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			10	μА
∆lcc		One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	μА
Ci	Control inputs	VI = VCC or GND	3.3 V		3.3		pF
Cio	A or B ports	VO = VCC or GND	3.3 V		5.4		pF

For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC =	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	
			MIN	MAX	MIN	MAX	
^t pd	A or B	B or A	1.5	6.5		7.5	ns
^t en	ŌĒ	A or B	1.5	8.5		9.5	ns
^t dis	ŌĒ	A or B	1.5	7.5		8.5	ns
^t sk(o) [¶]				1			ns

[¶] Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.



[‡] All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

[§] For I/O ports, the parameter IOZ includes the input leakage current.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$

PARAMETER			TEST CONDITIONS	TYP	UNIT
	Down discinction conseitence not transcelves	Outputs enabled	Cı = 50 pF. f = 10 MHz	33	
Cpd	Power dissipation capacitance per transceiver	Outputs disabled	C _L = 50 pF, f = 10 MHz	2	pF

PARAMETER MEASUREMENT INFORMATION TEST S1 O Open 500 Ω From Output Open tpd **Under Test** O GND 6 V tpLZ/tpZL GND tPHZ/tPZH CL = 50 pF 500 Ω (see Note A) 2.7 V LOAD CIRCUIT FOR OUTPUTS 1.5 V Timing Input tsu 27 V 2.7 V 1.5 V Input 1.5 V 1.5 V **Data Input** 0 V **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS PULSE DURATION** SETUP AND HOLD TIMES 2.7 V 2.7 V Output 1.5 V 1.5 V Input 1.5 V 1.5 V Control 0 V 0 V **tPZL tPHL tPLH** tpLZ Output VOH Waveform 1 1.5 V 1.5 V 1.5 V Output S1 at 6 V VOL (see Note B) ^tPHZ tPHL -^tPZH Output Vон V_{OH} - 0.3 V V_{OH} Waveform 2 1.5 V 1.5 V Output S1 at GND - VOL (see Note B) **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS** PROPAGATION DELAY TIMES **ENABLE AND DISABLE TIMES INVERTING AND NONINVERTING OUTPUTS** LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_f ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpzL and tpzH are the same as ten.
 - F. tplz and tpHz are the same as tdis.
 - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SCES008 - JULY 1995

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-833C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltages With 3.3-VV_{CC})
- Bus Hold on Data Inputs Eliminates the Need for External Pullup Resistors
- Package Options Include Shrink Small-Outline (DB), Plastic Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages

DB,	DW,	OR	PW	PA	CKA	GE
	- (TOF	VIE	W١	ı	

			1
DIR [1	O 20	Vcc
A1 [2	19] OE
A2 [] B1
A3 [17] B2
A4 [16] B3
A5 [15] B4
A6 [14] B5
A7 [· 13] B6
A8 [9	12	B 7
GND [10	11] B8

description

This octal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation; it can interface to a 5-V system environment.

The SN74LVCH245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVCH245 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

INP	UTS	OPERATION
ŌĒ	DIR	OPERATION
L	L	B data to A bus
L	н	A data to B bus
Н	Х	Isolation

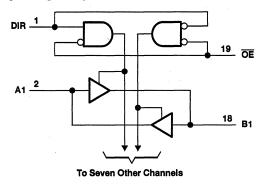
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SCES008 - JULY 1995

logic symbolt

ŌĒ G3 3EN1[BA] 3EN2[AB] В1 Δ 2∇ 17 **B2** 16 В3 5 15 R4 14 **B**5 7 13 A6 **B6** 8 12 **B7** 9 11 **B8**

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} –0.5 V to	6.5 V
Input voltage range, V _I (see Note 1)	6.5 V
Voltage range applied to any output in the high-impedance	
or power-off state, V _O (see Note 1)	6.5 V
Voltage range applied to any output in the high	
or low state, V _O (see Notes 1 and 2)	0.5 V
Input clamp current, $I_{ K }(V_1 < 0)$ — 5	60 mA
Output clamp current, I_{OK} ($V_O < 0$) ± 5	50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) $\pm $	60 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): DB package	
DW package	1.6 W
PW package	0.7 W
Storage temperature range, T _{stg} –65°C to	

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
V	Supply voltage	Operating	2 3.6		V	
VCC		Data retention only	1.5		· ·	
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧	
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧	
VI	Input voltage data inputs		0	5.5	٧	
V-	Output voltage	High or low state	0	VCC V		
v _O		3 state	0	5.5		
1	High-level output current	V _{CC} = 2.7 V		-12	T	
ЮН		V _{CC} = 3 V		-24	mA	
1		V _{CC} = 2.7 V		12	mA	
IOL	Low-level output current	V _{CC} = 3 V		24		
Δt/Δν	Input transition rise or fall rate		0	10	ns/V	
TA	Operating free-air temperature	:	-40	85	°C	

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P	ARAMETER	TEST CO	ONDITIONS	v _{cc} t	MIN	TYP‡	MAX	UNIT
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -C).2			
V		10 10						V
VOH		I _{OH} = - 12 mA		3 V	2.4			V
		I _{OH} = -24 mA		3 V	2.2			
		I _{OL} = 100 μA		MIN to MAX			0.2	
VOL		I _{OL} = 12 mA					0.4	V
		I _{OL} = 24 mA	3 V			0.55		
II		V _I = 5.5 V or GND	3.6 V			±5	μА	
		V _I = 0.8 V		3 V	75			
l(hold)	ı	V _I = 2 V	3 V	-75			μА	
		V _I = 0 to 3.6 V	3.6 V			±500		
		VO = VCC or GND	VO = VCC or GND				±10	
loz§		V _O = 3.6 V or 5.5 V		MIN to MAX			±50	μΑ
ICC		VI = VCC or GND,	IO = 0	3.6 V			10	μА
Δlcc		One input at V _{CC} - 0.6 V,	Other inputs at VCC or GND	2.7 V to 3.6 V			500	μА
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V		3.3		pF
Cio	A or B ports	Vo = Vcc or GND		3.3 V		5.4		рF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions. ‡ All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C. § For I/O ports, the parameter I_{OZ} includes the input leakage current.

SN74LVCH245 OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES008 - JULY 1995

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

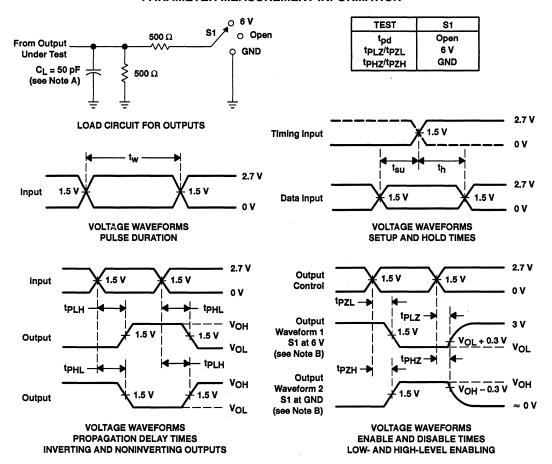
PARAMETER	FROM	TO	V _{CC} =	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	1.5	7		8	ns
t _{en}	ŌĒ	A or B	1.5	8.5		9.5	ns
^t dis	ŌĒ	A or B	1.5	7.5		8.5	ns
tsk(o) [†]				1			ns

[†] Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER			TEST CONDITIONS		
	Down discinsting conscitutes new transactions	Outputs enabled	0. 50-5	f = 10 MHz	36	pF
Cpd	Power dissipation capacitance per transceiver	Outputs disabled	C _L = 50 pF,	1 = 10 MINZ	2	pr

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq 2.5 \ ns$, $t_f \leq 2.5 \ ns$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SCAS375A - MARCH 1994 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- 3.3-V to 5-V Bidirectional Level Shifter
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

description

This 8-bit (octal) noninverting bus transceiver contains two separate supply rails; B port has V_{CCB} , which is set at 3.3 V, and A port has V_{CCA} , which is set to operate at 5 V. This allows for translation from a 3.3-V to a 5-V environment and vice versa.

DB, DW, OR PW PACKAGE (TOP VIEW)

(5 V) V _{CCA} [1	_	24	V _{CCB} (3.3 V)
DIR [2		23	D V _{CCB} (3.3 V)
A1 [3		22) OE
A2 [4		21] B1
A3 [5		20] B2
A4 [6		19] B3
A5 [7		18] B4
A6 [8		17] B5
A7 [9		16] B6
A8 [10		15] B7
GND [11		14] B8
GND [12		13	GND

The SN74LVC4245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

The SN74LVC4245 pinout allows the designer to switch to a normal all-3.3-V or all-5-V 20-pin '245 device without board re-layout. The designer uses the datapaths for pins 2 through 11 and 14 through 23 of the SN74LVC4245 to achieve the conventional '245 layout.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC4245 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

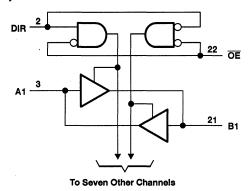
FORCTION TABLE					
INP	UTS	OPERATION			
ŌE	DIR	OPERATION			
L	L	B data to A bus			
L	Н	A data to B bus			
Н	Χ	Isolation			

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SCAS375A - MARCH 1994 - REVISED JULY 1995

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range for V_{CCA} at 5 V (unless otherwise noted)[†]

Supply voltage range, V_{CCA} . Input voltage range, V_{I} (see Note 1) Output voltage range, V_{O} (see Note 1) Input clamp current, I_{IK} (V_{I} < 0 or V_{I} > V_{CCA}) Output clamp current, I_{OK} (V_{O} < 0 or V_{O} > V_{CCA}) Continuous output current, I_{O} (V_{O} = 0 to V_{CCA}) Continuous current through each V_{CCA} or GND	-0.5 V to V _{CCA} + 0.5 V -0.5 V to V _{CCA} + 0.5 V -50 mA ±50 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 2) Storage temperature range, T_{Sto}	DW package

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. This value is limited to 6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

SCAS375A - MARCH 1994 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range for V_{CCB} at 3.3 V (unless otherwise noted)

Supply voltage range, V _{CCB} 0.5 V to 4.6 V
Input voltage range, V _I (except I/O ports) (see Note 3)
Input voltage range, V _I (I/O ports) (see Note 3)
Output voltage range, V _O (see Note 3)
Input clamp current, $I_{ K }(V_1 < 0)$ —50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CCB})
Continuous output current, I _O (V _O = 0 to V _{CCB})
Continuous current through V _{CCB} or GND ±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 2): DB package
DW package 1.7 W
PW package 0.7 W
Storage temperature range, T _{sto} —65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology

 Data Book, literature number SCBD002B.
 - 3. This value is limited to 4.6 V maximum.

recommended operating conditions for V_{CCA} at 5 V (see Note 4)

		MIN	MAX	UNIT
VCCA	Supply voltage	4.5	5.5	٧
V _{IH} .	High-level input voltage	2		٧
VIL	Low-level input voltage		0.8	٧
VI	Input voltage	0	VCCA	٧
VO	Output voltage	0	VCCA	٧
ЮН	High-level output current		-24	mA
loL	Low-level output current		24	· mA
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
TA	Operating free-air temperature	-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

recommended operating conditions for V_{CCB} at 3.3 V (see Note 4)

,			MIN	MAX	UNIT
VCCB	Supply voltage		2.7	3.6	V
VIH	High-level input voltage	V _{CCB} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CCB} = 2.7 V to 3.6 V		0.8	V
٧į	Input voltage		0	VCCB	٧
٧o	Output voltage		0	VCCB	V
lou	High level output ourrent	V _{CCB} = 2.7 V		-12	A
ЮН	High-level output current	V _{CCB} = 3 V		-24	mA
lo	Low-level output current	V _{CCB} = 2.7 V		12	^
lOL	V _{CCB} = 3 V			24	mA
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	. 85	•c

NOTE 4: Unused inputs must be held high or low to prevent them from floating.



SCAS375A - MARCH 1994 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range for V_{CCA} = 5 V (unless otherwise noted) (see Note 5)

PA	RAMETER	TEST CONDITIONS	VCCA	MIN	TYP	MAX	UNIT
		1004	4.5 V	4.3			
,		ΙΟΗ = -100 μΑ	5.5 V	5.3			V
VOH		L 04 A	4.5 V	3.7			V
		IOH = -24 mA	5.5 V	4.7			
		1 100 4	4.5 V			0.2	
l.,		I _{OL} = 100 μA	5.5 V			0.2	V
VOL		Jan. 04 mA	4.5 V			0.55	V
		I _{OL} = 24 mA	. 5.5 V			0.55	
l _l	Control inputs	V _I = V _{CCA} or GND	5.5 V			5	μА
loz‡	A or B ports	V _O = V _{CCA} or GND	5.5 V				μА
Icc		$V_I = V_{CCA}$ or GND, $I_O = 0$	5.5 V				μА
ΔICC§		One input at 3.4 V, Other inputs at V _{CCA} or GND					μА
Ci	Control inputs	V _I = V _{CCA} or GND	5 V				pF
Cio	A or B ports	V _O = V _{CCA} or GND	5 V				pF

[†] All typical values are measured at $V_{CC} = 3.3 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$.

electrical characteristics over recommended operating free-air temperature range for $V_{CCB} = 3.3 V$ (unless otherwise noted) (see Note 6)

PAI	RAMETER	TEST CO	ONDITIONS	V _{CCB} ¶	MIN	TYP	MAX	UNIT
		IOH = -100 μA		MIN to MAX	VCC-0	.2		
V		lov. 10 mA		2.7 V	2.2			- v
VOH		I _{OH} = -12 mA		3 V	2.4			٧
		I _{OH} = -24 mA		3 V	2			
		I _{OL} = 100 μA		MIN to MAX			0.2	
VOL		I _{OL} = 12 mA		2.7 V			0.4	V
		I _{OL} = 24 mA		3 V			0.55	
l _l	Control inputs	V _I = V _{CCB} or GND		3.6 V			5	μА
loz‡		VO = VCCB or GND		3.6 V				μА
Icc		V _I = V _{CCB} or GND,	I _O = 0	3.6 V				μА
ΔICC		One input at V _{CCB} - 0.6 V,	Other inputs at V _{CCB} or GND	2.7 V to 3.6 V				μА
Ci	Control inputs	V _I = V _{CCB} or GND		3.3 V				pF
C _{io}	A or B ports	VO = VCCB or GND		3.3 V				pF

[†] All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

NOTE 6: $V_{CCA} = 5 V \pm 0.5 V$



[‡] For I/O ports, the parameter IOZ includes the input leakage current.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or the corresponding V_{CC}. NOTE 5: V_{CCB} = 2.7 V to 3.6 V

For I/O ports, the parameter IOZ includes the input leakage current.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or the corresponding VCC.

[¶] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

SN74LVC257 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

SCAS294B - JANUARY 1993 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Inputs Accept Voltages to 5.5 V
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D,	DB,	OR	PW	PA	CKA	GI
		ďΩ	P VI	FW	١	

		7	1
Ā/B		U 16] v _{cc}
1A	[2	15] Œ
1B	[] 3		
1Y	[] 4] 4B
2A	[5	12] 4Y
2B	6	11	
2Y	[] 7	10] 3B
GND	8	9] 3Y
			ı

description

This quadruple 2-line to 1-line data selector/multiplexer is designed for 2.7-V to 3.6-V V_{CC} operation; it can interface to a 5-V system environment.

The SN74LVC257 is designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output enable (\overline{OE}) input is at a high logic level.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

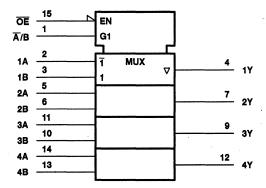
The SN74LVC257 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

	OUTPUT			
Œ	A/B	Α	В	Y
Н	Х	Х	Х	. Z
L	L	L	Х	L
L	L	Н	Χ	Н
L	Н	X	L	L
L	Н	Χ	Н	н

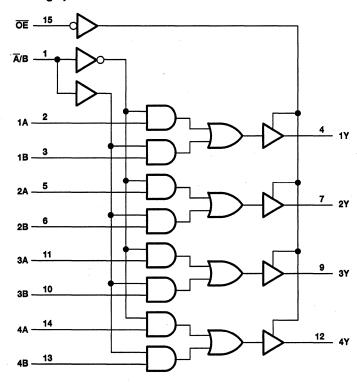
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





SN74LVC257 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

SCAS294B - JANUARY 1993 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)		0.5 V to 6.5 V
Output voltage range, VO (see Notes 1 and 2)	0.5	V to V_{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)		–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})		±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})		±50 mA
Continuous current through V _{CC} or GND		±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3)	: D package	1.3 W
	DB package	0.55 W
	PW package	0.5 W
Storage temperature range, T _{sto}		-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

		*	MIN	MAX	UNIT
\/	Cumplicustings	Operating	2	3.6	v
VIL Low-level input voltage VI Input voltage VO Output voltage IOH High-level output current IOL Low-level output current Δt/Δv Input transition rise or fall rate	Data retention only	1.5		V	
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		8.0	٧
٧ _I	Input voltage		0	5.5	V
V _O	Output voltage		0	VCC	٧
1	Lieb level evitevit eviment	V _{CC} = 2.7 V	1	-12	mA
ЮН	nign-level output current	. V _{CC} = 3 V		-24	IIIA
la.	Levy level entropy entropy	V _{CC} = 2.7 V		12	mA
OL	Low-level output current	V _{CC} = 3 V		24	IIIA
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

SN74LVC257 **QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER** WITH 3-STATE OUTPUTS SCAS294B - JANUARY 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} t	MIN TYP‡ I	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Vall	la 10 mA	2.7 V	2.2		ν
VOH	IOH = - 12 mA	3 V	2.4		v
	I _{OH} = -24 mA	3 V	2.2		
	l _{OL} = 100 μA	MIN to MAX		0.2	
VOL	I _{OL} = 12 mA	2.7 V		0.4	v
	I _{OL} = 24 mA	3 V		0.55	
lj :	V _I = 5.5 V or GND	3.6 V		±5	μА
loz	V _O = V _{CC} or GND	MIN to MAX		±10	μА
loc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		10	μА
ΔlCC	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μА
Ci	V _I = V _{CC} or GND	3.3 V	5		pF
Co	V _O = V _{CC} or GND	3.3 V	5		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	V _{CC} = ± 0.	3.3 V 3 V	V _{CC} =	2.7 V	UNIT
	(INPUT)	(001701)	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	. 1	7		8	
	Ā/B		1	8		9	ns
^t en	ŌĒ	Υ	1	8		9	ns
^t dis	ŌĒ	Y	1.	6		6.5	ns
t _{sk(o)} §				1			ns

[§] Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

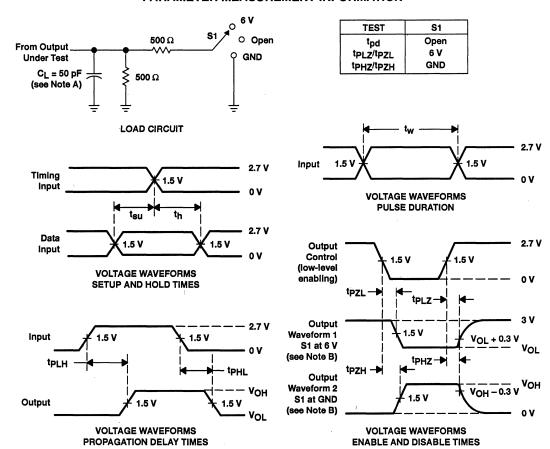
operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	C _L = 50 pF, f = 10 MHz	15.5	pF

 $[\]ddagger$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SCAS294B - JANUARY 1993 - REVISED JULY 1995

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \, \Omega$, $t_f \leq 2.5 \, \text{ns}$, $t_f \leq 2.5 \, \text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

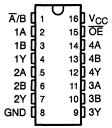
Figure 1. Load Circuit and Voltage Waveforms

SN74LVC258 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUPUTS

SCAS345A - MARCH 1994 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Typical V_{OLP} (Output Ground Bounce) $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) **Packages**
- Inputs Accept Voltages to 5.5 V

D. DB, OR PW PACKAGE (TOP VIEW)



description

This quadruple 2-line to 1-line data selector/multiplexer is designed for 2.7-V to 3.6-V V_{CC} operation; it can interface to a 5-V system environment.

The SN74LVC258 is designed to multiplex signals from 4-bit data sources to 4-output data lines in bus-organized systems. The 3-state outputs do not load the data lines when the output enable (\overline{OE}) input is at a high logic level.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC258 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

	INPL	OUTPUT		
ŌĒ	A/B	Α	В	Y
Н	Х	Х	Х	Z
L	L	L	х	Н
L	L	Н	X	L
L	н	X	L	н
L	н	X	Н	L

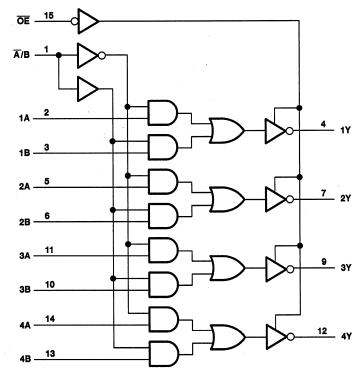
EPIC is a trademark of Texas Instruments Incorporated



15 ŌĒ ΕN 1 A/B G1 MUX 1A 3 1B 5 2A 6 2B 11 **3A** 10 3B 14 12 13 4B

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN74LVC258 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUPUTS

SCAS345A - MARCH 1994 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)	0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance state	
or power-off state, V _O (see Note 1)	0.5 V to 6.5 V
Voltage range applied to any output in the high	
or low state, V _O (see Notes 1 and 2)	V to V_{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): D package	1.3 W
DB package	
PW package	0.5 W
Storage temperature range, T _{stq}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

	,		MIN	MAX	UNIT	
V	Cumply valtage	Operating	2	3.6	٧	
VCC	Supply voltage	Data retention only	1.5		٧	
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V	
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧	
۷۱	Input voltage		0	VCC	٧	
v _O	Output voltage	High or low state	0	Vcc	V	
		3 state	0	5.5	V	
lau	High lovel autout august	V _{CC} = 2.7 V		-12	2	
ЮН	High-level output current	V _{CC} = 3 V		-24	mA	
lo	Low-level output current	V _{CC} = 2.7 V		12	mA	
lor	Low-level output current	V _{CC} = 3 V		24	ш	
Δt/Δν	Input transition rise or fall rate		0	10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: Unused inputs must be held high or low to prevent them from floating.



SN74LVC258 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUPUTS

SCAS345A - MARCH 1994 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcct	MIN TYP‡	MAX	UNIT	
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			
V	la 10 mA	2.7 V	2.2		v	
Voн	I _{OH} = - 12 mA	3 V	2.4		'	
	I _{OH} = -24 mA	3 V	2			
	I _{OL} = 100 μA	MIN to MAX		0.2		
VOL	I _{OL} = 12 mA	2.7 V		0.4	٧	
	I _{OL} = 24 mA	3 V		0.55		
4	V _I = V _{CC} or GND	3.6 V		±5	μΑ	
	V _O = V _{CC} or GND	MIN to MAX		±10	μА	
loz	$V_{O} = 3.6 \text{ V to } 5.5 \text{ V}$	WIIN to WAX		±50	μΑ	
ICC	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μΑ	
ΔICC	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μА	
Ci	V _I = V _{CC} or GND	3.3 V			pF	
Co	V _O = V _{CC} or GND	3.3 V			pF	

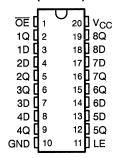
[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions. ‡ All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

SN74LVC373A OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS295C - JANUARY 1993 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted) **CMOS) Submicron Process**
- Typical V_{OLP} (Output Ground Bounce) $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB. DW. OR PW PACKAGE (TOP VIEW)



description

This octal transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation; it can interface to a 5-V system environment.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

OE does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC373A is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each latch)

- 6				
		INPUTS		OUTPUT
	ŌĒ	LE	D	Q
	L	Н	Н	Н
	L	Н	L	L
	L	L	Χ	Q_0
	Н	X	X	z

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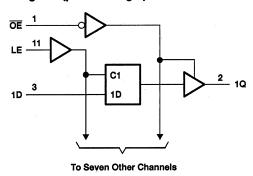
DALLAS, TEXAS 75265

SCAS295C - JANUARY 1993 - REVISED JULY 1995

logic symbolt

ŌĒ ΕN 11 C1 3 2 1D 1Q 1D 4 5 2D 2Q 6 3D **3Q** 8 9 4Q 4D 12 13 5D 5Q 14 15 6Q 6D 17 16 7D **7Q** 18 19 8D

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} —0. Input voltage range, V_{I} (see Note 1) —0.	.5 V to 6.5 V .5 V to 6.5 V
Voltage range applied to any output in the high-impedance state or power-off state, V _O (see Note 1)	
Voltage range applied to any output in the high or low state, V _O (see Notes 1 and 2)	V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) Output clamp current, I_{OK} ($V_O < 0$) Continuous current I_{OK} ($V_O < 0$)	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) Continuous current through V_{CC} or GND Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package	. ±100 mA
DW package PW package	1.6 W
Storage temperature range, T _{stg} 65	°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
V	Cumplus altage	Operating	2	3.6	v	
VCC	Supply voltage	Data retention only	1.5			
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧	
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧	
VI	Input voltage		0	5.5	٧	
v _o	Output voltage	High or low state	0	VCC	v	
		3 state	0	5.5	'	
1	LPSt. Level v. Av. A	V _{CC} = 2.7 V		-12		
ЮН	High-level output current	V _{CC} = 3 V		-24	mA	
1	Law law aloute the surrout	V _{CC} = 2.7 V	1	12	mA	
IOL	Low-level output current VCC = 3 V	V _{CC} = 3 V		24	,mA	
Δt/Δν	Input transition rise or fall rate		0	10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} t	MIN TY	P‡ MAX	UNIT	
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			
Vou	I _{OH} = – 12 mA	2.7 V	2.2		v	
Voн	IOH = - 12 IIIA	3 V	2.4		, v	
	I _{OH} = -24 mA		2.2			
	I _{OL} = 100 μA	MIN to MAX		0.2		
VOL	I _{OL} = 12 mA	2.7 V		0.4	V	
	I _{OL} = 24 mA	3 V		0.55		
4	V _I = 5.5 V or GND	3.6 V		±5	μА	
1	V _O = V _{CC} or GND	MIN to MAX		±10		
loz	V _O = 3.6 V or 5.5 V	WIIN to WAX		±50	μА	
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		10	μА	
ΔlCC	One input at V _{CC} – 0.6 V, Other inputs	at V _{CC} or GND 2.7 V to 3.6 V		500	μА	
C _i	V _I = V _{CC} or GND	3.3 V		3	pF	
Co	V _O = V _{CC} or GND	3.3 V	3	3.5	рF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V _{CC} = 3.3 V ± 0.3 V	V _{CC} = 2.7 V	UNIT
		MIN MAX	MIN MAX].
t _W	Pulse duration, LE high	3.3	3.3	ns
t _{su}	Setup time, data before LE↓	2	2	ns
th	Hold time, data after LE↓	1.5	1.5	ns

[‡] All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

SN74LVC373A **OCTAL TRANSPARENT D-TYPE LATCH** WITH 3-STATE OUTPUTS SCAS295C - JANUARY 1993 - REVISED JULY 1995

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

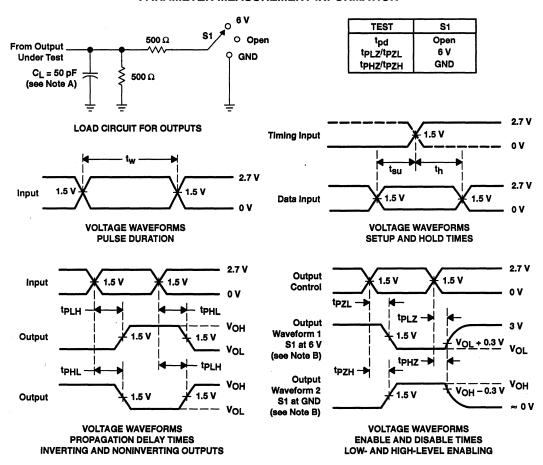
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	
		(001701)	MIN	MAX	MIN	MAX	
	D	Q	1.5	7.5		8.5	ns
^t pd	LE		2	8.5		9.5	
t _{en}	ŌĒ	Q	1.5	7.5		8.5	ns
^t dis	ŌĒ	Q	1.5	7		8	ns
t _{sk(o)} †	,			1			ns

[†] Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT	
C _{pd} Power dissipation capacitance per	Power dissinction conscitance per letch	Outputs enabled	Cı = 50 pF. f = 10 MHz	20	ρF
	Fower dissipation capacitance per laten	Outputs disabled	C _L = 50 pF, f = 10 MHz	3.5	ρг

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tplz and tpHz are the same as tdis.
- F. tp_{ZL} and tp_{ZH} are the same as t_{en} .
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SN74LVC374A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS296C - JANUARY 1993 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Supports Mixed-Mode Signal Operation on All Ports (5-V input/Output Voltage With 3.3-V V_{CC})
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB,	DW,	OR	PW	PACI	KAGE
	- 1	TOF	VIE	:wn	

			ì
ŌE		O 20	Vcc
1Q] 8Q
1D		18] 8D
2D (] 7D
2Q	5] 7Q
3Q] 6	15] 6Q
3D (14] 6D
4D] 5D
4Q	9	12] 5Q
GND	10	11	CLK

description

This octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation; it can interface to a 5-V system environment.

The SN74LVC374A features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, input/output (I/O) ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC374A is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each flip-flop)

	INPUTS		OUTPUT
ŌĒ	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	H or L	X	Q ₀
Н	X	Х	z

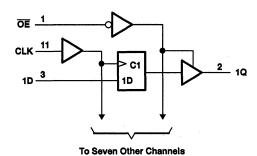
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TEXAS INSTRUMENTS
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logic symbol†

CLK C1 1D 1Q 5 2Q 2D 6 3D 3Q 8 9 4Q 4D 13 12 50 5D 14 15 6D 17 16 7Q 7D 18 19 8D

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} –0.5 V to 6.5 V	/
Input voltage range, V _I (see Note 1)	/
Voltage range applied to any output in the high impedance state	
or power off state, V _O (see Note 1)	/
Voltage range applied to any output in the high	
or low state, V _O (see Notes 1 and 2)	/
Input clamp current, $I_{ K }(V_1 < 0)$ —50 mA	٩
Output clamp current, I _{OK} (V _O < 0) ±50 mA	٩
Continuous output current, I _O (V _O = 0 to V _{CC}) ±50 m/s	٩
Continuous current through V _{CC} or GND ±100 m/	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB package	
DW package 1.6 W	
PW package 0.7 W	
Storage temperature range, T _{stq} –65°C to 150°C)

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
	Cumuluundhara	Operating	2	3.6		
VCC	Supply voltage	Data retention only	1.5		V	
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧	
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧	
٧١	Input voltage		0	5.5	٧	
٧o	Output voltage	High or low state	0	Vcc	-1 V 1	
		3 state	0	5.5		
1	High-level output current	V _{CC} = 2.7 V		-12	T	
ЮН		V _{CC} = 3 V		-24	mA	
1	Lavelaval autorit autorit	V _{CC} = 2.7 V		12	1	
lOL	Low-level output current	V _{CC} = 3 V		24	mA	
Δt/Δν	Input transition rise or fall rate		0	10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} †	MIN TYP‡	MAX	UNIT
	l _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
V	la 10 mA	2.7 V	2.2		ν
Voн	I _{OH} = - 12 mA	3 V	2.4		v
	I _{OH} = -24 mA	3 V	2.2		
	l _{OL} = 100 μA	MIN to MAX		0.2	
VOL	I _{OL} = 12 mA	2.7 V		0.4	V
	I _{OL} = 24 mA	3 V		0.55	
· II	V _I = 5.5 V or GND	3.6 V		±5	μА
	VO = VCC or GND	MIN to MAX		±10	μА
loz	$V_O = 3.6 \text{ V or } 5.5 \text{ V}$	IVIIIN TO IVIAX		±50	μΑ
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА
ΔlCC	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μА
Ci	V _I = V _{CC} or GND	3.3 V	3		pF
Co	V _O = V _{CC} or GND	3.3 V	3.5		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V _{CC}	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	
		MIN	MAX	MIN	MAX	
fclock	Clock frequency	0	100	0	80	MHz
t _w	Pulse duration, CLK high or low	3.3		3.3		ns
tsu	Setup time, data before CLK↑	1.5		1.5		ns
th	Hold time, data after CLK↑	1.5		1.5		ns

 $[\]ddagger$ All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

SN74LVC374A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS SCAS296C - JANUARY 1993 - REVISED JULY 1996

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

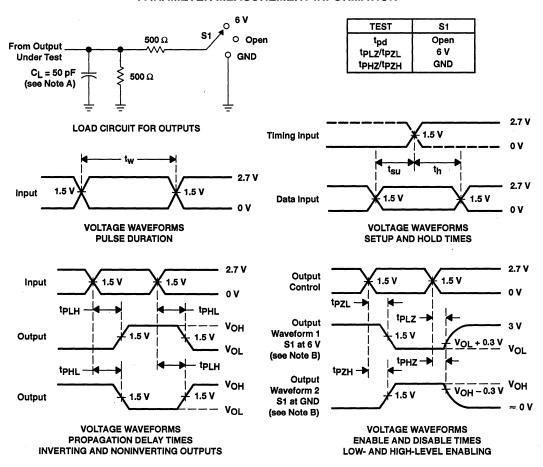
PARAMETER	RAMETER FROM TO (INPUT) (OUTPUT)		V _{CC} =	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	
		MIN	MAX	MIN	MAX	į	
f _{max}			100		80		MHz
t _{pd}	CLK	Q	1.5	8.5		9.5	ns
t _{en}	ŌĒ	Q	1.5	8.5		9.5	ns
^t dis	ŌĒ	Q	1.5	7		- 8	ns
t _{sk(o)} †			'	1			ns

[†] Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

	PARAMETER		TEST CONDITIONS	TYP	UNIT
C .	Power dissipation capacitance per flip-flop	Outputs enabled	C ₁ = 50 pF, f = 10 MHz	18	nE
Cpd	rower dissipation capacitance per hip-hop	Outputs disabled	CL = 50 pr, 1 = 10 Minz	9	p⊦

PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_r \leq 2.5 \,\text{ns}$, $t_f \leq 2.5 \,\text{ns}$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms

 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	DB, DW, OR PW PACKAGE (TOP VIEW)
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	OE1 1 20 V _{CC}
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	A1 2 19 0E2 A2 3 18 Y1 A3 4 17 Y2
 Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17 	A4 5 16 Y3 A5 6 15 Y4
 Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline 	A6 7 14 Y5 A7 8 13 Y6
(DB), and Thin Shrink Small-Outline (PW) Packages	A8 [] 9 12 [] Y7 GND [] 10 11 [] Y8

description

This octal buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC540 is ideal for driving bus lines or buffer memory address registers. The device features inputs and outputs on opposite sides of the package that facilitate printed-circuit-board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable (OE1 or OE2) input is high, all outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC540 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

	INPUTS		OUTPUT
OE1	OE2	Α	Y
L	L	L	Н
L	L	Н	L
Н	X	X	z
х	н	X	z

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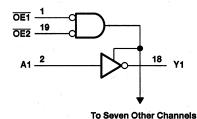


logic symbol†

EΝ OE₂ 18 17 Y2 A2 16 **Y3** ΑЗ 5 15 **Y4** 14 **A5** 13 **Y6** Α6 8 12 **Y7** Α7 11 **Y8**

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	
Continuous output current, I _O (V _O = 0 to V _{CC})	
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB package .	
	1.6 W
	0.7 W
Storage temperature range, Teta	

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MiN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
٧ı	Input voltage		0	5.5	٧
Vo	Output voltage		0	VCC	٧
1	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН		V _{CC} = 3 V		-24	
la.	Low-level output current	V _{CC} = 2.7 V		12	mA
IOL	Low-level output current	V _{CC} = 3 V		24	ША
Δt/ΔV	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} t	MIN TYP‡	MAX	UNIT
	i _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Vou	lou 10 mA	2.7	2.2		v
VOH	IOH = - 12 mA	3	2.4		. •
	i _{OH} = -24 mA	3	2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
VOL	I _{OL} = 12 mA	2.7		0.4	v
	I _{OL} = 24 mA	3		0.55	
lj .	V _I = 5.5 V or GND	3.6		±5	μА
loz	V _O = V _{CC} or GND	3.6		±10	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6		20	μА
ΔlCC	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V		500	μΑ
Ci	VI = VCC or GND	3.3	5.5		pF
Co	V _O = V _{CC} or GND	3.3	5.8		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

Ī	PARAMETER FROM TO (OUTPUT)		TO (OUTPUT)	V _{CC} =	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	
L		(114-01)	(001701)	MIN	MAX	MIN	MAX	
	^t pd	Α	Y	1.5	7.5		8.5	ns
	^t en	ŌĒ	Y	1.5	8		9	ns
	^t dis	ŌĒ	Y	1.5	7.5		8.5	ns

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CO	TYP	UNIT		
C _{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled Outputs disabled	C _L = 50 pF,	f = 10 MHz	27	pF

PARAMETER MEASUREMENT INFORMATION TEST S1 500 Ω O Open Open ^tpd From Output tpLZ/tpZL 6 V **GND Under Test GND** tPHZ/tPZH CL = 50 pF 500 Ω (see Note A) 2.7 V LOAD CIRCUIT FOR OUTPUTS 1.5 V **Timing Input** 27 V 1.5 V Input 1.5 V 1.5 V **Data Input** 0 V **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS PULSE DURATION** SETUP AND HOLD TIMES 2.7 V Output 1.5 V 1.5 V 1.5 V Input 1.5 V Control 0 V **tpz**L **tPHL tPLH tPLZ** Output 3 V VOH Waveform 1 Output 1.5 V 1.5 V S1 at 6 V VOL (see Note B) tPHZ → tpHL -^tPZH Output VOH Waveform 2 V_{OH} - 0.3 V 1.5 V Output S1 at GND (see Note B) **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS** PROPAGATION DELAY TIMES **ENABLE AND DISABLE TIMES** INVERTING AND NONINVERTING OUTPUTS LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq$ 2.5 ns, $t_t \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzi and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms



 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	DB, DW, OR PW PACKAGE (TOP VIEW)
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	OE1 1 20 V _{CC} A1 2 19 OE2
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	A2 3 18 Y1 A3 4 17 Y2
 Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17 	A4 0 5 16 Y3 A5 0 6 15 Y4
 Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline 	A6
(DB), and Thin Shrink Small-Outline (PW) Packages	A8 🛛 9 12 🗓 Y7 GND 🖟 10 11 🗓 Y8

description

This octal buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC541 is ideal for driving bus lines or buffering memory address registers. The device features inputs and outputs on opposite sides of the package to facilitate printed-circuit-board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output enable (OE1 or OE2) input is high, all eight outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

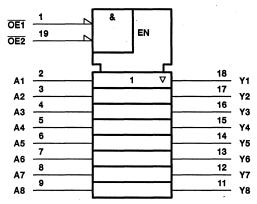
The SN74LVC541 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

	INPUTS	OUTPUT	
OE1	OE2	Α	Υ
L	L	L	L
L	L	Н	Н
н	X	X	z
х	н	Х	Z

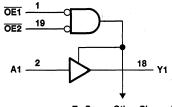
EPIC is a trademark of Texas Instruments Incorporated.

logic symbolt



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	–0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to 6.5 V
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3): DB package	0.6 W
DW package	1.6 W
PW package	0.7 W
Storage temperature range, T _{stq}	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
VI	Input voltage		0	5.5	٧
Vo	Output voltage		0	Vcc	٧
1	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН		V _{CC} = 3 V		-24	"IA
1	Law lavel autout aument	V _{CC} = 2.7 V	Τ .	12	mA
I _{OL} Low-level output current		V _{CC} = 3 V		24	mA
Δt/ΔV	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcct	MIN TYP#	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Vou	104	2.7	2.2		v
VOH	IOH = - 12 mA	3	2.4		V
	I _{OH} = -24 mA		2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
V _{OL}	I _{OL} = 12 mA	2.7		0.4	V
	I _{OL} = 24 mA	3		0.55	
l _l	V _I = 5.5 V or GND	3.6		±5	μА
loz	VO = VCC or GND	3.6		±10	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6		20	μΑ
ΔlCC	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V	,	500	μА
Ci	V _I = V _{CC} or GND	3.3	5.5		pF
Co	VO = VCC or GND	3.3	5.8		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	1 ±0.3 V 1		V _{CC} = 2.7 V	UNIT
	(INFOT)	(0011-01)	MIN	MAX	MIN MAX	
^t pd	A	Y	1.5	7	. 8	ns
ten	ŌĒ	· Y	1.5	8	9	ns
^t dis	ŌĒ	. Y	1.5	7.5	8.5	ns

 $[\]ddagger$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CO	TYP	UNIT		
	Power dissination conscitance per buffer/driver	Outputs enabled	C: 50 pE	f = 10 MHz	26.7	nE
Cpd Power dissipation capacitance per buffer/driver	Outputs disabled	$C_L = 50 pF$,	T = TO MINZ	1.8	pF	

PARAMETER MEASUREMENT INFORMATION 6 V TEST S1 **500** Ω Open Open ^tpd From Output tpLZ/tpZL 6 V Under Test GND tPHZ/tPZH GND CL = 50 pF 500 Ω (see Note A) 2.7 V LOAD CIRCUIT FOR OUTPUTS 1.5 V **Timing Input** 0 V tsu th 2.7 V 2.7 V 1.5 V Input 1.5 V 1.5 V **Data Input** 0 V 0 V **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS PULSE DURATION** SETUP AND HOLD TIMES 2.7 V 2.7 V Output 1.5 V 1.5 V Input 1.5 V Control 0 V 0 V **tPZL** ^tPHL **tPLH tPLZ** Output VOH Waveform 1 Output S1 at 6 V VOL (see Note B) tPHZ → **tPLH** tPHL: tpzH → Output VOH V_{OH} - 0.3 V Waveform 2 1.5 V Output S1 at GND VOL (see Note B) **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS**

NOTES: A. C_I includes probe and jig capacitance.

- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.

ENABLE AND DISABLE TIMES

LOW- AND HIGH-LEVEL ENABLING

- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.

PROPAGATION DELAY TIMES

INVERTING AND NONINVERTING OUTPUTS

- F. tpzl and tpzH are the same as ten.
- G. tplH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms



SN74LVC543 OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS299A - JANUARY 1993 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Typical VOLP (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2 V at V_{CC} = 3.3 V, T_A = 25 °C$
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) **Packages**

DB, DW, OR PW PACKAGE (TOP VIEW)

LEBA [₁ U	24] v _{cc}
OEBA [2	23	CEBA
A1 [22] B1
A2 [21] B2
A3 [] B3
A4 [] B4
A5 [] B5
A6 [] B6
A7 [] B7
A8 [1] B8
CEAB [14	LEAB
GND [12	13	OEAB

description

This octal registered transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC543 contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (CEAB) input must be low to enter data from A or to output data from B. If CEAB is low and LEAB is low, the A-to-B latches are transparent; a subsequent low-to-high transition of LEAB places the A latches in the storage mode. With CEAB and OEAB both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow for B to A is similar to that of A to B but uses CEBA, LEBA, and OFBA.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC543 is characterized for operation from -40°C to 85°C.

FUNCTION TABLET

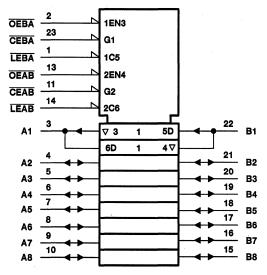
	INPUTS					
CEAB	LEAB	OEAB	Α	В		
Н	Х	Х	Х	Z		
X	X	Н	Х	z		
L	Н	L	X	в ₀ ‡		
L	L	L	L	L		
L	L	L	Н	н		

[†] A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

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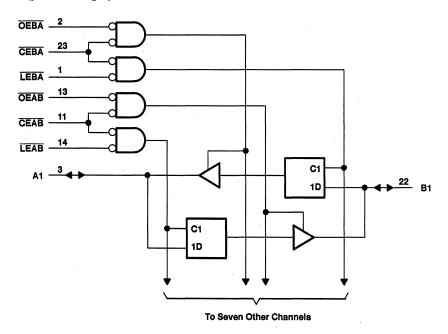
Output level before the indicated steady-state input conditions were established

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





SN74LVC543 OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS299A - JANUARY 1993 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

	0.7141 4.014
Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)	0.5 V to 6.5 V
i/O ports (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3)	: DB package 0.65 W
	DW package 1.7 W
	PW package 0.7 W
Storage temperature range, T _{sto}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	V
v_{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
٧ _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
VI	lanut voltage	Control inputs	0	5.5	V
	Input voltage	Data inputs	0	Vcc	v
V _O	Output voltage		0	VCC	٧
lavi	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН	nigirievei output current	V _{CC} = 3 V		-24	IIIA
la.	Law level cutout current	V _{CC} = 2.7 V		12	A
OL	Low-level output current VCC = 3 \			24	mA
Δt/Δν	Input transition rise or fall rate		0	. 10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

SN74LVC543 OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS299A - JANUARY 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	PARAMETER TEST CONDITIONS		v _{cc} †	MIN	TYP‡	MAX	UNIT	
		I _{OH} = -100 μA		MIN to MAX	V _{CC} -0.	2		
		iOH = - 12 mA		2.7 V	2.2			v
VOH		IOH = - 12111A		3 V	2.4			. *
		I _{OH} = -24 mA		3 V	2.2			
		I _{OL} = 100 μA		MIN to MAX			0.2	
V _{OL}		I _{OL} = 12 mA		2.7 V			0.4	٧
		I _{OL} = 24 mA	()	3 V			0.55	
i _l		V _I = 5.5 V or GND		3.6 V			±5	μА
IOZ§		VO = VCC or GND		3.6 V			±10	μА
Icc		V _I = V _{CC} or GND,	IO = 0	3.6 V			20	μА
ΔICC		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			500	μА
Ci	Control inputs	V _I = V _{CC} or GND	,	3.3 V		4.6		pF
Cio	A or B ports	VO = VCC or GND	· · · · · · · · · · · · · · · · · · ·	3.3 V		7.2		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
		MIN	MAX	MIN	MAX	
t _w	Pulse duration	4		4		ns
t _{su}	Setup time, data before LET or CET	1.5		1.5		ns
th	Hold time, data after LE↑ or CE↑	2.5		2.5		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	UNIT
	(INFOT)	(001701)	MIN	MAX	MIN MAX	
	A or B	B or A	1.5	8	9	
^t pd	LE	BOLA	1.5	9.5	10.5	ns
	ŌĒ	A B	1.5	8.5	9.5	
^t en	<u>CE</u>	A or B	1.5	9	10	ns
^t dis	ŌĒ	A or D	1.5	8.5	9.5	
	CE	A or B	1.5	9	. 10	ns

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. § For I/O ports, the parameter I_{OZ} includes the input leakage current.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER			TEST CO	TYP	UNIT	
	Power discination conscitance per transciver	Outputs enabled	C _I = 50 pF.	f = 10 MHz	32	nE
Opd	Power dissipation capacitance per transceiver	Outputs disabled	C[= 50 pr,	1 = 10 MHZ	4.6	p⊦

PARAMETER MEASUREMENT INFORMATION TEST S1 **500** Ω Open tpd From Output 6 V tPLZ/tPZL **Under Test** GND GND tPHZ/tPZH CL = 50 pF 500 Ω (see Note A) 2.7 V LOAD CIRCUIT FOR OUTPUTS 1.5 V Timing Input 0 V tsu 2.7 V 2.7 V 1.5 V Input 1.5 V 1.5 V **Data Input** o v **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS PULSE DURATION** SETUP AND HOLD TIMES 2.7 V 2.7 V Output 1.5 V 1.5 V Input Control ٥v 0 V tpzL **tPLH** tpLZ Output VOH Waveform 1 Output S1 at 6 V VOL (see Note B) tPHZ -^tPLH tPZH -Output ۷он ۷он Waveform 2 V_{OH} - 0.3 V 1.5 V Output S1 at GND VOL (see Note B) **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS** PROPAGATION DELAY TIMES **ENABLE AND DISABLE TIMES INVERTING AND NONINVERTING OUTPUTS** LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms



SN74LVC544 OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS346A - MARCH 1994 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

description

This octal registered transceiver is designed for 2.7-V to 3.6-V V_{CC} operation; it can interface to a 5-V system environment.

LEBA [24 🛛 V_{CC} OEBA [] 2 23 CEBA 22 🕅 B1 A1 [] 3 A2 🛮 4 21 B2 ΑЗΠ 20 N B3 19 B4 А4 П A5 [18 B5 17 N B6 A6 ∏ 8 A7 ∏ 9 16 N B7 A8 🛮 10 15 B8 14 🛭 LEAB CEAB 11 13 OEAB GND [12

DB, DW, OR PW PACKAGE (TOP VIEW)

The SN74LVC544 contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (CEAB) input must be low to enter data from A or to output data from B. If CEAB is low and LEAB is low, the A-to-B latches are transparent; a subsequent low-to-high transition of LEAB places the A latches in the storage mode. With CEAB and OEAB both low, the 3-state B outputs are active and reflect the inverted data present at the output of the A latches. Data flow from B to A is similar to A to B, but requires using the CEBA, LEBA, and OEBA.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC544 is characterized for operation from -40°C to 85°C.

FUNCTION TABLET

	INPUTS					
CEAB	LEAB	OEAB	A	В		
Н	Х	Х	Х	Z		
L'	Х	н	X	z		
L	Н	L	X	В ₀ ‡		
L	L	L	L	н		
L	L	L	Н	L		

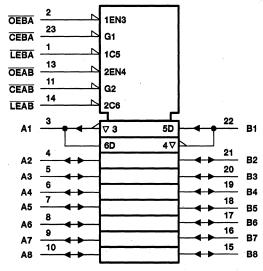
[†] A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

EPIC is a trademark of Texas Instruments Incorporated.



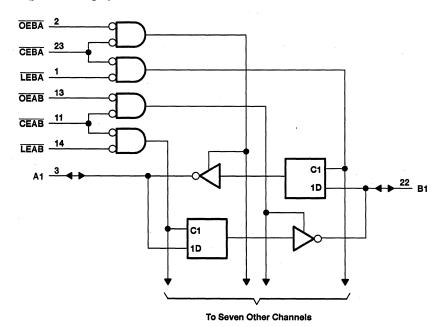
[‡] Output level before the indicated steady-state input conditions were established

logic symbolt



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN74LVC544 OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS346A - MARCH 1994 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5 V to 6.5 V
Input voltage range, V ₁
Voltage range applied to any output in the high impedance state or power off state,
V _O (see Note 1)
Voltage range applied to any output in the high or low state, Vo (see Note 1)0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)
Input clamp current, $I_{ K }(V_1 < 0)$ —50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})
Continuous output current, I _O (V _O = 0 to V _{CC})
Continuous current through V _{CC} or GND
Maximum power dissipation at TA = 55°C (in still air) (see Note 3): DB package
DW package 1.7 W
PW package 0.7 W
Storage temperature range, Teta

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V	Supply voltage	Operating	2	3.6	v
VCC		Data retention only	1.5		v
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V	T	0.8	٧
۷į	Input voltage		0	5.5	٧
\/-	Output voltage	High or low state	0	Vcc	V
v _O		3 state	0	5.5	v
1	I link lavel autout aumant	V _{CC} = 2.7 V	-12		4
ЮН	High-level output current	V _{CC} = 3 V		-24	mA
la.	Law lavel authorit aumont	V _{CC} = 2.7 V		12	4
IOL	Low-level output current VCC = 3 V			24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.



SN74LVC544 OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P/	PARAMETER TEST CONDITIONS			v _{cc} †	MIN	TYP‡	MAX	UNIT
		I _{OH} = -100 μA		MIN to MAX	V _{CC} -0.	2		
		10 4		2.7 V	2.2			.,
VOH		I _{OH} = - 12 mA		3 V	2.4			٧
		I _{OH} = -24 mA		3 V	2.2	,		
VoL		I _{OL} = 100 μA I _{OL} = 12 mA		MIN to MAX			0.2	
				2.7 V			0.4	V
		I _{OL} = 24 mA	·	3 V			0.55	
lį		V _I = 5.5 V or GND		3.6 V			±5	μА
IOZ§		V _O = 5.5 V or GND		3.6 V			±10	μА
Icc		V _I = V _{CC} or GND,	I _O = 0	3.6 V			20	μА
ΔlCC		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	μА
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V				pF
Cio	A or B ports	VO = VCC or GND		3.3 V				pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. § For I/O ports, the parameter I_{OZ} includes the input leakage current.

OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS300B - JANUARY 1993 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Typical V_{OLP} (Output Ground Bounce) $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) **Packages**

DB, DW, OR PW PACKAGE (TOP VIEW)

ŌĒ [1	U	20	vcc
1D [2		19] 1Q
2D [3		18	2Q
3D [4		17] 3Q
4D [5		16] 4Q
5D [6		15	5Q
6D [7		14] 6Q
7D [8		13	7Q
8D [9		12] 8Q
GND [10		11	LE

description

This octal transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation; it can interface to a 5-V system

The SN74LVC573A features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, input/output (I/O) ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without the need for interface or pullup components.

OE does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC573A is characterized for operation from -40°C to 85°C.

EPIC is a trademark of Texas Instruments Incorporated. PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas instruments standard warranty. Production processing does not necessarily include testing of all parameters.

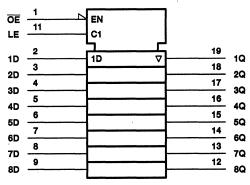


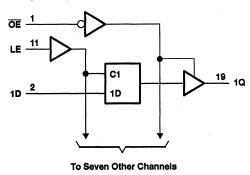
FUNCTION TABLE (each latch)

INPUTS			OUTPUT
ŌĒ	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	X	Q ₀
Н	X	X	z

logic symbolt

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} 0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)
Voltage range applied to any output in the high impedance state
or power off state, V _O (see Note 1)
Voltage range applied to any output in the high
or low state, V _O (see Notes 1 and 2)
Input clamp current, $I_{ K }(V_1 < 0)$ —50 mA
Output clamp current, I _{OK} (V _O < 0)
Continuous output current, IO (VO = 0 to VCC)
Continuous current through V _{CC} or GND
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB package
DW package 1.6 W
PW package 0.7 W
Storage temperature range, T _{sto}

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

This value is limited to 4.6 V maximum.

^{3.} The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
	Cumply vallage	Operating	2	3.6	ν
VCC	Supply voltage	Data retention only	1.5		٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
۷Į	Input voltage		0	5.5	٧
.,	Output valtage	Output voltage High or low state	0	VCC	v
VO	3 state	0	5.5	, v	
1	I line in the second	V _{CC} = 2.7 V		-12	A
ЮН	High-level output current	V _{CC} = 3 V		-24	mA
1	Law law law day day day and an amanda	V _{CC} = 2.7 V		12	
lOL	Low-level output current	output current V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} t	MIN TYP‡	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Vou	IOH = - 12 mA	2.7 V	2.2		v
VOH	IOH = - 12 IIIA	3 V	2.4		٧
	I _{OH} = -24 mA	3 V	2.2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
VOL	I _{OL} = 12 mA	2.7 V		0.4	٧
	I _{OL} = 24 mA	3 V		0.55	
l)	V _I = 5.5 V or GND	3.6 V		±5	μА
	VO = VCC or GND	MIN to MAX		±10	4
loz	V _O = 3.6 V or 5.5 V	IVIIN to IVIAX		±50	μΑ
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		10	μА
ΔlCC	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μА
Ci	VI = VCC or GND	3.3 V	3		pF
Co	VO = VCC or GND	3.3 V	3.5		рF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V _{CC} = 3.3 V ± 0.3 V	V _{CC} = 2.7 V	UNIT
		MIN MAX	MIN MAX	1
t _w	Pulse duration, LE high	3.3	3.3	ns
t _{su}	Setup time, data before LE↓	2	2	ns
th	Hold time, data after LE↓	1.5	1.5	ns



[‡] All typical values are measured at $V_{CC} = 3.3 \text{ V}$, $T_{A} = 25 ^{\circ}\text{C}$.

SN74LVC573A OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS300B - JANUARY 1993 - REVISED JULY 1995

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

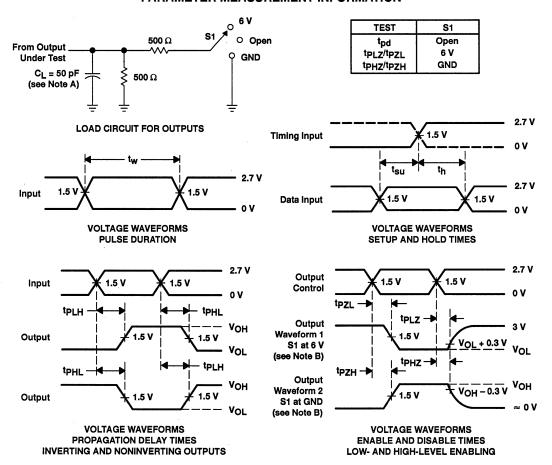
PARAMETER	PARAMETER FROM TO (OUTPUT)		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
	(114-01)	(001701)	MIN	MAX	MIN	MAX	
	D	0	1.5	7.5		8.5	
^t pd	LE	Q	2	8.5		9.5	ns
t _{en}	ŌĒ	Q	1.5	7.5		8.5	ns
tdis	ŌĒ	Q	1.5	7		8	ns
t _{sk(o)} †				1			ns

T Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT	
	Dower dissination conscitance per lately	Outputs enabled	C. FO. F. 10 MHz	20	~-
Cpd Power dissipation capacitance per latch	Outputs disabled	C _L = 50 pF, f = 10 MHz	3.5	p⊦	

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C₁ includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SN74LVC574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS301A - JANUARY 1993 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V Vcc)
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE (TOP VIEW)

1			
OE [O 20	Vcc
1D [2	19] 1Q
	3	18] 2Q
	4	17] 3Q
4D [5	16] 4Q
5D [6	15] 5Q
6D [7	14] 6Q
7D [8	13] 7Q
8D [9	12] 8Q
GND [10	11] CLK

description

This octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation; it can interface to a 5-V system environment.

The SN74LVC574A features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC574A is characterized for operation from -40°C to 85°C.

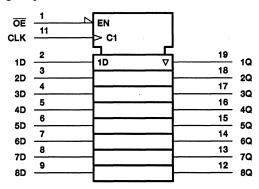
TEXAS INSTRUMENTS

SCAS301A - JANUARY 1993 - REVISED JULY 1995

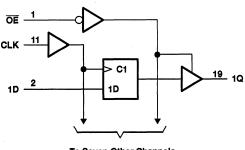
FUNCTION TABLE (each flip-flop)

INPUTS			OUTPUT
ŌĒ	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	L	Х	Q ₀
Н	X	Х	Z

logic symbol†



logic diagram (positive logic)



To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)	0.5 V to 6.5 V
Voltage range applied to any output in the high impedance state	
or power off state, VO (see Note 1)	0.5 V to 6.5 V
Voltage range applied to any output in the high	
or low state, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3)	: DB package 0.6 W
	DW package 1.6 W
	PW package 0.7 W
Storage temperature range, T _{stq}	

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SCAS301A - JANUARY 1993 - REVISED JULY 1995

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
	Cumplicus	Operating	2	3.6	v
vcc	Supply voltage	Data retention only	1.5		'
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
٧ _I	Input voltage		0	5.5	٧
	Output voltage High or low state 3 state	0	VCC	v	
v _O		3 state	0	5.5	'
1	High level autout aumont	V _{CC} = 2.7 V		-12	4
ЮН	High-level output current	V _{CC} = 3 V		-24	mA
	Law tard a same at	V _{CC} = 2.7 V		12	
IOL	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate	-	0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} t-	MIN TYP‡	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Vau	I _{OH} = - 12 mA	2.7 V	2.2		v
VOH	IOH = - 12 IIIA	3 V	2.4		V
	I _{OH} = -24 mA	3 V	2.2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
VOL	I _{OL} = 12 mA	2.7 V		0.4	٧
	I _{OL} = 24 mA	3 V		0.55	
l _l	V _I = 5.5 V or GND	3.6 V		±5	μА
	VO = VCC or GND	MIN to MAX		±10	4
loz	V _O = 3.6 V or 5.5 V	WIIN to WAX		±50	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		10	μА
ΔICC	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μА
Ci	V _I = V _{CC} or GND	3.3 V	3		pF
Co	V _O = V _{CC} or GND	3.3 V	3.5		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
		MIN	MAX	MIN	MAX	
fclock	Clock frequency	0	100	0	80	MHz
t _W	Pulse duration, CLK high or low	3.3		3.3		ns
t _{su}	Setup time, data before CLK↑	1.5		1.5		ns
th	Hold time, data after CLK↑	1.5		1.5		ns

 $[\]ddagger$ All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

SN74LVC574A **OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP** WITH 3-STATE OUTPUTS SCAS301A - JANUARY 1993 - REVISED JULY 1995

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	то (оитрит)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
	(INFOI)		MIN	MAX	MIN	MAX	
fmax			100		80		MHz
^t pd	D	Q	1.5	8.5		9.5	ns
t _{en}	ŌĒ	Q	1.5	7.5		8.5	ns
^t dis	ŌĒ	Q	1.5	7		8	ns
tsk(o) [†]				1			ns

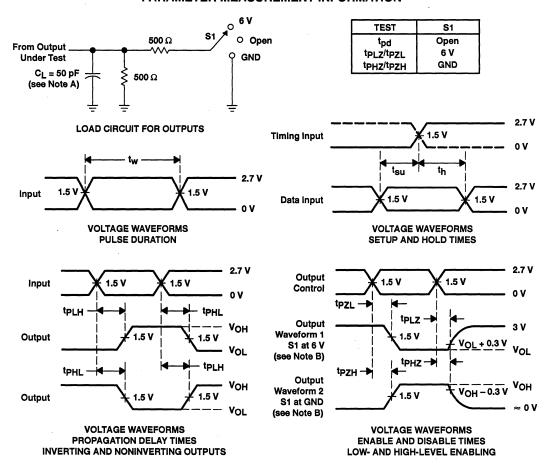
[†] Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	C ₁ = 50 pF. f = 10 MHz	18	ρF
		Outputs disabled	C _L = 50 pF, f = 10 MHz	9	рг

SCAS301A - JANUARY 1993 - REVISED JULY 1995

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \,\Omega$, $t_r \leq 2.5 \,ns$, $t_f \leq 2.5 \,ns$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms

SN74LVC646 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS302A - JANUARY 1993 - REVISED JULY 1995

 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	DB, DW, OR F (TOP	
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	CLKAB [1 SAB [2	24 V _{CC} 23 CLKBA
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	DIR [] 3 A1 [] 4	22 SBA 21 OE
 Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17 	A2 [] 5 A3 [] 6	20] B1 19] B2
 Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline 	A4 [] 7 A5 [] 8	18 DB3 17 DB4
(DB), and Thin Shrink Small-Outline (PW) Packages	A6 [] 9 A7 [] 10	16 B5 15 B6
description	A8 [] 11 GND [] 12	14 B7 13 B8

This octal bus transceiver and register is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC646 consists of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74LVC646.

Output-enable (OE) and direction-control (DIR) inputs control the transceiver functions. In the transceiver mode, data present at the high-impedance port can be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. DIR determines which bus receives data when \overline{OE} is low. In the isolation mode (\overline{OE} high), A data can be stored in one register and B data can be stored in the other register.

When an output function is disabled, the input function is still enabled and can be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC646 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

		INP	INPUTS			DATA	A I/Os	OPERATION OR FUNCTION
ŌĒ	DIR	CLKAB	CLKBA	SAB	SBA	A1 – A8	B1 – B8	OPERATION OR FUNCTION
X	Х	1	Х	Х	Х	Input	Unspecified [†]	Store A, B unspecified [†]
Х	Х	Х	1	X	Х	Unspecified [†]	Input	Store B, A unspecified [†]
Н	Х	1	1	Х	X	Input	Input	Store A and B data
Н	X	H or L	H or L	Х	Х	Input disabled	Input disabled	Isolation, hold storage
L	L	Х	Х	Х	L	Output	Input	Real-time B data to A bus
L	L	Х	H or L	X	Н	Output	Input	Stored B data to A bus
L	Н	Х	Х	L	Х	Input	Output	Real-time A data to B bus
ĹĹ	Н	H or L	Х	Н	Х	Input	Output	Stored A data to B bus

[†] The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition of the clock inputs.

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SCAS302A - JANUARY 1993 - REVISED JULY 1995

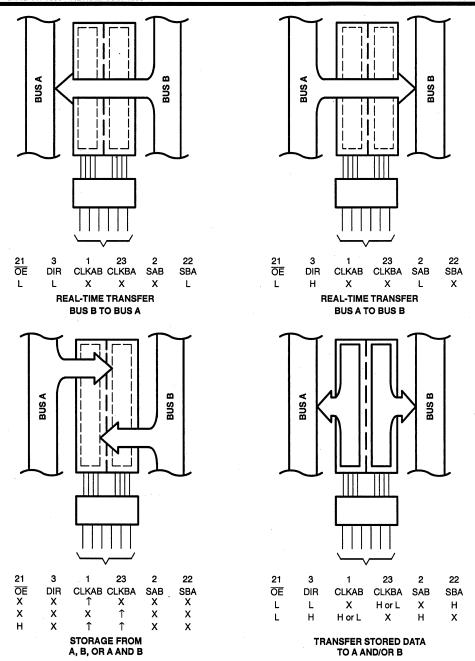
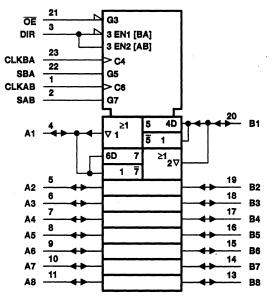


Figure 1. Bus-Management Functions

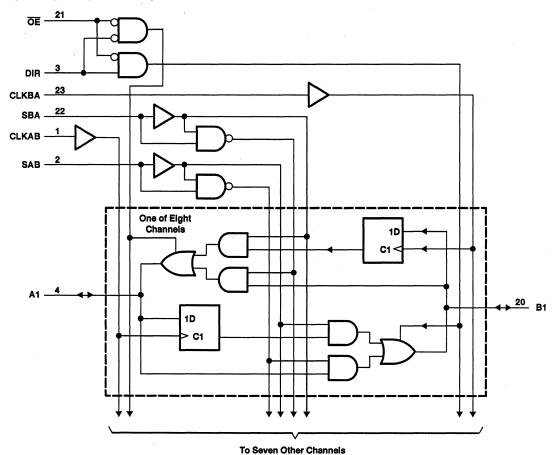


logic symbolt



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN74LVC646 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS302A - JANUARY 1993 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB p	ackage 0.65 W
DW;	package 1.7 W
PW	package 0.7 W
Storage temperature range, T _{sto}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	٧
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
۷ _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
V.	Input voltage	Control inputs	0	0.8 5.5 VCC VCC -12 -24	V
VĮ	input voltage	Data inputs	0	Vcc	v
٧o	Output voltage		0	Vcc	٧
lau	High-level output current	V _{CC} = 2.7 V		-12	A
ЮН	nigh-level output current	V _{CC} = 3 V		-24	mA
1	Lavelavel authorit auswant	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current	V _{CC} = 3 V		24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

SN74LVC646 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS302A - JANUARY 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	AMETER	TEST CONDITIONS	v _{cc} t	MIN TYP‡	MAX	UNIT
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
V		I _{OH} = – 12 mA	2.7 V	2.2		v
VOH		IOH = - 12 IIIA	3 V	2.4		V
		I _{OH} = -24 mA	3 V	2		
		I _{OL} = 100 μA	MIN to MAX		0.2	
VOL		I _{OL} = 12 mA	2.7 V		0.4	V
		I _{OL} = 24 mA	3 V		0.55	
IJ		V _I = 5.5 V or GND	3.6 V		±5	μА
loz§		V _O = V _{CC} or GND	3.6 V		±10	μА
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА
Δlcc		One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V		500	μА
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V	4.6		pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V	7.2		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

		V _{CC} =	3.3 V 3 V	VCC =		UNIT
		MIN	MAX	MIN	MAX	
t _w	Pulse duration	5		5		ns
t _{su}	Setup time, data before CLK↑	5		5		ns
th	Hold time, data after CLK↑	1		1		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	FROM TO		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	
	(INPO1)	(OUTPUT)	MIN	MAX	MIN	MAX	
f _{max}		i	100		80		MHz
	A or B	B or A	1.5	8		9.2	
^t pd	CLK	A or B	1.5	9		11	ns
	SBA or SAB	A or B	1.5	9		11	
t _{en}	ŌĒ	A or B	1.5	8.5		9.5	ns
^t dis	ŌĒ	A or B	1.5	8.5		9.5	ns
t _{en}	DIR	A or B	1.5	9		10	ns
^t dis	DIR	A or B	1.5	9		10	ns

[‡] All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

[§] For I/O ports, the parameter IOZ includes the input leakage current.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER			TEST CON	IDITIONS	TYP	UNIT
C _{pd}	Dower discination consultance nor transcriver	Outputs enabled	C: 50 pE	f 10 MU=	38	pF
	Power dissipation capacitance per transceiver	Outputs disabled	C _L = 50 pF, f = 10 MHz	1 = 10 WITZ	4.2	br

PARAMETER MEASUREMENT INFORMATION **TEST** S1 **500** Ω Open tpd From Output tPLZ/tPZL 6 V **Under Test** Q GND **GND** tPHZ/tPZH $C_L = 50 pF$ 500 Ω (see Note A) 2.7 V LOAD CIRCUIT FOR OUTPUTS 1.5 V Timing Input 0 V tsu 2.7 V 2.7 V 1.5 V Input 1.5 V 1.5 V **Data Input** 0 V ٥v **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS PULSE DURATION** SETUP AND HOLD TIMES 2.7 V 2.7 V Output 1.5 V 1.5 V Input 1.5 V 1.5 V Control 0 V 0 V **tPZL** ^tPLH **tPHL tPLZ** Output VOH Waveform 1 1.5 V Output S1 at 6 V VOL (see Note B) tPHZ **tPLH** tPHL tpzH -Output V_{OH} - 0.3 V Waveform 2 Output S1 at GND VOL (see Note B) **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS** PROPAGATION DELAY TIMES **ENABLE AND DISABLE TIMES** INVERTING AND NONINVERTING OUTPUTS LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_r \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tplz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tod.

Figure 2. Load Circuit and Voltage Waveforms



OCTAL BUS TRANSCEIVER AND REGIS WITH 3-STATE OUTPUTS

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SCAS303A - JANUARY 1993 - REVISED JULY 1995

 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	DB, DW, OR PW PACKAGI (TOP VIEW)	E
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	CLKAB 1 24 V _{CC} SAB 2 23 CLK	
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	OEAB 3 22 SBA A1 4 21 OEB	
 Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17 	A2 [5 20] B1 A3 [6 19] B2	
 Package Options include Plastic Small-Outline (DW), Shrink Small-Outline 	A4 [] 7 18] B3 A5 [] 8 17] B4	
(DB), and Thin Shrink Small-Outline (PW) Packages	A6 U 9 16 U B5 A7 U 10 15 U B6	

description

This octal bus transceiver and register is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC652 consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Output-enable (OEAB and OEBA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input selects real-time data, and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74LVC652.

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration, each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

To ensure the high-impedance state during power up or power down, OEBA should be tied to VCC through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The SN74LVC652 is characterized for operation from -40°C to 85°C.

SN74LVC652 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS SCAS303A - JANUARY 1993 - REVISED JULY 1995

FUNCTION TABLE

INPUTS			DATA I/OT			OPERATION OR FUNCTION		
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
L	Н	H or L	H or L	X	Х	Input	Input	Isolation
L	Н	1	1	X	х	Input	Input	Store A and B data
X	н	1	H or L	X	Х	Input	Unspecified‡	Store A, hold B
н	н	1	1	x‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	1	1	X	χ‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	x	н	Output	Input	Stored B data to A bus
Н	Н	X	Х	L	Х	Input	Output	Real-time A data to B bus
н	н	H or L	Х	Н	X	Input	Output	Stored A data to B bus
н	L	H or L	H or L	н	н	Output	Output	Stored A data to B bus and stored B data to A bus

[†] The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition on the clock inputs.

[‡] Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered in order to load both registers.

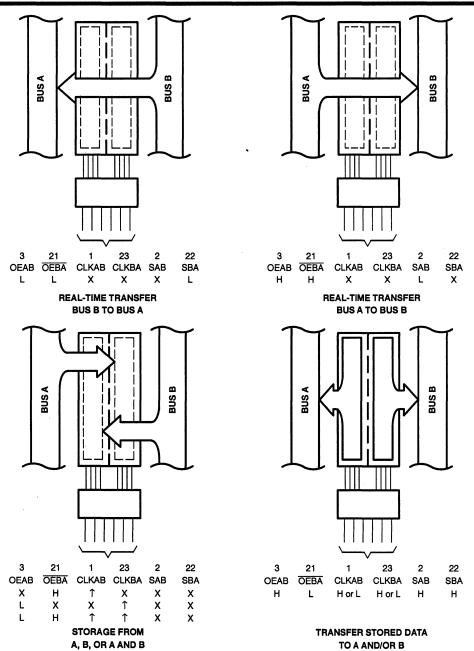
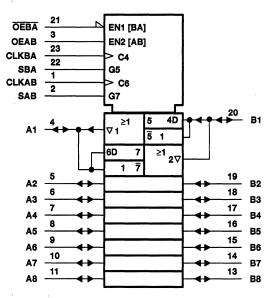


Figure 1. Bus-Management Functions

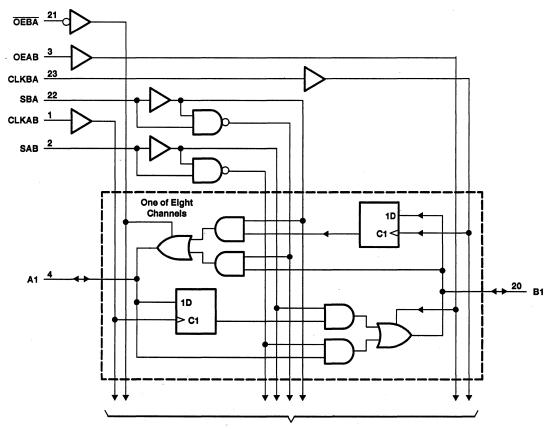


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels

SCAS303A - JANUARY 1993 - REVISED JULY 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} 0.5 V to 4.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)
I/O ports (see Notes 1 and 2)0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)0.5 V to VCC + 0.5 V
Input clamp current, I _{IK} (V _I < 0)
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)
Continuous output current, IO (VO = 0 to VCC) ±50 mA
Continuous current through V _{CC} or GND
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): DB package
DW package 1.7 W
PW package 0.7 W
Storage temperature range, T _{stg} –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V	Cumuluundhaan	Operating	2	3.6	v
VIH VIL VI VO	Supply voltage	Data retention only	1.5		· ·
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
VI	1	Control inputs	0	5.5	v
	Input voltage Data	Data inputs	0	Vcc	V
Vo	Output voltage		0	Vcc	٧
1	Light level cute it coment	V _{CC} = 2.7 V		-12	^
ЮН	High-level output current	V _{CC} = 3 V	2 3.0 1.5 2 0.6 0 5.0 0 V _{CC} 0 V _{CC} -1: -2.0 1.2 0 11	-24	mA
1	Laveland autoritaria	V _{CC} = 2.7 V		12	
IOL	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

SCAS303A - JANUARY 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P/	RAMETER	TEST CONDITIONS	v _{cc} t	MIN TYP#	MAX	UNIT
		IOH = -100 μA	MIN to MAX	V _{CC} -0.2		
V		10 mA	2.7 V	2.2		v
VOH		IOH = - 12 mA	3 V	2.4		, v
		I _{OH} = -24 mA	3 V	2		
		I _{OL} = 100 μA	MIN to MAX		0.2	
VOL		I _{OL} = 12 mA	2.7 V		0.4	V
		I _{OL} = 24 mA	3 V		0.55	
II		V _I = 5.5 V or GND	3.6 V		±5	μА
IOZ§		V _O = V _{CC} or GND	3.6 V		±10	μА
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА
Δlcc		One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V		500	μА
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V	4.6		pF
Cio	A or B ports	V _O = V _{CC} or GND	3.3 V	7.2		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

		V _{CC} =	3.3 V 3 V	V _{CC} =	2.7 V	UNIT
		MIN	MAX	MIN	MAX	
fclock	Clock frequency	0	100	0	80	MHz
t _w	Pulse duration	5		5		ns
t _{su}	Setup time, data before CLK↑	5		5		ns
th	Hold time, data after CLK↑	1		1		ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	
	(INPOT)	(001701)	MIN	MAX	MIN	MAX	
fmax			100		80		MHz
	A or B	B or A	1.5	. 8		9.2	
t _{pd}	CLK	A or B	1.5	9		11	ns
	SAB or SBA	A or B	1.5	9		11	
^t en	ŌĒ	A or B	1.5	8.5		9.5	ns
t _{dis}	ŌĒ	A or B	1.5	8.5		9.5	ns
∟ t _{en}	OE	A or B	1.5	9		10	ns
^t dis	OE	A or B	1.5	9		10	ns

[‡] All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

[§] For I/O ports, the parameter IOZ includes the input leakage current.

SCAS303A - JANUARY 1993 - REVISED JULY 1995

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT	
C .	Power dissipation conscitance per transceiver	Outputs enabled	Cr = 50 pF. f = 10 MHz	38	nE
Cpd	Power dissipation capacitance per transceiver	Outputs disabled	C _L = 50 pF, f = 10 MHz	4.2	p⊢

PARAMETER MEASUREMENT INFORMATION 6 V TEST S1 **500** Ω O Open Open tod From Output 6 V tPLZ/tPZL **Under Test** GND tPHZ/tPZH **GND** CL = 50 pF 500 Ω (see Note A) 2.7 V LOAD CIRCUIT FOR OUTPUTS 1.5 V Timing Input tsu th 2.7 V 2.7 V 1.5 V Input Data Input 1.5 V 1.5 V 0 V 0 V **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS PULSE DURATION** SETUP AND HOLD TIMES 2.7 V 2.7 V Output 1.5 V 1.5 V 1.5 V 1.5 V Input Control 0 V **tPZL tPLH** ^tPHL tpLZ Output VOH Waveform 1 1.5 V 1.5 V Output S1 at 6 V VOL (see Note B) tPHZ → **t**PLH tPHL tpzH Output VOH Waveform 2 VOH - 0.3 1.5 V 1.5 V Output S1 at GND VOL (see Note B) **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS** PROPAGATION DELAY TIMES **ENABLE AND DISABLE TIMES** INVERTING AND NONINVERTING OUTPUTS LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tod.

Figure 2. Load Circuit and Voltage Waveforms



10-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

13**∏** CLK

SCAS304A - MARCH 1993 - REVISED JULY 1995

 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	DB, DW, OR PW PACKAGE (TOP VIEW)
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	OE 1 24 V _{CC}
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	2D [] 3 22 [] 2Q 3D [] 4 21 [] 3Q
 Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17 	4D [[5 20]] 4Q 5D [[6 19]] 5Q
 Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline 	6D []7 18]] 6Q 7D []8 17]] 7Q
(DB), and Thin Shrink Small-Outline (PW) Packages	8D []9 16 [] 8Q 9D []10 15 [] 9Q
● Inputs Accept Voltages to 5.5 V	10D []11 14 [] 10Q

description

This 10-bit bus-interface flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC821 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

GND II 12

The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable (\overline{OE}) input can be used to place the ten outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (OE) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC821 is characterized for operation from -40°C to 85°C.

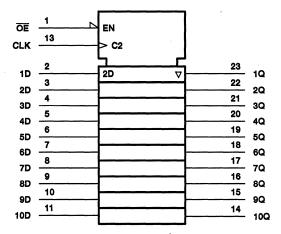
FUNCTION TABLE (each flip-flop)

	INPUTS	OUTPUT	
ŌĒ	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	H or L	Χ	Q ₀
Н	Х	Х	Z

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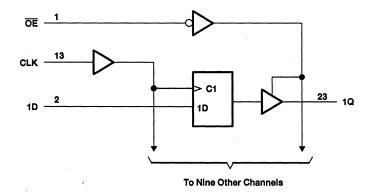


logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN74LVC821 10-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS304A - MARCH 1993 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, $I_{IK}(V_I < 0)$	– 50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB p	package 0.65 W
DW	package 1.7 W
PW	package 0.7 W
Storage temperature range, T _{stg}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vaa	Cumplicumiters	Operating	2	3.6	·V
VCC	Supply voltage	Data retention only	1.5		٧.
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V
۷ _I	Input voltage		0	5.5	٧
V-	Outrottualtage	High or low state	0	Vcc	V
VO	Output voltage	3 state	0	5.5	v
1	List level cubrut aument	V _{CC} = 2.7 V		-12	4
ЮН	High-level output current	V _{CC} = 3 V		-24	mA
1	V _{CC} = 2.7 \			12	4
lOL	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.



SN74LVC821 10-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS SCAS304A - MARCH 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} t	MIN TYP‡	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
V	lav. 10 mA	2.7 V	2.2		v
VOH	I _{OH} = - 12 mA	3 V	2.4		V
	I _{OH} = -24 mA	3 V	2.2		
	I _{OL} = 100 μA	MIN to,MAX		0.2	
VOL	I _{OL} = 12 mA	2.7 V		0.4	V
	I _{OL} = 24 mA	3 V		0.55	
11	V _I = 5.5 V or GND	3.6 V		±5	μА
loz	V _O = 5.5 V or GND	3.6 V		±10	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		10	μА
ΔlCC	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μА
Ci	V _I = V _{CC} or GND	3.3 V			pF
Co	V _O = V _{CC} or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

9-BIT BUS-INTERFACE FLIP-FL WITH 3-STATE OUTPUTS

 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	DB, DW, OR PW PACKAGE (TOP VIEW)
 Typical V_{OLP} (Output Ground Bounce) 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	OE (1 24 V _{CC}
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	2D 03 22 0 2Q 3D 04 21 0 3Q
 Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17 	4D 0 5 20 0 4Q 5D 0 6 19 0 5Q
 Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline 	6D [] 7 18] 6Q 7D] 8 17] 7Q
(DB), and Thin Shrink Small-Outline (PW) Packages	8D 9 16 8Q 9D 10 15 9Q
lescription	CLR 11 14 CLKEN GND 12 13 CLK

This 9-bit bus-interface flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC823 is designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

With the clock-enable (CLKEN) input low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking CLKEN high disables the clock buffer, latching the outputs. The SN74LVC823 has noninverting data (D) inputs. Taking the clear (CLR) input low causes the nine Q outputs to go low independently of the clock.

A buffered output-enable (\overline{OE}) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or a high-impedance state. The output-enable (OE) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\sf OE}$ should be tied to ${\sf V}_{\sf CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

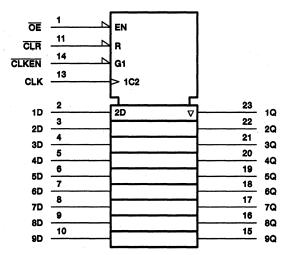
The SN74LVC823 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each flip-flop)

		INPUTS			OUTPUT
ŌĒ	CLR	CLKEN	CLK	D	Q
L	L	Х	Х	Х	L
L	Н	L	1	Н	н
L	Н	L	1	L	L
L	Н	н	X	Χ	Q_0
н	Х	X	Χ	Χ	Z

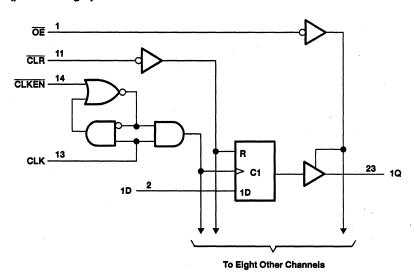
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



9-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS305A - MARCH 1993 - REVISED AUGUST 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, V _O (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	
Continuous output current, I _O (V _O = 0 to V _{CC})	
Continuous current through V _{CC} or GND	
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): DB package	
DW package	1.7 W
PW package	0.7 W
Storage temperature range, T _{stg}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
۷Į	Input voltage		0	5.5	V
٧o	Output voltage		0	VCC	٧
lau	High-level output current $ \frac{V_{CC} = 2.7 \text{ V}}{V_{CC} = 3 \text{ V}} $	V _{CC} = 2.7 V		-12	mA
ЮН		V _{CC} = 3 V		-24	IIIA
lai	Low lovel output ourront	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current VCC = 3 V			24	IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

SCAS305A - MARCH 1993 - REVISED AUGUST 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} †	MIN TYP‡	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Vali	V 10 10	2.7 V	2.2		v
Voн	I _{OH} = – 12 mA	3 V	2.4		V
	I _{OH} = -24 mA	3 V	2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
V _{OL}	I _{OL} = 12 mA	2.7 V		0.4	V
•	I _{OL} = 24 mA	3 V		0.55	
l ₁	V _I = 5.5 V or GND	3.6 V		±5	μА
loz	$V_O = V_{CC}$ or GND	3.6 V		±10	μА
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА
ΔlCC	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V		500	μА
Ci	V _I = V _{CC} or GND	3.3 V	9		pF
Co	V _O = V _{CC} or GND	3.3 V	. 10		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				V _{CC} = 3.3 V ± 0.3 V V _C		V _{CC} = 2.7 V	
			MIN			MAX	
fclock	Clock frequency		0	100	. 0	80	MHz
	Pulse duration	CLR low	5		5		
tw		CLK high or low	4		4		ns
	Setup time, data before CLK↑	CLR inactive	1		1		
^t su		Data	2		3		ns
		CLKEN low	3.5		4.5		
.	Hald the and the COLUM	Data	2		2		
^t h	Hold time, data after CLKT CLKEN low		0.5		0.5		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)				3.3 V 3 V	V _{CC} =	2.7 V	UNIT
		(001701)	MIN	MAX	MIN	MAX	ı	
fmax			100		80		MHz	
	CLK	Q	2	8	2	9		
^t pd -	CLR	Q	1.5	8	1.5	9	ns	
t _{en}	ŌĒ	. Q	1.5	8.5	1.5	9.5	ns	
^t dis	ŌĒ	Q	1.5	8	1.5	9	ns	

 $[\]ddagger$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SCAS305A - MARCH 1993 - REVISED AUGUST 1995

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT	
C .	Power dissinction conscitance per flip flep	Outputs enabled	C _I = 50 pF,	f = 10 MHz	22	nE
C _{pd}	Power dissipation capacitance per flip-flop	Outputs disabled	C[= 50 pr,	I = 10 MI12	12	pF

PARAMETER MEASUREMENT INFORMATION **TEST** S1 O Open **500** Ω From Output Open tpd **Under Test** 6 V O GND tpLZ/tpZL tPHZ/tPZH GND $C_L = 50 pF$ 500 Ω (see Note A) 2.7 V LOAD CIRCUIT FOR OUTPUTS 1.5 V **Timing Input** tsu 2.7 V 2.7 V 1.5 V Input 1.5 V 1.5 V Data Input 0 V 0 V **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS PULSE DURATION** SETUP AND HOLD TIMES 2.7 V 2.7 V Output 1.5 V 1.5 V 1.5 V 1.5 V Input Control 0 V 0 V **tPZL** ^tPHL Output VOH Waveform 1 Output S1 at 6 V VOL (see Note B) ^tPHZ **t**PLH tPHL -^tPZH Output VOH V_{OH} - 0.3 V Waveform 2 Output S1 at GND (see Note B) **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS** PROPAGATION DELAY TIMES **ENABLE AND DISABLE TIMES INVERTING AND NONINVERTING OUTPUTS** LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLz and tpHz are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SN74LVC827 10-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS306B - MARCH 1993 - REVISED JULY 1995

 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	DB, DW, OR PW PACKAGE (TOP VIEW)
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	OE1 1 24 V _{CC}
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	A2 3 22 Y2 A3 4 21 Y3
 Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17 	A4
 Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline 	A6 [] 7 18 [] Y6 A7 [] 8 17 [] Y7
(DB), and Thin Shrink Small-Outline (PW) Packages	A8 [] 9 16 [] Y8 A9 [] 10 15 [] Y9
description	A10 11 14 Y10 GND 12 13 OE2

This 10-bit buffer/bus driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC827 provides a high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable (OE1) or OE2) input is high, all ten outputs are in the high-impedance state. The SN74LVC827 provides true data at its outputs.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC827 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

	INPUTS		OUTPUT
OE1	OE2	Α	Y
L	L	L	٦
L	L	Н	н
Н	X	Х	z
х	н	X	z

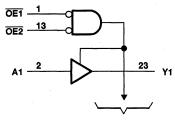
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SCAS306B - MARCH 1993 - REVISED JULY 1995

logic symbol[†]

OE1 13 EN OE2 23 ⊽ 3 22 Y2 A2 21 A3 **Y3** 20 A4 6 19 A5 **Y5** 18 A6 Y6 17 8 **Y7** Α7 16 **Y8 A8** 10 15 A9 11 14 A10

logic diagram (positive logic)



To Nine Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} –0.5 \	/ to 4.6 V
Input voltage range, V _I (see Note 1)	/ to 6.5 V
Output voltage range, VO (see Notes 1 and 2)	C + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	-50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, IO (VO = 0 to VCC)	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): DB package	0.65 W
DW package	. 1.7 W
PW package	. 0.7 W
Storage temperature range, T _{stq}	to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SCAS306B - MARCH 1993 - REVISED JULY 1995

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
VI	Input voltage		0	5.5	٧
Vo	Output voltage		0	Vcc	٧
1	High-level output current	V _{CC} = 2.7 V		-12	^
ЮН		V _{CC} = 3 V		-24	mA
1	Law law law a summer	V _{CC} = 2.7 V		12	
IOL	Low-level output current VCC = 3 V			24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CO	NDITIONS	v _{cc} †	MIN T	YP‡ MAX	UNIT
	I _{OH} = -100 μA		MIN to MAX	V _{CC} -0.2		
Vali	la 10 mA		2.7 V	2.2		v
Voн	IOH = - 12 IIIA	IOH = - 12 mA		2.4		٧
	IOH = -24 mA		3 V	2		
	I _{OL} = 100 μA		MIN to MAX		0.2	
V _{OL}	I _{OL} = 12 mA		2.7 V		0.4	٧
	I _{OL} = 24 mA		3 V		0.55	
lı	V _I = 5.5 V or GND		3.6 V		±5	μА
loz	V _O = V _{CC} or GND		3.6 V		±10	μА
lcc	$V_{I} = V_{CC}$ or GND,	I _O = 0	3.6 V		20	μА
ΔlCC	One input at V _{CC} - 0.6 V,	Other inputs at VCC or GND	3 V to 3.6 V		500	μА
Ci	VI = VCC or GND		3.3 V		9	pF
Co	VO = VCC or GND		3.3 V		10	pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, CL = 50 pF (unless otherwise noted) (see Figure 1)

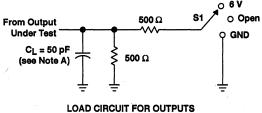
PARAMETER	FROM	FROM TO (INPUT)		3.3 V 3 V	V _{CC} =	2.7 V	UNIT
	(INFOT)	(001701)	MIN	MAX	MIN	MAX	
^t pd	A	Y	1.5	7		8	ns
^t en	ŌE .	Υ	1.5	9		11	ns
^t dis	ŌE	, Y	1.5	8		9	ns

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

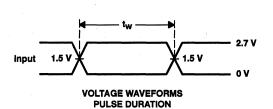
operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

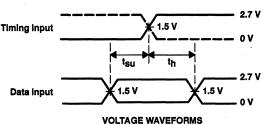
PARAMETER		TEST CONDITIONS	TYP	UNIT	
C _{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	C _I = 50 pF, f = 10 MHz	25	nE
		Outputs disabled	C _L = 50 pF, f = 10 MHz	2.5	p⊢

PARAMETER MEASUREMENT INFORMATION O 6 V TEST

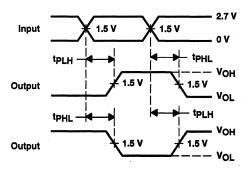


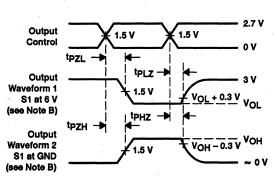






SETUP AND HOLD TIMES





VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_f ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms



SN74LVC828 10-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS347A - MARCH 1994 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

<u>OE1</u> [1	U ₂₄ j _{VCC}
A1 🛮 2	23 🛮 Y1
A2 🛛 3	22 🛭 Y2
A3 🛛 4	21 🛭 Y3
A4 🛮 5	20 🛭 Y4
A5 🛛 6	19 🛮 Y5
A6 🛛 7	18]] Y6
A7 🚺 8	17 🛭 Y7
A8 []9	16 🛭 Y8
A9 🛛 10	15 🛮 Y9
A10 🛮 11	14 🛭 Y10
GND [] 12	13 OE2

DB, DW, OR PW PACKAGE

(TOP VIEW)

description

This 10-bit buffer/bus driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC828 provides a high-performance bus interface for wide datapaths or buses carrying parity.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable (OE1) input is high, all ten outputs are in the high-impedance state. The SN74LVC828 provides inverting data at its outputs.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC828 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

	INPUTS	OUTPUT	
OE1	OE2	Α	Y
L	L	L	Н
L	L	Н	L
н	Х	Χ	z
х	н	Х	z

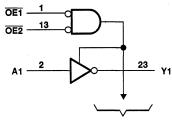
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SCAS347A - MARCH 1994 - REVISED JULY 1995

logic symbol[†]

ΕN 13 OF2 23 V **Y1** 3 22 **Y2** A2 4 21 **Y3** АЗ 5 20 Α4 **Y4** 6 19 Α5 **Y5** 7 18 **Y6** A6 8 17 **Y7** Α7 9 16 **Y8 A8** 10 15 **Y9** A9 11 14 Y10 A10

logic diagram (positive logic)



To Nine Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} 0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)
Output voltage range, V _O (see Notes 1 and 2)
Input clamp current, I_{IK} ($V_I < 0$) — 50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)
Continuous output current, I _O (V _O = 0 to V _{CC}) ±50 mA
Continuous current through V _{CC} or GND
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB package
DW package 1.7 W
PW package 0.7 W
Storage temperature range, T _{stg}

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
٧ _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
VI	Input voltage		0	5.5	٧
VO	Output voltage		0	Vcc	٧
1	High-level output current $ \frac{V_{CC} = 2.7 \text{ V}}{V_{CC} = 3 \text{ V}} $		-12	mA	
ЮН		V _{CC} = 3 V		-24	'''\^
1	V _{CC} = 2.7 V	V _{CC} = 2.7 V		12	
loL	Low-level output current V _{CC} = 3 V			24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcct	MIN TYP‡	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
Vari	lau 12 mA	2.7 V	2.2		v
VOH	I _{OH} = - 12 mA	3 V	2.4)
	I _{OH} = -24 mA	3 V	2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
v_{OL}	I _{OL} = 12 mA	2.7 V		0.4	V
	I _{OL} = 24 mA	3 V		0.55	
11	V _I = 5.5 V or GND	3.6 V		±5	μА
loz	V _O = V _{CC} or GND	3.6 V		±10	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μΑ
ΔlCC	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V		500	μА
Ci	V _I = V _{CC} or GND	3.3 V	9		pF
Co	V _O = V _{CC} or GND	3.3 V	10		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	
	(114F01)		MIN	MAX	MIN	MAX	
^t pd	Α	Y	1.5	8		9	ns
^t en	ŌĒ	Y	1.5	9		10	ns
^t dis	ŌĒ	Υ	1.5	8		9	ns

 $[\]ddagger$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$

PARAMETER		TEST CO	TYP	UNIT		
O Boundies alies and the standard and the standard and		Outputs enabled *	Cı = 50 pF. f = 10 MHz		27	
Cpd	Power dissipation capacitance per buffer/driver	Outputs disabled	$C_L = 50 pF$,	I = IU MITZ	2.4	pF

PARAMETER MEASUREMENT INFORMATION TEST S1 O Open **500** Ω From Output Open ^tpd **Under Test** o GND tpLZ/tpZL 6 V **GND** tPHZ/tPZH CL = 50 pF 500 Ω (see Note A) 2.7 V LOAD CIRCUIT FOR OUTPUTS 1.5 V Timing input tsu 2.7 V 2.7 V 1.5 V Input 1.5 V 1.5 V 1.5 V **Data Input** 0 V 0 V **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS PULSE DURATION** SETUP AND HOLD TIMES 2.7 V 2.7 V Output 1.5 V 1.5 V 1.5 V Input Control 0 V 0 V **tPZL** ^tPHL **tPLH tPLZ** Output VOH Waveform 1 1.5 V 1.5 V Output S1 at 6 V VOL (see Note B) ^tPHZ **t**PLH **tPHL** ^tPZH Output Vон V_{OH} - 0.3 V Waveform 2 1.5 V 1.5 V Output S1 at GND - Vol (see Note B) **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS** PROPAGATION DELAY TIMES **ENABLE AND DISABLE TIMES INVERTING AND NONINVERTING OUTPUTS** LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tPLH and tPHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SN74LVC841 10-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS307A - MARCH 1993 - REVISED JULY 1995

 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	DB, DW, OR PW PACKAGE (TOP VIEW)
 Typical V_{OLP} (Output Ground Bounce) 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	OE (1 24) V _{CC}
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	2D [] 3 22 [] 2Q 3D [] 4 21 [] 3Q
 Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC}) 	4D
Package Options include Plastic Small-Outline (DW), Shrink Small-Outline	7D 8 17 7Q 8D 9 16 8Q
(DB), and Thin Shrink Small-Outline (PW) Packages	9D [10 15] 9Q 10D [11 14] 10Q GND [12 13] LE

description

This 10-bit bus-interface D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation; it can interface to a 5-V system environment.

The SN74LVC841 is designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The ten latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

A buffered output-enable (\overline{OE}) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC841 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUT		
ŌĒ	LE	D	Q		
L	Н	Н	Н		
L	н	L	L		
L	L	Χ	Q ₀		
Н	Х	Х	Z		

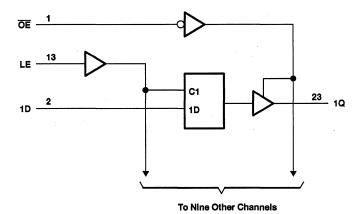
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ŌĒ LE	13	EN C1				
1D 2D 3D 4D 5D 6D	2 3 4 5 6 7	1D	D	▼-	23 22 21 20 19 18	1Q 2Q 3Q 4Q 5Q 6Q
7D 8D 9D 10D	9 10 11				17 16 15 14	7Q 8Q 9Q 10Q

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN74LVC841 10-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS307A - MARCH 1993 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)	0.5 V to 6.5 V
Voltage range applied to any output in the high impedance state	*
or power off state, V _O (see Note 1)	0.5 V to 6.5 V
Voltage range applied to any output in the high	
or low state, V _O (see Notes 1 and 2)	V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	– 50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): DB package	0.65 W
DW package	1.7 W
PW package	0.7 W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
	Supply voltage	Operating	2	3.6	V
VCC	Supply voltage	Data retention only			
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
VĮ	Input voltage		0	5.5	٧
۷o	Output voltage	High or low state	0	VCC	v
		3 state	0	5.5	
lau	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН	High-level output current	V _{CC} = 3 V		-24	IIIA
la.	Low-level output current	V _{CC} = 2.7 V		12	mA
IOL	Low-level output current	V _{CC} = 3 V		24	mA
∆t/∆v	Input transition rise or fall rate		0	10	ns/V
T _A Operating free-air temperature		-40	85	°C	

NOTE 4: Unused inputs must be held high or low to prevent them from floating.



SN74LVC841 10-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS SCAS307A - MARCH 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcct	MIN TYP#	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
V	Jan. 10 mA	2.7 V	2.2		v
VOH	I _{OH} = - 12 mA	3 V	2.4		\ \
	I _{OH} = -24 mA	3 V	2.2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
VOL	I _{OL} = 12 mA	2.7 V		0.4	V
	I _{OL} = 24 mA	3 V		0.55	
l _l	V _I = 5.5 V or GND	3.6 V		±5	μА
loz	V _O = 5.5 V or GND	3.6 V		±10	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		10	μА
Δlcc	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μА
Ci	V _I = V _{CC} or GND	3.3 V	17		рF
Co	V _O = V _{CC} or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

9-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS308A - MARCH 1993 - REVISED JULY 1995

 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	DB, DW, OR PW PACKAGE (TOP VIEW)
 Typical V_{OLP} (Output Ground Bounce) 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	OE 1 24 V _{CC}
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1D 2
 Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC}) 	4D 0 5 20 4Q 5D 0 6 19 0 5Q
 Package Options include Plastic Small-Outline (DW), Shrink Small-Outline 	7D
(DB), and Thin Shrink Small-Outline (PW) Packages	9D 10 15 9Q CLR 11 14 PRE GND 12 13 LE

description

This 9-bit bus-interface D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation; it can interface to a 5-V system environment.

The SN74LVC843 is designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The nine latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

A buffered output-enable (OE) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC843 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

<u> </u>		INPUTS			OUTPUT
PRE	CLR	OE	LE	D	Q
L	Х	L	Х	Х	Н
Н	L	L	Χ	Χ	L
н	Н	L	Н	L	L
н	н	L	Н	Н	н
н	Н	L	L	Χ	Q ₀
Х	Х	Н	Х	Х	Z

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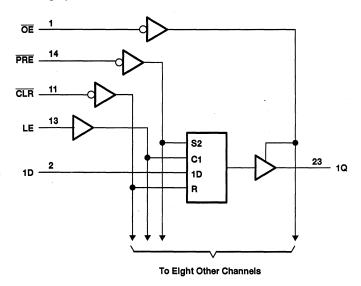


logic symbolt

OE PRE CLR LE	1 14 11 13	EN \$2 R C1		
1D	3	1D 2 ▽	23	1Q
2D 3D	4		21	2Q 3Q
4D			20	4Q
5D	6		19	5Q
6D	7		18	6Q
7D			17	7Q
8D	9		16	8Q
9D	10		15	9Q

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN74LVC843 9-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS308A - MARCH 1993 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)	
Voltage range applied to any output in the high impedance state	
or power off state, V _O (see Note 1)	-0.5 V to 6.5 V
Voltage range applied to any output in the high	
or low state, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, $I_{IK}(V_I < 0)$	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	
Continuous output current, I _O (V _O = 0 to V _{CC})	
Continuous current through V _{CC} or GND	
5 5 5	
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): DB	package 0.65 W
DW	package 1.7 W
PW	package 0.7 W
Storage temperature range, Teta	, -

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

,			MIN	MAX	UNIT	
V	Cumply yellone	Operating	2	3.6	V	
VCC	Supply voltage	Data retention only	1.5		v	
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧	
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		8.0	٧	
۷ _I	Input voltage		0	5.5	٧	
V-	Output voltage	High or low state	0	Vcc	- v 1	
VO		3 state	0	5.5		
lavi	Link lavel autout aument	V _{CC} = 2.7 V	T	-12		
ЮН	High-level output current	V _{CC} = 3 V	T	-24	mA	
lou	Low level and a death and a second	V _{CC} = 2.7 V		12	A	
IOL	Low-level output current VCC = 3 V			24	mA	
Δt/Δν	Input transition rise or fall rate		0	10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: Unused inputs must be held high or low to prevent them from floating.



SN74LVC843 9-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS SCAS308A - MARCH 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcct	MIN TYP#	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
W	10 40 4	2.7 V	2.2		v
VOH	I _{OH} = - 12 mA	3 V	2.4		٧
	I _{OH} = -24 mA	3 V	2.2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
VOL	I _{OL} = 12 mA	2.7 V		0.4	V
	IOL = 24 mA	3 V		0.55	
l _l	V _I = 5.5 V or GND	3.6 V		±5	μА
loz	V _O ≈ 5.5 V or GND	3.6 V		±10	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА
ΔICC	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μА
Ci	V _I = V _{CC} or GND	3.3 V			рF
Co	V _O = V _{CC} or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SN74LVC861 10-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS309A - MARCH 1993 - REVISED JULY 1995

 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	DB, DW, OR PW PACKAGE (TOP VIEW)
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	OEBA 1 24 V _{CC}
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	A2 [3 22] B2 A3 [4 21] B3
 Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17 	A4 [5 20] B4 A5 [6 19] B5
 Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline 	A6 [7 18] B6 A7 [8 17] B7
(DB), and Thin Shrink Small-Outline (PW) Packages	A8 [] 9 16 [] B8 A9 [] 10 15 [] B9
description	A10 11 14 B10 GND 12 13 OEAB

This 10-bit bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC861 is designed for asynchronous communication between data buses. The control-function implementation allows for maximum flexibility in timing.

This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the output-enable (OEAB and OEBA) inputs.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC861 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

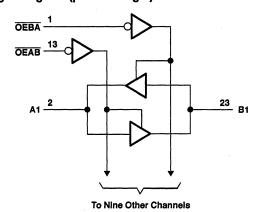
INP	UTS	ODEDATION
OEAB	OEBA	OPERATION
L	Н	A data to B bus
Н	L	B data to A bus
H	Н	Isolation
L	L	Latch A and B (A = B)

EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†

OEBA EN2 OEAB 2∇ B2 A2 21 АЗ 20 **B4** 19 **A5 B5** 18 **B6** A6 17 **B7** Δ7 16 **B8 8**A 15 **B9** A9 11 **B10**

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, $I_{ K }(V_1 < 0)$	
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): D	B package 0.65 W
D	W package 1.7 W
	W package 0.7 W
Storage temperature range, T _{stg}	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
V _{I.}	Input voltage	Control inputs	0	5.5	V
		Data inputs	0	Vcc	l v
Vo	Output voltage		0	Vcc	٧
1	High-level output current	V _{CC} = 2.7 V		-12	
ЮН		V _{CC} = 3 V		-24	mA
1	Law law law law law law law law law law l	V _{CC} = 2.7 V		12	4
IOL	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMET	R	TEST CONDITIONS	v _{cc} †	MIN	TYP‡	MAX	UNIT
		l _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			
V		la 10 mA	2.7 V	2.2			v
Vон		IOH = - 12 mA	3 V	2.4			V
		I _{OH} = -24 mA	3 V	2			
		l _{OL} = 100 μA	MIN to MAX			0.2	
VOL		I _{OL} = 12 mA	2.7 V			0.4	V
		I _{OL} = 24 mA	3 V			0.55	
lį		V _I = V _{CC} or GND	3.6 V			±5	μА
loz§		V _O = V _{CC} or GND	3.6 V			±10	μА
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			20	μА
ΔICC		One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V			500	μА
C _i Control	inputs	V _I = V _{CC} or GND	3.3 V		9		рF
Cio A or B p	orts	V _O = V _{CC} or GND	3.3 V		10		рF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	
	(1147-01)	(001701)	MIN	MAX	MIN	MAX	
^t pd	A or B	B or A	1.5	7		8	ns
t _{en}	OEAB or OEBA	A or B	1.5	9		10	ns
^t dis	OEAB or OEBA	A or B	1.5	8		9	ns

 $^{^{\}ddagger}$ All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

[§] For I/O ports, the parameter IOZ includes the input leakage current.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CO	TYP	UNIT	
C _{pd} Power dissipation capacitance per transceiver	Outputs enabled	C: 50 pE	f = 10 MHz	28	pF
	Outputs disabled	C _L = 50 pF,		2	pΓ

PARAMETER MEASUREMENT INFORMATION 6 V TEST S1 500 Ω O Open Open ^tpd From Output 6 V tpLZ/tpZL GND **Under Test** GND tPHZ/tPZH CL = 50 pF **500** Ω (see Note A) 2.7 V LOAD CIRCUIT FOR OUTPUTS **Timing Input** 1.5 V tsu 2.7 V 2.7 V 1.5 V Input Data Input 1.5 V 1.5 V 0 V o v **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS PULSE DURATION** SETUP AND HOLD TIMES 2.7 V 2.7 V Output 1.5 V 1.5 V Input 1.5 V 1.5 V Control n v ^tPZL **tPLH** t_{PHL} tPLZ . Output VOH Waveform 1 1.5 V .5 V Output 1.5 V VOL + 0.3 V S1 at 6 V VOL VOL (see Note B) tpHZ → **tPLH** tPHL -^tPZH Output ۷он Waveform 2 V_{OH} - 0.3 **Output** S1 at GND VOL (see Note B) **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS** PROPAGATION DELAY TIMES **ENABLE AND DISABLE TIMES** INVERTING AND NONINVERTING OUTPUTS LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms



SCAS310A - MARCH 1993 - REVISED JULY 1995

 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	DB, DW, OR PW PACKAGE (TOP VIEW)
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	OEBA1 1 24 V _{CC}
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	A2 3 22 B2 A3 4 21 B3
 Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17 	A4] 5 20] B4 A5 [] 6 19] B5
 Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline 	A6[]7 18]] B6 A7[]8 17]] B7
(DB), and Thin Shrink Small-Outline (PW) Packages	A8
description	OEBA2 11 14 OEAB2 GND 12 13 OEAB1

This 9-bit bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC863 is designed for asynchronous communication between data buses. The control-function implementation allows for maximum flexibility in timing.

This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the output-enable (OEAB and OEBA) inputs.

The outputs are in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC863 is characterized for operation from -40°C to 85°C.

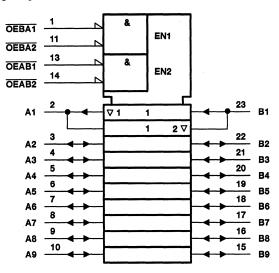
FUNCTION TABLE

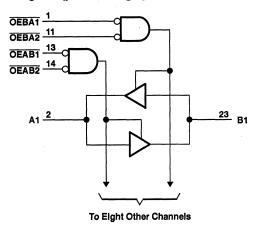
	INPUTS									
	INP	OPERATION								
OEAB1	OEAB2	OEBA1	OEBA2	OPERATION						
L	L	L	L	Latch A and B						
L	L	Н	Х	A to B						
L	L	Х	Н	A 10 B						
Н	Х	L	L	B to A						
X	Н	L:	L	D IO A						
Н	Х	Н	Х							
Н	Х	Х	н	laalatian						
×	Н	Х	н	Isolation						
х	Н	Н	X							

EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} 0.5 V to 4.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)
I/O ports (see Notes 1 and 2)
Output voltage range, V _O (see Notes 1 and 2)
Input clamp current, I _{IK} (V _I < 0)
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)
Continuous output current, I _O (V _O = 0 to V _{CC})
Continuous current through V _{CC} or GND
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB package
DW package 1.7 W
PW package 0.7 W
Storage temperature range, T _{stg} –65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
VI	Input voltage	Control inputs	0	5.5	V
		Data inputs	0	VCC	L v
Vo	Output voltage		0	Vcc	٧
1	High-level output current	V _{CC} = 2.7 V		-12	A
IOH		V _{CC} = 3 V		-24	mA
1	Laveland autorit aurorit	V _{CC} = 2.7 V		12	mA
IOL	Low-level output current	V _{CC} = 3 V		24	IIIA
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	vcct	MIN TYP‡ MAX	UNIT
		l _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2	
\ _V		I _{OH} = – 12 mA	2.7 V	2.2	V
VOH		IOH = - 12 IIIA	3 V	2.4	v
		I _{OH} = -24 mA	3 V	2	
		l _{OL} = 100 μA	MIN to MAX	0.2	!
VOL		I _{OL} = 12 mA	2.7 V	0.4	V
		I _{OL} = 24 mA	3 V		;
IJ		V _I = 5.5 V or GND	3.6 V	±ŧ	μА
IOZ§		V _O = V _{CC} or GND	3.6 V	±10) μΑ
ICC		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	20) μΑ
Δlcc		One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V	500) μΑ
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V	9	pF.
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V	10	pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	
	(147-01)	(001901)	MIN	MAX	MIN	MAX	1
t _{pd}	A or B	B or A	1.5	7		8	ns
t _{en}	OEAB or OEBA	A or B	1.5	9		10	ns
^t dis	OEAB or OEBA	A or B	1.5	8		9	ns

 $^{^{\}ddagger}$ All typical values are V_{CC} = 3.3 V, T_A = 25°C.

[§] For I/O ports, the parameter IOZ includes the input leakage current.

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per transceiver	Outputs enabled	O. 50 = 5 40 MH=	27	ρF
	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	2	pr

PARAMETER MEASUREMENT INFORMATION 6 V **TEST S1** 500 Ω O Open Open tpd From Output 6 V tPLZ/tPZL **Under Test** GND GND tPHZ/tPZH CL = 50 pF **500** Ω (see Note A) 2.7 V LOAD CIRCUIT FOR OUTPUTS 1.5 V **Timing Input** tsu 2.7 V Input 1.5 V 1.5 Data Input 1.5 V 1.5 V 0 V **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS** PULSE DURATION SETUP AND HOLD TIMES 2.7 V Output Input 1.5 V 1.5 V 1.5 V Control 0 V **tPZL** ^tPLH ^tPHL tpLZ -Output VOH 3 V Waveform 1 Output 1.5 V VOL + 0.3 V S1 at 6 V VOL (see Note B) **tPHZ tPLH** tPHL tpzH -Output Vон Waveform 2 VOH - 0.3 V 1.5 V Output S1 at GND VOL (see Note B) **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS** PROPAGATION DELAY TIMES **ENABLE AND DISABLE TIMES** INVERTING AND NONINVERTING OUTPUTS LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_f ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- tpLZ and tpHZ are the same as tdis-
- tpzL and tpzH are the same as ten.
- tPLH and tPHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms



PRODUCT PREVIEW

SN74LVC2952 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS311A - JANUARY 1993 - REVISED JULY 1995

 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	DB, DW, OR PW PACKAGE (TOP VIEW)
 Typical V_{OLP} (Output Ground Bounce) 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	B8 1 24 V _{CC} B7 1 2 23 A8
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	B6 0 3 22 0 A7 B5 0 4 21 0 A6
 Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC}) 	B4
 Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) 	B1 8 17 A2 OEAB 9 16 A1 CLKAB 10 15 OEBA
Packages	CLKENAB [] 11 14 [] CLKBA GND [] 12 13 [] CLKENBA

description

This octal bus transceiver and register is designed for 2.7-V to 3.6-V V_{CC} operation; it can interface to a 5-V system environment.

The SN74LVC2952 consists of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable (CLKENBA) input is low. Taking the output-enable (OEAB or OEBA) input low accesses the data on either port.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC2952 is characterized for operation from -40°C to 85°C.

FUNCTION TABLET

	INPUTS					
CLKENAB	CLKAB	OEAB	Α	В		
Н	Х	L	Х	B ₀ ‡		
Χ .	H or L	L	Х	В ₀ ‡ В ₀ ‡		
L	1	L	L	L		
L	1	L	Н	н		
X	X	Н	Х	z		

[†] A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENBA, CLKBA, and OEBA.

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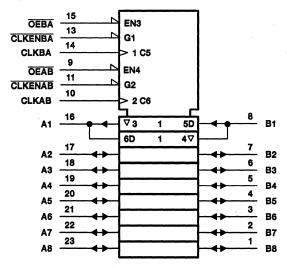


[‡]Level of B before the indicated steady-state input conditions were established

SN74LVC2952 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

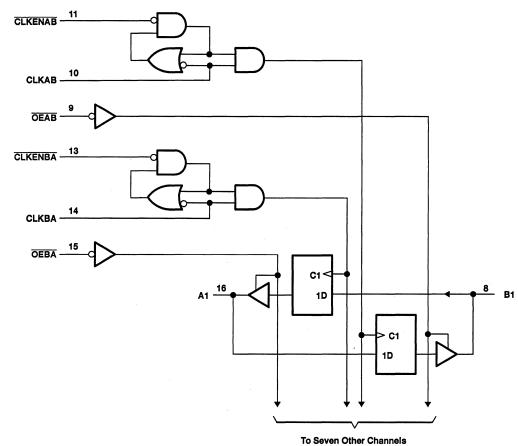
SCAS311A - JANUARY 1993 - REVISED JULY 1995

logic symbolt



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)	0.5 V to 6.5 V
Voltage range applied to any output in the high impedance state	
or power off state, VO (see Note 1)	0.5 V to 6.5 V
Voltage range applied to any output in the high	
or low state, V _O (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Note 1)	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	
Continuous output current, IO (VO = 0 to VCC)	
Continuous current through V _{CC} or GND	
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3):	
	DW package 1.7 W
	PW package 0.7 W
Storage temperature range, T _{sto}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
	Cumplusaltage	Operating	2	3.6	V
VCC	Supply voltage	Data retention only	1.5		٧.
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
۷ _{JL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
۷j	Input voltage		0	5.5	٧
V-	Output voltage	High or low state	0	Vcc	٧
V _O Output voltage	3 state	0	5.5	V	
1	Link level enteret enteret	V _{CC} = 2.7 V		-12	4
IOH	High-level output current	V _{CC} = 3 V		-24	mA
la.	Low-level output current	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

SN74LVC2952 **OCTAL BUS TRANSCEIVER AND REGISTER** WITH 3-STATE OUTPUTS SCAS311A - JANUARY 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P/	ARAMETER	TEST CONDITIONS	vcct	MIN TYP‡	MAX	UNIT
VOH		$I_{OH} = -100 \mu\text{A}$	MIN to MAX	V _{CC} -0.2		
		10 10	2.7 V	2.2		v
		IOH = - 12 mA	3 V	2.4		V
		I _{OH} = -24 mA	3 V	2.2		
		I _{OL} = 100 μA	MIN to MAX		0.2	
VOL		I _{OL} = 12 mA	2.7 V		0.4	٧
		I _{OL} = 24 mA	3 V		0.55	
l _l		V _I = 5.5 V or GND	3.6 V		±5	μА
loz§		V _O = 5.5 V or GND	3.6 V		±10	μΑ
lcc		V _I = V _{CC} or GND, I _O = 0	3.6 V		20	μА
Δlcc		One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V		500	μÁ
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V			pF
Cio	A or B ports	V _O = V _{CC} or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C. § For I/O ports, the parameter I_{OZ} includes the input leakage current.

General Information	1
ALB Widebus™	2
ALVC Widebus™	3
LVT Octals	4
LVTZ Octals: Power Up and 3 State	5
LVT Widebus™	6
LVT JTAG/IEEE 1149.1	7
LVC MSI and Octals	8
LVC Widebus™	9
LV MSI and Octals	10
GTL Transceivers and Backplane Drivers	11
Application Reports	12
Characteristics Information	13
Mechanical Data	14

Contents

	•	Page
SN74LVC16240	16-Bit Buffer/Driver With 3-State Outputs	9-3
SN74LVC16241	16-Bit Buffer/Driver With 3-State Outputs	9-7
SN74LVC16244A	16-Bit Buffer/Driver With 3-State Outputs	9-11
SN74LVCH16244A	16-Bit Buffer/Driver With 3-State Outputs	9-17
SN74LVC162244	16-Bit Buffer/Driver With 3-State Outputs	9-23
SN74LVC16245A	16-Bit Bus Transceiver With 3-State Outputs	9-29
SN74LVCH16245A	16-Bit Bus Transceiver With 3-State Outputs	9-35
SN74LVCR162245	16-Bit Bus Transceiver With 3-State Outputs	9-41
SN74LVC16373	16-Bit Transparent D-Type Latch With 3-State Outputs	9-47
SN74LVC16374	16-Bit Edge-Triggered D-Type Flip-Flop With 3-State Outputs	9-53
SN74LVC16540	16-Bit Buffer/Driver With 3-State Outputs	9-59
SN74LVC16541	16-Bit Buffer/Driver With 3-State Outputs	9-63
SN74LVC16543	16-Bit Registered Transceiver With 3-State Outputs	9-67
SN74LVC16646	16-Bit Bus Transceiver and Register With 3-State Outputs	9-75
SN74LVC16652	16-Bit Bus Transceiver and Register With 3-State Outputs	9-83
SN74LVC16952	16-Bit Registered Transceiver With 3-State Outputs	9-93

SN74LVC16240 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS312A - NOVEMBER 1993 - REVISED JULY 1995

 Member of the Texas Instruments Widebus™ Family 		L PACKAGE VIEW)
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	1 <u>OE</u> [1	48 2OE
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1Y1	47 11A1 46 11A2 45 GND
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1Y3 5 1Y4 6	44 1 1A3 43 1 1A4
 Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown 	V _{CC} 7 2Y1 [8	42 V _{CC} 41 2A1
Resistors Supports Mixed-Mode Signal Operation on	2Y2 9 GND 1 0	C
All Ports (5-V Input/Output Voltage With 3.3-V V _{CC})	2Y3 11 2Y4 12	37 2 A4
 Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink 	3Y1 [13 3Y2 [14 GND [15	35 3A2
Small-Outline (DGG) Packages description	3Y3 [16 3Y4 [17	33 🛚 3A3
This 16-bit buffer/driver is designed for 2.7-V to	V _{CC} [18 4Y1 [19	
3.6-V V _{CC} operation; it can interface to a 5-V system environment.	4Y2 20 GND 21	29 🛚 4A2
The SN74LVC16240 is designed specifically to improve both the performance and density of	4Y3 [22 4Y4 [23	
3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.	4 0E [24	25 3 OE

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides inverting outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16240 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 4-bit buffer)

INP	JTS	OUTPUT
ŌĒ	Α	Y
L	Н	L
L	L	н
н	X	z

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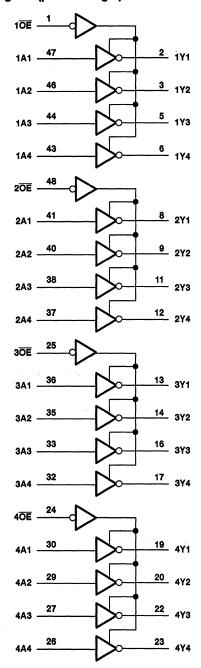


logic symbol†

	1 48 25 24	4 4 4	EN1 EN2 EN3 EN4			
_	47		ــــــــــــــــــــــــــــــــــــــ	1		2
1 · 2 ·	46		 		1 ▽	3
2 · 3 ·	44		ļ			5
4	43		 			6
1	41			1	2▽	8
1 · 2 ·	40				2 V	9
3	38					11
4 .	37		 			12
1	36		 	1	3∇	13
2 .	35			<u> </u>		14
3 .	33		ļ			16
4 .	32		ļ			17
1 .	30			1	4 ▽	19
2 .	29				7 V	20
3 .	27		 			22
, .	26		 -			23

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



DL package 1.2 W

Storage temperature range, T_{stg} –65°C to 150°C

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
1/	Complexed	Operating	2	3.6	· V	
VCC	Supply voltage	Data retention only	1.5		٠ ٧	
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧	
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧	
۷Į	Input voltage		0	VCC	٧	
٧o	Output voltage		0	5.5	٧	
lavi	Link lavel autaut aumont	V _{CC} = 2.7 V		-12	A	
ЮН	High-level output current	V _{CC} = 3 V		-24	24 mA	
lo	Low-level output current	V _{CC} = 2.7 V		12	A	
IOL	Low-level output current	V _{CC} = 3 V		24	mA	
Δt/Δν	Input transition rise or fall rate		0	10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	vcct	MIN TYP‡	MAX	UNIT	
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			
		104	2.7 V	2.2		.,	
VOH		I _{OH} = -12 mA	3 V	2.4	-	V	
		I _{OH} = -24 mA	3 V	2.2			
		I _{OL} = 100 μA	MIN to MAX		0.2		
VOL		I _{OL} = 12 mA	2.7 V		0.4	v	
		I _{OL} = 24 mA	3 V		0.55		
l _l		V _I = 5.5 V or GND	3.6 V		±5	μА	
	Data insuta	V _I = 0.8 V	0.1/	75			
l(hold)	Data inputs	V _I = 2 V	3 V	-75		μА	
loz		V _O = 5.5 V or GND	3.6 V		±10	μА	
Icc		V _I = V _{CC} or GND, I _O = 0	3.6 V		40	μА	
ΔICC		One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or G	ND 2.7 V to 3.6 V		500	μА	
Ci		V _I = V _{CC} or GND	3.3 V			pF	
Co		V _O = V _{CC} or GND	3.3 V			pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

 $[\]ddagger$ All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

SN74LVC16241 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS348A - MARCH 1994 - REVISED JULY 1995

Member of the Texas Instruments Widebus™ Family	DGG OR DL PACKAGE (TOP VIEW)
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	10E 1 48 20E
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1Y1
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1Y3 5 44 1A3 1Y4 6 43 1A4
 Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown 	V _{CC}
Resistors Supports Mixed-Mode Signal Operation on	2Y2 9 40 2A2 GND 10 39 GND
All Ports (5-V Input/Output Voltage With 3.3-V V _{CC})	2Y3
 Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages 	3Y2 14 35 3A2 GND 15 34 GND
description	3Y3
This 16-bit buffer/driver is designed for 2.7-V to 3.6-V V _{CC} operation; it can interface to a 5-V	V _{CC}
system environment. The SN74LVC16241 is designed specifically to	GND 21 28 GND 4Y3 22 27 4A3
improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.	4Y4 23 26 4A4 4OE 24 25 3OE

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and complementary output-enable (\overline{OE}) inputs.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16241 is characterized for operation from -40°C to 85°C.

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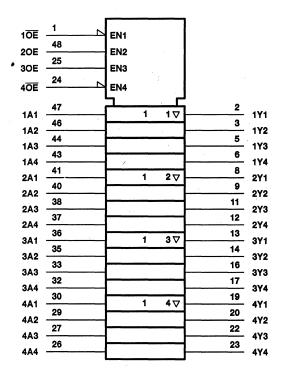
FUNCTION TABLES

INPUTS 10E, 40E 1A, 4A		OUTPUTS
		1Y, 4Y
L	Н	Н
L'	L	L
н .	X	z

INPL	OUTPUTS	
20E, 30E	2OE, 3OE 2A, 3A	
Н	Н	Н
н	L	L
L	X	z

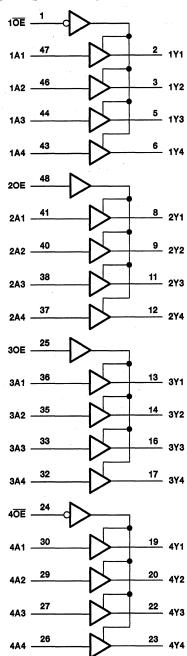
logic symbol†

PRODUCT PREVIEW



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 6.5 V
Input voltage range, V ₁	
Voltage range applied to any output in the high-impedance state	
or power-off state, VO (see Note 1)	0.5 V to 6.5 V
Voltage range applied to any output in the high	
or low state, V _O (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	
Continuous output current, I _O (V _O = 0 to V _{CC})	
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	
	1.2 W
Storage temperature range, T _{sto}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
	0	Operating	2	3.6	.,	
VCC	Supply voltage	Data retention only	1.5		٧	
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧	
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	V	
VI	Input voltage		0	5.5	٧	
Vo	Output voltage		0	VCC	٧	
la	I the bound of the common to t	V _{CC} = 2.7 V		-12	4	
ЮН	High-level output current	V _{CC} = 3 V		-24	mA	
1		V _{CC} = 2.7 V		12	A	
IOL	Low-level output current	V _{CC} = 3 V		24	mA	
Δt/Δν	Input transition rise or fall rate		0	10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	v _{cc} †	MIN TYP‡	MAX	UNIT
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
		10 = 4	2.7 V	2.2		v
VOH		IOH = -12 mA	3 V	2.4		v
		I _{OH} ≈ -24 mA	3 V	2.2		
		I _{OL} = 100 μA	MIN to MAX		0.2	
VOL		I _{OL} = 12 mA	2.7 V		0.4	V
		I _{OL} = 24 mA	3 V		0.55	
lj .		V _I = 5.5 V or GND	3.6 V		±5	μА
lea en	Data innuta	V _I = 0.8 V	0.1/	75		
l(hold)	Data inputs	V _I = 2 V	3 V	-75		μA
loz		V _O = 5.5 V or GND	3.6 V		±10	μА
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μА
ΔICC		One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μА
Ci		V _I = V _{CC} or GND	3.3 V			pF
Co		V _O = V _{CC} or GND	3.3 V			pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

 $[\]ddagger$ All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

SCESORIA - DECEMBER 1995 - REVISED JANIJARY 1996

 Member of the Texas Instruments Widebus™ Family 	DGG OR DL PACKAGE (TOP VIEW)	
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	23	48 2 0E 47 1A1
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1Y2 🛚 3	46 1A2 45 GND
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1Y3 ∐ 5	44 1 1A3 43 1 1A4
 Supports Mixed-Mode Signal Operation (5-V Input/Output Voltage With 3.3-V V_{CC}) 	2Y1 🛛 8	42 V _{CC} 41 2A1
 ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 	GND 🛚 10	40 2A2 39 GND
200 V Using Machine Model (C = 200 pF, R = 0)	2Y4 🛚 12	38 2A3 37 2A4 36 3A1
Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17	3Y2 🛚 14	35] 3A2 34] GND
 Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages 	3Y3 🛚 16	33] 3A3 32] 3A4
description	4Y1 🛛 19	31 V _{CC} 30 4A1
This 16-bit buffer/driver is designed for 2.7-V to 3.6-V V _{CC} operation.	GND 🛮 21	29 4A2 28 GND 27 4A3
The SN74LVC16244A is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers,	4Y4 🛚 23	26 4A4 25 3OE

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC16244A is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 4-bit buffer)

INPL	JTS	OUTPUT
ŌĒ	Α	Y
L	Н	Н
L.	L	L
Н	X	z

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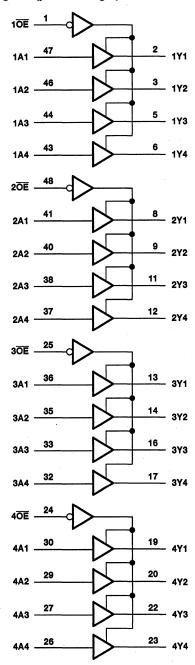
and bus-oriented receivers and transmitters.

logic symbol†

48	EN1		
	EN2	'	
25	EN3		
24	EN4		
47			2
46		1▽	3
44			5
43			6
41			8
40	1	2 ▽	9
38			11
37			12
36	1	3▽	13
35			14
33			16
32			17
30	1	4▽	19
29			20
27			22
26			23

[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SCESOSIA - DECEMBER 1005 - REVISED IANI IARY 1006

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		-0.5 V to 6.5 V
Input voltage range, V _I (see Note 1)		
Voltage range applied to any output in the high-impedance state		
or power-off state, V _O (see Note 1)		-0.5 V to 6.5 V
Voltage range applied to any output in the high		
or low state, VO (see Notes 1 and 2)		V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)		–50 mA
Output clamp current, IOK (VO < 0 or VO > VCC)		±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})		±50 mA
Continuous current through each V _{CC} or GND		
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3):	DGG package	0.85 W
	DL package	1.2 W
Operating free-air temperature range, T _A		
Storage temperature range, T _{sto}		-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
Vcc	Supply voltage	Operating	2	3.6	V	
Ç	Data Data	Data retention only	1.5		٧	
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧	
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		8.0	٧	
VI	Input voltage		0	5.5	٧	
V-	Output voltage	High or low state	0	Vcc	- V	
Vo		3 state	0	5.5		
lavi	High-level output current	V _{CC} = 2.7 V		-12	mA	
ЮН	High-lever output current	V _{CC} = 3 V		-24	mA	
io.		V _{CC} = 2.7 V		12	mA	
lOL	Low-level output current VCC = 3 V			24	IIIA	
Δt/Δν	Input transition rise or fall rate		0	10	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

SCES061A - DECEMBER 1995 - REVISED JANUARY 1996

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcct	MIN TYP‡	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		
V	I _{OH} = -12 mA	2.7 V	2		v
VOH	I _{OH} = -12 mA	3 V	2.2		,
	$I_{OH} = -24 \text{ mA}$	3 V	2		
	I _{OL} = 100 μA	MIN to MAX		0.2	
VOL	I _{OL} = 12 mA	2.7 V		0.4	٧
	I _{OL} = 24 mA	3 V		0.55	
i II	V _I = 5.5 V or GND	3.6 V		±5	μА
loff	V_I or $V_O = 5.5 V$	0		50	μА
loz	V _O = 0 to 5.5 V	3.6 V		±20	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА
Δlcc	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V	,	500	μА
Ci	V _I = V _{CC} or GND	3.3 V	4.7		pF
C _o	V _O = V _{CC} or GND	3.3 V	6.1		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	
			MIN	MAX	MIN	MAX	
^t pd	Α	Υ	1.5	5.2		5.8	ns
^t en	ŌĒ	Y	1.5	7.5		8.2	ns
^t dis	ŌĒ	Y	1.5	7		7.7	ns
t _{sk(o)} §				. 1			ns

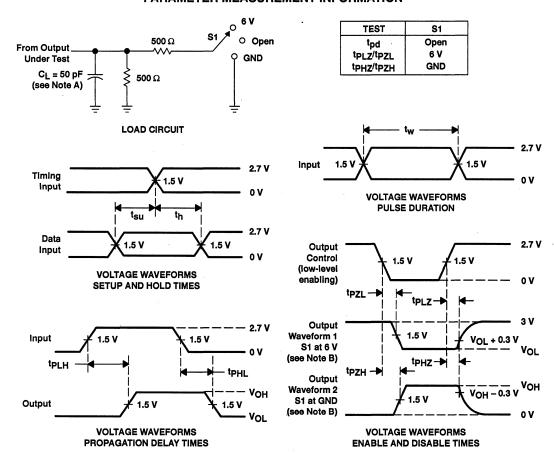
[§] Skew between any tow outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER			TEST CO	TYP	UNIT	
C _{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	C _L = 50 pF,	f = 10 MHz	20.2	pF
		Outputs disabled			3.6	

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms

SCAS313B - NOVEMBER 1993 - REVISED AUGUST 1995

 Member of the Texas Instruments Widebus™ Family 	DGG OR DL PACKAGE (TOP VIEW)			
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	10E 1 1Y1 2	48 2 0E		
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1Y2 3 GND 04	47 [] 1A1 46 [] 1A2 45 [] GND		
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1Y3 [5 1Y4 [6	44 1 1A3 43 1 1A4		
 Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 	V _{CC} [7 2Y1] 8	42 V _{CC} 41 2A1		
3.3-V V _{CC}) ■ ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds	2Y2 [] 9 GND [] 10 2Y3 [] 11	40		
200 V Using Machine Model (C = 200 pF, R = 0)	2Y4 🛘 12 3Y1 🗓 13	37 0 2A4 36 0 3A1		
 Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17 	3Y2 1 14 GND 1 15 3Y3 1 16	34 🏿 GND		
Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors	3Y4 [] 17 V _{CC} [] 18	32 [] 3A4		
Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink	4Y1 19 4Y2 20			
Small-Outline (DGG) Packages	GND [] 21 4Y3 [] 22 4Y4 [] 23			
description	4 0E 24	25 3 OE		

This 16-bit buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVCH16244A is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVCH16244A is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 4-bit buffer)

INPL	JTS	OUTPUT
ŌĒ A		Y
L	Н	Н
L	L	L
Н	Х	Z

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TEXAS INSTRUMENTS
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SN74LVCH16244A 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

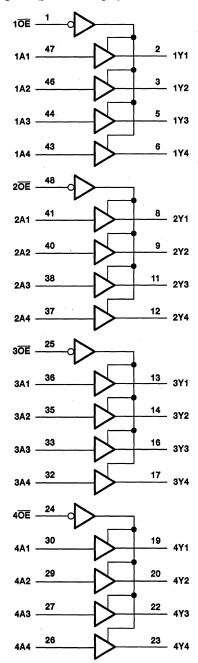
SCAS313B - NOVEMBER 1993 - REVISED AUGUST 1995

logic symbolt

10E 20E 30E 40E	1 48 25 24	EN1 EN2 EN3 EN4				
1A1	47		1	1▽	2	1Y1
1A2	46				3	1Y2
1A2	44	 			5	1Y3
1A4	43	 			6	1Y4
2A1	41	 	1	2∇	8	2Y1
2A2	40	 			9	2Y2
2A3	38	-			11	2Y3
2A4	37	 -			12	2Y4
3A1	36		1	3▽	13	3Y1
3A2	35	-			14	3Y2
3A3	33	\vdash			16	3Y3
3A4	32	 			17	3Y4
4A1	30	 	1	4▽	19	4Y1
4A2	29	 		<u> </u>	20	4Y2
4A3	27	 			22	4Y3
4A4	26	 			23	4Y4

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SCAS313B - NOVEMBER 1993 - REVISED AUGUST 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Voltage range applied to any output in the high-impedance state	0.5 v to 0.5 v
or power-off state, V _O (see Note 1)	0.5 V to 6.5 V
Voltage range applied to any output in the high	
or low state, V _O (see Note 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$)	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	
Continuous current through each V _{CC} or GND	
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 3): DGG package .	
	1.2 W
Storage temperature range, T _{stg}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
V	Cumplicialities	Operating	2	3.6	v	
VCC	Supply voltage	Data retention only	1.5		٧	
ViH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧	
VIL	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	٧	
۷į	Input voltage		0	5.5	٧	
Va	Output voltage	High or low state	. 0	VCC	V	
V _O	Output voltage	3 state	0	5.5	v	
lau	High lovel cutout current	V _{CC} = 2.7 V		-12	A	
ЮН	High-level output current	V _{CC} = 3 V		-24	mA	
la.	Low-level output current	V _{CC} = 2.7 V		12	A	
lOL	Low-level output current	V _{CC} = 3 V		24	24 mA	
Δt/ΔV	Input transition rise or fall rate		0	10	ns/V	
TA	Operating free-air temperature	,	-40	85	°င	

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SCAS313B - NOVEMBER 1993 - REVISED AUGUST 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} t	MIN TYP#	MAX	UNIT	
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			
	10 mA	2.7	2.2		V	
VOH	I _{OH} = -12 mA	3	2.4		V	
	I _{OH} = -24 mA	3	2			
	I _{OL} = 100 μA	MIN to MAX		0.2		
V _{OL}	I _{OL} = 12 mA	2.7		0.4	V	
	I _{OL} ≈ 24 mA	3		0.55		
l _l	V _I = 5.5 V or GND	3.6		±5	μA	
	V _I = 0.8 V	3	75			
(l(hold)	V _I = 2 V		- 75		μА	
, i	V _I = 0 to 3.6 V	3.6		±500		
loff	$V_I \text{ or } V_O = 5.5 \text{ V}$	0		±50	μА	
loz	$V_0 = 0 \text{ to } 5.5 \text{ V}$	3.6		±20	μА	
loc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6		20	μΑ	
ΔlCC	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μΑ	
Ci	V _I = V _{CC} or GND	3.3	4.7		pF	
Co	$V_O = V_{CC}$ or GND	3.3	6.1		pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	V _{CC} = 3.3	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	
PANAMEIEN	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	UNIT
^t pd	A	Υ	1.5	5.2		5.8	ns
t _{en}	ŌĒ	Y	1.5	7.5		8.2	ns
^t dis	ŌĒ	Υ	1.5	7		7.7	ns
t _{sk(o)} §				1			ns

[§] Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

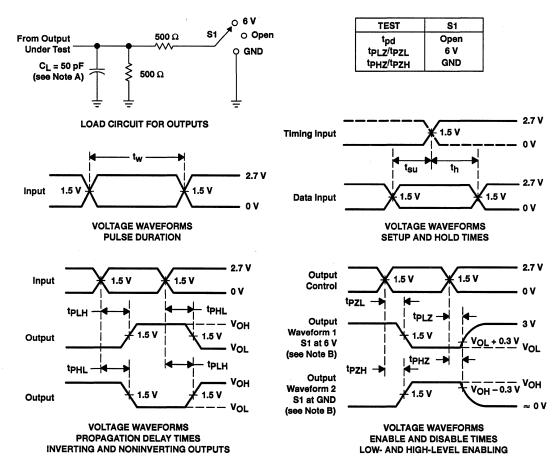
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT	
C .	Power dissipation capacitance per buffer/driver	Outputs enabled	C. 50 - F	f = 10 MHz	20.2	
C _{pd}	rower dissipation capacitance per buller/driver	Outputs disabled	C _L = 50 pF,	I = IU MINZ	3.6	pF



 $[\]ddagger$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_I includes probe and lig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms

SCAS545 - OCTOBER 1995

 Member of the Texas Instruments Widebus™ Family 	DGG OR DL PACKAGE (TOP VIEW)		
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	3	20E	
 Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required Typical V_{OLP} (Output Ground Bounce) 	1Y2 3 46 GND 4 45 1Y3 5 44] 1A1] 1A2] GND] 1A3] 1A4	
< 0.8 V at V _{CC} = 3.3 V, T _A = 25°C ■ Typical V _{OHV} (Output V _{OH} Undershoot) > 2 V at V _{CC} = 3.3 V, T _A = 25°C	V _{CC}	V _{CC} 2A1 2A2	
 ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0) 	2Y3 11 38 2Y4 12 37] GND] 2A3] 2A4] 3A1	
 Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17 	GND 🛚 15 34	3A2 GND	
 Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors 	3Y4 0 17 32 V _{CC} 0 18 31] 3A3] 3A4] V _{CC}	
 Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages 	4Y2 020 29 GND 21 28] 4A1] 4A2] GND] 4A3	
description	4Y4 🛮 23 26	4A4 3OE	
This is his bufferfeld to a declared for 0.7 V to		1	

This 16-bit buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC162244 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable (\overline{OE}) inputs. The outputs, which are designed to sink up to 12 mA, include 26- Ω resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC162244 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 4-bit buffer)

INPL	JTS	OUTPUT
OE	Α	Y
L	Н	Н
L	L	L
Н	Х	Z

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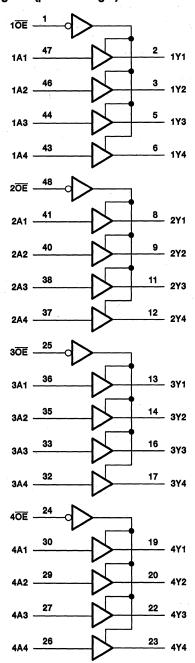
TEXAS INSTRUMENTS

SCAS545 - OCTOBER 1995 logic symbol†

10E 20E	1 48	EN1 EN2				
3OE	25	EN3				
4ŌĒ	24	EN4		لے		
1A1	47		1	1▽	2	1Y1
1A2	46				<u>3</u>	1Y2
1A3	43				6	1Y3
1A4	41				8	1Y4
2A1	40	<u> </u>	1	2▽	9	2Y1
2A2 2A3	38	 			11	2Y2 2Y3
2A4	37	 			12	213 2Y4
3A1	36		1	3 ▽	13	3Y1
3A2	35				14	3Y2
3A3	33				16	3Y3
3A4	32				17	3Y4
4A1	29		1	4∇	20	4Y1
4A2	27	<u> </u>			22	4Y2
4A3	26	<u> </u>			23	4Y3
4A4		L				4Y4

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SCAS545 - OCTOBER 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)		
Output voltage range, VO (see Notes 1 and 2)	0.5	V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)		
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)		±50 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$		±50 mA
Continuous current through V _{CC} or GND		
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3):		
	DL package	1.4 W
Storage temperature range, T _{stg}		-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
VI	Input voltage		0	VCC	٧
Vo	Output voltage	Output voltage		VCC	٧
lou	High-level output current	V _{CC} = 2.7 V		-8	mA
ЮН	High-level output current	V _{CC} = 3 V		-12	ША
la.	Low-level output current	V _{CC} = 2.7 V		8	m^
lor	V _{CC} = 3 V			12	mA
∆t/∆V	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN74LVC162244 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS545 - OCTOBER 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST C	ONDITIONS	vcct	MIN	TYP‡	MAX	UNIT
		I _{OH} = -100 μA		MIN to MAX	VCC-C).2		
		I _{OH} = -6 mA,	V _{IH} = 2 V	3	2.4			v
VOH		$I_{OH} = -8 \text{ mA},$	V _{IH} = 2 V	2.7	2			V
}		I _{OH} = ~12 mA,	V _{IH} = 2 V	3	2			
Voi		I _{OL} = 100 μA		MIN to MAX			0.2	
VOL		IOL = 6 mA,	V _{IL} = 0.8 V	3			0.55	v
		I _{OL} = 8 mA,	V _{IL} = 0.8 V	2.7			0.6	· •
		I _{OL} = 12 mA,	V _{IL} = 0.8 V	3			0.8	
l _l		V _I = V _{CC} or GND		3.6			±5	μА
		V _I = 0.8 V		3	75			
li(hold)		V _i = 2 V		3	-75			μА
		V _I = 0 to 3.6 V		3.6			± 500	
loz		VO = VCC or GND		3.6			±10	μА
ICC		V _I = V _{CC} or GND,	IO = 0	3.6			20	μА
Δlcc		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	μА
Ci	Control inputs	V _I = V _{CC} or GND		3.3		2.5		pF
C _o	A or B ports	V _O = V _{CC} or GND		3.3		3.5		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} =	UNIT	
PARAMETER	(INPUT)		MIN	MAX	MIN	MAX	ONIT
^t pd	Α.	Y	1.5	7	1.5	8	ns
^t en	ŌĒ	Y	1.5	9	1.5	10	ns
^t dis	ŌĒ	Y	1.5	7	1.5	8	ns

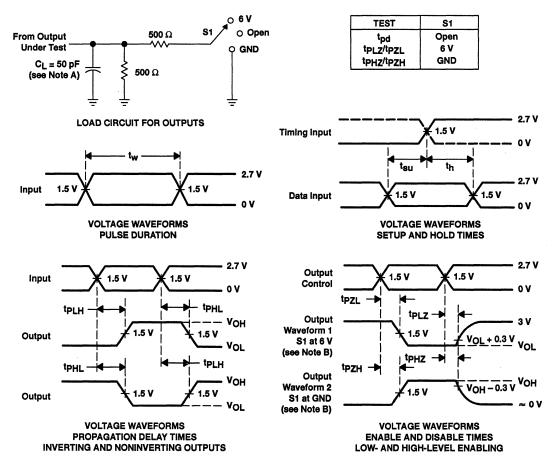
operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER			NDITIONS	TYP	UNIT
C .	Power dissipation capacitance per buffer/driver	Outputs enabled	C _I = 50 pF.	f = 10 MHz	20	
Opd	r ower dissipation capacitance per bullendriver	Outputs disabled	OL = 50 pr.,	I = IU WITZ	2	pF

 $[\]ddagger$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SCAS545 – OCTOBER 1995

PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_r \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms



48 10E

47 1 1A1

46 1 1A2

45 GND

44 🛮 1A3

43 🛮 1A4

42 V_{CC}

41 🛮 1A5

40 🛮 1A6

39 [] GND

38 1 1A7 37 1 1A8

36 D 2A1

35 2A2

34 D GND

33 D 2A3

32 D 2A4

31 V_{CC}

30 D 2A5

29 D 2A6

28 GND

27 D 2A7

26 2A8

25 20E

DGG OR DL PACKAGE

(TOP VIEW)

1DIR 1

1B1 2

1B2 []3

GND 4

1B3 🛮 5

1B4 🛮 6

V_{CC} []7

1B5 🛚 8

1B6 🛮 9

GND [] 10

1B7 🛮 11

1B8 | 12 2B1 | 13

2B2 [] 14

GND [] 15

2B3 🛮 16

2B4 [] 17

V_{CC} [] 18

2B5 🛮 19

2B6 []20

GND 21

2B7 122

2B8 [] 23

2DIR 1 24

SCES062 - DECEMBER 1995

Member of the Texas Instruments Widebus™ Family FPIC™ (Enhanced-Performance in the second sec

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V Vcc)
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit (dual-octal) noninverting bus transceiver is designed for 2.7-V to 3.6-V $V_{\rm CC}$ operation; it can interface to a 5-V system environment.

The SN74LVC16245A is designed for asynchronous communication between data buses. The control function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC16245A is characterized for operation from -40°C to 85°C.

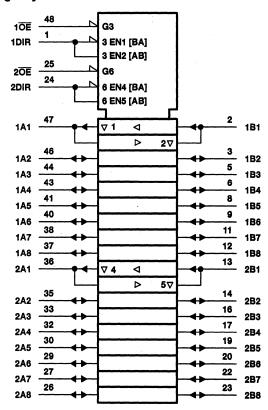
FUNCTION TABLE (each 8-bit section)

	(oddii o bit occitori)							
	INPUTS OE DIR		OPERATION					
			OPERATION					
	L	L	B data to A bus					
	L	Н	A data to B bus					
	Н	Х	Isolation					

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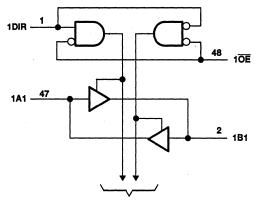
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALIAS, TEXAS 75265

logic symbol†

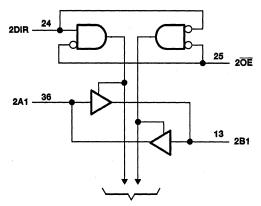


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels



To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}
or power-off state, V _O (see Note 1)
foltage applied to any output in the high or low state, V_O (see Notes 1 and 2)0.5 V to V_{CC} + 6.5 V
nput clamp current, I _{IK} (V _I < 0)
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC}) ±50 mA
Continuous output current, IO (VO = 0 to VCC) ±50 mA
Continuous current through each V _{CC} or GND
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package
DL package 1.2 W
Storage temperature range, T _{stg} 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V	Supply voltage	Operating	2	3.6	V
VCC		Data retention only	1.5		V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
۷ _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
٧ _I	Input voltage			5.5	٧
Vo.	Output voltage	High or low state	0	VCC	v
VO		3 state	0	5.5	l v
l	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН		V _{CC} = 3 V		-24	MA
la.	Low-level output current	V _{CC} = 2.7 V		12	mA
IOL	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate		0	5	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

SN74LVC16245A 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES062 - DECEMBER 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P/	ARAMETER	TEST CONDITIONS		vcct	MIN	TYP‡	MAX	UNIT
		I _{OH} = -100 μA		MIN to MAX	V _{CC} -0	.2		
V		I _{OH} = -12 mA		2.7 V	2			V
VOH		I _{OH} = -12 mA		3 V	2.2			V
		IOH = -24 mA		3 V	2			
		I _{OL} = 100 μA		MIN to MAX			0.2	
VOL		IOL = 12 mA		2.7 V			0.4	٧
		I _{OL} = 24 mA		3 V			0.55	
lγ		V _I = 5.5 V or GND		3.6 V			±5	μА
loff		V _I or V _O = 5.5 V		0			50	μА
I _{OZ} §		V _O = 0 to 5.5 V	,	3.6 V			±20	μА
Icc		VI = VCC or GND, IC) = 0	3.6 V			20	μА
Δlcc		One input at V _{CC} - 0.6 V, O	Other inputs at V _{CC} or GND	3 V to 3.6 V			500	μА
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V		5.4		pF
Cio	A or B ports	VO = VCC or GND		3.3 V		9		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	PARAMETER FROM TO (OUTPUT)	Vcc =	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		
		(001701)	MIN	MAX	MIN	MAX	İ
^t pd	. А	Y	1	5.2		5.8	ns
^t en	ŌĒ	Y	1.5	7.2		8	ns
t _{dis}	ŌĒ	Υ	1.5	7.2		8	ns
tsk(o)¶				1			ns

Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

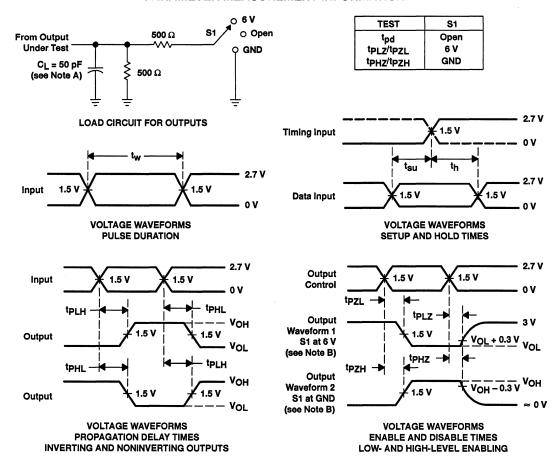
PARAMETER			TEST CO	NDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per transceiver	Outputs enabled Outputs disabled	C _L = 50 pF,	f = 10 MHz	24 3.7	pF

 $[\]ddagger$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[§] For I/O ports, the parameter IOZ includes the input leakage current.

SCES062 - DECEMBER 1995

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpzL and tpzH are the same as ten.
- F. tpLz and tpHz are the same as tdis.
- G. tplH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



SN74LVCH16245A **16-BIT BUS TRANSCEIVER** WITH 3-STATE OUTPUTS

SCES063 - DECEMBER 1995

 Member of the Texas Instruments Widebus™ Family 		OR DL PA	ACKAGE (W)
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	1DIR 0		48 10E 47 1A1
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1B2	з .	46 1 1A2 45 1 GND
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1B3 [1B4 [5	44 1 1A3 43 1A4
Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.2 V V -)	V _{CC} 1 1B5	8	42 V _{CC} 41 1 1A5
3.3-V V _{CC}) ■ ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds	1B6 GND 1B7	10 11	40 0 1A6 39 0 GND 38 0 1A7
200 V Using Machine Model (C = 200 pF, R = 0)	2B1 [13	37 1 1A8 36 2A1
 Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17 	2B2 GND	15	35 2A2 34 GND 33 2A3
 Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown 	2B3 L 2B4 L V _{CC}	17	32 2 2A3 32 2A4 31 2V _{CC}
Resistors Package Options Include Plastic 300-mil	2B5 [2B6 [19	30 2A5 29 2A6
Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages	GND [2B7 [21	28 GND 27 2A7
description	2B8 [2DIR [23	26 2A8 25 2 0E
This 16 hit (dust eats) manipulation has			

This 16-bit (dual-octal) noninverting bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVCH16245 is designed for asynchronous communication between data buses. The control function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVCH16245 is characterized for operation from -40°C to 85°C.

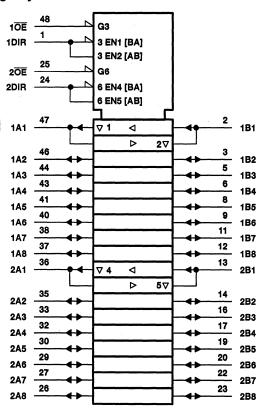


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FUNCTION TABLE (each 8-bit section)

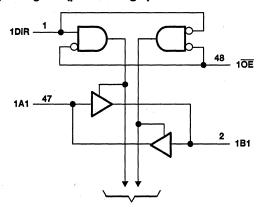
INP	UTS	OPERATION
ŌĒ	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	Χ	Isolation

logic symbol†

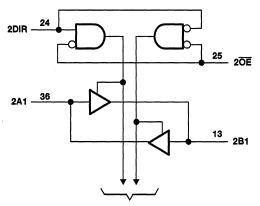


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels



To Seven Other Channels

SCES063 - DECEMBER 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} 0.5 V to 6.5 V Input voltage range, V _I : Except I/O ports (see Note 1)0.5 V to 6.5 V
I/O ports (see Notes 1 and 2)0.5 V to V _{CC} + 0.5 V
Voltage applied to any output in the high-impedance state
or power-off state, V _O (see Note 1)
Voltage applied to any output in the high or low state, V _O (see Notes 1 and 2) −0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) —50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})
Continuous output current, I _O (V _O = 0 to V _{CC})
Continuous current through each V _{CC} or GND
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package
DL package 1.2 W
Storage temperature range, T _{stg} –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V	0 1 1	Operating	2	3.6	٧
vcc	Supply voltage	Data retention only	1.5		V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	٧
۷ _I	Input voltage		0	5.5	٧
	Output voltage	High or low state	0	VCC	V
VO		3-state	0	5.5	V
1	Liliah Jawa andan dan mana	V _{CC} = 2.7 V		-12	4
ЮН	High-level output current	V _{CC} = 3 V		-24	mA
1	Laurianal autorit aurmant	V _{CC} = 2.7 V		12	4
lOL	Low-level output current	V _{CC} = 3 V		24	mA
Δt/ΔV	Input transition rise or fall rate		0	5	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



SN74LVCH16245A 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES063 - DECEMBER 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		vcct	MIN	TYP‡	MAX	UNIT
		I _{OH} = -100 μA		MIN to MAX	VCC-0	.2		
		l 40 mA		2.7 V	2			v
VOH		I _{OH} = -12 mA	,	3 V	2.2			v
l		I _{OH} = -24 mA		3 V	2			
		I _{OL} = 100 μA		MIN to MAX			0.2	
VOL		I _{OL} = 12 mA		2.7 V			0.4	V
		IOL = 24 mA		3 V			0.55	
11	Control inputs	V _I = 5.5 V or GND		3.6 V			±5	μА
		V ₁ = 0.8 V		0.1/	75			
I(hold)		V _I = 2 V		3 V	-75			μА
` .		V _I = 0 to 3.6 V		3.6 V			±500	
loff		V _I or V _O = 5.5 V		0			50	μА
I _{OZ} §		V _O = 0 to 5.5 V	* . `	3.6 V			±20	μА
Icc		V _I = V _{CC} or GND,	l _O = 0	3.6 V			20	μА
ΔICC		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	μА
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V		5.4		pF
Cio	A or B ports	VO = VCC or GND		3.3 V		9		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM TO (INPUT)		V _{CC} =	3.3 V 3 V	V _{CC} =	2.7 V	UNIT
	(INFOT)	(001701)	MIN	MAX	MIN	MAX	
^t pd	A or B	B or A	1	5.2		5.8	ns
ten t	ŌĒ	A or B	1.5	7.2		8	ns
* ^t dis	ŌĒ	A or B	1.5	7.2		8	ns
^t sk(o) [¶]				1			ns

Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER			TEST CO	TYP	UNIT	
C _{pd}	Power dissipation capacitance per transceiver	Outputs enabled Outputs disabled	C _L = 50 pF,	f = 10 MHz	24 3.7	pF

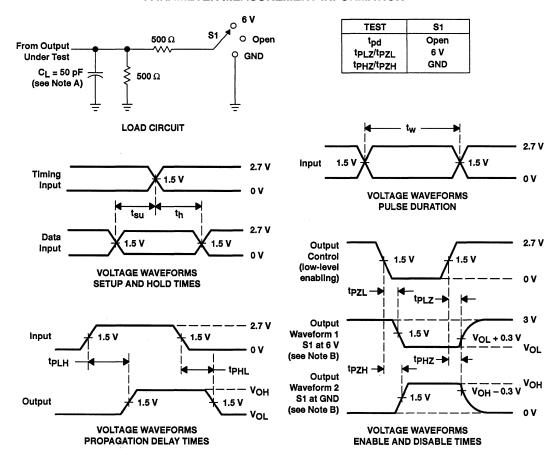


 $[\]ddagger$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

[§] For I/O ports, the parameter IOZ includes the input leakage current.

SCES063 - DECEMBER 1995

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzi and tpzH are the same as ten.
- G. tpl H and tpHI are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES047 - AUGUST 1995

 Member of the Texas Instruments Widebus™ Family 	DGG OR DL PACKAGE (TOP VIEW)		
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	1DIR 1 1B1 2	48 10E 47 1A1	
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1B2 [3 GND [4	46 🛭 1A2	
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1B3 5 1B4 6	44 🛭 1A3	
 ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 	V _{CC} [7 1B5 [8	41 🛭 1A5	
200 V Using Machine Model (C = 200 pF, R = 0)	1B6 9 GND 10	39 GND	
 Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17 	1B7 11 1B8 12	2 37 🛭 1A8	
 Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors 	2B1 [] 13 2B2 [] 14 GND [] 15	4 35 2A2	
 All Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors Are 	2B3 [16 2B4 [17	7 32 🕽 2A4	
Required Package Options Include Plastic Shrink	V _{CC} 18 2B5 19	9 30 2 2A5	
Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages	2B6 [] 20 GND [] 21 2B7 [] 22	1 28 GND	
description	2B8 [] 23 2DIR [] 24	3 26 2A8	

This 16-bit (dual-octal) noninverting bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVCR162245 is designed for asynchronous communication between data buses. The control function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

All outputs, which are designed to sink up to 12 mA, include $26-\Omega$ resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVCR162245 is characterized for operation from -40°C to 85°C.

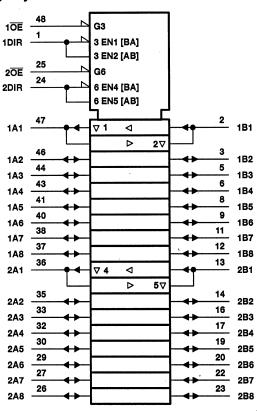


EPIC and Widebus are a trademarks of Texas Instruments Incorporated.

FUNCTION TABLE (each 8-bit section)

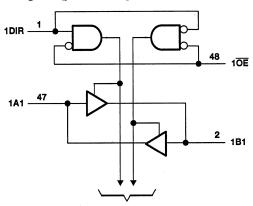
INP	UTS	OPERATION				
ŌĒ	DIR	OPERATION				
L	L	B data to A bus				
L	Н	A data to B bus				
Н	х	Isolation				

logic symbol†

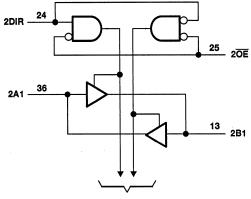


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels



To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	O mal coella ma mana M	051/4-401/
$\label{eq:localization} I/O \ ports \ (see \ Notes 1 \ and 2) \\ Output \ voltage \ range, \ V_O \ (see \ Notes 1 \ and 2) \\ Input \ clamp \ current, \ I_{ K } \ (V_ < 0) \\ Output \ clamp \ current, \ I_{OK} \ (V_O < 0 \ or \ V_O > V_{CC}) \\ Continuous \ output \ current, \ I_O \ (V_O = 0 \ to \ V_{CC}) \\ Continuous \ current \ through \ V_{CC} \ or \ GND \\ Maximum \ power \ dissipation \ at \ T_A = 55°C \ (in \ still \ air) \ (see \ Note 3): \ DGG \ package \\ DL \ package \\ DL \ package \\ 1.2 \ W$	Supply voltage range, v _{CC}	–0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) -0.5 V to $V_{CC} + 0.5 \text{ V}$ Input clamp current, I_{IK} ($V_I < 0$) -50 mA Output clamp current, I_{OK} ($V_O < 0 \text{ or } V_O > V_{CC}$) $\pm 50 \text{ mA}$ Continuous output current, I_O ($V_O = 0 \text{ to } V_{CC}$) $\pm 50 \text{ mA}$ Continuous current through V_{CC} or GND $\pm 100 \text{ mA}$ Maximum power dissipation at $T_A = 55^{\circ}\text{C}$ (in still air) (see Note 3): DGG package 0.85 W DL package 1.2 W	Input voltage range, VI: Except I/O ports (see Note 1)	0.5 V to V _{CC} + 4.6 V
Output voltage range, V_O (see Notes 1 and 2) -0.5 V to $V_{CC} + 0.5 \text{ V}$ Input clamp current, I_{IK} ($V_I < 0$) -50 mA Output clamp current, I_{OK} ($V_O < 0 \text{ or } V_O > V_{CC}$) $\pm 50 \text{ mA}$ Continuous output current, I_O ($V_O = 0 \text{ to } V_{CC}$) $\pm 50 \text{ mA}$ Continuous current through V_{CC} or GND $\pm 100 \text{ mA}$ Maximum power dissipation at $T_A = 55^{\circ}\text{C}$ (in still air) (see Note 3): DGG package 0.85 W DL package 1.2 W	I/O ports (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ± 50 mA Continuous output current, I_O (V_O = 0 to V_{CC}) ± 50 mA Continuous current through V_{CC} or GND ± 100 mA Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package 0.85 W DL package 1.2 W		
Continuous output current, I_O (V_O = 0 to V_{CC}) ± 50 mA Continuous current through V_{CC} or GND ± 100 mA Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package 0.85 W DL package 1.2 W	Input clamp current, $I_{ K }(V_1 < 0)$	
Continuous current through V_{CC} or GND		
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	Continuous output current, IO (VO = 0 to VCC)	±50 mA
DL package 1.2 W	Continuous current through V _{CC} or GND	±100 mA
	Maximum power dissipation at T _A = 55°C (in still air) (see Note 3	3): DGG package 0.85 W
Storage temperature range, T _{stg} 65°C to 150°C		DL package 1.2 W
	Storage temperature range, T _{stg}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
VĮ	Input voltage		0	VCC	٧
Vo	Output voltage		0	νcc	>
lou	High-level output current $ \frac{V_{CC} = 2.7 \text{ V}}{V_{CC} = 3 \text{ V}} $	V _{CC} = 2.7 V		-8	mA
ЮН		V _{CC} = 3 V		-12	
loi	Low-level output current	V _{CC} = 2.7 V		8	mA
lor	V _{CC} = 3 V			12	
Δt/ΔV	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	ပ္

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN74LVCR162245 **16-BIT BUS TRANSCEIVER** WITH 3-STATE OUTPUTS

SCES047 - AUGUST 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER	TEST C	ONDITIONS	v _{cc} t	MIN	TYP‡	MAX	UNIT
		I _{OH} = -100 μA		MIN to MAX	VCC-C	.2		
		I _{OH} = -4 mA,	V _{IH} = 2 V	2.7 V	2.2			
VOH		I _{OH} = -8 mA,	V _{IH} = 2 V	2.7 V	2			٧
		I _{OH} = -6 mA,	V _{IH} = 2 V	3 V	2.4			
		IOH = -12 mA,	V _{IH} = 2 V	3 V	2			
		IOH = -100 μA		MIN to MAX			0.2	
		I _{OH} = -4 mA,	V _{IL} = 0.8 V	2.7 V			0.4	
VOL		I _{OH} = -8 mA,	V _{IL} = 0.8 V	2.7 V			0.6	٧
		I _{OH} = -6 mA,	V _{IL} = 0.8 V	3 V			0.55	
		I _{OH} = -12 mA,	V _{IL} = 0.8 V	3 V			0.8	
lj		V _I = V _{CC} or GND		3.6 V			±5	μА
		V _I = 0.8 V		3 V	75			^
I(hold)		V _I = 2 V		7 3*	-75			μА
		V _I = 0 to 3.6 V		3.6 V			±500	μА
I _{OZ} §		VO = VCC or GND		3.6 V			±10	μА
Icc		V _I = V _{CC} or GND,	IO = 0	3.6 V			20	μА
Δlcc		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	μА
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V		2.5		pF
Cio	A or B ports	VO = VCC or GND		3.3 V		3.5		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

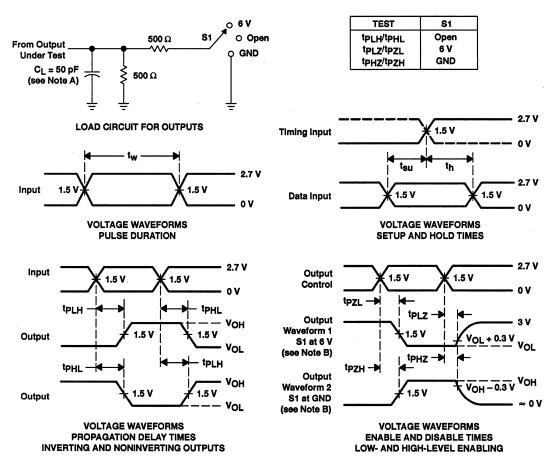
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	V _{CC} = 3.3 V ± 0.3 V	V _{CC} =	2.7 V	UNIT
	(HAPOT)	(001701)	MIN	MAX	MIN	MAX	
^t pd	A or B	B or A	1.5	7.5	1.5	8.5	ns
t _{en} .	ŌĒ	A or B	1.5	9	1.5	10	ns
^t dis	ŌĒ	A or B	1.5	7.5	1.5	8.5	ns

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT	
C _{pd} Power dissipation capacitance per trans	Power dissipation canaditance per transceiver	Outputs enabled	C: 50 pE 4 10 MHz	20	
		Outputs enabled	$C_L = 50 pF, f = 10 MHz$	2	pF

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. § For I/O ports, the parameter I_{OZ} includes the input leakage current.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as tden.
- G. tpHL and tpLH are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms



a-46

SN74LVC16373 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS315B - NOVEMBER 1993 - REVISED JULY 1995

•	
 Member of the Texas Instruments Widebus™ Family 	DGG OR DL PACKAGE (TOP VIEW)
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 	1 <u>OE</u> 1 48 1LE 1Q1 2 47 1D1
 Typical V_{OLP} (Output Ground Bounce) 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1Q2 3 46 1D2 GND 4 45 GND
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1Q3 [5 44] 1D3 1Q4 [6 43] 1D4
 Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17 	V _{CC} [7 42] V _{CC} 1Q5 [8 41] 1D5
Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown	1Q6 9 40 1D6 GND 10 39 GND
Resistors Package Options Include Plastic 300-mil Shalak Small Quality (DL) and Tala Shalak	1Q7
Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages	2Q2 1 14 35 2D2 GND 15 34 GND
description	2Q3 [16 33] 2D3 2Q4 [17 32] 2D4
This 16-bit transparent D-type latch is designed for 2.7-V to 3.6-V V _{CC} operation.	V _{CC} 18 31 V _{CC} 2Q5 19 30 2D5
The SN74LVC16373 is particularly suitable for implementing buffer registers, I/O ports,	2Q6
bidirectional bus drivers, and working registers. It can be used as two 8-bit latches or one 16-bit	2Q7 [22 27] 2D7 2Q8 [23 26] 2D8
latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels	2 0E [24 25] 2LE

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16373 is characterized for operation from -40°C to 85°C.

TEXAS INSTRUMENTS

set up at the D inputs.

FUNCTION TABLE (each 8-bit section)

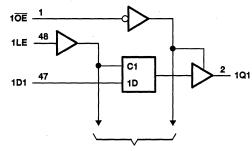
	INPUTS	OUTPUT	
ŌĒ	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Χ	Q ₀
Н	X	Χ	Z

logic symbol†

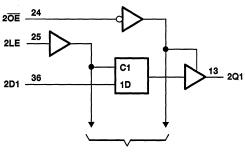
10E 1EN 48 1LE СЗ 24 2OE 2EN 25 2LE C4 47 2 3D 1Q1 1D1 1 ▽ 46 3 1D2 1Q2 5 44 1D3 1Q3 43 6 1D4 1Q4 41 8 1D5 1Q5 40 9 1D6 1Q6 38 11 1D7 **1Q7** 37 12 1D8 1Q8 36 13 2D1 4D 2 ▽ 2Q1 35 14 2D2 2Q2 33 16 2D3 2Q3 17 32 2D4 2Q4 30 19 2D5 2Q5 29 20 2D6 2Q6 27 22 2D7 2Q7 26 23 2D8 2Q8

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels



To Seven Other Channels

SN74LVC16373 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V ₁ (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3	
	DL package 1.2 W
Storage temperature range, Teta	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	٧
VI	Input voltage		0	VCC	٧
VO	Output voltage		0	VCC	٧
lou	High-level output current $ \frac{V_{CC} = 2.7 \text{ V}}{V_{CC} = 3 \text{ V}} $		-12	mA	
ЮН		V _{CC} = 3 V		-24	ША
lo	Low-level output current	V _{CC} = 2.7 V		12	mA
lor	V _{CC} = 3 V			24	IIIA
Δt/ΔV	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN74LVC16373 16-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS315B - NOVEMBER 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	vcct	MIN TYP	MAX	UNIT	
,		I _{OH} = ~100 μA	MIN to MAX	V _{CC} -0.2			
		I _{OH} = -12 mA	2.7	2.2		v	
VOH		IOH = - 12 MA	3	2.4		V	
Ì		I _{OH} = -24 mA	3	2			
		I _{OL} = 100 μA	MIN to MAX		0.2		
VOL		I _{OL} = 12 mA	2.7		0.4	.4 V	
		I _{OL} = 24 mA	3		0.55		
lį		V _I = V _{CC} or GND	3.6		±5	μА	
	Data issues	V _I = 0.8 V		3	75		4
I (hold)	Data inputs	$V_{\parallel} = 2 V$	7 °	- 75		μА	
loz		V _O = V _{CC} or GND	3.6		±10	μА	
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6		40	μА	
ΔICC		One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V		500	μА	
Ci		V _I = V _{CC} or GND	3.3	3.5		рF	
Co		V _O = V _{CC} or GND	3.3	7		pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
	· ·	MIN	MAX	MIN	MAX	
t _W	Pulse duration, LE high	4		4		ns
t _{su}	Setup time, data before LE↓	2		2		ns
th	Hold time, data after LE↓	2		2		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
	(INFOT)		MIN	MAX	MIN	MAX	
1	D	- Q	1.5	7		8	ns
^t pd	LE		2	8		9	
t _{en}	ŌĒ	Q	1.5	8		9	ns
^t dis	ŌĒ	Q	1.5	7		8	ns

operating characteristics, $T_{\Delta} = 25^{\circ}C$

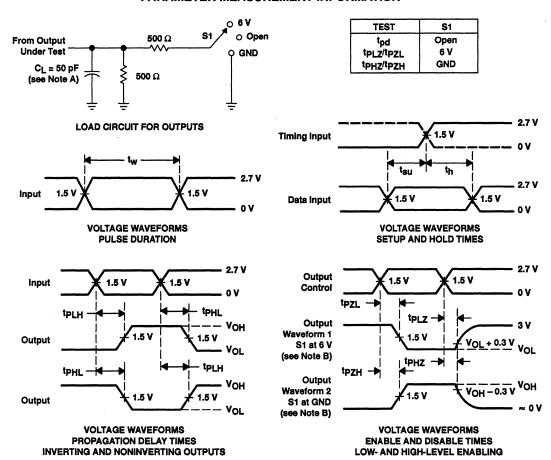
PARAMETER		TEST CON	NDITIONS	TYP	UNIT	
C	Power dissipation capacitance per latch	Outputs enabled	C:	6 10 MU=	20	pF
C _{pd} Power dissipation capaci	- Ower dissipation capacitance per laten	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	4	рг	



[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SCAS315B - NOVEMBER 1993 - REVISED JULY 1995

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \Omega$, $t_{r} \leq$ 2.5 ns, $t_{t} \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten-
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SN74LVC16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS316B - NOVEMBER 1993 - REVISED JULY 1995

 Member of the Texas Instruments Widebus™ Family 	DGG OR DL PACK (TOP VIEW)	
 EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process 		1 1 CLK
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1Q2 🛚 3 46	1D2 GND
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1Q3 🛮 5 44	1D3 1D4
 Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17 	1Q5 []8 41	V _{CC} 1D5
Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Positors	GND 10 39	1D6 GND 1D7
Resistors Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink	1Q8	1D8 2D1
Small-Outline (DGG) Packages	GND [] 15 34	2D2 GND
description		2D3 2D4
This 16-bit edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.	V _{CC}	V _{CC} 2D5
The SN74LVC16374 is particularly suitable for implementing buffer registers, I/O ports,	GND 21 28	2D6 GND
bidirectional bus drivers, and working registers. It can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock	2Q8 [] 23 26	2D7 2D8 2CLK
(CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.		F

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16374 is characterized for operation from -40°C to 85°C.

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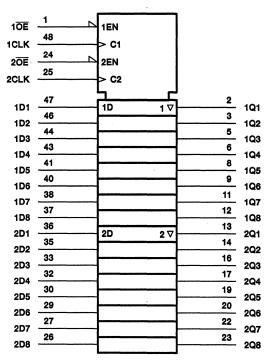


SCAS316B - NOVEMBER 1993 - REVISED JULY 1995

FUNCTION TABLE (each flip-flop)

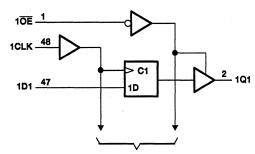
	INPUTS		OUTPUT
ŌĒ	CLK	D	Q
L	↑	Н	Н
L	1	L	L
L	H or L	Х	Q ₀
• н	X	X	Z

logic symbolt

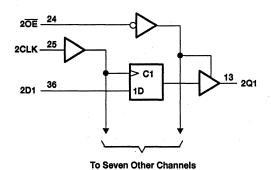


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels



SN74LVC16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS316B - NOVEMBER 1993 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

to 4.6 V
to 4.6 V
+ 0.5 V
-50 mA
$\pm 50 mA$
±50 mA
100 mA
0.85 W
. 1.2 W
to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
٧ _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
٧ _I	Input voltage		0	VCC	V
Vo	Output voltage		0	Vcc	٧
la		V _{CC} = 2.7 V		-12	A
ЮН	High-level output current	V _{CC} = 3 V	`	-24	mA
1	Laur laural autout aumant	V _{CC} = 2.7 V		12	4
lOL	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN74LVC16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS316B - NOVEMBER 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CO	ONDITIONS	vcct	MIN	TYP‡	MAX	UNIT	
		I _{OH} = -100 μA	l _{OH} = -100 μA		V _{CC} -0	.2			
		10		2.7 V	2.2			v	
VOH		I _{OH} = -12 mA		3 V	2.4			٧	
		I _{OH} = -24 mA		3 V	2				
		I _{OL} = 100 μA		MIN to MAX			0.2		
VOL		I _{OL} = 12 mA		2.7 V			0.4	٧	
		I _{OL} = 24 mA		3 V			0.55		
4		V _I = V _{CC} or GND		3.6 V			±5	μА	
		V _I = 0.8 V		3 V	75				
I _{I(hold)}	Data inputs	V _I = 2 V]	-75			μA	
` .	1	V _I = 0 to 3.6 V		3.6 V			±500		
loz		VO = VCC or GND		3.6 V			±10	μА	
ICC		V _I = V _{CC} or GND,	IO = 0	3.6 V			40	μА	
ΔlCC		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			500	μА	
Ci		V _I = V _{CC} or GND	•	3.3 V		3.5		рF	
Co		V _O = V _{CC} or GND		3.3 V		7		pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			VCC =	: 3.3 V .3 V	Vcc =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	100	0	80	MHz
t _w	Pulse duration, CLK high or low		4		4		ns
t _{su}	Setup time, data before CLK↑	High or low	2		3		ns
th	Hold time, data after CLK↑	High or low	1.5		1.5		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
	(INFOI)	(001701)	MIN	MAX	MIN	MAX	
fmax			100		80		MHz
^t pd	CLK	Q	1.5	7.5	1.5	8.5	ns
t _{en}	ŌĒ	Q	1.5	7.5	1.5	8.5	ns
^t dis	. ŌĒ	Q	1.5	7	1.5	8	ns

 $[\]ddagger$ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SCAS316B - NOVEMBER 1993 - REVISED JULY 1995

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$

	PARAMETER		TEST CONDITIONS	TYP	UNIT
	Down discinstion consistence nor file flor	Outputs enabled	O. 50 pE 4 40 MH=	22	
Cpd Power dissipation capacitance per flip-flop		Outputs disabled	C _L = 50 pF, f = 10 MHz	9	pF

PARAMETER MEASUREMENT INFORMATION **TEST** S1 O Open **500** Ω From Output Open tpd **Under Test** O GND 6 V tpLZ/tpZL tPHZ/tPZH GND CL = 50 pF **500** Ω (see Note A) 2.7 V LOAD CIRCUIT FOR OUTPUTS 1.5 V **Timing Input** tsu 2.7 V 2.7 V 1.5 V Input 1.5 V 1.5 V **Data Input** n V 0 V **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS PULSE DURATION SETUP AND HOLD TIMES** 2.7 V 2.7 V Output 1.5 V Input 1.5 V 1.5 V Control 0 V 0 V **tPZL** ^tPHL **tPLZ** Output VOH Waveform 1 Output S1 at 6 V VOL (see Note B) **tPHZ tPLH** tPHL: ^tPZH Output VOH Waveform 2 V_{OH} - 0.3 V Output S1 at GND (see Note B) **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS** PROPAGATION DELAY TIMES **ENABLE AND DISABLE TIMES INVERTING AND NONINVERTING OUTPUTS** LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - tpzL and tpzH are the same as ten.
 - G. tplH and tpHL are the same as tod.

Figure 1. Load Circuit and Voltage Waveforms



SN74LVC16540 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCAS349A - MARCH 1994 - REVISED JULY 1995

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Bus Hold on Data inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation; it can interface to a 5-V system environment.

SN74LVC16540 provides performance bus interface for wide datapaths.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable (OE1 or OE2) input is high, all corresponding outputs are in the high-impedance state.

(TOP VIEW) 10

DGG OR DL PACKAGE

10E1	1 ^U	48	
1Y1 [1A1
1Y2 [3		1A2
GND [GND
1Y3 [5		1A3
1Y4 [43] 1A4
v _{cc} [7	42	v _{cc}
1Y5 [8	41	1A5
1Y6 [9	40	1A6
GND[GND
1Y7 [38	1A7
1Y8 [12	37	1A8
2Y1 [13	36	2A1
2Y2[14	35	2A2
GND [34	GND
2Y3 [2A3
2Y4 [17		2A4
v _{cc} [18	31	v _{cc}
2Y5		30	2A5
2Y6 [20		2A6
GND[21		GND
2Y7 [2A7
2Y8 [23] 2A8
20E1	24	25	2 0E2
	1		

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC16540 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 8-bit section)

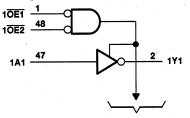
	INPUTS		OUTPUT
OE1	OE2	Α	Y
L	L	L	Н
L	L	Н	Ł
Н	X	Х	z
X	Н	Х	z

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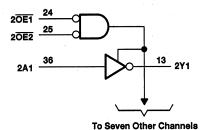
SCAS349A - MARCH 1994 - REVISED JULY 1995 logic symbolt

gic symboli						
1 <u>OE1</u>	48	&	EN1			
10E2 20E1	24	&				
2 OE2	25		EN2			
1A1	47			2	1Y1	
1A2	46			3	1Y2	
	44			5	1Y3	
1A3 1A4	43			6	1Y4	
1A5	41			8	1Y5	
1A6	40			9	1Y6	
1A7	38			11	1Y7	
1A7	37			12	1Y8	
	36		4 057	13		
2A1 2A2	35	<u> </u>	1 2▽	14	2Y1 2Y2	
2A3	33	<u> </u>		16	2Y3	
2A4	32			17	2Y4	
2A5	30	 		19	2Y5	
2A6	29			20	2Y6	
2A7	27	·		22	2Y7	
2A8	26			23	2Y8	

logic diagram (positive logic)



To Seven Other Channels



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 6.5 V
Input voltage range, V ₁	0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance state	
or power-off state, V _O (see Note 1)	0.5 V to 6.5 V
Voltage range applied to any output in the high	
or low state, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG p	ackage 0.85 W
DL pac	kage 1.2 W
Storage temperature range, T _{stg}	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.



recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V	Supply voltage	Operating		3.6	V
VCC	Supply voltage	Data retention only	1.5		V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
٧ _I	Input voltage		0	5.5	٧
٧o	Output voltage		0	Vcc	٧
la	High lovel output ourrent	V _{CC} = 2.7 V		-12	mA
ЮН	High-level output current	V _{CC} = 3 V		-24	IIIA
1	Low-level output current	V _{CC} = 2.7 V		12	mA
OL	Low-level output current	V _{CC} = 3 V		24	. IIIA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	v _{cc} †	MIN TYP#	MAX	UNIT	
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			
\ _{V=}		I _{OH} = -12 mA	2.7 V	2.2		v	
VOH		10H = -12 IIIA	3 V	2.4		v	
		I _{OH} = -24 mA	3 V	2.2			
		I _{OL} = 100 μA	100 μA MIN to MAX		0.2		
VOL		I _{OL} = 12 mA	2.7 V		0.4	٧	
		I _{OL} = 24 mA	3 V		0.55		
lį		V _I = 5.5 V or GND	3.6 V		±5	μА	
lia in	Data inputs	V _I = 0.8 V	3 V	75		μА	
I(hold)	Data inputs	V _I = 2 V	7 3 4	- 75			
loz		V _O = 5.5 V or GND	3.6 V		±10	μА	
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μА	
Δlcc		One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V		500	μА	
Ci		$V_{I} = V_{CC}$ or GND	3.3 V			pF	
Co		V _O = V _{CC} or GND	3.3 V			pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

 $[\]ddagger$ All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

DGG OR DL PACKAGE Member of the Texas Instruments (TOP VIEW) Widebus™ Family EPIC™ (Enhanced-Performance Implanted 10E1 48 10E2 **CMOS) Submicron Process** 1Y1 🛮 2 47 🛮 1A1 Typical V_{OLP} (Output Ground Bounce) 1Y2 🛮 3 46 🛮 1A2 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C GND []4 45 GND Typical V_{OHV} (Output V_{OH} Undershoot) 1Y3 🛮 5 44 🛭 1A3 $> 2 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$ 1Y4 🛮 6 43**[**] 1A4 Bus Hold on Data Inputs Eliminates the 42 V_{CC} V_{CC} 47 Need for External Pullup/Pulldown 1Y5 I 8 41 N 1A5 Resistors 1Y6 🛮 9 40 🛮 1A6 Supports Mixed-Mode Signal Operation on GND 1 10 39 🛛 GND All Ports (5-V Input/Output Voltage With 1Y7 11 38**[**] 1A7 3.3-V V_{CC}) 1Y8 🛮 12 37 D 1A8 2Y1 13 36 2A1 Package Options Include Plastic 300-mil 2Y2 114 35 D 2A2 Shrink Small-Outline (DL) and Thin Shrink GND 115 34 GND Small-Outline (DGG) Packages 2Y3 116 33 D 2A3 description 32 🛮 2A4 2Y4 1 17 V_{CC} [] 18 31 D VCC This 16-bit buffer/driver is designed for 2.7-V to 2Y5 19 30 2A5 3.6-V V_{CC} operation; it can interface to a 5-V 2Y6 20 29 D 2A6 system environment. GND 1 21 28 GND 2Y7 22 27 🛮 2A7 The SN74LVC16541 is a noninverting 16-bit buffer composed of two 8-bit sections with 2Y8 II 23 26 II 2A8 20E1 24 25 20E2 separate output-enable signals. For either 8-bit

10E2 or 20E1 and 20E2) inputs must both be low for the corresponding Y outputs to be active. If eithe output-enable input is high, the outputs of that 8-bit buffer section are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVC16541 is characterized for operation from -40°C to 85°C.

buffer section, the two output-enable (1OE1 and

FUNCTION TABLE (each 8-bit section)

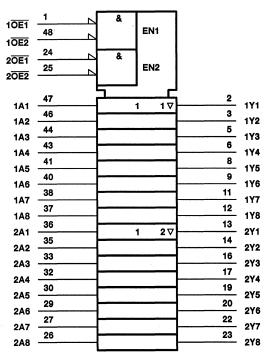
(
INPUTS			OUTPUT				
OE1	OE2	Α	Y				
L	L	L	L				
L	L	Н	н				
Н	X	Χ	z				
×	Н	Χ	z				

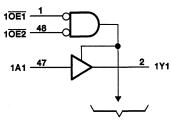
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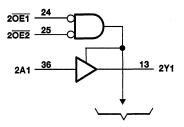
logic symbol†

logic diagram (positive logic)





To Seven Other Channels



To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} –0.5 V to 6.5 V
Input voltage range, V ₁
Voltage range applied to any output in the high-impedance state
or power-off state, V _O (see Note 1)
Voltage range applied to any output in the high
or low state, V _O (see Notes 1 and 2)
Input clamp current, $I_{ K }(V_1 < 0)$ —50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ± 50 mA
Continuous output current, I _O (V _O = 0 to V _{CC}) ±50 mA
Continuous current through V _{CC} or GND
Maximum power dissipation at TA = 55°C (in still air) (see Note 3): DGG package
DL package 1.2 W
Storage temperature range, T _{stq} –65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

RODUCT PREVIEW

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V	Cumples soltage	Operating		3.6	V
VCC	Supply voltage	Data retention only	1.5		V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
VΙ	Input voltage		0	VCC	٧
Vo	Output voltage		0	Vcc	٧
la	High-level output current	V _{CC} = 2.7 V		-12	mA
ЮН		V _{CC} = 3 V		-24	IIIA
la.	Low-level output current	V _{CC} = 2.7 V		12	mA
lOL	Low-level output current	V _{CC} = 3 V		24	IIIA
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	v _{cc} †	MIN	TYP‡	MAX	UNIT	
		I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.:	2			
l.,		I _{OH} = -12 mA	2.7 V	2.2			v	
VOH		IOH = - 12 IIIA	3 V	2.4			, v	
		$I_{OH} = -24 \text{ mA}$	3 V	2.2				
VOL		I _{OL} = 100 μA	MIN to MAX			0.2		
		I _{OL} = 12 mA	2.7 V			0.4	V	
		I _{OL} = 24 mA	3 V			0.55		
II		V _I = 5.5 V or GND	3.6 V			±5	μА	
ha in	Data inputs	V ₁ = 0.8 V	3 V	75				
l(hold)	Data inputs	V _I = 2 V	7	-75			μΑ	
loz		V _O = 5.5 V or GND	3.6 V			±10	μА	
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ	
Δlcc		One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	μА	
Ci		V _I = V _{CC} or GND	3.3 V				pF	
Co		V _O = V _{CC} or GND	3.3 V				pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

 $[\]ddagger$ All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS317A - NOVEMBER 1993 - REVISED OCTOBER 1995

 Member of the Texas Instruments Widebus™ Family 		OR DL PACI (TOP VIEW)	
 EPIC ™ (Enhanced-Performance Implanted CMOS) Submicron Process 	10EAB [1 OEBA
 Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C 	1CEAB [GND [3 54	1 ICEBA 1 GND
 Typical V_{OHV} (Output V_{OH} Undershoot) 2 V at V_{CC} = 3.3 V, T_A = 25°C 	1A1 [1A2 [5 52	1B1 1B2
 Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17 	V _{CC} [7 50	V _{CC}
 Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown 	1A4 [1A5 [10 47] 1B4] 1B5
Resistors Package Options Include Plastic 300-mil	GND [1A6 [12 45	GND 1B6
Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages	1A7 [1A8 [14 43] 1B7] 1B8
description	2A1 [2A2 [2A3 [16 41] 2B1] 2B2] 2B3
This 16-bit registered transceiver is designed for low-voltage (3.3-V) V_{CC} operation.	GND [2A4 [18 39] GND] 2B4
The SN74LVC16543 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate	2A5 [2A6 [20 37] 2B5] 2B6
latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each	V _{CC} [2A7 [23 34] V _{CC}] 2B7
register to permit independent control in either direction of data flow.	2A8 [GND [25 32] 2B8] GND
The A-to-B enable (CEAB) input must be low in order to enter data from A or to output data from B. If CEAB is low and LEAB is low, the A-to-B	2CEAB [2LEAB [2OEAB [27 30] 2CEBA] 2LEBA] 2OEBA
latches are transparent; a subsequent low-to-high transition of LEAB puts the A latches in the storage mode. With CEAB and OEAB both low,			

the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the CEBA, LEBA, and OEBA inputs.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16543 is characterized for operation from -40°C to 85°C.

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FUNCTION TABLET (each 8-bit section)

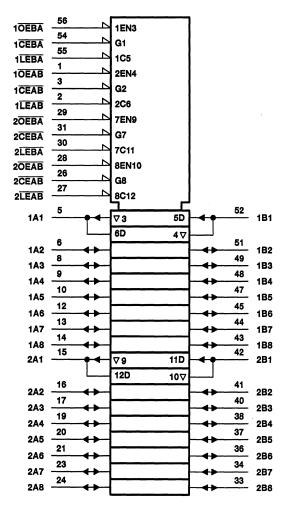
	OUTPUT					
CEAB	LEAB	OEAB	Α	В		
Н	Х	Х	Х	Z		
х	Х	Н	Χ	z		
L	Н	L	X	в ₀ ‡		
L	L	L	L	L		
L	L	L	Н	н		

[†] A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

[‡] Output level before the indicated steady-state input conditions were established

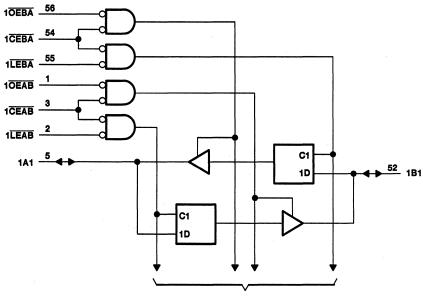
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logic symbol†

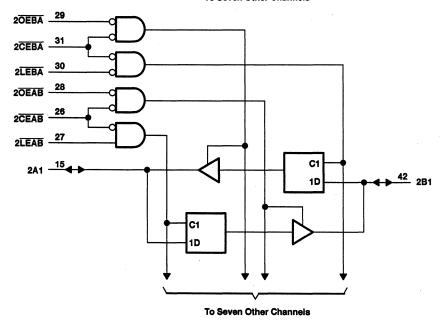


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels



SCAS317A - NOVEMBER 1993 - REVISED OCTOBER 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG packag	je 1 W
DL package	1.4 W
Storage temperature range, T _{stg}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

	· · · · · · · · · · · · · · · · · · ·		MIN	MAX	UNIT
VCC	Supply voltage		2.7	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
VI	Input voltage		0	Vcc	٧
۷o	Output voltage		0	Vcc	٧
la	High-level output current	V _{CC} = 2.7 V		-12	m 1
ЮН		V _{CC} = 3 V		-24	mA
la.	Low level output current	V _{CC} = 2.7 V		12	A
lOL	Low-level output current VCC = 3 V			24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SCAS317A - NOVEMBER 1993 - REVISED OCTOBER 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	vcct	MIN TYP‡	MAX	UNIT	
		i _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2			
\ _{V=-}		la., 10 mA	2.7 V	2.2		v	
VOH		I _{OH} = -12 mA	3 V	2.4		V	
		I _{OH} = -24 mA	3 V	2			
		I _{OL} = 100 μA	MIN to MAX		0.2		
VOL		I _{OL} = 12 mA	2.7 V	,	0.4	0.4 V	
		I _{OL} = 24 mA	3 V	0.55			
Ιţ	Control inputs	V _I = V _{CC} or GND	3.6 V		±5	μА	
	A D	V _I = 0.8 V	3 V	75		4	
l(hold)	A or B ports	V _I = 2 V		- 75	,	μА	
I _{OZ} §		V _O = V _{CC} or GND	3.6 V		±10	μА	
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		40	μА	
Δlcc		One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GN	3 V to 3.6 V		500	μА	
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V	3		pF	
Cio	A or B ports	V _O = V _{CC} or GND	3.3 V	7		pF	

 $[\]dagger$ For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions. \ddagger All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V _{CC} = 3.3 V ± 0.3 V		V _{CC} =	UNIT	
		MIN	MAX	MIN	MAX	
tw	Pulse duration, LE or CE low	4		4		ns
t _{su}	Setup time, Data before LE, CE	2		2		ns
th	Hold time, Data after LE, CE	2		2		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	3.3 V 3 V	V _{CC} =	2.7 V	UNIT
	(INFOT)	(001701)	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	1.5	8	1.5	9	ns
t _{pd}	ĪĒ.	A or B	1.5	9	1.5	10	ns
t _{en}	CE	A or B	1.5	9	1.5	10	ns
^t dis	CE	A or B	1.5	9	1.5	10	ns
ten	ŌĒ	A or B	1.5	8.5	1.5	9.5	ns
^t dis	ŌĒ	A or B	1.5	8.5	1.5	9.5	ns

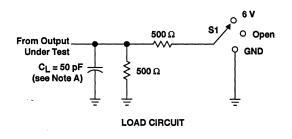


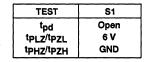
[§] For I/O ports, the parameter IOZ includes the input leakage current.

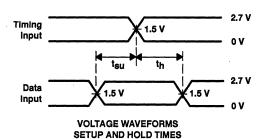
operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

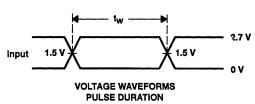
	PARAMETER			TEST CONDITIONS		
Γ	Power dissipation capacitance per transceiver	Outputs enabled	C. 50 nE	f = 10 MHz	21	pF
1	pd Power dissipation capacitance per transceiver	Outputs disabled	$C_L = 50 pF$,	1 = 10 MITZ	3.5	pr-

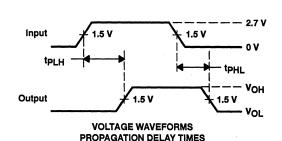
PARAMETER MEASUREMENT INFORMATION

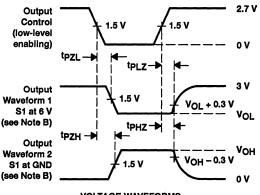












VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns.}$ tf \leq 2.5 ns. $t_r \leq$ 2.5 ns.
- The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tpd.

SCAS318B - NOVEMBER 1993 - REVISED JULY 1995

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted **CMOS) Submicron Process**
- Typical VOLP (Output Ground Bounce) $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit bus transceiver and register is designed for low-voltage (3.3-V) V_{CC} operation.

The SN74LVC16646 can be used as two 8-bit transceivers or one 16-bit transceiver. The device consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers.

Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74LVC16646.

DGG OR DL PACKAGE (TOP VIEW)

		U		L
1DIR [56	10E
1CLKAB			55	1CLKBA
1SAB [3		54] 1SBA
GND [4] GND
1A1 🛭	5] 1B1
1A2 [6		51	1B2
v _{cc} [7		50	V _{CC}
1A3 [8		49	1B3
1A4 [9		48	1B4
1A5 [10		47] 1B5
GND [11		46	GND
1A6 [12		45] 1B6
1A7 [13		44] 1B7
1A8 [14			1B8
2A1 [15		42	2B1
2A2 [16		41] 2B2
2A3 [17] 2B3
GND [18		39	GND
2A4 [19		38] 2B4
2A5 [20			2B5
2A6 [21			2B6
V _{CC} [22		35] v _{cc}
2A7 [23		34	2B7
2A8 [24		33	2B8
GND [25		32	GND
2SAB				2SBA
2CLKAB				2CLKBA
2DIR	28			20E

Output-enable (OE) and direction-control (DIR) inputs control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. DIR determines which bus receives data when \overline{OE} is low. In the isolation mode (\overline{OE} high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and can be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or floating data inputs at a valid logic level.

The SN74LVC16646 is characterized for operation from -40°C to 85°C.

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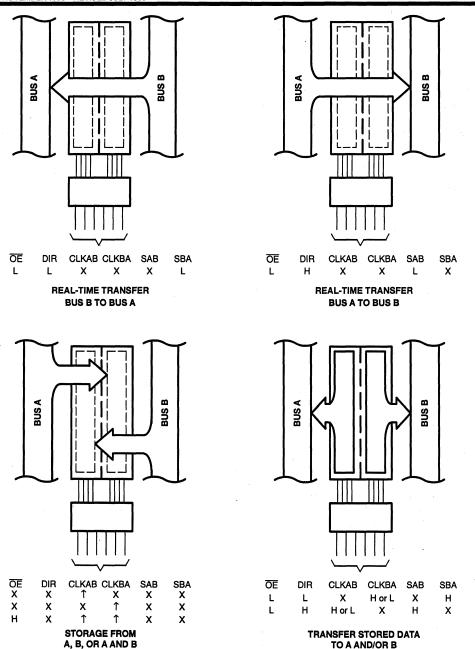
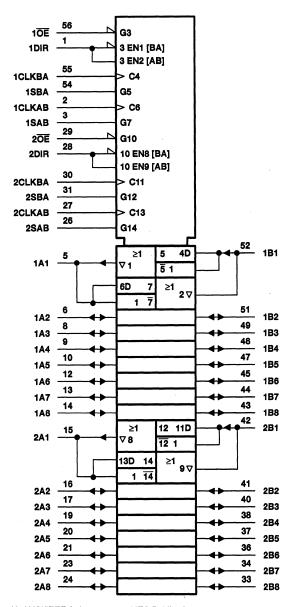


Figure 1. Bus-Management Functions



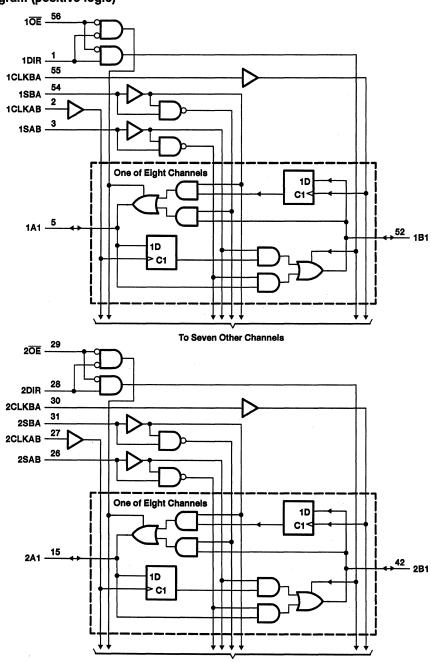
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logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





To Seven Other Channels

SCAS318B - NOVEMBER 1993 - REVISED JULY 1995

FUNCTION TABLE

	INPUTS			DATA	A I/Os	OPERATION OR FUNCTION		
OE	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
X	X	1	Х	Х	Х	Input	Unspecified [†]	Store A, B unspecified†
х	X	X	1	X	X	Unspecified†	Input	Store B, A unspecified [†]
Н	Х	1	1	Х	Х	Input	Input	Store A and B data
н	Х	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	Х	Х	Х	L	Output	Input	Real-time B data to A bus
L	L	Х	H or L	X	Н	Output	Input	Stored B data to A bus
L	Н	Х	Х	L	Х	Input	Output	Real-time A data to B bus
L	Н	H or L	X	Н	X	Input	Output	Stored A data to B bus

[†] The data output functions may be enabled or disabled by various signals at the $\overline{\text{OE}}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)	
I/O ports (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, $I_{ K }(V_1 < 0)$	–50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3):	
,,	DL package 1.4 W
Storage temperature range, T _{stg}	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

SCAS318B - NOVEMBER 1993 - REVISED JULY 1995

recommended operating conditions (see Note 4)

		,	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
۷į	Input voltage		0	Vcc	٧
٧o	Output voltage		0	Vcc	٧
1	Ligh level subsub surrent	V _{CC} = 2.7 V		-12	mA
ЮН	High-level output current	V _{CC} = 3 V		-24	IIIA
1	Low level autout aument	V _{CC} = 2.7 V		12	^
lOL	Low-level output current	V _{CC} = 3 V		24	mA
Δt/ΔV	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	vcct	MIN TYP	MAX	UNIT
		IOH = -100 μA	MIN to MAX	V _{CC} -0.2		
V		lou 12 mA	2.7	2.2		v
VOH		I _{OH} = -12 mA	3	2.4		ľ
		I _{OH} = -24 mA	3	2		
		I _{OL} = 100 μA	MIN to MAX		0.2	
VOL		I _{OL} = 12 mA	2.7		0.4	V
		I _{OL} = 24 mA	3		0.55	
Ц	Control inputs	V _I = V _{CC} or GND	3.6		±5	μА
		V _I = 0.8 V	3	75		
II(hold)	A or B ports	V _I = 2 V	7	-75		μА
		V _I = 0 to 3.6 V	3.6		±500	
l _{OZ} §		V _O = V _{CC} or GND	3.6		±10	μА
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6		40	μА
Δlcc		One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V		500	μА
Ci	Control inputs	VI = VCC or GND	3.3	3	1	pF
Cio	A or B ports	V _O = V _{CC} or GND	3.3	7	•	рF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. § For I/O ports, the parameter I_{OZ} includes the input leakage current.

SCAS318B - NOVEMBER 1993 - REVISED JULY 1995

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V _{CC} =	3.3 V 3 V	V _{CC} =	2.7 V	UNIT
			MIN	MAX	MIN	MAX	
^f clock	Clock frequency		0	100	0	80	MHz
tw	Pulse duration, CLK high or low		4.5		4.5		ns
t _{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	Data high or low	5		5		ns
th	Hold time, A or B after CLKAB↑ or CLKBA↑	Data high or low	0		0		ns

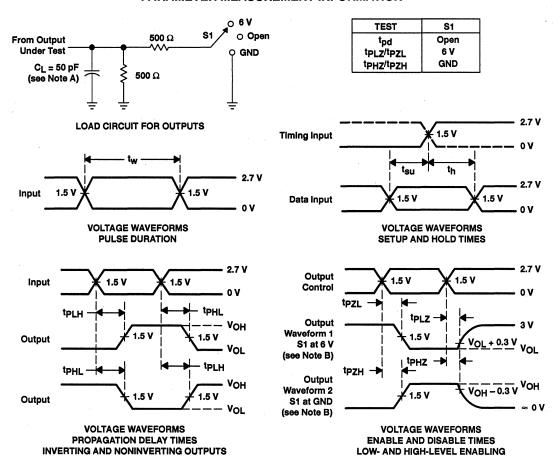
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =		V _{CC} =	2.7 V	UNIT	
	(INFOI)	(OUTPOT)	MIN	MAX	MIN	MAX		
f _{max}			100		80		MHz	
	A or B	B or A	1.5	7		8		
^t pd	CLKAB or CLKBA	A or B	1.5	8.5		9.5	ns	
	SAB or SBA		1.5	8.5		9.5		
	ŌĒ	Asse	1.5	8		9		
^t en	DIR	A or B	1.5	8		9	ns	
+	ŌĒ	A or B	1.5	8.5		9.5		
^t dis	DIR	A OF B	1.5	8.5		9.5	ns	

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	TYP	UNIT	
	Device discinsting considers and transfer	Outputs enabled	0. 505 4 40.40-	17	
Cpd	Power dissipation capacitance per transceiver	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	4	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq 2.5 \ ns$, $t_f \leq 2.5 \ ns$.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 2. Load Circuit and Voltage Waveforms

SCAS319B - NOVEMBER 1993 - REVISED JULY 1995

•	Member of	the Texas	Instruments
	Widebus™	Family	

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit bus transceiver and register is designed for low-voltage (3.3-V) V_{CC} operation.

The SN74LVC16652 consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary output-enable (OEAB and OEBA) inputs control the transceiver functions. Select-control (SAB and SBA) inputs select whether real-time or stored data is transferred. A

DGG OR DL PACKAGE (TOP VIEW)

10EAB	₁ O	56	1OEBA
1CLKAB	2		1CLKBA
1SAB	3] 1SBA
GND [4		GND
1A1 [52] 1B1
1A2 [1B2
v _{cc}]	7	50] v _{cc}
1Ă3 🛚	8	49] 1B3
1A4 🛚		48	1B4
1A5 🏻	10	47	1B5
GND [11	46	GND
1A6 🛚		45] 1B6
1A7 🛚			1B7
1A8 🏻] 1B8
2A1 🛚			2B1
2A2 🛚		41	2B2
2A3 🛚		40] 2B3
GND [GND
2A4 🛚			2B4
2A5 🛚			2B5
2A6 🛚	21		2B6
v _{cc} [22	35] v _{cc}
2A7 🛚	23		2B7
2A8 🛚] 2B8
GND [GND
2SAB [26		2SBA
2CLKAB	27	30	2CLKBA
20EAB	28	29	2 OEBA
			•

low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74LVC16652.

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SCAS319B - NOVEMBER 1993 - REVISED JULY 1995

description (continued)

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration, each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last level configuration.

To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to V_{CC} through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry holds unused or floating data inputs at a valid logic level.

The SN74LVC16652 is characterized for operation from -40°C to 85°C.



WITH 3-STATE OUTPUTS SCAS319B - NOVEMBER 1993 - REVISED JULY 1995 **BUSA BUSA** BUS BUS OEAB OEBA CLKAB CLKBA SAB SBA OEAB OEBA CLKAB CLKBA SAB SBA х Н н Х **REAL-TIME TRANSFER REAL-TIME TRANSFER BUS B TO BUS A BUS A TO BUS B** BUS B **BUSA** 8 **BUSA** BUS OEAB OEBA CLKAB CLKBA SAB SBA OEAB OEBA CLKAB SBA CLKBA SAB Χ н 1 Χ Χ Х Н L H or L H or L Н L Х 1 Х Х Х L 1 Н Х

Figure 1. Bus-Management Functions

TRANSFER STORED DATA

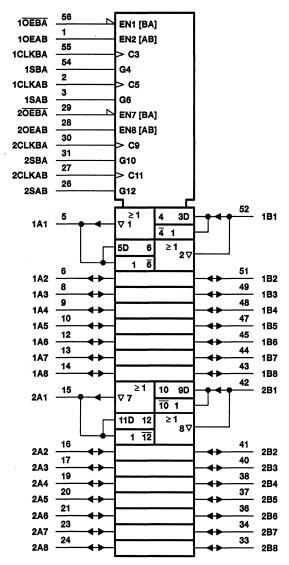
TO A AND/OR B

STORAGE FROM

A, B, OR A AND B



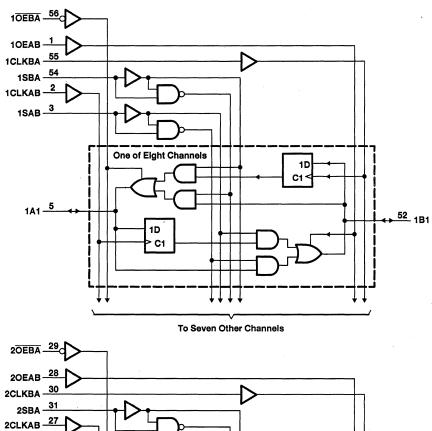
logic symbol†

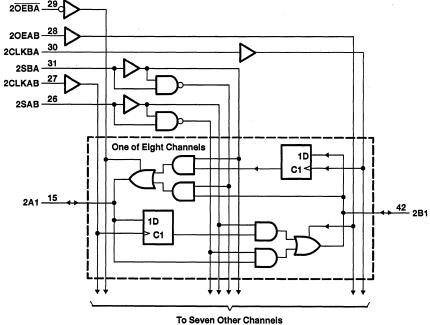


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)







SN74LVC16652 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS319B - NOVEMBER 1993 - REVISED JULY 1998

FUNCTION TABLE

INPUTS						DATA	a vot	OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	OPERATION OR FUNCTION
L	Н	H or L	H or L	X	Х	Input	Input	Isolation
L	Н	1	1	X	X	Input	Input	Store A and B data
X	Н	1	H or L	Χ.	Х	Input	Unspecified [‡]	Store A, hold B
Н	Н	1:	1	X ‡	X	Input	Output	Store A in both registers
L	X	H or L	1	X	X	Unspecified [‡]	Input	Hold A, store B
L	L	1	1	X	χ‡	Output	Input	Store B in both registers
L	L	X	Х	х	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	н	Output	Input	Stored B data to A bus
Н	Н	X	X	L	X	Input	Output	Real-time A data to B bus
Н	Н	H or L	X	Н	Х	Input	Output	Stored A data to B bus
н	L	H or L	H or L	н	Н	Output	Output	Stored A data to B bus and Stored B data to A bus

[†] The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition on the clock inputs.

Select control = H; clocks must be staggered in order to load both registers.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)	0.5 V to 4.6 V
	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0)	–50 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3)	: DGG package 1 W
	DL package 1.4 W
Storage temperature range, T _{stg}	

[§] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

[‡] Select control = L; clocks can occur simultaneously.

16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS319B - NOVEMBER 1993 - REVISED JULY 1995

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	٧
٧ _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		V
٧ _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		8.0	٧
VI	Input voltage		0	VCC	٧
٧o	Output voltage		0	Vcc	٧
	$V_{CC} = 2.7 \text{ V}$			-12	mA
V _O	High-level output current	V _{CC} = 3 V		-24	IIIA
la:	Levelevel entent current	V _{CC} = 2.7 V		12	A
IOL	Low-level output current VCC = 3 V			24	mA
Δt/ΔV	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CO	ONDITIONS	v _{cc} t	MIN	TYP‡	MAX	UNIT
		I _{OH} = -100 μA		MIN to MAX	VCC-0	.2		
		IOH = -12 mA		2.7	2.2			v
VOH		IOH = - 12 IIIA		3	2.4			V
		IOH = -24 mA		3	2			
		I _{OL} = 100 μA	1	MIN to MAX			0.2	
VOL		I _{OL} = 12 mA		2.7			0.4	٧
		I _{OL} = 24 mA		3			0.55	
lį	Control inputs	V _I = V _{CC} or GND		3.6			±5	μA
		V _i = 0.8 V		3	75			
l(hold)	A or B ports	V _I = 2 V]. "	-75			μА
		V _I = 0 to 3.6 V		3.6			±500	
loz§		VO = VCC or GND		3.6			±10	μА
ICC		$V_I = V_{CC}$ or GND,	IO = 0	3.6			40	μА
Δlcc		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			500	μА
Ci	Control inputs	V _I = V _{CC} or GND		3.3		3		pF
Cio	A or B ports	VO = VCC or GND		3.3		7		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. § For I/O ports, the parameter I_{OZ} includes the input leakage current.

SN74LVC16652 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS319B - NOVEMBER 1993 - REVISED JULY 1995

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V _{CC} =		V _{CC} =	V _{CC} = 2.7 V	
			MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	100	0	80	MHz
t _W	Pulse duration, CLK high or low		4.5		4.5		ns
t _{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	Data high or low	5		5		ns
th	Hold time, A or B after CLKAB↑ or CLKBA↑	Data high or low	0		0		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

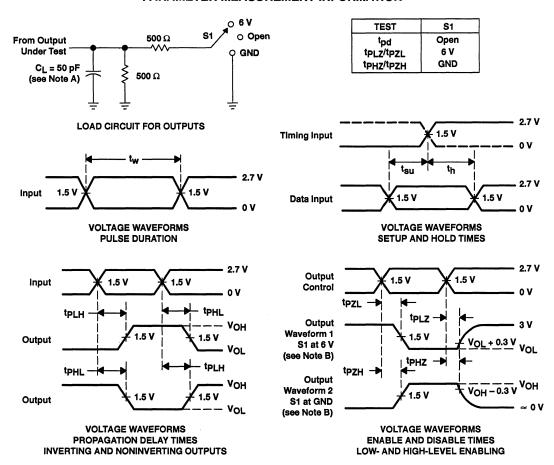
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	
	(14-01)	(001701)	MIN	MAX	MIN	MAX	İ
fmax			100		80		MHz
	A or B	B or A	1.5	7		8	
t _{pd}	CLKAB or CLKBA	A or D	1.5	8.5		9.5	ns
	SAB or SBA	A or B	1.5	8.5		9.5	
t _{en}	OE or OE	A or B	1.5	8		9	ns
^t dis	OE or OE	A or B	1.5	8.5		9.5	ns

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER			TEST CONDITIONS	TYP	UNIT
C	Power dissipation capacitance per transceiver	Outputs enabled Outputs disabled	C _L = 50 pF, f = 10 MHz	25 4	pF

SCAS319B - NOVEMBER 1993 - REVISED JULY 1995

PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tplH and tpHL are the same as tod.

Figure 2. Load Circuit and Voltage Waveforms

SN74LVC16952 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS320A - NOVEMBER 1993 - REVISED JULY 1995

•	Member of	the	Texas	Instruments
	Widebus™	Far	nily	

- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

description

This 16-bit registered transceiver is designed for low-voltage (3.3-V) V_{CC} operation; it can interface to a 5-V system environment.

The SN74LVC16952 contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. It can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable (CEAB or CEBA) input is low. Taking the output-enable (OEAB or OEBA) input low accesses the data on either port.

DGG OR DL PACKAGE (TOP VIEW)

_		ι,		_
1OEAB]1	_	56	10EBA
1CLKAB [2] 1CLKB/
1CEAB			54	1CEBA
GND [53	GND
1A1 [5] 1B1
1A2 []6		51] 1B2
v _{cc} []7		50	v_{cc}
1A3 [8		49	1B3
1A4 []9		48] 1B4
1A5 [10		47] 1B5
GND [11		46	GND
1A6 [12		45] 1B6
1A7 [44] 1B7
1A8 [14		43] 1B8
2A1 [42] 2B1
2A2 [41	2B2
2A3 [17		40	2B3
GND [GND
2A4 [38	2B4
2A5 [37	2B5
2A6 [21		36	2B6
v _{cc} [22		35] v _{cc}
2A7 [23		34	2B7
2A8 [24		33] 2B8
GND [32	GND
2CEAB			31	2CEBA
2CLKAB [27		30	2CLKB/
2 OEAB [28		29	2 OEBA

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16952 is characterized for operation from -40°C to 85°C.

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SN74LVC16952 16-BIT REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

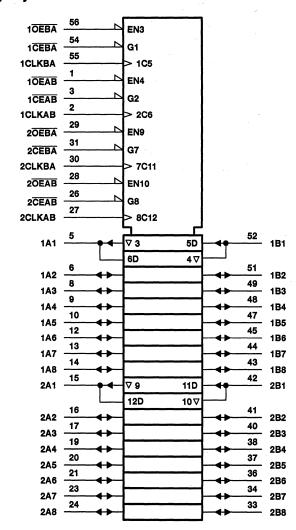
SCAS320A - NOVEMBER 1993 - REVISED JULY 1995

FUNCTION TABLET

	OUTPUT			
CLKENAB	CLKAB	OEAB	В	
Н	Х	L	Х	B ₀ ‡
х	L.	L	Х	В ₀ ‡ В ₀ ‡
L	1	L	L	L
L	1	L	Н	Н
х	X	н	Х	z

[†] A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENBA, CLKBA, and OEBA.

logic symbol†

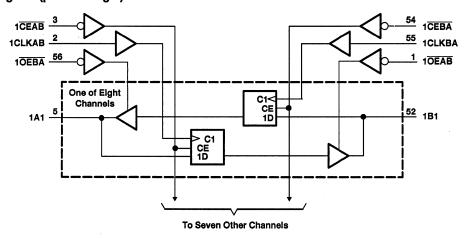


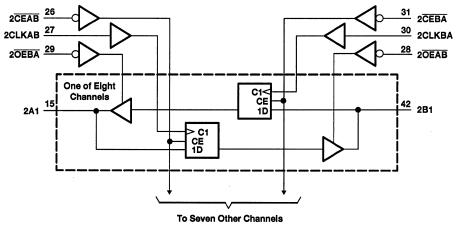
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



[‡] Level of B before the indicated steady-state input conditions were established

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 6.5 V
Input voltage range, V ₁	0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance state	
or power-off state, V _O (see Note 1)	0.5 V to 6.5 V
Voltage range applied to any output in the high	
or low state, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{ K }(V_1 < 0)$	–50 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, IO (VO = 0 to VCC)	±50 mA
Continuous current through V _{CC} or GND	±100 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	ge 1 W
DL package	1.4 W
Storage temperature range, T _{sto}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Voc	Supply voltage	Operating	2	3.6	V
VCC	Supply Voltage	Data retention only	1.5		· ·
٧ _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2		٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V		0.8	٧
۷Į	Input voltage		0	5.5	٧
٧o	Output voltage		0	VCC	٧
lou	High lovel output ourrent	V _{CC} = 2.7 V		-12	mA
IOH	OH High-level output current	V _{CC} = 3 V		-24	IIIA
lou	Low-level output current	V _{CC} = 2.7 V		12	
lOL	Low-level output current	V _{CC} = 3 V		24	mA
Δt/Δν	Input transition rise or fall rate		0	10	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

SN74LVC16952 **16-BIT REGISTERED TRANSCEIVER** WITH 3-STATE OUTPUTS SCAS320A - NOVEMBER 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST COND	ITIONS	vcct	MIN	TYP‡	MAX	UNIT	
		lOH = -100 μA		MIN to MAX	V _{CC} -0.	2			
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \		lass 10 mA		2.7 V	2.2			v	
VOH		IOH = -12 mA	,	3 V	2.4			0.2 0.4 V	
		I _{OH} = -24 mA		3 V	2.2				
		I _{OL} = 100 μA		MIN to MAX			0.2		
VOL		I _{OL} = 12 mA		2.7 V			0.4	V	
ļ		I _{OL} = 24 mA		3 V	0.5		0.55	}	
l _l		V _I = 5.5 V or GND		3.6 V			±5	μА	
	A au B name	V _I = 0.8 V		0.1/	75				
I(hold)	A or B ports	V _I = 2 V		3 V75		-75		- μΑ	
I _{OZ} §		V _O = 5.5 V or GND		3.6 V			±10	μА	
Icc		VI = VCC or GND, IO	= 0	3.6 V			40	μA	
ΔlCC		One input at V _{CC} - 0.6 V, Ot	her inputs at V _{CC} or GND	2.7 V to 3.6 V			500	μА	
Ci	Control inputs	VI = VCC or GND		3.3 V				pF	
Cio	A or B ports	VO = VCC or GND		3.3 V				pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. § For I/O ports, the parameter I_{OZ} includes the input leakage current.

General Information	1
ALB Widebus™	2
ALVC Widebus™	3
LVT Octals	4
LVTZ Octals: Power Up and 3 State	5
LVT Widebus™	6
LVT JTAG/IEEE 1149.1	7
LVC MSI and Octals	8
LVC Widebus™	9
LV MSI and Octals	10
GTL Transceivers and Backplane Drivers	11
Application Reports	12
Characteristics Information	13
Mechanical Data	14

Contents

		Page
SN74LV00	Quadruple 2-Input Positive-NAND Gate	10-3
SN74LV02	Quadruple 2-Input Positive-NOR Gate	10-7
SN74LV04	Hex Inverter	10-11
SN74LVU04	Hex Inverter	10-15
SN74LV08	Quadruple 2-Input Positive-AND Gate	10-19
SN74LV14	Hex Schmitt-Trigger Inverter	10-23
SN74LV32	Quadruple 2-Input Positive-OR Gate	10-27
SN74LV74	Dual Positive-Edge-Triggered D-Type Flip-Flop	10-31
SN74LV125	Quadruple Bus Buffer Gate With 3-State Outputs	10-37
SN74LV138	3-Line to 8-Line Decoder/Demultiplexer	10-41
SN74LV164	8-Bit Parallel-Out Serial Shift Register	10-47
SN74LV165	Parallel-Load 8-Bit Shift Register	10-53
SN74LV174	Hex D-Type Flip-Flop With Clear	10-59
SN74LV240	Octal Buffer/Driver With 3-State Outputs	10-63
SN74LV244	Octal Buffer/Driver With 3-State Outputs	10-67
SN74LV245	Octal Bus Transceiver With 3-State Outputs	
SN74LV273	Octal D-Type Flip-Flop With Clear	10-75
SN74LV373	Octal Transparent D-Type Latch With 3-State Outputs	10-79
SN74LV374	Octal Edge-Triggered D-Type Flip-Flop With 3-State Outputs	10-83
SN74LV573	Octal Transparent D-Type Latch With 3-State Outputs	10-87
SN74LV574	Octal Edge-Triggered D-Type Flip-Flop With 3-State Outputs	10-91

SN74LV00 QUADRUPLE 2-INPUT POSITIVE-NAND GATE

SCLS182A - FEBRUARY 1993 - REVISED JULY 1995

 EPIC™ (Enhanced-Performance Implanted CMOS) 2-μ Process

- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE (TOP VIEW)

1A 1B 1Y 2A 2B 2Y GND	2 3 4 5 6	12 11 10 9	V _{CC} 4B 4A 4Y 3B 3A 3Y
GND	7	8] 3Y

description

This quadruple 2-input positive-NAND gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV00 performs the Boolean functions $Y = \overline{A} \cdot \overline{B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN74LV00 is available in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV00 is characterized for operation from -40°C to 85°C.

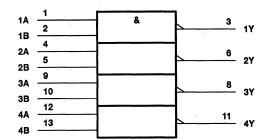
FUNCTION TABLE (each gate)

INP	UTS	OUTPUT
Α	В	Υ
Н	Н	L
′ L	X	н
×	L	н

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logic symbol†

logic diagram, each gate (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} 0.5 V to 4.6 V	
Input voltage range, V _I (see Note 1)	
Output voltage range, V _O (see Notes 1 and 2)	
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ±20 mA	
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ± 50 mA	
Continuous output current, I _O (V _O = 0 to V _{CC}) ±25 mA	
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): D package	
DB or PW package 0.5 W	
Storage temperature range, T _{sto} –65°C to 150°C	

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2.7	3.3	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	٧
VI	Input voltage		0		VCC	٧
Vo	Output voltage		0	300	VCC	٧
ЮН	High-level output current				-6	mA _.
lOL	Low-level output current				6	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74LV00 QUADRUPLE 2-INPUT POSITIVE-NAND GATE

SCLS182A - FEBRUARY 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} t	MIN TYP	MAX	UNIT
V	I _{OH} = −100 µA	MIN to MAX	V _{CC} -0.2		v
VOH	I _{OH} = -6 mA	3 V	2.4		V
Vo	I _{OL} = 100 μA	MIN to MAX		0.2	V
VOL	$I_{OL} = 6 \text{ mA}$	3 V		0.4	V
lį	V _I = V _{CC} or GND	3.6 V		±1	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА
ΔlCC	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V		500	μА
Ci	V _I = V _{CC} or GND	3.3 V	2.5		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

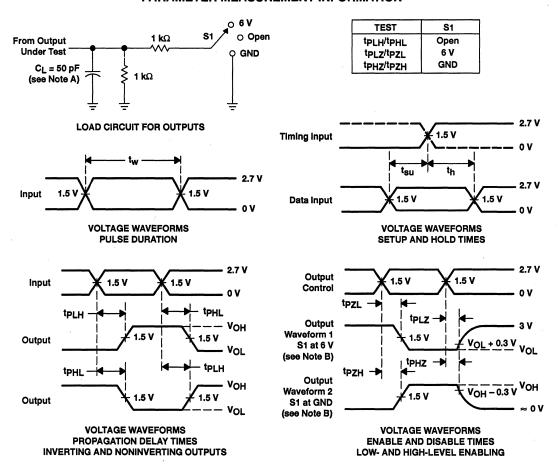
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	V _{CC} =	3.3 V ±	0.3 V	V _{CC} =	2.7 V	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	ONLI
^t pd	Α	Y		9	18		23	ns

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CO	NDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per gate	C _L = 50 pF,	f = 10 MHz	23	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



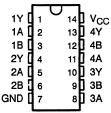
SN74LV02 QUADRUPLE 2-INPUT POSITIVE-NOR GATE

SCLS183A - FEBRUARY 1993 - REVISED JULY 1995

 EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process

- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE (TOP VIEW)



description

This quadruple 2-input positive-NOR gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV02 performs the Boolean functions $Y = \overline{A} + \overline{B}$ or $Y = \overline{A} \bullet \overline{B}$ in positive logic.

The SN74LV02 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV02 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each gate)

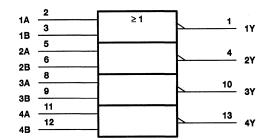
	INP	UTS	OUTPUT			
Г	Α	В	Y			
	Н	Х	L			
	Х	Н	L			
l	L	L	Н			

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logic symbolt

logic diagram, each gate (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	
input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	
Continuous current through V _{CC} or GND	±50 mA
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): D package	
DB or PW package	0.5 W
Storage temperature range, T _{stq}	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2.7	3.3	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	٧
۷Į	Input voltage		0		Vcc	٧
Vo	Output voltage		0		Vcc	٧
ЮН	High-level output current				-6	mA
lOL	Low-level output current				6	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SCLS183A - FEBRUARY 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcct	MIN TYP	MAX	UNIT
V _{OH}	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		ν
	I _{OH} = -6 mA	3 V	2.4		V
	I _{OL} = 100 μA	MIN to MAX		0.2	V
VOL	I _{OL} = 6 mA	3 V		0.4	V
11	V _I = V _{CC} or GND	3.6 V		±1	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μA
ΔlCC	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V		500	μА
Ci	V _I = V _{CC} or GND	3.3 V	2.5		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

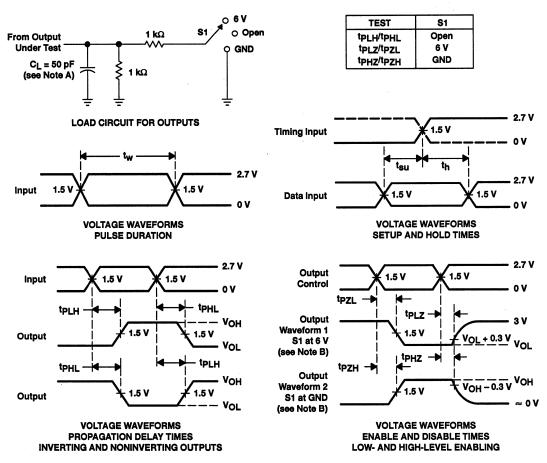
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	V _{CC} =	3.3 V ±	0.3 V	V _{CC} =	2.7 V	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	ONLI
^t pd	Α	Y		9	16		20	ns

operating characteristics, $V_{CC} = 3.3 V$, $T_A = 25 ^{\circ}C$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per gate	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	16	pF

PARAMETER MEASUREMENT INFORMATION



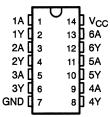
NOTES: A. Cl. includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE (TOP VIEW)



description

This hex inverter is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV04 contains six independent inverters. The device performs the Boolean function $Y = \overline{A}$.

The SN74LV04 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV04 is characterized for operation from -40°C to 85°C.

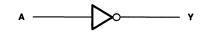
FUNCTION TABLE (each Inverter)

(each inverter)							
INPUT A	OUTPUT Y						
Н	L						
L	н						

logic symbol†

1Y 1A 3 4 2Y 2A 5 6 ЗА **3Y** 9 8 4A 4Y 11 10 5A 5Y 13 12 6A 6Y

logic diagram, each inverter (positive logic)



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TEXAS INSTRUMENTS

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): D package	1.25 W
DB or PW packag	ge 0.5 W
Storage temperature range, T _{stg}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage	ly voltage		3.3	3.6	٧
VIH	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	٧
٧Į	Input voltage		0		Vcc	\ V
Vo	Output voltage		0		VCC	٧
ЮН	High-level output current				-6	mA
loL	Low-level output current				6	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC} ‡	MIN	TYP	MAX	UNIT
VOH	I _{OH} = -100 μA		MIN to MAX	V _{CC} -0.2	2		ν
	I _{OH} = -6 mA		3 V	2.4			V
V	I _{OL} = 100 μA		MIN to MAX			0.2	V
VOL	I _{OL} = 6 mA		3 V			0.4	v
lį	VI = VCC or GND		3.6 V			±1	μА
lcc	V _I = V _{CC} or GND,	lo = 0	3.6 V			20	μА
ΔICC	One input at V _{CC} - 0.6 V,	Other inputs at VCC or GND	3 V to 3.6 V			500	μА
Ci	VI = VCC or GND		3.3 V		2.5		pF

[‡] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



SCLS184A - FEBRUARY 1993 - REVISED JULY 1995

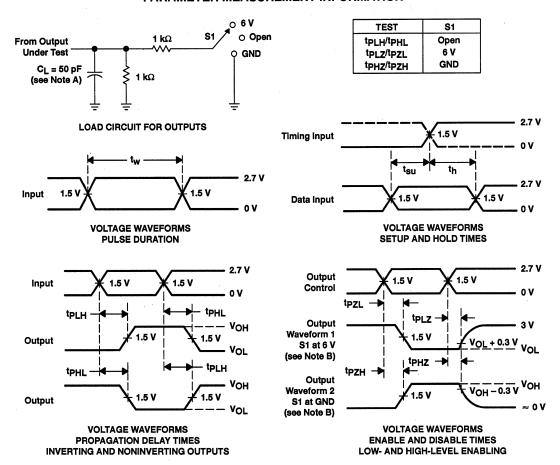
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	V _{CC} =	3.3 V ±	0.3 V	V _{CC} =	2.7 V	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	ONII
t _{pd}	Α	Y		7	15		19	ns

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per inverter	C _L = 50 pF, f = 10 MHz	18	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCLS185A - FEBRUARY 1993 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB,	OR P	W P	ACKAGE
	(TOP	VIEV	N)

	_		-	1		
1A [1	O	14	þ	Vcc	
1Y [2		13		V _{CC}	
2A [3		12		6Y	
2Y [4		11	ן	5A	
3A [5		10	ן	5Y	
3Y [6		9	1	4A	
GND [7		8		4Y	

description

This hex inverter is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVU04 contains six independent inverters with unbuffered outputs. The device performs the Boolean function $Y = \overline{A}$.

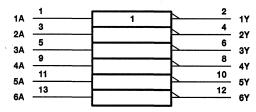
The SN74LVU04 is available in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LVU04 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each inverter)

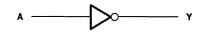
(,									
INPUT	OUTPUT								
Α	Υ								
Н	L								
L	Н								

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each inverter (positive logic)



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TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): D package	1.25 W
	ge 0.5 W
Storage temperature range, T _{stg}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		2.7	3.3	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2.4			٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.5	V ,
٧ı	Input voltage		0		Vcc	٧
VΟ	Output voltage		0		VCC	٧
Юн	High-level output current				-6	mA
loL	Low-level output current				6	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST C	ONDITIONS	v _{cc} ‡	MIN	TYP	MAX	UNIT
Vari	VI = VIL,	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.5			V
VOH	V _I = GND,	IOH = - 6 mA	3 V	2.4			V
Voi	VI = VIH,	I _{OL} = 100 μA	MIN to MAX			0.5	v
V _{OL}	$V_{I} = V_{CC}$	I _{OL} = 6 mA	3 V			0.4	v
l _i	V _I = V _{CC} or GND		3.6 V			±1	μА
lcc	V _I = V _{CC} or GND,	1 ₀ = 0	3.6 V			20	μА
ΔlCC	One input at V _{CC} - 0.6 V,	Other inputs at VCC or GND	3 V to 3.6 V			500	μА
Ci	V _I = V _{CC} or GND		3.3 V		7		pF

For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

SCLS185A - FEBRUARY 1993 - REVISED JULY 1995

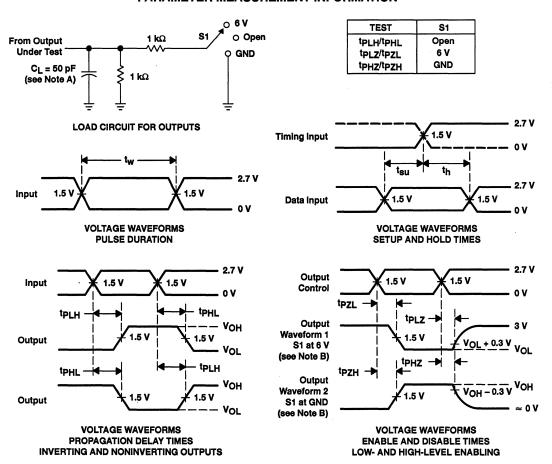
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	V _{CC} = 3.3 V ± 0.3 V			V _{CC} =	UNIT	
FANAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	UNII
^t pd	Α	Y		6	14		18	ns

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
Cpt	d Power dissipation capacitance per inverter	C _L = 50 pF, f = 10 MHz	7	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \Omega$, $t_{r} \leq 2.5$ ns, $t_{f} \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.

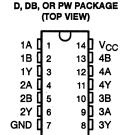
Figure 1. Load Circuit and Voltage Waveforms

SN74LV08 QUADRUPLE 2-INPUT POSITIVE-AND GATE

SCLS186A - FEBRUARY 1993 - REVISED JULY 1995

 EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process

- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages



description

This quadruple 2-input positive-AND gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV08 performs the Boolean functions $Y = A \bullet B$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN74LV08 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV08 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each gate)

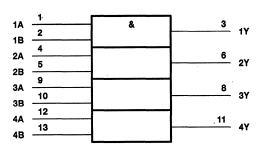
ı	INP	UTS	OUTPUT
1	Α	В	Y
ı	Н	H	Н
İ	L	X	L
ı	Х	L	L

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SCLS186A - FEBRUARY 1993 - REVISED JULY 1995

logic symbol†

logic diagram, each gate (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})	
Output clamp current, IOK (VO < 0 or VO > VCC)	
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): D package	1.25 W
DB or DW packa	ge 0.5 W
Storage temperature range, T _{sto}	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		2.7	3.3	3.6	V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	٧
VI	Input voltage		0		VCC	٧
Vο	Output voltage		0		Vcc	٧
ЮН	High-level output current				-6	mA
loL	Low-level output current				6	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SCLS186A - FEBRUARY 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDIT	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Vou	lOH = -100 μA		MIN to MAX	V _{CC} -0.	2		v
VOH	I _{OH} = – 6 mA		3 V	2.4			V
Vo	l _{OL} = 100 μA		MIN to MAX			0.2	V
VOL	I _{OL} = 6 mA		3 V			0.4	V
lį	V _I = V _{CC} or GND		3.6 V			±1	μА
lcc	V _I = V _{CC} or GND,) = 0	3.6 V			20	μА
ΔlCC	One input at V _{CC} - 0.6 V, O	ther inputs at V _{CC} or GND	3 V to 3.6 V			500	μА
Ci	V _I = V _{CC} or GND		3.3 V		2.5		рF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

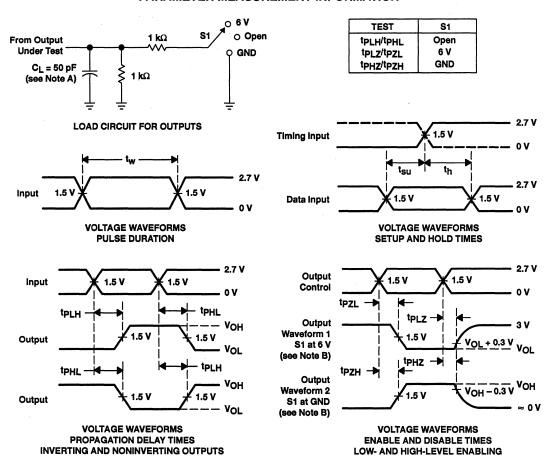
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	V _{CC} =	3.3 V ±	0.3 V	V _{CC} =	2.7 V	UNIT
	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	UNII
^t pd	Α	Y		10	18		23	ns

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CON	TYP	UNIT	
C _{pd}	Power dissipation capacitance per gate	C _L = 50 pF,	f = 10 MHz	24	рF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

HEX SCHMITT-TRIGGER INVERTER

SCLS187A - FEBRUARY 1993 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process
- Typical V_{OLP} (Output Ground Bounce) $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) **Packages**

D,	DB,	OR	PW	PAG	CKA	GE
		(TO	P VI	EW))	

1A [1	U ₁₄	h v
1Y [2	13] V _{CC}] 6A
11 1		13	H OA
2A [3	12	6Y
2Y [4		5A
3A [5	10] 5Y
3Y [6	9] 4A
GND [7	8] 4Y

description

This hex Schmitt-trigger inverter is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV14 contains six independent inverters. The device performs the Boolean function $Y = \overline{A}$.

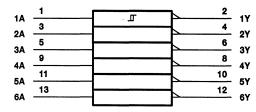
The SN74LV14 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV14 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each inverter)

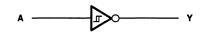
INPUT A	OUTPUT
_ ^	•
н	L
L	Н

logic symbolt



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each inverter (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): D package	1.25 W
DB or PW packag	e 0.5 W
Storage temperature range, T _{stg}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

				NOM	MAX	UNIT
Vcc	CC Supply voltage		2.7	3.3	3.6	٧
٧ _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2.4			٧
۷ _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.4	٧
۷ _I	Input voltage		0		VCC	٧
Vo	Output voltage		0		VCC	٧
ЮН	High-level output current				-6	mA
loL	Low-level output current				6	mA
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

SCLS187A - FEBRUARY 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITION	v _{cc} †	MIN	TYP MAX	UNIT
V _{T+}		2.7 V	1	2	
Positive-going		3 V	1.2	2.2	_ v
threshold		3.6 V	1.5	2.4	
V _T _		2.7 V	0.4	1.4	
Negative-going		3 V	0.6	1.5	7 v
threshold		3.6 V	0.8	1.8	
		2.7 V	0.3	1.	
ΔV _T Hysteresis (V _{T+} – V _{T-})		3 V	0.4	1.2	: V
11ysteresis (V + - V _)		3.6 V	0.4	1.2	· ·
V	IOH = -100 μA	MIN to MAX	VCC-0.2	2	V
VOH	IOH = - 6 mA	3 V	2.4		7 °
VOL	I _{OL} = 100 μA	MIN to MAX		0.2	V
	IOL = 6 mA	3 V		0.4	
lį	VI = VCC or GND	3.6 V		±.	μА
loc	$V_1 = V_{CC}$ or GND, $I_0 = 0$	3.6 V		20	μА
Δlcc	One input at V _{CC} - 0.6 V, Other in	puts at V _{CC} or GND 3 V to 3.6 V		500	μА
Ci	VI = VCC or GND	3.3 V		2.5	pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

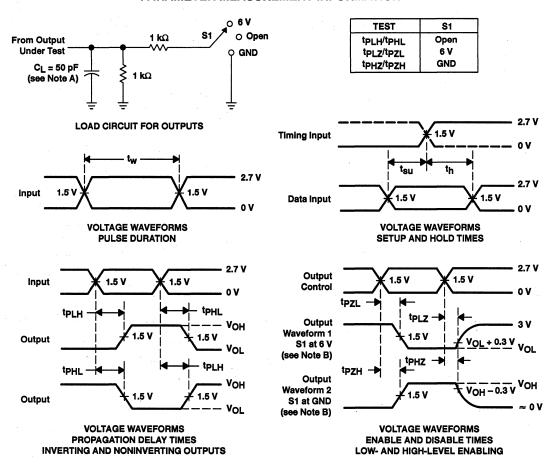
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

	DADAMETED	FROM	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT
•	PARAMETER	(INPUT)		MIN	TYP	MAX	MIN	MAX	ONIT
	^t pd	Α	Y		13	30		36	ns

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CONDITIONS	UNIT		
1	C _{pd} Power dissipation capacitance per inverter	C _L = 50 pF, f = 10 MHz	22	ρF	ı

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq 2.5 \ ns$, $t_f \leq 2.5 \ ns$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN74LV32 QUADRUPLE 2-INPUT POSITIVE-OR GATE

D. DB. OR PW PACKAGE

SCLS188A - FEBRUARY 1993 - REVISED JULY 1995

 EPIC ™ (Enhanced-Performance Implanted CMOS) 2-µ Process

- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

_,,	(TOP VIEW)									
4	$\overline{}$									
1A 🗓	1	14 <u> </u>	VCC							
1B 🛛	2	13	V _{CC} 4B							
1Y 🛛	3	12	4A							
2A 🚺	4	11 🛭	4Y							
2B 🚺	5	10	3B							
2Y 🚺	6	9]	ЗА							
GND I	7	вħ	3Y							

description

This quadruple 2-input positive-OR gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV32 performs the Boolean functions Y = A + B or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

The SN74LV32 is packaged in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV32 is characterized for operation from -40°C to 85°C.

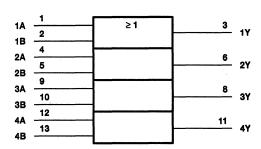
FUNCTION TABLE (each gate)

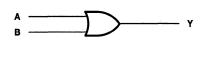
(======									
INP	UTS	OUTPUT							
Α	В	Y							
Н	Х	Н							
Х	н	Н							
L	L	L							

EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†

logic diagram, each gate (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	-0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): D package	
	ge 0.5 W
Storage temperature range, Teta	

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		2.7	3.3	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			٧
V _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	V
۷į	. Input voltage		0		VCC	٧
Vo	Output voltage		0		VCC	V
ЮН	High-level output current				-6	mA
loL	Low-level output current				6	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

SCLS188A - FEBRUARY 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDI	TIONS	vcct	MIN	TYP	MAX	UNIT
V	I _{OH} = -100 μA		MIN to MAX	V _{CC} -0.	2		V
VOH	I _{OH} = -6 mA		3 V	2.4			V
Vai	I _{OL} = 100 μA		MIN to MAX			0.2	ν
VOL	I _{OL} = 6 mA		3 V			0.4	V
lj .	V _I = V _{CC} or GND		3.6 V			±1	μА
lcc	V _I = V _{CC} or GND,	O = 0	3.6 V			20	μА
ΔlCC	One input at V _{CC} - 0.6 V, C	Other inputs at V _{CC} or GND	3 V to 3.6 V			500	μА
Ci	VI = VCC or GND		3.3 V		2.5		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

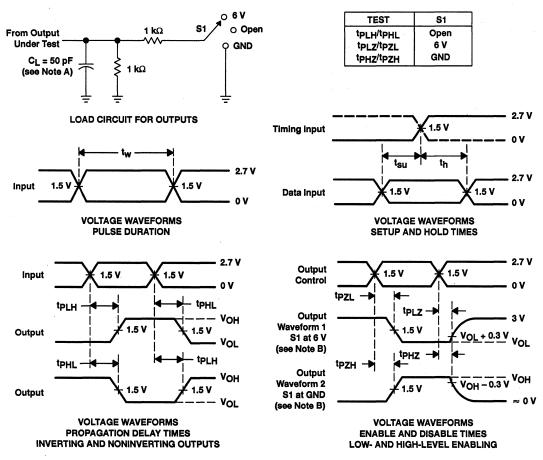
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER		FROM	то	V _{CC} =	3.3 V ±	0.3 V	V _{CC} =	2.7 V	UNIT
	PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	ONIT
	^t pd	A	Y		8	17		22	ns

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER Parameter param		TEST CONDITIONS		
C _{pd}	Power dissipation capacitance per gate	C _L = 50 pF,	f = 10 MHz	23	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_f ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

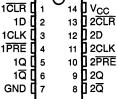
Figure 1. Load Circuit and Voltage Waveforms

SN74LV74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCLS189A - FEBRUARY 1993 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB, OR PW PACKAGE (TOP VIEW) CLR 1 14 V_{CC} 1D 2 13 2CLF



description

This dual positive-edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

The SN74LV74 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV74 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

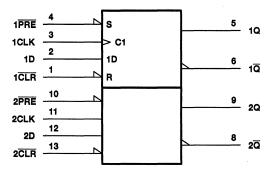
	INP	OUT	PUTS		
PRE	CLR	CLK	D	Q	Q
L	Н	Х	Х	Н	L
Н	L	X	Х	L	Н
L	L	X	Х	н†	нt
Н	н	1	Н	Н	L
Н	Н	1	L	L	Н
Н	Н	L	Х	Q ₀	₫0

[†] This configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

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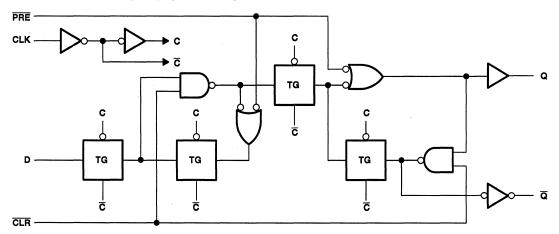
SCLS189A - FEBRUARY 1993 - REVISED JULY 1995

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each flip-flop (positive logic)



SN74LV74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCLS189A - FEBRUARY 1993 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

	· ·
Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note	3): D package 1.25 W
•	DB or PW package 0.5 W
Storage temperature range, T _{sto}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book. literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2.7	3.3	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	٧
VI	Input voltage	4.	0		Vcc	٧
Vo	Output voltage		0		Vcc	٧
ЮН	High-level output current				-6	mA
loL	Low-level output current				6	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
·ΤΑ	Operating free-air temperature		-40		85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITION	s v _{cc}	; ‡	MIN	TYP	MAX	UNIT
Vou	IOH = -100 μA	MIN to	MAX	V _{CC} -0.2	2		V
Voн	I _{OH} = -6 mA	3	٧	2.4			V
Voi	l _{OL} = 100 μA	MIN to	MAX			0.2	٧
VOL	I _{OL} = 6 mA	3	٧			0.4	V
lı	V _I = V _{CC} or GND	3.6	٧			±1	μА
lcc	$V_1 = V_{CC}$ or GND, $I_0 = 0$	3.6	٧			20	μА
ΔICC	One input at V _{CC} - 0.6 V, Other	inputs at V _{CC} or GND 3 V to 3	3.6 V			500	μА
Ci	VI = VCC or GND	3.3	٧		2.5		pF

[‡] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



SN74LV74 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCLS189A - FEBRUARY 1993 - REVISED JULY 1995

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V _{CC} =	3.3 V 3 V	V _{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	24	0	19	MHz
	Dulas duration	PRE or CLR low	20		25		
t _w	Pulse duration	CLK high or low	20		25		ns
	Out on the contract to the form OUT	Data	13		16		
tsu	Setup time, data before CLKT		8		10		ns
th	Hold time, data after CLK↑		3		3		ns

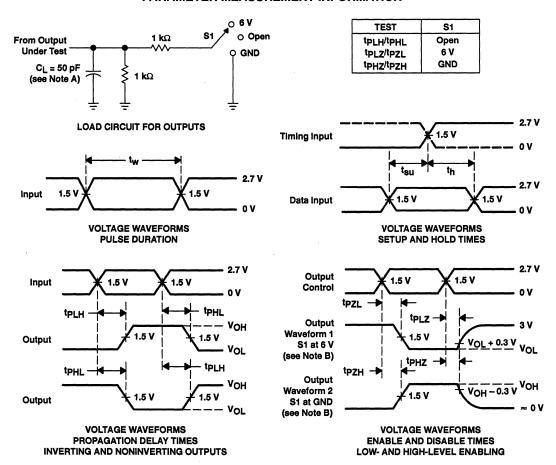
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	V _{CC} =	3.3 V ±	0.3 V	V _{CC} =	2.7 V	UNIT	
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	ONIT	
f _{max}			24	100		19		MHz	
	PRE or CLR	QorQ		16	34		43	ns	
^t pd	CLK	- Qorq		15	28		35	115	

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CO	TEST CONDITIONS			
C _{pd}	Power dissipation capacitance per flip-flop	C _L = 50 pF,	f = 10 MHz	32	pF	

PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

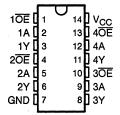
Figure 1. Load Circuit and Voltage Waveforms

SN74LV125 **QUADRUPLE BUS BUFFER GATE** WITH 3-STATE OUTPUTS

SCES003A - NOVEMBER 1994 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) **Packages**

D, DB, OR PW PACKAGE (TOP VIEW)



description

This quadruple bus buffer gate is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV125 features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is high.

The SN74LV125 is characterized for operation from -40°C to 85°C.

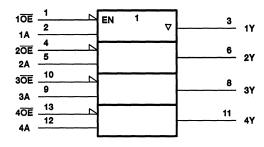
FUNCTION TABLE (each buffer)

INPL	JTS	OUTPUT
ŌĒ	Α	Y
L	Н	Н
L	L	L
Н	Х	Z

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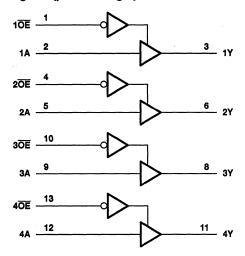
SCES003A - NOVEMBER 1994 - REVISED JULY 1995

logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})	±20 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	
Continuous output current, I _O (V _O = 0 to V _{CC})	±35 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): D package	
DB or PW package	0.5 W
Operating free-air temperature range, T _A	
Storage temperature range, T _{stq}	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

SCES003A - NOVEMBER 1994 - REVISED JULY 1995

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2.7	3.3	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	٧
VI	Input voltage		0		VCC	V
Vo	Output voltage		0		VCC	٧
ЮН	High-level output current				-8	mA
lOL	Low-level output current				8	mA
Δt/ΔV	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CO	NDITIONS	Vcc	MIN	TYPT	MAX	UNIT
VOH	I _{OH} = -100 μA		MIN to MAX‡	V _{CC} -0.2	2		ν
V ОН	iOH = -8 mA		3 V	2.4			V
Vai	IOL = 100 μA		MIN to MAX‡			0.2	V
VOL	IOL = 8 mA		3 V			0.4	V
11	VI = VCC or GND		3.6 V			±1	μА
loz	VO = VCC or GND		3.6 V			±5	μА
lcc	$V_I = V_{CC}$ or GND,	IO = 0	3.6 V			20	μА
ΔlCC	One input at V _{CC} - 0.6 V,	Other inputs at VCC or GND	3 V to 3.6 V			500	μА
Ci	V _I = V _{CC} or GND		3.3 V		3.5		pF
Co	VO = VCC or GND		3.3 V		8		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	VC	c = 3.3 ± 0.3 V	V	V _{CC} =	2.7 V	UNIT
L		(INPOT)	(001701)	MIN	TYPT	MAX	MIN	MAX	ns
	^t pd	A	Y		10	21		26	ns
	^t en	ŌĒ	Υ		11	29		36	ns
Γ	^t dis	ŌĒ	Y		10	26		32	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

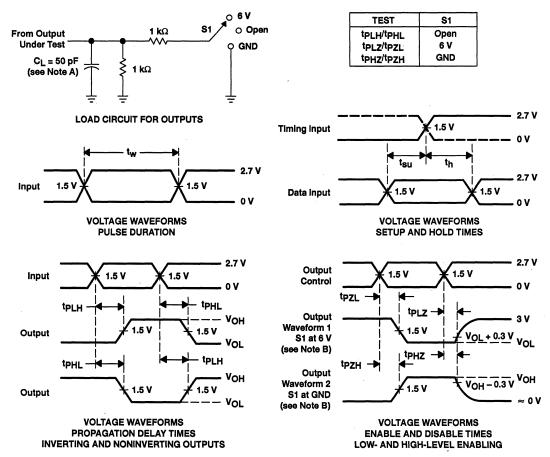
operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER			NDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	Outputs enabled	C: 50 pE	f = 10 MHz	45	pF
	rower dissipation capacitance	Outputs disabled	$C_L = 50 \text{ pF},$	1 = 10 MINZ	5	PΓ

[‡] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

SCES003A - NOVEMBER 1994 - REVISED JULY 1995

PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_f \leq 2.5 \ ns$, $t_f \leq 2.5 \ ns$.

D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

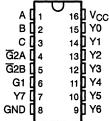


SN74LV138 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

SCLS190A - FEBRUARY 1993 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

D, DB,	OR	PW	PAC	KAGE
	ση	P VI	EW)	



description

This 3-line to 8-line decoder/demultiplexer is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV138 is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The SN74LV138 is available in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV138 is characterized for operation from -40°C to 85°C.

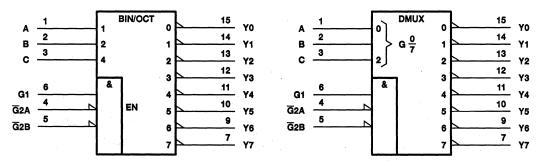
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SCLS190A - FEBRUARY 1993 - REVISED JULY 1995

FI	IN	CT	101	N T	ГΔ	RI	F

ENA	BLE INF	PUTS	SEL	ECT INF	UTS				OUT	PUTS			
G1	G2A	G2B	С	В	Α	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
Х	Н	Х	Х	Х	Х	Н	Н	Н	н	Н	Н	Н	Н
X	X	Н	Х	· X	X	н	Н	Н	н	Н	Н	H	Н
L	X	X	Х	X	Χ	Н	Н	Н	Н	H	Н	н	н
н	L	L	L	L	L	L	Н	Н	н	Н	Н	H 1	Ĥ
Н	L	L	L	L	Н	Н	L	н	Н	Н	Н	Н	Н
Н	L	L	L	Н	L	н	Н	L	Н	Н	Н	Н	Н
Н	L	L	L	Н	Н	н	Н	н	L	Н	Н	н	Н
Н	L	L	Н	L	L	Н	Н	н	Н	L	Н	Н	Н
н	L	L	Н	L	Н	Н	Н	н	Н	Н	L	Н	Н
Н	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н
н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L

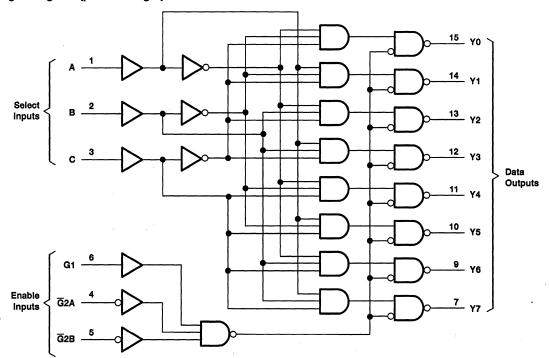
logic symbols (alternatives)†



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SCLS190A - FEBRUARY 1993 - REVISED JULY 1995

logic diagram (positive logic)



SCLS190A - FEBRUARY 1993 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}			
Input voltage range, V _I (see Note 1)		-0.5 V to V _{CC}	+ 0.5 V
Output voltage range, VO (see Notes 1 and 2)		-0.5 V to V _{CC}	+ 0.5 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})			
Output clamp current, IOK (VO < 0 or VO > VCC)			±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})			±25 mA
Continuous current through V _{CC} or GND			±50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3):	D package		1.3 W
	DB package		0.55 W
	PW package		0.5 W
Storage temperature range, T _{stg}		65°C to	o 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		2.7	3.3	3.6	٧
VIH	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			V
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	٧
VI	Input voltage		0		VCC	٧
Vo	Output voltage		0		Vcc	٧
ЮН	High-level output current				-6	mA
loL	Low-level output current				6	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST COND	ITIONS	v _{cc} ‡	MIN	TYP	MAX	UNIT
Vau	I _{OH} = -100 μA		MIN to MAX	V _{CC} -0.2	2		V
VOH	I _{OH} = -6 mA		3 V	2.4			V
Vo	l _{OL} = 100 μA		MIN to MAX			0.2	V
VOL	IOL = 6 mA		3 V			0.4	v
lţ .	V _I = V _{CC} or GND		3.6 V			±1	μА
lcc	$V_I = V_{CC}$ or GND,	0=0	3.6 V			20	μА
ΔICC	One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			500	μА
Ci	V _I = V _{CC} or GND		3.3 V		2.5		pF

For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



SN74LV138 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

SCLS190A - FEBRUARY 1993 - REVISED JULY 1995

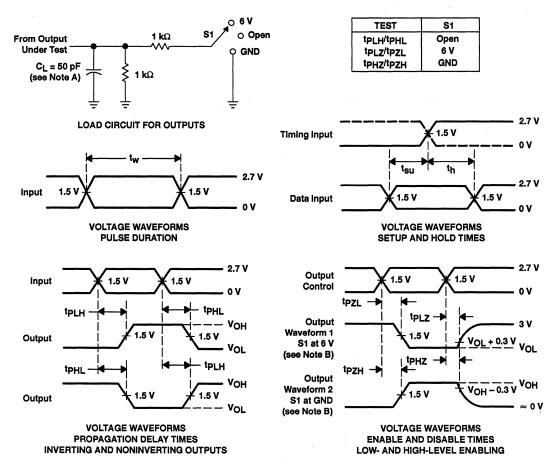
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	V _{CC} =	3.3 V ±	0.3 V	V _{CC} =	2.7 V	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	UNII
	A, B, or C	_		14	29		36	ns
^t pd	Enable	,		16	33		41	115

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER		TEST CONDITIONS		
C _{pd}	Power dissipation capacitance per channel	C _L = 50 pF,	f = 10 MHz	47	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

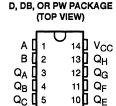
SCLS191A - FEBRUARY 1993 - REVISED JULY 1995

10 QE

9 CLR

8∏ CLK

- EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) **Packages**



 $Q_D [] 6$

GND 17

description

This 8-bit parallel-out serial shift register is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV164 features AND-gated serial (A and B) inputs and an asynchronous clear (CLR) input. The gated serial inputs permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock (CLK) input.

The SN74LV164 is available in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV164 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

	INPL	JTS	(OUTPUT	S	
CLR	CLK	Α	В	QA	QB.	QH
L	Х	Х	Х	L	L	L
Н	L	Х	X	Q _{A0}	Q _{B0}	Q _{H0}
Н	1	Н	Н	Н	Q_{An}	QGn
н	1	L	X	L	Q_{An}	Q_{Gn}
Н	1	Х	L	L	Q_{An}	Q_{Gn}

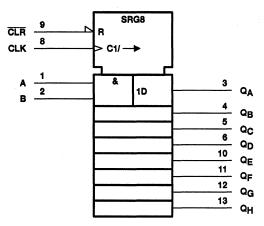
 Q_{A0} , Q_{B0} , Q_{H0} = the level of Q_{A} , Q_{B} , or Q_{H} , respectively, before the indicated steady-state inputs conditions were established

QAn, QGn = the level of QA or QG before the most recent T transition of the clock: indicates a 1-bit shift

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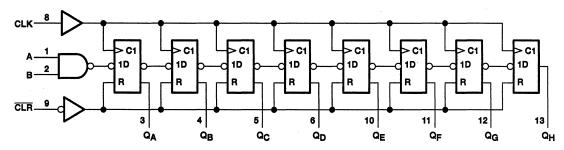
SCLS191A - FEBRUARY 1993 - REVISED JULY 1995

logic symbol†

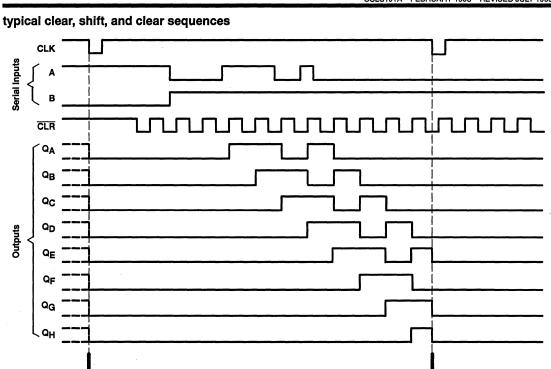


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Clear



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} 0.5 V	to 4.6 V
Input voltage range, V _I (see Note 1)	+ 0.5 V
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, $I_{ K }(V_1 < 0 \text{ or } V_1 > V_{CC})$	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): D package	
DB or PW package	0.5 W
Storage temperature range, T _{stq} 65°C to	150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - This value is limited to 4.6 V maximum.

Clear

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.



SN74LV164 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

SCLS191A - FEBRUARY 1993 - REVISED JULY 1995

recommended operating conditions (see Note 4)

		1.50	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2.7	3.3	3.6	V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			8.0	٧
Vı	Input voltage		0		VCC	V
.Vo	Output voltage		0		VÇC	٧
ЮН	High-level output current				-6	mA
loL	Low-level output current				6	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	့

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} t	MIN	TYP MAX	UNIT
Vou	l _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		V
VOH	I _{OH} = -6 mA	3 V	2.4] <u> </u>
Vol	i _{OL} = 100 μA	MIN to MAX		0.2	2 v
VOL	IOL = 6 mA			0.4	
lį	V _I = V _{CC} or GND	3.6 V		±.	μA
loc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20) μΑ
ΔlCC	One input at V _{CC} - 0.6 V, Other inputs at V _C	C or GND 3 V to 3.6 V		500) μΑ
Ci	V _I = V _{CC} or GND	3.3 V		2.5	ρF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX		
fclock	Clock frequency		0	24	0	, 19	MHz	
	Pulse duration	CLR low	20		25			
t _w	ruise duration	CLK high or low	20		25		ns	
	Catura time a data hafana OLICA	Data	13		16			
t _{su} Set	Setup time, data before CLK1	CLR inactive			14		ns	
th	Hold time, data after CLK↑		5		5		ns	

SN74LV164 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

SCLS191A - FEBRUARY 1993 - REVISED JULY 1995

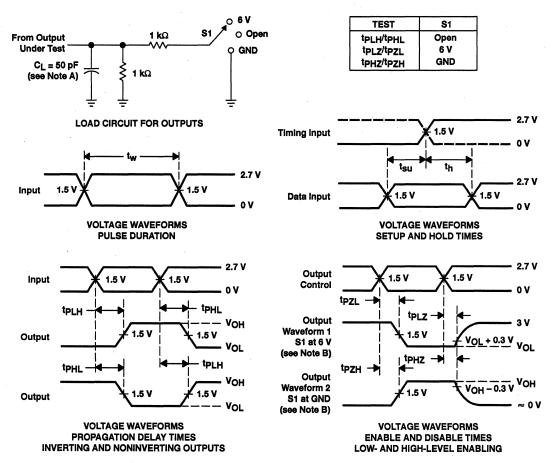
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	V _{CC} =	3.3 V ±	0.3 V	V _{CC} =	2.7 V	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	UNIT
fmax			24	75		19		MHz
^t pd	CLK	Q		16	29		36	ns
^t PHL	CLR	Q		16	29		36	ns

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	C _L = 50 pF, f = 10 MHz	74	pF

PARAMETER MEASUREMENT INFORMATION

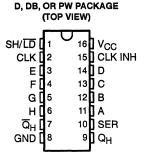


NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17



description

The SN74LV165 is a parallel-load, 8-bit shift register designed for 2.7-V to 3.6-V V_{CC} operation.

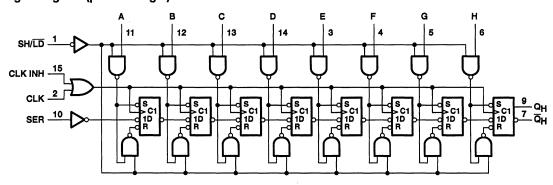
When the device is clocked, data is shifted toward the serial output Q_H . Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the SH/ \overline{LD} input. The SN74LV165 features a clock inhibit function and a complemented serial output \overline{Q}_H .

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while SH/\overline{LD} is held high and clock inhibit (CLK INH) is held low. The functions of the CLK and CLK INH inputs are interchangeable. Since a low CLK input and a low-to-high transition of CLK INH accomplishes clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when SH/\overline{LD} is held high. The parallel inputs to the register are enabled while SH/\overline{LD} is held low independently of the levels of CLK, CLK INH, or SER.

FUNCTION TABLE

	INPUTS		OPERATION
SH/LD	CLK	CLK INH	OPERATION
L	Х	Х	Parallel load
Н	Н	X	Q ₀
Н	X	Н	Q ₀
Н	L	1	Shift
Н	1	L	Shift

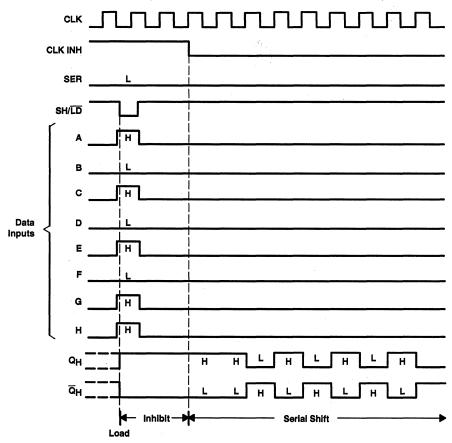
logic diagram (positive logic)



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TEXAS INSTRUMENTS

typical shift, load, and inhibit sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} Input voltage range, V_I (see Note 1)): DB package D package PW package	-0.5 V to V _C .	C + 0.5 V C + 0.5 V $\pm 20 \text{ mA}$ $\pm 50 \text{ mA}$ $\pm 25 \text{ mA}$ $\pm 50 \text{ mA}$ $\cdot 0.55 W$ $\cdot 1.30 W$ $\cdot 0.5 W$
Storage temperature range, T _{stg}		−65°C	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		2.7	3.3	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	٧
٧١	Input voltage		0		VCC	٧
٧o	Output voltage		0		VCC	٧
ЮН	High-level output current				-6	mA
lOL	Low-level output current				6	mA .
Δt/Δν	Input transition rise or fall rate	,	0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc‡}	MIN	TYP	MAX	UNIT
Vari	IOH = -100 μA	MIN to MAX	V _{CC} -0.2			V
VOH	I _{OH} = -6 mA	3 V	. 2.4			٧
Voi	I _{OL} = 100 μA	MIN to MAX			0.2	V
VOL	I _{OL} = 6 mA	3 V			0.4	V
lį	V _I = V _{CC} or GND	3.6 V			±1	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			20	μА
ΔlCC	One input at V _{CC} - 0.6 V, Other inpu	s at V _{CC} or GND 3 V to 3.6 V			500	μА
Ci	VI = VCC or GND	3.3 V		2.5		pF

For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.



timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V _{CC} =		V _{CC} =	2.7 V	UNIT
		•	MIN	MAX	MIN	MAX	
fclock	Clock frequency		. 0	24	0	19	MHz
	Pulse duration CLK high or low SH/LD low	CLK high or low	20		25		
t _w		20		25		ns	
		SH/LD high before CLK↑	15		19		
	Oakus thus	SER before CLK↑	13		16		
^t su	Setup time	CLK INH before CLK↑ 13 16	16		ns		
		Data before SH/LD↑	15		19		
4.	Hold time	SER data after CLK↑	8		8		T
th	noid time	Parallel data after SH/LD↑	8		8	ns	

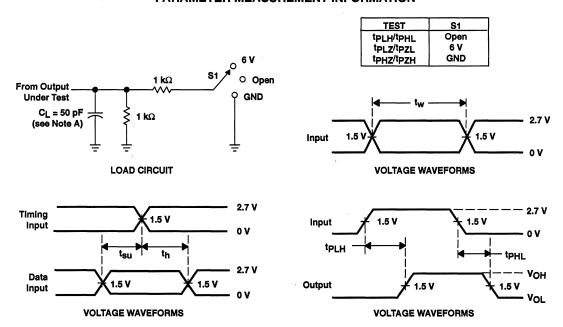
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO	Vcc =	3.3 V ±	0.3 V	V _{CC} =	2.7 V	UNIT
PARAMETER	(INPUT)		MIN	TYP	MAX	MIN	MAX	UNII
f _{max}			24	75		19		MHz
	CLK			20	44		55	
t _{pd}	SH/LD	Q _H or $\overline{\mathbf{Q}}_{H}$		19	41		51	ns
	Н			15	34		43	

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CON	TYP	UNIT	
C _{pd} Power dissipation capacitance		C _L = 50 pF,	f = 10 MHz	33	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. The outputs are measured one at a time with one transition per measurement.

C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2.5 \text{ ns.}$ $t_f \leq 2.5 \text{ ns.}$

Figure 1. Load Circuit and Voltage Waveforms

HEX D-TYPE FLIP-FLOP WITH CLEAR

SCLS192A - FEBRUARY 1993 - REVISED JULY

- EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process
- Typical V_{OLP} (Output Ground Bounce) $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) **Packages**

D,	DB,	OR	PW	PAC	KAGE
		ſΤΟ	P VI	EW)	

		TT	1	
CLR [16	þ	Vcc
1Q [2	15	þ	6Q
1D [3	14	0	6D
2D [13	þ	5D
2Q [12	þ	5Q
3D [11	þ	4D
3Q [10		4Q
GND [8	9	D	CLK

description

This hex D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV174 is a monolithic positive-edge-triggered flip-flop with a direct clear (CLR) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of the clock pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

The SN74LV174 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

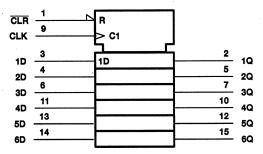
The SN74LV174 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

	INPUTS	OUTPUT	
CLR	CLK	D	Q
L	Х	Х	L
Н	1	Н	н
н	1	L	L
Н	L	Х	Q ₀

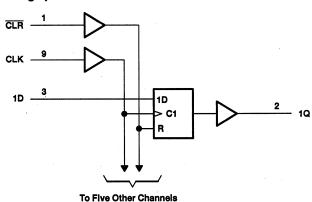
EPIC is a trademark of Texas Instruments Incorporated

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	
Continuous output current, I _O (V _O = 0 to V _{CC})	
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): D package	1.3 W
DB package	0.55 W
PW package	0.5 W
Storage temperature range, T _{sto}	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - This value is limited to 4.6 V maximum.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.



recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage	·	2.7	3.3	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	V
٧ _I	Input voltage		0		Vcc	٧
٧o	Output voltage		0		Vcc	٧
ЮН	High-level output current				-6	mA
loL	Low-level output current				6	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		v _{cc} †	MIN	TYP	MAX	UNIT	
· Va	I _{OH} = -100 μA		MIN to MAX	V _{CC} -0.	2		V	
VOH	I _{OH} = - 6 mA		3 V	2.4			V	
· Vo.	I _{OL} = 100 μA		MIN to MAX			0.2	v	
VOL	i _{OL} = 6 mA		3 V			0.4	V	
Ŋ	VI = VCC or GND		3.6 V			±1	μА	
loc	VI = VCC or GND,	I _O = 0	3.6 V			20	μА	
ΔlCC	One input at V _{CC} – 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			500	μА	
Ci	V _I = V _{CC} or GND		3.3 V		2.5		pF	

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
			MIN MAX	MIN	MAX		
fclock	Clock frequency			24	0	19	MHz
	Pulse duration	CLR low	20		25		ns
t _w		CLK high or low	20		25		
t _{su}	Setup time before CLK↑	Data	13		16		ns
		CLR inactive	5		5		
th	Hold time, data after CLK↑		5		5		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Vcc =	V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V	
TANAMETER			MIN	TYP	MAX	MIN	MAX	UNIT
fmax			24	80		19		MHz
+	CLR	Q		12	26		33	ns
^t pd	CLK			13	33		41	



operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CON	NDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per flip-flop	C _L = 50 pF,	f = 10 MHz	24	pF

PARAMETER MEASUREMENT INFORMATION O 6 V TEST S1 S1 O Open 1 kΩ From Output tPLH/tPHL Open **Under Test** O GND 6 V tPLZ/tPZL GND tPHZ/tPZH $C_L = 50 pF$ 1 kΩ (see Note A) 2.7 V LOAD CIRCUIT FOR OUTPUTS 1.5 V **Timing Input** tsu 2.7 V 2.7 V Input 1.5 1.5 V 1.5 V 1.5 V **Data Input** 0 V 0 V **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS PULSE DURATION** SETUP AND HOLD TIMES 2.7 V 2.7 V Output 1.5 V Input 1.5 V 1.5 V Control 0 V tpzL **tPHL tPLH tPLZ** Output VOH Waveform 1 1.5 V Output S1 at 6 V VOL (see Note B) tPHZ **tPLH** tPHL -^tPZH Output Vон V_{OH} - 0.3 V Waveform 2 1.5 V 1.5 V Output S1 at GND VOL (see Note B) **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS** PROPAGATION DELAY TIMES **ENABLE AND DISABLE TIMES INVERTING AND NONINVERTING OUTPUTS** LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns. $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



SCLS193A - FEBRUARY 1993 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) **Packages**

DB, DW, OR PW PACKAGE (TOP VIEW)

		TT		
10E [O	20	l v _{cc}
1A1 [20E
2Y4 [] 1Y1
1A2 [2A4
2Y3 [1Y2
1A3 [2A3
2Y2 [] 1Y3
1A4 [13	2A2
2Y1 [9		12	1Y4
GND [10		11	2A1

description

This octal buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV240 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN74LV240 is organized as two 4-bit buffers/line drivers with separate output-enable (OE) inputs. When OE is low, the device passes data from the A inputs to the Y outputs. When OE is high, the outputs are in the high-impedance state.

The SN74LV240 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

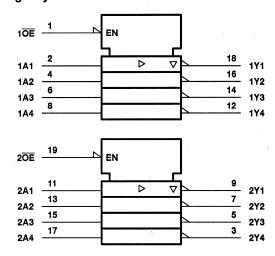
The SN74LV240 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each buffer)

INP	JTS	OUTPUT
ŌĒ	Α	Y
L	Н	L
L	L	н
н	Х	z

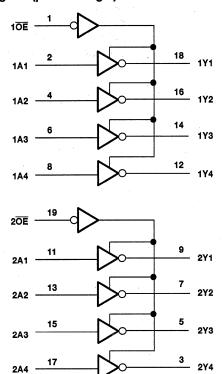
EPIC is a trademark of Texas Instruments Incorporated

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V _{CC} or GND	±70 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB pa	ckage 0.6 W
DW pa	ackage 1.6 W
	ackage 0.7 W
Storage temperature range, T _{sto}	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.



recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2.7	3.3	3.6	V
VIH	High-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2			٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	٧
٧ı	Input voltage		0		VCC	V
Vο	Output voltage		0		VCC	٧
ЮН	High-level output current				-8	mA
lOL	Low-level output current				8	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	•C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		v _{cc} †	MIN	TYP	MAX	UNIT
Vou	I _{OH} = -100 μA		MIN to MAX	V _{CC} -0.2			V
VOH	I _{OH} = -8 mA		3 V	2.4			V
Voi	I _{OL} = 100 μA		MIN to MAX			0.2	V
V _{OL}	IOL = 8 mA		3 V			0.4	V
lį	VI = VCC or GND		3.6 V			±1	μА
loz	VO = VCC or GND		3.6 V			±5	μА
loc	V _I = V _{CC} or GND,	IO = 0	3.6 V			20	μА
Δlcc	One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			500	μА
Ci	V _I = V _{CC} or GND		3.3 V		3		pF
C _o	VO = VCC or GND		3.3 V		8		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

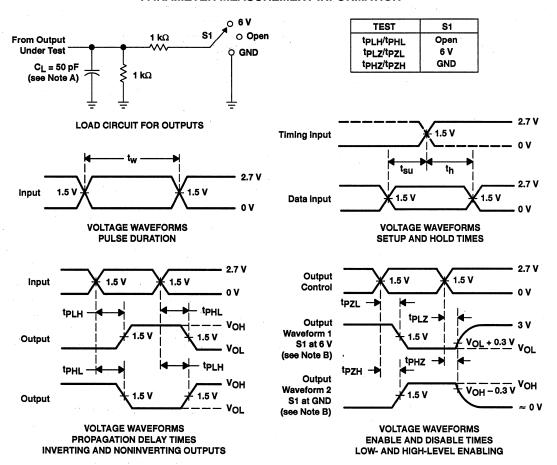
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	V _{CC} =	3.3 V ±	0.3 V	V _{CC} =	2.7 V	UNIT
PANAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	UNII
t _{pd}	A	Υ		10	21		26	ns
t _{en}	ŌĒ	Υ		15	28		35	ns
^t dis	ŌĒ	Y		17	27		33	ns

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

	PARAMETER		TEST CO	TYP	UNIT	
C .	Power dissipation capacitance per buffer/driver	Outputs enabled	C: 50 pF	f = 10 MHz	45	ρF
Cpd		Outputs disabled	C _L = 50 pF,	I = IU MICZ	2.5	рг

PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN74LV244 OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCLS194A - FEBRUARY 1993 - REVISED JULY 1995

•	EPIC ™ (Enhanced-Performance	Implanted
	CMOS) 2-μ Process	

- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE (TOP VIEW)

10E [1	O 20	vcc
1A1 [2	19] 20E
2Y4 [3] 1Y1
1A2 [4] 2A4
2Y3 [5] 1Y2
1A3 [6	15] 2A3
2Y2 [7] 1Y3
1A4 [8	13] 2A2
2Y1 [9	12] 1Y4
GND [10	11	2A1

description

This octal buffer/line driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV244 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN74LV244 is organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

The SN74LV244 is available in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV244 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each buffer)

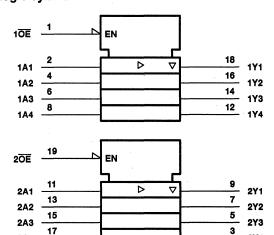
	•	
INP	JTS	OUTPUT
ŌĒ	Α	Y
L	Н	Н
L	L	L
Н	Χ	z

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SCLS194A - FEBRUARY 1993 - REVISED JULY 1995

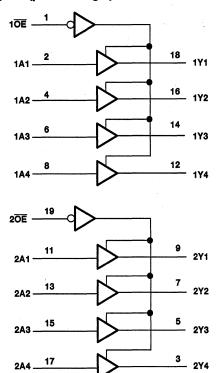
logic symbol†

2A4



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

2Y4

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	
Continuous output current, I _O (V _O = 0 to V _{CC})	±35 mA
Continuous current through V _{CC} or GND	±70 mA
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): DB package	0.6 W
DW package	1.6 W
PW package	0.7 W
Storage temperature range, T _{sto}	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

^{2.} This value is limited to 4.6 V maximum.

SCLS194A - FEBRUARY 1993 - REVISED JULY 1995

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2.7	3.3	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			٧
V _{IL}	Low-level input voltage	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$			0.8	٧
VI	Input voltage		0		VCC	٧
Vo	Output voltage		0		VCC	V
ЮН	High-level output current				-8	mA
lOL	Low-level output current				8	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} †	MIN	TYP	MAX	UNIT
Vari	$I_{OH} = -100 \mu\text{A}$ MII		V _{CC} -0.2			V
VOH	I _{OH} = -8 mA	3 V	2.4			٧
Va	l _{OL} = 100 μA	MIN to MAX			0.2	V
VOL	IOL = 8 mA	3 V			0.4	V
l ₁	V _I = V _{CC} or GND	3.6 V			±1	μА
loz	VO = VCC or GND	3.6 V			±5	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			20	μА
Δlcc	One input at V _{CC} - 0.6 V, Other inputs at	V _{CC} or GND 3 V to 3.6 V			500	μА
Ci	V _I = V _{CC} or GND	3.3 V		3		pF
Co	V _O = V _{CC} or GND	3.3 V		8		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

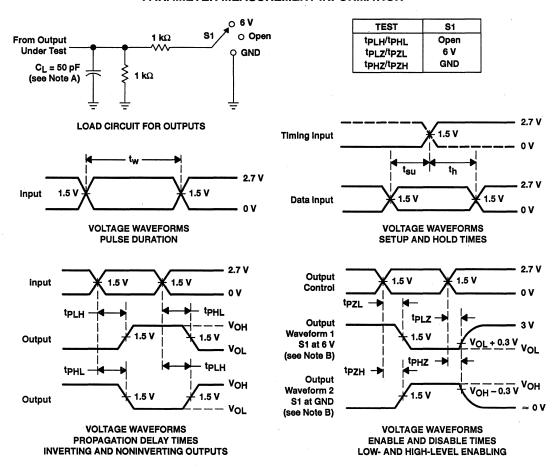
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	V _{CC} =	3.3 V ±	0.3 V	V _{CC} =	2.7 V	UNIT
PANAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	ONIT
^t pd	Α	Y		10	19		24	ns
t _{en}	ŌĒ	Υ		14	26		33	ns
^t dis	ŌĒ	Y		15	26		32	ns

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER			TEST CO	TYP	UNIT	
	Power dissipation capacitance per buffer/driver	Outputs enabled	C: 50 %	f = 10 MHz	40	-F
Opd	rower dissipation capacitance per buller/driver	Outputs disabled	$C_L = 50 pF$,	I = IO MINZ	4	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \Omega$, $t_{r} \leq$ 2.5 ns, $t_{t} \leq$ 2.5 ns,
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCLS075C - JANUARY 1991 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process
- Typical V_{OLP} (Output Ground Bounce) $< 0.8 \text{ V at V}_{CC} = 3.3 \text{ V}, T_A = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) $> 2 \text{ V at V}_{CC} = 3.3 \text{ V, T}_{A} = 25^{\circ}\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) **Packages**

DB, DW, OR PW PACKAGE (TOP VIEW)

		TT		
DIR [1	O	20	v_{cc}
A1 [2		19] Œ
A2 [3		18	B1
АЗ [4		17] B2
A4 [5		16] B3
A5 [6		15] B4
A6 [7		14	B5
A7 🛛	8		13] B6
A8 [9		12	B7
GND [10		11] B8

description

This octal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

The SN74LV245 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV245 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

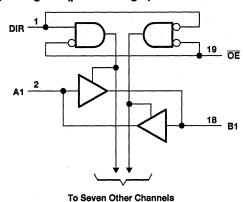
INP	UTS	OPERATION
ŌĒ	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	Χ	Isolation

EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†

3EN1[BA] 3EN2[AB] 18 2∇ 17 **B2** 16 **B**3 15 В4 Α4 14 A5 В5 13 **A6 B6** 12 В7 **A7** 11 В8

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} –0.5 V to 4.6 V
Input voltage range, V _I : Except I/O ports (see Note 1)
I/O ports (see Notes 1 and 2)
Output voltage range, V _O (see Notes 1 and 2)
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ± 50 mA
Continuous output current, I _O (V _O = 0 to V _{CC}) ±35 mA
Continuous current through V _{CC} or GND
Maximum power dissipation at TA = 55°C (in still air) (see Note 3): DB package
DW package 1.6 W
PW package 0.7 W
Storage temperature range, T _{sta} –65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		2.7	3.3	3.6	V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			V
٧ _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	V
Vį	Input voltage		0		Vcc	V
Vo	Output voltage		0		VCC	٧
ЮН	High-level output current				-8	mA
loL	Low-level output current				8	mA
Δt/Δν	Input transition rise or fall rate		0		50	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CO	ONDITIONS	vcct	MIN	TYP	MAX	UNIT
V		I _{OH} = -100 μA		MIN to MAX	V _{CC} -0.	2		V
VOH		I _{OH} = -8 mA		3 V	2.4			V
Voi		I _{OL} = 100 μA		MIN to MAX			0.2	V
VOL		I _{OL} = 8 mA		3 V			0.4	٧
Ц		V _I = V _{CC} or GND		3.6 V			±1	μА
loz‡		VO = VCC or GND		3.6 V			±5	μА
Icc		V _I = V _{CC} or GND,	I _O = 0	3.6 V			20	μА
ΔICC		One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			500	μА
Ci	Control inputs	V _I = V _{CC} or GND		3.3 V		2.5		рF
C _{io}	A or B ports	VO = VCC or GND		3.3 V		7		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

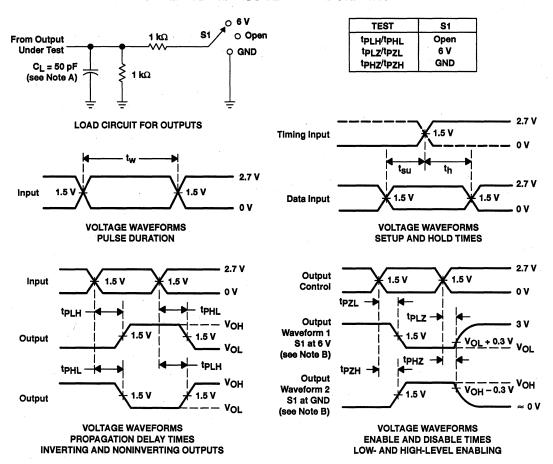
PARAMETER	FROM	то	V _{CC} =	3.3 V ±	0.3 V	V _{CC} =	2.7 V	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	UNIT
^t pd	A or B	B or A		8	16		20	ns
t _{en}	ŌĒ	A or B		13	23		29	ns
^t dis	ŌĒ	A or B		14	25		31	ns

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CO	TYP	UNIT		
C .	Power dissipation capacitance per transceiver	Outputs enabled	C: E0 aE	f = 10 MHz	36	ρF
Cbq	rower dissipation capacitance per transceiver	Outputs disabled	C _L = 50 pF,	1 = 10 MIN2	4	рг

[‡] For I/O ports, the parameter IOZ includes the input leakage current.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SCLS195A - FEBRUARY 1993 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE (TOP VIEW)

CLR [\int_{1}	\bigcup_{20}	v _{cc}
1Q [2	19] 8Q
1D [18	[] 8D
2D [4	17	7D
2Q [16] 7Q
3Q [6] 6Q
3D [7	14] 6D
4D [] 5D
4Q [] 9	12] 5Q
GND [10	11] CLK

description

This octal D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV273 is a positive-edge-triggered flip-flop with a direct clear (CLR) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

The SN74LV273 is available in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

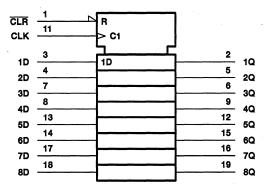
The SN74LV273 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each flip-flop)

	(1-7
	INPUTS	OUTPUT	
CLR	CLK	D	Q
L	X	Х	L
Н	1	Н	н
Н	1	L	L
Н	L	Χ	Q ₀

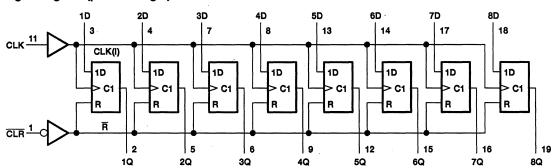
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB package	0.6 W
DW package	1.6 W
PW package	0.7 W
Storage temperature range, T _{sto}	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.



recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		2.7	3.3	3.6	٧
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	٧
VI	Input voltage	_	0		Vcc	٧
Vo	Output voltage		0		Vcc	٧
ЮН	High-level output current				-6	mA
lOL	Low-level output current	·			6	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITION	v _{cc} t	MIN	TYP	MAX	UNIT	
Vou	lOH = -100 μA		MIN to MAX	V _{CC} -0.2	?		٧
Voн	I _{OH} = -6 mA	3 V	2.4			V	
Voi	l _{OL} = 100 μA	MIN to MAX			0.2	V	
VOL	IOL = 6 mA	3 V			0.4	V	
l _l	V _I = V _{CC} or GND		3.6 V			±1	μА
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$		3.6 V			20	μА
ΔlCC	One input at V _{CC} - 0.6 V, Other	nputs at V _{CC} or GND	3 V to 3.6 V			500	μΑ
Ci	V _I = V _{CC} or GND	_	3.3 V		2.5		рF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT	
			MIN MAX MIN MAX			MAX]	
fclock	Clock frequency		0	24	0	19	MHz	
	Pulse duration	CLR low	20		25		ns	
t _w	Pulse duration	CLK high or low	20		25			
	0-1	Data	16		20			
^t su	Setup time before CLK↑	CLR inactive	5		5		ns	
th	Hold time, data after CLK↑		5		5		ns	

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	V _{CC} =	3.3 V ±	0.3 V	V _{CC} =	2.7 V	UNIT	
FANAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	ONI	
f _{max}				90		19		MHz	
^t pd	CLK	Q		12	25		31	ns	
^t PHL	CLR	Q		13	26		33	ns	



operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER		TEST CONDITIONS		
C _{pd}	Power dissipation capacitance per flip-flop	C _L = 50 pF,	f = 10 MHz	32	pF

PARAMETER MEASUREMENT INFORMATION TEST S1 O Open 1 $k\Omega$ From Output tPLH/tPHL Open **Under Test** O GND tPLZ/tPZL 6 V tPHZ/tPZH **GND** CL = 50 pF 1 kΩ (see Note A) 2.7 V LOAD CIRCUIT FOR OUTPUTS 1.5 V **Timing Input** tsu 2.7 V 2.7 V 1.5 V Input 1.5 V **Data Input** 0 V 0 V **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS PULSE DURATION** SETUP AND HOLD TIMES 2.7 V Output 1.5 V Input 1.5 V 1.5 V Control 0 V **tPZL tPHL** Output VOH Waveform 1 Output S1 at 6 V VOL (see Note B) **tPHZ** tPHL tpzh -Output ۷он Waveform 2 1.5 V Output S1 at GND (see Note B) **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS** PROPAGATION DELAY TIMES **ENABLE AND DISABLE TIMES INVERTING AND NONINVERTING OUTPUTS LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



SN74LV373 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCLS196A - FEBRUARY 1993 - REVISED JULY 1995

•	EPIC™ (Enhanced-Performance Implanted
	CMOS) 2-μ Process

- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB.	DW.	OR	PW	PACI	KAGE
•			VIE		

		$\tau \tau$		
OE [1		20] v _{cc}
	2] 8Q
1D 🛚	3		18	8D
2D [4		17	7D
2Q [5] 7Q
3Q [6		15] 6Q
3D [7		14] 6D
4D [8		13	5D
4Q [9		12] 5Q
GND [10		11	LE

description

This octal transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LV373 is available in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

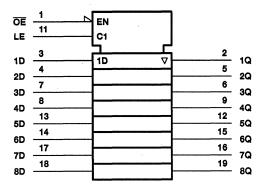
The SN74LV373 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each latch)

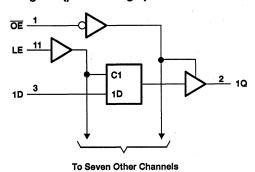
	,		·
	INPUTS	OUTPUT	
ŌĒ	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	Ĺ	X	Q ₀
н	X	Х	z

EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at $T_A = 55^{\circ}$ C (in still air) (see Note 3): DB package	0.6 W
DW package	1.6 W
PW package	0.7 W
Storage temperature range, Teta	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2.7	3.3	3.6	٧
VιΗ	High-level input voltage	V _{CC} ≠ 2.7 V to 3.6 V	2			٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	٧
VI	Input voltage		0		Vcc	٧
Vo	Output voltage		0		VCC	V
ЮН	High-level output current				-8	mA
lOL	Low-level output current				8	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

SCLS196A - FEBRUARY 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CO	ONDITIONS	v _{cc} †	MIN	TYP	MAX	UNIT
Vari	I _{OH} = -100 μA		MIN to MAX	V _{CC} -0.2	!		٧
Voн	I _{OH} = -8 mA		3 V	2.4			v
Vo.	I _{OL} = 100 μA		MIN to MAX			0.2	V
, VOL	I _{OL} = 8 mA		3 V			0.4	v
lį	V _I = V _{CC} or GND		3.6 V			±1	μА
loz	V _O = V _{CC} or GND		3.6 V			±5	μА
Icc	$V_I = V_{CC}$ or GND,	IO = 0	3.6 V			20	μА
ΔlCC	One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			500	μА
Ci	VI = VCC or GND		3.3 V		2.5		pF
Co	$V_O = V_{CC}$ or GND		3.3 V	1	7		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V _{CC} =	3.3 V 3 V		UNIT	
			MIN	MAX	MIN	MAX	
t _W	Pulse duration, LE high		20		25		ns
t _{su}	Setup time, data before LE↓	High or low	10		13		ns
th	Hold time, data after LE↓	High or low	10		10		ns

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

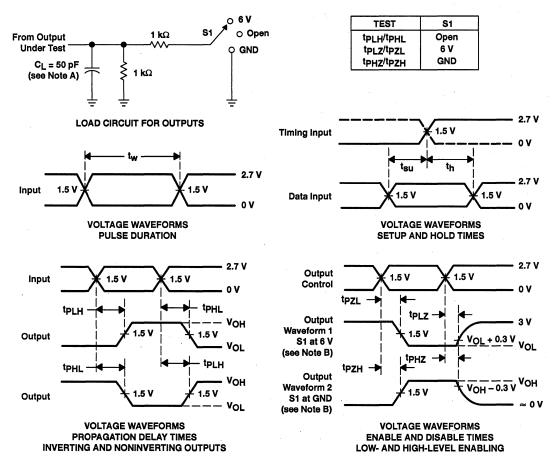
Γ	PARAMETER	FROM	то	V _{CC} = 3.3 V	± 0.3 V	V _{CC} = 2.7 V	UNIT
L	PANAMETEN	(INPUT)	(OUTPUT)	MIN TY	MAX	MIN MAX	ONII
ſ		D		1	1 25	31	
L	^t pd	LE]	1	5 29	36	ns
	t _{en}	ŌĒ	Q	1	5 29	36	ns
I	^t dis	ŌĒ	Q	1	5 29	36	ns

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$

	PARAMETER		TEST CO	NDITIONS	TYP	UNIT
	Dower discipation considered non-fateb	Outputs enabled	0 50 - 5	4 40 1411-	47	
Cpd	Power dissipation capacitance per latch	Outputs disabled	$C_L = 50 \text{ pF},$	f = 10 MHz	29	ρF

SCLS196A - FEBRUARY 1993 - REVISED JULY 1995

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O =$ 50 Ω , $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN74LV374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCLS197A - FEBRUARY 1993 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted CMOS) 2-μ Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB,	DW,	OR	PW	PA	CKA	GE
	(TOF	VIE	W)		

	_	$\overline{}$	1
OE [O 20	vcc
1Q [2	19] 8Q
1D 🛛] 8D
2D 🛛			7D
2Q []		16	7Q
3Q 🛛		15	6Q
3D 🛚		14] 6D
4D 🛛	8		5D
	9	12	5Q
GND [10	11	CLK

description

This octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV374 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable (OE) input can be used to place the eight outputs in either as normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LV374 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV374 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each flip-flop)

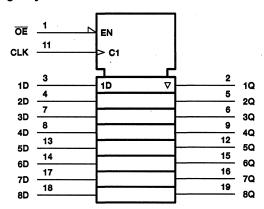
	INPUTS	OUTPUT	
ŌĒ	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	L	X	Q ₀
Н	Х	Х	Z

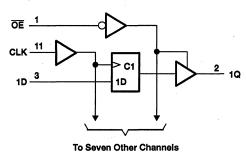
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logic symbol†

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, IOK (VO < 0 or VO > VCC)	±50 mA
Continuous output current, IO (VO = 0 to VCC)	±35 mA
Continuous current through V _{CC} or GND	
Maximum power dissipation at $T_A = 55$ °C (in still air) (see Note 3): DE	
DV	W package 1.6 W
	V package 0.7 W
Storage temperature range, T _{stg}	65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This value is limited to 4.6 V maximum.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SCLS197A - FEBRUARY 1993 - REVISED JULY 1995

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		2.7	3.3	3.6	V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	٧
۷į	Input voltage		0		VCC	٧
Vo	Output voltage		0		VCC	٧
ЮН	High-level output current				-8	mA
lOL	Low-level output current				8	mA
Δt/Δv	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	. ℃

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CO	NDITIONS	v _{cc} †	MIN	TYP	MAX	UNIT
Vau	I _{OH} = -100 μA		MIN to MAX	V _{CC} -0.	2		V
VOH	I _{OH} = -8 mA		3 V	2.4			V
Vo	I _{OL} = 100 μA		MIN to MAX			0.2	V
VOL	I _{OL} = 8 mA		3 V			0.4	٧
Ц.	V _I = V _{CC} or GND		3.6 V			±1	μА
loz	VO = VCC or GND	,	3.6 V			±5	μA
lcc	$V_I = V_{CC}$ or GND,	IO = 0	3.6 V			20	μА
ΔlCC	One input at V _{CC} - 0.6 V,	Other inputs at V _{CC} or GND	3 V to 3.6 V			500	μА
Ci	V _I = V _{CC} or GND		3.3 V		2.5		pF
Co	V _O = V _{CC} or GND		3.3 V		7		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V _{CC} =	3.3 V 3 V	AX MIN MAX 24 0 19 25	UNIT	
			MIN	MAX	MIN	MAX	1
fclock	Clock frequency		0	24	0	19	MHz
tw	Pulse duration, CLK high or low		20		25		ns
t _{su}	Setup time before CLK↑	High or low	13		16		ns
^t h	Hold time, data after CLK↑		5		5		ns

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	V _{CC} =	V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V	
FANAMETER	(INPUT)		MIN	TYP	MAX	MIN	MAX	UNIT
fmax			24	75		19		MHz
^t pd	CLK	Q	1	14	30		38	ns
^t en	ŌĒ	Q		15	29		36	ns
^t dis	ŌĒ	Q		15	29		36	ns



SCLS197A - FEBRUARY 1993 - REVISED JULY 1995

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER		TEST CONDITIONS	TYP	UNIT
Cnd Power dissipation capacitance per flip-flop	Outputs enabled	C _I = 50 pF, f = 10 MHz	52	pF	
Cpd	r ower dissipation capacitance per hip-hop	Outputs disabled		34	Pi

PARAMETER MEASUREMENT INFORMATION TEST S1 O Open 1 kΩ From Output Open tPLH/tPHL **Under Test** 6 V O GND tPLZ/tPZL GND tPHZ/tPZH C_L = 50 pF 1 kΩ (see Note A) 2.7 V LOAD CIRCUIT FOR OUTPUTS 1.5 V **Timing Input** tsu 2.7 V 2.7 V 1.5 V 1.5 V Input 1.5 V 1.5 V **Data Input** 0 V 0 V **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS PULSE DURATION SETUP AND HOLD TIMES** 2.7 V 2.7 V Output 1.5 V 1.5 V Input 1.5 V 1.5 V Control 0 V O V **tPZL tPLH tPHL tPLZ** Output VOH Waveform 1 1.5 V Output S1 at 6 V VOL (see Note B) ^tPHZ tPHL -^tPZH Output ۷он Waveform 2 1.5 V Output S1 at GND - VOL (see Note B) **VOLTAGE WAVEFORMS VOLTAGE WAVEFORMS** PROPAGATION DELAY TIMES **ENABLE AND DISABLE TIMES INVERTING AND NONINVERTING OUTPUTS** LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. CL includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
 - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



SN74LV573 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCLS198A - FEBRUARY 1993 - REVISED JULY 1995

- EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE (TOP VIEW)

ŌE [1	U	20	vcc
1D [2		19] 1Q
2D [3		18	2Q
3D [4		17	3Q
4D [5		16] 4Q
5D [6		15] 5Q
6D [7		14] 6Q
7D [8		13] 7Q
8D [9		12] 8Q
GND [10		11	LE

description

This octal transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV573 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (OE) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LV573 is available in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV573 is characterized for operation from -40°C to 85°C.

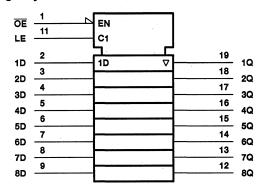
FUNCTION TABLE (each latch)

	INPUTS		OUTPUT
ŌĒ	LE	D	Q
L	Н	Н	Н
L	Н	L	L
L	L	Х	Q ₀
Н	Х	Х	Z

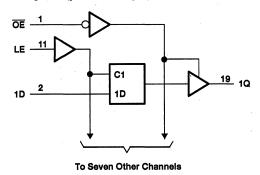
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logic symbol†



logic diagram (positive logic)



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC} 0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)
Output voltage range, VO (see Notes 1 and 2)
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ± 50 mA
Continuous output current, IO (VO = 0 to VCC) ±35 mA
Continuous current through V _{CC} or GND
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB package
DW package 1.6 W
PW package 0.7 W
Storage temperature range. Teta ————————————————————————————————————

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2.7	3.3	3.6	V
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			٧
VIL	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	V
VI	Input voltage		0		VCC	V
Vo	Output voltage		0		VCC	٧
ЮН	High-level output current				-8	mA
loL	Low-level output current				8	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.



SCLS198A - FEBRUARY 1993 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v _{cc} †	MIN TYP	MAX	UNIT
	I _{OH} = -100 μA	MIN to MAX	V _{CC} -0.2		ν
VOH	I _{OH} = -8 mA	3 V	2.4		V
V	I _{OL} = 100 μA	MIN to MAX		0.2	V
VOL	I _{OL} = 8 mA	3 V		0.4	
łį	V _I = V _{CC} or GND	3.6 V		±1	μA
loz	V _O = V _{CC} or GND	3.6 V		±5	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V		20	μА
ΔlCC	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V		500	μА
Ci	VI = VCC or GND	3.3 V	2.5		pF
Co	V _O = V _{CC} or GND	3.3 V	7		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		UNIT
		MIN	MAX	MIN	MAX	
t _W	Pulse duration, LE high	20		25		ns
t _{su}	Setup time, data before LE↓	10	_	13		ns
th	Hold time, data after LE↓	8		8		ns

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

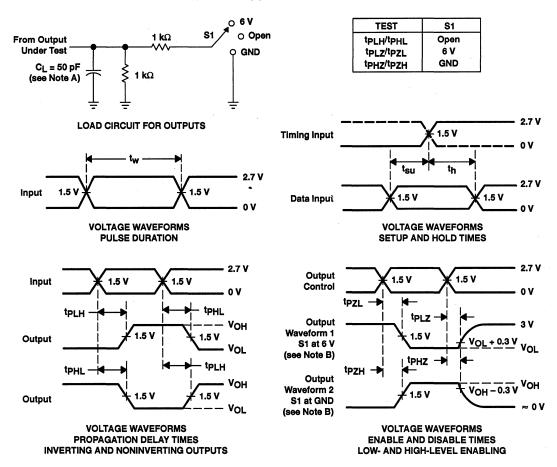
PARAMETER	FROM	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	UNIT
PANAMETEN	(INPUT)		MIN TYP	MAX	MIN MAX	UNII
	D 0		11	29	36	ns
^t pd	LE	Q	15	30	38] "
^t en	ŌĒ	Q	13	26	33	ns
^t dis	ŌĒ	Q	15	32	39	ns

operating characteristics, V_{CC} = 3.3 V, T_A = 25°C

		••				
	PARAMETER		TEST CO	NDITIONS	TYP	UNIT
<u> </u>	Power dissipation capacitance per latch	Outputs enabled	C:	f = 10 MHz	30	pF
Cbq	Fower dissipation capacitance per laten	Outputs disabled	$C_L = 50 pF$,	I = IU MHZ	14	pr

SCLS198A - FEBRUARY 1993 - REVISED JULY 1995

PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement,

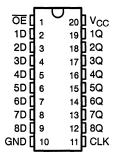
Figure 1. Load Circuit and Voltage Waveforms

SN74LV574 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

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- EPIC™ (Enhanced-Performance Implanted CMOS) 2-µ Process
- Typical V_{OLP} (Output Ground Bounce)
 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 2 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE (TOP VIEW)



description

This octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV574 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LV574 is available in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV574 is characterized for operation from -40°C to 85°C.

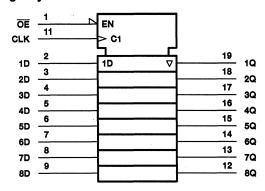
FUNCTION TABLE (each flip-flop)

	INPUTS	OUTPUT	
ŌĒ	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	L	Х	Q ₀
Н	X	Х	z

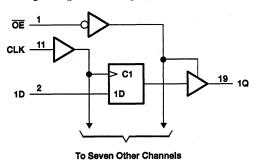
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logic symbolt



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V _{CC} or GND	±70 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DB pa	ckage 0.6 W
DW pa	ackage 1.6 W
PW pa	ackage 0.7 W
Storage temperature range, T _{stg}	–65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This value is limited to 4.6 V maximum.
 - The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology
 Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage	2.7	3.3	3.6	٧	
VIH	High-level input voltage	V _{CC} = 2.7 V to 3.6 V	2			٧
۷ _{IL}	Low-level input voltage	V _{CC} = 2.7 V to 3.6 V			0.8	٧
٧ı	Input voltage		0		Vcc	V
۷o	Output voltage		0		Vcc	٧
ЮН	High-level output current				-8	mA
loL	Low-level output current				8	mA
Δt/Δν	Input transition rise or fall rate		0		100	ns/V
TA	Operating free-air temperature		-40		85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST COND	vcct	MIN	TYP	MAX	UNIT	
Vari	I _{OH} = -100 μA		MIN to MAX	V _{CC} -0.2			٧
VOH	I _{OH} = -8 mA	I _{OH} = -8 mA		2.4			١ '
V	I _{OL} = 100 μA	I _{OL} = 100 μA				0.2	٧
VOL	I _{OL} = 8 mA	3 V			0.4	v	
li	V _I = V _{CC} or GND		3.6 V			±1	μА
loz	VO = VCC or GND		3.6 V			±5	μА
Icc	V _I = V _{CC} or GND, I _C) = 0	3.6 V			20	μА
Δlcc	One input at V _{CC} - 0.6 V, O	ther inputs at V _{CC} or GND	3 V to 3.6 V			500	μА
Ci	V _I = V _{CC} or GND		3.3 V		2.5		pF
Co	VO = VCC or GND		3.3 V		7		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V _{CC} =	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V	
			MIN	MAX	MIN	MAX	
fclock	ock Clock frequency		0	24	0	19	MHz
tw	Pulse duration, CLK high or low		20		25		ns
tsu	Setup time before CLK↑	High or low	13		16		ns
th	Hold time, data after CLK↑		5		5		ns

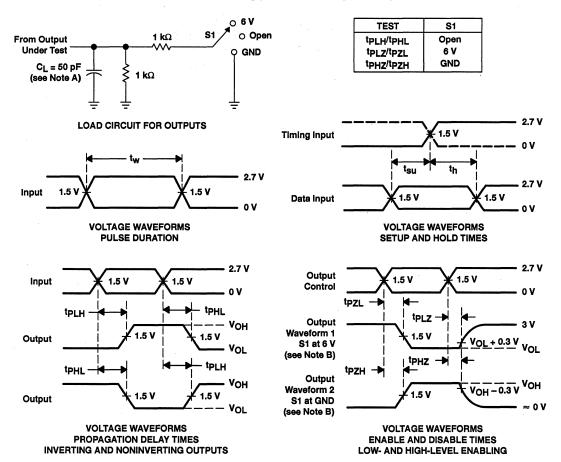
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		UNIT
PANAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	UNIT
fmax			24	70		19		MHz
^t pd	CLK	Q		14	30		38	ns
^t en	ŌĒ	Q		13	27		34	ns
^t dis	ŌĒ	Q		15	29		36	ns

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER			TEST CO	TYP	UNIT	
Cpd	Power dissipation capacitance per flip-flop	Outputs enabled	C _I = 50 pF,	f = 10 MHz	40	pF
Opg Fower dissipatio	1 office dissipation capacitation per hip-hop	Outputs disabled	C[= 50 pr,	1 = 10 MIF12	22	Pi-

PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z $_{O}$ = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

General Information	18
ALB Widebus™	2
ALVC Widebus™	3
LVT Octals	4
LVTZ Octals: Power Up and 3 State	5
LVT Widebus™	6
LVT JTAG/IEEE 1149.1	7
LVC MSI and Octals	8
LVC Widebus™	9
LV MSI and Octals	10
GTL Transceivers and Backplane Drivers	11
Application Reports	12
Characteristics Information	13
Mechanical Data	14

661

Contents

		Page
SN54/74GTL16612	18-Bit GTL/LVT Universal Bus Transceivers	11-3
SN54/74GTL16616	17-Bit GTL/LVT Universal Bus Transceivers With Buffered Clock Outputs	11-9
SN54/74GTL16622	18-Bit LVTTL to GTL/GTL+ Bus Transceivers	11-17
SN54/74GTL16921	20-Bit Flip-Flops With GTL I/O Levels	11-25

SN54GTL16612, SN74GTL16612 18-BIT GTL/LVT UNIVERSAL BUS TRANSCEIVERS

SCBS480C - JUNE 1994 - REVISED JULY 1995

- Translate Between GTL Logic Levels and LVTTL or 5-V TTL Logic Levels
- **Members of the Texas Instruments** Widebus™ Family
- **Support Mixed-Mode Signal Operation on**
- Universal Bus Transceiver (UBT™) Combines D-Type Latches and D-Type Flip-Flops With Qualified Storage Enable
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors on A Port
- Flow-Through Architecture Optimizes **Printed-Circuit-Board Layout**
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Ceramic Flat (WD) Packages

description

These 18-bit bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

The B port operates at GTL levels while the A port and control inputs are compatible with LVTTL or 5-V TTL logic levels.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock or latch-enable can be controlled by the clock-enable (CEAB and CEBA) inputs. For A-to-B data flow, the devices operate

SN54GTL16612...WD PACKAGE SN74GTL16612...DGG OR DL PACKAGE (TOP VIEW)

		U		
OEAB [_		CEAB
LEAB [CLKAB
A1 [54] B1
GND [GND
A2 🛚			52	B2
АЗ [] B3
V _{CC} (3.3 V)	7		50	V _{CC} (5 V)
A4 [8		49] B4
A5 [48] B5
A6 🛚			47] B6
GND [11			GND
A7 🛚	12		45] B7
A8 [13		44] B8
A9 [14		43] B9
A10 🛚	15		42	B10
A11 [B11
A12 🛚				B12
GND [18] GND
A13 🛚] B13
A14 🛚			37	B14
A15 🛚] B15
V _{CC} (3.3 V)	22		35] v _{REF}
A16 🛚	23			B16
A17 🛚	24		33	B17
GND [25		32	GND
A18 🛚	26		31	B18
OEBA [27		30	CLKBA
LEBA 🛚			29	
	_		_	1

in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if \overline{CEAB} is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if \overline{CEAB} is also low. \overline{OEAB} is active low. When \overline{OEAB} is low, the outputs are active. When OEAB is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that for A to B but uses OEBA, LEBA, CLKBA, and CEBA.

To ensure the high-impedance state during power up or power down, $\overline{\sf OE}$ should be tied to V $_{\sf CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54GTL16612 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74GTL16612 is characterized for operation from -40°C to 85°C.

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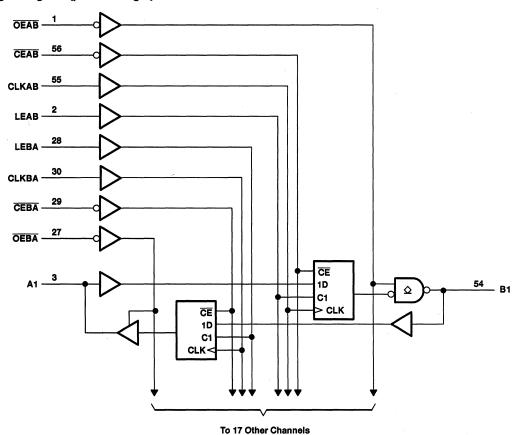
SCBS480C - JUNE 1994 - REVISED JULY 1995

		LET

		INPUTS			OUTPUT	MODE
CEAB	OEAB	LEAB	CLKAB	Α	В	MODE
X	Н	Х	Х	Х	Z	′
L	L	L	Н	Χ	в ₀ ‡	Latched storage of A data
L	L	L	L	Х	B ₀ §	
X	L	Н	Х	L	L	Transparent
Х	L	Н	Х	Н	Н	Transparent
L	L	L	1	L	L	Clasked storage of A data
L	L	L	1	Н	Н	Clocked storage of A data
Н	L	L	Х	Х	B ₀ §	Clock inhibit

[†] A-to-B data flow is shown: B-to-A data flow is similar but uses $\overline{\text{OEBA}}$, LEBA, CLKBA, and $\overline{\text{CEBA}}$.

logic diagram (positive logic)



[‡] Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

[§] Output level before the indicated steady-state input conditions were established

SN54GTL16612, SN74GTL16612 18-BIT GTL/LVT UNIVERSAL BUS TRANSCEIVERS

SCBS480C - JUNE 1994 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} : 3.3 V	0.5 V to 4.6 V
5 V	0.5 V to 7 V
Input voltage range, V _I (see Note 1): A port	
	0.5 V to 4.6 V
Voltage range applied to any output in the high or	
power-off state, VO (see Note 1): A port	0.5 V to 7 V
B port	0.5 V to 4.6 V
Current into any A-port output in the low state, IO	
Current into any B-port output in the low state, IO	
Current into any A-port output in the high state, IO (see Note 2)	
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, I_{OK} ($V_O < 0$)	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3	B): DGG package 1 W
	DL package 1.4 W
Storage temperature range, T _{stq}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and $V_O > V_{CC}$.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

				SN54GTL	16612		N74GTL1	6612	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
V	Supply voltage, 3.3 V		3.15	3.3	3.45	3.15	3.3	3.45	V
vcc	Supply voltage, 5 V		4.75	5	5.25	4.75	5	5.25	l
VREF	Supply voltage			0.8			0.8		٧
V.	Input voltage	B port			∜ CC (3.3 V)			V _{CC} (3.3 V)	V
VI	input voitage	Except B port			∜ 5.5			5.5	\ \
Vu	High level input voltage	B port	V _{REF} +50		,	V _{REF} +50	mV		V
VIH	High-level input voltage	Except B port	2	~~		2			\ \ \
Vu	Low-level input voltage	B port		Š	VREF -50 mV			VREF -50 mV	V
٧L	Low-level input voltage	Except B port		ŝ	0.8			8.0	V
ΊΚ	Input clamp current		á	.	-18			-18	mA
ЮН	High-level output current	A port			-32			-32	mA
1	Low-level output current	A port			64			64	mA
<u>o</u> L	Low-level output current	B port			40			40	l IIIA
TA	Operating free-air tempera	ature	-55		125	-40		85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

SN54GTL16612, SN74GTL16612 18-BIT GTL/LVT UNIVERSAL BUS TRANSCEIVERS

SCBS480C - JUNE 1994 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range, $V_{REF} = 0.8 \text{ V}$ (unless otherwise noted)

DADAI	METER	TEST CON	DITIONS	SN5	4GTL16	612	SN7	4GTL16	612	UNIT	
PAKAI	MEIER	TEST CON	DITIONS	MIN	TYPT	MAX	MIN	TYP	MAX	UNII	
VOH A port VCC (3.3 VCC (5 V		V _{CC} (3.3 V) = 3.15 V, V _{CC} (5 V) = 4.75 V	I _I = -18 mA			-1.2			-1.2	٧	
	,	V _{CC} = MIN to MAX [‡] ,	I _{OH} = -100 μA	Vcc-	0.2		Vcc-	0.2			
Vон	A port	V _{CC} (3.3 V) = 3.15 V,	I _{OH} = -8 mA	2.4			2.4	**		V	
	<u> </u>	V _{CC} (5 V) = 4.75 V	I _{OH} = - 32 mA	2			2				
			I _{OL} = 100 μA			0.2			0.2		
	A port	V _{CC} (3.3 V) = 3.15 V,	IOL = 16 mA			0.4			0.4		
VOL	1,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	V _{CC} (5 V) = 4.75 V	IOL = 32 mA			0.5			0.5	v	
- OL			I _{OL} = 64 mA	<u> </u>		0.55			0.55	-	
	B port	V _{CC} (3.3 V) = 3.15 V, V _{CC} (5 V) = 4.75 V	I _{OL} = 40 mA			0.4			0.4		
	Control inputs	V _{CC} = 0 or MAX [‡] ,	V _I = 5.5 V			10			10		
			V _I = 5.5 V			20			20		
l _l	A port	V _{CC} (3.3 V) = 3.45 V, V _{CC} (5 V) = 5.25 V	VI = VCC			_ 1			1	μА	
		V(() (0 V) = 0.20 V	V _I = 0			<i>⟨</i> ं)−30			-30		
	B port	V _{CC} (3.3 V) = 3.45 V,	V _I = V _{CC} (3.3 V)		Į,	5			5		
	B port	V _{CC} (5 V) = 5.25 V	V _I = 0			-5			-5		
loff		V _{CC} = 0,	V_1 or $V_0 = 0$ to 4.5 V		Ç.	100			100	μA	
lia in	A port	V_{CC} (3.3 V) = 3.15 V,	V _i = 0.8 V	75	0		75			μА	
I(hold)	1,000	V _{CC} (5 V) = 4.75 V	V _I = 2 V	-750	**		-75			<u> </u>	
lozh	A port	V _{CC} (3.3 V) = 3.45 V,	V _O = 3 V			1			1	μА	
·OZN	B port	V _{CC} (5 V) = 5.25 V	V _O = 1.2 V			10			10	μΛ	
lozL	A port	V_{CC} (3.3 V) = 3.45 V,	V _O = 0.5 V	<u> </u>		-1			-1	μА	
OZL	B port	V _{CC} (5 V) = 5.25 V	V _O = 0.4 V			-10			-10	p	
	1	V _{CC} (3.3 V) = 3.45 V,	Outputs high	<u> </u>		1		i	1		
ICC (3.3 V)	A or B port	V_{CC} (5 V) = 5.25 V, I_{O} = 0,	Outputs low			5			5	mA	
		V _I = V _{CC} (3.3 V) or GND	Outputs disabled	ļ ·		1			1		
		V _{CC} (3.3 V) = 3.45 V,	Outputs high			120			120		
ICC (5 V)	A or B port	V _{CC} (5 V) = 5.25 V,	Outputs low			120			120	mA	
		$I_O = 0$, $V_I = V_{CC}$ (3.3 V) or GND	Outputs disabled	ļ		120			120		
Δl _{CC} §		V _{CC} (3.3 V) = 3.45 V, A or control inputs at V _{CC} One input at 2.7 V	V _{CC} (5 V) = 5.25 V, (3.3 V) or GND,			1			1	mA	
Ci	Control inputs	V _I = 3.15 V or 0			3.5			3.5		pF	
C:-	A port	V _O = 3.15 V or 0			12			12		рF	
Cio	B port	Per IEEE Standard 1149.0-	-1991			5			5	þΓ	

 $[\]uparrow$ All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.

[‡] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SN54GTL16612, SN74GTL16612 18-BIT GTL/LVT UNIVERSAL BUS TRANSCEIVERS

SCBS480C - JUNE 1994 - REVISED JULY 1995

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 0.8 V (unless otherwise noted)

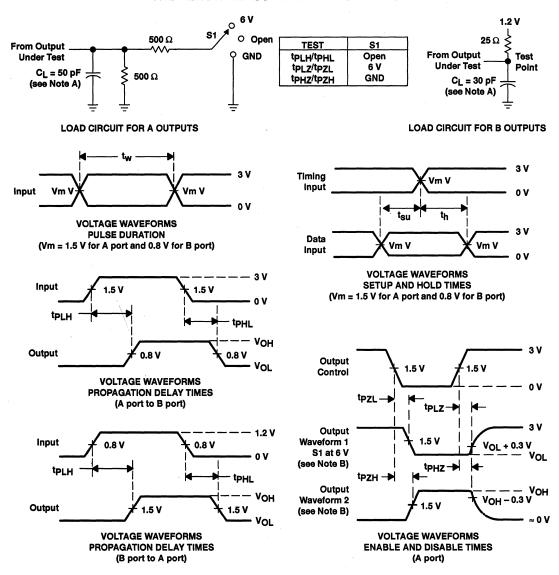
			SN54G	TL16612	SN74G	TL16612		
			MIN	MAX	MIN MAX		UNIT	
fclock	Clock frequency		0	95	0	95	MHz	
	Pulse duration	LEAB or LEBA high	3.3		3.3			
t _w	Pulse duration	CLKAB or CLKBA high or low	5.6		5.6		ns	
		A before CLKAB↑	0.9		. 0			
		B before CLKBA↑	3.4	42.	2.5		1	
	Catum time	A before LEAB↓	1.2	.84	0.4		١	
t _{su}	Setup time	B before LEBA↓	1		0.9		ns	
		CEAB before CLKAB↑	2.1	~	1		ĺ	
		CEBA before CLKBA↑	2.6)	2.1		1	
		A after CLKAB↑	2,9		2.7			
•		B after CLKBA↑	Q4.1		0.4		1	
	I I a lad Attack a	A after LEAB↓	4.5		3.4		l	
th	Hold time	B after LEBA↓	4.3		3.3		ns	
		CEAB after CLKAB↑	2		1.5		1	
		CEBA after CLKBA↑	0.5		0.4		1	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $V_{REF} = 0.8 \text{ V}$ (see Figure 1)

DADAMETED	FROM	то	SN5	4GTL16	612	SN7	4GTL16	612	UNIT	
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYPT	MAX	MIN	TYPT	MAX	UNII	
fmax			95			95			MHz	
tPLH	Α	В	1	2.6	3.8	1	2.6	3.8		
t _{PHL}	^	В	. 1	2.2	4	1	2.2	4	ns	
tPLH	LEAB	В	1.8	3.6	5.4	1.8	3.6	5.4	ns	
tPHL	LEAD		1.5	3.3	5.5	1.5	3.3	5.5	20	
t _{PLH}	ÇLKAB	В	1.8	3.7	5.3	1.8	3.7	5.3		
^t PHL	OLIVAB		1.5	3.3	5.5	1.5	3.3	5.5	ns	
tPLH	ŌEAB	В	1.6	3.3	\$ 4.7	1.6	3.3	4.7	ns	
^t PHL			1.3	3.20		1.3	3.2	5.5	113	
t _r	Transition time, B or	utputs (0.5 V to 1 V)		<i>≸</i> ;3			1.3		ns	
tf	Transition time, B or	utputs (1 V to 0.5 V)		0.5			0.5		ns	
^t PLH	В	Α	2,	\$ 4.8	6.9	2	4.8	6.9		
^t PHL	. В		1.4	3.6	5.1	1.4	3.6	5.1	ns	
tPLH	LEBA	Α	2.1	4.3	6.1	2.1	4.3	6.1	ns	
t _{PHL}	LEDA	A	1.9	3.6	5.1	1.9	3.6	5.1	ns	
tPLH	CLKBA	Α	2.3	4.5	6.4	2.3	4.5	6.4	-	
tPHL	ULNDA	A	2.2	4	5.6	2.2	4	5.6	ns	
t _{en}	ŌĒBĀ	Α	1.9	4.7	7.2	1.9	4.7	7.2		
^t dis	OEBA	A	2.5	4.6	6.9	2.5	4.6	6.9	ns	

[†] All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



SCBS481B - JUNE 1994 - REVISED JULY 1995

- Translate Between GTL Signal Levels and LVTTL or 5-V TTL Signal Levels
- Members of the Texas Instruments Widebus™ Family
- Support Mixed-Mode Signal Operation on A Port
- Universal Bus Transcelver (UBT™)
 Combines D-Type Latches and D-Type
 Flip-Flops With Qualified Storage Enable
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors on A Port
- Flow-Through Architecture Optimizes
 PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Ceramic Flat (WD) Packages

description

These 17-bit registered bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes. The 'GTL16616 provide for a copy of CLKAB at GTL logic levels (CLKOUT) and also provide a conversion of the GTL clock to a TTL environment (CLKIN).

The B port operates at GTL levels while the A port and control inputs are compatible with LVCMOS, LVTTL, or 5-V TTL logic levels.

SN54GTL16616... WD PACKAGE SN74GTL16616... DGG OR DL PACKAGE (TOP VIEW)

		_	
OEAB [1	56	CEAB
LEAB [55	CLKAB
A1 [54] B1
GND [4	53	GND
A2 [5] B2
АЗ] B3
V _{CC} (3.3 V)	7	50	V _{CC} (5 V)
A4 🛚		49] B4
A5 [48] B5
A6 [] B6
GND [GND
A7 🛚] B7
A8 [] B8
A9 [] B9
A10 [15	42	B10
A11 [] B11
A12 🛚			B12
GND [18	39] GND
A13 🛚] B13
A14 🛚	20		B14
A15 🛚			B15
V _{CC} (3.3 V)	22	35] v _{REF}
A16 🕻			B16
A17 🛭			B17
GND [25] GND
CLKIN [31	CLKOUT
OEBA [30	CLKBA
LEBA [28	29	CEBA

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock or latch-enable can be controlled by the clock-enable (CEAB and CEBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CEAB is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if CEAB is also low. OEAB is active low. When OEAB is low, the outputs are active. When OEAB is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, CLKBA, and CEBA.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74GTL16616 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54GTL16616 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74GTL16616 is characterized for operation from -40°C to 85°C.

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SN54GTL16616, SN74GTL16616 17-BIT GTL/LVT UNIVERSAL BUS TRANSCEIVERS WITH BUFFERED CLOCK OUTPUTS SCBS481B - JUNE 1994 - REVISED JULY 1995

FUNCTION TABLET

		INPUTS			OUTPUT	MODE
CEAB	OEAB	LEAB	CLKAB	Α	В	MODE
X	Н	Х	Х	Х	Z	
L	L	L	H or L	Χ	В ₀ ‡	Latched storage of A data
L	L	L	H or L	Х	В ₀ §	
X	L	Н	Х	L	L	Transparent
X	L	Н	Х	Н	н	Transparent
L	L	L	1	L	L	Cleaked starage of A data
L	. L	L	1	Н	Н	Clocked storage of A data
Н	L	L	Х	Х	B ₀ §	Clock inhibit

[†] A-to-B data flow is shown: B-to-A data flow is similar but uses OEBA, LEBA, CLKBA, and CEBA.

[‡] Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

[§] Output level before the indicated steady-state input conditions were established

SCBS481B - JUNE 1994 - REVISED JULY 1995

logic diagram (positive logic) OEAB _1 CEAB 56 CLKAB __55 LEAB 2 LEBA 28 CLKBA 30 CEBA 29 OEBA 27 CE 1D C1 > CLK CE 1D C1 1 of 17 Channels 31 CLKOUT CLKIN 26

SCBS481B - JUNE 1994 - REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} : 3.3 V	-0.5 V to 4.6 V 0.5 V to 7 V
Input voltage range, V _I (see Note 1): A port	0.5 V to 7 V
Voltage range applied to any output in the high or	
power-off state, V _O (see Note 1): A port	0.5 V to 7 V
B port	-0.5 V to 4.6 V
Current into any A-port output in the low state, IO	
Current into any B-port output in the low state, Io	80 mA
Current into any A-port output in the high state, IO (see Note 2)	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, $I_{OK}(V_O < 0)$	50 mA
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	
Storage temperature range, T _{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and VO > VCC.

recommended operating conditions (see Note 4)

				SN54GTL16	616	s	N74GTL	16616	UNIT	
			MIN	NOM	MAX	MIN	NOM	MAX	ONII	
	Supply voltage, 3.3 V		3.15	3.3	3.45	3.15	3.3	3.45	V	
vcc	Supply voltage, 5 V		4.75	5	5.25	4.75	5	5.25	V	
VREF	Supply voltage			0.8			0.8		٧	
Vı	Innuit valtage	B port			VCC (3.3 V)			V _{CC} (3.3 V)	٧	
۸I	Input voltage	Except B port			5.5			5.5	v	
	High-level input voltage	B port	V _{REF} +50			VREF +50	mV		V	
VIH	nigh-level input voltage	Except B port	2	Λ.		2			V	
V.	Low lovel input voltage	B port	,		REF -50 mV			V _{REF} -50 mV	V	
VIL	Low-level input voltage	Except B port		ి	0.8			0.8	_ v	
ŀΚ	Input clamp current		<	*	-18			-18	mA	
Юн	High-level output current	A port			-32			-32	mA	
la.	Lave lavel autout autout	A port			64			64		
IOL	Low-level output current	B port			40			40	mA	
TA	Operating free-air tempera	-55		125	-40		85	°C		
IOTE A	Unused insurts must be be	lal black on law to		. f						

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

SCBS481B - JUNE 1994 - REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range, V_{REF} = 0.8 V (unless otherwise noted)

DADAI	METER	TEST CON	DITIONS	SN5	4GTL16	616	SN7	4GTL16	616	UNIT
FARAI	WIETER		DITIONS	MIN	TYPT	MAX	MIN	TYPT	MAX	ONII
VIK		V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	l _j = –18 mA			-1.2			-1.2	>
		$V_{CC} = MIN \text{ to } MAX^{\ddagger}$,	I _{OH} = -100 μA	Vcc-	0.2		Vcc-0).2		
Vон	A port	V_{CC} (3.3 V) = 3.15 V,	IOH = -8 mA	2.4			2.4			V
		V _{CC} (5 V) = 4.75 V	$I_{OH} = -32 \text{ mA}$	2			2			
			I _{OL} = 100 μA			0.2			0.2	
	A port	V_{CC} (3.3 V) = 3.15 V,	I _{OL} = 16 mA	<u> </u>		0.4			0.4	
VOL		V _{CC} (5 V) = 4.75 V	I _{OL} = 32 mA	<u> </u>		0.5			0.5	v
OL			I _{OL} = 64 mA	<u> </u>		0.55			0.55	
	B port	V_{CC} (3.3 V) = 3.15 V, V_{CC} (5 V) = 4.75 V	I _{OL} = 40 mA			0.4			0.4	
	Control inputs	V _{CC} = 0 or MAX [‡] ,	V _j = 5.5 V			10			10	
		V (0.0.V) 0.45.V	V _I = 5.5 V			20			20	
կ	A port	V _{CC} (3.3 V) = 3.45 V, V _{CC} (5 V) = 5.25 V	V _I = V _{CC}			1			1	μA
		100 (0 1) = 0.20 1	V _I = 0			_30			-30	
	B port	V_{CC} (3.3 V) = 3.45 V,	$V_{I} = V_{CC} (3.3 \text{ V})$		5				5	
	I port	V _{CC} (5 V) = 5.25 V	V ₁ = 0	<u> </u>		<u>" –5</u>			-5	
loff		V _{CC} = 0,	V _I or V _O = 0 to 4.5 V		100	100			100	μA
II(hold)	A port	V_{CC} (3.3 V) = 3.15 V,	V _j = 0.8 V	75 💸			75			μА
		V _{CC} (5 V) = 4.75 V	V _I = 2 V	-75			-75			
lozh	A port	V_{CC} (3.3 V) = 3.45 V,	V _O = 3 V	8	<u> </u>	1	<u> </u>	·	1	μΑ
	B port	V _{CC} (5 V) = 5.25 V	V _O = 1.2 V	ļ		10	ļ		10	
IOZL	A port	V_{CC} (3.3 V) = 3.45 V,	V _O = 0.5 V			-1			-1	μА
	B port	V _{CC} (5 V) = 5.25 V	V _O = 0.4 V	ļ		-10			-10	
	l	V _{CC} (3.3 V) = 3.45 V, V _{CC} (5 V) = 5.25 V,	Outputs high	<u> </u>		1			1	
ICC (3.3 V)	A or B port	10 = 0,	Outputs low	5				5	mA	
	<u> </u>	V _I = V _{CC} (3.3 V) or GND	Outputs disabled			1			1	
		V_{CC} (3.3 V) = 3.45 V,	Outputs high			120			120	
ICC (5 V)	A or B port	V _{CC} (5 V) = 5.25 V, I _O = 0,	Outputs low			120			120	mA
	ļ	V _I = V _{CC} (3.3 V) or GND	Outputs disabled			120			120	
Δl _{CC} §		V _{CC} (3.3 V) = 3.45 V, A or control inputs at V _{CC} One input at 2.7 V	V _{CC} (5 V) = 5.25 V, (3.3 V) or GND,			1			1	mA
Ci	Control inputs	V _I = 3.15 V or 0			3.5			3.5		pF
C.	A port	V _O = 3.15 V or 0	O = 3.15 V or 0		12		12			pF
Cio	B port	Per IEEE 1194.0-1991				5			5	PΓ

[†] All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C. ‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SCBS481B - JUNE 1994 - REVISED JULY 1995

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 0.8 V (unless otherwise noted)

			SN54G	TL16616	SN74G	TL16616	UNIT
			MIN	MAX	MIN	MAX	UNII
fclock	Clock frequency		0	95	0	95	MHz
	Pulse duration	LEAB or LEBA high	3.3		3.3		
tw	Pulse duration	CLKAB or CLKBA high or low	5.5		5.5	,	ns
		A before CLKAB↑	1.1		1.1		
		B before CLKBA↑	2.6	di.	2.6		1
	O advisa disa a	A before LEAB↓	0	24	0		1
t _{su}	Setup time	B before LEBA↓	1		1		ns
		CEAB before CLKAB↑	1.8	~	1.8		
		CEBA before CLKBA↑	2.15 t)6	,	2.1		1
		A after CLKAB↑	, OF		1.6		
		B after CLKBA↑	₹0.2		0.2		Ì
	I ladel Norwa	A after LEAB↓	4.3		4.3		
th	Hold time	B after LEBA↓	2.8		2.8		ns
		CEAB after CLKAB↑	0.8		0.8		
		CEBA after CLKBA↑	0.7		0.7		1



SN54GTL16616, SN74GTL16616 17-BIT GTL/LVT UNIVERSAL BUS TRANSCEIVERS WITH BUFFERED CLOCK OUTPUTS SCBS481B, JUNE 1994 - REVISED JULY 1995

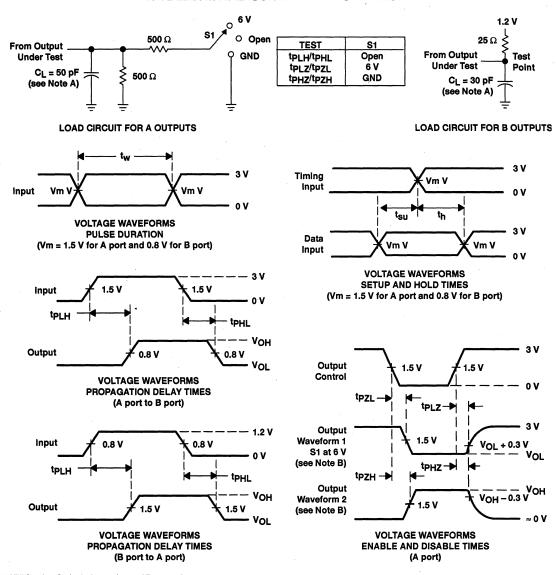
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $V_{\text{REF}} = 0.8 \text{ V}$ (see Figure 1)

PARAMETER	FROM	то	SNS	4GTL16	616	SN7	4GTL16	616	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYPT	MAX	MIN	TYPT	MAX	UNII
fmax			95			95			MHz
^t PLH	A	В	1	2.5	3.8	1	2.5	3.8	ns
t _{PHL}			1	2	3.8	1	2	3.8	118
^t PLH	LEAB	В	1.5	3.4	5.1	1.5	3.4	5.1	ns
t _{PHL}	LLAD		1.4	3.2	5.1	1.4	3.2	5.1	115
t _{PLH}	CLKAB	В	1.5	3.6	5	1.5	3.6	5	ns
t _{PHL}	CLMB		1.4	4.1	5	1.4	4.1	5	118
t _{PLH}	CLKAB	CLKOUT	3.4	6	7.7	3.4	6	7.7	ns
t _{PHL}	OLIVAB	CLROUT	4.3	7.4	10.4	4.3	7.4	10.4	113
t _{PLH}	<u>OEAB</u>	В	1.3	3.2	5	1.3	3.2	5	ns
t _{PHL}	OEAB		1.1	\$1	5	1.1	3.1	5	115
t _r	Transition time, B o	utputs (0.5 V to 1 V)		্রী.2			1.2		ns
tş	Transition time, B o	utputs (1 V to 0.5 V)	å	0.7			0.7		ns
t _{PLH}	В	Α	2.1	4.4	6.5	2.1	4.4	6.5	ns
, tphl		, ,	1.3	3.3	4.8	1.3	3.3	4.8	110
t _{PLH}	LEBA	Α	1.7	3.9	6	1.7	3.9	6	ns
t _{PHL}	LEDA	^	1.3	3.3	4.6	1.3	3.3	4.6	110
t _{PLH}	CLKBA	Α	1.7	4.1	6.3	1.7	4.1	6.3	ns
^t PHL	OLKDA	^	1.4	3.6	5.3	1.4	3.6	5.3	110
t _{PLH}	CLKOUT	CLKIN	6.5	10.5	14.3	6.5	10.5	14.3	ns
tPHL	OLNO01	CERIN	5.1	8.8	11.8	5.1	8.8	11.8	113
t _{en}	OEBA	Α	1.8	4.7	6.9	1.8	4.7	6.9	ns
^t dis	L		2	4.7	6.7	2	4.7	6.7	

[†] All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.

SCBS481B - JUNE 1994 - REVISED JULY 1995

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



SN54GTL16622, SN74GTL16622 18-BIT LVTTL TO GTL/GTL+ BUS TRANCEIVERS

•	Translate I	Between	GTL/GTL+	Signal	Level	S
	and LVTTL	_				

Members of the Texas Instruments Widebus™ Family

- Support GTL/GTL+ Signal Operation on
- D-Type Flip-Flops With Qualified Storage Enable
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors on A Port
- Flow-Through Architecture Optimizes **PCB Layout**
- Packaged in Plastic Thin Shrink Small-Outline (DGG) Package

description

The 'GTL16622 18-bit registered bus transceivers contain two sets of D-type flip-flops for temporary storage of data flowing in either direction.

The B port operates at GTL/GTL+ levels, while the A port and control inputs are compatible with LVTTL logic level.

Data flow in each direction is controlled by output-enable (OEAB and OEBA) and the clock (CLKAB and CLKBA) inputs. The clock-enable (CEAB and CEBA) inputs are designed to control nine bits at a time, which makes the device more versatile.

For A-to-B data flow, the devices operate on the low-to-high transition of CLKAB if CEAB is low. When OEAB is low, the outputs are active. When OEAB is high, the outputs are in the highimpedance state. Data flow for B to A is similar to that for A to B but uses OEBA, CLKBA, and CEBA.

DGG PACKAGE (TOP VIEW)

OEAB	q	1	O	64	þ	CLKAB
1A1		2		63	D	1CEAB
GND		3		62	D	1CEBA
1A2	q	4		61	p	1B1
1A3	_	5				GND
GND		6		59	p	1B2
VCC	q			58	0	1B3
1A4		8		57	0	V _{CC}
GND		9		56	P	1B4
1A5	g	10		55	0	1B5
1A6	П	11		54	U	1B6
GND		12				GND
·1A7		13		52	p	1B7
1A8		14		51	p	1B8
GND	q	15		50	D	GND
1A9	q	16				1B9
2A1		17		48	P	2B1
GND		18		47	0	GND
2A2		19		46	D	2B2
2A3		20				2B3
GND	q	21		44	þ	GND
2A4	q	22		43		2B4
2A5		23				2B5
GND	Q	24				2B6
2A6	-	25		40	0	V_{REF}
Vcc	q	26				2B7
GND		27		38	0	2B8
2A7	0	28		37	þ	GND
2A8	q	29		36	1	2B9
GND	_	30		35		2CEBA
2A9	4	31				2CEAB
OEBA	q	32		33	p	CLKBA

To ensure the high-impedance state during power up or power down, $\overline{\sf OE}$ should be tied to ${\sf V}_{\sf CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54GTL16622 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74GTL16622 is characterized for operation from -40°C to 85°C.

Widebus is a trademark of Texas Instruments Incorporated



SN54GTL16622, SN74GTL16622 18-BIT LVTTL TO GTL/GTL+ BUS TRANCEIVERS

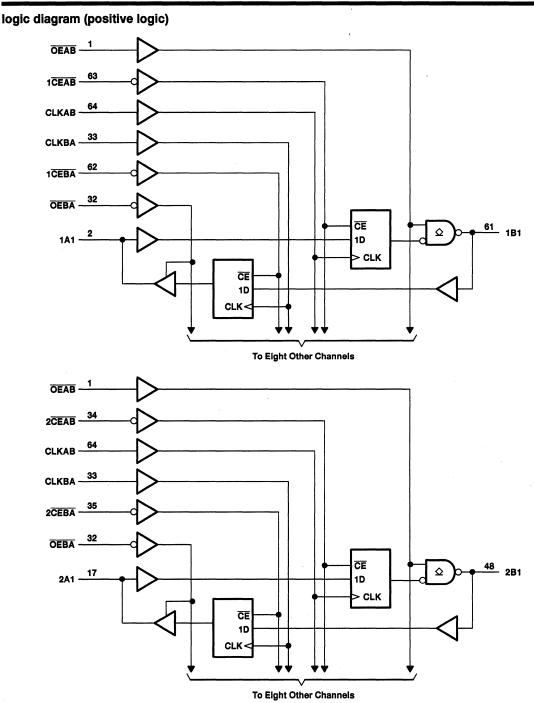
SCES049 - AUGUST 1995

FUNCTION TABLET

HODE	OUTPUT		INPUTS		
MODE	В	Α	CLKAB	OEAB	CEAB
	Z	Х	Х	Н	Х
1 -1-b-d -11 A d-1-	B ₀ ‡	Х	X	L	Н
Latched storage of A data	в ₀ ‡	X	H or L	L	X
Cleated storono of A data	L	L	1	L	L
Clocked storage of A data	н	н	↑	L	L

† A-to-B data flow is shown: B-to-A data flow is similar but uses OEBA, CLKBA, and CEBA.

[‡] Output level before the indicated steady-state input conditions were established





SN54GTL16622, SN74GTL16622 18-BIT LVTTL TO GTL/GTL+ BUS TRANCEIVERS

SCES049 - AUGUST 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} –0.5 V to 4.6	3 V
Input voltage range, V _I (see Note 1): A port	3 V
B port0.5 V to 4.6	3 V
Voltage range applied to any output in the high or	
power-off state, V _O (see Note 1): A port	3 V
B port	3 V
Current into any A-port output in the low state, I _O	
Current into any B-port output in the low state, IO	
Current into any A-port output in the high state, IO (see Note 2)	
Input clamp current, $I_{ K }(V_1 < 0)$	
Output clamp current, $I_{OK}(V_O < 0)$ —50 r	mΑ
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3)	
Storage temperature range, T _{stri}	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

- 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
- The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
 For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

recommended operating conditions (see Note 4)

			SN	54GTL	16622	SN	4GTL	16622	HAUT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage		3.15	3.3	3.45	3.15	3.3	3.45	V
VTT	Termination voltage		1.14	1.5	1.65	1.14	1.5	1.65	V
VREF	Supply voltage		0.74	1	. 1.1	0.74	1	1.1	٧
. V.	Innutualtage	B port			VCC			VCC	V
٧ı	Input voltage	Except B port			5.5			5.5	V
	Lieb level innut veltage	B port	V _{REF} +50 m	٧		VREF +50 m	/		V
VIH	High-level input voltage	Except B port	2			2			٧
V	Levelovel input voltage	B port			VREF -50 mV			VREF -50 mV	V
VIL	Low-level input voltage	Except B port			0.8			0.8	٧
ΊΚ	Input clamp current				-18			-18	mA
ЮН	High-level output current	A port			-24			-24	mA
1	l and land and an annual	A port			24			24	^
lOL	Low-level output current B port				50			50	mA
TA	Operating free-air tempera	ature	-55		125	-40		85	°C
NOTE 4	Unused inputs must be be	ld bigb or love to	avarrant than fo	and flac	lina.				

NOTE 4: Unused inputs must be held high or low to prevent them from floating.



ADVANCE INFORMATION

electrical characteristics over recommended operating free-air temperature range, V_{REF} = 1 V (unless otherwise noted)

D4.D	AMETER	TECT OO	NDITIONS	SN5	4GTL16	622	SN7	4GTL16	622	UNIT
PAH	AMEIER	I EST CO	NUTTIONS	MIN	TYPT	MAX	MIN	TYP	MAX	UNII
VIK		V _{CC} = 3.15 V,	I _I = -18 mA			-1.2			-1.2	٧
		V _{CC} = MIN to MAX [‡] ,	I _{OH} = -100 μA	Vcc-	0.2		Vcc-	0.2		
VOH	A port	V 215 V	I _{OH} = – 8 mA	2.4			2.4			٧
	İ	V _{CC} = 3.15 V	IOH = -24 mA	2			2			
			I _{OL} = 100 μA			0.2			0.2	
	A port	V _{CC} = 3.15 V	I _{OL} = 8 mA			0.4			0.4	V
			I _{OL} = 24 mA			0.5			0.5	
VOL		V _{CC} = MIN to MAX [‡] ,	I _{OL} = 100 μA			0.2			0.2	
	B port		I _{OL} = 10 mA			0.2			0.2	v
	B port	V _{CC} = 3.15 V	I _{OL} = 40 mA			0.4			0.4	٧
			I _{OL} = 50 mA			0.55			0.55	
Ц		V _{CC} = 3.45 V,	VI = VCC or GND			±5			±5	μА
loff		$V_{CC} = 0$,	V _I or V _O = 0 to 5.5 V			100			100	μА
l	A	V _{CC} = 3.15 V	V _I = 0.8 V	75			75			4
l (hold)	A port	VCC = 3.15 V	V _I = 2 V	-75			-75			μА
la	A port	V _{CC} = 3.45 V	V _O = 3 V			1			1	
lozh	B port	VCC = 3.45 V	V _O = 1.5 V			10			10	μΑ
la=:	A port	V _{CC} = 3.45 V	V _O = 0.5 V			-1			-1	μА
IOZL	B port	VCC = 3.45 V	V _O = 0.4 V			-10			-10	μА
		V _{CC} = 3.45 V,	Outputs high							
Icc	A or B port	lo = 0,	Outputs low							mΑ
		V _I = V _{CC} or GND	Outputs disabled							
∆l _{CC} §		V _{CC} = 3.45 V, A or control inputs at V _{CC} One input at 2.7 V	or GND,			1			1	mA
Ci	Control inputs	V _I = 3.15 V or 0			3.5			3.5		pF
C·.	A port	V _O = 3.15 V or 0			7			7		nΕ
C _{io}	B port	Per IEEE Standard 1149.	0-1991		6			6		pF

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. ‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

SCES049 - AUGUST 1995

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V (unless otherwise noted)

			SN54G	SN54GTL16622		SN74GTL16622		
			MIN	MAX	MIN	MAX	UNIT	
fclock	Clock frequency		0		0	200	MHz	
tw	Pulse duration, CLK high or low		2		2		ns	
		Data before CLK↑	2		2			
t _{su}	Setup time	CE before CLK↑	3		3		ns	
	Hold time	Data after CLK↑	0		0			
th	noid time	CE after CLK↑	0		0		ns	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V (see Figure 1)

PARAMETER	FROM	то	SNS	4GTL16	622	SN7	4GTL16	622	LIMIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYPT	MAX	MIN	TYPT	MAX	UNIT
fmax						200			MHz
tPLH	CLKAB	В						5	ns
tPHL t	OLIVAD							5.5	115
tPLH .	OEAB	В						5	ns
t _{PHL}] UEAB	D						5	IIS
Slew rate	Both tra	insitions				0.3		0.8	V/ns
t _r	Transition time, B ou	tputs (0.6 V to 1.3 V)				0.9		2.3	ns
tf	Transition time, B ou	tputs (1.3 V to 0.6 V)				0.9		2.3	ns
^t PLH	CLKBA	A						5	200
tPHL] CLNDA	^						5	ns
^t en	OEBA	_						6.5	no
^t dis]	Α						6	ns

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

ADVANCE INFORMATION

timing requirements over recommended ranges of supply voltage and operating free-air temperature, $V_{TT}=1.2\ V$ and $V_{REF}=0.8\ V$ (unless otherwise noted)

			SN54G	TL16622	SN74G		
		•	MIN	MAX	MIN	MAX	UNIT
fclock	Clock frequency		0		0	200	MHz
tw	Pulse duration, CLK high or low						ns
	Sotun time	Data before CLK↑					
t _{su}	Setup time	CE before CLK↑					ns
4.	Light time	Data after CLK↑					
th	Hold time	CE after CLK↑					ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.2 V and V_{REF} = 0.8 V (see Figure 1)

PARAMETER	FROM	то	SN5	4GTL16	622	SN7	4GTL16	622	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYPT	MAX	MIN	TYPT	MAX	UNII
fmax						200			MHz
t _{PLH}	CLKAB	В							ns
tPHL	OLIVAD								110
^t PLH	<u>ŌĒĀB</u>	В							ns
t _{PHL}	OEAB								12
Slew rate	Both tra	nsitions							V/ns
t _r	Transition time, B or	utputs (0.6 V to 1 V)							ns
tf	Transition time, B or	utputs (1 V to 0.6 V)							ns
tPLH .	CLKBA	Α							ns
^t PHL	CLRBA	^							115
^t en	OEBA	А							ns
^t dis	OLBA	^							118

[†] All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

PARAMETER MEASUREMENT INFORMATION V_{TT} = 1.5 V, V_{REF} = 1 V 500 Ω O Open TEST S1 From Output GND From Output **Under Test** Open Test tPLH/tPHL **Under Test** tpLZ/tpZL 6 V **Point** CL = 50 pF 500 Ω GND tPHZ/tPZH C_L = 30 pF (see Note A) (see Note A) LOAD CIRCUIT FOR A OUTPUTS LOAD CIRCUIT FOR B OUTPUTS 3 V Timing 1.5 V 3 V Input 0 V 1.5 V Input **VOLTAGE WAVEFORMS** 3 V Data Input **PULSE DURATION** 1.5 V 1.5 V A Port 0 V **VTT** Data Input VREF VREF **B** Port 3 V Input 0 V 1.5 V **VOLTAGE WAVEFORMS SETUP AND HOLD TIMES** tPLH (Vm = 1.5 V for A port and 0.8 V for B port) VOH 3 V Output VREF Output $\mathsf{v}_{\mathsf{REF}}$ VOL Control **VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES** (A to B port) tPLZ 3 V Output Input Waveform 1 1.5 V VOL + 0.3 V S1 at 6 V (see Note B) tpHZ→ **tPLH tPHL** ^tPZH VOH Output VOH V_{OH} – 0.3 V Waveform 2 Output 1.5 V (see Note B) VOL

NOTES: A. CL includes probe and jig capacitance.

VOLTAGE WAVEFORMS

PROPAGATION DELAY TIMES

(B to A port)

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{\rm O}$ = 50 Ω , $t_{\rm f} \leq$ 2.5 ns, $t_{\rm f} \leq$ 2.5 ns.

VOLTAGE WAVEFORMS

ENABLE AND DISABLE TIMES

(A port)

D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



PRODUCT PREVIEW

- EPIC-IIB™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Members of the Texas Instruments
 Widebus™ Family
- Provide GTL Signals Levels on Both inputs and Outputs
- Distributed V_{CC} and GND Pin Configuration
 Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes
 PCB Layout
- Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages, and Ceramic Flat (WD) Package

description

The 'GTL16921 have 20 single-bit flip-flops, which are designed to provide terminated GTL logic levels.

These devices can be used as one 20-bit flip-flop. The 20 flip-flops are edge-triggered D-type flip-flops. The 'GTL16921 provide true data at the Q outputs on the positive transition of the clock (CLK) input.

The output-enable (\overline{OE}) input can be used to place the outputs in a high state. The output-enable input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54GTL16921 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74GTL16921 is characterized for operation from 0°C to 70°C.

SN54GTL16921 ... WD PACKAGE SN74GTL16921 ... DGG OR DL PACKAGE (TOP VIEW)

Q1 [1	\cup_{56}]CLK
Q2 [55	D1
GND [D2
Q3 [53	D3
Q4 [5	52] D4
GND [6	51] GND
Q5 [7] D5
Q6 [49] D6
Q7 [9	48] D7
GND [47]GND
Q8 [11] D8
Q9 [45] D9
Q10 [D10
v _{cc} [14	43]v _{cc}
GND [42	VREF
Q11 [41	OE
Q12 [D11
Q13 [39	D12
GND [D13
Q14 [] GND
Q15 [36	D14
Q16 [D15
GND [D16
Q17 [GND
Q18 [D17
GND [D18
Q19 [D19
Q20 [28	29	D20

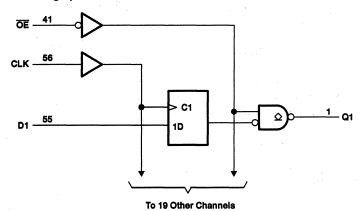
FUNCTION TABLE (each flip-flop)

	INPUTS	OUTPUT	
ŌĒ	CLK	D	Q
L	1	Н	Н
L	1	L	L
L	L	X	Q ₀
н	Х	Х	z

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 4.6 V
Input voltage range, V _I (see Note 1)	
Current into any output in the low state, IO	80 mA
Input clamp current, I _{IK} (V _I < 0)	
Output clamp current, $l_{OK}(V_O < 0 \text{ or } V_O > 0)$	
Continuous current through V _{CC} or GND	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 2): DGG package	
DL package	
Storage temperature range, Teta	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

^{2.} The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

PRODUCT PREVIEW

recommended operating conditions

		SN54GTL16921		SN7	SN74GTL16921				
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
VCC	Supply voltage	3		3.6	3		3.6	٧	
VREF	Supply voltage	0.74	0.8	0.87	0.74	0.8	0.87	٧	
VI	Input voltage	0		VCC	0		VCC	٧	
VOH	High-level output voltage			3.6			3.6	٧	
VIH	High-level input voltage	V _{REF} +50 mV			VREF +50 mV			٧	
VIL	Low-level input voltage		,	VREF - 50 mV		,	VREF - 50 mV	٧	
liK	Input clamp current			-18			-18	mA	
lOL	Low-level output current			40			40	mA	
TA	Operating free-air temperature	-55		125	0		70	ပံ	

electrical characteristics over recommended operating free-air temperature range, V_{REF} = 0.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SNS	SN54GTL16921			SN74GTL16921			
				MIN	TYP	MAX	MIN	TYP	MAX	UNIT	
٧ıĸ		V _{CC} = 3 V,	l _l = –18 mA			-1.2			-1.2	٧	
VOL		V _{CC} = 3 V,	I _{OL} = 40 mA			0.4			0.4	٧	
II		V00 - 2 V	VI = VCC			5		,	5	5 μA	
		V _{CC} = 3 V	V _I = 0			-5			-5	μх	
ЮН		V _{CC} = 3 V,	V _{OH} = 3.6 V							μА	
	Outputs high	V _{CC} = 3 V,	IO = 0,							mA	
Outputs low		V _I = V _{CC} or GND	-					'''^			
Ci		Per IEEE1194.0-1991			4			4		pF	
Co		Per IEEE1194.0-1991			6			6		pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

General Information	1
ALB Widebus™	2
ALVC Widebus™	3
LVT Octals	4
LVTZ Octals: Power Up and 3 State	5
LVT Widebus™	6
LVT JTAG/IEEE 1149.1	7
LVC MSI and Octals	8
LVC Widebus™	9
LV MSI and Octals	10
GTL Transceivers and Backplane Drivers	11
Application Reports	12
Characteristics Information	13
Mechanical Data	14

Contents

	taran da karangan da karangan da karangan da karangan da karangan da karangan da karangan da karangan da karan	aye
Mixing It Up With 3.3 Volts		12-3
Low-Cost, Low-Power Leve	el Shifting in Mixed-Voltage Systems	12-13

Mixing It Up With 3.3 Volts

Ken Ristow Steve Perna Advanced System Logic – Semiconductor Group

SCBA005



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Contents

	Contents	
	Title	Page
Introdu	uction	12–7
The Ma	arket for Low Voltage	12–8
Migrat	tion to 3.3 V	12–8
Mixed-	-Mode Operation	12-9
LVT F	amily Characteristics	12–10
Bus Ho	12–12	
Conclu	ision	12–12
	List of Illustrations	
Figure	Title	Page
1	3-V to 5-V Power Versus Frequency Comparison	12–7
2	Comparison of 3.3-V and 5-V Interfaces	12–9
3	Simplified LVT Output Structure	12–11
4	ABT Versus LVT Output Drive Comparison	12–11

Introduction

The evolution to a 3.3-V supply voltage is being driven by a complex matrix of requirements. Leading the way are the characteristics of advanced semiconductor processing and the need to reduce system power without a corresponding tradeoff in system performance. Reduction of the horizontal and vertical feature sizes of transistors is the most common method of increasing the density of cells that can be contained in an integrated circuit. These feature sizes or geometries are typically represented as minimum process dimensions for advanced products such as dynamic random access memories (DRAMs).

DRAM manufacturers have forecasted that all 64M-bit versions will be developed for operation from a supply voltage of 3.3 ± 0.3 V. For 16M-bit DRAM products, there is no such rule of thumb as certain vendors expect to operate from 3.3 V, while others offer different product versions with differing voltage levels. An approach used by several manufacturers is to provide 5-V power-supply operation externally with internal step-down conversion to 3.3 V. For static random access memories (SRAMs), manufacturers have announced that most 16M versions will operate at 3.3 V or lower (down to 2.7 V).

Typical 1M-bit DRAM geometries are on the order of 1.2 µm and it is not a problem to apply a 5-V power supply to this type of product. However, as the feature sizes of DRAMs shrink, the stresses of 5-V operation can preclude their reliable operation due to high field-effect failures. One such effect is hot-carrier injection that over time increases the transistor's threshold, leading to eventual nonoperation. Another field-effect concern is the breakdown of the transistor's gate oxide causing internal shorts; therefore, reducing the supply voltage is one way to ensure reliable operation of devices fabricated in state-of-the-art processes.

The reduction of V_{CC} from 5 V to 3.3 V reduces the power consumed by the device, which increases system reliability while reducing costs associated with the removal of the heat. The power consumption of a device is primarily a function of its capacitive load, frequency of operation, and supply voltage. However, capacitive load and frequency have a linear effect on a device's power consumption while supply voltage has a square relationship. Because of this square relationship, a small reduction in voltage significantly reduces the power consumed, as illustrated in Figure 1, and is a driving factor to 3.3-V operation.

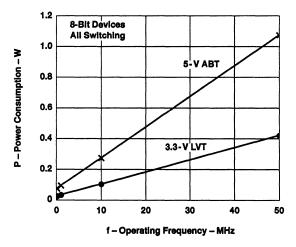


Figure 1. 3-V to 5-V Power Versus Frequency Comparison

The Market for Low Voltage

User demand for low-voltage products can be grouped into specific brackets depending on their performance-power priorities. End equipments, such as multiuser servers, engineering workstations, high-end desktop PCs, and other high-performance motherboards, favor high performance over low power, but are interested in 3.3-V products to reduce or eliminate bulky, noisy cooling fans in the attempt to shrink external case size for better desktop fit. Some end equipments favor low power at the expense of high performance such as battery-powered notebooks and palmtop computers, portable test equipment, and point-of-sale terminals. A few end equipments require equal priority for high performance and low power, such as laptop computers, automotive, and air/space products.

The universal benefits to users of low-voltage products are higher reliability and lower cost. The higher reliability is relative to standard 5-V solutions and results from lower stress gradients on device junctions and oxides, lower buildup of heat due to lower power consumption, and improved signal integrity from the reduction in ground bounce and signal noise. Lower power consumption usually yields lower costs since power costs money to generate and heat costs money to dissipate. All things considered, it is desirable to use inexpensive plastic packages instead of metal or ceramic to dissipate heat. For battery users, an added benefit of the lower power consumption of low-voltage products is one of increased battery lifetime.

Of all the end-equipment groups that can benefit from the use of low-voltage products, it appears that demand will be initially driven by battery-operated computers. This market segment is defined by notebook and palmtop computers, as well as point-of-sale terminals, which are designed to capture data at remote field sites and either store it for downloading later or transmit it real time via an on-board transmitter. The goal for these systems is to have a battery life of eight to ten hours, roughly the equivalent of one workday or the time to complete a transcontinental airplane trip.

The unregulated battery market is itself quite varied however, because different batteries exhibit very different voltage characteristics between fully charged and discharged states. Two AA batteries provide for 3-V supply when charged, decreasing to about 2.7 V after use. Three NiCad batteries provide for a baseline 3.6-V supply fully charged, but the spread actually runs from about 3.3 V up to 3.9 V. For now, the unregulated battery market demands low-voltage products that are optimized to run from 2.7 V up as high as 3.9 V. Since performance is directly related to supply voltage, it is more important for device optimization to be extended down to 2.7 V, where devices slow down appreciably.

There are some barriers for low-voltage acceptance in the short term. Specification standardization remains an issue. Also, the access to adequate supplies of 3.3-V devices can be a problem. Generally, DRAM memories are leading the way into 3.3-V operation with SRAM memories close behind. Coupled with the low-voltage microprocessors now available, systems are being implemented with the core components operating at 3.3 V. Hindering the migration to a full 3.3-V system is the availability of support products such as: disk drives, LCDs, A/D converters, RF transmitters, and EPROMS.

Migration to 3.3 V

The need to migrate to power supplies with supply voltages less than 3.3 V has been an issue since 1984 when two JEDEC standards were adopted. Standard 8.0 was intended to address both regulated (3-V to 3.6-V) and unregulated (2-V to 3.6-V) battery applications. Standard 8.1 was intended to address higher-performance applications operating from a regulated power supply that could interface to a standard 5-V TTL device as well as a low-voltage device. Essentially Standard 8.0 established regulated low-voltage CMOS (LVCMOS) and unregulated low-voltage battery-operated (LVBO) interfaces, and Standard 8.1 established the low-voltage TTL (LVTTL) interface.

Committee members have since determined that the original two standards are inadequate. Since most systems currently require a TTL interface, Standard 8.1 LVTTL is the most critical one being reviewed now. When ratified, the new LVTTL standard will present methods for interfacing with 5-V systems and contain a provision for battery-operated systems. Until this happens, a generic lack of compatibility will exist between the various 3.3-V and 5-V interfaces.

Existing solutions for 3.3-V operation have historically been 5-V products and processes characterized for 3.3-V operation. A CMOS process is typically chosen because of the scaling effect of the inverter thresholds with respect to the supply voltage. HCMOS and Advanced CMOS devices support both 5-V and 3.3-V operation by this method. One drawback is slower propagation delay when compared to parts specifically designed for 3-V operation. A limitation of many of these devices is their inability to directly interface to a 5-V system when running off a 3.3-V supply, due to diodes from the input and input/output (I/O) pins to $V_{\rm CC}$. This limits input voltages to $V_{\rm CC}$ + 0.5 V and limits direct connection to a 5-V system.

Mixed-Mode Operation

This dilemma of device incompatibility between the large installed base of 5-V systems with the newly emerging 3.3-V systems is a serious industry concern. Mixed-mode operation allows for direct communication between the two systems. Devices that support this mode must be designed for maximum input voltages of 5.5 V, without any long-term reliability issues. Another concern is that the output drive must be capable of driving a standard-TTL backplane, while still providing for rail-to-rail switching for compatibility with 3-V CMOS systems.

Figure 2 compares the standard-TTL dc interface levels with two of the emerging low-voltage standards. Low-voltage CMOS (LVCMOS) is a pure CMOS specification that specifies low current rail-to-rail output drive along with input voltage levels, V_{IH} and V_{IL} , which are ratios of V_{CC} . Low-voltage TTL (LVTTL) utilizes the standard-TTL input levels of 0.8 V and 2 V, as well as specifying a higher dc output drive than LVCMOS. To ensure interoperability between these three varied standards, a multipurposed low-voltage interface device must meet all of the requirements of the three different specifications.

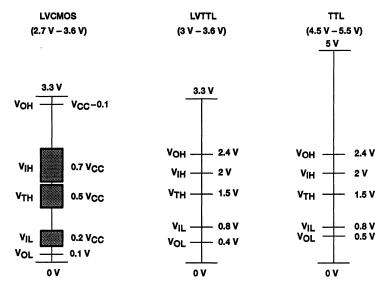


Figure 2. Comparison of 3.3-V and 5-V Interfaces

LVT Family Characteristics

To address the need for a complete low-voltage interface solution, Texas Instruments has developed a new generation of logic devices capable of mixed-mode operation. The LVT series of devices rely on a state-of-the-art submicron BiCMOS process to provide up to a 90% reduction in static power dissipation over ABT devices and provides the following family characteristics:

5.5-V maximum input voltage

Specified 2.7-V to 3.6-V supply voltage

I/O structures that support power-on (live) insertion

Standard TTL output drives of: $V_{OH} = 2 \text{ V}$ at $I_{OH} = -32 \text{ mA}$ $V_{OL} = 0.55 \text{ V}$ at $I_{OL} = 64 \text{ mA}$

Rail-to-rail switching for driving CMOS

Maximum supply currents of:

 $I_{CCL} = 15 \text{ mA}$ $I_{CCH} = 250 \text{ }\mu\text{A}$ $I_{CCZ} = 250 \text{ }\mu\text{A}$

Propagation delays of:

 $t_{pd} < 4.6 \text{ ns}$ t_{pd} (LE to Q) < 5.1 ns t_{pd} (CLK to Q) < 6.3 ns

Surface-mount packaging support including fine-pitch packages:

48- and 56-pin SSOP for LVT Widebus[™] 20- and 24-pin TSSOP for standard LVT

LVT input/output characteristics

Figure 3 shows a simplified LVT output and illustrates the mixed-mode signal drive designed into the output stage. This combination of a high-drive TTL stage with the rail-to-rail CMOS switching gives the LVT series of product extreme application flexibility. These parts have the same drive characteristics as 5-V ABT devices, as shown in Figure 4, providing the dc drive needed for existing 5-V backplanes and allowing for a simple solution to reduce system power via the migration to 3.3-V operation.

Not only can LVT devices operate as 3-V-to-5-V level translators by supporting input or I/O voltages of 5.5 V with $V_{CC} = 2.7 \text{ V}$ to 3.6 V, the inputs can withstand 5.5 V even when $V_{CC} = 0 \text{ V}$. This allows for the devices to be used under partial system power-down applications or when live insertion is required.

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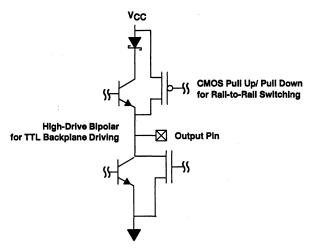


Figure 3. Simplified LVT Output Structure

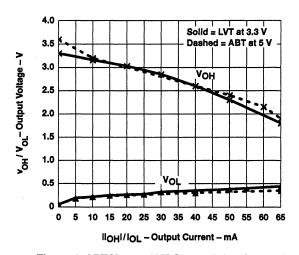


Figure 4. ABT Versus LVT Output Drive Comparison

Bus Hold

Many times devices are used in applications that do not provide a pullup or pulldown voltage to the input or I/O pin when the driving device goes into a high-impedance state, as in the case of CMOS buses or nonbused lines. To prevent application problems or oscillations, a large pullup resistor is typically used, but this consumes board area and contributes to driver loading. The LVT series of devices incorporate active circuitry that holds unused or floating inputs or I/Os at a valid logic level. This circuitry provides for a typical holding current, $\pm 100~\mu$ A, that is sufficient enough to overcome any CMOS-type leakages. Since this is an active circuit, it does take current, approximately $\pm 500~\mu$ A, to toggle the state of the input. This current is negligible when compared to the magnitude of current that is needed to charge a capacitive load and does not affect the propagation delay of the driving output.

Conclusion

LVT devices solve the system need for a transparent interface between the low-voltage and 5-V sections by providing for mixed-signal operation. The devices support live insertion or partial-power applications while providing low-input leakage currents. The outputs are capable of driving today's 5-V backplanes with a considerable reduction in the device's power consumption and are packaged in state-of-the-art fine-pitch surface-mount packages.

Low-Cost, Low-Power Level Shifting in Mixed-Voltage Systems

Mark McClear Advanced System Logic – Semiconductor Group

SCBA002



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Contents

	Title	Page
Introd	uction	12–17
Split-R	Rail Level Shifters	12–17
5-V Tolerant, Pure 3.3-V V _{CC} Level Shifters		12–17
	12–18	
More S	12–21	
Conclu	ision	12–21
		•
	List of Illustrations	
Figure		Page
1	Basic Logic Data Transceiver	
2	Basic CMOS Input Structure and Typical ΔI_{CC} Current	
3	ΔI _{CC} – 16-Bit Device	12–19
4	V _{OH} of FCT164245 and 'LVT16245A	12–20
5	Total System Power Dissipation Impact	
6	LVT Bus-Hold Cell	12–21

Introduction

The increasing demand for lower system power consumption has brought many new design challenges. Among them is the problem of safely and efficiently interfacing the various switching levels in today's mixed 3.3-V and 5-V systems while maintaining the lowest possible total-system power consumption. Two competing methods of accomplishing this mixed-mode signal translation have emerged:

Split-rail or dual 3.3-V and 5-V V_{CC} devices

Completely 5-V tolerant, pure 3.3-V V_{CC} components

This application report deals with the pros and cons of using both device types and offers additional suggestions for even greater system-power savings.

Split-Rail Level Shifters

Split-rail level shifters are a class of transceiver devices that have both a 5-V and 3.3-V V_{CC} rail. Products in this class can be used effectively as level shifters and datapath voltage translators, but the following precautions are usually recommended:

Dual- V_{CC} rail devices typically have strict power sequencing requirements to prevent leakage or even damage to the devices in the event that one V_{CC} rail ramps faster than the other. These stringent requirements are often difficult to meet from a system-timing standpoint and offer little flexibility for partial system power down or other advanced power-saving design techniques.

Simply because the device has a 5-V V_{CC} pin does not necessarily ensure that the part will actually switch all the way to the 5-V rail. Switching to 5 V is one way to reduce the power consumption in 5-V memories or other pure 5-V CMOS circuits that are driven by a level-shifter device (this application report demonstrates others as well).

A quick check of the data sheet for the product in question reveals if the part drives all the way to the 5-V rail. If the output high voltage (V_{OH}) minimum is around 4.44 V, it does drive to the rail. Five-volt level shifters with TTL-compatible outputs typically drive only to around 3.6 V.

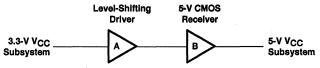
5-V Tolerant, Pure 3.3-V V_{CC} Level Shifters

A second class of products created to meet these design challenges offers the same voltage translation and level-shifting capabilities as the split-rail devices previously mentioned. From a single V_{CC} source, they avoid the power-sequencing problems of the split rails and are also offered in a number of functions, bit widths, and storage options. The one potential drawback of the single- V_{CC} products is that the outputs do not pull all the way to the 5-V V_{CC} rail . . . but is this really a drawback?

The Misconception About ∆I_{CC}

The component selection of a level shifter impacts two major aspects of total system-power dissipation:

The impact that the V_{OH} level of the driving part (A in Figure 1) has on the power dissipation of the receiving device (B in Figure 1), commonly known as ΔI_{CC} , and the power of the device itself.



Note: Unidirectional mode illustrated for simplicity.

Figure 1. Basic Logic Data Transceiver

 ΔI_{CC} is the added power dissipation induced into a TTL-compatible 5-V CMOS device (B in Figure 1) due to the V_{OH} level of the driving device (A in Figure 1). It would correctly be expected that a TTL-compatible 5-V CMOS product have higher power dissipation if it was driven by a device with a V_{OH} of 3.6 V than if that same device was driven by a 5-V V_{OH} driver.

Figure 2 shows a typical CMOS input stage and the ΔI_{CC} current associated with switching the device through the input voltage range from 0 to V_{CC} .

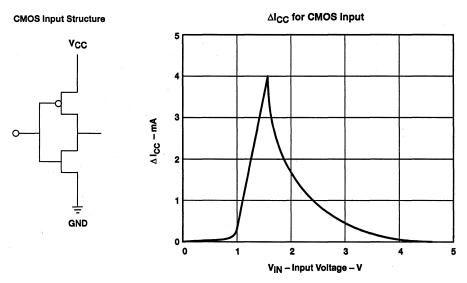


Figure 2. Basic CMOS Input Structure and Typical ∆I_{CC} Current

As expected, the ΔI_{CC} current approaches zero at the V_{CC} and ground rails, and peaks in the TTL-threshold region of 1.5 V.

Figure 3 is a graph of the ΔI_{CC} (i.e., additional I_{CC}) that is induced into a 16-bit device (all outputs switching) as a function of V_{OH} and frequency.

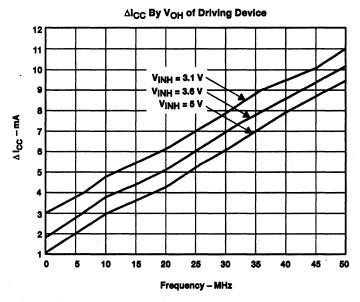


Figure 3. ∆I_{CC} – 16-Bit Device

As shown in Figure 3, ΔI_{CC} is in fact 2 to 3 mA higher for the case where V_{OH} is only 3.1 V than for the same device driven to the 5-V rail by a pure 5-V CMOS device. From this, one might be tempted to conclude that the best possible solution would be to always select a part that switches all the way to the 5-V rail, but this conclusion fails to consider the system-power impact of the driving device.

Figure 4 shows the V_{OH} of two devices: the FCT164245 split-rail device from Integrated Device Technologies and the TVT16245A from Texas Instruments.

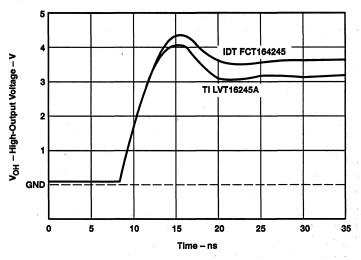


Figure 4. VOH of FCT164245 and 'LVT16245A

From Figure 4, it can be correctly concluded that the induced ΔI_{CC} current in a part driven by the LVT part would be higher than the FCT device. The problem with this conclusion is that ΔI_{CC} is only one of the two components of total-system power dissipation that selection of a level-shifter device has from system standpoint.

Figure 5 shows the total power dissipation of the same IDT split-rail device, the TI LVT16245A, and the worst-case ΔI_{CC} ($V_{OH} = 3.1$ V) graphed on the same vertical scale.

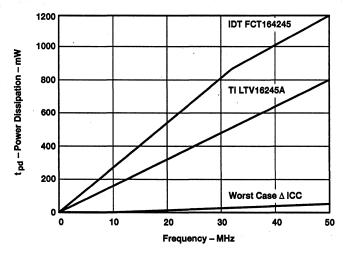


Figure 5. Total-System Power-Dissipation Impact

From Figure 5, it can be seen that even if a split-rail device pulls all the way to the 5-V rail (which the IDT part does not), the power savings in ΔI_{CC} is more than offset by the huge switching currents that the split rail draws from the 5-V rail. The negative implications on heating, reliability, and battery life are obvious.

More Savings Are Possible

Some systems use a means of power savings known as partial power down. In partial power-down mode, a system basically shuts off the V_{CC} to some unused circuits during times of inactivity, thus eliminating even low standby currents. All of the members of TI's low-voltage technology (LVT) product line previously mentioned offer a parametric specification I_{off} , which ensures that the output pins of the parts remain in a high-impedance state when the supply voltage is at 0 V. This prevents an inactive LVT device from dragging down the bus of an active part in the system and allows the LVT part to become a partition for the partially powered-down unused subsystem. The LVT device still functions as a level shifter and voltage translator when power is restored to the inactive subsystem.

Another aspect of system power dissipation is the use of passive resistor pullups to keep a local bus from floating and causing damage to the devices on the bus. Pullups were sufficient for the older desktop systems where power consumption was not as much of a concern, but pullup resistors in portable equipment can have a serious impact on battery life, and as such must be addressed.

Products like the LVT16245A (and others) from TI have a circuit feature called a bus-hold cell (shown in Figure 6). This cell eliminates these passive components and all of the procurement costs, board space, bus parasitics, and, also, power dissipation associated with them. The bus-hold cell does not load down the bus or add any significant power dissipation to the LVT device.

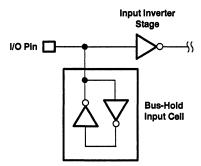


Figure 6. LVT Bus-Hold Cell

Conclusion

Mixed 3.3-V and 5-V systems can be optimized for low power and low cost by the judicious selection of the appropriate voltage-level shifter component. Split-rail level shifters can affect this voltage translation, but selection of this device is burdened with serious design tradeoffs in power sequencing, partial system power down, and system power dissipation. Further savings in both power and component cost can be realized if the component selected has a bus-hold cell or other means of eliminating passive system components.

General Information	1
ALB Widebus™	2
ALVC Widebus™	3
LVT Octals	4
LVTZ Octals: Power Up and 3 State	5
LVT Widebus™	6
LVT JTAG/IEEE 1149.1	7
LVC MSI and Octals	8
LVC Widebus™	9
LV MSI and Octals	10
GTL Transceivers and Backplane Drivers	11
Application Reports	12
Characteristics Information	13
Mechanical Data	14

LVT Family Characteristics

Ken Ristow Advanced System Logic – Semiconductor Group

SCEA002



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Introduction

To address the need for a complete low-voltage interface solution, Texas Instruments has developed a new generation of logic devices capable of mixed-mode operation. The LVT series rely on a state-of-the-art submicron BiCMOS process to provide up to a 90% reduction in static power dissipation over ABT, as well as the following family characteristics:

5.5-V maximum input voltage

Specified 2.7-V to 3.6-V supply voltage

I/O structures which support live insertion

Standard TTL output drives of: V_{OH} = 2 V at I_{OH} = -32 mA V_{OL} = 0.55 V at I_{OL} = 64 mA

Rail-to-rail switching for driving CMOS

Maximum supply currents of: $I_{CCL} \le 15 \text{ mA}$ $I_{CCH} \le 200 \text{ }\mu\text{A}$ $I_{CCZ} \le 200 \text{ }\mu\text{A}$

Propagation delays of: $t_{pd} < 4.6 \text{ ns}$ t_{pd} (LE to Q) < 5.1 ns t_{pd} (CLK to Q) < 6.3 ns

Surface mount packaging support including fine-pitch packages: 48-/56-pin SSOP and TSSOP for LVT WidebusTM 20-/24-pin SOIC and TSSOP for standard LVT

LVT Input/Output Characteristics

Figure 1 shows a simplified LVT output and illustrates the mixed-mode-signal drive designed into the output stage. This combination of a high-drive TTL stage along with the rail-to-rail CMOS switching gives the LVT series of product extreme application flexibility. These parts have the same drive characteristics as 5-V ABT devices (see Figure 2), and provide the dc drive needed for existing 5-V backplanes. This allows for a simple solution to reduce system power via the migration to 3.3-V operation.

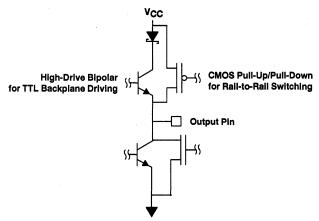


Figure 1. Simplified LVT Output Structure

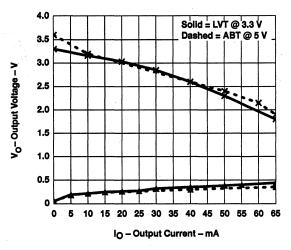


Figure 2. ABT Versus LVT Output-Drive Comparison

Not only can LVT devices operate as 3-V to 5-V level translators by supporting input or I/O voltages of 5.5 V with $V_{CC} = 2.7 \text{ V}$ to 3.6 V, the inputs can withstand 5.5 V even when $V_{CC} = 0 \text{ V}$. This allows for the devices to be used under partial system power-down applications or those which require live insertion.

Bus Hold

Many times, devices are used in applications that do not provide a pullup or pulldown voltage to the input or I/O pin when the driving device goes into a high-impedance state, as in the case of CMOS buses or nonbused lines. To prevent application problems or oscillations, a large pullup resistor is typically used, but this consumes board area and contributes to driver loading. The LVT series of devices incorporate active circuitry that holds unused or floating inputs or I/Os at a valid logic level. This circuitry provides for a typical holding current, $\pm 100~\mu$ A, that is sufficient enough to overcome any CMOS-type leakages. Since this is an active circuit, it does take current, approximately $\pm 500~\mu$ A, to toggle the state of the input. This current is trivial when compared to the tens of mA of current that is needed to charge a capacitive load, thereby not affecting the propagation delay of the driving output.

Conclusion

LVT devices solve the system need for a transparent seam between the low-voltage and 5-V sections by providing for mixed-signal operation. The devices support live-insertion or partial-power applications, while providing for low-input leakage currents. The outputs are capable of driving today's 5-V backplanes, with a considerable reduction in device power consumption, as well as being packaged in state-of-the-art fine-pitch surface-mount packages.

Widebus is a trademark of Texas Instruments Incorporated.

'LVT244 Characteristics

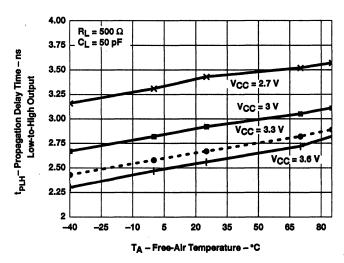


Figure 3. Propagation Delay Versus Free-Air Temperature

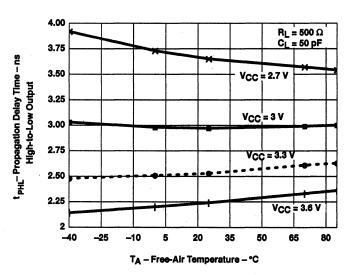


Figure 4. Propagation Delay Versus Free-Air Temperature

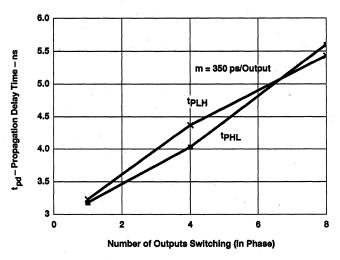


Figure 5. Propagation Delay Versus Outputs Switching

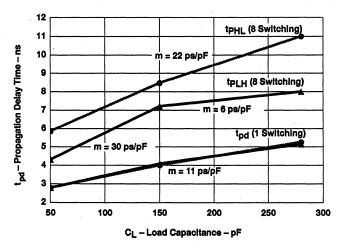


Figure 6. Propagation Delay Versus Load Capacitance

LVT244 Typical dc Characteristics

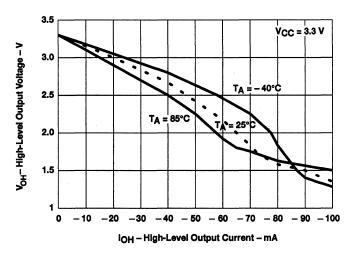


Figure 7. High-Level Output Voltage Versus High-Level Output Current

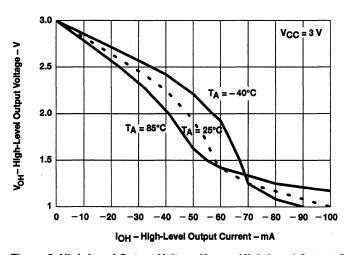


Figure 8. High-Level Output Voltage Versus High-Level Output Current

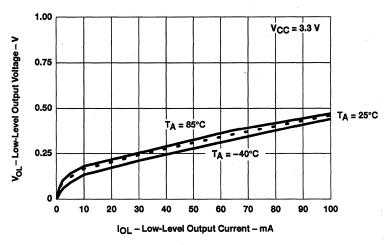


Figure 9. Low-Level Output Voltage Versus Low-Level Output Current

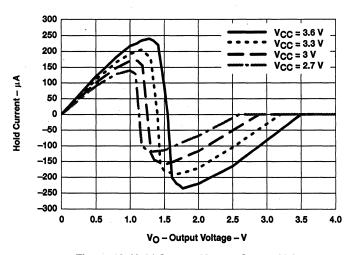


Figure 10. Hold Current Versus Output Voltage

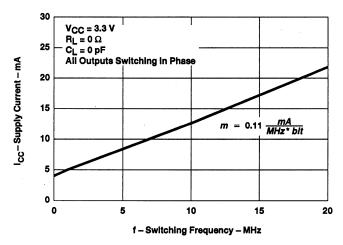


Figure 11. Supply Current Versus Switching Frequency

Unloaded t_r and t_f Rates

The circuit shown in Figure 12 was used to measure the unloaded transition rates of the output.

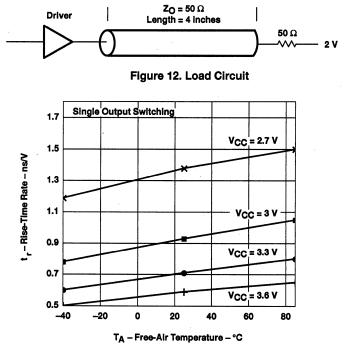


Figure 13. Rise-Time Rate Versus Free-Air Temperature

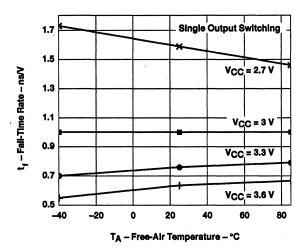


Figure 14. Fall-Time Rate Versus Free-Air Temperature

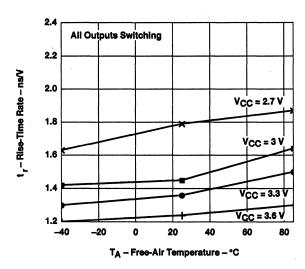


Figure 15. Rise-Time Rate Versus Free-Air Temperature

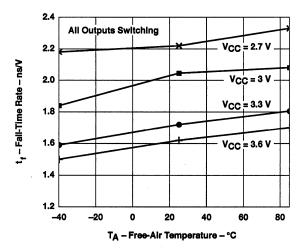


Figure 16. Fall-Time Rate Versus Free-Air Temperature

'LVT646 Characteristics

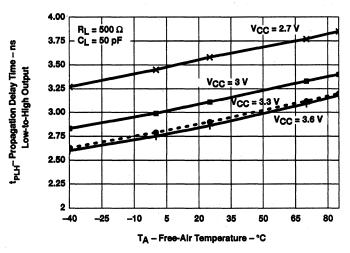


Figure 17. Through-Mode Propagation Delay Versus Free-Air Temperature

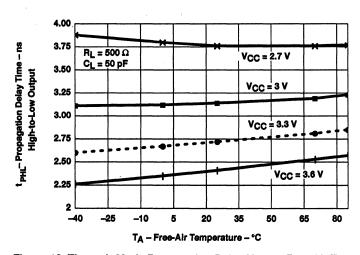


Figure 18. Through-Mode Propagation Delay Versus Free-Air Temperature

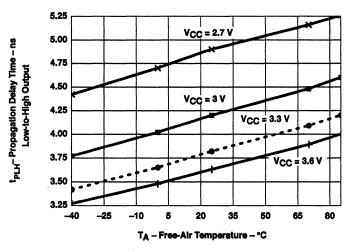


Figure 19. Clock-to-Q Propagation Delay Versus Free-Air Temperature

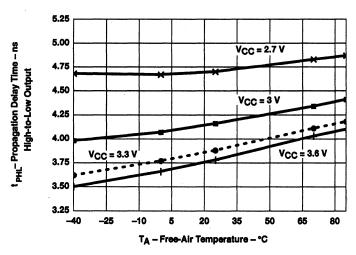


Figure 20. Clock-to-Q Propagation Delay Versus Free-Air Temperature

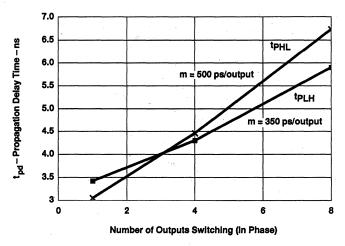


Figure 21. Propagation Delay Versus Outputs Switching

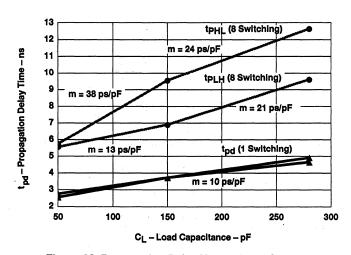
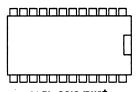


Figure 22. Propagation Delay Versus Load Capacitance

Packaging Options



24-Pin SOIC (DW)†
Area = 165 mm²
Height = 2.65 mm
Lead pitch = 1.27 mm



24-Pin TSSOP (PW)† Area = 54 mm² Height = 1.1 mm Lead Pitch = 0.65 mm

† TI package designators

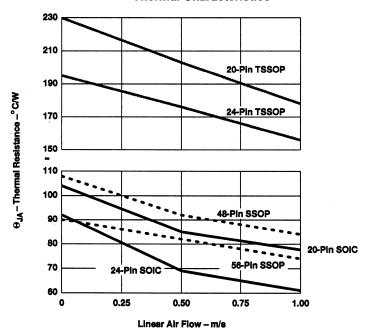


48-Pin SSOP (DL)[†] Area = 171 mm² Height = 2.74 mm Lead pitch = 0.635 mm



48-Pin TSSOP (DGG)† Area = 108 mm² Height = 1.1 mm Lead Pitch = 0.5 mm

Thermal Characteristics



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General Information	1
ALB Widebus™	2
ALVC Widebus™	3
LVT Octals	4
LVTZ Octals: Power Up and 3 State	5
LVT Widebus™	6
LVT JTAG/IEEE 1149.1	7
LVC MSI and Octals	8
LVC Widebus™	9
LV MSI and Octals	10
GTL Transceivers and Backplane Drivers	11
Application Reports	12
Characteristics Information	13
Mechanical Data	14

Contents

		Page
Ordering Instructions		
Mechanical Data		14-5
D (R-PDSO-G**)		14-5
DB (R-PDSO-G**)		14-6
DGG (R-PDSO-G**)		14-7
DL (R-PDSO-G**)		14-8
DW (R-PDSO-G**)		
FK (S-CQCC-N**)		14-10
HV (S-GDFP-F68)	• • • • • • • • • • • • • • • • • • • •	14-11
J (R-GDIP-T**)		14-12
JT (R-GDIP-T**)		14-13
PM (S-PQFP-G64)		14-14
PW (R-PDSO-G**)		14-15
WD (R-GDFP-F**)	• • • • • • • • • • • • • • • • • • • •	14-16

741 VTO44 A

. =

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a three-part type number as explained in the following example.

EVAMBLE.

	EXAMPLE:	SN	74LVT244A	PW	LE
Prefix		/			
MUST CONTAIN TWO TO FOUR LETTERS				/	
SN = Standard prefix SNJ = MIL-STD-883 processed and screened per JEDEC Standard 101					
Unique Circuit Description		_		/	
MUST CONTAIN SIX TO TWELVE CHARACTERS		/	/ /		
Examples: 74LV00 74LVT244A 74ALVCH16244					
Package —————	/	,			
MUST CONTAIN ONE TO THREE LETTERS					
D, DW = plastic small-outline package DB, DL = plastic shrink small-outline package DGG, PW = plastic thin shrink small-outline package FK = leadless ceramic chip carrier	/				
HV = ceramic quad flat package J, JT = dual-in-line package					
PM = plastic quad flat package					
WD = ceramic flat package (from pin-connection diagram on individual data sheet)					
Tape and Reel Packaging	•				

Valid for surface-mount packages only. All orders for tape and reel must be for whole reels.

MUST CONTAIN ONE OR TWO LETTERS

LE = Left embossed tape and reel (required for DB and PW packages)

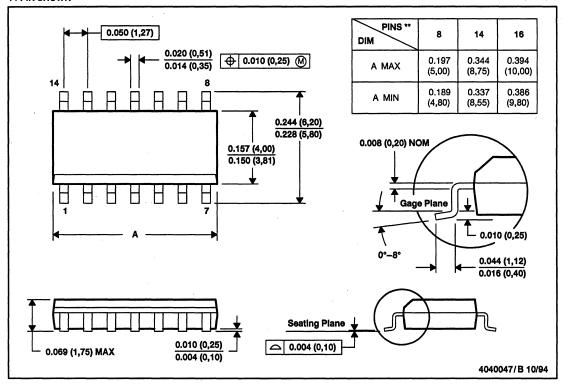
= Standard tape and reel (required for DGG; optional for D, DW, and DL packages)



D (R-PDSO-G**)

14 PIN SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Four center pins are connected to die mount pad.
 - E. Falls within JEDEC MS-012

DB (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE 28 PIN SHOWN 0,38 0,22 ⊕ 0,15 M 0,15 NOM 5,00 Gage Plane 0,25 1,03 0,63 Seating Plane 2,00 MAX 0,05 MIN **△** 0,10 PINS ** 14 16 20 24 28 30 38 DIM A MAX 6,50 10,50 10,50 12,90 6,50 7,50 8,50 A MIN 5,90 5,90 6,90 7,90 9,90 9,90 12,30 4040065 / B 10/94

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

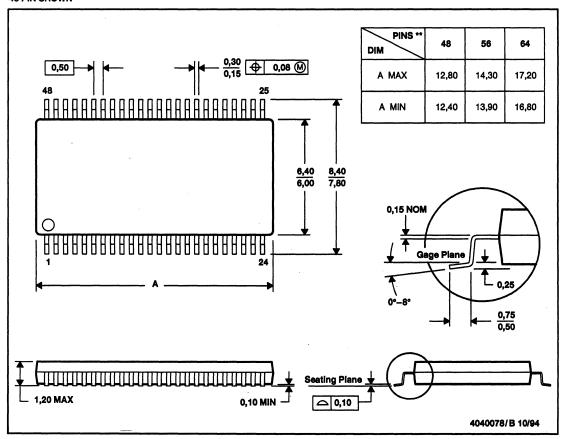
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PIN SHOWN



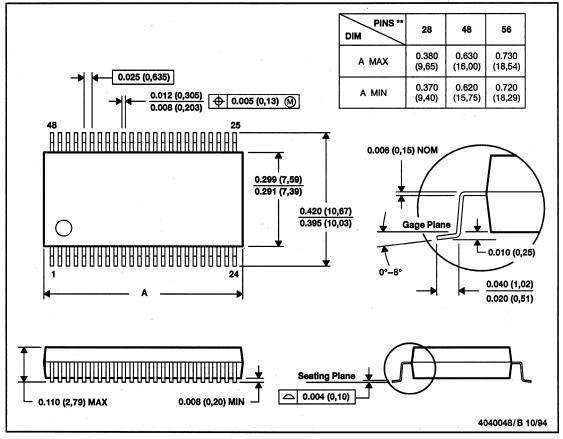
NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

DL (R-PDSO-G**)

48 PIN SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

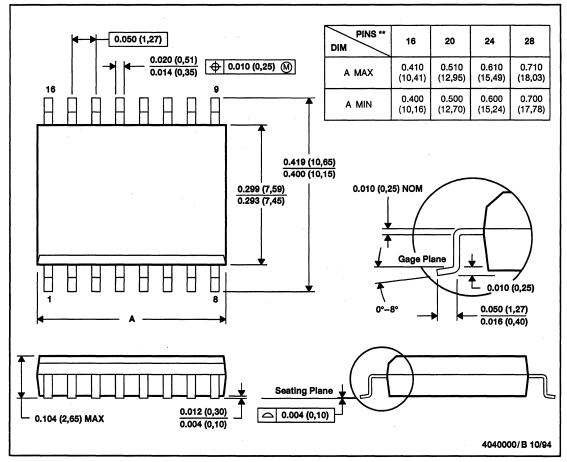
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

DW (R-PDSO-G**)

D ... (...) ...

PLASTIC SMALL-OUTLINE PACKAGE

16 PIN SHOWN



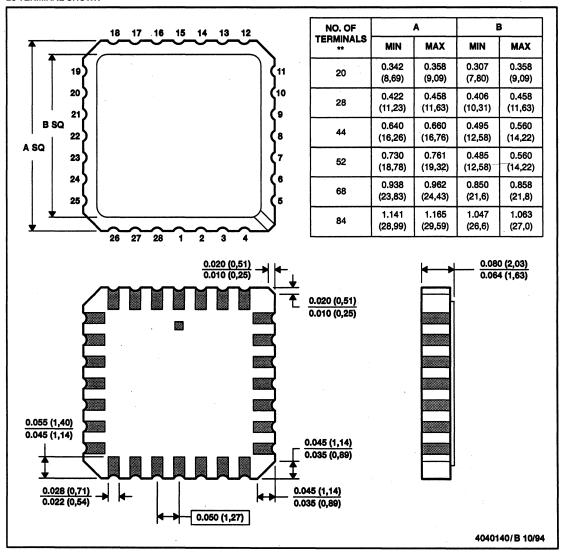
NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES: A. All linear dimensions are in inches (millimeters).

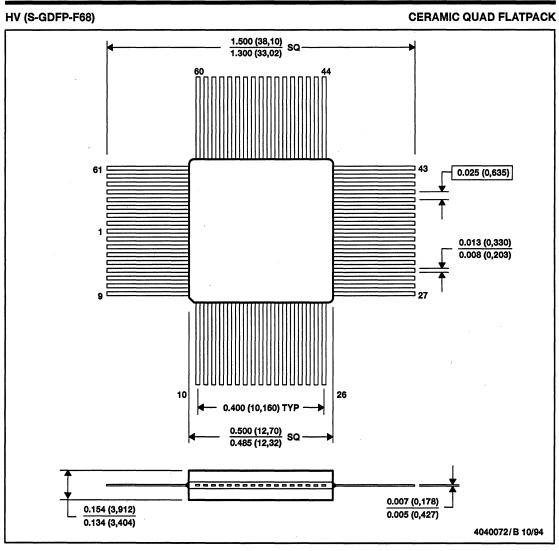
B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a metal lid.

D. The terminals are gold plated.

E. Falls within JEDEC MS-004



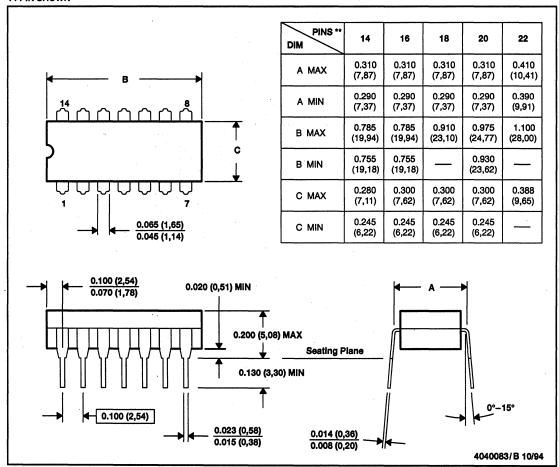


NOTES: A. All linear dimensions are in inches (millimeters). B. This drawing is subject to change without notice.

J (R-GDIP-T**)

14 PIN SHOWN

CERAMIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a ceramic lid using glass frit.

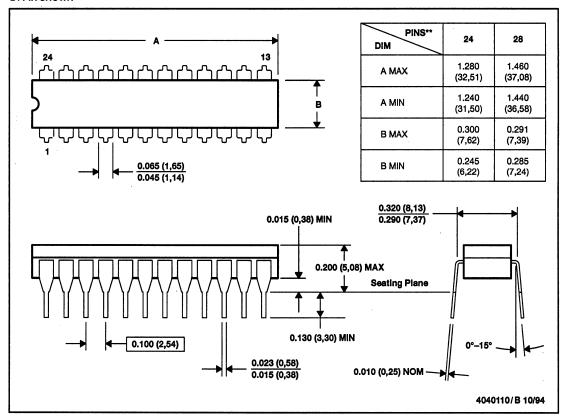
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.

E. Falls within MIL-STD-1835 GDIP1-T14, GDIP1-T16, GDIP1-T18, GDIP1-T20, and GDIP1-T22

JT (R-GDIP-T**)

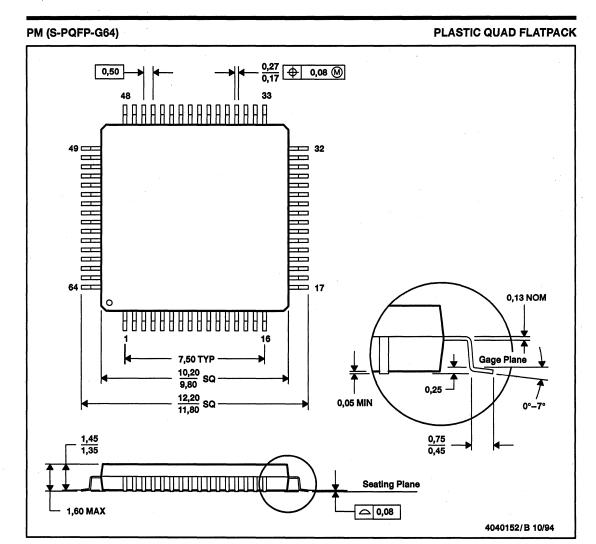
24 PIN SHOWN

CERAMIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL-STD-1835 GDIP-T24 and GDIP-T28 and JEDEC MO-058AA and MO-058AB



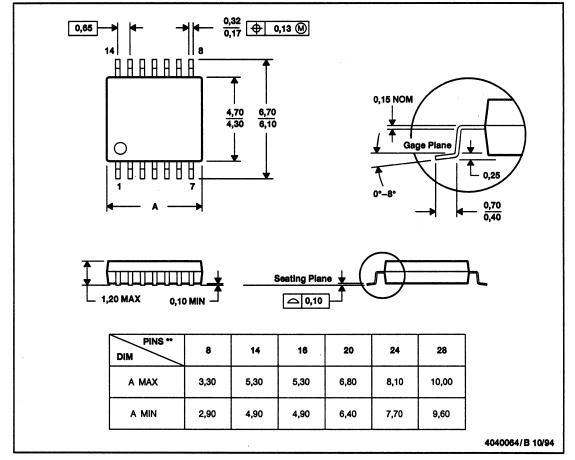
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-136

PW (R-PDSO-G**)

14 PIN SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

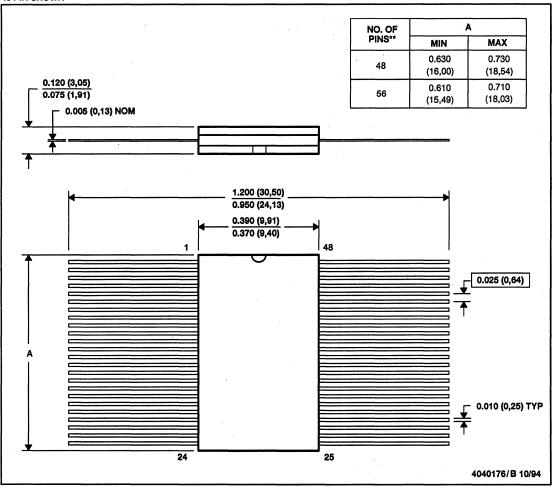
B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

WD (R-GDFP-F**)

CERAMIC DUAL FLATPACK

48 PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for pin identification only.
- E. Falls within MIL-STD-1835: GDFP1-F48 and JEDEC MO-146AA

GDFP1-F56 and JEDEC MO-146AB

NOTES

NOTES

NOTES

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