High-Speed Memory Interface Logic Data Book

Address Drivers, Data Transceivers, Clock Drivers, and Synchronous DRAMs

Printed on Recycled Paper

INTRODUCTION

Texas Instruments (TI) Advanced System Logic group has a broad portfolio of devices designed for high-speed memory interfacing. Sections 2, 3, and 4–Data Transceivers/Multiplexers, Address Buffers/Latches/Flip-Flops, and Clock-Distribution Circuits–contain devices that have set the industry standards for fast propagation-delay speeds, bus hold, and low simultaneous-switching noise. Device families within this text include:

ALVC – One of the highest-performance 3.3-V bus-interface device families is ALVC. These specially designed 3.3-V products are processed in 0.6-μ CMOS technology, giving propagation of delays less than 3 ns, along with current drive of 24 mA and static power consumption of 40 μA for bus-interface functions. The ALVC devices have bus-hold cells on inputs to eliminate the need for external pullup/pulldown resistors for floating inputs. The family also includes innovative functions with integrated series-damping resistors for memory interleaving, multiplexing, and interfacing to synchronous DRAMS.

SSTL – TI is the first to offer interface logic based on the new SSTL_3 (stub series terminated logic) standard. With both an address driver and a clock driver that conform to this standard, TI continues to innovate logic for future generations of SDRAM.

LVT – The specially designed 3.3-V LVT family uses the latest 0.8-μ BiCMOS-process technology for bus-interface functions. LVT can provide up to 24 mA of drive, 4-ns propagation delays, and, in addition, consumes less than 100 μA of standby current. The inputs have the bus-hold feature to eliminate the need for external pullup/pulldown resistors and I/Os that can tolerate up to 7 volts, which can allow them to act as 5-V/3.3-V translators.

ALB – The specially designed 3.3-V ALB family uses the latest in 0.6-μ technology for bus-interface functions. ALB provides 25 mA of drive at 3.3 V and boasts a maximum propagation delay of 2.2 ns, making it the fastest TI logic family to date. The inputs have clamping diodes to eliminate signal overshoot and undershoot.

CDC – TI's CDCs provide accurate clock-generation circuitry fundamental to every digital system, producing timing signals that are used to synchronize system activity. To meet the stringent clock-signal timing requirements of today's systems, TI offers a series of low-propagation delay and skew, high-fan-out clock drivers designed to effectively drive high-performance clocking systems.

CBT – The CBT (crossbar technology) family is the industry's bus switch of choice. CBT enables a bus-interface device to function in one of two valuable roles. When the switch is closed, it is a very fast bus switch , effectively isolating buses. When the switch is open, it offers very little propagation delay. These devices can function as high-speed bus interfaces for computer-system components such as the central processing unit (CPU) and memory.

For more information on these or other TI products, please contact your local TI representative, authorized distributor, the TI technical support hotline at 972-644-5580, or visit the TI home page at http://www.ti.com.

For a complete listing of all TI logic products, please order the Logic Selection Guide (literature number SDYU001) by calling our literature response center at 1-800-477-8924.

Contents

INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

operating conditions and characteristics (in sequence by letter symbols)

C_i **Input capacitance**

The internal capacitance at an input of the device

C_{io} **Input/output capacitance**

Input-to-output internal capacitance; transcapacitance

C_o **Output capacitance**

The internal capacitance at an output of the device

C_{pd} **Power dissipation capacitance**

Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$

f_{max} **Maximum clock frequency**

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification

I_{CC} **Supply current**

The current into* the V_{CC} supply terminal of an integrated circuit

ΔI_{CC} **Supply current change**

The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}

I_{CEX} **Output high leakage current**

The maximum leakage current into the collector of the pulldown output transistor when the output is high and the output forcing condition $V_O = 5.5$ V

$I_{I(hold)}$ **Input hold current**

Input current that holds the input at the previous state when the driving device goes to a high-impedance state

I_{IH} **High-level input current**

The current into* an input when a high-level voltage is applied to that input

I_{IL} **Low-level input current**

The current into* an input when a low-level voltage is applied to that input

I_{off} **Input/output power-off leakage current**

The current into a circuit mode when the device or a portion of the device affecting that circuit node is in the off state

I_{OH} **High-level output current**

The current into* an output with input conditions applied that, according to the product specification, establish a high level at the output

*Current out of a terminal is given as a negative value.

t_{PHL} **Propagation delay time, high-to-low level output**

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level

t_{PHZ} **Disable time (of a 3-state output) from high level**

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to the high-impedance (off) state

t_{PLH} **Propagation delay time, low-to-high level output**

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level

t_{PLZ} **Disable time (of a 3-state output) from low level**

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined low level to the high-impedance (off) state

t_{PZH} **Enable time (of a 3-state output) to high level**

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined high leve

t_{PZL} **Enable time (of a 3-state output) to low level**

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined low level

$t_{sk(I)}$ **Input skew**

The difference between any two propagation delay times that originate at different inputs and terminate at a single output. Input skew describes the ability of a device to manipulate (stretch, shrink, or chop) a clock signal. This is typically accomplished with a multiple-input gate wherein one of the inputs acts as a controlling signal to pass the clock through. $t_{sk(I)}$ describes the ability of the gate to shape the pulse to the same duration regardless of the input used as the controlling input.

$t_{sk(I)}$ **Limit skew**

The difference between 1) the greater of the maximum specified values of t_{PLH} and t_{PHL} and 2) the lesser of the minimum specified values of t_{PLH} and t_{PHL}. Limit skew is not directly observed on a device but rather is calculated from the data sheet limits for t_{PLH} and t_{PHL}. $t_{sk(I)}$ quantifies for the designer how much variation in propagation delay time will be induced by operation over the entire ranges of supply voltage, temperature, output load, and other specified operating conditions. Specified as such, $t_{sk(i)}$ also accounts for process variation. In fact, all other skew specifications [$t_{sk(o)}$, $t_{sk(i)}$, $t_{sk(p)}$, and $t_{sk(pr)}$] are subsets of $t_{sk(i)}$; they are never greater than $t_{sk(i)}$.

$t_{sk(o)}$ **Output Skew**

The difference between any two propagation delay times when a single switching input or multiple inputs switching simultaneously cause multiple outputs to switch, as observed across all switching outputs. This parameter is used to describe the fanout capability of a clock driver and is of concern when making decisions on clock buffering and distribution networks.

$t_{sk(p)}$ **Pulse Skew**

The difference between propagation delay times t_{PHL} and t_{PLH} when a single switching input causes one or more outputs to switch. $t_{sk(p)}$ quantifies the duty cycle characteristic of a clock driver. Certain applications require a fixed duty cycle for proper operation. As an example, the CLK2 input of an MC68020 processor operating at 40 MHz requires a duty cycle of 50 ± 5%. $t_{sk(p)}$ is a measure of a clock driver's ability to supply such a precisely controlled pulse.

The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
↶	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state output
a . . . h	=	the level of steady-state inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$	=	complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
⎍	=	one high-level pulse
⎾	=	one low-level pulse
Toggle	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑

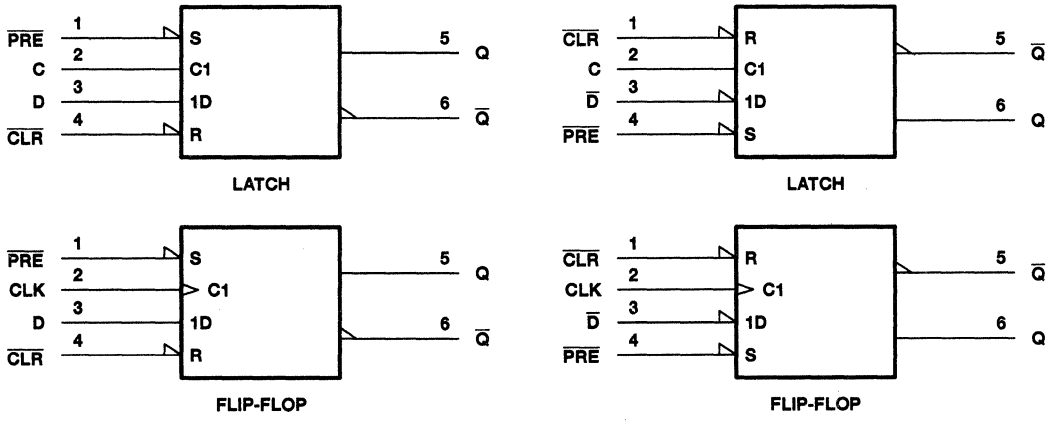
If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎾, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called preset (PRE). An input that causes a $\overline{Q}$ output to go high or a Q output to go low is called clear (CLR). Bars are used over these pin names (PRE and CLR) if they are active low.

The devices on several data sheets are second-source designs, and the pin name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits $\overline{D}$ and Q.

In some applications, it may be advantageous to redesignate the data input from D to $\overline{D}$ or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown.



The figures show that when Q and $\overline{Q}$ exchange names, the preset and clear pins also exchange names. The polarity indicators (⊵) on $\overline{PRE}$ and $\overline{CLR}$ remain, as these inputs are still active low, but the presence or absence of the polarity indicator changes at D (or $\overline{D}$), Q, and $\overline{Q}$. Pin 5 (Q or $\overline{Q}$) is still in phase with the data input (D or $\overline{D}$); their active levels change together.

DERATING CURVES FOR 210-MIL SHRINK SMALL-OUTLINE PACKAGE (DB)

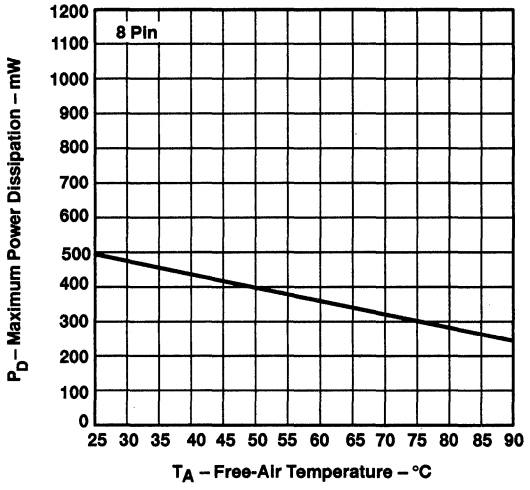


Figure 2

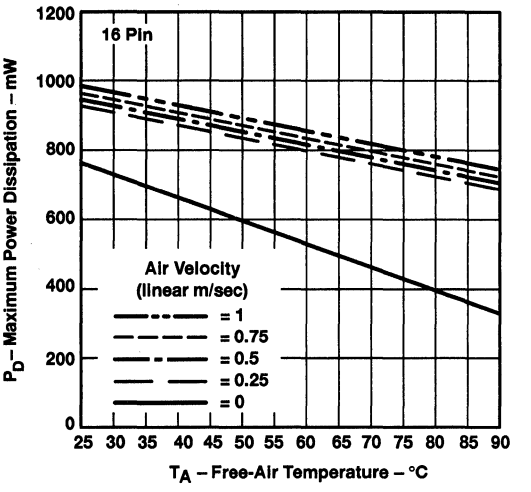


Figure 3

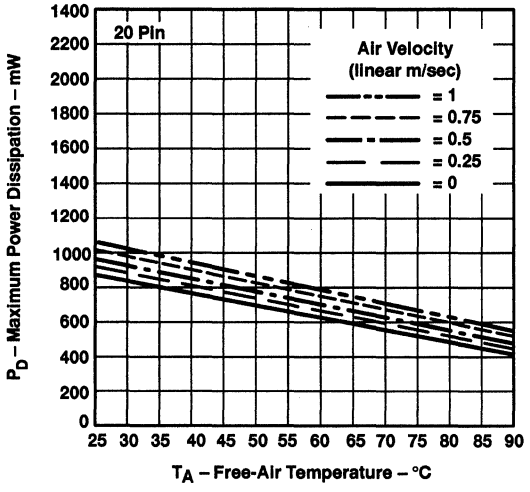


Figure 4

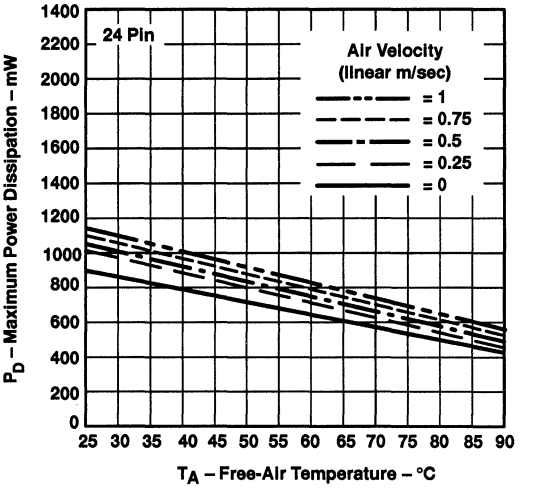
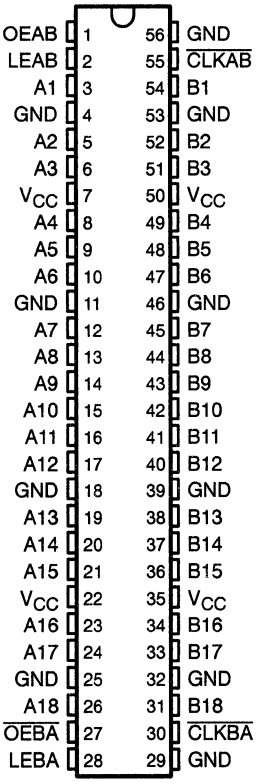


Figure 5

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 18-bit universal bus transceiver is designed for 2.3-V to 3.6-V V_{CC} operation.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock ($\overline{CLKAB}$ and $\overline{CLKBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CLKAB}$ is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of $\overline{CLKAB}$. Output-enable OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$. The output enables are complementary (OEAB is active high, and $\overline{OEBA}$ is active low).

To ensure the high-impedance state during power up or power down, $\overline{OEBA}$ should be tied to V_{CC} through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16500 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16500 is characterized for operation from –40°C to 85°C.

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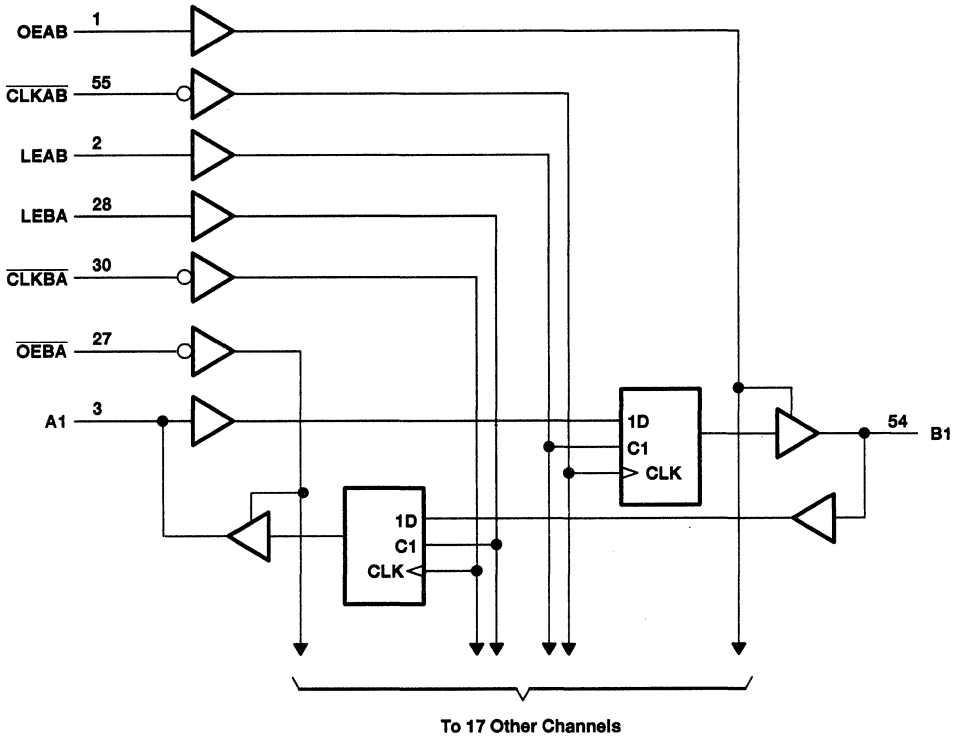
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, VI: Except I/O ports (see Note 1) ..... –0.5 V to 4.6 V
I/O ports (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	0	150	MHz
t_w	Pulse duration	LE high	3.3		3.3		3.3		ns
		$\overline{CLK}$ high or low	3.3		3.3		3.3		
t_{su}	Setup time	Data before $\overline{CLK}\downarrow$	1.7		1.4		1.3		ns
		Data before LE↓, $\overline{CLK}$ high	1.1		1		1		
		Data before LE↓, $\overline{CLK}$ low	1.9		1.6		1.4		
t_h	Hold time	Data after $\overline{CLK}\downarrow$	1.7		1.6		1.3		ns
		Data after LE↓, $\overline{CLK}$ high	2		1.8		1.5		
		Data after LE↓, $\overline{CLK}$ low	1.6		1.5		1.2		

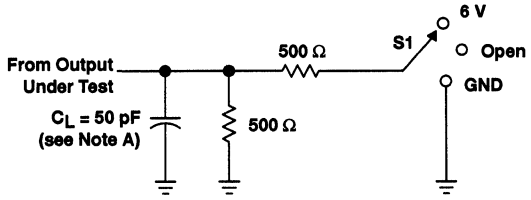
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			150		150		150		MHz
t_{pd}	A or B	B or A	1	5.7		4.7	1	3.9	ns
	LEAB or LEBA	A or B	1	6.5		5.5	1	4.7	
	$\overline{CLKAB}$ or $\overline{CLKBA}$	A or B	1	7.2		6.6	1.1	5.5	
t_{en}	OEAB	B	1	6.2		5.4	1	4.6	ns
t_{dis}	OEAB	B	1.7	6.3		5.7	1.5	5	ns
t_{en}	$\overline{OEBA}$	A	1	6.7		6.2	1	5.2	ns
t_{dis}	$\overline{OEBA}$	A	1	5.6		4.6	1	4.3	ns

operating characteristics, T_A = 25°C

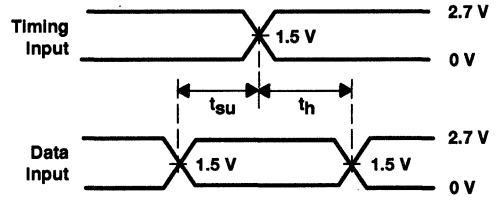
PARAMETER			TEST CONDITIONS	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 10 MHz	40	51	pF
		Outputs disabled		6	6	

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V

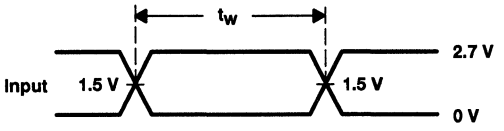


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

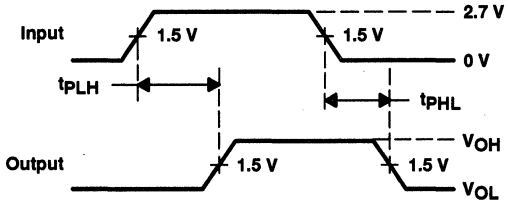
LOAD CIRCUIT



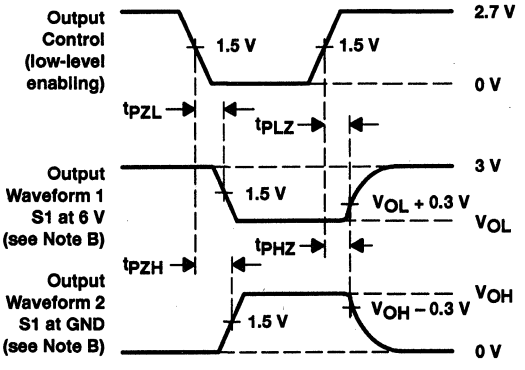
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



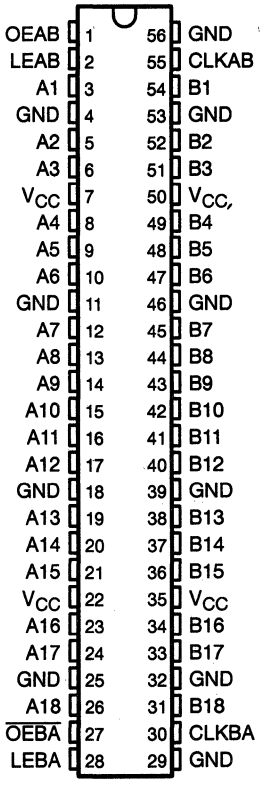
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 18-bit universal bus transceiver is designed for 2.3-V to 3.6-V V_{CC} operation.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OEBA}$ should be tied to V_{CC} through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

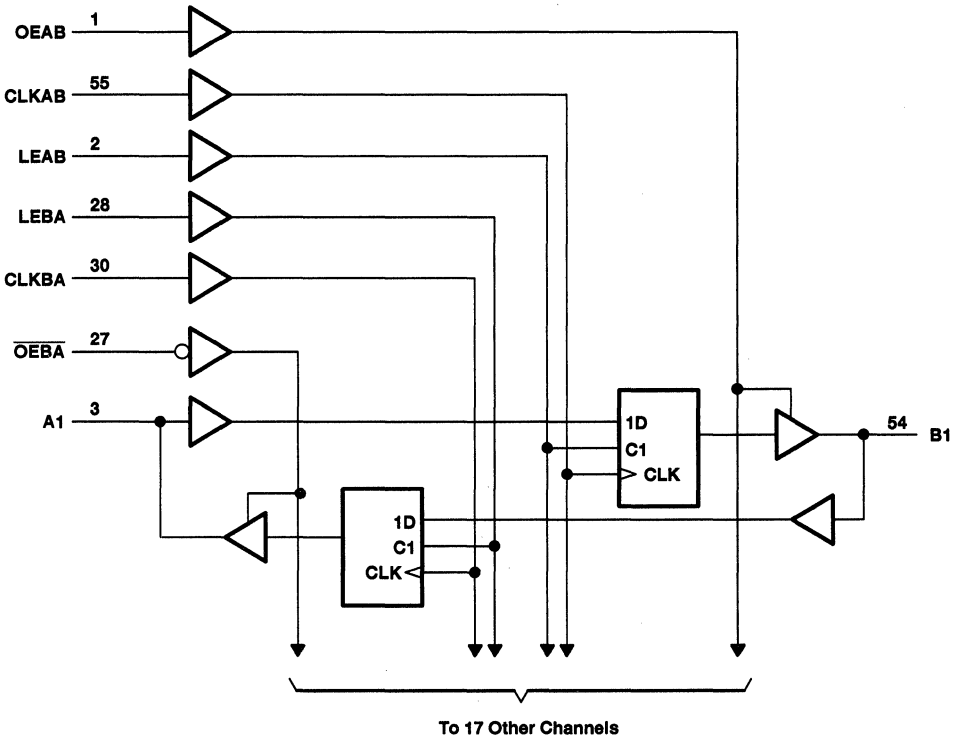
Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and $\overline{OEBA}$ is active low).

The SN74ALVCH16501 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16501 is characterized for operation from –40°C to 85°C.

EPIC, UBT, and Widebus are trademarks of Texas Instruments Incorporated.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I: Except I/O ports (see Note 1) ..... –0.5 V to 4.6 V
I/O ports (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	0	150	MHz
t_w	Pulse duration	LE high	3.3		3.3		3.3		ns
		CLK high or low	3.3		3.3		3.3		
t_{su}	Setup time	Data before CLK↑	2.2		2.1		1.7		ns
		Data before LE↓, CLK high	1.9		1.6		1.5		
		Data before LE↓, CLK low	1.3		1.1		1		
t_h	Hold time	Data after CLK↑	0.6		0.6		0.7		ns
		Data after LE↓, CLK high or low	1.4		1.7		1.4		

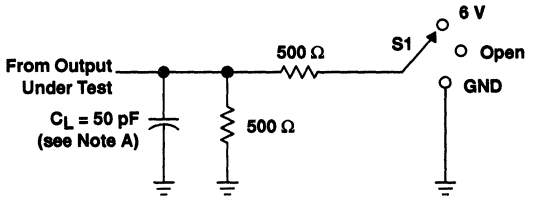
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			150		150		150		MHz
t_{pd}	A or B	B or A	1.2	5.4	4.5		1	3.9	ns
	LE	A or B	1.6	6.3	5.3		1.3	4.6	
	CLK	A or B	1.7	6.7	5.6		1.4	4.9	
t_{en}	OEAB	B	1.1	6.3	5.3		1	4.6	ns
t_{dis}	OEAB	B	2.2	6.4	5.7		1.4	5	ns
t_{en}	$\overline{OEBA}$	A	1.4	6.8	6		1.1	5	ns
t_{dis}	$\overline{OEBA}$	A	2	5.5	4.6		1.3	4.2	ns

operating characteristics, T_A = 25°C

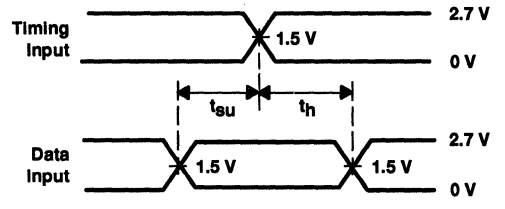
PARAMETER			TEST CONDITIONS	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 10 MHz	44	54	pF
		Outputs disabled		6	6	

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V

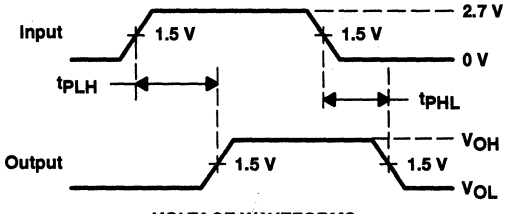


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

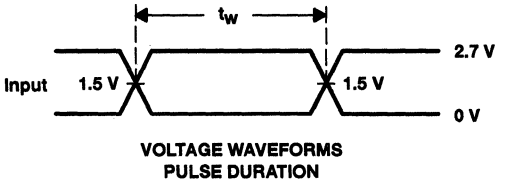
LOAD CIRCUIT



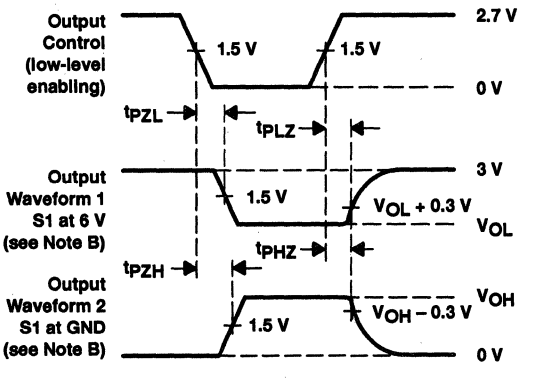
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



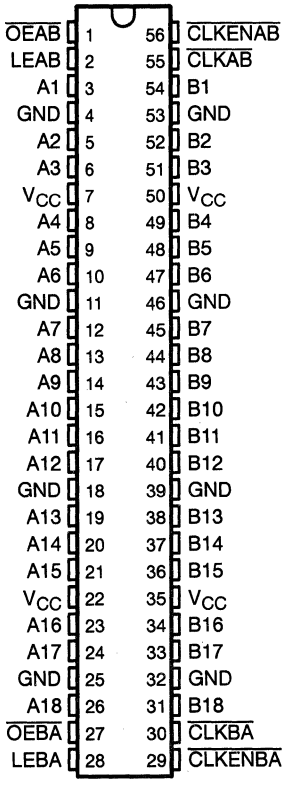
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 18-bit universal bus transceiver is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16600 combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock ($\overline{CLKAB}$ and $\overline{CLKBA}$) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CLKAB}$ is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of $\overline{CLKAB}$. Output enable $\overline{OEAB}$ is active low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, $\overline{CLKBA}$, and $\overline{CLKENBA}$.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16600 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16600 is characterized for operation from –40°C to 85°C.

EPIC, UBT, and Widebus are trademarks of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, VI: Except I/O ports (see Note 1) ..... –0.5 V to 4.6 V
I/O ports (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book.*

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		–12	mA
		V_{CC} = 2.7 V		–12	
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		12	mA
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

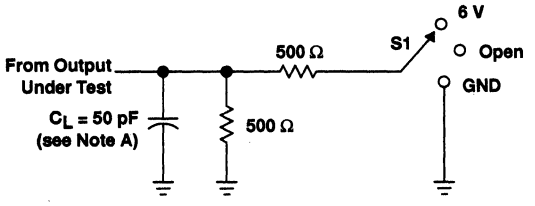
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			150		150		150		MHz
t_{pd}	A or B	B or A	1	5.7		4.7	1	4	ns
	LEAB or LEBA	A or B	1	6.5		5.5	1	4.8	
	$\overline{CLKAB}$ or $\overline{CLKBA}$	A or B	1.4	7.9		6.8	1.3	5.7	
t_{en}	$\overline{OEAB}$ or $\overline{OEBA}$	A or B	1.1	7.1		6.3	1.1	5.2	ns
t_{dis}	$\overline{OEAB}$ or $\overline{OEBA}$	A or B	1.7	5.7		4.7	1.2	4.4	ns

operating characteristics, T_A = 25°C

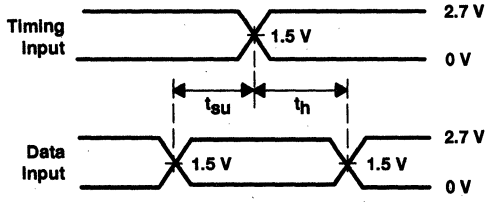
PARAMETER			TEST CONDITIONS	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 10 MHz	43	56	pF
		Outputs disabled		6	6	

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V

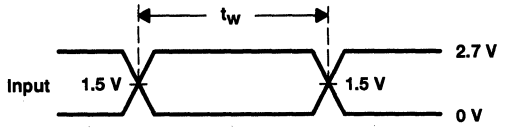


LOAD CIRCUIT

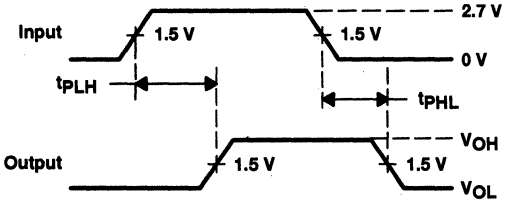
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



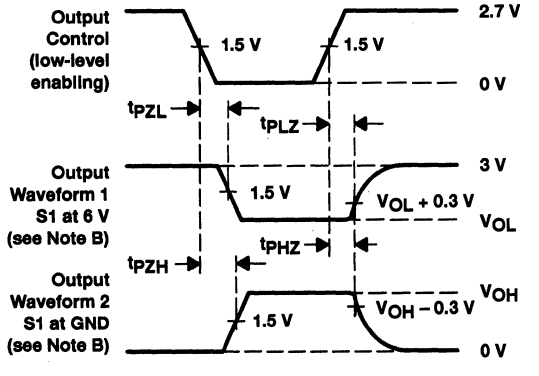
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



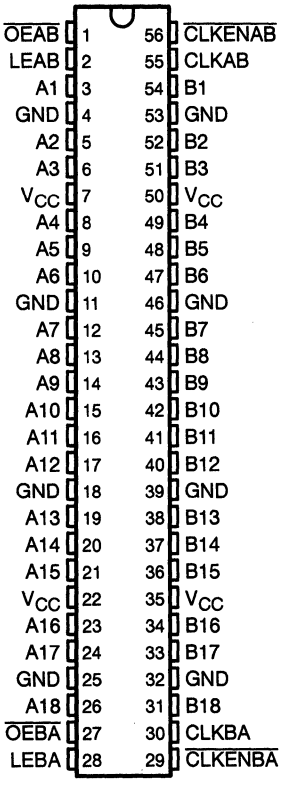
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 18-bit universal bus transceiver is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16601 combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Output enable $\overline{OEAB}$ is active low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CLKENBA}$.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16601 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16601 is characterized for operation from –40°C to 85°C.

EPIC, UBT, and Widebus are trademarks of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, VI: Except I/O ports (see Note 1) ..... –0.5 V to 4.6 V
I/O ports (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		–12	mA
		V_{CC} = 2.7 V		–12	
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		12	mA
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

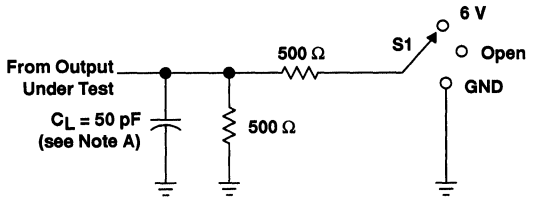
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			150		150		150		MHz
t_{pd}	A or B	B or A	1.3	4.9		4.6		4.1	ns
	LEAB or LEBA	A or B	1.2	5.6		5.3		4.7	
	CLKAB or CLKBA	A or B	1.7	6.2		5.8		5	
t_{en}	$\overline{OEAB}$ or $\overline{OEBA}$	A or B	1.2	6.1		6.1		5.2	ns
t_{dis}	$\overline{OEAB}$ or $\overline{OEBA}$	A or B	2.1	5.4		4.8		4.4	ns

operating characteristics, T_A = 25°C

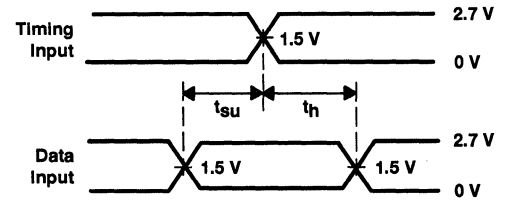
PARAMETER			TEST CONDITIONS	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 10 MHz	41	52	pF
		Outputs disabled		6	6	

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V

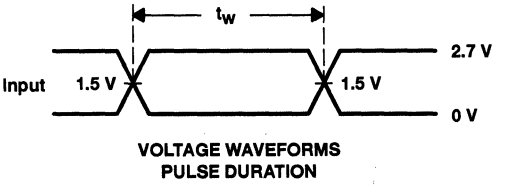


LOAD CIRCUIT

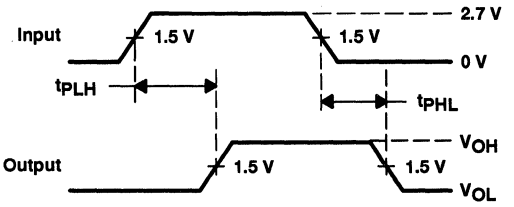
TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 6 V GND



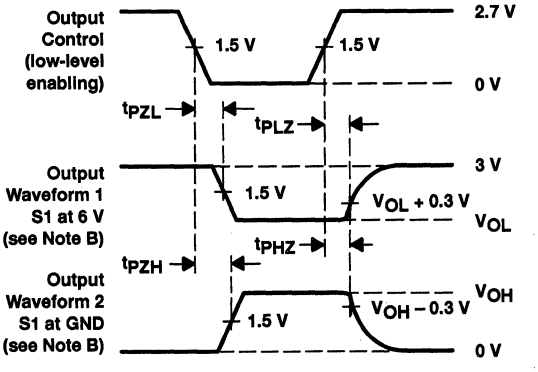
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



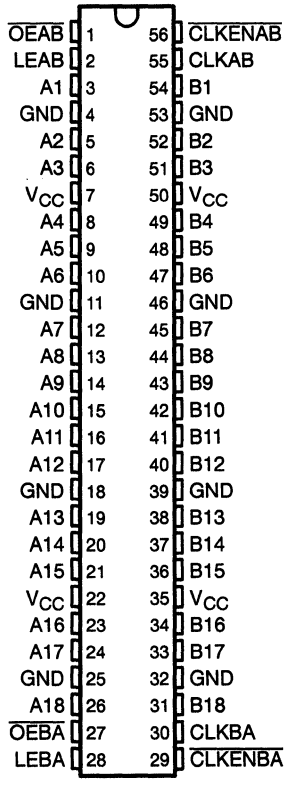
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode**
- **Output Ports Have Equivalent 26-Ω Series Resisters, So No External Resistors Are Required**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 18-bit universal bus transceiver is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH162601 combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CLKENBA}$.

The B-port outputs include 26-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

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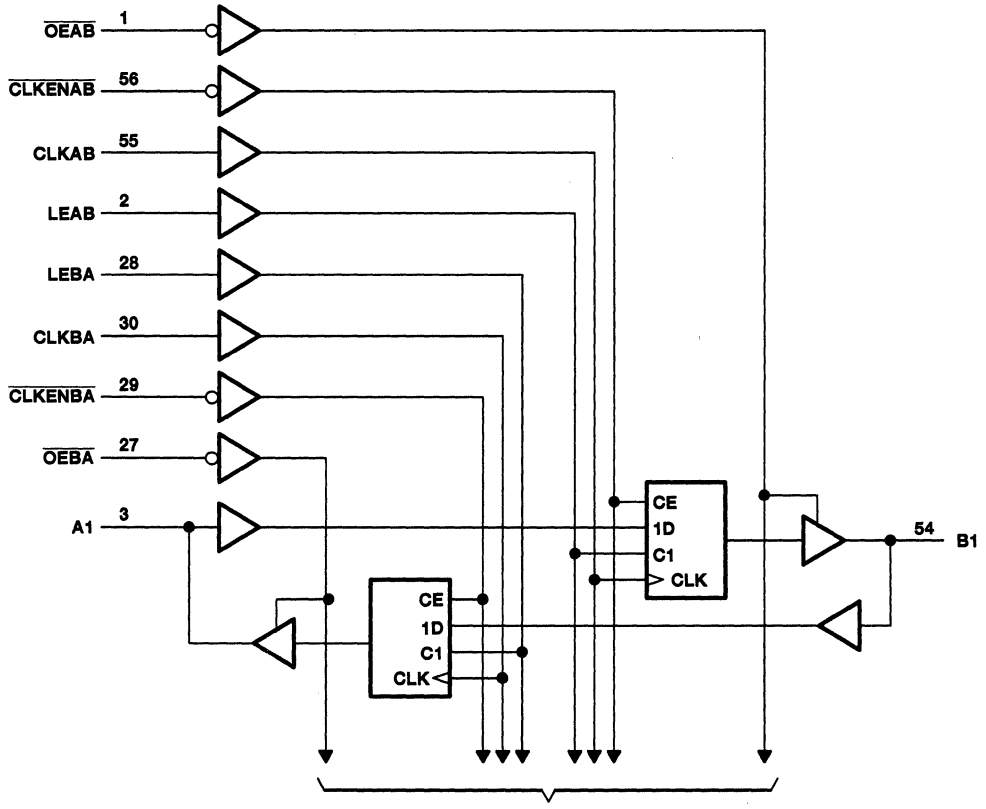
logic diagram (positive logic)

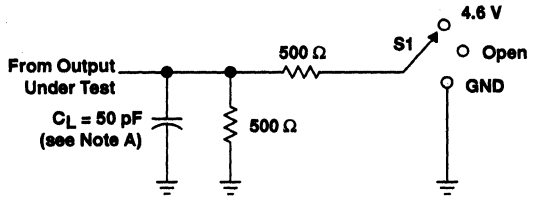


electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH} (B port)		I_{OH} = –100 µA		2.3 V to 3.6 V	V_{CC}–0.2			V
		I_{OH} = –4 mA,	V_{IH} = 1.7 V	2.3 V	1.9			
		I_{OH} = –6 mA	V_{IH} = 1.7 V	2.3 V	1.7			
			V_{IH} = 2 V	3 V	2.4			
		I_{OH} = –8 mA,	V_{IH} = 2 V	2.7 V	2			
		I_{OH} = –12 mA,	V_{IH} = 2 V	3 V	2			
V_{OH} (A port)		I_{OH} = –100 µA		2.3 V to 3.6 V	V_{CC}–0.2			V
		I_{OH} = –6 mA,	V_{IH} = 1.7 V	2.3 V	2			
		I_{OH} = –12 mA	V_{IH} = 1.7 V	2.3 V	1.7			
			V_{IH} = 2 V	2.7 V	2.2			
			V_{IH} = 2 V	3 V	2.4			
		I_{OH} = –24 mA,	V_{IH} = 2 V	3 V	2			
V_{OL} (B port)		I_{OL} = 100 µA		2.3 V to 3.6 V			0.2	V
		I_{OL} = 4 mA,	V_{IL} = 0.7 V	2.3 V			0.4	
		I_{OL} = 6 mA	V_{IL} = 0.7 V	2.3 V			0.55	
			V_{IL} = 0.8 V	3 V			0.55	
		I_{OL} = 8 mA,	V_{IL} = 0.8 V	2.7 V			0.6	
		I_{OL} = 12 mA,	V_{IL} = 0.8 V	3 V			0.8	
V_{OL} (A port)		I_{OL} = 100 µA		2.3 V to 3.6 V			0.2	V
		I_{OL} = 6 mA,	V_{IL} = 0.7 V	2.3 V			0.4	
		I_{OL} = 12 mA	V_{IL} = 0.7 V	2.3 V			0.7	
			V_{IL} = 0.8 V	2.7 V			0.4	
		I_{OL} = 24 mA,	V_{IL} = 0.8 V	3 V			0.55	
I_I		V_I = V_{CC} or GND		3.6 V			±5	µA
$I_{I(hold)}$		V_I = 0.7 V		2.3 V	45			µA
		V_I = 1.7 V			–45			
		V_I = 0.8 V		3 V	75			
		V_I = 2 V			–75			
		V_I = 0 to 3.6 V‡		3.6 V			±500	
I_{OZ}§		V_O = V_{CC} or GND		3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	µA
ΔI_{CC}		One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND	3 V to 3.6 V			750	µA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		4		pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V		8		pF

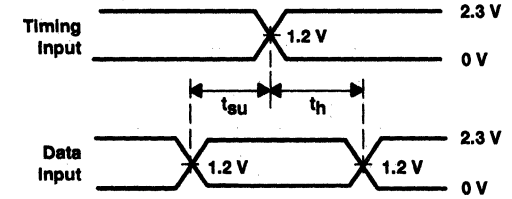
† All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

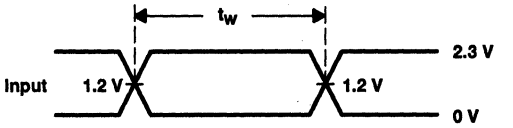


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND

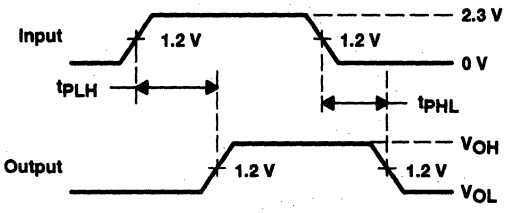
LOAD CIRCUIT



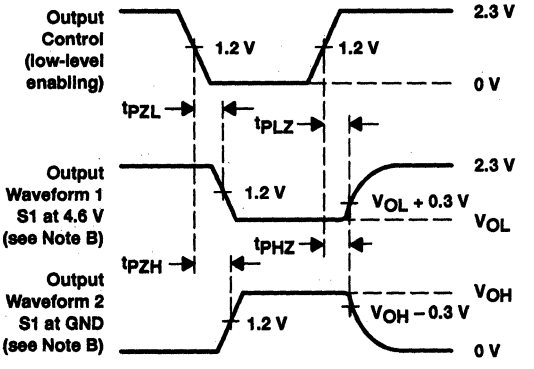
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



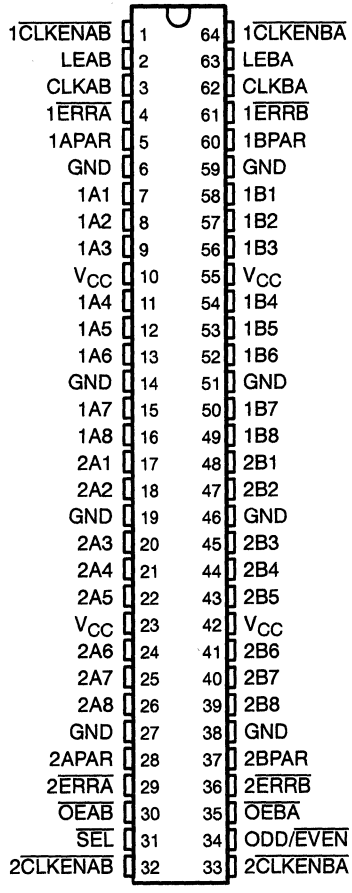
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus+*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **Simultaneously Generates and Checks Parity**
- **Option to Select Generate Parity and Check or Feed-Through Data/Parity in A-to-B or B-to-A Directions**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Packaged in Thin Shrink Small-Outline Package**

DGG PACKAGE
(TOP VIEW)



description

This 18-bit (dual-octal) noninverting registered transceiver is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16901 is a dual 9-bit to dual 9-bit parity transceiver with registers. The device can operate as a feed-through transceiver or it can generate/check parity from the two 8-bit data buses in either direction.

The SN74ALVCH16901 features independent clock (CLKAB or CLKBA), latch-enable (LEAB or LEBA), and dual 9-bit clock-enable ($\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$) inputs. It also provides parity-enable ($\overline{\text{SEL}}$) and parity-select (ODD/$\overline{\text{EVEN}}$) inputs and separate error-signal ($\overline{\text{ERRA}}$ or $\overline{\text{ERRB}}$) outputs for checking parity. The direction of data flow is controlled by $\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$. When $\overline{\text{SEL}}$ is low, the parity functions are enabled. When $\overline{\text{SEL}}$ is high, the parity functions are disabled and the device acts as an 18-bit registered transceiver.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

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FUNCTION TABLE†

INPUTS					OUTPUT
$\overline{\text{CLKENAB}}$	$\overline{\text{OEAB}}$	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0‡
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B_0‡
L	L	L	H	X	B_0§

† A-to-B data flow is shown: B-to-A flow is similar, but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKENBA}}$.

‡ Output level before the indicated steady-state input conditions were established

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I: Except I/O ports (see Note 1) ..... –0.5 V to 4.6 V
I/O ports (see Notes 1 and 2 ..... –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3) ..... 1 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		–12	mA
		V_{CC} = 2.7 V		–12	
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		12	mA
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

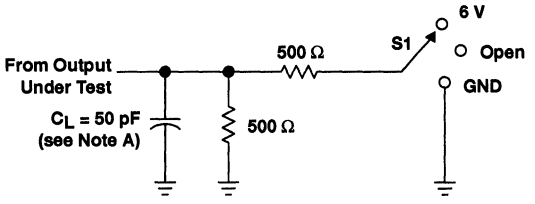
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			125		125		125		MHz
t_{pd}	A or B	B or A	1.5	5.8		4.8	1	4.4	ns
	A or B	BPAR or APAR	2.5	9.5		7.6	2	6.7	
	APAR or BPAR	BPAR or APAR	1.5	6.3		5.2	1	4.7	
	APAR or BPAR	$\overline{ERRA}$ or $\overline{ERRB}$	2.5	10.3		8.7	2	7.5	
	ODD/$\overline{EVEN}$	$\overline{ERRA}$ or $\overline{ERRB}$	2	9.3		7.9	1.5	6.8	
	ODD/$\overline{EVEN}$	BPAR or APAR	2	8.9		7.6	1.5	6.5	
	$\overline{SEL}$	BPAR or APAR	1.5	6.7		5.9	1	5.1	
	CLKAB or CLKBA	A or B	1.5	7		5.8	1	5.1	
	CLKAB or CLKBA	BPAR or APAR parity feedthrough	2	7.7		6.3	1.5	5.6	
	CLKAB or CLKBA	BPAR or APAR parity generated	3	10.8		8.7	2	7.7	
	CLKAB or CLKBA	$\overline{ERRA}$ or $\overline{ERRB}$	3	11.1		8.9	2	7.9	
	LEAB or LEBA	A or B	1.5	6.6		5.5	1	4.8	
	LEAB or LEBA	BPAR or APAR parity feedthrough	2	7.3		6	1.5	5.3	
	LEAB or LEBA	BPAR or APAR parity generated	3	10.4		8.3	2	7.4	
	LEAB or LEBA	$\overline{ERRA}$ or $\overline{ERRB}$	3	10.5		8.5	2	7.5	
t_{en}	$\overline{OEAB}$ or $\overline{OEBA}$	B, BPAR or A, APAR	1.5	6.8		6.1	1	5.3	ns
t_{dis}	$\overline{OEAB}$ or $\overline{OEBA}$	B, BPAR or A, APAR	2	6.3		5.2	1.5	4.9	ns
t_{en}	$\overline{OEAB}$ or $\overline{OEBA}$	$\overline{ERRA}$ or $\overline{ERRB}$	1.5	6.7		5.5	1	4.9	ns
t_{dis}	$\overline{OEAB}$ or $\overline{OEBA}$	$\overline{ERRA}$ or $\overline{ERRB}$	2	7.5		6.5	1	5.7	ns
t_{en}	$\overline{SEL}$	$\overline{ERRA}$ or $\overline{ERRB}$	1.5	7.2		6.5	1	5.5	ns
t_{dis}	$\overline{SEL}$	$\overline{ERRA}$ or $\overline{ERRB}$	2	6.6		5.4	1.5	4.9	ns

operating characteristics, T_A = 25°C

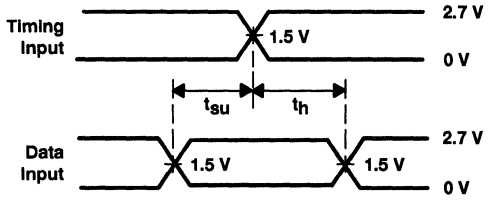
PARAMETER			TEST CONDITIONS	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 10 MHz	22	27	pF
		Outputs disabled		5	8	

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V

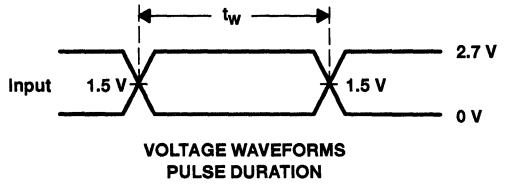


LOAD CIRCUIT

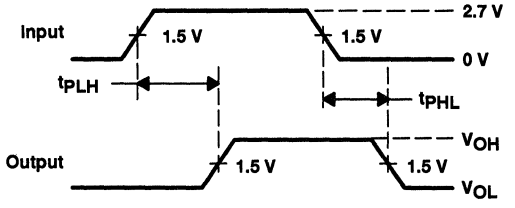
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



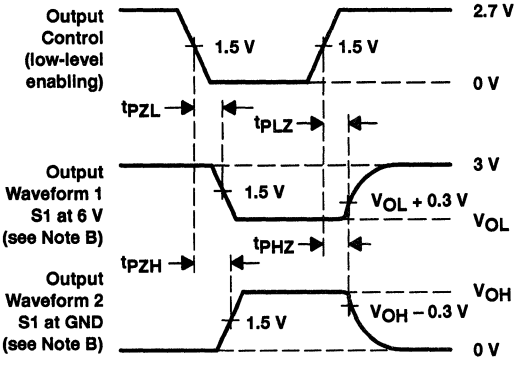
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



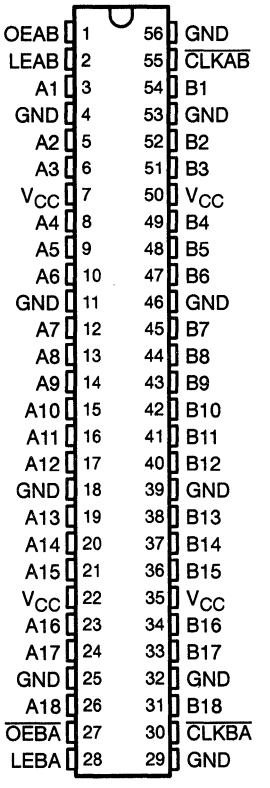
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments *Widebus*™ Family
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- *UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Support Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVT16500 . . . WD PACKAGE
SN74LVT16500 . . . DGG OR DL PACKAGE
(TOP VIEW)



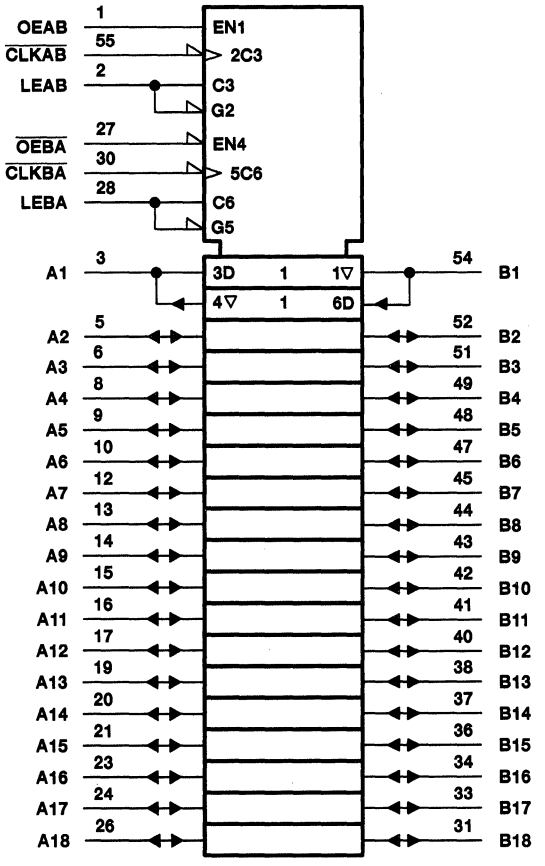
description

The 'LVT16500 are 18-bit universal bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock ($\overline{\text{CLKAB}}$ and $\overline{\text{CLKBA}}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{\text{CLKAB}}$ is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of $\overline{\text{CLKAB}}$. Output-enable OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

Widebus and UBT are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

recommended operating conditions (see Note 4)

			SN54LVT16500		SN74LVT16500		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54LVT16500				SN74LVT16500				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	125	0	150	0	125	MHz
t_w	Pulse duration	LE high	3.3		3.3		3.3		3.3		ns
		$\overline{CLK}$ high or low	3.3		3.3		3.3		3.3		
t_{su}	Setup time	A before $\overline{CLKAB}$↓	1.8		1.1		1.8		1.1		ns
		B before $\overline{CLKBA}$↓	1.9		1.2		1.9		1.2		
		A or B before LE↓, $\overline{CLK}$ high	2.2		1.3		2.2		1.3		
		A or B before LE↓, $\overline{CLK}$ low	2.7		1.9		2.7		1.9		
t_h	Hold time	A or B after $\overline{CLK}$↓	1.2		1.2		1.2		1.2		ns
		A or B after LE↓	0.9		1.1		0.9		1.1		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16500				SN74LVT16500					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
f_{max}			150		125		150			125		MHz
t_{PLH}	B or A	A or B	1.7	5.8		7	1.7	3	5.4		6.8	ns
t_{PHL}			1.6	6		7.8	1.6	3.2	5.9		7.7	
t_{PLH}	LEBA or LEAB	A or B	2.3	7.3		8.9	2.3	4	7		8.5	ns
t_{PHL}			2.7	8.2		9.8	2.7	4.3	7.9		9.7	
t_{PLH}	$\overline{CLKBA}$ or $\overline{CLKAB}$	A or B	2	7.4		8.8	2	4.1	7		8.3	ns
t_{PHL}			2.4	8.1		10	2.4	4.4	7.9		9.9	
t_{PZH}	$\overline{OEBA}$ or OEAB	A or B	1.2	5.2		6.1	1.2	3	5		5.9	ns
t_{PZL}			1.5	5.9		7	1.5	3	5.8		6.9	
t_{PHZ}	$\overline{OEBA}$ or OEAB	A or B	2.7	7.7		8.6	2.7	4.6	7.4		8.3	ns
t_{PLZ}			2.8	7.3		7.7	2.8	4.7	6.7		7.2	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
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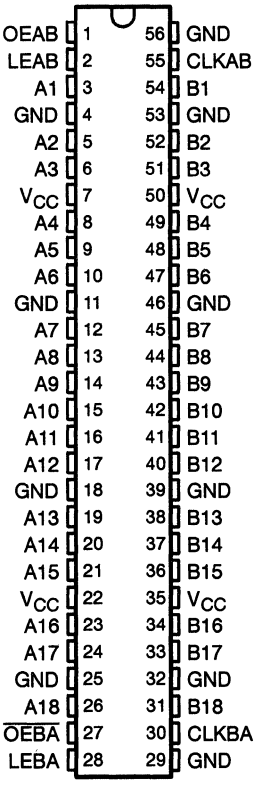
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVT16501 . . . WD PACKAGE
SN74LVT16501 . . . DGG OR DL PACKAGE
(TOP VIEW)



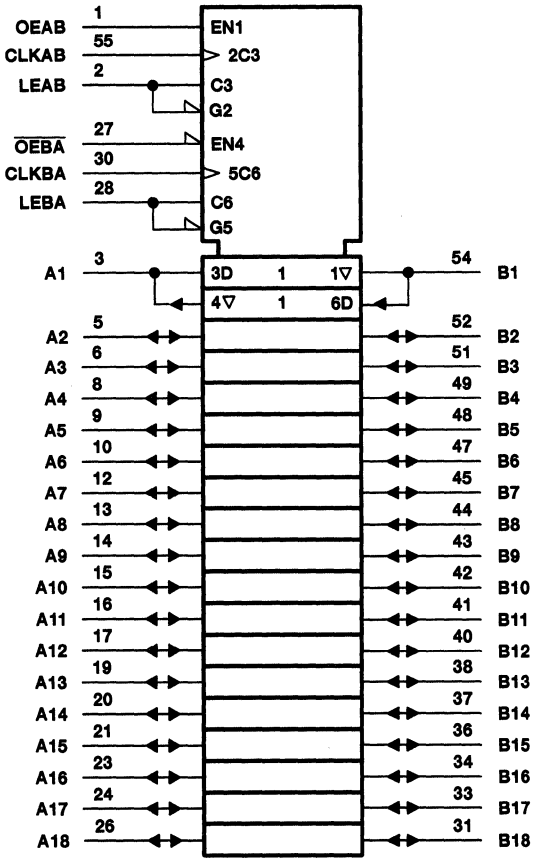
description

The 'LVT16501 are 18-bit universal bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Widebus and UBT are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

recommended operating conditions (see Note 4)

			SN54LVT16501		SN74LVT16501		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54LVT16501				SN74LVT16501				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	125	0	150	0	125	MHz
t_w	Pulse duration	LE high	3.3		3.3		3.3		3.3		ns
		CLK high or low	3.3		3.3		3.3		3.3		
t_{su}	Setup time	A before CLKAB↑	1.6		2.1		1.6		2.1		ns
		B before CLKBA↑	1.6		2.1		1.6		2.1		
		A or B before LE↓, $\overline{CLK}$ high	3.1		2.7		2.6		1.9		
		A or B before LE↓, $\overline{CLK}$ low	2.6		2.0		2		1.3		
t_h	Hold time	A or B after CLK↑	2		2.1		2		2.1		ns
		A or B after LE↓	1.3		1.2		0.9		1.2		

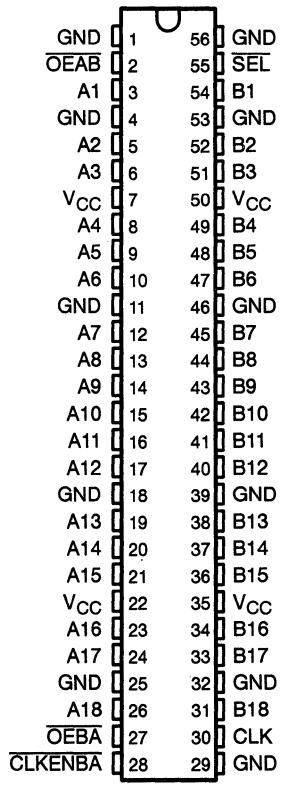
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16501				SN74LVT16501					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
f_{max}			150		125		150			125		MHz
t_{PLH}	B or A	A or B	1.7	5.4		6.8	1.7	3	5.4		6.8	ns
t_{PHL}			1.6	6		7.8	1.6	3.2	5.9		7.7	
t_{PLH}	LEBA or LEAB	A or B	2.3	7.3		9	2.3	4	7		8.5	ns
t_{PHL}			2.7	8.2		9.8	2.7	4.3	7.9		9.7	
t_{PLH}	CLKBA or CLKAB	A or B	2.5	8.3		9.7	2.5	4.1	7.9		9.2	ns
t_{PHL}			3.5	9.4		10.7	3.5	5.4	8.9		10.4	
t_{PZH}	$\overline{OEBA}$ or OEAB	A or B	1.2	5.1		6.1	1.2	3	5		5.9	ns
t_{PZL}			1.5	5.9		7	1.5	3	5.8		6.9	
t_{PHZ}	$\overline{OEBA}$ or OEAB	A or B	2.7	7.5		8.5	2.7	4.6	7.4		8.3	ns
t_{PLZ}			2.8	6.8		7.5	2.8	4.7	6.7		7.2	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 18-bit universal bus transceiver is designed for 2.3-V to 3.6-V V_{CC} operation.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$) and clock enable ($\overline{CLKENBA}$) inputs. For the A-to-B data flow, the data flows through a single register. The B-to-A data can flow through a four-stage pipeline register path, or through a single register path, depending on the state of $\overline{SEL}$.

Data is stored in the internal registers on the low-to-high transition of the CLK input, provided that the appropriate $\overline{CLKENBA}$ input is low. The B-to-A data transfer is synchronized with the CLK input.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16524 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16524 is characterized for operation from –40°C to 85°C.

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FUNCTION TABLE
B-TO-A STORAGE ($\overline{OEBA}$ = L)

INPUTS				OUTPUT
$\overline{CLKENBA}$	CLK	$\overline{SEL}$	B	A
H	X	X	X	A_0†
L	↑	H	L	L
L	↑	H	H	H
L	↑	L	L	L‡
L	↑	L	H	H‡

† Output level before the indicated steady-state input conditions were established
‡ Four positive CLK edges are needed to propagate data from B to A when $\overline{SEL}$ is low.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

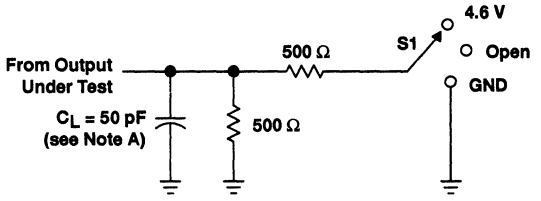
PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}		I_{OH} = −100 µA		2.3 V to 3.6 V	V_{CC}−0.2			V
		I_{OH} = −6 mA,	V_{IH} = 1.7 V	2.3 V	2			
		I_{OH} = −12 mA	V_{IH} = 1.7 V	2.3 V	1.7			
			V_{IH} = 2 V	2.7 V	2.2			
			V_{IH} = 2 V	3 V	2.4			
		I_{OH} = −24 mA,	V_{IH} = 2 V	3 V	2			
V_{OL}		I_{OL} = 100 µA		2.3 V to 3.6 V			0.2	V
		I_{OL} = 6 mA,	V_{IL} = 0.7 V	2.3 V			0.4	
		I_{OL} = 12 mA	V_{IL} = 0.7 V	2.3 V			0.7	
			V_{IL} = 0.8 V	2.7 V			0.4	
		I_{OL} = 24 mA,	V_{IL} = 0.8 V	3 V			0.55	
I_I		V_I = V_{CC} or GND		3.6 V			±5	µA
I_{hold}		V_I = 0.7 V		2.3 V	45			µA
		V_I = 1.7 V			−45			
		V_I = 0.8 V		3 V	75			
		V_I = 2 V			−75			
		V_I = 0 to 3.6 V‡		3.6 V			±500	
I_{OZ}§		V_O = V_{CC} or GND		3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	µA
ΔI_{CC}		One input at V_{CC} − 0.6 V,	Other inputs at V_{CC} or GND	3 V to 3.6 V			750	µA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		3		pF
C_o	A or B ports	V_O = V_{CC} or GND		3.3 V		7		pF

† All typical values are at V_{CC} = 3.3, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

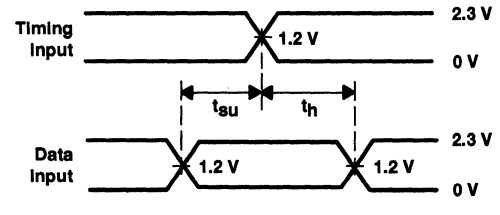
			VCC = 2.5 V ±0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	120	0	125	0	150	MHz
t_w	Pulse duration, CLK high or low		3.2		3.2		3		ns
t_{su}	Setup time	B data before CLK↑	1.5		1.2		1.1		ns
		$\overline{SEL}$ before CLK↑	2.7		2.4		2.1		
		$\overline{CLKENBA}$ before CLK↑	2.7		2.6		2		
t_h	Hold time	B data after CLK↑	1		0.6		1.2		ns
		$\overline{SEL}$ after CLK↑	0.5		0.2		0.8		
		$\overline{CLKENBA}$ after CLK↑	0.1		0.1		0.3		

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

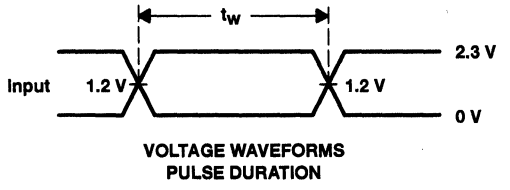


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND

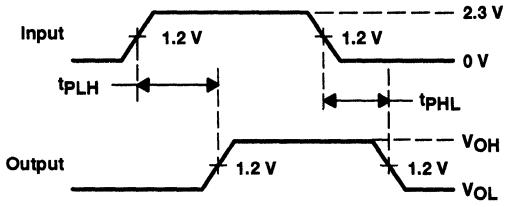
LOAD CIRCUIT



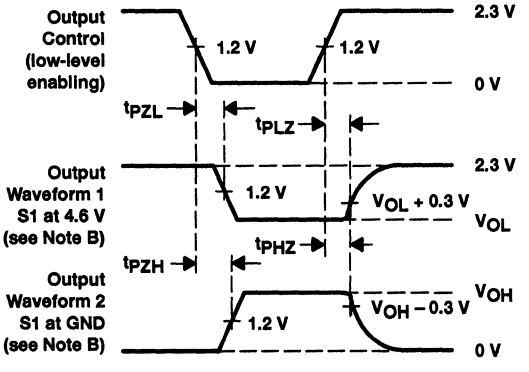
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



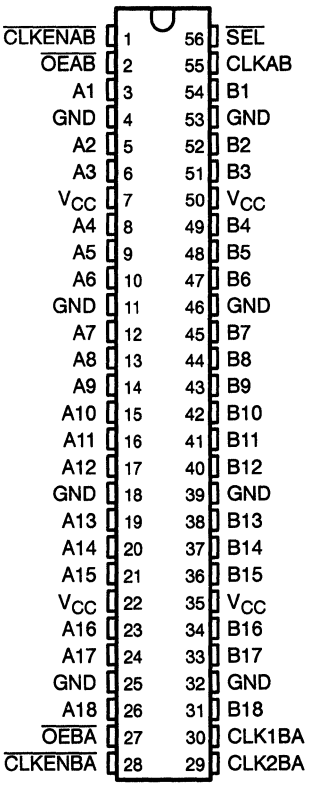
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015;Exceeds 200V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Option Includes Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 18-bit universal bus transceiver is designed for 2.3-V to 3.6-V V_{CC} operation.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$) and clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For the A-to-B data flow, the data flows through a single register. The B-to-A data can flow through a four-stage pipeline register path, or through a single register path, depending on the state of $\overline{SEL}$.

Data is stored in the internal registers on the low-to-high transition of the CLK input, provided that the appropriate $\overline{CLKEN}$ inputs are low. The A-to-B data transfer is synchronized to the CLKAB input, and B-to-A data transfer is synchronized with the CLK1BA and CLK2BA inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16525 is characterized for operation from –40°C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

Function Tables

A-TO-B STORAGE ($\overline{OEAB}$ = L)

INPUTS			OUTPUT
$\overline{CLKENAB}$	CLKAB	A	B
H	X	X	B_0†
L	↑	L	L
L	↑	H	H

† Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE ($\overline{OEBA}$ = L)

INPUTS					OUTPUT
$\overline{CLKENBA}$	CLK2BA	CLK1BA	$\overline{SEL}$	B	A
H	X	X	X	X	A_0†
L	↑	X	H	L	L
L	↑	X	H	H	H
L	↑	↑	L	L	L‡
L	↑	↑	L	H	H‡

† Output level before the indicated steady-state input conditions were established

‡ Three CLK1BA edges and one CLK2BA edge are needed to propagate data from B to A when $\overline{SEL}$ is low.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

timing requirements over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

			V_{CC} = 2.5 V ±0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	120	0	125	0	150	MHz
t_w	Pulse duration, CLK high or low		3.2		3.2		3		ns
t_{su}	Setup time	A data before CLKAB↑	1.3		1.3		1.3		ns
		B data before CLK2BA↑	2.1		1.8		1.7		
		B data before CLK1BA↑	1.3		1.2		1.1		
		$\overline{SEL}$ before CLK2BA↑	3.3		3.3		3.3		
		$\overline{CLKENAB}$ before CLKAB↑	2.1		1.9		1.6		
		$\overline{CLKENBA}$ before CLK1BA↑	2.7		2.5		2.1		
		$\overline{CLKENBA}$ before CLK2BA↑	2.7		2.5		2.2		
t_h	Hold time	A data after CLKAB↑	0.7		0.4		0.9		ns
		B data after CLK2BA↑	0.4		0		0.6		
		B data after CLK1BA↑	0.8		0.4		1		
		$\overline{SEL}$ after CLK2BA↑	0		0		0.1		
		$\overline{CLKENAB}$ after CLKAB↑	0.1		0.3		0.3		
		$\overline{CLKENBA}$ after CLK1BA↑	0		0		0.1		
		$\overline{CLKENBA}$ after CLK2BA↑	0		0		0		

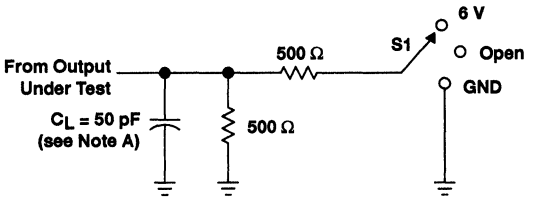
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			120		125		150		MHz
t_{pd}	CLKAB or CLK2BA	A or B	1	5.1		4.4	1	4.2	ns
t_{en}	$\overline{OEAB}$ or $\overline{OEBA}$	A or B	1	6.6		6.1	1	5.1	ns
t_{dis}	$\overline{OEAB}$ or $\overline{OEBA}$	A or B	1	6.5		5.4	1	4.9	ns

operating characteristics, T_A = 25°C

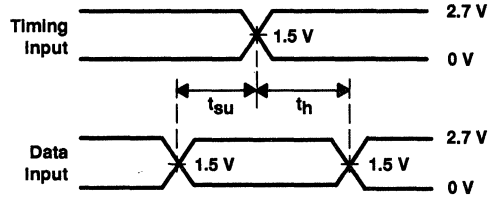
PARAMETER			TEST CONDITIONS	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 10 MHz	160	160	pF
		Outputs disabled				

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V

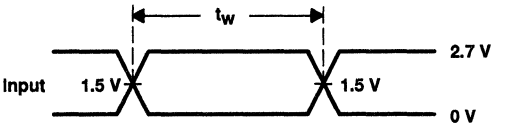


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

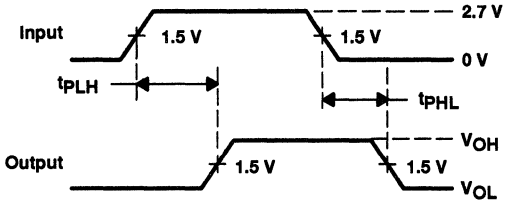
LOAD CIRCUIT



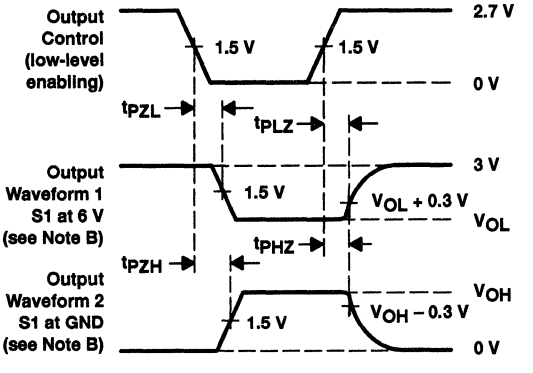
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



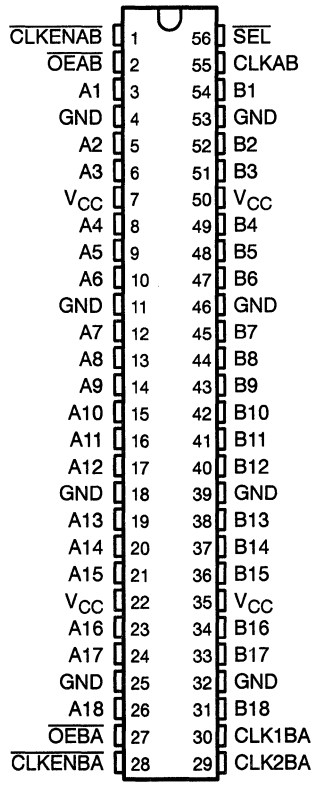
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **B-Port Outputs Have Equivalen 26-Ω Series Resistors, So No External Resistors Are Required**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015;Exceeds 200V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Option Includes Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 18-bit universal bus transceiver is designed for 2.3-V to 3.6-V V_{CC} operation.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$) and clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For the A-to-B data flow, the data flows through a single register. The B-to-A data can flow through a four-stage pipeline register path, or through a single register path, depending on the state of $\overline{SEL}$.

Data is stored in the internal registers on the low-to-high transition of the CLK input, provided that the appropriate $\overline{CLKEN}$ inputs are low. The A-to-B data transfer is synchronized to the CLKAB input, and B-to-A data transfer is synchronized with the CLK1BA and CLK2BA inputs.

The B outputs, which are designed to sink up to 12 mA, include 26-Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162525 is characterized for operation from –40°C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

Function Tables

A-TO-B STORAGE ($\overline{OEAB}$ = L)

INPUTS			OUTPUT
$\overline{CLKENAB}$	CLKAB	A	B
H	X	X	B_0†
L	↑	L	L
L	↑	H	H

† Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE ($\overline{OEBA}$ = L)

INPUTS					OUTPUT
$\overline{CLKENBA}$	CLK2BA	CLK1BA	$\overline{SEL}$	B	A
H	X	X	X	X	A_0†
L	↑	X	H	L	L
L	↑	X	H	H	H
L	↑	↑	L	L	L‡
L	↑	↑	L	H	H‡

† Output level before the indicated steady-state input conditions were established

‡ Three CLK1BA edges and one CLK2BA edge are needed to propagate data from B to A when $\overline{SEL}$ is low.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

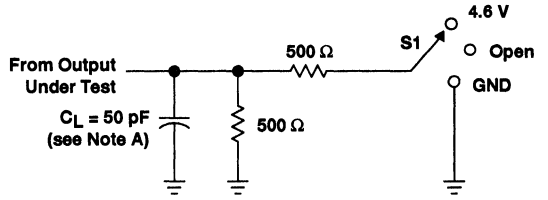
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book.*

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH} (A port)		I_{OH} = –100 µA		2.3 V to 3.6 V	V_{CC}–0.2			V
		I_{OH} = –6 mA,	V_{IH} = 1.7 V	2.3 V	2			
		I_{OH} = –12 mA	V_{IH} = 1.7 V	2.3 V	1.7			
			V_{IH} = 2 V	2.7 V	2.2			
			V_{IH} = 2 V	3 V	2.4			
		I_{OH} = –24 mA,	V_{IH} = 2 V	3 V	2			
V_{OH} (B port)		I_{OH} = –100 µA		2.3 V to 3.6 V	V_{CC}–0.2			V
		I_{OH} = –4 mA,	V_{IH} = 1.7 V	2.3 V	1.9			
		I_{OH} = –6 mA	V_{IH} = 1.7 V	2.3 V	1.7			
			V_{IH} = 2 V	3 V	2.4			
		I_{OH} = –8 mA,	V_{IH} = 2 V	2.7 V	2			
		I_{OH} = –12 mA,	V_{IH} = 2 V	3 V	2			
V_{OL} (A port)		I_{OL} = 100 µA		2.3 V to 3.6 V			0.2	V
		I_{OL} = 6 mA,	V_{IL} = 0.7 V	2.3 V			0.4	
		I_{OL} = 12 mA	V_{IL} = 0.7 V	2.3 V			0.7	
			V_{IL} = 0.8 V	2.7 V			0.4	
		I_{OL} = 24 mA,	V_{IL} = 0.8 V	3 V			0.55	
V_{OL} (B port)		I_{OL} = 100 µA		2.3 V to 3.6 V			0.2	V
		I_{OL} = 4 mA,	V_{IL} = 0.7 V	2.3 V			0.4	
		I_{OL} = 6 mA	V_{IL} = 0.7 V	2.3 V			0.55	
			V_{IL} = 0.8 V	3 V			0.55	
		I_{OL} = 8 mA,	V_{IL} = 0.8 V	2.7 V			0.6	
		I_{OL} = 12 mA,	V_{IL} = 0.8 V	3 V			0.8	
I_I		V_I = V_{CC} or GND		3.6 V			±5	µA
I_{hold}		V_I = 0.7 V		2.3 V	45			µA
		V_I = 1.7 V			–45			
		V_I = 0.8 V		3 V	75			
		V_I = 2 V			–75			
		V_I = 0 to 3.6 V‡		3.6 V			±500	
I_{OZ}§		V_O = V_{CC} or GND		3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	µA
ΔI_{CC}		One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND	3 V to 3.6 V			750	µA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		3		pF
C_o	A or B ports	V_O = V_{CC} or GND		3.3 V		7		pF

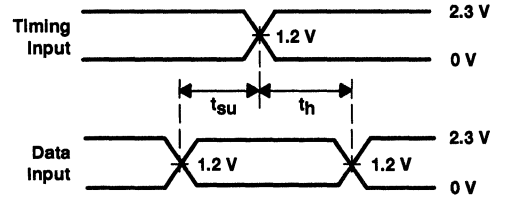
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

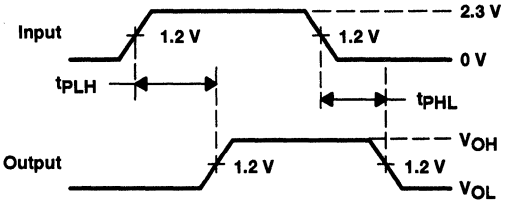


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND

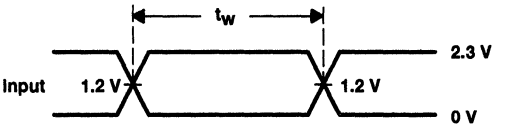
LOAD CIRCUIT



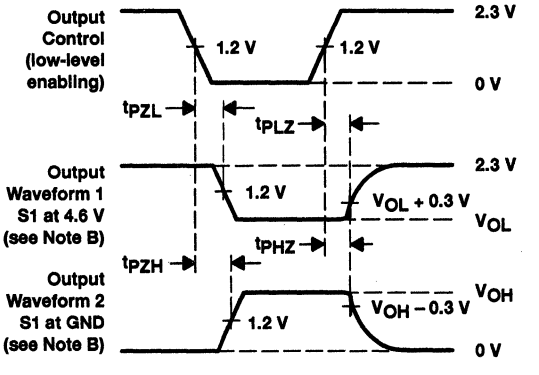
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
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G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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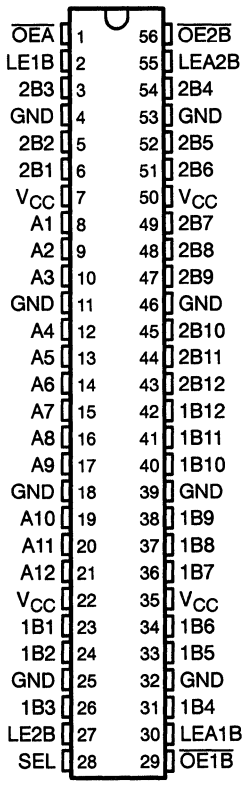
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 12-bit to 24-bit multiplexed D-type latch is designed for 2.3-V to 3.6-V_{CC} operation.

The SN74ALVCH16260 is used in applications where two separate datapaths must be multiplexed onto, or demultiplexed from, a single datapath. Typical applications include multiplexing and/or demultiplexing address and data information in microprocessor or bus-interface applications. This device is also useful in memory-interleaving applications.

Three 12-bit I/O ports (A1–A12, 1B1–1B12, and 2B1–2B12) are available for address and/or data transfer. The output-enable ($\overline{OE1B}$, $\overline{OE2B}$, and $\overline{OEA}$) inputs control the bus transceiver functions. The $\overline{OE1B}$ and $\overline{OE2B}$ control signals also allow bank control in the A-to-B direction.

Address and/or data information can be stored using the internal storage latches. The latch-enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch-enable input is high, the latch is transparent. When the latch-enable input goes low, the data present at the inputs is latched and remains latched until the latch-enable input is returned high.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

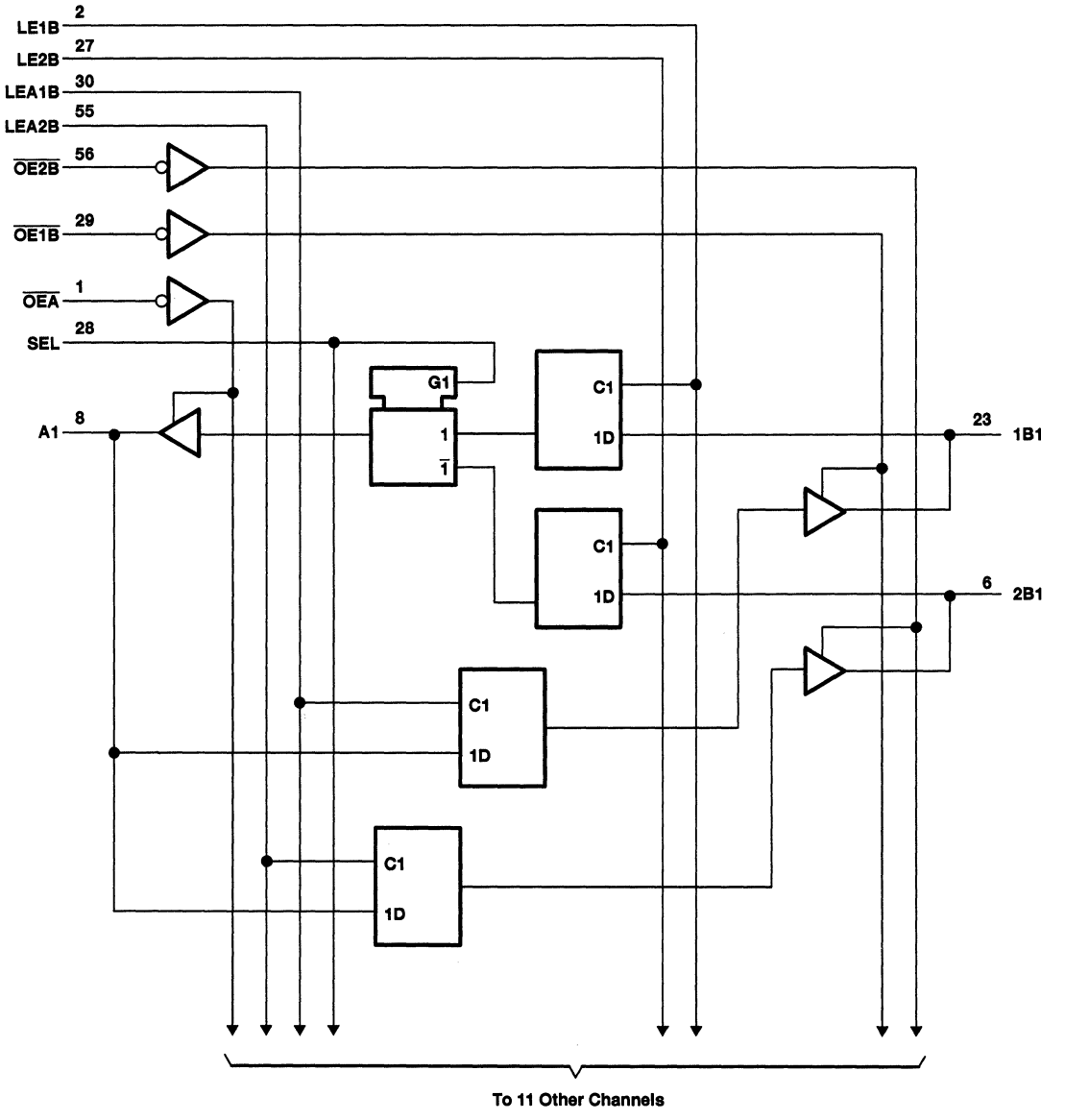
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16260 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16260 is characterized for operation from −40°C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic diagram (positive logic)



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

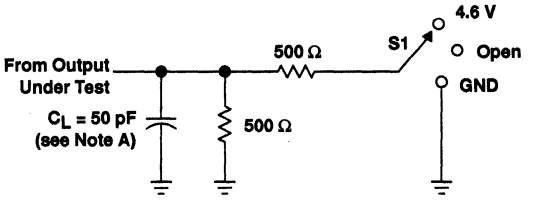
PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}	I_{OH} = –100 µA		2.3 V to 3.6 V	V_{CC}–0.2			V
	I_{OH} = –6 mA,	V_{IH} = 1.7 V	2.3 V	2			
	I_{OH} = –12 mA	V_{IH} = 1.7 V	2.3 V	1.7			
		V_{IH} = 2 V	2.7 V	2.2			
		V_{IH} = 2 V	3 V	2.4			
	I_{OH} = –24 mA,	V_{IH} = 2 V	3 V	2			
V_{OL}	I_{OL} = 100 µA		2.3 V to 3.6 V			0.2	V
	I_{OL} = 6 mA,	V_{IL} = 0.7 V	2.3 V			0.4	
	I_{OL} = 12 mA	V_{IL} = 0.7 V	2.3 V			0.7	
		V_{IL} = 0.8 V	2.7 V			0.4	
	I_{OL} = 24 mA,	V_{IL} = 0.8 V	3 V			0.55	
I_I	V_I = V_{CC} or GND		3.6 V			±5	µA
$I_{I(hold)}$	V_I = 0.7 V		2.3 V	45			µA
	V_I = 1.7 V			–45			
	V_I = 0.8 V		3 V	75			
	V_I = 2 V			–75			
	V_I = 0 to 3.6 V‡		3.6 V			±500	
I_{OZ}§	V_O = V_{CC} or GND		3.6 V			±10	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	µA
ΔI_{CC}	One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND	3 V to 3.6 V			750	µA
C_i Control inputs	V_I = V_{CC} or GND		3.3 V		3.5		pF
C_{io} A or B ports	V_O = V_{CC} or GND		3.3 V		9		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

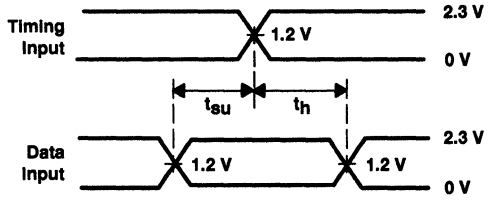
		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high	3.3		3.3		3.3		ns
t_{su}	Setup time, data before LE1B, LE2B, LEA1B, or LEA2B	1.4		1.1		1.1		ns
t_h	Hold time, data after LE1B, LE2B, LEA1B, or LEA2B	1.6		1.9		1.5		ns

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

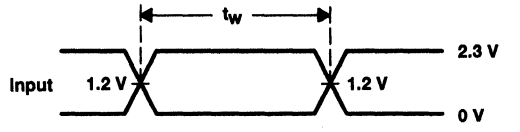


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND

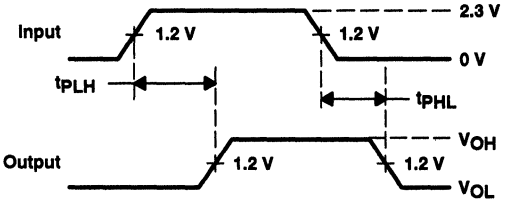
LOAD CIRCUIT



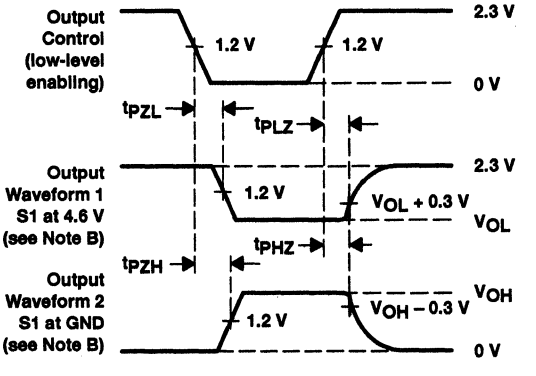
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



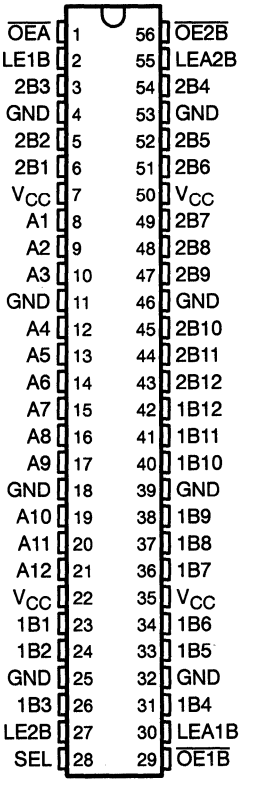
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **B-Port Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Thin-Shrink Small-Outline (DGG) and Plastic Shrink Small-Outline (DL) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 12-bit to 24-bit multiplexed D-type latch is designed for 2.3-V to 3.6-V_{CC} operation.

The SN74ALVCH162260 is used in applications where two separate datapaths must be multiplexed onto, or demultiplexed from, a single datapath. Typical applications include multiplexing and/or demultiplexing address and data information in microprocessor or bus-interface applications. This device is also useful in memory-interleaving applications.

Three 12-bit I/O ports (A1–A12, 1B1–1B12, and 2B1–2B12) are available for address and/or data transfer. The output-enable ($\overline{OE1B}$, $\overline{OE2B}$, and $\overline{OEA}$) inputs control the bus transceiver functions. The $\overline{OE1B}$ and $\overline{OE2B}$ control signals also allow bank control in the A-to-B direction.

Address and/or data information can be stored using the internal storage latches. The latch-enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch-enable input is high, the latch is transparent. When the latch-enable input goes low, the data present at the inputs is latched and remains latched until the latch-enable input is returned high.

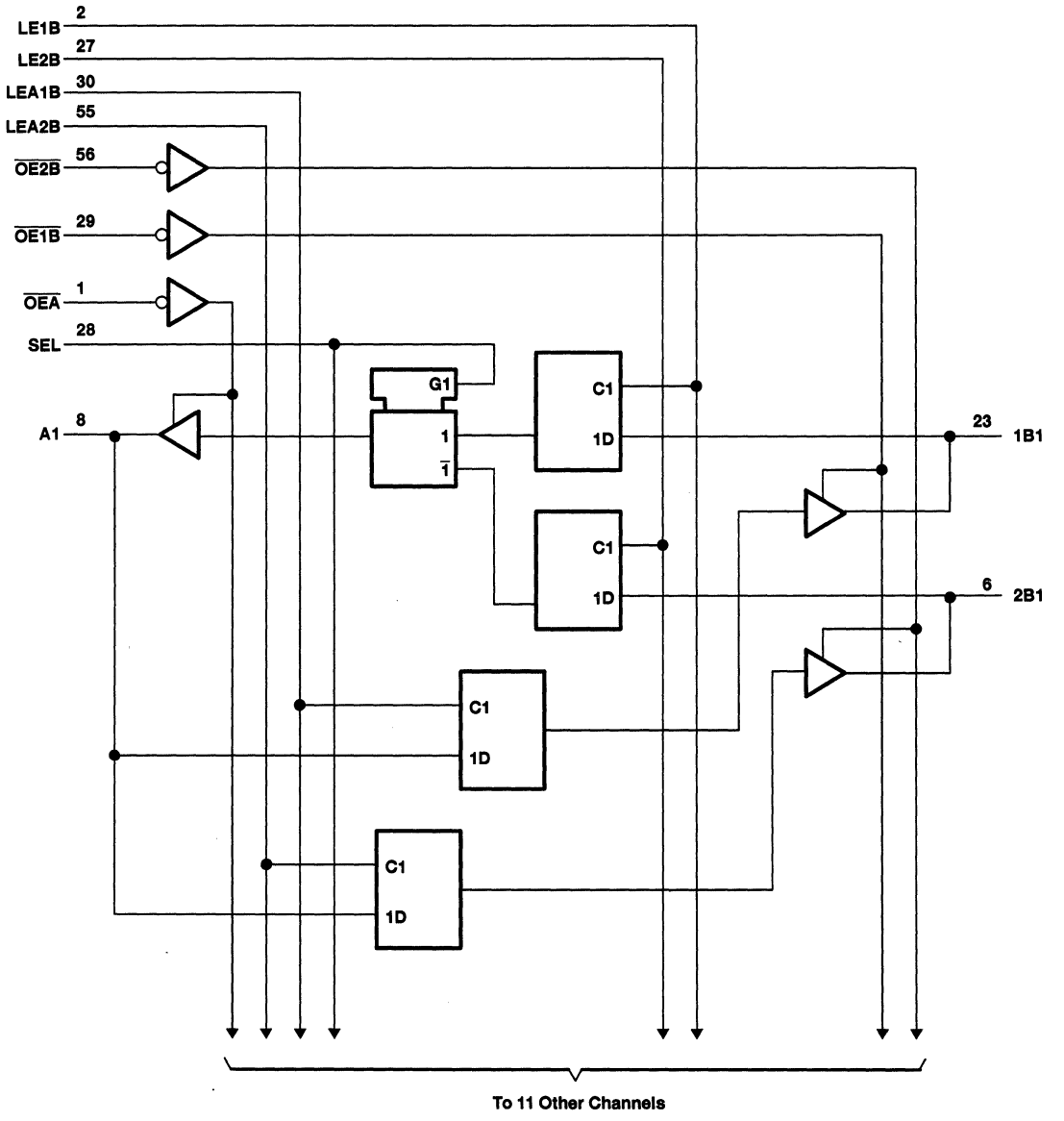
The B outputs, which are designed to sink up to 12 mA, include 26-Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic diagram (positive logic)

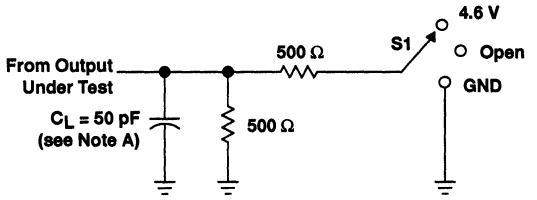


electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH} (A port)		I_{OH} = −100 µA		2.3 V to 3.6 V	V_{CC}−0.2			V
		I_{OH} = −6 mA,	V_{IH} = 1.7 V	2.3 V	2			
		I_{OH} = −12 mA	V_{IH} = 1.7 V	2.3 V	1.7			
			V_{IH} = 2 V	2.7 V	2.2			
			V_{IH} = 2 V	3 V	2.4			
		I_{OH} = −24 mA,	V_{IH} = 2 V	3 V	2			
V_{OH} (B port)		I_{OH} = −100 µA		2.3 V to 3.6 V	V_{CC}−0.2			V
		I_{OH} = −4 mA,	V_{IH} = 1.7 V	2.3 V	1.9			
		I_{OH} = −6 mA	V_{IH} = 1.7 V	2.3 V	1.7			
			V_{IH} = 2 V	3 V	2.4			
		I_{OH} = −8 mA,	V_{IH} = 2 V	2.7 V	2			
		I_{OH} = −12 mA,	V_{IH} = 2 V	3 V	2			
V_{OL} (A port)		I_{OL} = 100 µA		2.3 V to 3.6 V			0.2	V
		I_{OL} = 6 mA,	V_{IL} = 0.7 V	2.3 V			0.4	
		I_{OL} = 12 mA	V_{IL} = 0.7 V	2.3 V			0.7	
			V_{IL} = 0.8 V	2.7 V			0.4	
		I_{OL} = 24 mA,	V_{IL} = 0.8 V	3 V			0.55	
V_{OL} (B port)		I_{OL} = 100 µA		2.3 V to 3.6 V			0.2	V
		I_{OL} = 4 mA,	V_{IL} = 0.7 V	2.3 V			0.4	
		I_{OL} = 6 mA	V_{IL} = 0.7 V	2.3 V			0.55	
			V_{IL} = 0.8 V	3 V			0.55	
		I_{OL} = 8 mA,	V_{IL} = 0.8 V	2.7 V			0.6	
		I_{OL} = 12 mA,	V_{IL} = 0.8 V	3 V			0.8	
I_I		V_I = V_{CC} or GND		3.6 V			±5	µA
$I_{I(hold)}$		V_I = 0.7 V		2.3 V	45			µA
		V_I = 1.7 V			−45			
		V_I = 0.8 V		3 V	75			
		V_I = 2 V			−75			
		V_I = 0 to 3.6 V‡		3.6 V			±500	
I_{OZ}§		V_O = V_{CC} or GND		3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	µA
ΔI_{CC}		One input at V_{CC} − 0.6 V,	Other inputs at V_{CC} or GND	3 V to 3.6 V			750	µA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		3.5		pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V		4.5		pF

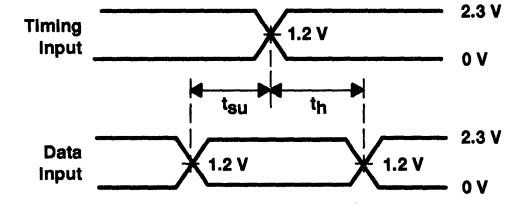
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

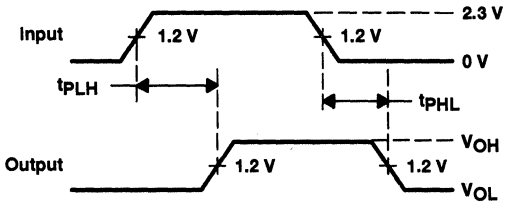


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND

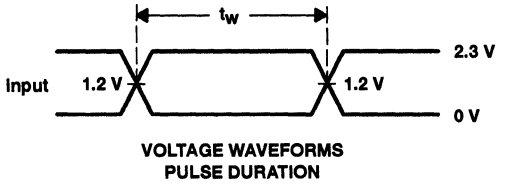
LOAD CIRCUIT



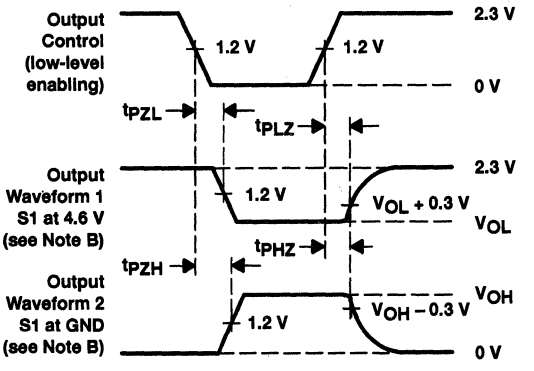
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



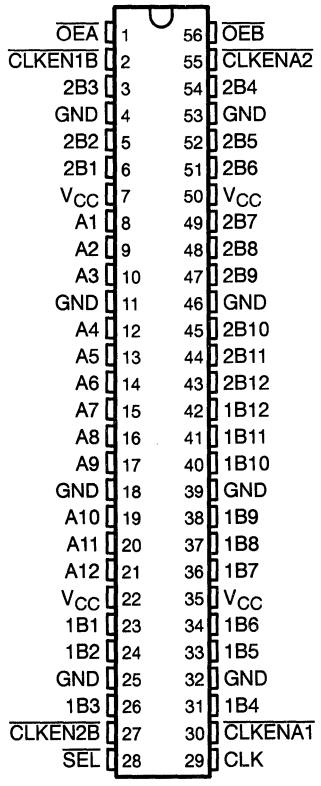
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **B-Port Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 12-bit to 24-bit registered bus exchanger is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH162268 is used for applications where data must be transferred from a narrow high-speed bus to a wide, lower-frequency bus.

The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable ($\overline{CLKEN}$) inputs are low. The select ($\overline{SEL}$) line is synchronous with CLK and selects 1B or 2B input data for the A outputs.

For data transfer in the A-to-B direction, a two-stage pipeline is provided in the A-to-1B path with a single storage register in the A-to-2B path. Proper control of these inputs allows two sequential 12-bit words to be presented synchronously as a 24-bit word on the B port. Data flow is controlled by the active-low output enables ($\overline{OEA}$, $\overline{OEB}$). These control terminals are registered so bus direction changes are synchronous with CLK.

The B outputs, which are designed to sink up to 12 mA, include 26-Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162268 is characterized for operation from –40°C to 85°C.

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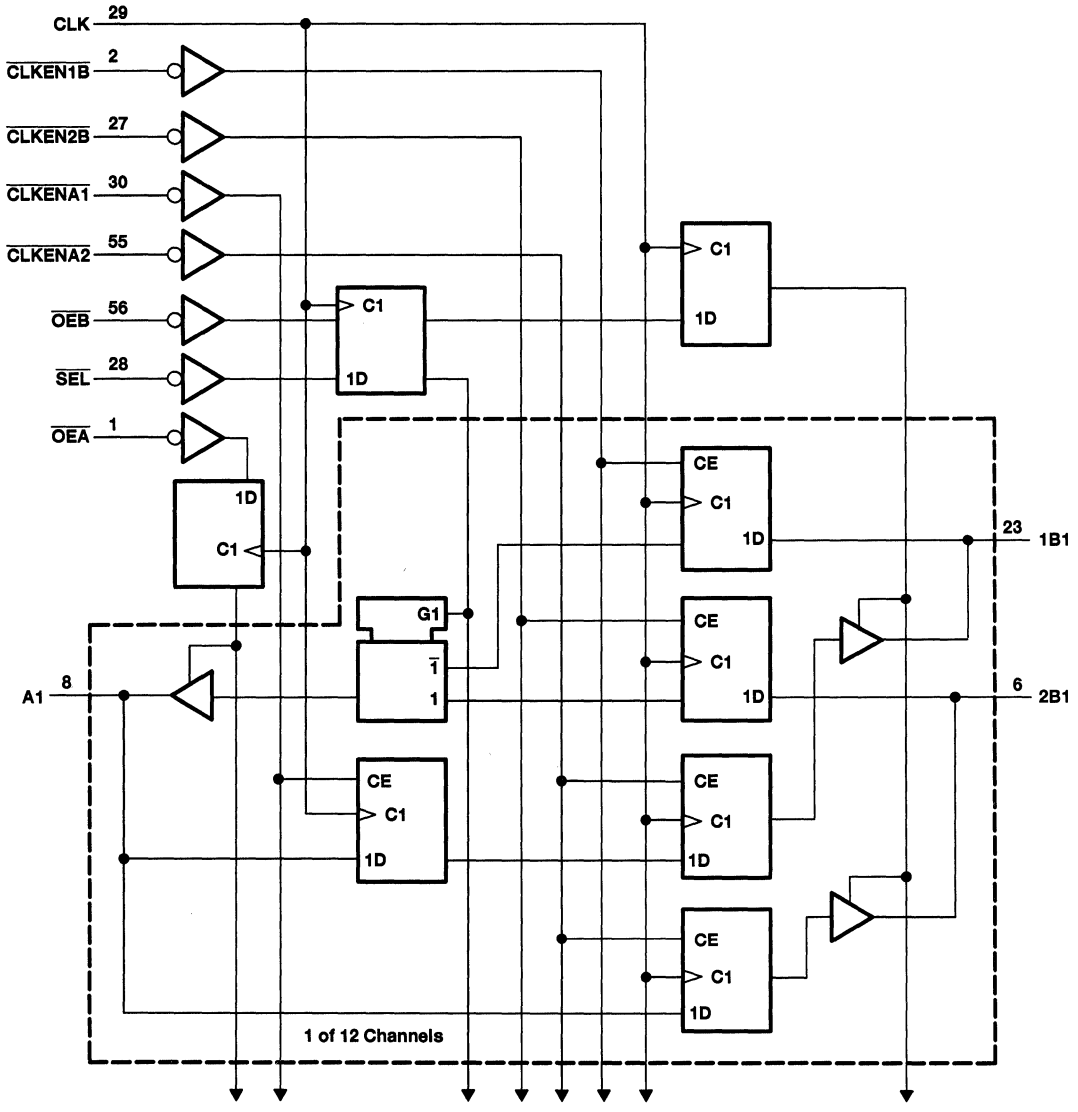
logic diagram (positive logic)

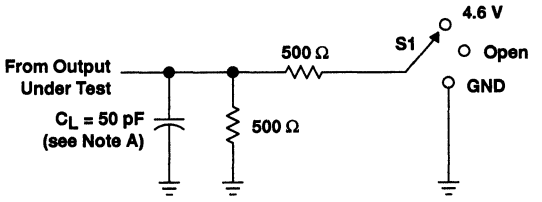


electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH} (B port)		I_{OH} = −100 µA		2.3 V to 3.6 V	V_{CC}−0.2			V
		I_{OH} = −4 mA,	V_{IH} = 1.7 V	2.3 V	1.9			
		I_{OH} = −6 mA	V_{IH} = 1.7 V	2.3 V	1.7			
			V_{IH} = 2 V	3 V	2.4			
		I_{OH} = −8 mA,	V_{IH} = 2 V	2.7 V	2			
		I_{OH} = −12 mA,	V_{IH} = 2 V	3 V	2			
V_{OL} (B port)		I_{OL} = 100 µA		2.3 V to 3.6 V			0.2	V
		I_{OL} = 4 mA,	V_{IL} = 0.7 V	2.3 V			0.4	
		I_{OL} = 6 mA	V_{IL} = 0.7 V	2.3 V			0.55	
			V_{IL} = 0.8 V	3 V			0.55	
		I_{OL} = 8 mA,	V_{IL} = 0.8 V	2.7 V			0.6	
		I_{OL} = 12 mA,	V_{IL} = 0.8 V	3 V			0.8	
V_{OH} (A port)		I_{OH} = −100 µA		2.3 V to 3.6 V			V_{CC}−0.2	V
		I_{OH} = −6 mA,	V_{IH} = 1.7 V	2.3 V	2			
		I_{OH} = −12 mA	V_{IH} = 1.7 V	2.3 V	1.7			
			V_{IH} = 2 V	2.7 V	2.2			
			V_{IH} = 2 V	3 V	2.4			
		I_{OH} = −24 mA,	V_{IH} = 2 V	3 V	2			
V_{OL} (A port)		I_{OL} = 100 µA		2.3 V to 3.6 V			0.2	V
		I_{OL} = 6 mA,	V_{IL} = 0.7 V	2.3 V			0.4	
		I_{OL} = 12 mA	V_{IL} = 0.7 V	2.3 V			0.7	
			V_{IL} = 0.8 V	2.7 V			0.4	
		I_{OL} = 24 mA,	V_{IL} = 0.8 V	3 V			0.55	
I_I		V_I = V_{CC} or GND		3.6 V			±5	µA
$I_{I(hold)}$		V_I = 0.7 V		2.3 V	45			µA
		V_I = 1.7 V			−45			
		V_I = 0.8 V		3 V	75			
		V_I = 2 V			−75			
		V_I = 0 to 3.6 V‡		3.6 V			±500	
I_{OZ}§		V_O = V_{CC} or GND		3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	µA
ΔI_{CC}		One input at V_{CC} − 0.6 V,	Other inputs at V_{CC} or GND	3 V to 3.6 V			750	µA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		3.5		pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V		9		pF

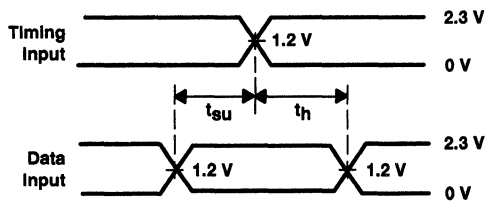
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ For I/O ports, the parameter I_{OZ} includes the input-leakage current.

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

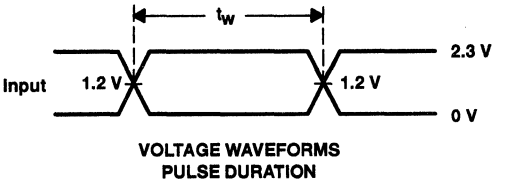


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND

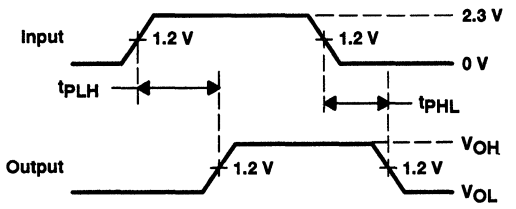
LOAD CIRCUIT



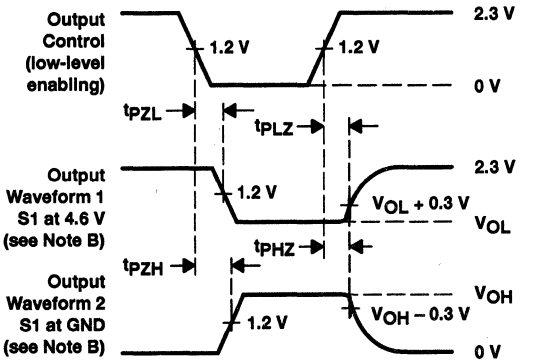
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



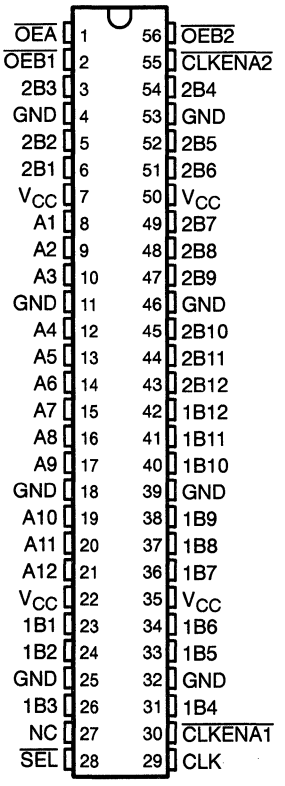
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



NC – No internal connection

description

This 12-bit to 24-bit registered bus transceiver is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16269 is used in applications where two separate ports must be multiplexed onto, or demultiplexed from, a single port. The device is particularly suitable as an interface between synchronous DRAMs and high-speed microprocessors.

Data is stored in the internal B-port registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable ($\overline{\text{CLKENA}}$) inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B port. For data transfer in the B-to-A direction, a single storage register is provided. The select ($\overline{\text{SEL}}$) line selects 1B or 2B data for the A outputs. The register on the A output permits the fastest possible data transfer, thus extending the period that the data is valid on the bus. The control terminals are registered so that all transactions are synchronous with CLK. Data flow is controlled by the active-low output enables ($\overline{\text{OEA}}$, $\overline{\text{OEB1}}$, $\overline{\text{OEB2}}$).

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

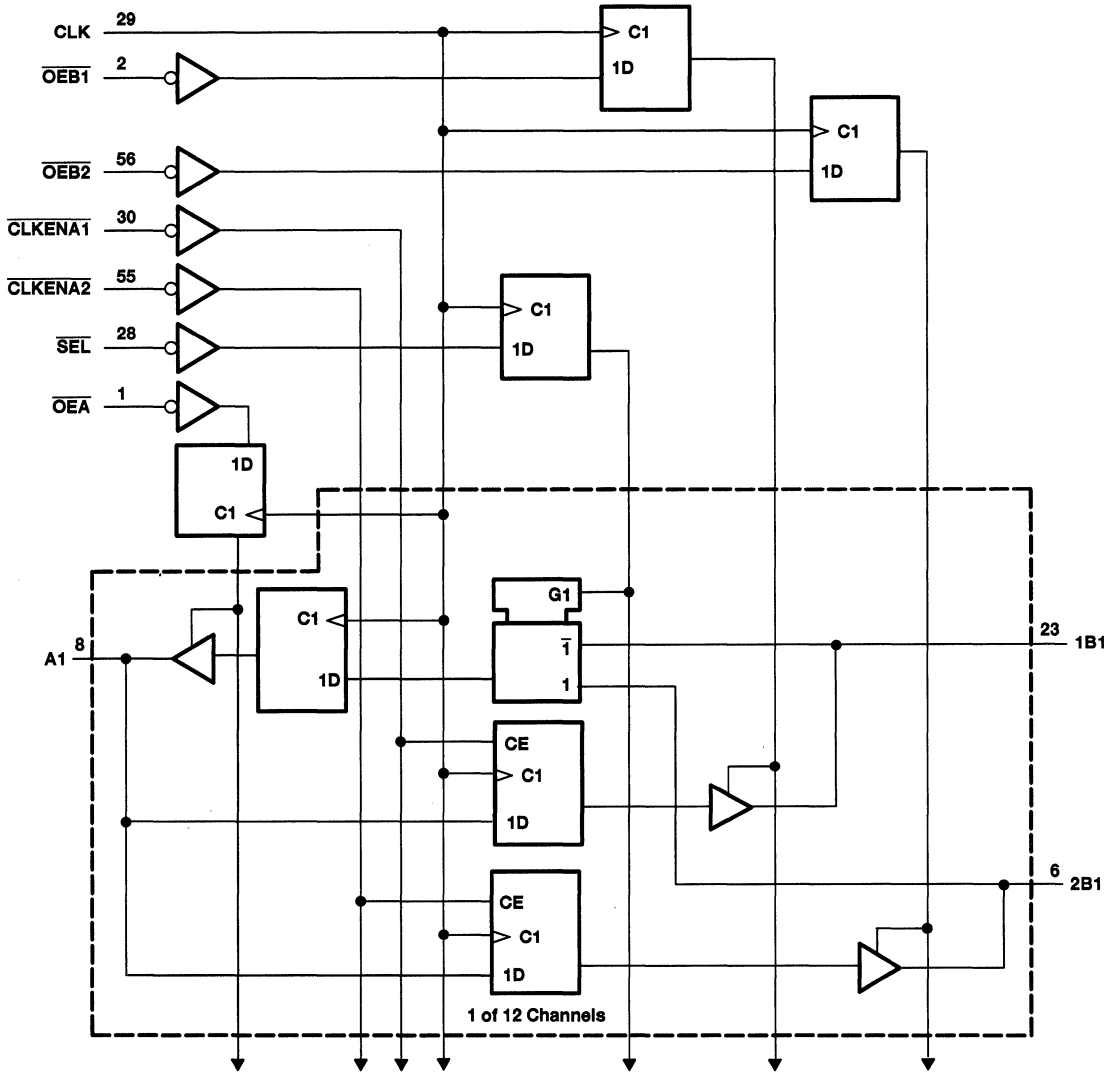
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16269 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16269 is characterized for operation from −40°C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic diagram (positive logic)

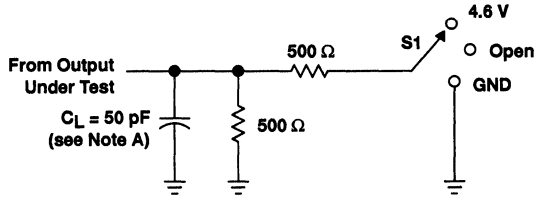


electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}		I_{OH} = –100 µA		2.3 V to 3.6 V	V_{CC}–0.2			V
		I_{OH} = –6 mA,	V_{IH} = 1.7 V	2.3 V	2			
		I_{OH} = –12 mA	V_{IH} = 1.7 V	2.3 V	1.7			
			V_{IH} = 2 V	2.7 V	2.2			
			V_{IH} = 2 V	3 V	2.4			
		I_{OH} = –24 mA,	V_{IH} = 2 V	3 V	2			
V_{OL}		I_{OL} = 100 µA		2.3 V to 3.6 V			0.2	V
		I_{OL} = 6 mA,	V_{IL} = 0.7 V	2.3 V			0.4	
		I_{OL} = 12 mA	V_{IL} = 0.7 V	2.3 V			0.7	
			V_{IL} = 0.8 V	2.7 V			0.4	
		I_{OL} = 24 mA,	V_{IL} = 0.8 V	3 V			0.55	
I_I		V_I = V_{CC} or GND		3.6 V			±5	µA
$I_{I(hold)}$		V_I = 0.7 V		2.3 V	45			µA
		V_I = 1.7 V			–45			
		V_I = 0.8 V		3 V	75			
		V_I = 2 V			–75			
		V_I = 0 to 3.6 V‡		3.6 V			±500	
I_{OZ}§		V_O = V_{CC} or GND		3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	µA
ΔI_{CC}		One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND	3 V to 3.6 V			750	µA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		3.5		pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V		9		pF

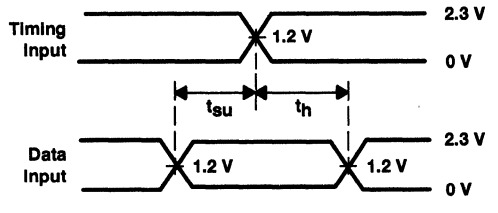
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ For I/O ports, the parameter I_{OZ} includes the input-leakage current.

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

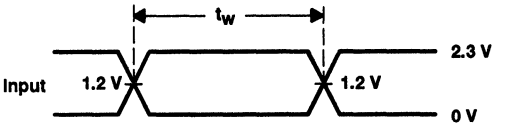


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND

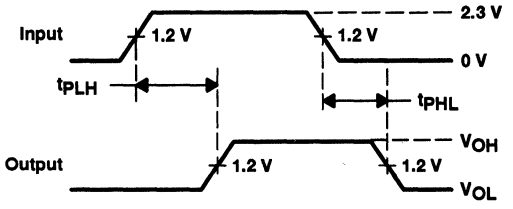
LOAD CIRCUIT



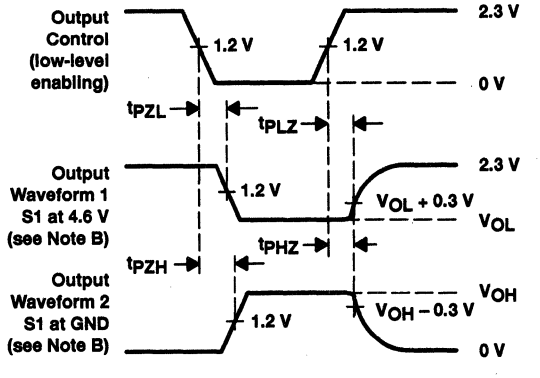
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



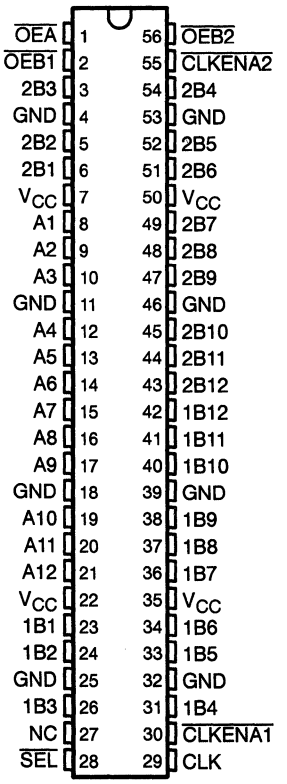
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **All Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



NC – No internal connection

description

This 12-bit to 24-bit registered bus exchanger is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCHR162269 is used in applications where two separate ports must be multiplexed onto, or demultiplexed from, a single port. It is particularly suitable as an interface between synchronous DRAMs and high-speed microprocessors.

Data is stored in the internal B-port registers on the low-to-high transition of the clock (CLK) input when the appropriate clock enable ($\overline{\text{CLKENA}}$) inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B port. For data transfer in the B-to-A direction, a single storage register is provided. The select ($\overline{\text{SEL}}$) line selects 1B or 2B data for the A outputs. The register on the A output permits the fastest possible data transfer, thus extending the period that the data is valid on the bus. The control terminals are registered so that all transactions are synchronous with CLK. Data flow is controlled by the active-low output enables ($\overline{\text{OEA}}$, $\overline{\text{OEB1}}$, and $\overline{\text{OEB2}}$).

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

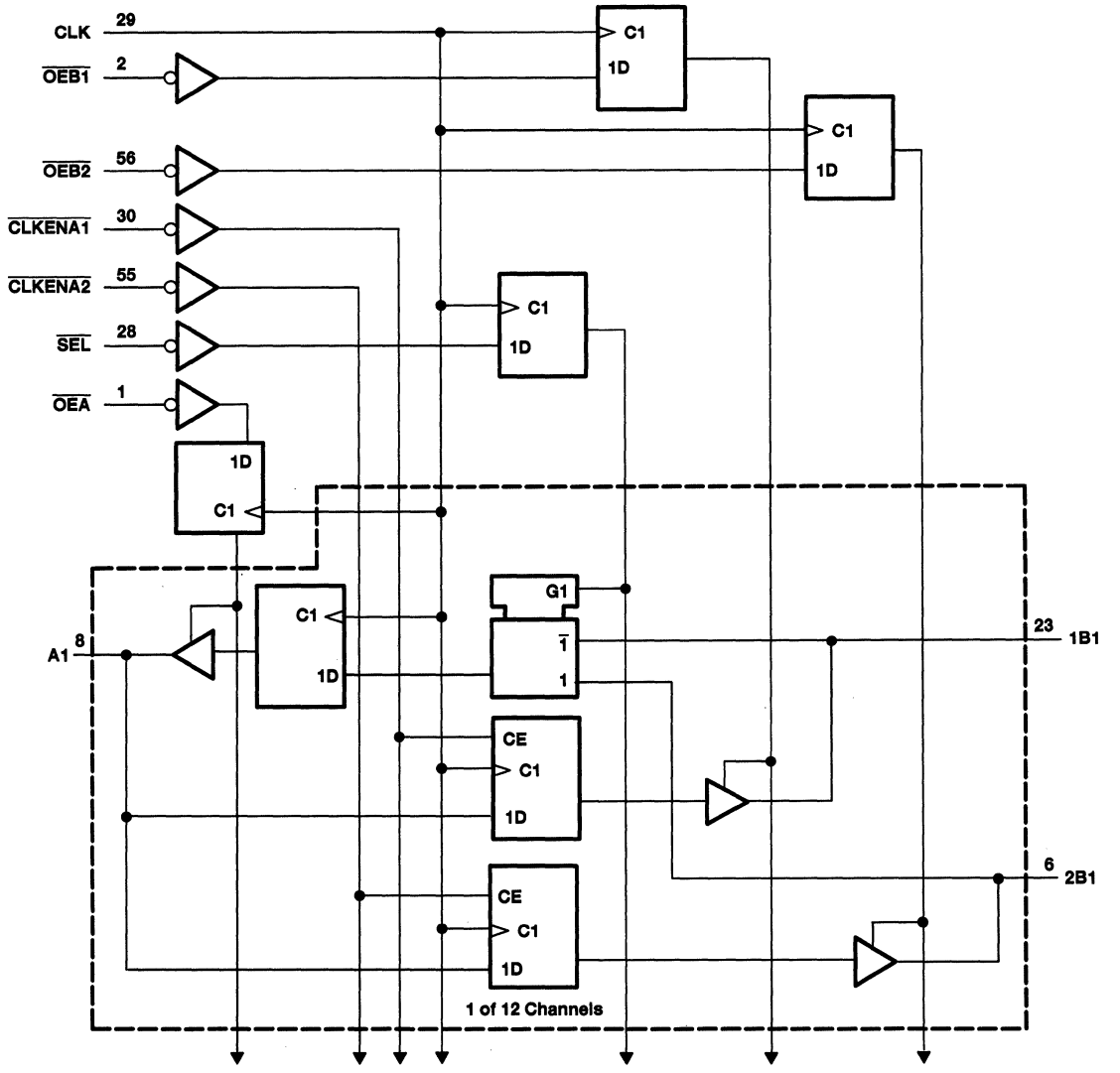
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

All outputs are designed to sink up to12 mA and include 26-Ω resistors to reduce overshoot and undershoot.

The SN74ALVCHR162269 is characterized for operation from –40°C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic diagram (positive logic)

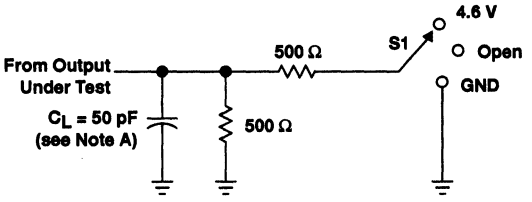


electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}		I_{OH} = −100 μA		2.3 V to 3.6 V	V_{CC}−0.2			V
		I_{OH} = −4 mA	V_{IH} = 1.7 V	2.3 V	1.9			
			V_{IH} = 2 V	2.7 V	2.2			
		I_{OH} = −6 mA	V_{IH} = 1.7 V	2.3 V	1.7			
			V_{IH} = 2 V	3 V	2.4			
		I_{OH} = −8 mA,	V_{IH} = 2 V	2.7 V	2			
		I_{OH} = −12 mA,	V_{IH} = 2 V	3 V	2			
V_{OL}		I_{OL} = 100 μA		2.3 V to 3.6 V			0.2	V
		I_{OL} = 4 mA	V_{IL} = 0.7 V	2.3 V			0.4	
			V_{IL} = 0.8 V	2.7 V			0.4	
		I_{OL} = 6 mA	V_{IL} = 0.7 V	2.3 V			0.55	
			V_{IL} = 0.8 V	3 V			0.55	
		I_{OL} = 8 mA,	V_{IL} = 0.8 V	2.7 V			0.6	
		I_{OL} = 12 mA,	V_{IL} = 0.8 V	3 V			0.8	
I_I		V_I = V_{CC} or GND		3.6 V			±5	μA
$I_{I(hold)}$		V_I = 0.7 V		2.3 V	45			μA
		V_I = 1.7 V			−45			
		V_I = 0.8 V		3 V	75			
		V_I = 2 V			−75			
		V_I = 0 to 3.6 V		3.6 V			±500	
I_{OZ}§		V_O = V_{CC} or GND‡		3.6 V			±10	μA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	μA
ΔI_{CC}		One input at V_{CC} − 0.6 V,	Other inputs at V_{CC} or GND	3 V to 3.6 V			750	μA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		3.5		pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V		9		pF

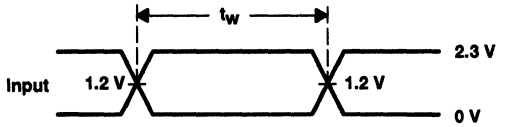
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

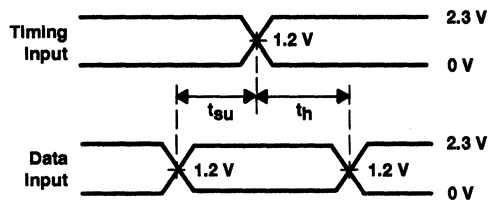


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND

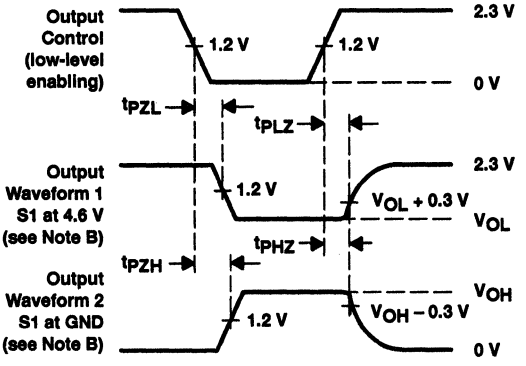
LOAD CIRCUIT



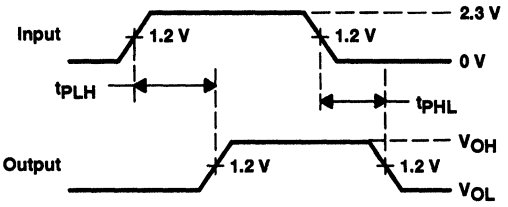
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
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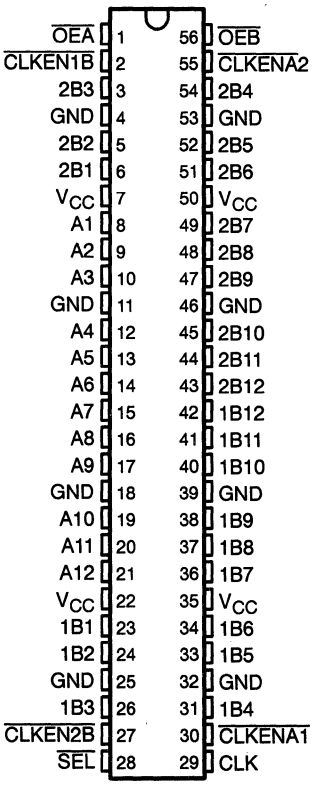
DGG OR DL PACKAGE
(TOP VIEW)



description

This 12-bit to 24-bit registered bus exchanger is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16270 is used in applications where data must be transferred from a narrow high-speed bus to a wide lower-frequency bus.

The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input when the appropriate $\overline{\text{CLKEN}}$ inputs are low. The select ($\overline{\text{SEL}}$) line selects 1B or 2B data for the A outputs. For data transfer in the A-to-B direction, a two-stage pipeline is provided in the A-to-1B path, with a single storage register in the A to 2B path. Proper control of the $\overline{\text{CLKENA}}$ inputs allows two sequential 12-bit words to be presented synchronously as a 24-bit word on the B port. Data flow is controlled by the active-low output enables ($\overline{\text{OEA}}$, $\overline{\text{OEB}}$). The control terminals are registered to synchronize the bus direction changes with CLK.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

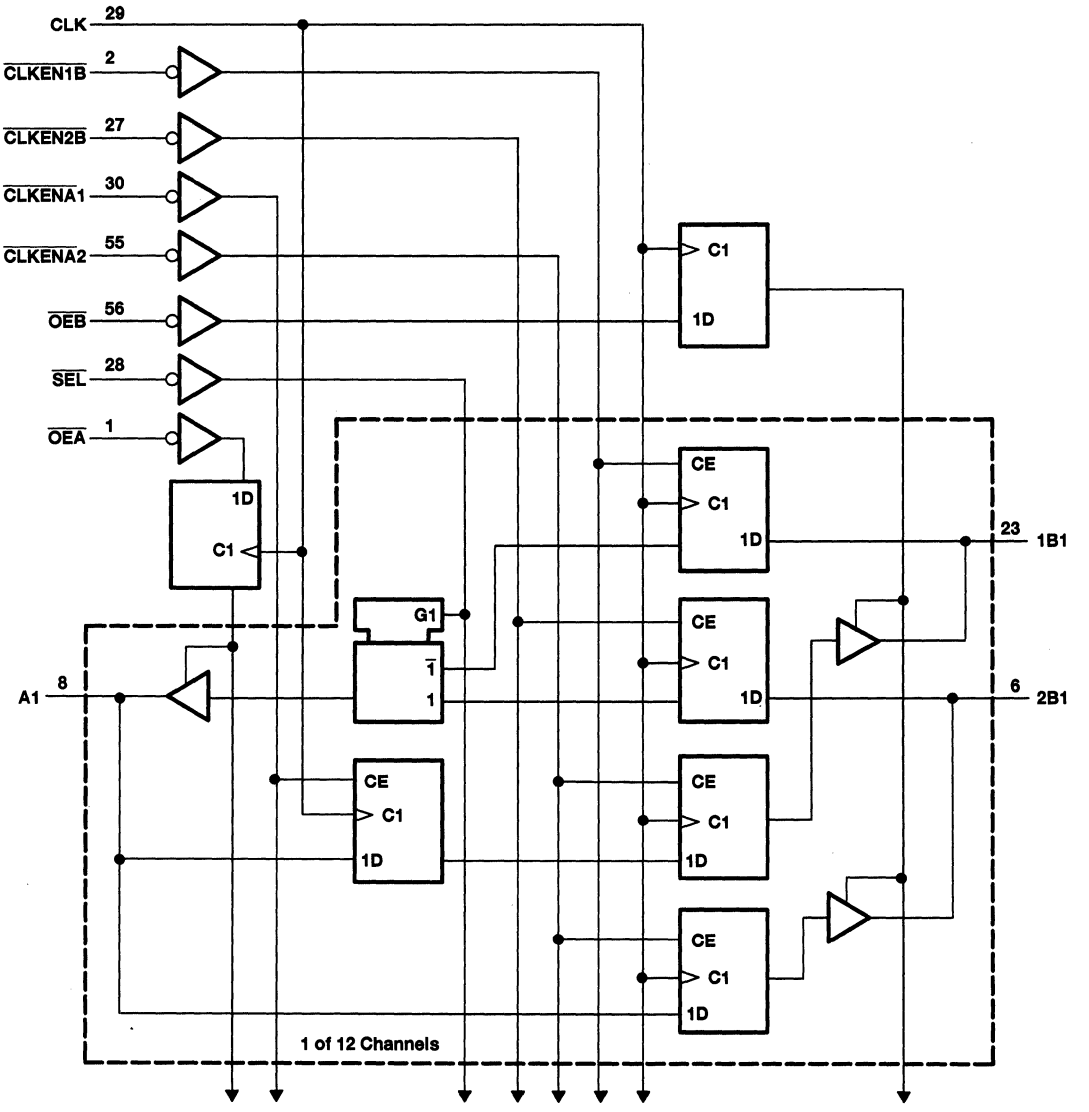
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16270 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16270 is characterized for operation from –40°C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic diagram (positive logic)

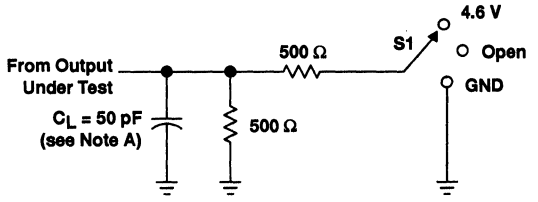


electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}		I_{OH} = –100 µA		2.3 V to 3.6 V	V_{CC}–0.2			V
		I_{OH} = –6 mA,	V_{IH} = 1.7 V	2.3 V	2			
		I_{OH} = –12 mA	V_{IH} = 1.7 V	2.3 V	1.7			
			V_{IH} = 2 V	2.7 V	2.2			
			V_{IH} = 2 V	3 V	2.4			
		I_{OH} = –24 mA,	V_{IH} = 2 V	3 V	2			
V_{OL}		I_{OL} = 100 µA		2.3 V to 3.6 V			0.2	V
		I_{OL} = 6 mA,	V_{IL} = 0.7 V	2.3 V			0.4	
		I_{OL} = 12 mA	V_{IL} = 0.7 V	2.3 V			0.7	
			V_{IL} = 0.8 V	2.7 V			0.4	
		I_{OL} = 24 mA,	V_{IL} = 0.8 V	3 V			0.55	
I_I		V_I = V_{CC} or GND		3.6 V			±5	µA
$I_{I(hold)}$		V_I = 0.7 V		2.3 V	45			µA
		V_I = 1.7 V			–45			
		V_I = 0.8 V		3 V	75			
		V_I = 2 V			–75			
		V_I = 0 to 3.6 V‡		3.6 V			±500	
I_{OZ}§		V_O = V_{CC} or GND		3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	µA
ΔI_{CC}		One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND	3 V to 3.6 V			750	µA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		3.5		pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V		9		pF

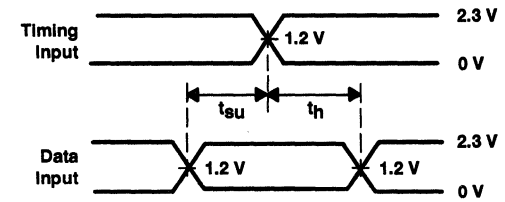
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

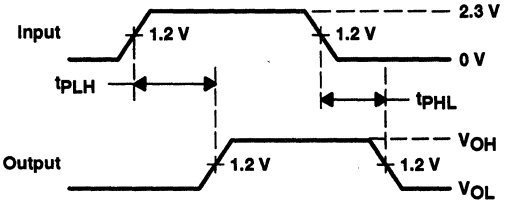


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND

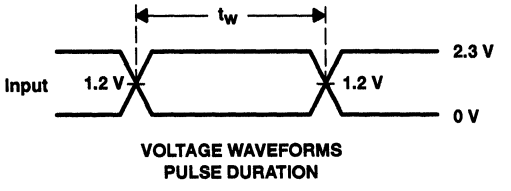
LOAD CIRCUIT



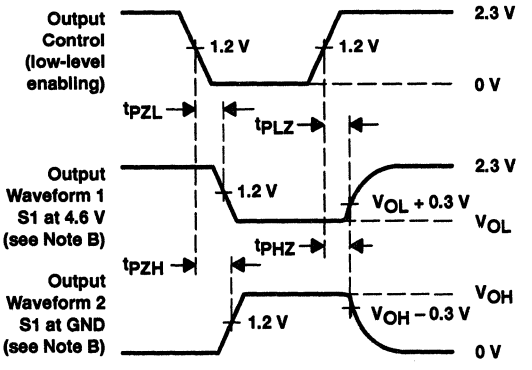
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



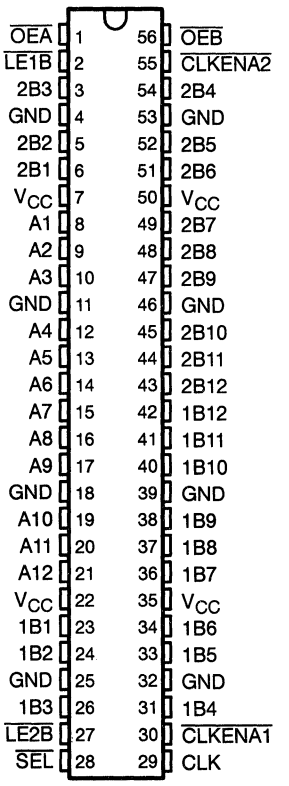
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Packaged in Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 12-bit to 24-bit bus exchanger is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16271 is intended for applications where two separate datapaths must be multiplexed onto, or demultiplexed from, a single datapath. This device is particularly suitable as an interface between conventional DRAMs and high-speed microprocessors.

A data is stored in the internal A-to-B registers on the low-to-high transition of the clock (CLK) input, provided that the $\overline{CLKENA}$ inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B port.

Transparent latches in the B-to-A path allow asynchronous operation in order to maximize memory access throughput. These latches transfer data when the latch-enable ($\overline{LE}$) inputs are low. The select ($\overline{SEL}$) line selects 1B or 2B data for the A outputs. Data flow is controlled by the active-low output enables ($\overline{OEA}$, $\overline{OEB}$).

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16271 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16271 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

Function Tables

OUTPUT ENABLE

INPUTS		OUTPUTS	
$\overline{OEA}$	$\overline{OEB}$	A	1B, 2B
H	H	Z	Z
H	L	Z	Active
L	H	Active	Z
L	L	Active	Active

A-TO-B STORAGE ($\overline{OEB}$ = L)

INPUTS				OUTPUTS	
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	A	1B	2B
H	H	X	X	$1B_0$†	$2B_0$†
L	X	↑	L	L	X
L	X	↑	H	H	X
X	L	↑	L	X	L
X	L	↑	H	A_0	H

B-TO-A STORAGE ($\overline{OEA}$ = L)

INPUTS				OUTPUT
$\overline{LE}$	$\overline{SEL}$	1B	2B	A
H	X	X	X	A_0†
H	X	X	X	A_0†
L	H	L	X	L
L	H	H	X	H
L	L	X	L	L
L	L	X	H	H

† Output level before the indicated steady-state input conditions were established

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, VI: Except I/O ports (see Note 1) ..... −0.5 V to 4.6 V
I/O ports (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... −50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

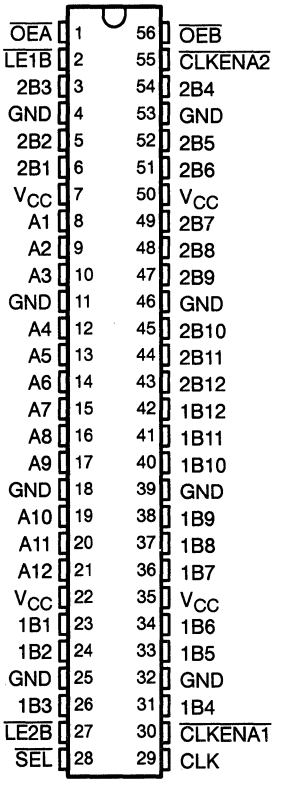
‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Packaged in Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 12-bit to 24-bit bus exchanger is designed for 2.3-V to 3.3-V V_{CC} operation.

The SN74ALVCH16272 is intended for applications where two separate datapaths must be multiplexed onto, or demultiplexed from, a single datapath. This device is particularly suitable as an interface between conventional DRAMs and high-speed microprocessors.

Data from the A inputs is stored in the internal registers on the low-to-high transition of the clock (CLK) input, when the $\overline{\text{CLKENA}}$ inputs are low. A two-stage pipeline is provided in each of the A-to-1B and A-to-2B paths to serve as a shallow write buffer.

Transparent latches are provided in the B-to-A path to allow asynchronous operation to maximize memory access throughput. These latches transfer data when the latch-enable ($\overline{\text{LE}}$) inputs are low. The select ($\overline{\text{SEL}}$) line selects 1B or 2B data for the A outputs. Data flow is controlled by the active-low output enables ($\overline{\text{OEA}}$, $\overline{\text{OEB}}$).

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16272 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16272 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

Function Tables

OUTPUT ENABLE

INPUTS		OUTPUTS	
$\overline{OEA}$	$\overline{OEB}$	A	1B, 2B
H	H	Z	Z
H	L	Z	Active
L	H	Active	Z
L	L	Active	Active

A-TO-B STORAGE ($\overline{OEB}$ = L)

INPUTS				OUTPUTS	
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	A	1B	2B
H	H	X	X	$1B_0$†	$2B_0$†
L	X	↑	L	L†	X
L	X	↑	H	H†	X
X	L	↑	L	X	L
X	L	↑	H	A_0	H

† Two CLK edges are needed to propagate data.

B-TO-A STORAGE ($\overline{OEA}$ = L)

INPUTS				OUTPUT
$\overline{LE}$	$\overline{SEL}$	1B	2B	A
H	X	X	X	A_0‡
H	X	X	X	A_0‡
L	H	L	X	L
L	H	H	X	H
L	L	X	L	L
L	L	X	H	H

‡ Output level before the indicated steady-state input conditions were established

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

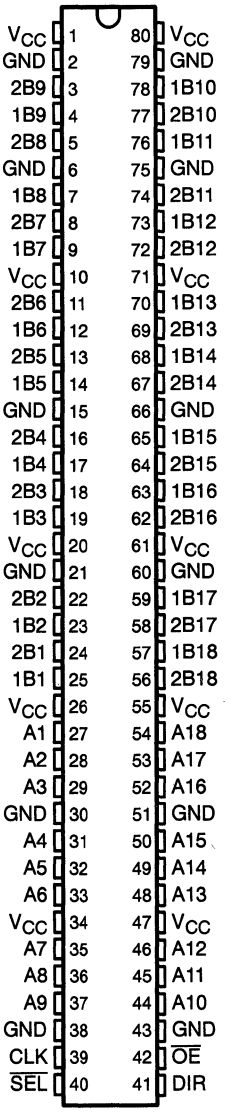
PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}		I_{OH} = −100 µA		2.3 V to 3.6 V	V_{CC}−0.2			V
		I_{OH} = −6 mA,	V_{IH} = 1.7 V	2.3 V	2			
		I_{OH} = −12 mA	V_{IH} = 1.7 V	2.3 V	1.7			
			V_{IH} = 2 V	2.7 V	2.2			
			V_{IH} = 2 V	3 V	2.4			
		I_{OH} = −24 mA,	V_{IH} = 2 V	3 V	2			
V_{OL}		I_{OL} = 100 µA		2.3 V to 3.6 V			0.2	V
		I_{OL} = 6 mA,	V_{IL} = 0.7 V	2.3 V			0.4	
		I_{OL} = 12 mA	V_{IL} = 0.7 V	2.3 V			0.7	
			V_{IL} = 0.8 V	2.7 V			0.4	
		I_{OL} = 24 mA,	V_{IL} = 0.8 V	3 V			0.55	
I_I		V_I = V_{CC} or GND		3.6 V			±5	µA
$I_{I(hold)}$		V_I = 0.7 V		2.3 V	45			µA
		V_I = 1.7 V			−45			
		V_I = 0.8 V		3 V	75			
		V_I = 2 V			−75			
		V_I = 0 to 3.6 V‡		3.6 V			±500	
I_{OZ}§		V_O = V_{CC} or GND		3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	µA
ΔI_{CC}		One input at V_{CC} − 0.6 V,	Other inputs at V_{CC} or GND	3 V to 3.6 V			750	µA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V				pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V				pF

† Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

PRODUCT PREVIEW

- **Member of the Texas Instruments Widebus™ Family**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Sub-Micron Process**
- **ESD Protection Exceeds 2000 V Per MIL-STD883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Packaged in Thin Shrink Small-Outline Package**

DBB PACKAGE
(TOP VIEW)



description

The SN74ALVCH16282 is an 18-bit to 36-bit registered bus exchanger designed for 2.3-V to 3.6-V V_{CC} operation. This part is intended for use in applications where data must be transferred from a narrow high-speed bus to a wide lower-frequency bus. It is designed specifically for low-voltage (3.3-V) V_{CC} operation.

The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the CLK input. For data transfer in the B-to-A direction, $\overline{SEL}$ selects 1B or 2B data for the A outputs.

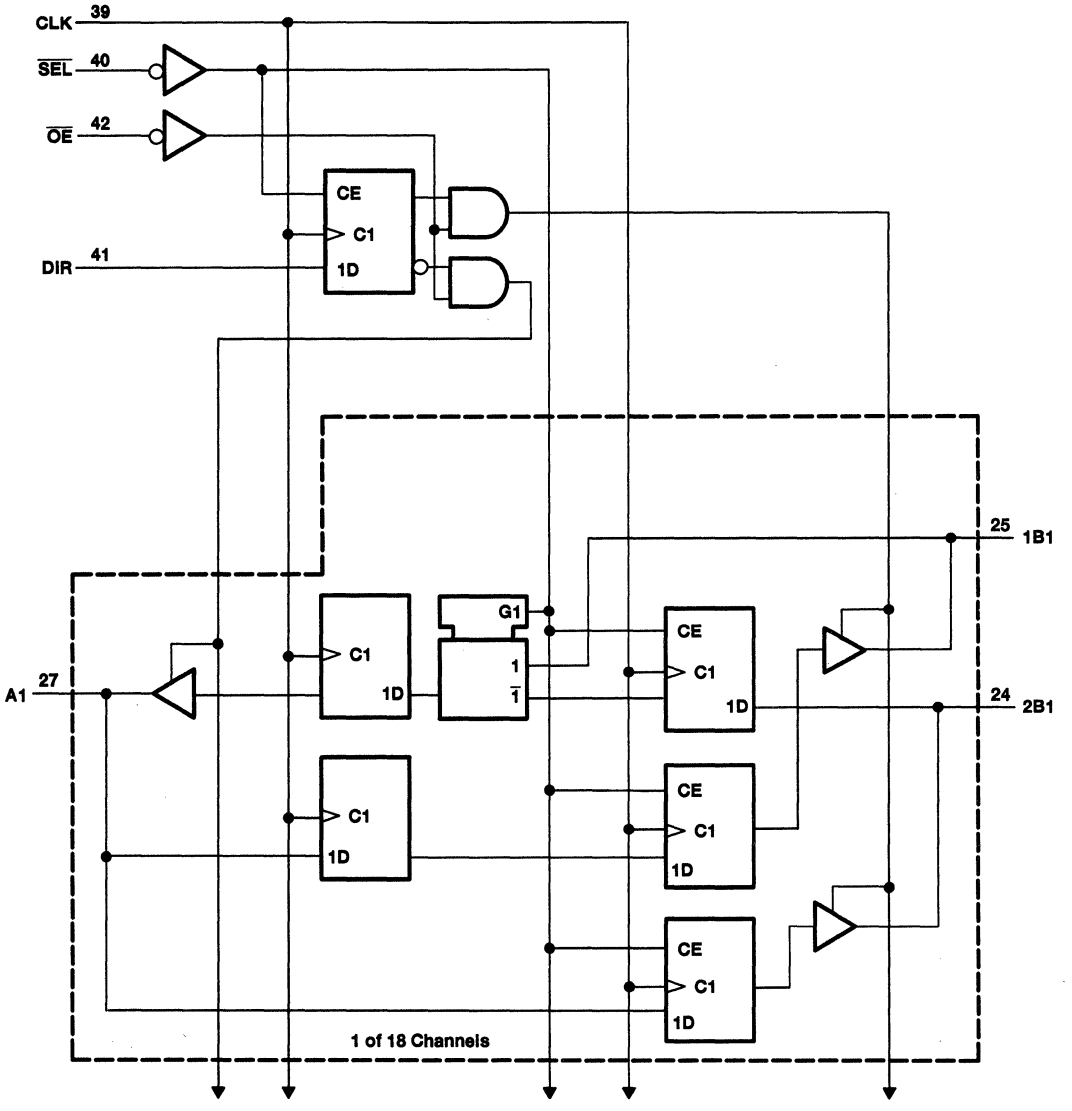
For data transfer in the A-to-B direction, a two-stage pipeline is provided in the 1B path, with a single storage register in the 2B path. Data flow is controlled by the active-low output enable ($\overline{OE}$) and the DIR input. The DIR control pin is registered to synchronize the bus direction changes with the clock.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16282 is characterized for operation from –40°C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic diagram (positive logic)



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

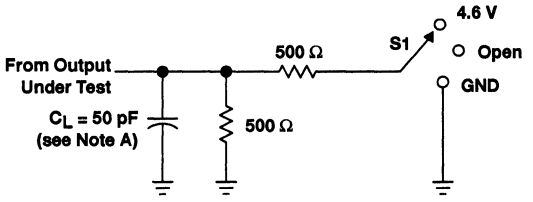
PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}		I_{OH} = –100 µA		2.3 V to 3.6 V	V_{CC}–0.2			V
		I_{OH} = –6 mA,	V_{IH} = 1.7 V	2.3 V	2			
		I_{OH} = –12 mA	V_{IH} = 1.7 V	2.3 V	1.7			
			V_{IH} = 2 V	2.7 V	2.2			
			V_{IH} = 2 V	3 V	2.4			
		I_{OH} = –24 mA,	V_{IH} = 2 V	3 V	2			
V_{OL}		I_{OL} = 100 µA		2.3 V to 3.6 V			0.2	V
		I_{OL} = 6 mA,	V_{IL} = 0.7 V	2.3 V			0.4	
		I_{OL} = 12 mA	V_{IL} = 0.7 V	2.3 V			0.7	
			V_{IL} = 0.8 V	2.7 V			0.4	
		I_{OL} = 24 mA,	V_{IL} = 0.8 V	3 V			0.55	
I_I		V_I = V_{CC} or GND		3.6 V			±5	µA
$I_{I(hold)}$		V_I = 0.7 V		2.3 V	45			µA
		V_I = 1.7 V			–45			
		V_I = 0.8 V		3 V	75			
		V_I = 2 V			–75			
		V_I = 0 to 3.6 V‡		3.6 V			±500	
I_{OZ}§		V_O = V_{CC} or GND		3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	µA
ΔI_{CC}		One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND	3 V to 3.6 V			750	µA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		4		pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V		8.5		pF

† Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

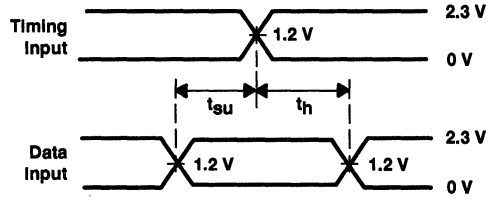
			V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			150		150		150	MHz
t_w	Pulse duration, CLK high or low		3.3		3.3		3.3		ns
t_{su}	Setup time	A data before CLK↑	2.4		2.3		2		ns
		B data before CLK↑	2.2		2.2		1.8		
		DIR before CLK↑	2.2		2.1		1.7		
		$\overline{SEL}$ before CLK↑	2		2		1.8		
t_h	Hold time	A data after CLK↑	0.5		0.5		0.7		ns
		B data after CLK↑	0.5		0.5		0.6		
		DIR after CLK↑	0.5		0.5		0.5		
		$\overline{SEL}$ after CLK↑	0.7		0.7		0.8		

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

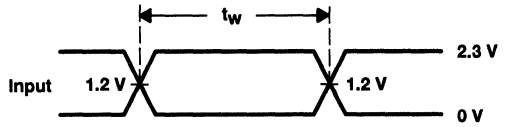


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND

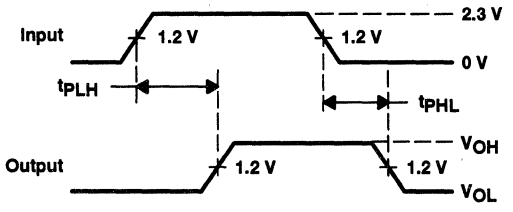
LOAD CIRCUIT



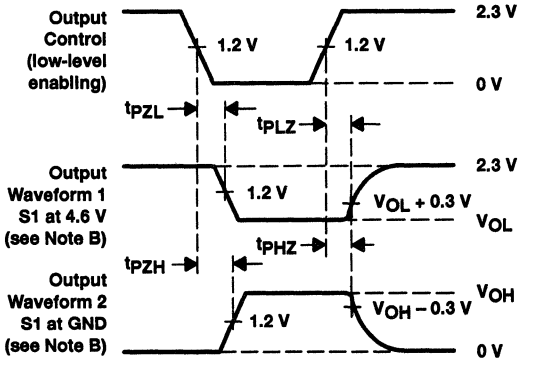
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



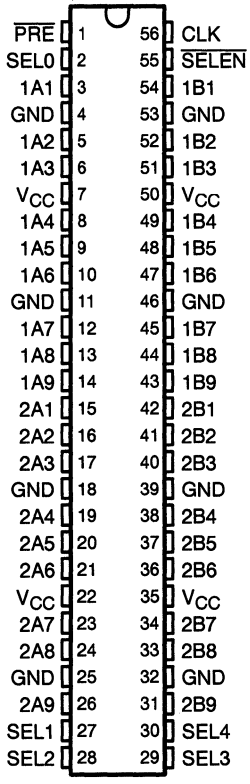
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus+*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- ***UBE*™ (Universal Bus Exchanger) Allows Synchronous Data Exchange**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 9-bit, 4-port universal bus exchanger is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16409 allows synchronous data exchange between four different buses.

Data flow is controlled by the select (SEL0–SEL4) inputs. A data-flow state is stored on the rising edge of the clock (CLK) input if the select-enable ($\overline{SELEN}$) input is low. Once a data-flow state has been established, data is stored in the flip-flop on the rising edge of CLK if $\overline{SELEN}$ is high.

The data-flow control logic is designed to allow glitch-free data transmission.

To ensure the high-impedance state during power up or power down, $\overline{SELEN}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16409 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16409 is characterized for operation from –40°C to 85°C.

Widebus+, EPIC, and UBE are trademarks of Texas Instruments Incorporated.

DATA-FLOW CONTROL FUNCTION TABLE

INPUTS							DATA FLOW
$\overline{SELEN}$	CLK	SEL0	SEL1	SEL2	SEL3	SEL4	
H	↑	X	X	X	X	X	No change
L	↑	0	0	0	0	0	None, all I/Os off
L	↑	0	0	0	0	1	Not used
L	↑	0	0	0	1	0	Not used
L	↑	0	0	0	1	1	Not used
L	↑	0	0	1	0	0	Not used
L	↑	0	0	1	0	1	Not used
L	↑	0	0	1	1	0	Not used
L	↑	0	0	1	1	1	Not used
L	↑	0	1	0	0	0	2A to 1A and 1B to 2B
L	↑	0	1	0	0	1	2A to 1A
L	↑	0	1	0	1	0	2B to 1B
L	↑	0	1	0	1	1	2A to 1A and 2B to 1B
L	↑	0	1	1	0	0	1A to 2A and 1B to 2B
L	↑	0	1	1	0	1	1A to 2A
L	↑	0	1	1	1	0	1B to 2B
L	↑	0	1	1	1	1	1A to 2A and 2B to 1B
L	↑	1	0	0	0	0	1A to 1B and 2B to 2A
L	↑	1	0	0	0	1	1A to 1B
L	↑	1	0	0	1	0	2A to 2B
L	↑	1	0	0	1	1	1A to 1B and 2A to 2B
L	↑	1	0	1	0	0	1B to 1A and 2A to 2B
L	↑	1	0	1	0	1	1B to 1A
L	↑	1	0	1	1	0	2B to 2A
L	↑	1	0	1	1	1	1B to 1A and 2B to 2A
L	↑	1	1	0	0	0	2B to 1A and 2A to 1B
L	↑	1	1	0	0	1	1B to 2A
L	↑	1	1	0	1	0	2B to 1A
L	↑	1	1	0	1	1	2B to 1A and 1B to 2A
L	↑	1	1	1	0	0	1A to 2B and 1B to 2A
L	↑	1	1	1	0	1	1A to 2B
L	↑	1	1	1	1	0	2A to 1B
L	↑	1	1	1	1	1	1A to 2B and 2A to 1B

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

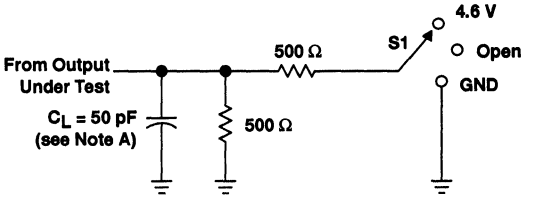
PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}		I_{OH} = –100 µA		2.3 V to 3.6 V	V_{CC}–0.2			V
		I_{OH} = –6 mA,	V_{IH} = 1.7 V	2.3 V	2			
		I_{OH} = –12 mA	V_{IH} = 1.7 V	2.3 V	1.7			
			V_{IH} = 2 V	2.7 V	2.2			
			V_{IH} = 2 V	3 V	2.4			
		I_{OH} = –24 mA,	V_{IH} = 2 V	3 V	2			
V_{OL}		I_{OL} = 100 µA,		2.3 V to 3.6 V			0.2	V
		I_{OL} = 6 mA,	V_{IL} = 0.7 V	2.3 V			0.4	
		I_{OL} = 12 mA	V_{IL} = 0.7 V	2.3 V			0.7	
			V_{IL} = 0.8 V	2.7 V			0.4	
		I_{OL} = 24 mA,	V_{IL} = 0.8 V	3 V			0.55	
I_I		V_I = V_{CC} or GND		3.6 V			±5	µA
$I_{I(hold)}$		V_I = 0.7 V		2.3 V	45			µA
		V_I = 1.7 V			–45			
		V_I = 0.8 V		3 V	75			
		V_I = 2 V			–75			
		V_I = 0 to 3.6 V‡		3.6 V			±500	
I_{OZ}§		V_O = V_{CC} or GND		3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	µA
ΔI_{CC}		One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND	3 V to 3.6 V			750	µA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		4		pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V		8		pF

† All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

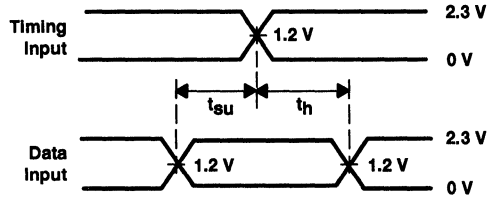
			V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	120	0	120	0	120	MHz
t_w	Pulse duration, CLK high or low		4.2		4.2		3		ns
t_{su}	Setup time	A or B before CLK↑	1.9		1.9		1.4		ns
		SEL before CLK↑	5.1		4.2		3.5		
		$\overline{SELEN}$ before CLK↑	2.5		2.5		1.8		
		$\overline{PRE}$ before CLK↑	1		1		0.7		
t_h	Hold time	A or B after CLK↑	0.8		0.8		1		ns
		SEL after CLK↑	0		0		0		
		$\overline{SELEN}$ after CLK↑	0.5		0.5		0.8		

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

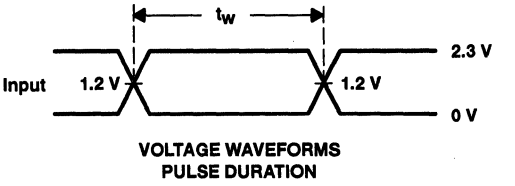


LOAD CIRCUIT

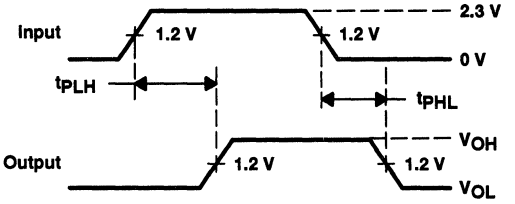
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND



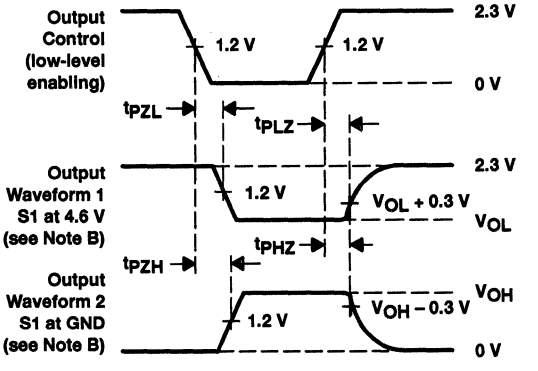
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



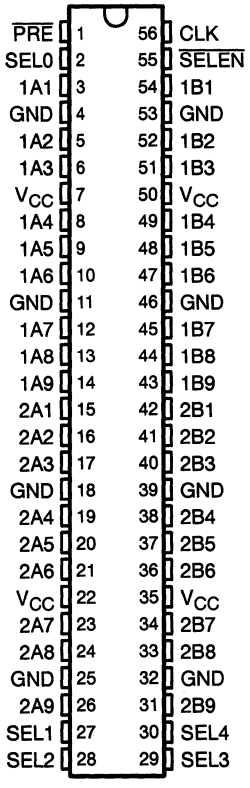
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus+*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **B-Port Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors are Required**
- ***UBE*™ (Universal Bus Exchanger) Allows Synchronous Data Exchange**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 9-bit 4-port universal bus exchanger is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCHR162409 allows synchronous data exchange between four different buses. Data flow is controlled by the select (SEL0–SEL4) inputs. A data-flow state is stored on the rising edge of the clock (CLK) input, provided the select-enable ($\overline{SELEN}$) input is low. Once a data-flow state is established, data is stored in the flip-flop on the rising edge of the CLK, provided $\overline{SELEN}$ is high.

The data-flow control logic is designed to allow glitch-free data transmission.

The B outputs, which are designed to sink up to 12 mA, include 26-Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{SELEN}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCHR162409 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCHR162409 is characterized for operation from –40°C to 85°C.

Widebus+, EPIC, and UBE are trademarks of Texas Instruments Incorporated.

DATA-FLOW CONTROL FUNCTION TABLE

INPUTS							DATA FLOW
$\overline{SELEN}$	CLK	SEL0	SEL1	SEL2	SEL3	SEL4	
H	↑	X	X	X	X	X	No change
L	↑	0	0	0	0	0	None, all I/Os off
L	↑	0	0	0	0	1	Not used
L	↑	0	0	0	1	0	Not used
L	↑	0	0	0	1	1	Not used
L	↑	0	0	1	0	0	Not used
L	↑	0	0	1	0	1	Not used
L	↑	0	0	1	1	0	Not used
L	↑	0	0	1	1	1	Not used
L	↑	0	1	0	0	0	2A to 1A and 1B to 2B
L	↑	0	1	0	0	1	2A to 1A
L	↑	0	1	0	1	0	2B to 1B
L	↑	0	1	0	1	1	2A to 1A and 2B to 1B
L	↑	0	1	1	0	0	1A to 2A and 1B to 2B
L	↑	0	1	1	0	1	1A to 2A
L	↑	0	1	1	1	0	1B to 2B
L	↑	0	1	1	1	1	1A to 2A and 2B to 1B
L	↑	1	0	0	0	0	1A to 1B and 2B to 2A
L	↑	1	0	0	0	1	1A to 1B
L	↑	1	0	0	1	0	2A to 2B
L	↑	1	0	0	1	1	1A to 1B and 2A to 2B
L	↑	1	0	1	0	0	1B to 1A and 2A to 2B
L	↑	1	0	1	0	1	1B to 1A
L	↑	1	0	1	1	0	2B to 2A
L	↑	1	0	1	1	1	1B to 1A and 2B to 2A
L	↑	1	1	0	0	0	2B to 1A and 2A to 1B
L	↑	1	1	0	0	1	1B to 2A
L	↑	1	1	0	1	0	2B to 1A
L	↑	1	1	0	1	1	2B to 1A and 1B to 2A
L	↑	1	1	1	0	0	1A to 2B and 1B to 2A
L	↑	1	1	1	0	1	1A to 2B
L	↑	1	1	1	1	0	2A to 1B
L	↑	1	1	1	1	1	1A to 2B and 2A to 1B

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

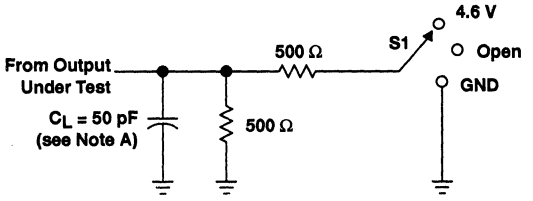
PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}	I_{OH} = –100 µA		2.3 V to 3.6 V	V_{CC}–0.2			V
	I_{OH} = –4 mA,	V_{IH} = 1.7 V	2.3 V	1.9			
	I_{OH} = –6 mA	V_{IH} = 1.7 V	2.3 V	1.7			
		V_{IH} = 2 V	3 V	2.4			
	I_{OH} = –8 mA,	V_{IH} = 2 V	2.7 V	2			
	I_{OH} = –12 mA,	V_{IH} = 2 V	3 V	2			
V_{OL}	I_{OL} = 100 µA		2.3 V to 3.6 V			0.2	V
	I_{OL} = 4 mA,	V_{IL} = 0.7 V	2.3 V			0.4	
	I_{OL} = 6 mA	V_{IL} = 0.7 V	2.3 V			0.55	
		V_{IL} = 0.8 V	3 V			0.55	
	I_{OL} = 8 mA,	V_{IL} = 0.8 V	2.7 V			0.6	
	I_{OL} = 12 mA,	V_{IL} = 0.8 V	3 V			0.8	
I_I	V_I = V_{CC} or GND		3.6 V			±5	µA
$I_{I(hold)}$	V_I = 0.7 V		2.3 V	45			µA
	V_I = 1.7 V			–45			
	V_I = 0.8 V		3 V	75			
	V_I = 2 V			–75			
	V_I = 0 to 3.6 V‡		3.6 V			±500	
I_{OZ}§	V_O = V_{CC} or GND		3.6 V			±10	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	µA
ΔI_{CC}	One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND	3 V to 3.6 V			750	µA
C_i Control inputs	V_I = V_{CC} or GND		3.3 V		4		pF
C_{io} A or B ports	V_O = V_{CC} or GND		3.3 V		8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

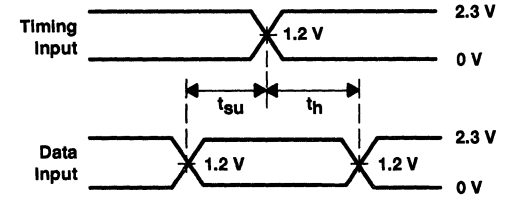
			V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	120	0	120	0	120	MHz
t_w	Pulse duration	CLK high or low	4.2		4.2		3		ns
t_{su}	Setup time	A or B before CLK↑	1.9		1.9		1.4		ns
		SEL before CLK↑	5.1		4.2		3.5		
		$\overline{SELEN}$ before CLK↑	2.5		2.5		1.8		
		$\overline{PRE}$ before CLK↑	1		1		0.7		
t_h	Hold time	A or B after CLK↑	0.8		0.8		1		ns
		S after CLK↑	0		0		0		
		$\overline{SELEN}$ after CLK↑	0.5		0.5		0.8		

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

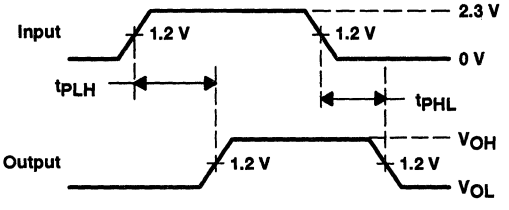


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND

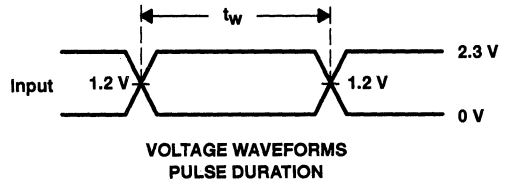
LOAD CIRCUIT



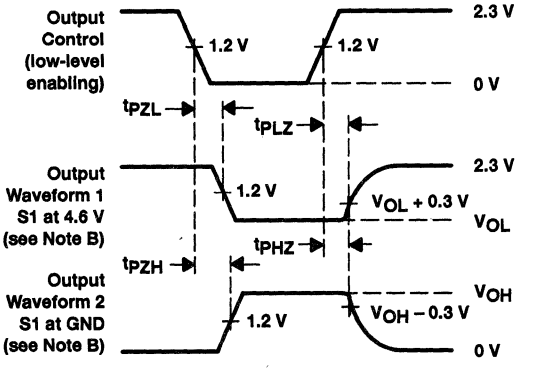
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

SCDS009F – MAY 1995 – REVISED AUGUST 1996

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG) and 300-mil Shrink Small-Outline (DL) Packages**

description

The SN74CBT16232 is a 16-bit to 32-bit synchronous switch used in applications in which two separate datapaths must be multiplexed onto, or demultiplexed from, a single path.

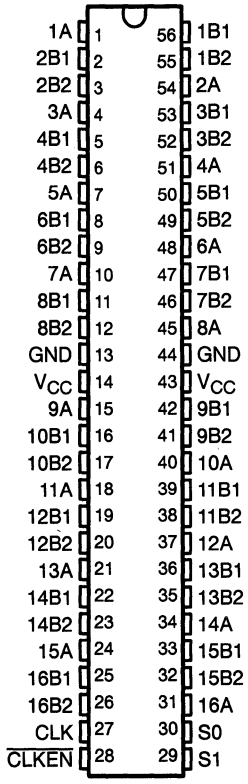
Two select inputs (S0 and S1) control the data flow. A clock (CLK) and a clock enable ($\overline{\text{CLKEN}}$) synchronize the device operation. When $\overline{\text{CLKEN}}$ is high, the bus switch remains in the last clocked function.

The SN74CBT16232 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

S1	S0	CLK	$\overline{\text{CLKEN}}$	FUNCTION
X	X	X	H	Last state
L	L	↑	L	Disconnect
L	H	↑	L	A = B1 and A = B2
H	L	↑	L	A = B1
H	H	↑	L	A = B2

DGG OR DL PACKAGE
(TOP VIEW)



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA					–1.2	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V or GND					±1	μA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND				3	μA
ΔI_{CC}‡	Control pins	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND				2.5	mA
C_I	Control pins	V_I = 3 V or 0					4.5		pF
$C_{io(OFF)}$	A port	V_O = 3 V or 0,	$\overline{CLKEN}$ = 0,	S0 = 0,	S1 = 0		6.5		pF
	B port						4		
r_{on}§		V_{CC} = 4 V,	V_I = 2.4 V,	I_I = 15 mA			14	20	Ω
		V_{CC} = 4.5 V	V_I = 0,	I_I = 64 mA			5	7	
			V_I = 0,	I_I = 30 mA			5	7	
			V_I = 2.4 V,	I_I = 15 mA			10	15	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			V_{CC} = 5 V ±0.5 V		V_{CC} = 4 V		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	MHz
t_w	Pulse duration	CLK high or low	3.3		3.3		ns
t_{su}	Setup time	S0, S1 before CLK↑	1.9		2.2		ns
		$\overline{CLKEN}$ before CLK↑	1.9		2.4		
t_h	Hold time	S0, S1 after CLK↑	1		0.5		ns
		$\overline{CLKEN}$ after CLK↑	1.8		1.9		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V ±0.5 V		V_{CC} = 4 V		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			150		150		MHz
t_{pd}¶	A or B	B or A		0.25		0.25	ns
t_{pd}	CLK	A or B	2	5.8		6.1	ns
t_{en}	CLK	A, B1, B2	1.8	6.2		6.8	ns
t_{en}	CLK	B1 or B2	3.1	7.9		8.5	ns
t_{dis}	CLK	A or B	1.9	6.2		5.8	ns

¶ This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

SCDS010D – MAY 1995 – REVISED AUGUST 1996

- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input and Output Levels**
- **Package Options Include Plastic Thin Shrink Small-Outline (DGG) and 300-mil Shrink Small-Outline (DL) Packages**

description

The SN74CBT16233 is a 16-bit to 32-bit switch used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single path. This device can be used for memory interleaving, where two different banks of memory need to be addressed simultaneously. The SN74CBT16233 can be used as two 8-bit to 16-bit multiplexers or as one 16-bit to 32-bit multiplexer.

Two select inputs (SEL1 and SEL2) control the data flow. When the TEST inputs are asserted, the A port is connected to both the B1 and the B2 ports. SEL1, SEL2, and the TEST inputs can be driven with a 5-V CMOS, a 5-V TTL, or a low-voltage TTL driver.

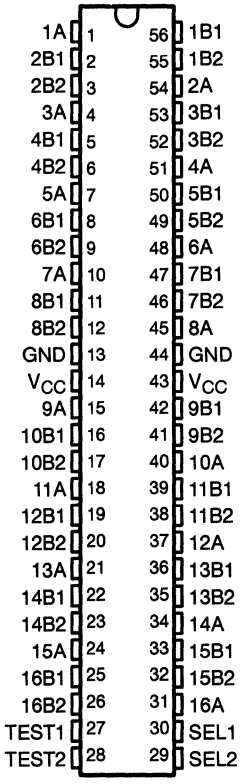
The SN74CBT16233 is specified by design not to have through current when switching directions.

The SN74CBT16233 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS		FUNCTION
SEL	TEST	
L	L	A = B1
H	L	A = B2
X	H	A = B1 and A = B2

DGG OR DL PACKAGE
(TOP VIEW)



recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.25	V
V_{IH}	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = –18 mA				–1.2	V
I_I		V_{CC} = 0	V_I = 5.25 V				10	µA
		V_{CC} = 5.25 V,	V_I = 5.25 V or GND				±1	µA
I_{CC}		V_{CC} = 5.25 V,	I_O = 0,	V_I = V_{CC} or GND			3	µA
ΔI_{CC}‡	Control pins	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_I	Control pins	V_I = 3 V or 0				4.5		pF
$C_{io(OFF)}$		V_O = 3 V or 0				4		pF
r_{on}§		V_{CC} = 4.75 V	V_I = 0,	I_I = 64 mA		5	7	Ω
			V_I = 2.4 V,	I_I = 30 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		7	12	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A, B) terminals.

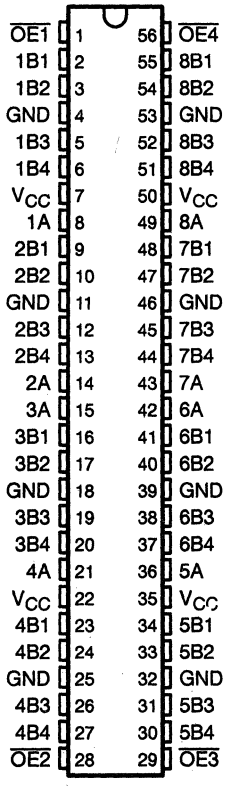
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 0°C TO 70°C		UNIT
			MIN	MAX	
t_{pd}¶	A or B	B or A		0.25	ns
t_{pd}	SEL	A	1.6	5.3	ns
t_{en}	TEST or SEL	B	1.3	5.2	ns
t_{dis}			1	5.3	

¶ This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74ALVCH16344 is a 1-bit to 4-bit address driver used in applications where four separate memory locations must be addressed by a single address.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN74ALVCH16344 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16344 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS		OUTPUT
$\overline{OE}$	A	BN
L	H	H
L	L	L
H	H	Z

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I: Except I/O ports (see Note 1) ..... –0.5 V to 4.6 V
I/O ports (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... –50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		–12	mA
		V_{CC} = 2.7 V		–12	
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		12	mA
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

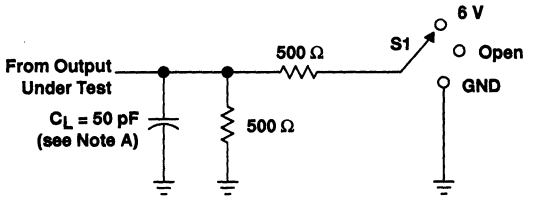
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.3	5.2		4.6	1.4	4	ns
t_{en}	$\overline{OE}$	B	1.1	6.7		6.2	1.2	5.1	ns
t_{dis}	$\overline{OE}$	B	1.5	5.3		4.4	1.2	4	ns
$t_{sk(o)}$†								0.35	ns
$t_{sk(o)}$‡								0.5	ns

† Skew between outputs of same bank and same package (same transition). This parameter is warranted but not production tested.
‡ Skew between outputs of all banks and same package (A1 through A8 tied together). This parameter is warranted but not production tested.

operating characteristics, T_A = 25°C

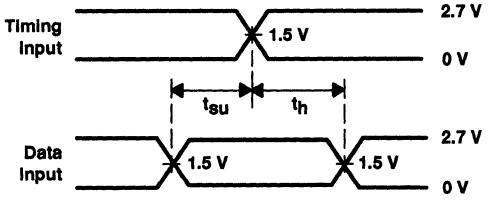
PARAMETER			TEST CONDITIONS		V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V	UNIT
					TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF,	f = 10 MHz	68	84	pF
		Outputs disabled			11	14	

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V

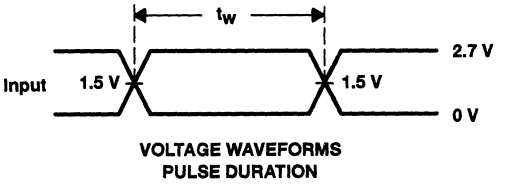


LOAD CIRCUIT

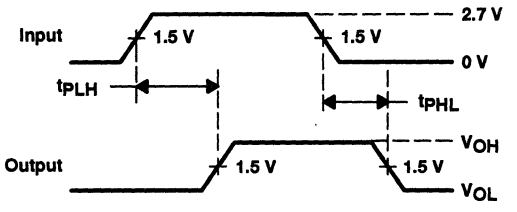
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



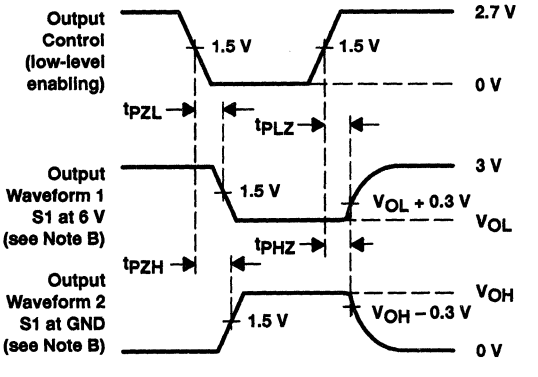
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



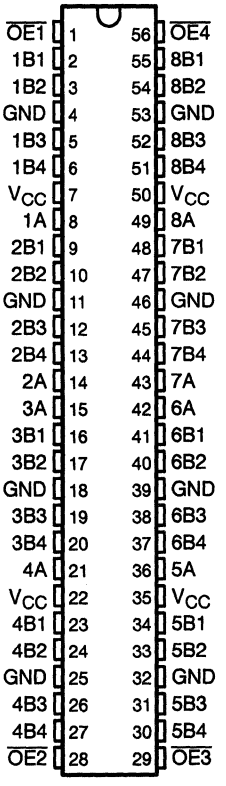
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DGG) and Thin Shrink Small-Outline (DL) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74ALVCH162344 is a 1-bit-to-4-bit address driver used in applications where four separate memory locations must be addressed by a single address.

The outputs, which are designed to sink up to 12 mA, include 26-Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN74ALVCH162344 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH162344 is characterized for operation from –40°C to 85°C.

A-TO-B FUNCTION TABLE

INPUTS		OUTPUT
$\overline{OE}$	A	Bn
L	H	H
L	L	L
H	X	Z

PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		–6	mA
		V_{CC} = 2.7 V		–8	
		V_{CC} = 3 V		–12	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		6	mA
		V_{CC} = 2.7 V		8	
		V_{CC} = 3 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

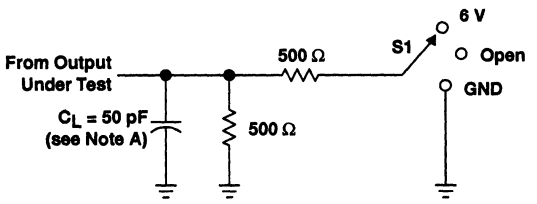
PRODUCT PREVIEW

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 0, f = 10 MHz			pF
		Outputs disabled				

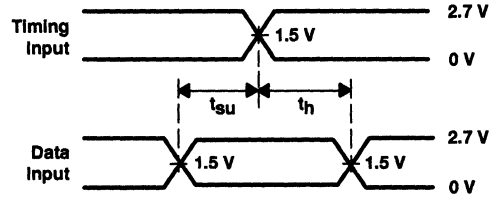
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V

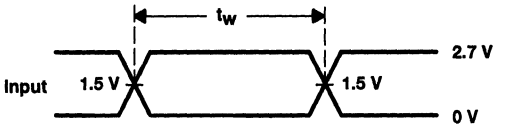


LOAD CIRCUIT

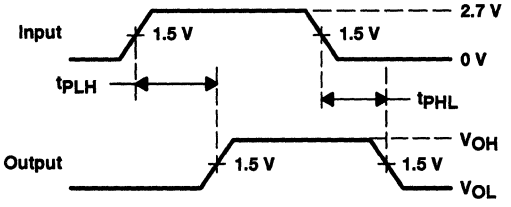
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



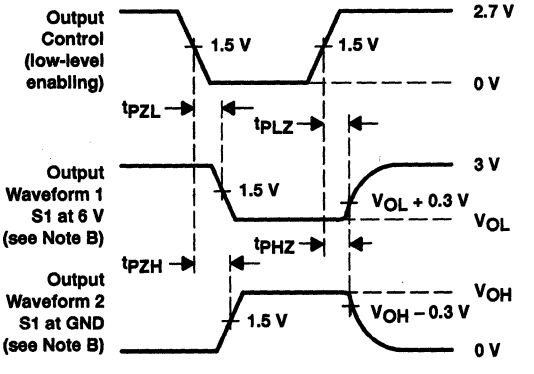
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **High-Impedance State During Power Up**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Packaged in Plastic 300-mil Thin Shrink Small-Outline Package**

description

This 1-bit-to-4-bit address register/driver is designed for 2.3-V to 3.6-V V_{CC} operation. The device is ideal for use in applications where a single address bus is driving four separate memory locations. The SN74ALVCH16831 can be used as a buffer or a register, depending on the logic level of the select ($\overline{SEL}$) input.

When $\overline{SEL}$ is logic high, the device is in the buffer mode. The outputs follow the inputs and are controlled by the two output-enable ($\overline{OE}$) controls. Each $\overline{OE}$ controls two groups of nine outputs.

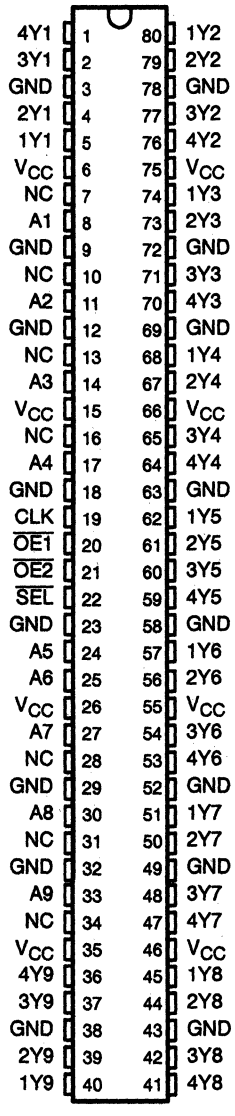
When $\overline{SEL}$ is logic low, the device is in the register mode. The register is an edge-triggered D-type flip-flop. On the positive transition of the clock (CLK) input, data set up at the A inputs is stored in the internal registers. $\overline{OE}$ controls operate the same as in buffer mode.

When $\overline{OE}$ is logic low, the outputs are in a normal logic state (high or low logic level). When $\overline{OE}$ is logic high, the outputs are in the high-impedance state.

$\overline{SEL}$ or $\overline{OE}$ does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

When V_{CC} is between 0 and 1.2 V, the device is in the high-impedance state during power up. However, to ensure the high-impedance state above 1.2 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

DBB PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCT PREVIEW

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3) ..... 0.84 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		–12	mA
		V_{CC} = 2.7 V		–12	
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		12	mA
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		μs/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

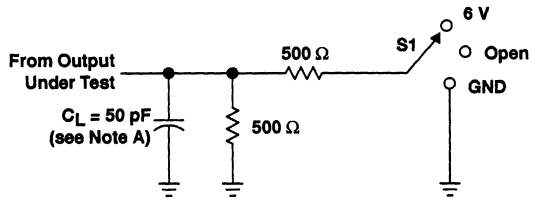
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			150		150		150		MHz
t_{pd}	A	Y							ns
	CLK								
	$\overline{SEL}$								
t_{en}	$\overline{OE}$	Y							ns
t_{dis}	$\overline{OE}$	Y							ns

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 0 pF, f = 10 MHz			pF
		Outputs disabled				

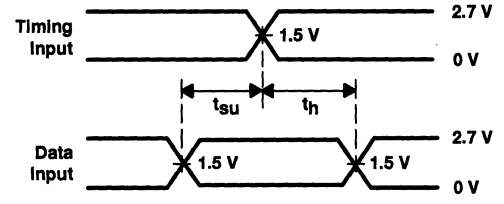
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V

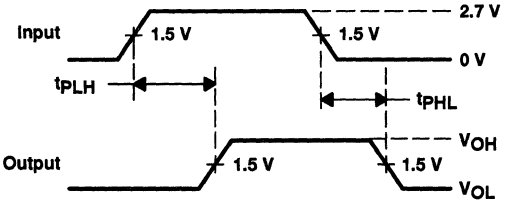


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

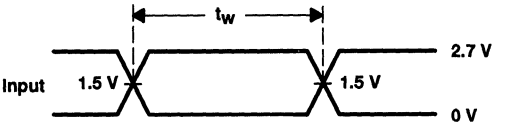
LOAD CIRCUIT



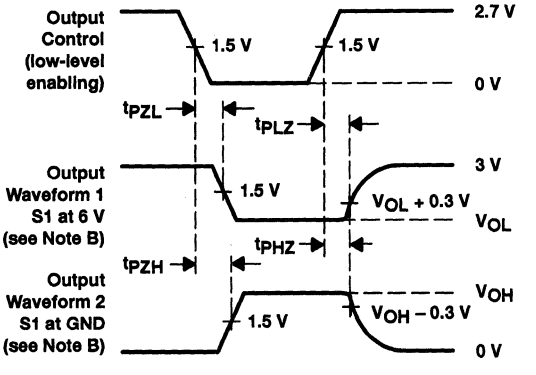
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

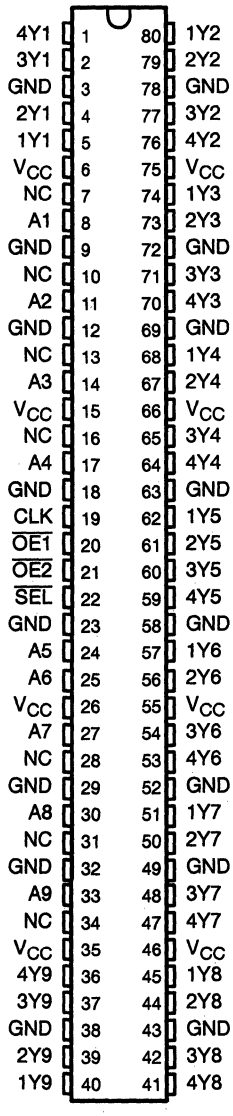
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**
- **High-Impedance State During Power Up**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Packaged in Plastic 300-mil Thin Shrink Small-Outline Package**

DBB PACKAGE
(TOP VIEW)



NC – No internal connection

description

This 1-bit-to-4-bit address register/driver is designed for 2.3-V to 3.6-V V_{CC} operation. The device is ideal for use in applications where a single address bus is driving four separate memory locations. The SN74ALVCH162831 can be used as a buffer or a register, depending on the logic level of the select ($\overline{SEL}$) input.

When $\overline{SEL}$ is logic high, the device is in the buffer mode. The outputs follow the inputs and are controlled by the two output-enable ($\overline{OE}$) controls. Each $\overline{OE}$ controls two groups of nine outputs.

When $\overline{SEL}$ is logic low, the device is in the register mode. The register is an edge-triggered D-type flip-flop. On the positive transition of the clock (CLK) input, data set up at the A inputs is stored in the internal registers. $\overline{OE}$ controls operate the same as in buffer mode.

When $\overline{OE}$ is logic low, the outputs are in a normal logic state (high or low logic level). When $\overline{OE}$ is logic high, the outputs are in high-impedance state.

$\overline{SEL}$ or $\overline{OE}$ does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to sink up to 12 mA, include 26-Ω resistors to reduce overshoot and undershoot.

PRODUCT PREVIEW

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... –50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3) ..... 0.84 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		–6	mA
		V_{CC} = 2.7 V		–8	
		V_{CC} = 3 V		–12	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		6	mA
		V_{CC} = 2.7 V		8	
		V_{CC} = 3 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		µs/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

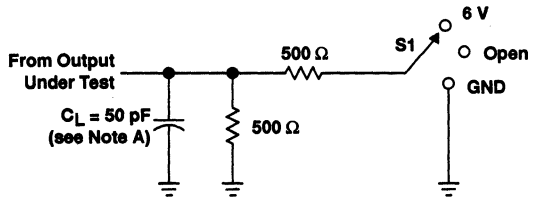
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			150		150		150		MHz
t_{pd}	A	Y							ns
	CLK								
	$\overline{SEL}$								
t_{en}	$\overline{OE}$	Y							ns
t_{dis}	$\overline{OE}$	Y							ns

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 0 pF, f = 10 MHz			pF
		Outputs disabled				

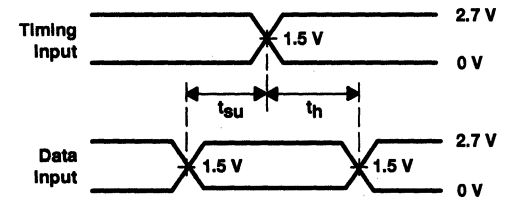
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V

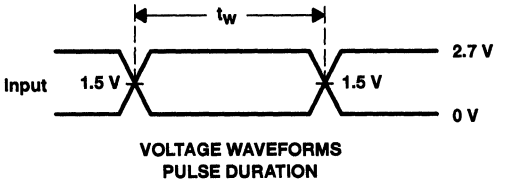


LOAD CIRCUIT

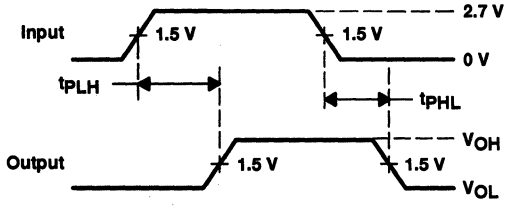
TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 6 V GND



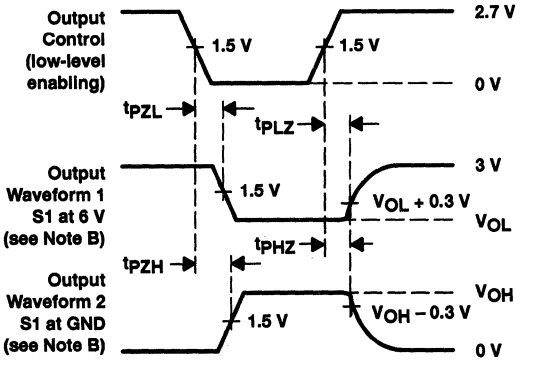
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



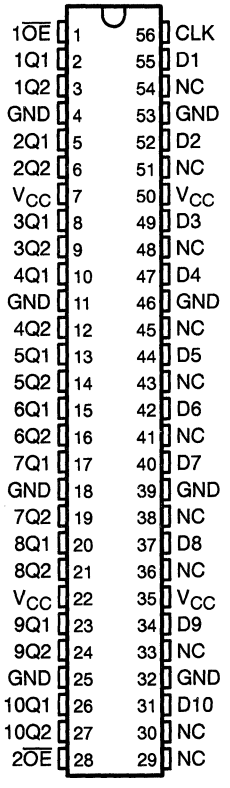
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



NC – No internal connection

description

This 10-bit flip-flop is designed for 2.3-V to 3.6-V V_{CC} operation.

The flip-flops of the SN74ALVCH16820 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the ten outputs in either a normal logic state (high or low logic level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16820 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16820 is characterized for operation from –40°C to 85°C.

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recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		–12	mA
		V_{CC} = 2.7 V		–12	
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		12	mA
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

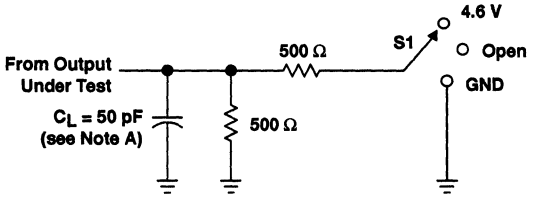
NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}		I_{OH} = –100 µA		2.3 V to 3.6 V	V_{CC}–0.2			V
		I_{OH} = –6 mA,	V_{IH} = 1.7 V	2.3 V	2			
		I_{OH} = –12 mA	V_{IH} = 1.7 V	2.3 V	1.7			
			V_{IH} = 2 V	2.7 V	2.2			
			V_{IH} = 2 V	3 V	2.4			
		I_{OH} = –24 mA,	V_{IH} = 2 V	3 V	2			
V_{OL}		I_{OL} = 100 µA		2.3 V to 3.6 V			0.2	V
		I_{OL} = 6 mA,	V_{IL} = 0.7 V	2.3 V			0.4	
		I_{OL} = 12 mA	V_{IL} = 0.7 V	2.3 V			0.7	
			V_{IL} = 0.8 V	2.7 V			0.4	
		I_{OL} = 24 mA,	V_{IL} = 0.8 V	3 V			0.55	
I_I		V_I = V_{CC} or GND		3.6 V			±5	µA
$I_{I(hold)}$		V_I = 0.7 V		2.3 V	45			µA
		V_I = 1.7 V			–45			
		V_I = 0.8 V		3 V	75			
		V_I = 2 V			–75			
		V_I = 0 to 3.6 V‡		3.6 V			±500	
I_{OZ}		V_O = V_{CC} or GND		3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	µA
ΔI_{CC}		One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND	3 V to 3.6 V			750	µA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		3.5		pF
	Data inputs					6		
C_o	Outputs	V_O = V_{CC} or GND		3.3 V		7		pF

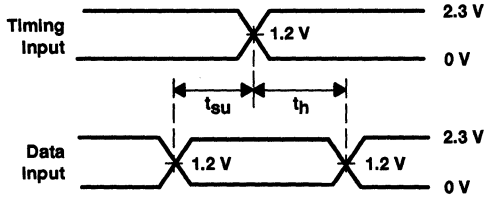
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

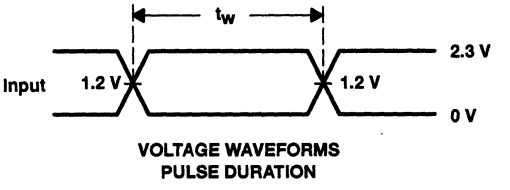


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND

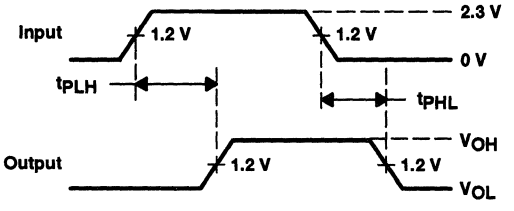
LOAD CIRCUIT



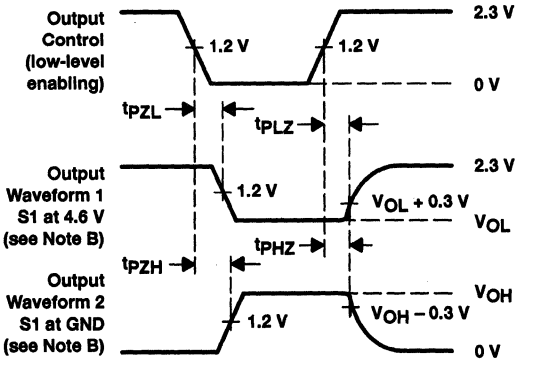
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



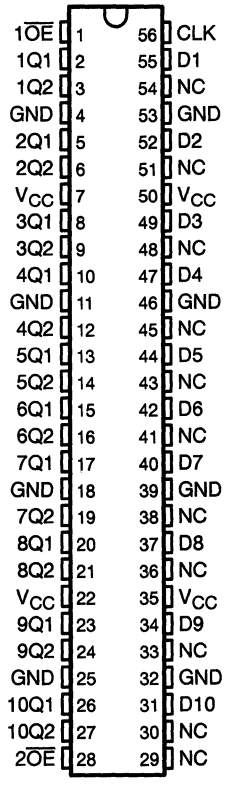
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required.**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



NC – No internal connection

description

This 10-bit flip-flop is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH162820 flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to sink up to 12 mA, include 26-Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

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recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		–6	mA
		V_{CC} = 2.7 V		–8	
		V_{CC} = 3 V		–12	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		6	mA
		V_{CC} = 2.7 V		8	
		V_{CC} = 3 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	150	0	150	0	150	MHz
t_w	Pulse duration, CLK high or low	3.3		3.3		3.3		ns
t_{su}	Setup time, data before CLK↑	1.7		1.8		1.4		ns
t_h	Hold time, data after CLK↑	1.1		1.1		1		ns

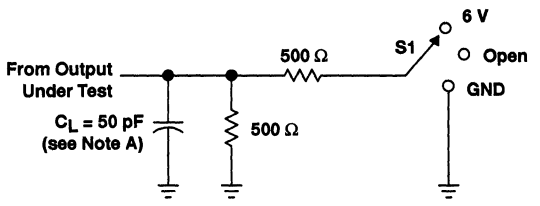
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			150		150		150		MHz
t_{pd}	CLK	Q	1	7		6.2	1	5.4	ns
t_{en}	$\overline{OE}$	Q	1	7.4		6.8	1	5.6	ns
t_{dis}	$\overline{OE}$	Q	1.3	6.4		5.5	1	5	ns

operating characteristics, T_A = 25°C

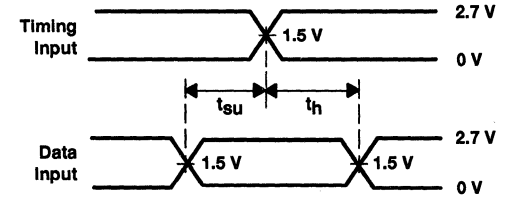
PARAMETER			TEST CONDITIONS	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 10 MHz	68	66	pF
		Outputs disabled		39	47	

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V

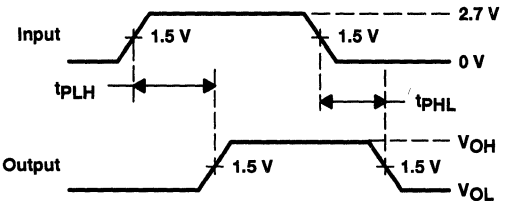


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

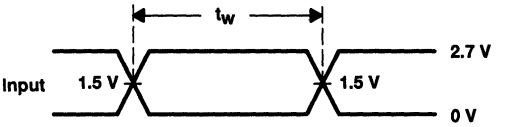
LOAD CIRCUIT



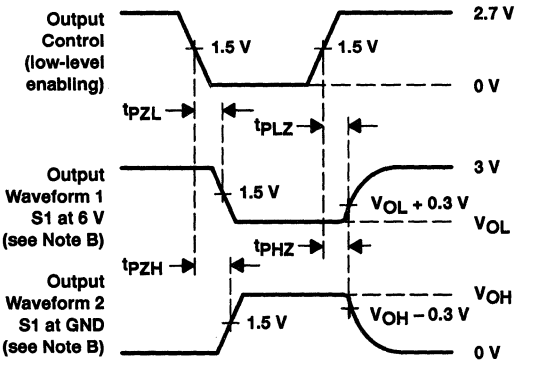
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Member of the Texas Instruments *Widebus*™ Family**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

description

This 16-bit universal bus driver is designed for 2.3-V to 3.6-V V_{CC} operation.

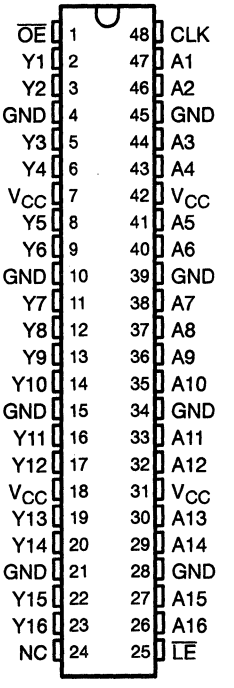
Data flow from A to Y is controlled by the output-enable ($\overline{OE}$) input. The device operates in the transparent mode when the latch-enable ($\overline{LE}$) input is low. The A data is latched if the clock (CLK) input is held at a high or low logic level. If $\overline{LE}$ is high, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLK. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16334 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16334 is characterized for operation from –40°C to 85°C.

DGG OR DL PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCT PREVIEW

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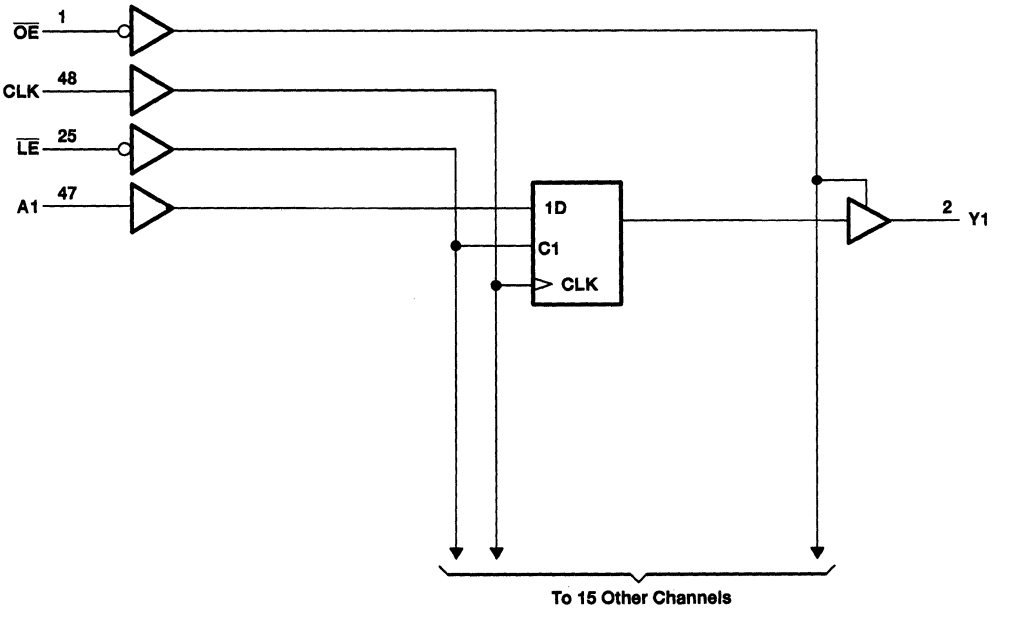
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}		I_{OH} = –100 µA		2.3 V to 3.6 V	V_{CC}–0.2			V
		I_{OH} = –6 mA,	V_{IH} = 1.7 V	2.3 V	2			
		I_{OH} = –12 mA	V_{IH} = 1.7 V	2.3 V	1.7			
			V_{IH} = 2 V	2.7 V	2.2			
			V_{IH} = 2 V	3 V	2.4			
		I_{OH} = –24 mA,	V_{IH} = 2 V	3 V	2			
V_{OL}		I_{OL} = 100 µA		2.3 V to 3.6 V			0.2	V
		I_{OL} = 6 mA,	V_{IL} = 0.7 V	2.3 V			0.4	
		I_{OL} = 12 mA	V_{IL} = 0.7 V	2.3 V			0.7	
			V_{IL} = 0.8 V	2.7 V			0.4	
		I_{OL} = 24 mA,	V_{IL} = 0.8 V	3 V			0.55	
I_I		V_I = V_{CC} or GND		3.6 V			±5	µA
I_{hold}		V_I = 0.7 V		2.3 V	45			µA
		V_I = 1.7 V			–45			
		V_I = 0.8 V		3 V	75			
		V_I = 2 V			–75			
		V_I = 0 to 3.6 V‡		3.6 V			±500	
I_{OZ}§		V_O = V_{CC} or GND		3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	µA
ΔI_{CC}		One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND	3 V to 3.6 V			750	µA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V				pF
	Data inputs							
C_o	Outputs	V_O = V_{CC} or GND		3.3 V				pF

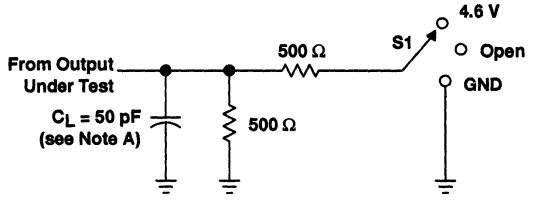
† All typical values are at V_{CC} = 3.3 V.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	$\overline{LE}$ low							ns
		CLK high or low							
t_{su}	Setup time	Data before CLK↑							ns
		Data before $\overline{LE}$↑, CLK high							
		Data before $\overline{LE}$↑, CLK low							
t_h	Hold time	Data after CLK↑							ns
		Data after $\overline{LE}$↑, CLK high or low							

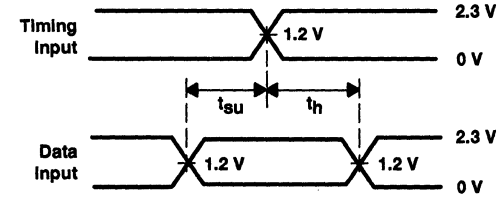
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

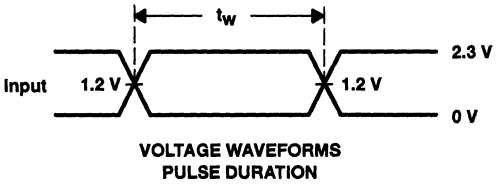


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND

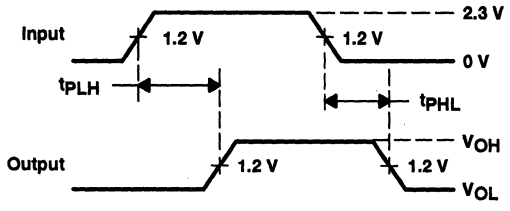
LOAD CIRCUIT



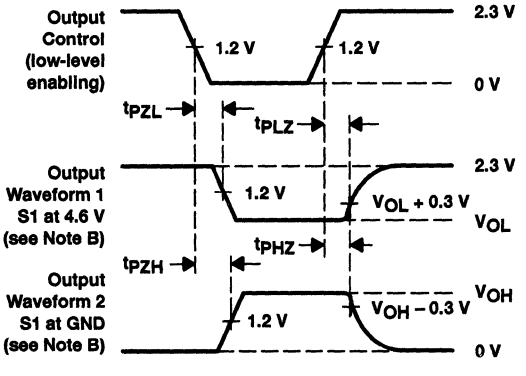
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

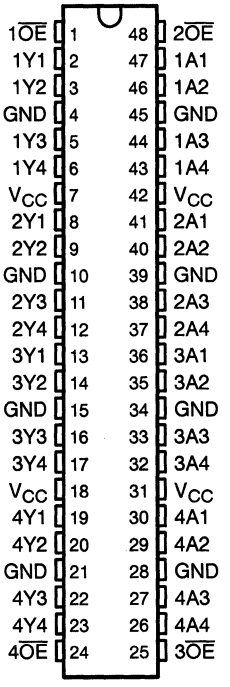
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **State-of-the-Art Advanced Low-Voltage BiCMOS Technology (ALB) Design for 3.3-V Operation**
- **Member of the Texas Instruments *Widebus*™ Family**
- **Schottky Diodes on All Inputs to Eliminate Overshoot and Undershoot**
- **Industry Standard '16244 Pinout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74ALB16244 16-bit buffer and line driver is designed for high-speed, low-voltage (3.3-V) V_{CC} operation. This device is intended to replace the conventional driver in any speed-critical path. The small propagation delay is achieved using a unity gain amplifier on the input and feedback resistors from input to output, which allows the output to track the input with a small offset voltage.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

The SN74ALB16244 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

Widebus is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I: Except I/O ports (see Note 1) ..... –0.5 V to 4.6 V
I/O ports (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book.*

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	3.6	V
I_{OH}‡	High-level output current			–18	mA
I_{OL}‡	Low-level output current			18	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5	ns/V
T_A	Operating free-air temperature		–40	85	°C

‡ Refer to Figures 1 and 2 for typical I/O ranges.

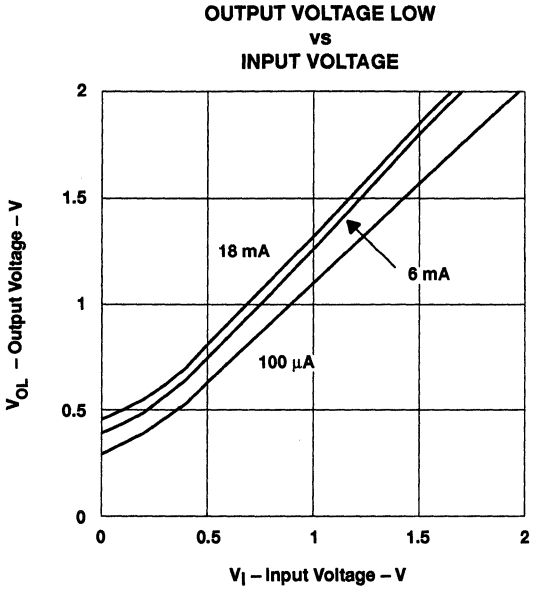


Figure 2. V_{OL} Over Recommended Free-Air Temperature Range

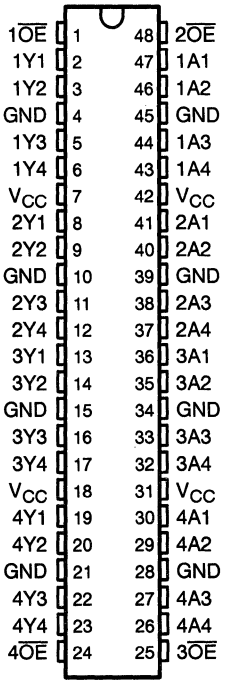
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			UNIT
			MIN	TYP†	MAX	
t_{pd}	A	Y	0.8	1.6	2.2	ns
t_{en}	$\overline{OE}$	Y	2.5	3.4	4.4	ns
t_{dis}	$\overline{OE}$	Y	2	2.9	4	ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit buffer/driver is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16244 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16244 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16244 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

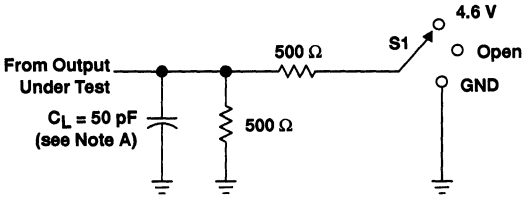
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		–12	mA
		V_{CC} = 2.7 V		–12	
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		12	mA
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

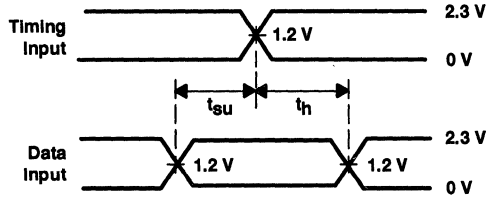
NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

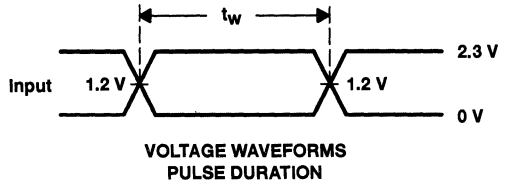


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND

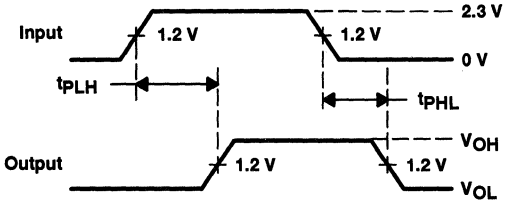
LOAD CIRCUIT



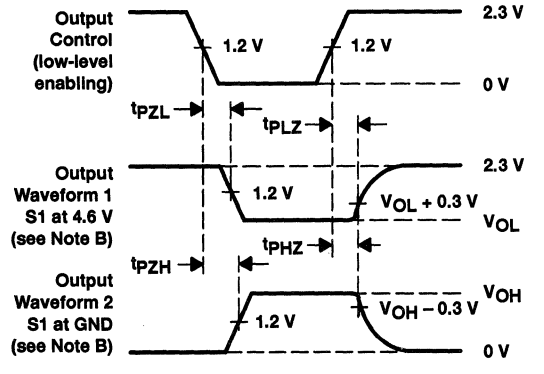
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



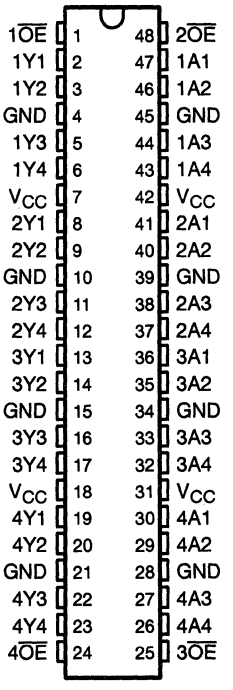
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required.**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit buffer/driver is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH162244 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

The outputs, which are designed to sink up to 12 mA, include 26-Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162244 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH162244 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

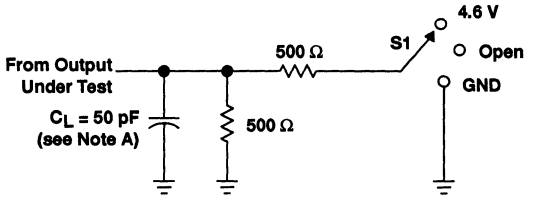
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		–6	mA
		V_{CC} = 2.7 V		–8	
		V_{CC} = 3 V		–12	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		6	mA
		V_{CC} = 2.7 V		8	
		V_{CC} = 3 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

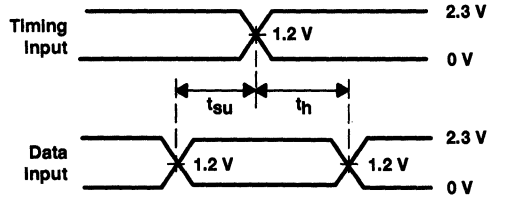
NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

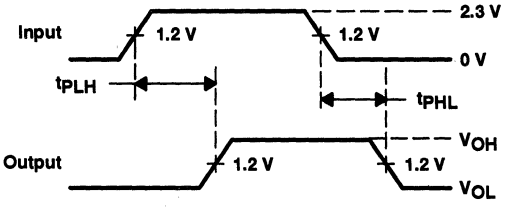


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND

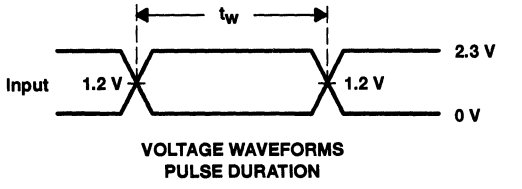
LOAD CIRCUIT



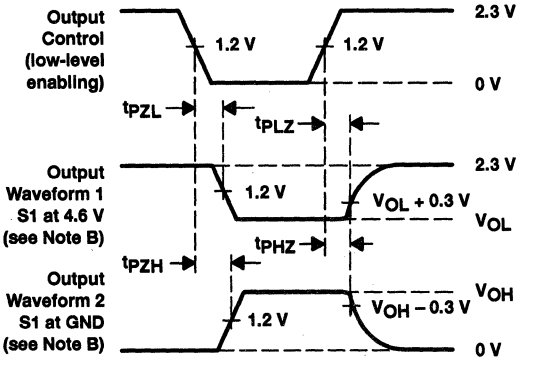
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



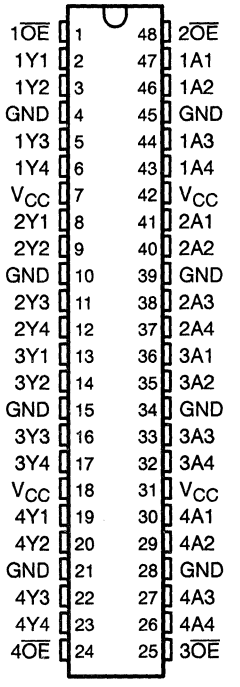
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Members of the Texas Instruments *Widebus*™ Family**
- **High-Impedance State During Power Up and Power Down**
- **5-V I/O Compatible**
- **High-Drive Capability (–32 mA/64 mA)**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Auto 3-State Eliminates Bus Current Loading When Voltage at the Output Exceeds V_{CC}**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Power Off Disables Inputs/Outputs, Permitting Live Insertion**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Package**

SN54ALVTH16244 . . . WD PACKAGE
SN74ALVTH16244 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description

The 'ALVTH16244 are 16-bit buffers/line drivers designed for 2.5-V or 3.3-V V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.2 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ALVTH16244 is available in TI's thin very small-outline package (DGV), which provides the same I/O pin count and functionality of standard Widebus packages in less than half the printed circuit board area.

The SN54ALVTH16244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALVTH16244 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

PRODUCT PREVIEW

Widebus is a trademark of Texas Instruments Incorporated.

recommended operating conditions, V_{CC} = 2.5 V ± 0.2 V (see Note 3)

			SN54ALVTH16244		SN74ALVTH16244		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.3	2.7	2.3	2.7	V
V_{IH}	High-level input voltage		1.7		1.7		V
V_{IL}	Low-level input voltage			0.7		0.7	V
V_I	Input voltage		0	5.5	0	5.5	V
I_{OH}	High-level output current			–6		–8	mA
I_{OL}	Low-level output current			6		8	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1 KHz			18		24	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused control inputs must be held high or low to prevent them from floating.

recommended operating conditions, V_{CC} = 3.3 V ± 0.3 V (see Note 3)

			SN54ALVTH16244		SN74ALVTH16244		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		3	3.6	3	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	5.5	0	5.5	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			24		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1 KHz			48		64	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused control inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

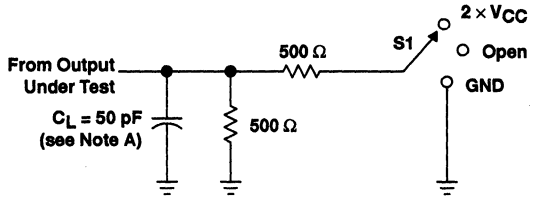
electrical characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

PARAMETER	TEST CONDITIONS			SN54ALVTH16244			SN74ALVTH16244			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 3 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = 3 V to 3.6 V,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 3 V	I_{OH} = – 24 mA		2						
		I_{OH} = – 32 mA					2			
V_{OL}	V_{CC} = 3 V to 3.6 V,	I_{OL} = 100 µA				0.2			0.2	V
	V_{CC} = 3 V	I_{OL} = 16 mA							0.4	
		I_{OL} = 24 mA				0.5				
		I_{OL} = 32 mA							0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control inputs			±1			±1	µA
	V_{CC} = 0 or 3.6 V,	V_I = 5.5 V	Control inputs			10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	Data inputs			20			20	
		V_I = V_{CC}	Data inputs			10			10	
		V_I = 0	Data inputs			–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V				±100			±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	Data inputs	75			75			µA
		V_I = 2 V	Data inputs	–75			–75			
	V_{CC} = 3.6 V‡,	V_I = 0 to 3.6 V	Data inputs			±500			±500	
I_{EX}§	V_{CC} = 3 V,	V_O = 5.5 V				125			125	µA
$I_{OZ(PU/PD)}$¶	V_{CC} ≤ 1.2 V, V_I = GND or V_{CC},	V_O = 0.5 V to V_{CC}, $\overline{OE}$ = don't care				±100			±100	µA
I_{OZH}	V_{CC} = 3.6 V, V_O = 3 V, V_I = 0.8 V or 2 V					5			5	µA
I_{OZL}	V_{CC} = 3.6 V, V_O = 0.5 V, V_I = 0.8 V or 2 V					–5			–5	µA
I_{CC}	V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND		Outputs high		0.07	0.09		0.07	0.09	mA
			Outputs low		3.2	5		3.2	5	
			Outputs disabled		0.07	0.09		0.07	0.09	
ΔI_{CC}#	V_{CC} = 3 V to 3.6 V, One input at V_{CC} –0.6 V, Other inputs at V_{CC} or GND					0.2			0.2	mA
C_i	V_{CC} = 3.3 V,	V_I = 3.3 V or 0			3			3		pF
C_o	V_{CC} = 3.3 V,	V_O = 3.3 V or 0			9			9		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ Current into an output in the high state when $V_O > V_{CC}$
¶ High-impedance state during power up/high-impedance state during power down
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

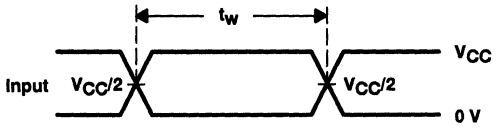
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

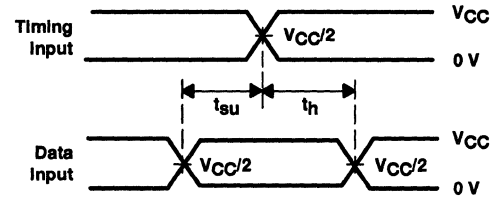


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

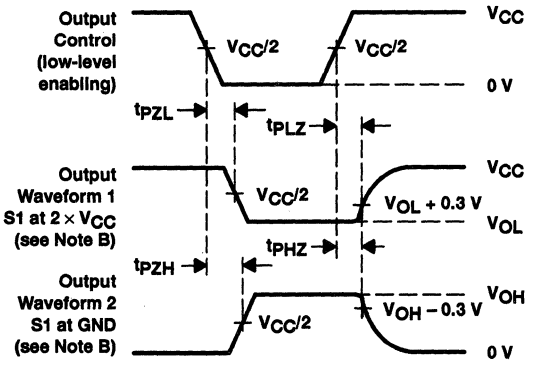
LOAD CIRCUIT



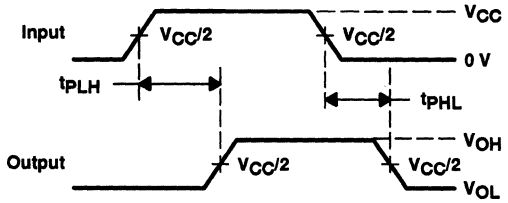
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

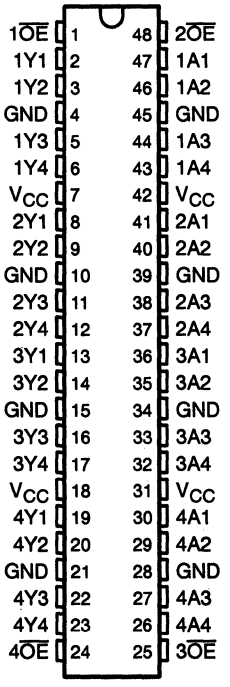
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **Members of the Texas Instruments *Widebus*™ Family**
- **Output Ports Have Equivalent 30-Ω Series Resistors, So No External Resistors Are Required**
- **High-Impedance State During Power Up and Power Down**
- **5-V I/O Compatible**
- **High-Drive Capability (–12 mA/12 mA)**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Auto 3-State Eliminates Bus Current Loading When Voltage at the Output Exceeds V_{CC}**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Power Off Disables Inputs/Outputs, Permitting Live Insertion**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Package**

SN54ALVTH162244 . . . WD PACKAGE
SN74ALVTH162244 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description

The 'ALVTH162244 are 16-bit buffers/line drivers designed for low-voltage 2.5-V or 3.3-V V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.2 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

All outputs are designed to sink up to 12 mA and include 30-Ω resistors to reduce overshoot and undershoot.

The SN74ALVTH162244 is available in TI's thin very small-outline package (DGV), which provides the same I/O pin count and functionality of standard Widebus packages in less than half the printed circuit board area.

The SN54ALVTH162244 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALVTH162244 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

Widebus is a trademark of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... –0.5 V to 7 V
Output current in the low state, I_O ..... 30 mA
Output current in the high state, I_O ..... –30 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package ..... 0.85 W
DGV package ..... 0.87 W
DL package ..... 1.2 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions, V_{CC} = 2.5 V ± 0.2 V (see Note 3)

			SN54ALVTH162244		SN74ALVTH162244		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.3	2.7	2.3	2.7	V
V_{IH}	High-level input voltage		1.7		1.7		V
V_{IL}	Low-level input voltage			0.7		0.7	V
V_I	Input voltage		0	5.5	0	5.5	V
I_{OH}	High-level output current						mA
I_{OL}	Low-level output current						mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused control inputs must be held high or low to prevent them from floating.

recommended operating conditions, V_{CC} = 3.3 V ± 0.3 V (see Note 3)

			SN54ALVTH162244		SN74ALVTH162244		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		3	3.6	3	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	5.5	0	5.5	V
I_{OH}	High-level output current			–8		–12	mA
I_{OL}	Low-level output current			8		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused control inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

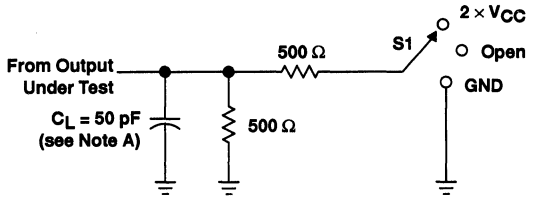
electrical characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

PARAMETER	TEST CONDITIONS			SN54ALVTH162244			SN74ALVTH162244			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 3 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = 3 V to 3.6 V,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 3 V	I_{OH} = – 8 mA								
		I_{OH} = – 12 mA								
V_{OL}	V_{CC} = 3 V to 3.6 V,	I_{OL} = 100 µA				0.2			0.2	V
	V_{CC} = 3 V	I_{OL} = 8 mA								
		I_{OL} = 12 mA								
I_I	V_{CC} = 3.6 V, V_I = V_{CC} or GND		Control inputs			±1			±1	µA
	V_{CC} = 0 or 3.6 V	V_I = 5.5 V				10			10	
	V_{CC} = 3.6 V	V_I = 5.5 V	Data inputs			20			20	
		V_I = V_{CC}				10			10	
		V_I = 0				–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V				±100			±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	Data inputs	75			75			µA
		V_I = 2 V		–75			–75			
	V_{CC} = 3.6 V‡,	V_I = 0 to 3.6 V				±500			±500	
I_{EX}§	V_{CC} = 3 V,	V_O = 5.5 V				125			125	µA
$I_{OZ(PU/PD)}$¶	V_{CC} ≤ 1.2 V, V_I = GND or V_{CC},	V_O = 0.5 V to V_{CC}, $\overline{OE}$ = don't care				±100			±100	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.07	0.09		0.07	0.09	mA
			Outputs low		3.2	5		3.2	5	
			Outputs disabled		0.07	0.09		0.07	0.09	
ΔI_{CC}#	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND					0.2			0.2	mA
C_i	V_{CC} = 3.3 V,	V_I = 3.3 V or 0			3			3		pF
C_o	V_{CC} = 3.3 V,	V_O = 3.3 V or 0			9			9		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ Current into an output in the high state when V_O > V_{CC}
¶ High-impedance state during power up/high-impedance state during power down
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

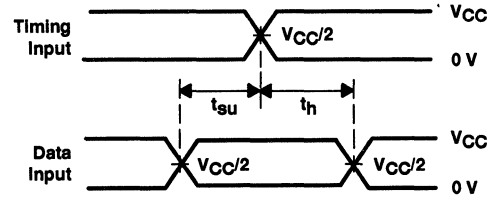
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

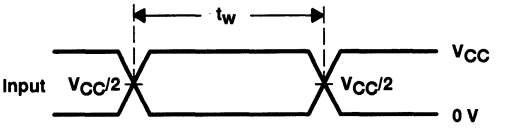


LOAD CIRCUIT

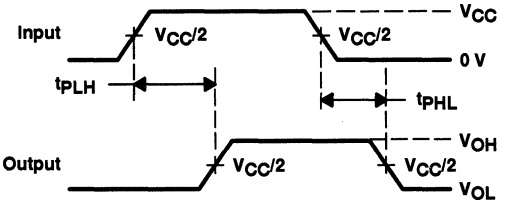
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



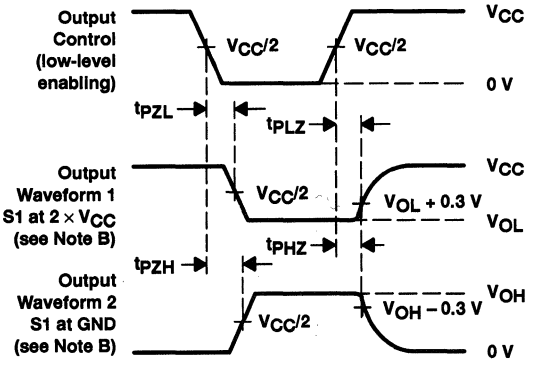
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

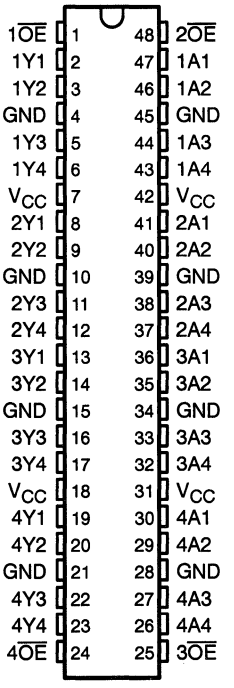
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments *Widebus*™ Family
- High-Impedance State During Power Up and Power Down
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Inputs/Outputs, Permitting Live Insertion
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Spacings

SN54LVTH16244A . . . WD PACKAGE
SN74LVTH16244A . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'LVTH16244A are 16-bit buffers and line drivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

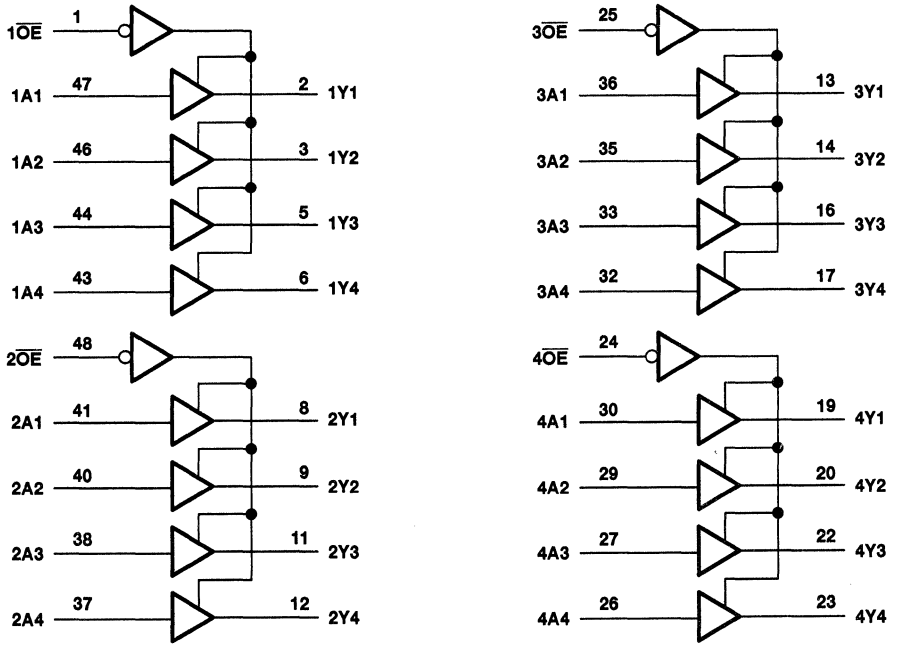
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5-V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5-V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVTH16244A is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

Widebus is a trademark of Texas Instruments Incorporated.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... –0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVTH16244A ..... 96 mA
SN74LVTH16244A ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH16244A ..... 48 mA
SN74LVTH16244A ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

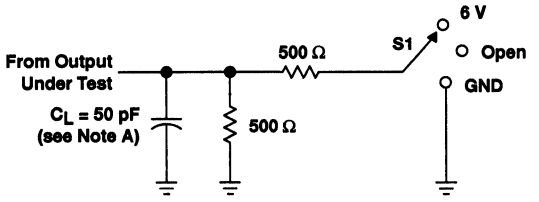
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVTH16244A			SN74LVTH16244A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = 2.7 V to 3.6 V,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = –8 mA		2.4			2.4			
	V_{CC} = 3 V	I_{OH} = –24 mA		2						
		I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2			0.2	V
		I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4			0.4	
		I_{OL} = 32 mA				0.5			0.5	
		I_{OL} = 48 mA				0.55				
		I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 0 or 3.6 V,	V_I = 5.5 V				10			10	µA
	V_{CC} = 3.6 V	V_I = V_{CC} or GND	Control inputs			±1			±1	
		V_I = V_{CC}	Data inputs			1			1	
		V_I = 0				–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V				±100			±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	Data inputs	75			75			µA
		V_I = 2 V		–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V,				5			5	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V,				–5			–5	µA
I_{OZPU}‡	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0			±100			±100	µA
I_{OZPD}‡	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0			±100			±100	µA
I_{CC}	V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND	Outputs high				0.19			0.19	mA
		Outputs low				5			5	
		Outputs disabled				0.19			0.19	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND					0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_o	V_O = 3 V or 0				9			9		pF

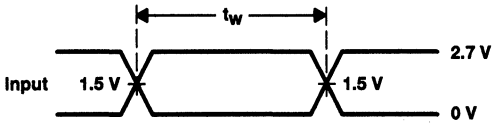
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This parameter is warranted by characterization but not production tested.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PARAMETER MEASUREMENT INFORMATION

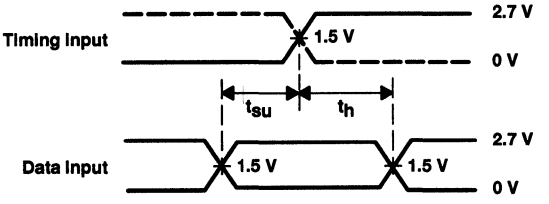


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

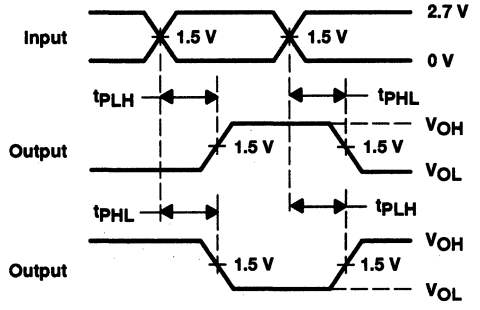
LOAD CIRCUIT



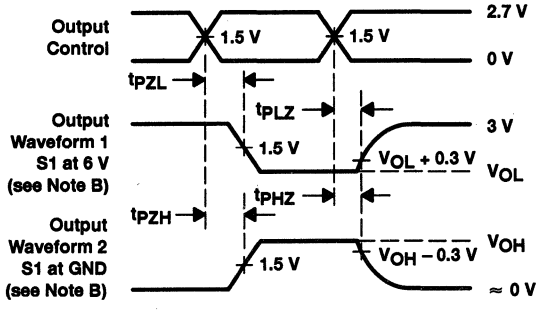
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



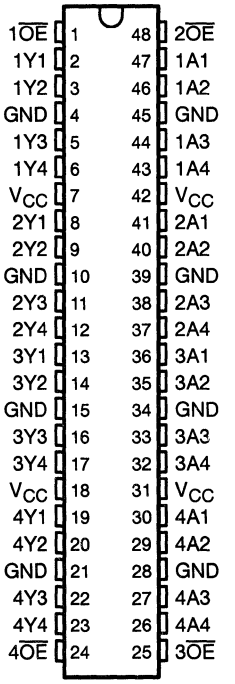
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Members of the Texas Instruments *Widebus*™ Family**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Support Unregulated Battery Operation Down to 2.7 V**
- **High-Impedance State During Power Up and Power Down**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Power Off Disables Inputs/Outputs, Permitting Live Insertion**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54LVTH162244 . . . WD PACKAGE
SN74LVTH162244 . . . DGG OR DL PACKAGE
(TOP VIEW)



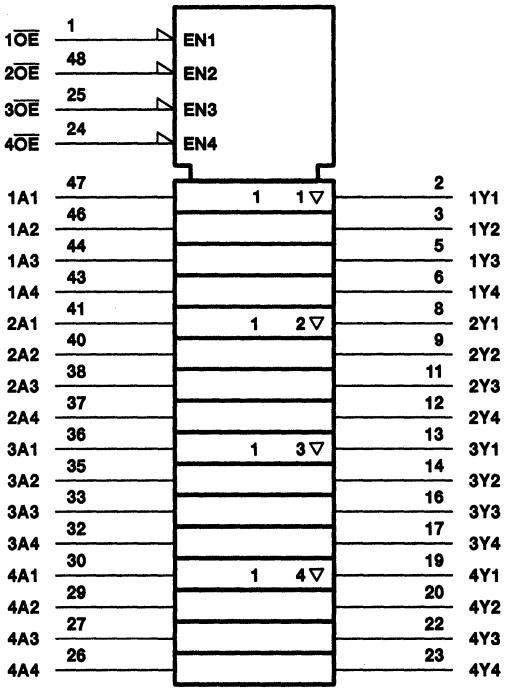
description

The 'LVTH162244 are 16-bit buffers and line drivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

The outputs, which are designed to source or sink up to 12 mA, include 22-Ω series resistors to reduce overshoot and undershoot.

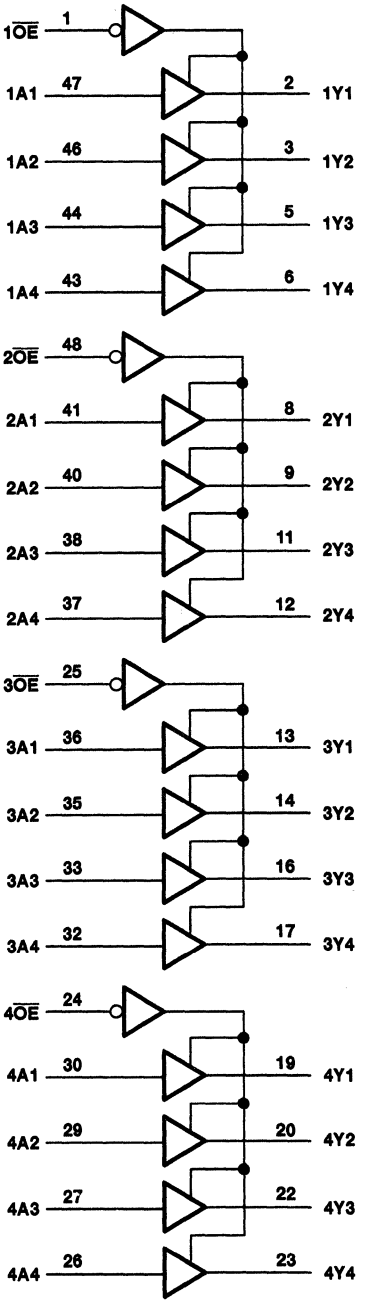
Widebus is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVTH162244			SN74LVTH162244			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = 3 V,	I_{OH} = –12 mA		2			2			V
V_{OL}	V_{CC} = 3 V,	I_{OL} = 12 mA				0.8			0.8	V
I_I	V_{CC} = 0 or 3.6 V	V_I = 5.5 V				10			10	µA
	V_{CC} = 3.6 V	V_I = V_{CC} or GND	Control pins			±1			±1	µA
		V_I = V_{CC}	Data pins			1			1	µA
		V_I = 0	Data pins			–5			–5	µA
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A inputs	75			75			µA
		V_I = 2 V	A inputs	–75			–75			µA
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				5			5	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–5			–5	µA
I_{OZPU}‡	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V, $\overline{OE}$ = X				±100			±100	µA
I_{OZPD}‡	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V, $\overline{OE}$ = X				±100			±100	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high			0.19			0.19	mA
			Outputs low			5			5	mA
			Outputs disabled			0.19			0.19	mA
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND					0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_o	V_O = 3 V or 0				9			9		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This parameter is characterized but not tested.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

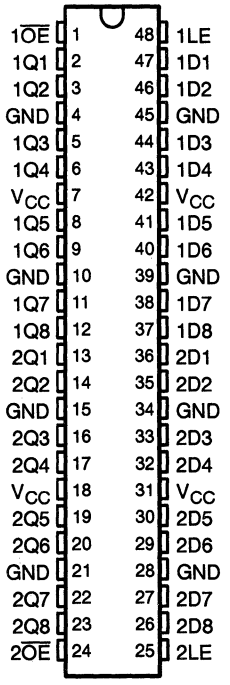
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH162244				SN74LVTH162244				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V	
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN MAX	
t_{PLH}	A	Y	1.3	4.5		5.1	1.4	3.4	4	4.8	ns
t_{PHL}			1.1	3.9		4.5	1.2	2.9	3.6	4.1	
t_{PZH}	$\overline{OE}$	Y	1.1	5.3		6.7	1.2	3.9	5.1	6.5	ns
t_{PZL}			1.3	4.7		6.1	1.4	3.8	4.5	5.8	
t_{PHZ}	$\overline{OE}$	Y	2.1	5.3		5.6	2.2	4.4	5	5.4	ns
t_{PLZ}			1.9	5.5		5.8	2	4.2	5	5.4	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per MIL-STD-833, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit transparent D-type latch is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16373 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. This device can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. $\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16373 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16373 is characterized for operation from –40°C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		–12	mA
		V_{CC} = 2.7 V		–12	
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		12	mA
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high or low	3.3		3.3		3.3		ns
t_{su}	Setup time, data before LE↓	1		1		1.1		ns
t_h	Hold time, data after LE↓	1.5		1.7		1.4		ns

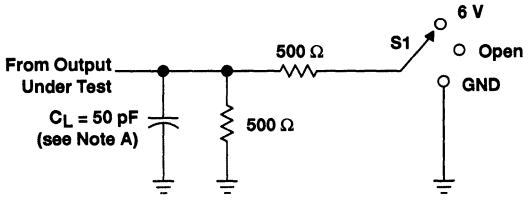
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	1	5.1		4.3	1.1	3.6	ns
	LE	Q	1	5.5		4.6	1	3.9	
t_{en}	$\overline{OE}$	Q	1	6.5		5.7	1	4.7	ns
t_{dis}	$\overline{OE}$	Q	1.9	5.3		4.5	1.4	4.1	ns

operating characteristics, T_A = 25°C

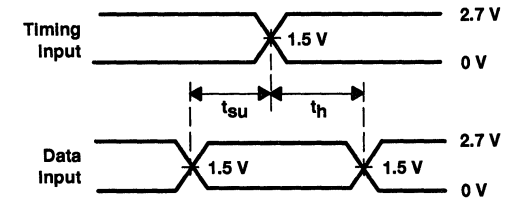
PARAMETER			TEST CONDITIONS	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 10 MHz	19	22	pF
		Outputs disabled		4	5	

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V

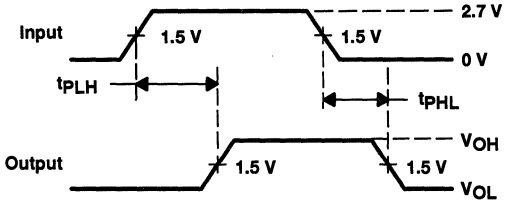


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

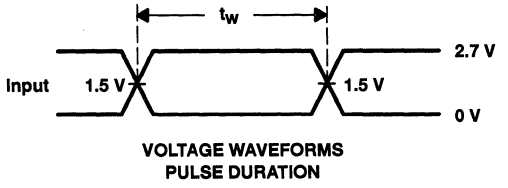
LOAD CIRCUIT



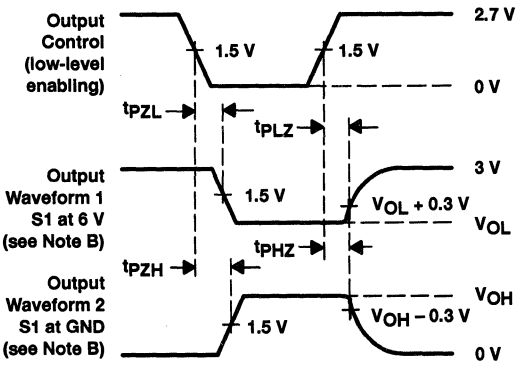
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



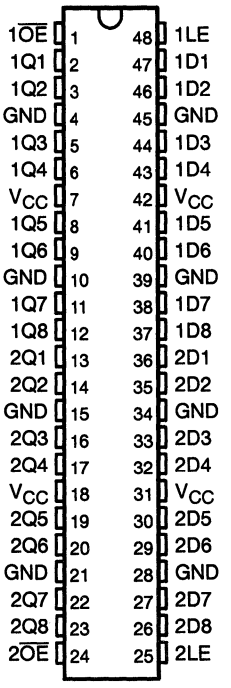
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments *Widebus*™ Family
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- High-Impedance State During Power Up and Power Down
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Inputs/Outputs, Permitting Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH16373 . . . WD PACKAGE
SN74LVTH16373 . . . DGG OR DL PACKAGE
(TOP VIEW)



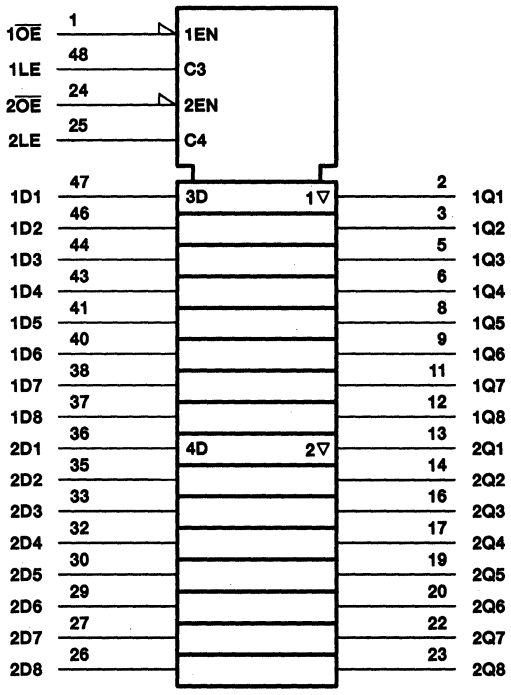
description

The 'LVTH16373 are 16-bit transparent D-type latches with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

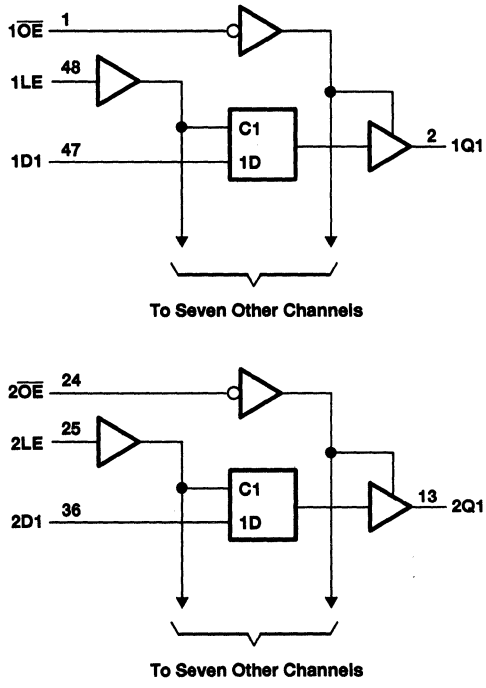
Widebus is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

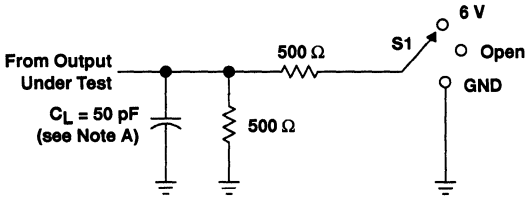
PARAMETER		TEST CONDITIONS		SN54LVTH16373			SN74LVTH16373			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 2.7 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 2.7 V to 3.6 V	I_{OH} = –100 µA	V_{CC}–0.2			V_{CC}–0.2			V
		V_{CC} = 2.7 V,	I_{OH} = –8 mA	2.4			2.4			
		V_{CC} = 3 V	I_{OH} = –24 mA	2						
			I_{OH} = –32 mA				2			
V_{OL}		V_{CC} = 2.7 V	I_{OL} = 100 µA			0.2			0.2	V
			I_{OL} = 24 mA			0.5			0.5	
		V_{CC} = 3 V	I_{OL} = 16 mA			0.4			0.4	
			I_{OL} = 32 mA			0.5			0.5	
			I_{OL} = 48 mA			0.55				
			I_{OL} = 64 mA						0.55	
I_I		V_{CC} = 0 or 3.6 V	V_I = 5.5 V			10			10	µA
	Control inputs	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1			±1	
	Data inputs	V_{CC} = 3.6 V	V_I = V_{CC}			1			1	
			V_I = 0			–5			–5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V			±100			±100	µA
$I_{I(hold)}$	Data inputs	V_{CC} = 3 V	V_I = 0.8 V	75			75			µA
			V_I = 2 V	–75			–75			
I_{OZH}		V_{CC} = 3.6 V,	V_O = 3 V			5			5	µA
I_{OZL}		V_{CC} = 3.6 V,	V_O = 0.5 V			–5			–5	µA
I_{OZPU}‡		V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V, $\overline{OE}$ = X			±100			±100	µA
I_{OZPD}‡		V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V, $\overline{OE}$ = X			±100			±100	µA
I_{CC}	Outputs high	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,			0.19			0.19	mA
	Outputs low					5			5	
	Outputs disabled					0.19			0.19	
ΔI_{CC}§		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND				0.2			0.2	mA
C_i		V_I = 3 V or 0			3			3		pF
C_o		V_O = 3 V or 0			9			9		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This parameter is characterized but not tested.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

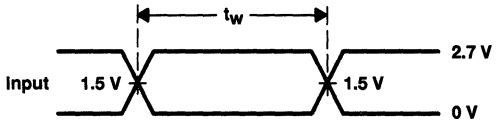
		SN54LVTH16373				SN74LVTH16373				UNIT
		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	3		3		3		3		ns
t_{su}	Setup time, data before LE↓	1		0.6		1		0.6		ns
t_h	Hold time, data after LE↓	1		1.1		1		1.1		ns

PARAMETER MEASUREMENT INFORMATION

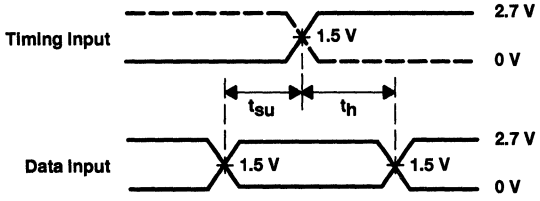


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

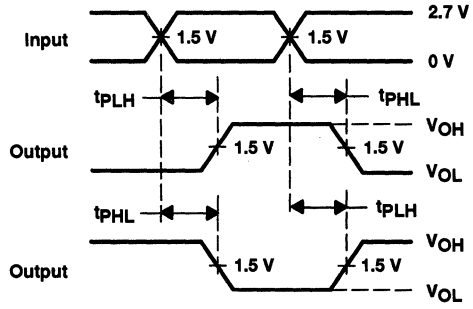
LOAD CIRCUIT FOR OUTPUTS



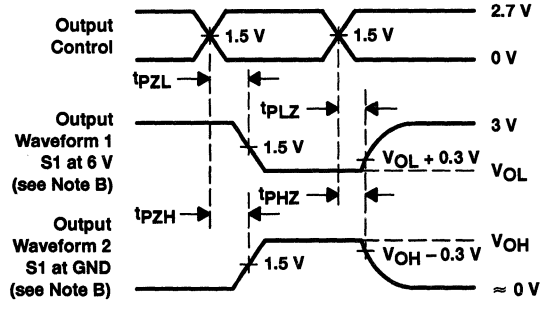
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



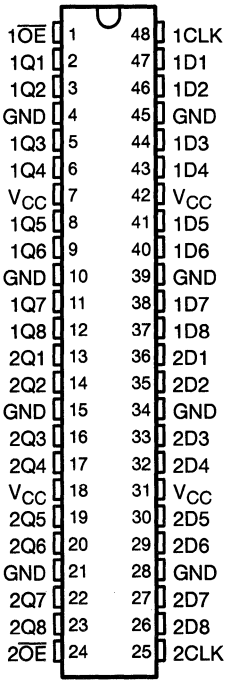
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per MIL-STD-833, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 16-bit edge-triggered D-type flip-flop is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs. $\overline{OE}$ can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components. $\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16374 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16374 is characterized for operation from –40°C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		–12	mA
		V_{CC} = 2.7 V		–12	
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		12	mA
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	150	0	150	0	150	MHz
t_w	Pulse duration, CLK high or low	3.3		3.3		3.3		ns
t_{su}	Setup time, data before CLK↑	2.1		2.2		1.9		ns
t_h	Hold time, data after CLK↑	0.6		0.5		0.5		ns

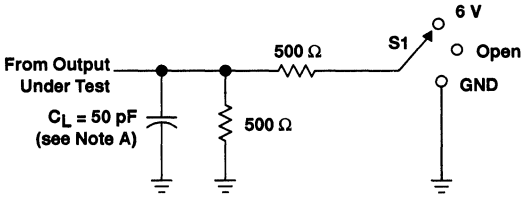
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			150		150		150		MHz
t_{pd}	CLK	Q	1	5.9		4.9	1	4.2	ns
t_{en}	CLK	Q	1	6.7		5.9	1	4.8	ns
t_{dis}	CLK	Q	1.7	5.5		4.7	1.2	4.3	ns

operating characteristics, T_A = 25°C

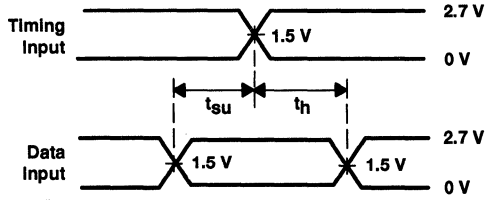
PARAMETER			TEST CONDITIONS	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 10 MHz	31	30	pF
		Outputs disabled		16	18	

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V

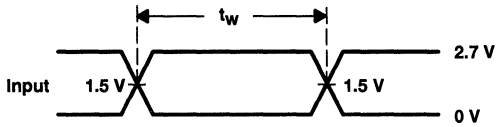


LOAD CIRCUIT

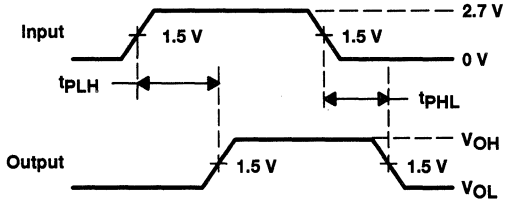
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



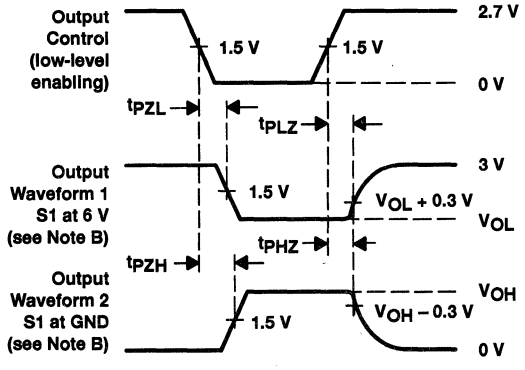
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



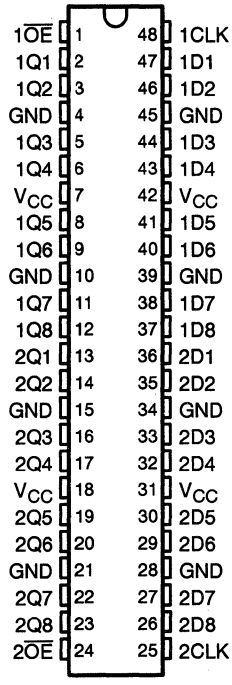
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments *Widebus*™ Family
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- High-Impedance State During Power Up and Power Down
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Inputs/Outputs, Permitting Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH16374 . . . WD PACKAGE
SN74LVTH16374 . . . DGG OR DL PACKAGE
(TOP VIEW)



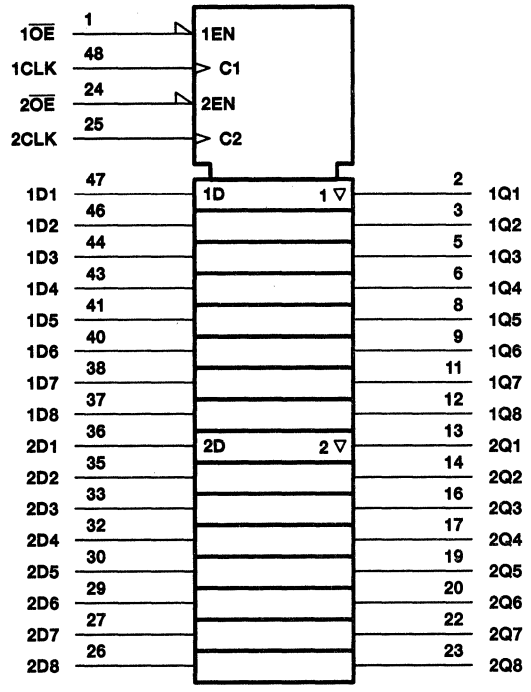
description

The 'LVTH16374 are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

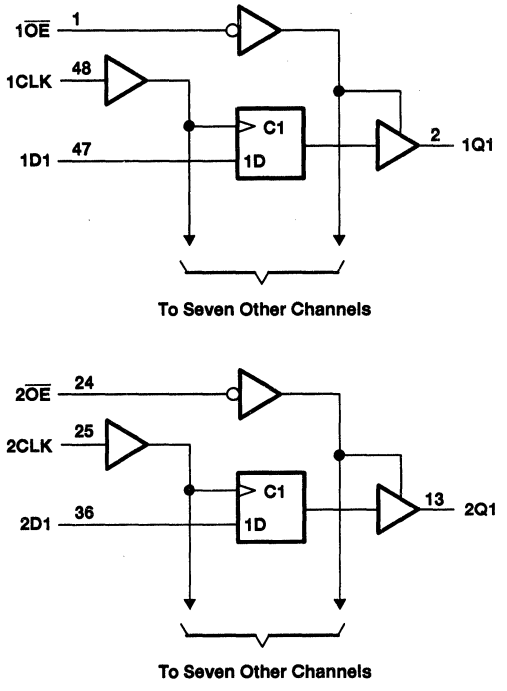
Widebus is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVTH16374 ..... 96 mA
SN74LVTH16374 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH16374 ..... 48 mA
SN74LVTH16374 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 0.85 W
DL package ..... 1.2 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

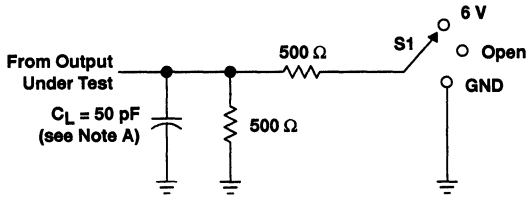
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH16374			SN74LVTH16374			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 2.7 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 2.7 V to 3.6 V	I_{OH} = –100 µA	V_{CC}–0.2			V_{CC}–0.2			V
		V_{CC} = 2.7 V,	I_{OH} = –8 mA	2.4			2.4			
		V_{CC} = 3 V	I_{OH} = –24 mA	2						
			I_{OH} = –32 mA				2			
V_{OL}		V_{CC} = 2.7 V	I_{OL} = 100 µA			0.2			0.2	V
			I_{OL} = 24 mA			0.5			0.5	
		V_{CC} = 3 V	I_{OL} = 16 mA			0.4			0.4	
			I_{OL} = 32 mA			0.5			0.5	
			I_{OL} = 48 mA			0.55				
			I_{OL} = 64 mA						0.55	
I_I		V_{CC} = 0 or 3.6 V	V_I = 5.5 V			10			10	µA
	Control inputs	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1			±1	
	Data inputs	V_{CC} = 3.6 V	V_I = V_{CC}			1			1	
			V_I = 0			–5			–5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V			±100			±100	µA
$I_{I(hold)}$	Data inputs	V_{CC} = 3 V	V_I = 0.8 V	75			75			µA
			V_I = 2 V	–75			–75			
I_{OZH}		V_{CC} = 3.6 V,	V_O = 3 V			5			5	µA
I_{OZL}		V_{CC} = 3.6 V,	V_O = 0.5 V			–5			–5	µA
I_{OZPU}‡		V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V, $\overline{OE}$ = X			±100			±100	µA
I_{OZPD}‡		V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V, $\overline{OE}$ = X			±100			±100	µA
I_{CC}	Outputs high	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,			0.19			0.19	mA
	Outputs low					5			5	
	Outputs disabled					0.19			0.19	
ΔI_{CC}§		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND				0.2			0.2	mA
C_i		V_I = 3 V or 0			3			3		pF
C_o		V_O = 3 V or 0			9			9		pF

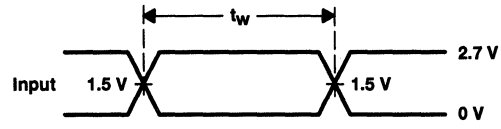
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This parameter is characterized but not tested.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PARAMETER MEASUREMENT INFORMATION

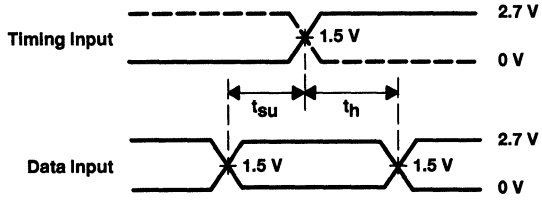


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

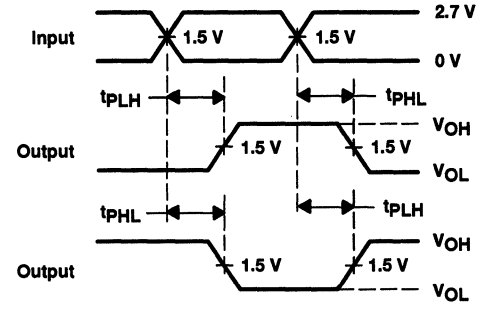
LOAD CIRCUIT FOR OUTPUTS



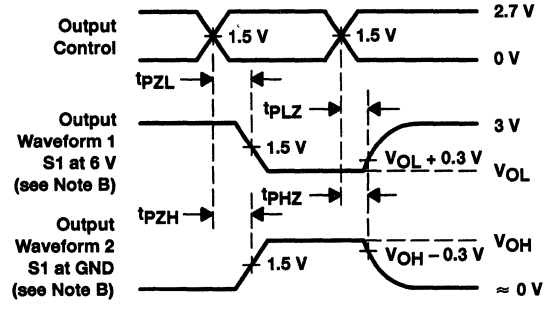
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



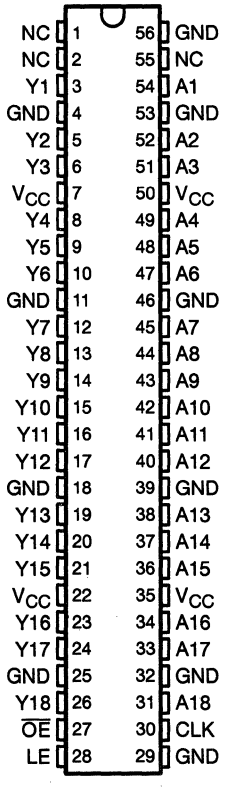
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



NC – No internal connection

description

This 18-bit universal bus driver is designed for 2.3-V to 3.6-V V_{CC} operation.

Data flow from A to Y is controlled by the output-enable ($\overline{OE}$). The device operates in the transparent mode when the latch-enable (LE) input is high. The A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLK. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

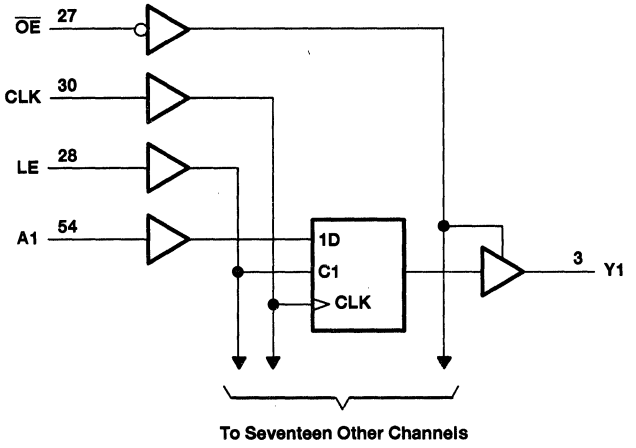
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16835 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16835 is characterized for operation from –40°C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book.*

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

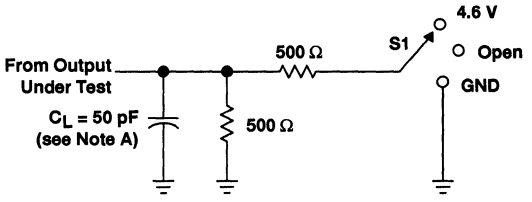
PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}		I_{OH} = –100 µA		2.3 V to 3.6 V	V_{CC}–0.2			V
		I_{OH} = –6 mA,	V_{IH} = 1.7 V	2.3 V	2			
		I_{OH} = –12 mA	V_{IH} = 1.7 V	2.3 V	1.7			
			V_{IH} = 2 V	2.7 V	2.2			
			V_{IH} = 2 V	3 V	2.4			
		I_{OH} = –24 mA,	V_{IH} = 2 V	3 V	2			
V_{OL}		I_{OL} = 100 µA		2.3 V to 3.6 V			0.2	V
		I_{OL} = 6 mA,	V_{IL} = 0.7 V	2.3 V			0.4	
		I_{OL} = 12 mA	V_{IL} = 0.7 V	2.3 V			0.7	
			V_{IL} = 0.8 V	2.7 V			0.4	
		I_{OL} = 24 mA,	V_{IL} = 0.8 V	3 V			0.55	
I_I		V_I = V_{CC} or GND		3.6 V			±5	µA
$I_{I(hold)}$		V_I = 0.7 V		2.3 V	45			µA
		V_I = 1.7 V		2.3 V	–45			
		V_I = 0.8 V		3 V	75			
		V_I = 2 V		3 V	–75			
		V_I = 0 to 3.6 V‡		3.6 V			±500	
I_{OZ}		V_O = V_{CC} or GND		3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	µA
ΔI_{CC}		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		3 V to 3.6 V			750	µA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		3.5		pF
	Data inputs	V_I = V_{CC} or GND		3.3 V		6		
C_{io}	Outputs	V_O = V_{CC} or GND		3.3 V		7		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

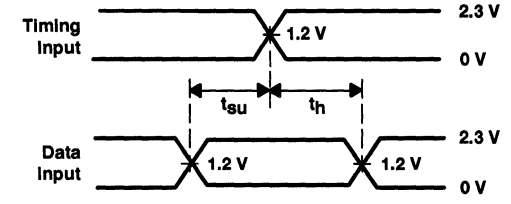
			V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	0	150	MHz
t_w	Pulse duration	LE high	3.3		3.3		3.3		ns
		CLK high or low	3.3		3.3		3.3		
t_{su}	Setup time	Data before CLK↑	2.2		2.1		1.7		ns
		Data before LE↓, CLK high	1.9		1.6		1.5		
		Data before LE↓, CLK low	1.3		1.1		1		
t_h	Hold time	Data after CLK↑	0.6		0.6		0.7		ns
		Data after LE↓, CLK high or low	1.4		1.7		1.4		

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

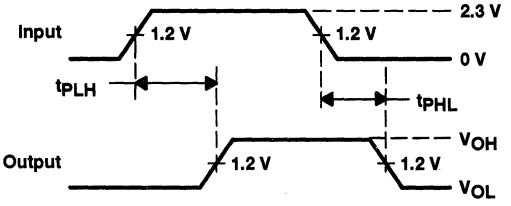


LOAD CIRCUIT

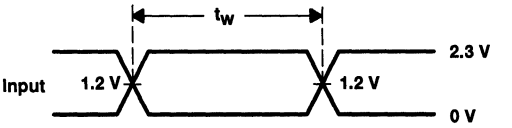
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND



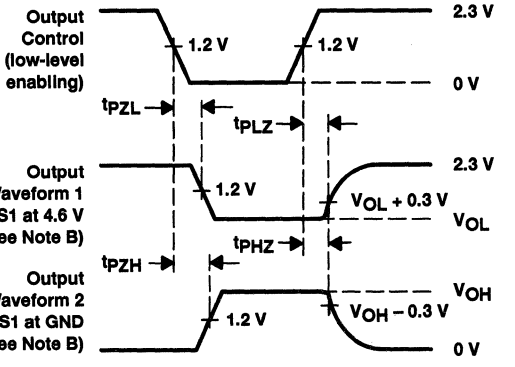
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



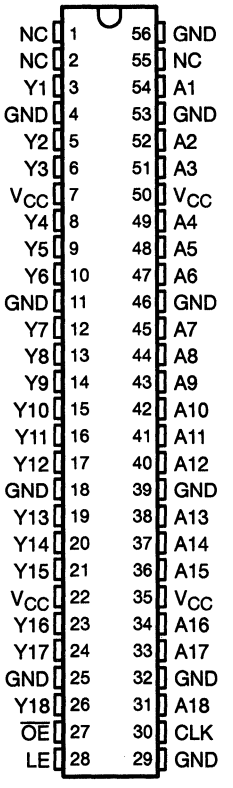
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Member of the Texas Instruments *Widebus*™ Family**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Supports Live Insertion**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages Using 25-mil Center-to-Center Spacings**

DGG OR DL PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN74LVT16835 is an 18-bit universal bus driver designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow from A to Y is controlled by the output-enable ($\overline{OE}$) input. This device operates in the transparent mode when the latch-enable (LE) input is high. The A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of the clock. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

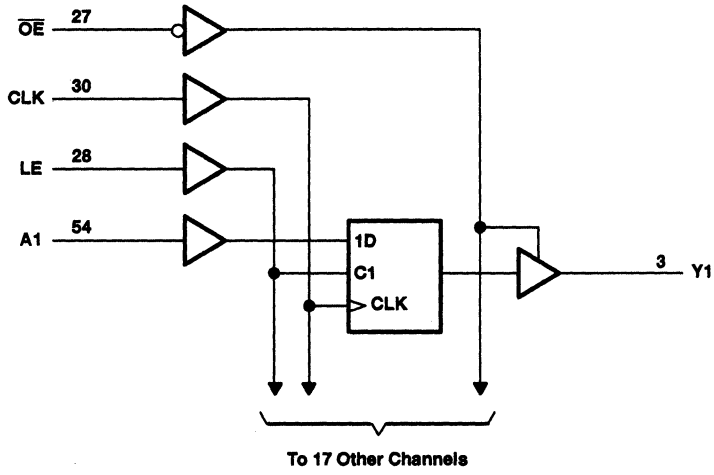
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16835 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the input/output (I/O) pins and functionality of standard small-outline packages in the same printed circuit board area.

The SN74LVT16835 is characterized for operation from –40°C to 85°C.

Widebus is a trademark of Texas Instruments Incorporated.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... –0.5 V to 7 V
Current into any output in the low state, I_O ..... 128 mA
Current into any output in the high state, I_O (see Note 2) ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Operating free-air temperature range, T_A ..... –40°C to 85°C
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	125	MHz
t_w	Pulse duration	LE high	3.3		3.3		ns
		CLK high or low	3.3		3.3		
t_{su}	Setup time	Data before CLK↑	1.6		2.1		ns
		Data before LE↓, CLK high	2.6		1.9		
		Data before LE↓, CLK low	2		1.3		
t_h	Hold time	Data after CLK↑	2		2.1		ns
		Data after LE↓	0.9		1.2		

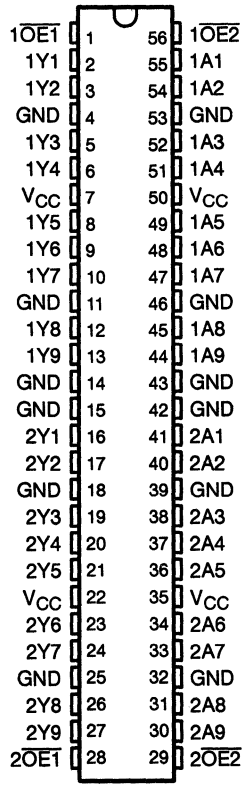
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP†	MAX	MIN	MAX	
f_{max}			150			150		MHz
t_{PLH}	A	Y	1.7	3	5.4		6.8	ns
t_{PHL}			1.6	3.2	5.9		7.7	
t_{PLH}	LE	Y	2.3	4	7		8.5	ns
t_{PHL}			2.7	4.3	7.9		9.7	
t_{PLH}	CLK	Y	2.5	4.1	7.9		9.2	ns
t_{PHL}			3.5	5.4	8.9		10.4	
t_{PZH}	$\overline{OE}$	Y	1.2	3	5		5.9	ns
t_{PZL}			1.5	3	5.8		6.9	
t_{PHZ}	$\overline{OE}$	Y	2.7	4.6	7.4		8.3	ns
t_{PLZ}			2.8	4.7	6.7		7.2	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 18-bit buffer and line driver is designed for 2.3-V to 3.6-V V_{CC} operation.

This SN74ALVCH16825 improves the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as two 9-bit buffers or one 18-bit buffer. It provides true data.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all nine affected outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN74ALVCH16825 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16825 is characterized for operation from –40°C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

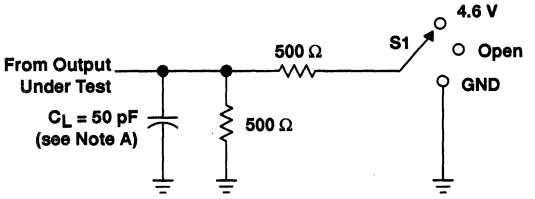
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		–12	mA
		V_{CC} = 2.7 V		–12	
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		12	mA
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

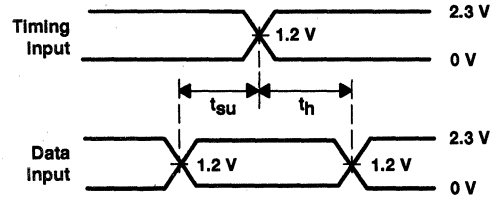
NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

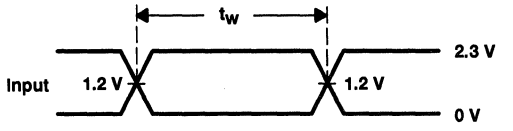


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND

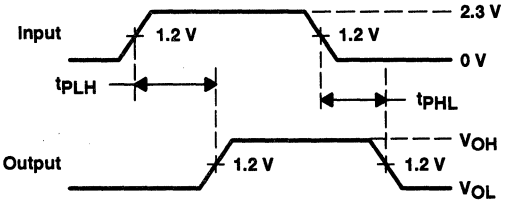
LOAD CIRCUIT



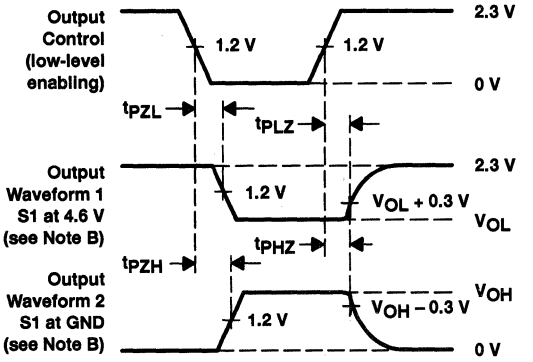
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



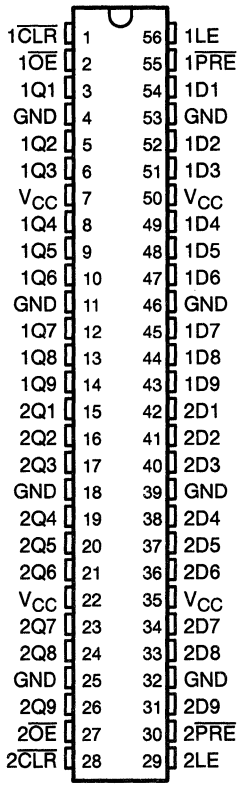
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 18-bit bus-interface D-type latch is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16843 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, unidirectional bus drivers, and working registers.

The SN74ALVCH16843 can be used as two 9-bit latches or one 18-bit latch. The 18 latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or a high-impedance state. The outputs also are in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN74ALVCH16843 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16843 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

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FUNCTION TABLE
(each 9-bit latch)

INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OE}$	LE	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q_0
X	X	H	X	X	Z

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions (see Note 4)

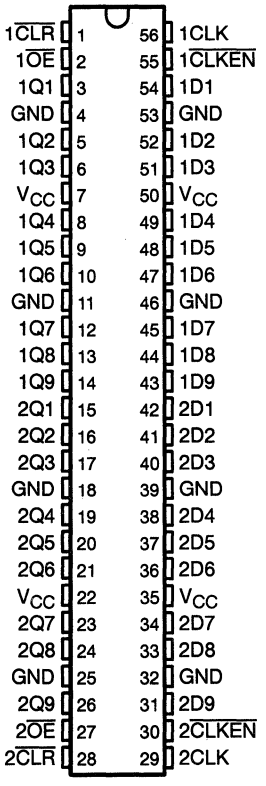
			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		–12	mA
		V_{CC} = 2.7 V		–12	
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		12	mA
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 18-bit bus-interface flip-flop is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16823 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The SN74ALVCH16823 can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable ($\overline{CLKEN}$) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high disables the clock buffer, thus latching the outputs. Taking the clear ($\overline{CLR}$) input low causes the Q outputs to go low independently of the clock.

A buffered output-enable ($\overline{OE}$) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable ($\overline{OE}$) input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

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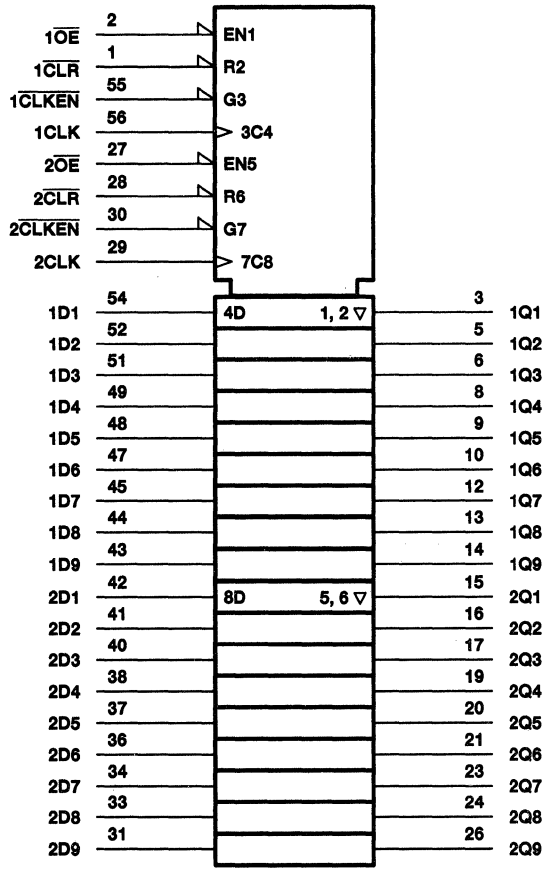
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		–12	mA
		V_{CC} = 2.7 V		–12	
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		12	mA
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	0	150	MHz
t_w	Pulse duration	$\overline{CLR}$ low	3.3		3.3		3.3		ns
		CLK high or low	3.3		3.3		3.3		
t_{su}	Setup time	$\overline{CLR}$ low	0.7		0.7		0.8		ns
		Data low	1.4		1.6		1.3		
		Data high	1.1		1.1		1		
		$\overline{CLKEN}$ low	1.8		1.9		1.5		
t_h	Hold time	Data low	0.4		0.5		0.5		ns
		Data high	0.7		0.1		0.8		
		$\overline{CLKEN}$ low	0.2		0.3		0.4		

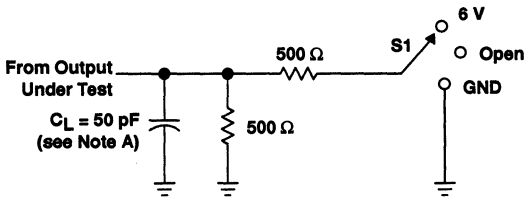
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			150		150		150		MHz
t_{pd}	CLK	Q	1	6.4		5.2	1	4.5	ns
	$\overline{CLR}$	Q	1.4	6		5.2	1.2	4.6	
t_{en}	$\overline{OE}$	Q	1	6.5		5.7	1	4.8	ns
t_{dis}	$\overline{OE}$	Q	1.8	5.6		4.7	1.3	4.5	ns

operating characteristics, T_A = 25°C

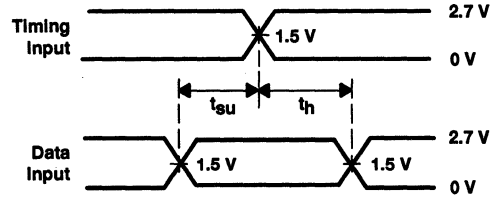
PARAMETER			TEST CONDITIONS	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 10 MHz	27	30	pF
		Outputs disabled		16	18	

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V

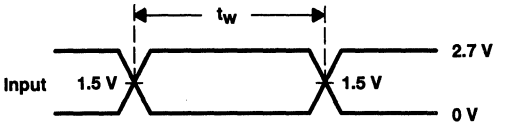


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

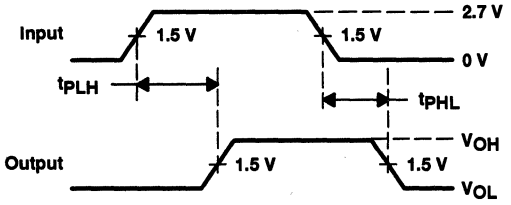
LOAD CIRCUIT



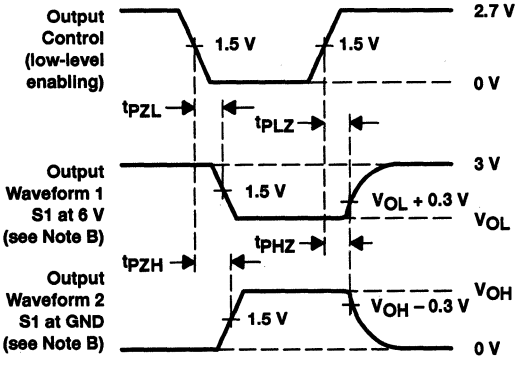
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Plastic 300-mil Thin Shrink Small-Outline Package**

description

This 1-bit-to-2-bit address driver is designed for 2.3-V to 3.6-V V_{CC} operation.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

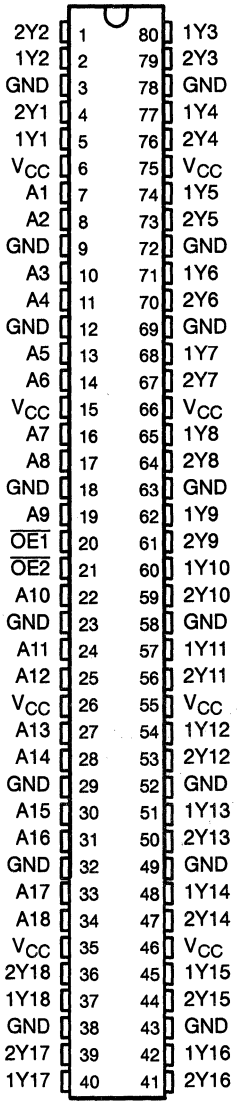
The SN74ALVCH16830 is packaged in TI's thin shrink small-outline (DBB) package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH16830 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{OE1}$	$\overline{OE2}$	A	1Yn	2Yn
L	H	H	H	Z
L	H	L	L	Z
H	L	H	Z	H
H	L	L	Z	L
L	L	H	H	H
L	L	L	L	L
H	H	X	Z	Z

DBB PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

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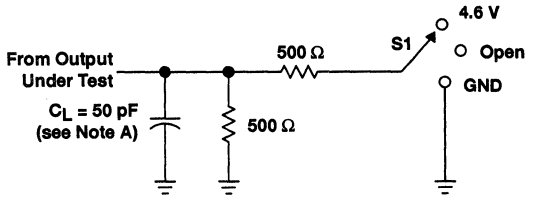
recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		–12	mA
		V_{CC} = 2.7 V		–12	
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		12	mA
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

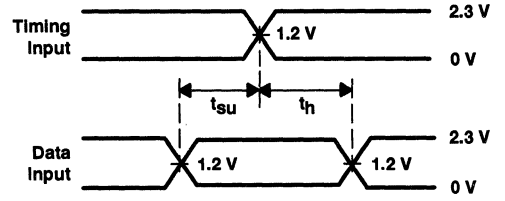
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

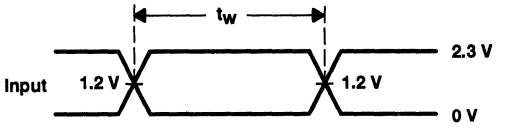


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND

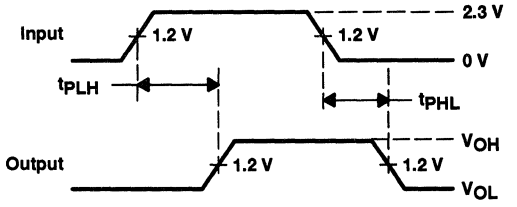
LOAD CIRCUIT



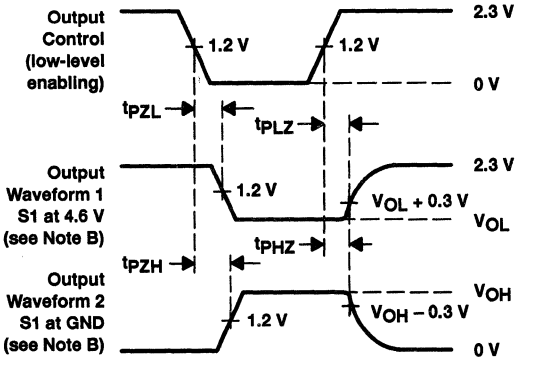
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

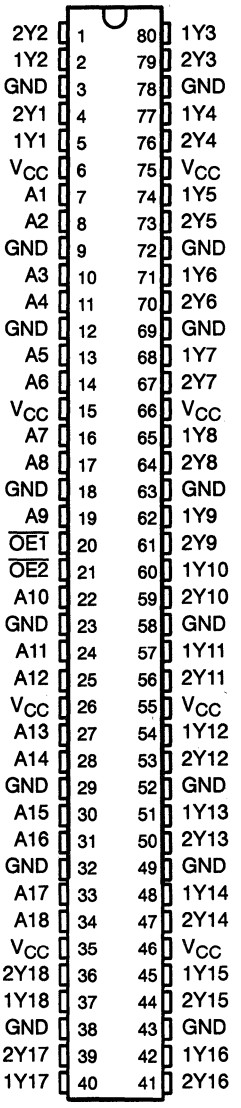
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Plastic 300-mil Thin Shrink Small-Outline Package**

DBB PACKAGE
(TOP VIEW)



description

This 1-bit-to-2-bit address driver is designed for 2.3-V to 3.6-V V_{CC} operation.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The outputs, which are designed to sink up to 12 mA, include 26-Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ALVCH162830 is packaged in TI's thin shrink small-outline (DBB) package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVCH162830 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{OE1}$	$\overline{OE2}$	A	1Yn	2Yn
L	H	H	H	Z
L	H	L	L	Z
H	L	H	Z	H
H	L	L	Z	L
L	L	H	H	H
L	L	L	L	L
H	H	X	Z	Z

PRODUCT PREVIEW

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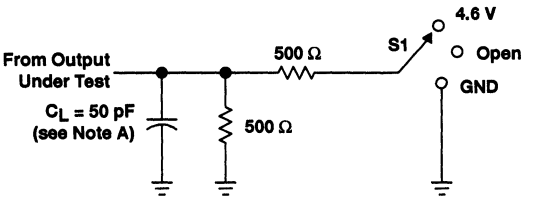
recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		–6	mA
		V_{CC} = 2.7 V		–8	
		V_{CC} = 3 V		–12	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		6	mA
		V_{CC} = 2.7 V		8	
		V_{CC} = 3 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

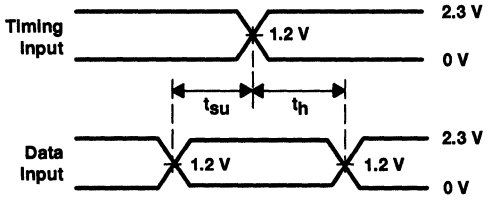
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

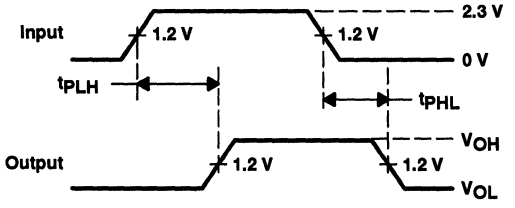


LOAD CIRCUIT

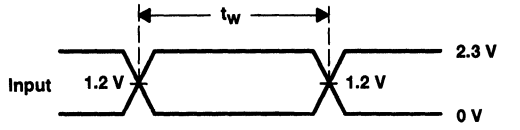
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND



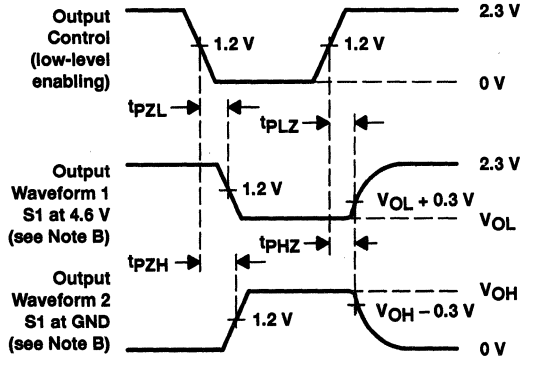
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Member of the Texas Instruments *Widebus*™ Family**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

description

This 20-bit universal bus driver is designed for 2.3-V to 3.6-V V_{CC} operation.

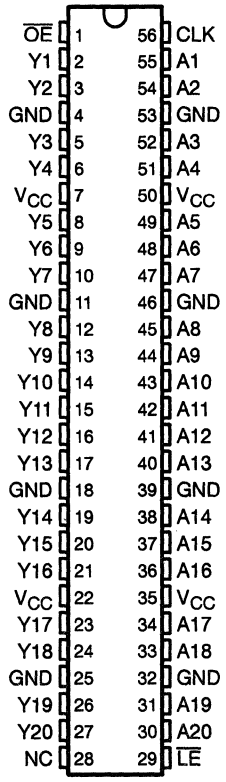
Data flow from A to Y is controlled by the output-enable ($\overline{OE}$) input. The device operates in the transparent mode when the latch-enable ($\overline{LE}$) input is low. The A data is latched if the clock (CLK) input is held at a high or low logic level. If $\overline{LE}$ is high, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLK. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16836 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16836 is characterized for operation from –40°C to 85°C.

DGG OR DL PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCT PREVIEW

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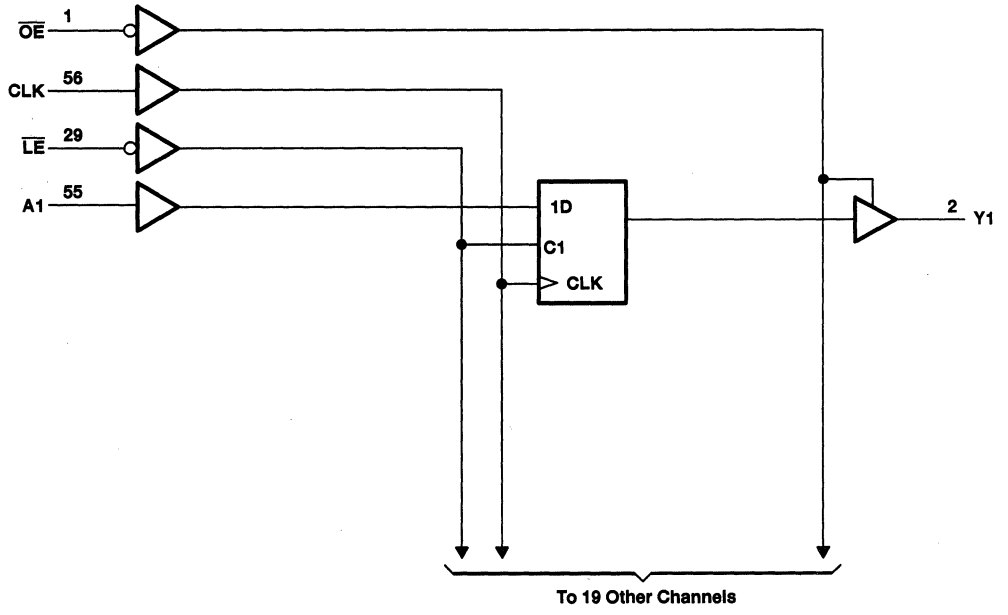
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}		I_{OH} = –100 µA		2.3 V to 3.6 V	V_{CC}–0.2			V
		I_{OH} = –6 mA,	V_{IH} = 1.7 V	2.3 V	2			
		I_{OH} = –12 mA	V_{IH} = 1.7 V	2.3 V	1.7			
			V_{IH} = 2 V	2.7 V	2.2			
			V_{IH} = 2 V	3 V	2.4			
		I_{OH} = –24 mA,	V_{IH} = 2 V	3 V	2			
V_{OL}		I_{OL} = 100 µA		2.3 V to 3.6 V			0.2	V
		I_{OL} = 6 mA,	V_{IL} = 0.7 V	2.3 V			0.4	
		I_{OL} = 12 mA	V_{IL} = 0.7 V	2.3 V			0.7	
			V_{IL} = 0.8 V	2.7 V			0.4	
		I_{OL} = 24 mA,	V_{IL} = 0.8 V	3 V			0.55	
I_I		V_I = V_{CC} or GND		3.6 V			±5	µA
I_{hold}		V_I = 0.7 V		2.3 V	45			µA
		V_I = 1.7 V			–45			
		V_I = 0.8 V		3 V	75			
		V_I = 2 V			–75			
		V_I = 0 to 3.6 V‡		3.6 V			±500	
I_{OZ}§		V_O = V_{CC} or GND		3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	µA
ΔI_{CC}		One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND	3 V to 3.6 V			750	µA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V				pF
	Data inputs							
C_o	Outputs	V_O = V_{CC} or GND		3.3 V				pF

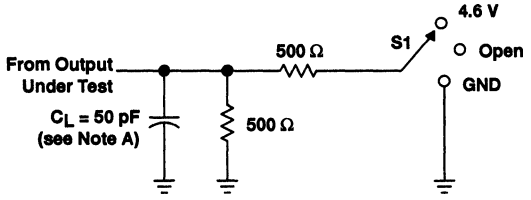
† All typical values are at V_{CC} = 3.3 V.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	$\overline{LE}$ low							ns
		CLK high or low							
t_{su}	Setup time	Data before CLK↑							ns
		Data before $\overline{LE}$↑, CLK high							
		Data before $\overline{LE}$↑, CLK low							
t_h	Hold time	Data after CLK↑							ns
		Data after $\overline{LE}$↑, CLK high or low							

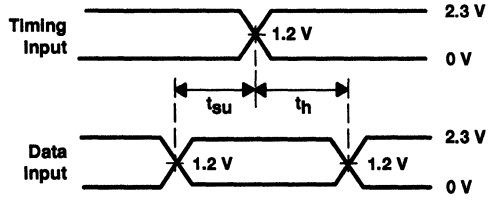
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

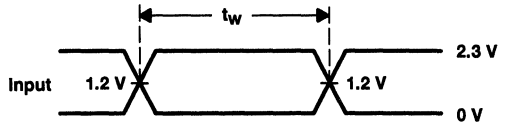


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND

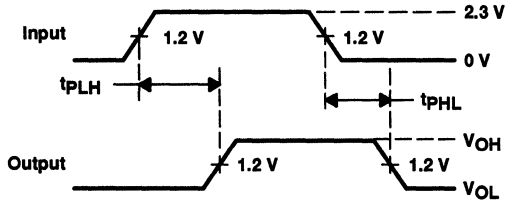
LOAD CIRCUIT



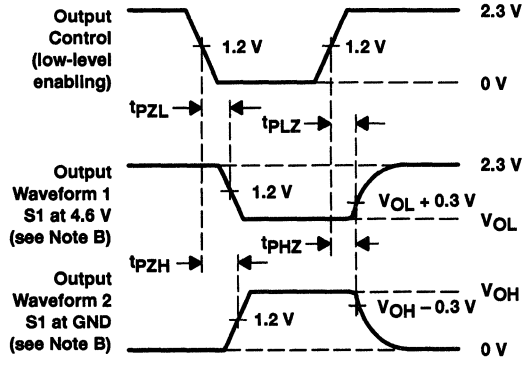
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



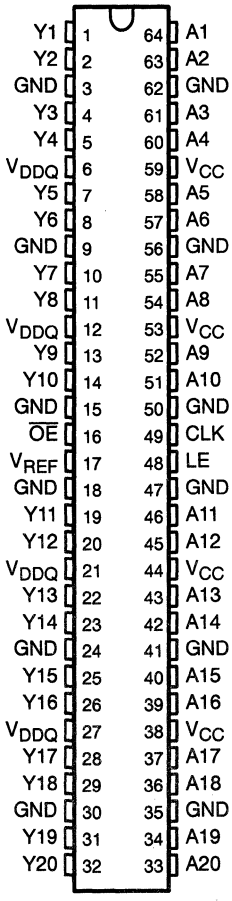
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments Widebus™ Family**
- **Supports SSTL_3 Signal Inputs and Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Meets SSTL_3 Class I and Class II Specifications**
- **Packaged in Plastic Thin Shrink Small-Outline Package**

DGG PACKAGE
(TOP VIEW)



description

This 20-bit universal bus driver is designed for 3-V to 3.6-V V_{CC} operation and SSTL_3 or LVTTL I/O levels.

Data flow from A to Y is controlled by the output-enable ($\overline{OE}$). The device operates in the transparent mode when LE is high. The A data is latched if LE is low and CLK is held at a high or low logic level. If LE is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLK. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74SSTL16837 is available in TI's thin shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74SSTL16837 is characterized for operation from –40°C to 85°C.

PRODUCT PREVIEW

Widebus is a trademark of Texas Instruments Incorporated.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		3.6	V
V_{DDQ}	I/O supply voltage		3		3.6	V
V_{REF}	Supply voltage		1.3	1.5	1.7	V
V_I	Input voltage		0		V_{CC}	V
V_{IH}	High-level input voltage	All pins	V_{REF}+200mV			V
V_{IL}	Low-level input voltage	All pins			V_{REF}–200mV	V
I_{OH}	High-level output current				–20	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature		–40		85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

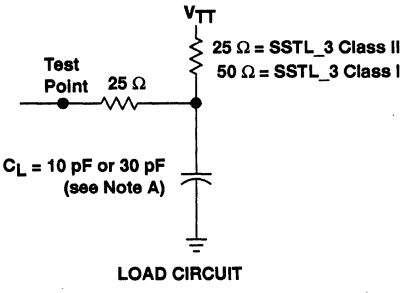
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3 V	I_I = –18 mA			–1.2	V
V_{OH}		V_{CC} = 3 V to 3.6 V	I_{OH} = –100 µA				V
		V_{CC} = 3 V	I_{OH} = –16 mA	2.2			
			I_{OH} = –20 mA	2.1			
V_{OL}		V_{CC} = 3 V to 3.6 V	I_{OL} = 100 µA				V
		V_{CC} = 3 V	I_{OH} = 16 mA			0.5	
			I_{OH} = 20 mA			0.55	
I_I	LE	V_{CC} = 3.6 V	V_I = 2.1 V or 0.9V, V_{REF} = 1.3 V or 1.7 V			±40	µA
	LE		V_I = 3.6 V or 0, V_{REF} = 1.3 V or 1.7 V			±500	
	Data inputs, $\overline{OE}$		V_I = 2.1 V or 0.9V, V_{REF} = 1.3 V or 1.7 V			±5	
	Data inputs, $\overline{OE}$		V_I = 3.6 V or 0, V_{REF} = 1.3 V or 1.7 V			±5	
	CLK		V_I = 2.1 V or 0.9V, V_{REF} = 1.3 V or 1.7 V			±150	
	CLK		V_I = 3.6 V or 0, V_{REF} = 1.3 V or 1.7 V			±2	mA
	V_{REF}		V_{REF} = 1.3 V or 1.7 V			±150	µA
I_{OZ}		V_{CC} = 3.6 V	V_O = 0.9 V or 2.1 V			±10	µA
			V_O = 0 or 3.6 V			±10	
I_{CC}		V_{CC} = 3.6 V	V_I = 2.1 V or 0.9 V, I_O = 0			90	mA
			V_I = 3.6 V or 0, I_O = 0			90	
C_i	Control pin	V_{CC} = 3.3 V	V_I = 2.1 V or 0.9 V				pF
	A port						
C_O	Y port	V_{CC} = 3.3 V	V_O = 2.1 V or 0.9 V				pF

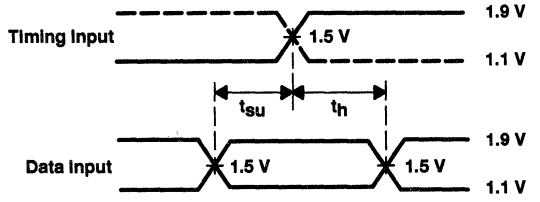
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PRODUCT PREVIEW

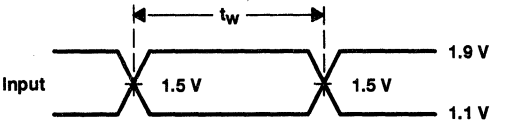
PARAMETER MEASUREMENT INFORMATION



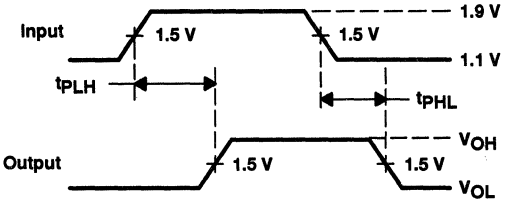
LOAD CIRCUIT



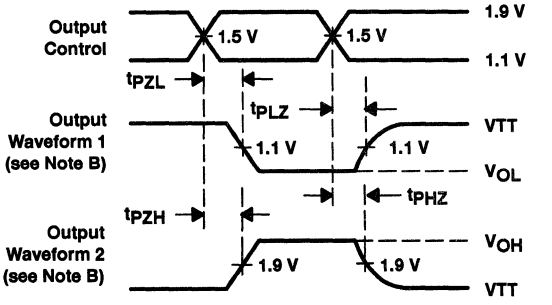
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

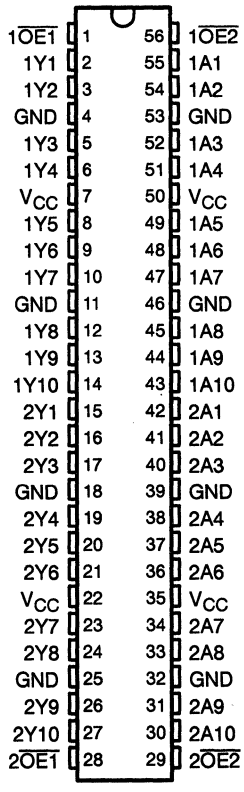
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 1 ns, t_f ≤ 1 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. VTT = V_{REF} = VCC X 0.45
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PHL} and t_{PLH} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 20-bit non-inverting buffer/driver is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16827 is composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable ($1\overline{OE1}$ and $1\overline{OE2}$ or $2\overline{OE1}$ and $2\overline{OE2}$) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16827 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16827 is characterized for operation from –40°C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

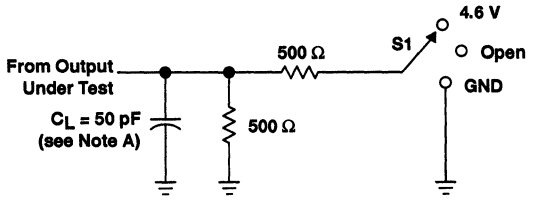
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		–12	mA
		V_{CC} = 2.7 V		–12	
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		12	mA
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

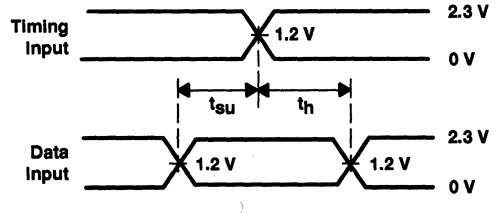
NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

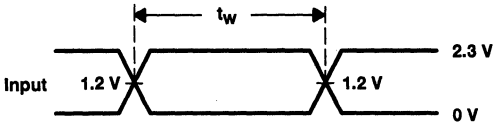


LOAD CIRCUIT

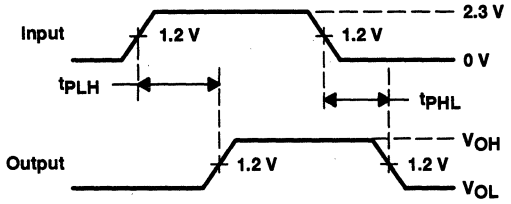
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND



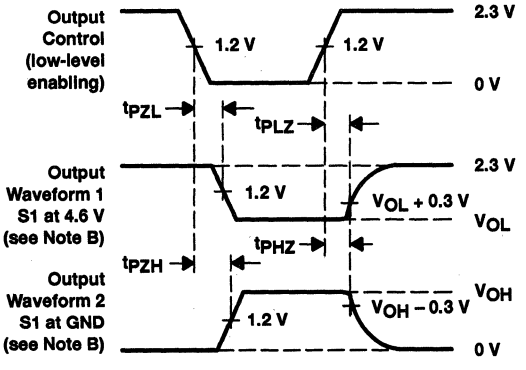
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



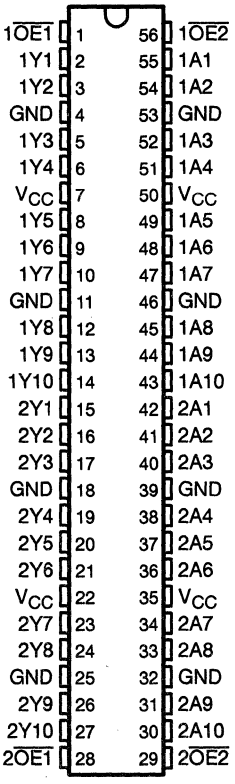
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 20-bit noninverting buffer/driver is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH162827 is composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable ($1\overline{OE1}$ and $1\overline{OE2}$ or $2\overline{OE1}$ and $2\overline{OE2}$) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

The outputs, which are designed to sink up to 12 mA, include 26-Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162827 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH162827 is characterized for operation from –40°C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

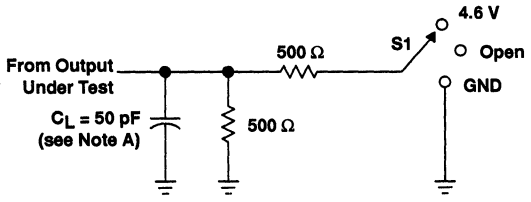
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		–6	mA
		V_{CC} = 2.7 V		–8	
		V_{CC} = 3 V		–12	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		6	mA
		V_{CC} = 2.7 V		8	
		V_{CC} = 3 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

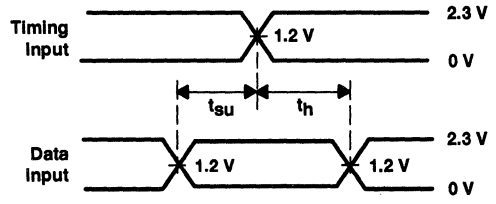
NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

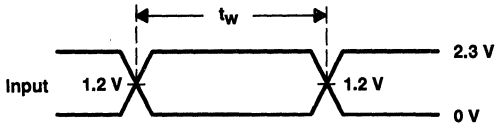


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND

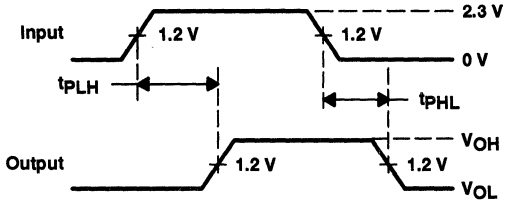
LOAD CIRCUIT



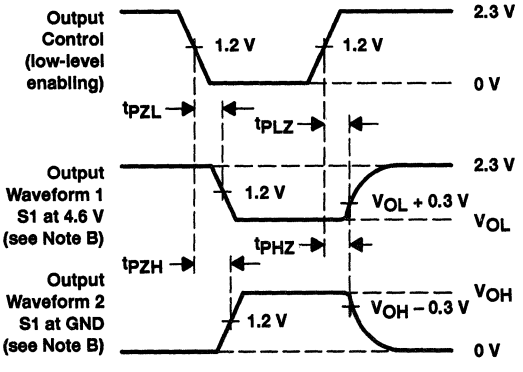
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



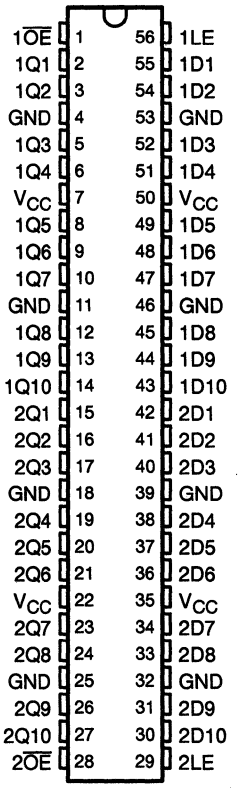
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 20-bit bus-interface D-type latch is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16841 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, unidirectional bus drivers, and working registers.

The SN74ALVCH16841 can be used as two 10-bit latches or one 20-bit latch. The 20 latches are transparent D-type latches. The device has noninverting data (D) inputs and provides true data at its outputs. While the latch-enable (1LE or 2LE) input is high, the Q outputs of the corresponding 10-bit latch follow the D inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($1\overline{OE}$ or $2\overline{OE}$) input can be used to place the outputs of the corresponding 10-bit latch in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

The output-enable ($\overline{OE}$) input does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating inputs at a valid logic level.

The SN74ALVCH16841 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16841 is characterized for operation from –40°C to 85°C.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) ..... –50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		–12	mA
		V_{CC} = 2.7 V		–12	
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		12	mA
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

timing requirements over recommended ranges of supply voltage and operating free-air temperature, (unless otherwise noted) (see Figures 1 and 2)

PARAMETER		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high or low	3.3		3.3		3.3		ns
t_{su}	Setup time, data before LE↑	0.9		0.7		1.1		ns
t_h	Hold time, data after LE↑	1.2		1.5		1.1		ns

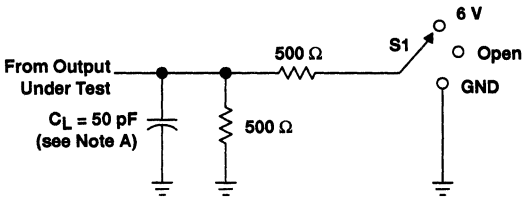
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	1.1	5.6	4.7		1.2	3.9	ns
	LE	Q	1	6.2	5.1		1	4.3	
t_{en}	$\overline{OE}$	Q	1	6.7	6		1	4.9	ns
t_{dis}	$\overline{OE}$	Q	1.8	5.5	4.3		1.3	4.1	ns

operating characteristics, T_A = 25°C

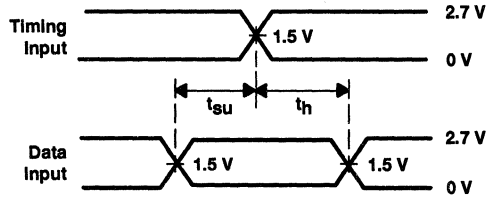
PARAMETER			TEST CONDITIONS	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 10 MHz	12	20	pF
		Outputs disabled		1	3	

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V

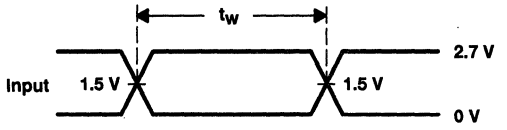


LOAD CIRCUIT

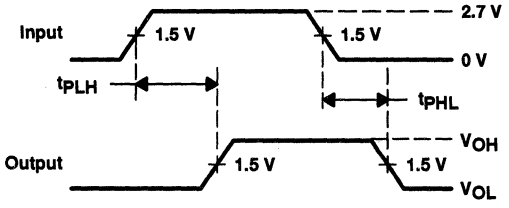
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



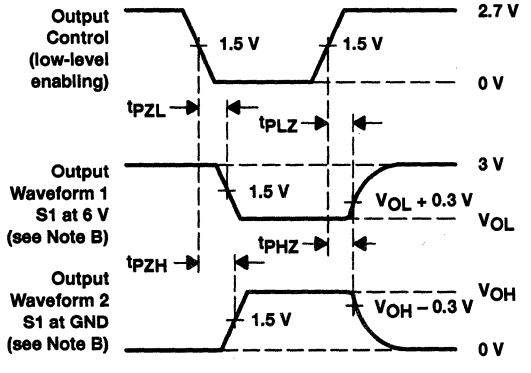
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



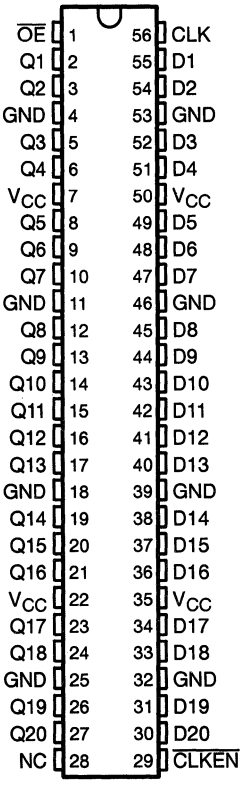
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



NC – No internal connection

description

This 20-bit flip-flop is designed specifically for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16721 20 flip-flops are edge-triggered D-type flip-flops with qualified clock storage. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs if the clock-enable ($\overline{CLKEN}$) input is low. If $\overline{CLKEN}$ is high, no data is stored.

A buffered output-enable ($\overline{OE}$) input places the 20 outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components. $\overline{OE}$ does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16721 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16721 is characterized for operation from –40°C to 85°C.

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recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		–12	mA
		V_{CC} = 2.7 V		–12	
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		12	mA
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

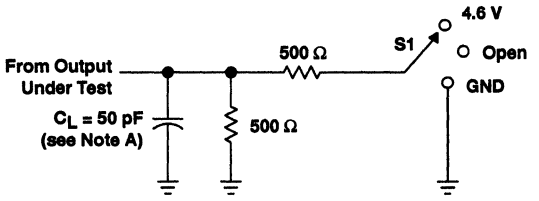
NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}		I_{OH} = –100 µA		2.3 V to 3.6 V	V_{CC}–0.2			V
		I_{OH} = –6 mA,	V_{IH} = 1.7 V	2.3 V	2			
		I_{OH} = –12 mA,	V_{IH} = 1.7 V	2.3 V	1.7			
		I_{OH} = –12 mA,	V_{IH} = 2 V	2.7 V	2.2			
		I_{OH} = –12 mA,	V_{IH} = 2 V	3 V	2.4			
		I_{OH} = –24 mA,	V_{IH} = 2 V	3 V	2			
V_{OL}		I_{OL} = 100 µA		2.3 V to 3.6 V			0.2	V
		I_{OL} = 6 mA,	V_{IL} = 0.7 V	2.3 V			0.4	
		I_{OL} = 12 mA,	V_{IL} = 0.7 V	2.3 V			0.7	
		I_{OL} = 12 mA,	V_{IL} = 0.8 V	2.7 V			0.4	
		I_{OL} = 24 mA,	V_{IL} = 0.8 V	3 V			0.55	
I_I		V_I = V_{CC} or GND		3.6 V			±5	µA
$I_{I(hold)}$		V_I = 0.7 V		2.3 V	45			µA
		V_I = 1.7 V			–45			
		V_I = 0.8 V		3 V	75			
		V_I = 2 V			–75			
		V_I = 0 to 3.6 V‡		3.6 V			±500	
I_{OZ}		V_O = V_{CC} or GND		3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	µA
ΔI_{CC}		One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND	3 V to 3.6 V			750	µA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		3.5		pF
	Data inputs					6		
C_{io}	Data inputs	V_O = V_{CC} or GND		3.3 V		7		pF

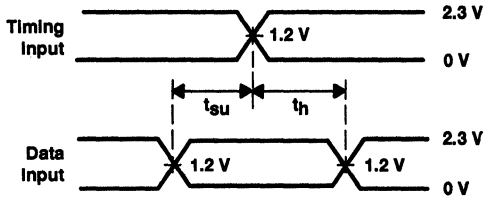
† Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

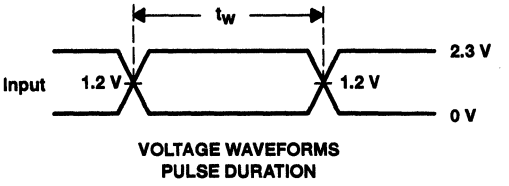


LOAD CIRCUIT

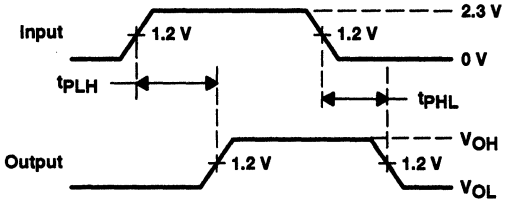
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND



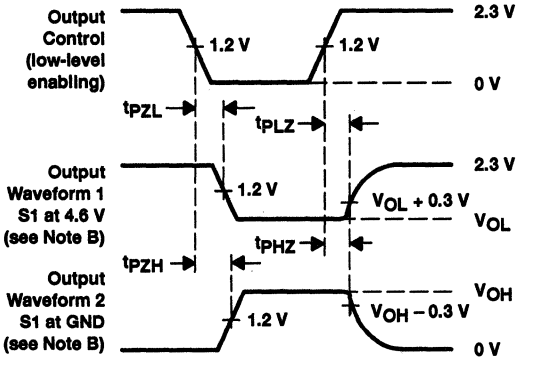
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



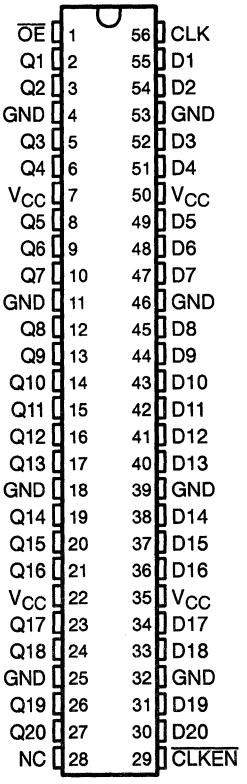
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



NC – No internal connection

description

This 20-bit flip-flop is designed for low-voltage 2.3-V to 3.6-V V_{CC} operation.

The 20 flip-flops are edge-triggered D-type flip-flops with qualified clock storage. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs if the clock-enable ($\overline{CLKEN}$) input is low. If $\overline{CLKEN}$ is high, no data is stored.

A buffered output-enable ($\overline{OE}$) input places the 20 outputs in either a normal logic state (high or low level) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components. $\overline{OE}$ does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or floating data inputs at a valid logic level.

The outputs, which are designed to sink up to 12 mA, include 26-Ω resistors to reduce overshoot and undershoot.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package ..... 1 W
DL package ..... 1.4 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.3 V		–6	mA
		V_{CC} = 2.7 V		–8	
		V_{CC} = 3 V		–12	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		6	mA
		V_{CC} = 2.7 V		8	
		V_{CC} = 3 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figures 1 and 2)

			V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	0	150	MHz
t_w	Pulse duration, CLK high or low		3.3		3.3		3.3		ns
t_{su}	Setup time	Data before CLK↑	4		3.6		3.1		ns
		$\overline{CLKEN}$ before CLK↑	3.4		3.1		2.7		
t_h	Hold time	Data after CLK↑	0		0		0		ns
		$\overline{CLKEN}$ after CLK↑	0		0		0		

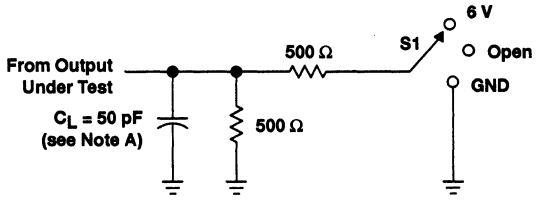
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			150		150		150		MHz
t_{pd}	CLK	Q	1	7.5		6.4	1	5.5	ns
t_{en}	$\overline{OE}$	Q	1	7.9		7.2	1	6	ns
t_{dis}	$\overline{OE}$	Q	1	6.7		5.6	1	5.2	ns

operating characteristics, T_A = 25°C

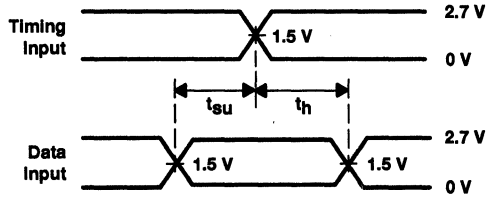
PARAMETER			TEST CONDITIONS	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V	UNIT
				TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 10 MHz	55	59	pF
		Outputs disabled		46	49	

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.7 V AND 3.3 V ± 0.3 V

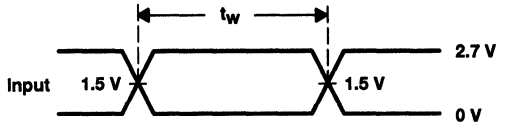


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

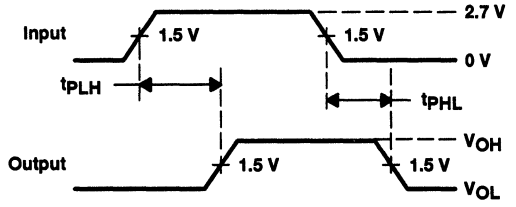
LOAD CIRCUIT



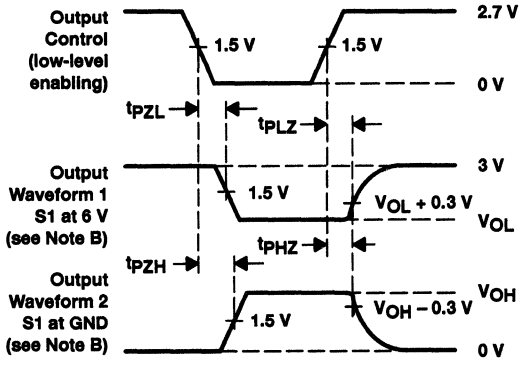
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



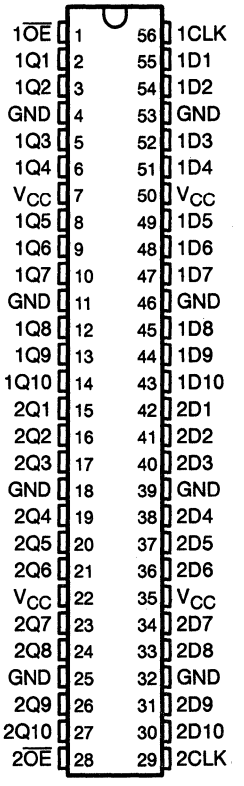
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)



description

This 20-bit bus-interface flip-flop is designed for 2.3-V to 3.6-V V_{CC} operation.

The SN74ALVCH16821 can be used as two 10-bit flip-flops or one 20-bit flip-flop. The 20 flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the ten outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16821 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed circuit board area.

The SN74ALVCH16821 is characterized for operation from –40°C to 85°C.

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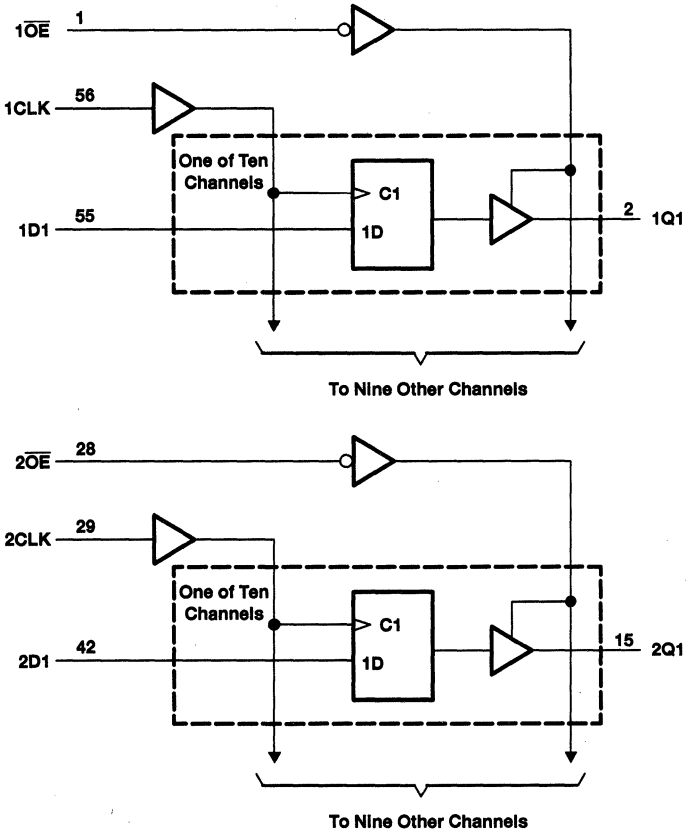
logic diagram (positive logic)

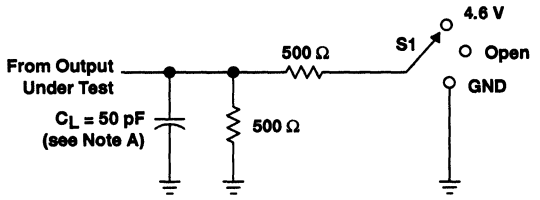


electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}		I_{OH} = –100 µA		2.3 V to 3.6 V	V_{CC}–0.2			V
		I_{OH} = –6 mA,	V_{IH} = 1.7 V	2.3 V	2			
		I_{OH} = –12 mA	V_{IH} = 1.7 V	2.3 V	1.7			
			V_{IH} = 2 V	2.7 V	2.2			
			V_{IH} = 2 V	3 V	2.4			
		I_{OH} = –24 mA,	V_{IH} = 2 V	3 V	2			
V_{OL}		I_{OL} = 100 µA		2.3 V to 3.6 V			0.2	V
		I_{OL} = 6 mA,	V_{IL} = 0.7 V	2.3 V			0.4	
		I_{OL} = 12 mA	V_{IL} = 0.7 V	2.3 V			0.7	
			V_{IL} = 0.8 V	2.7 V			0.4	
		I_{OL} = 24 mA,	V_{IL} = 0.8 V	3 V			0.55	
I_I		V_I = V_{CC} or GND		3.6 V			±5	µA
$I_{I(hold)}$		V_I = 0.7 V		2.3 V	45			µA
		V_I = 1.7 V			–45			
		V_I = 0.8 V		3 V	75			
		V_I = 2 V			–75			
		V_I = 0 to 3.6 V‡		3.6 V			±500	
I_{OZ}		V_O = V_{CC} or GND		3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	µA
ΔI_{CC}		One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND	3 V to 3.6 V			750	µA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		3.5		pF
	Data inputs					6		
C_o	Outputs	V_O = V_{CC} or GND		3.3 V		7		pF

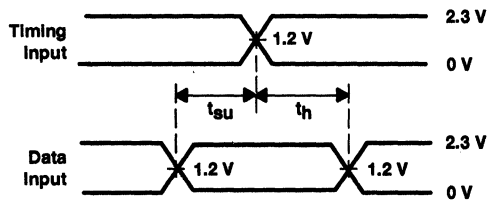
† All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.

PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5 V ± 0.2 V

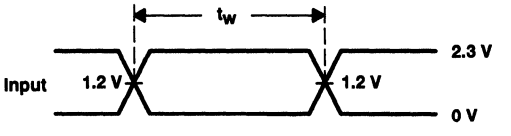


LOAD CIRCUIT

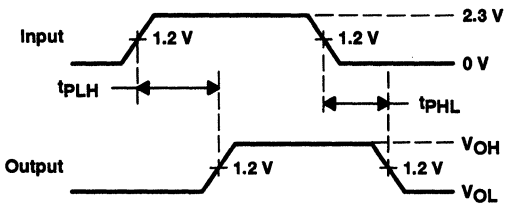
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	4.6 V
t_{PHZ}/t_{PZH}	GND



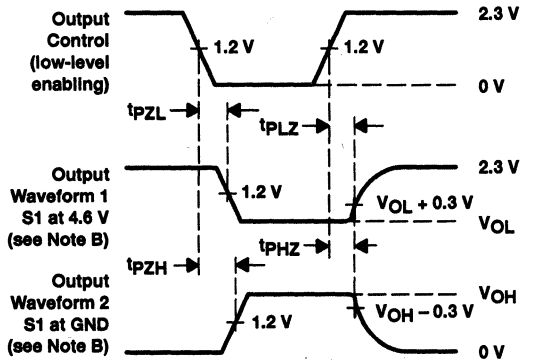
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



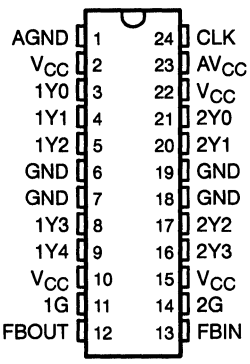
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

- **Phase-Lock Loop Clock Distribution for Synchronous DRAM Applications**
- **Distributes One Clock Input to One Bank of Five and One Bank of Four Outputs**
- **Separate Output Enable for Each Output Bank**
- **External Feedback (FBIN) Pin Is Used to Synchronize the Outputs to the Clock Input**
- **No External RC Network Required**
- **Operates at 3.3-V V_{CC}**
- **Packaged in Plastic 24-Pin Thin Shrink Small-Outline Package**

PW PACKAGE
(TOP VIEW)



description

The CDC509 is a high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The CDC509 operates at 3.3-V V_{CC} and is designed to drive up to five clock loads per output.

One bank of five outputs and one bank of four outputs provide nine low-skew, low-jitter copies of CLK. Output signal duty cycles are adjusted to 50 percent, independent of the duty cycle at CLK. Each bank of outputs can be enabled or disabled separately via the control (1G and 2G) inputs. When the G inputs are high, the outputs switch in phase and frequency with CLK; when the G inputs are low, the outputs are disabled to the logic-low state.

Unlike many products containing PLLs, the CDC509 does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CDC509 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at CLK, as well as following any changes to the PLL reference or feedback signals. The PLL can be bypassed for test purposes by strapping AV_{CC} to ground.

The CDC509 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUTS		
1G	2G	CLK	1Y (0:4)	2Y (0:3)	FBOUT
X	X	L	L	L	L
L	L	H	L	L	H
L	H	H	L	H	H
H	L	H	H	L	H
H	H	H	H	H	H

PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	TERMINAL NO.	TYPE	DESCRIPTION
CLK	24	I	Clock input. CLK provides the clock signal to be distributed by the CDC509 clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
FBIN	13	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN.
1G	11	I	Output bank enable. 1G is the output enable for outputs 1Y(0:4). When 1G is low, outputs 1Y(0:4) are disabled to a logic-low state. When 1G is high, all outputs 1Y(0:4) are enabled and switch at the same frequency as CLK.
2G	14	I	Output bank enable. 2G is the output enable for outputs 2Y(0:3). When 2G is low, outputs 2Y(0:3) are disabled to a logic low state. When 2G is high, all outputs 2Y(0:3) are enabled and switch at the same frequency as CLK.
FBOUT	12	O	Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL.
1Y(0:4)	3, 4, 5, 8, 9	O	Clock outputs. These outputs provide low-skew copies of CLK. Output bank 1Y(0:4) is enabled via the 1G input. These outputs can be disabled to a logic-low state by deasserting the 1G control input.
2Y(0:3)	16, 17, 20 21	O	Clock outputs. These outputs provide low-skew copies of CLK. Output bank 2Y(0:3) is enabled via the 2G input. These outputs can be disabled to a logic-low state by deasserting the 2G control input.
AV_{CC}	23	Power	Analog power supply. AV_{CC} provides the power reference for the analog circuitry. In addition, AV_{CC} can be used to bypass the PLL for test purposes. When AV_{CC} is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
V_{CC}	2, 10, 15, 22	Power	Power supply
GND	6, 7, 18, 19	Ground	Ground

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 6.5 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance state
or power-off state, V_O (see Note 1) ..... –0.5 V to 6.5 V
Voltage range applied to any output in the high
or low state, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3) ..... 0.7 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

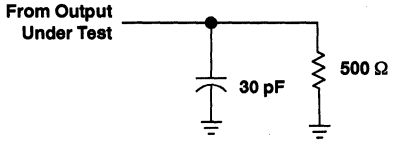
PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (see Note 5 and Figures 1 and 2)

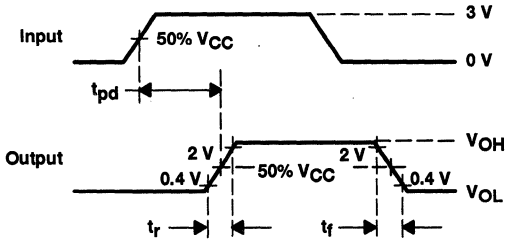
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.165 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
$t_{phase\ error}$†	CLKIN↑	FBIN↑			–150	150	ps
$t_{sk(o)}$†	Any Y or FBOUT	Any Y or FBOUT				250	ps
$Jitter_{(pk-pk)}$		Any Y or FBOUT			–100	100	ps
Duty cycle		Any Y or FBOUT			45%	55%	
t_r		Any Y or FBOUT	0.4	1.6	0.5	2	ns
t_f		Any Y or FBOUT	0.4	1.6	0.5	2	ns

† The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.
NOTE 5: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

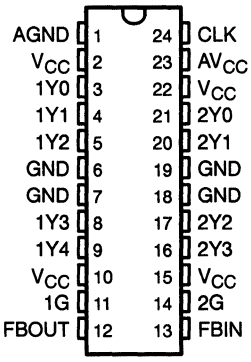
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 100 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **Phase-Lock Loop Clock Distribution for Synchronous DRAM Applications**
- **Distributes One Clock Input to One Bank of Five and One Bank of Four Outputs**
- **Separate Output Enable for Each Output Bank**
- **External Feedback (FBIN) Pin Is Used to Synchronize the Outputs to the Clock Input**
- **On-Chip Series Damping Resistors**
- **No External RC Network Required**
- **Operates at 3.3-V V_{CC}**
- **Packaged in Plastic 24-Pin Thin Shrink Small-Outline Package**

PW PACKAGE
(TOP VIEW)



description

The CDC2509 is a high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The CDC2509 operates at 3.3-V V_{CC} and provides integrated series-damping resistors that make it ideal for driving point-to-point loads.

One bank of five outputs and one bank of four outputs provide nine low-skew, low-jitter copies of CLK. Output signal duty cycles are adjusted to 50 percent, independent of the duty cycle at CLK. Each bank of outputs can be enabled or disabled separately via the control (1G and 2G) inputs. When the G inputs are high, the outputs switch in phase and frequency with CLK; when the G inputs are low, the outputs are disabled to the logic-low state.

Unlike many products containing PLLs, the CDC2509 does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CDC2509 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at CLK, as well as following any changes to the PLL reference or feedback signals. The PLL can be bypassed for test purposes by strapping AV_{CC} to ground.

The CDC2509 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUTS		
1G	2G	CLK	1Y (0:4)	2Y (0:3)	FBOUT
X	X	L	L	L	L
L	L	H	L	L	H
L	H	H	L	H	H
H	L	H	H	L	H
H	H	H	H	H	H

PRODUCT PREVIEW

Terminal Functions

TERMINAL NAME	TERMINAL NO.	TYPE	DESCRIPTION
CLK	24	I	Clock input. CLK provides the clock signal to be distributed by the CDC2509 clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
FBIN	13	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN.
1G	11	I	Output bank enable. 1G is the output enable for outputs 1Y(0:4). When 1G is low, outputs 1Y(0:4) are disabled to a logic-low state. When 1G is high, all outputs 1Y(0:4) are enabled and switch at the same frequency as CLK.
2G	14	I	Output bank enable. 2G is the output enable for outputs 2Y(0:3). When 2G is low, outputs 2Y(0:3) are disabled to a logic low state. When 2G is high, all outputs 2Y(0:3) are enabled and switch at the same frequency as CLK.
FBOUT	12	O	Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL. FBOUT has and integrated 25-Ω series-damping resistor.
1Y (0:4)	3, 4, 5, 8, 9	O	Clock outputs. These outputs provide low-skew copies of CLK. Output bank 1Y(0:4) is enabled via the 1G input. These outputs can be disabled to a logic-low state by deasserting the 1G control input. Each output has an integrated 25-Ω series-damping resistor.
2Y (0:3)	16, 17, 20, 21	O	Clock outputs. These outputs provide low-skew copies of CLK. Output bank 2Y(0:3) is enabled via the 2G input. These outputs can be disabled to a logic-low state by deasserting the 2G control input. Each output has an integrated 25-Ω series-damping resistor.
AV_{CC}	23	Power	Analog power supply. AV_{CC} provides the power reference for the analog circuitry. In addition, AV_{CC} can be used to bypass the PLL for test purposes. When AV_{CC} is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
V_{CC}	2, 10, 15, 22	Power	Power supply
GND	6, 7, 18, 19	Ground	Ground

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency		25	125	MHz
	Input clock duty cycle		40%	60%	
	Stabilization time†	After power up		1	ms

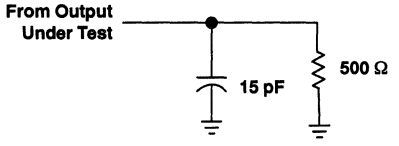
† Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 15 pF (see Note 5 and Figures 1 and 2)

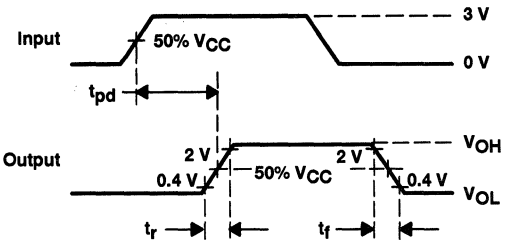
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.165 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
$t_{phase\ error}$‡	CLKIN↑	FBIN↑			–150	150	ps
$t_{sk(o)}$‡	Any Y or FBOUT	Any Y or FBOUT				250	ps
$Jitter_{(pk-pk)}$		Any Y or FBOUT			–100	100	ps
Duty cycle		Any Y or FBOUT			45%	55%	
t_r		Any Y or FBOUT	0.4	1.6	0.5	2	ns
t_f		Any Y or FBOUT	0.4	1.6	0.5	2	ns

‡ The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.
NOTE 5: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

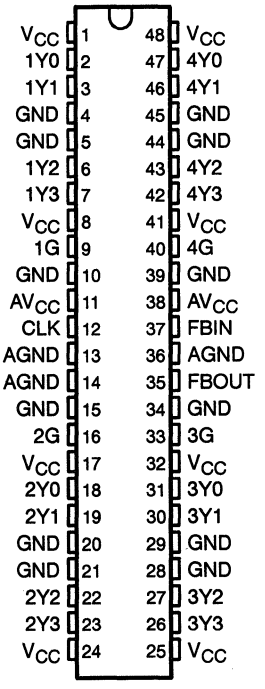
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 100 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

- **Phase-Lock Loop Clock Distribution for Synchronous DRAM Applications**
- **Distributes One Clock Input to Four Banks of Four Outputs**
- **Separate Output Enable for Each Output Bank**
- **External Feedback Pin (FBIN) Is Used to Synchronize the Outputs to the Clock Input**
- **No External RC Network Required**
- **Operates at 3.3-V V_{CC}**
- **Packaged in Plastic 48-Pin Thin Shrink Small-Outline Package**

DGG PACKAGE
(TOP VIEW)



description

The CDC516 is a high-performance, low-skew, low-jitter, phase-lock loop clock driver. It uses a phase-lock loop (PLL) to precisely align, in both frequency and phase, the feedback output (FBOUT) to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The CDC516 operates at 3.3-V V_{CC} and is designed to drive up to five clock loads per output.

Four banks of four outputs provide 16 low-skew, low-jitter copies of the input clock. Output signal duty cycles are adjusted to 50 percent, independent of the duty cycle at the input clock. Each bank of outputs can be enabled or disabled separately via the 1G, 2G, 3G, and 4G control inputs. When the G inputs are high, the outputs switch in phase and frequency with CLK; when the G inputs are low, the outputs are disabled to the logic-low state.

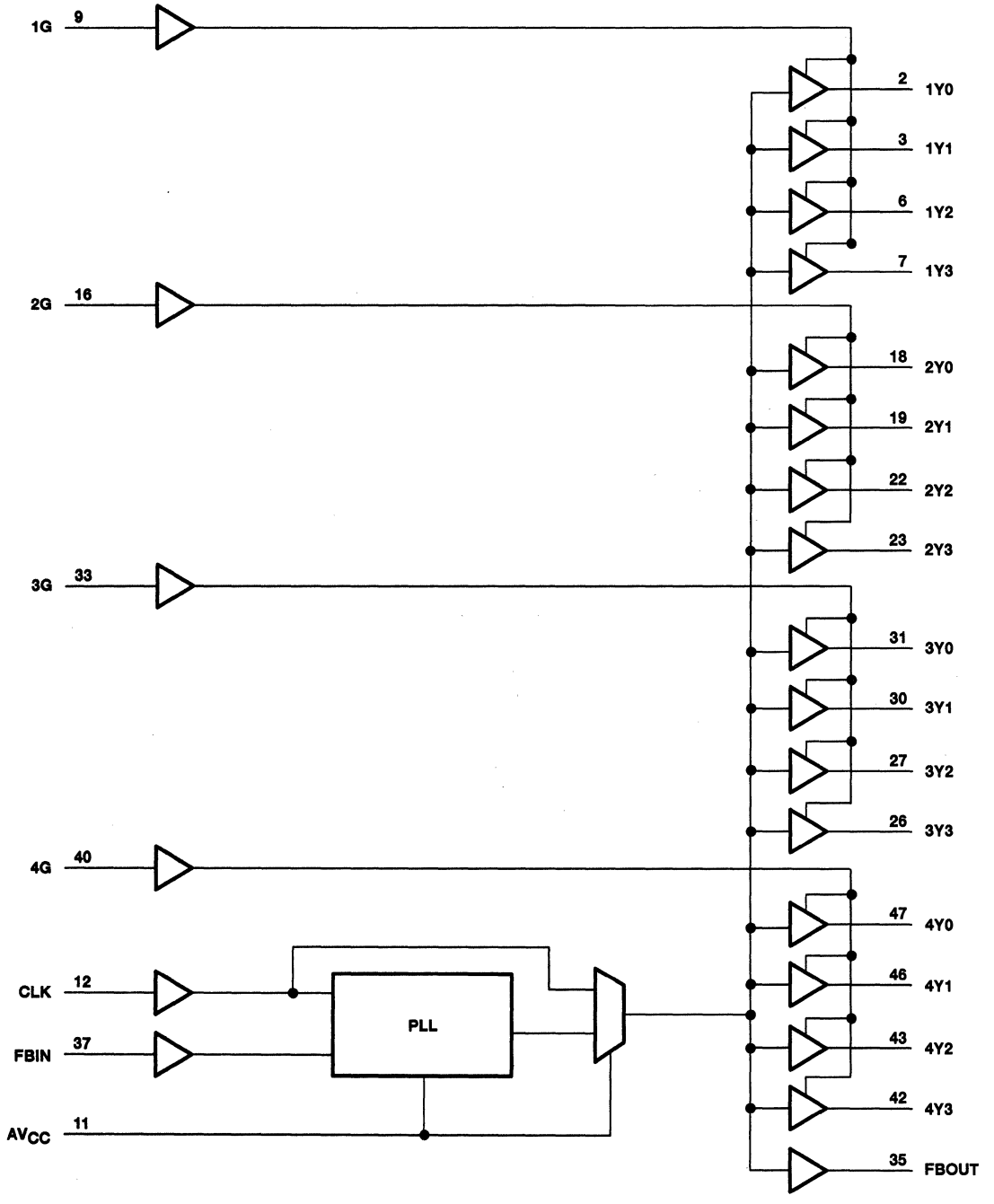
Unlike many products containing PLLs, the CDC516 does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CDC516 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required following power up and application of a fixed-frequency, fixed-phase signal at CLK, as well as following any changes to the PLL reference or feedback signals. The PLL may be bypassed for test purposes by strapping AV_{CC} to ground.

The CDC516 is characterized for operation from 0°C to 70°C.

PRODUCT PREVIEW

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 6.5 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance state
or power-off state, V_O (see Note 1) ..... –0.5 V to 6.5 V
Voltage range applied to any output in the high
or low state, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3) ..... 0.85 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
I_{OH}	High-level output current		–20	mA
I_{OL}	Low-level output current		20	mA
T_A	Operating free-air temperature	0	70	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP‡	MAX	UNIT
V_{IK}	I_I = –18 mA		3 V			–1.2	V
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2			V
	I_{OH} = –20 mA		3 V	2.4			
V_{OL}	I_{OL} = 100 µA		MIN to MAX			0.2	V
	I_{OL} = 20 mA		3 V			0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V			±5	µA
I_{CC}	$V_I = V_{CC}$ or GND	I_O = 0	3.6 V				mA
ΔI_{CC}	One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND	3.3 V to 3.6 V			500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V		4		pF
C_o	$V_O = V_{CC}$ or GND		3.3 V		6		pF

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

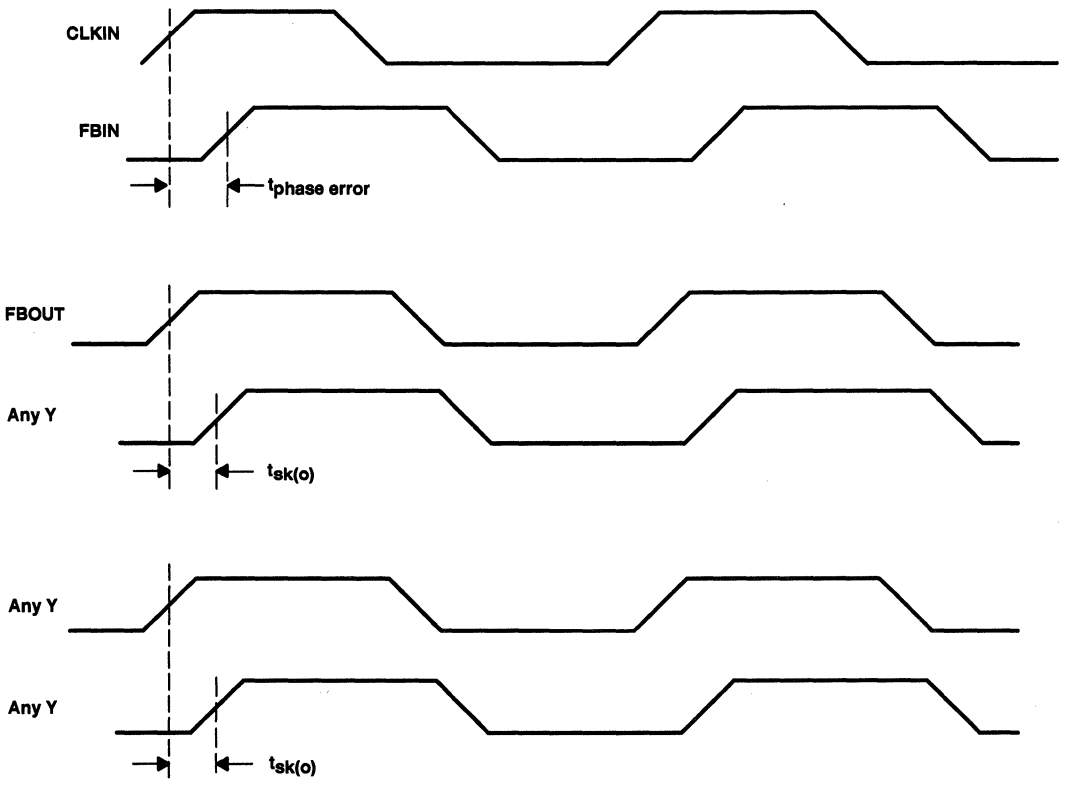
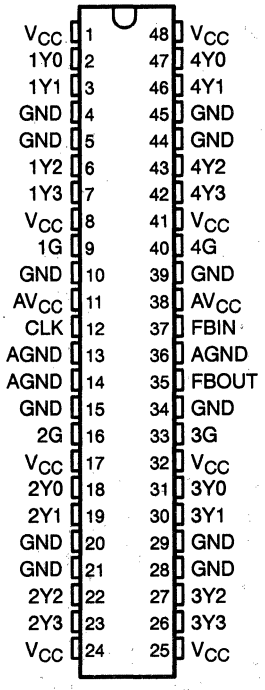


Figure 2. Phase Error and Skew Calculations

- **Phase-Lock Loop Clock Distribution for Synchronous DRAM Applications**
- **Distributes One Clock Input to Four Banks of Four Outputs**
- **Separate Output Enable for Each Output Bank**
- **External Feedback Pin (FBIN) Is Used to Synchronize the Outputs to the Clock Input**
- **On-Chip Series-Damping Resistors**
- **No External RC Network Required**
- **Operates at 3.3-V V_{CC}**
- **Packaged in Plastic 48-Pin Thin Shrink Small-Outline Package**

DGG PACKAGE
(TOP VIEW)



description

The CDC2516 is a high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the feedback output (FBOUT) to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The CDC2516 operates at 3.3-V V_{CC} and provides integrated series-damping resistors that make it ideal for driving point-to-point loads.

Four banks of four outputs provide 16 low-skew, low-jitter copies of the input clock. Output signal duty cycles are adjusted to 50 percent, independent of the duty cycle at the input clock. Each bank of outputs can be enabled or disabled separately via the 1G, 2G, 3G, and 4G control inputs. When the G inputs are high, the outputs switch in phase and frequency with CLK; when the G inputs are low, the outputs are disabled to the logic-low state.

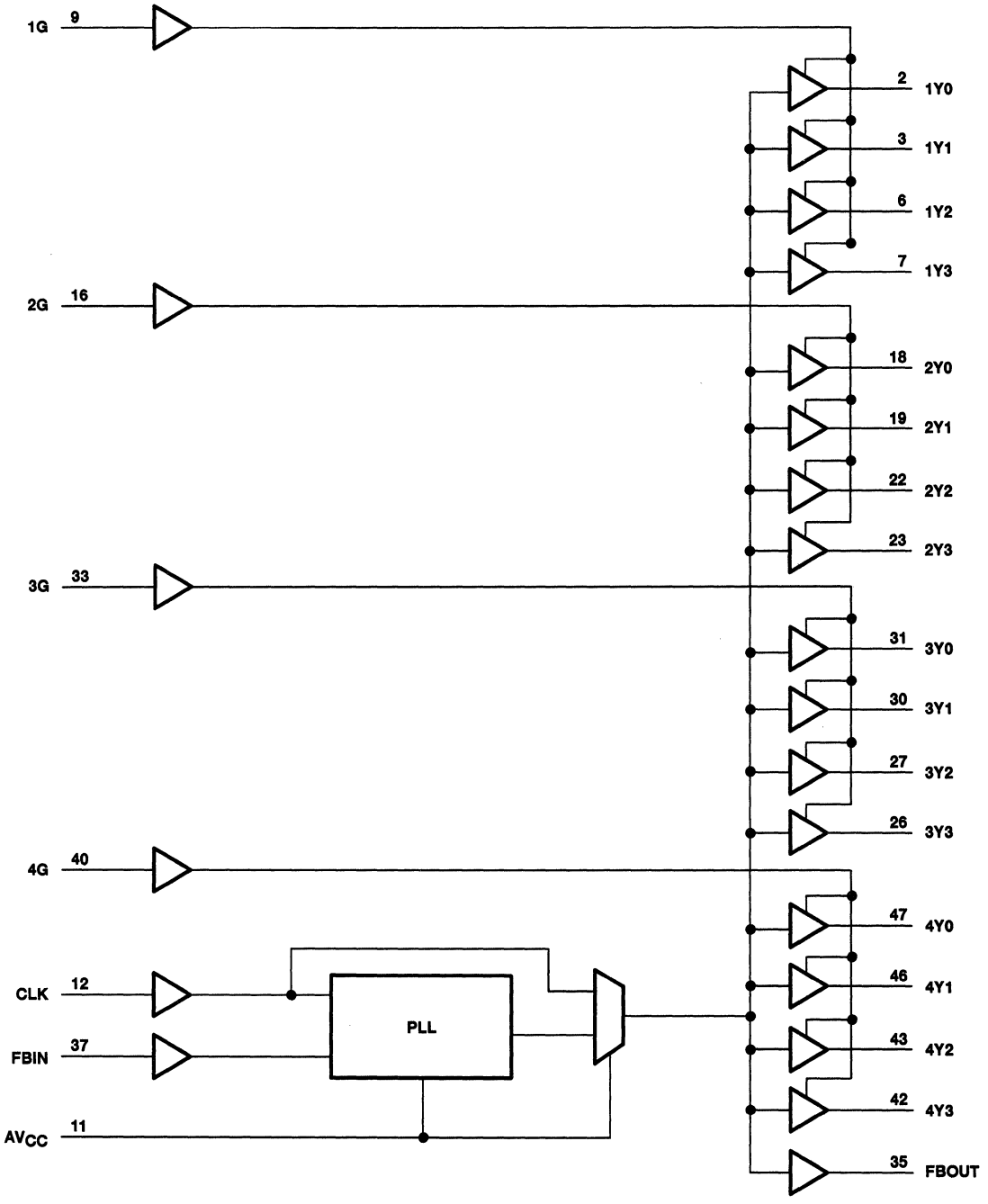
Unlike many products containing PLLs, the CDC2516 does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CDC2516 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required following power up and application of a fixed-frequency, fixed-phase signal at CLK, as well as following any changes to the PLL reference or feedback signals. The PLL may be bypassed for test purposes by strapping AV_{CC} to ground.

The CDC2516 is characterized for operation from 0°C to 70°C.

PRODUCT PREVIEW

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 6.5 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance state
or power-off state, V_O (see Note 1) ..... –0.5 V to 6.5 V
Voltage range applied to any output in the high
or low state, V_O (see Notes 1 and 2) ..... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) ..... –50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±50 mA
Continuous current through each V_{CC} or GND ..... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3) ..... 0.85 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
I_{OH}	High-level output current		–12	mA
I_{OL}	Low-level output current		12	mA
T_A	Operating free-air temperature	0	70	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP‡	MAX	UNIT
V_{IK}	I_I = –18 mA		3 V			–1.2	V
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2			V
	I_{OH} = –12 mA		3 V	2.4			
V_{OL}	I_{OL} = 100 µA		MIN to MAX			0.2	V
	I_{OL} = 12 mA		3 V			0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V			±5	µA
I_{CC}	$V_I = V_{CC}$ or GND	I_O = 0	3.6 V				mA
ΔI_{CC}	One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND	3.3 V to 3.6 V			500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V		4		pF
C_o	$V_O = V_{CC}$ or GND		3.3 V		6		pF

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

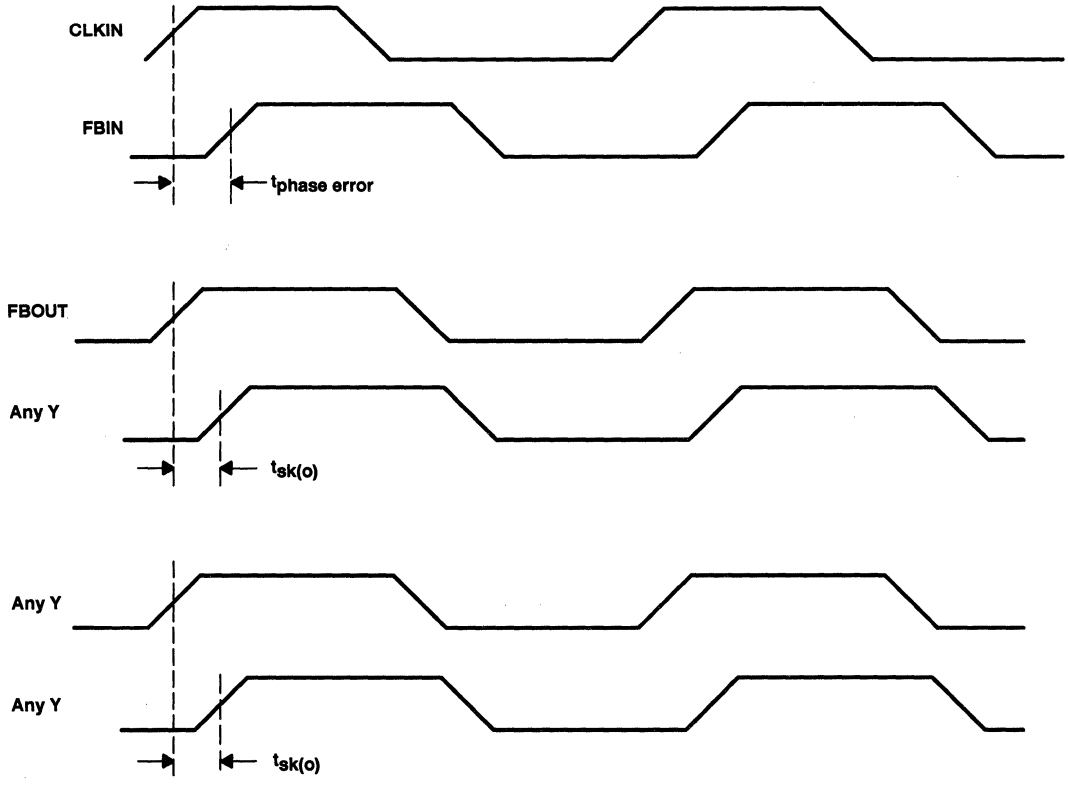
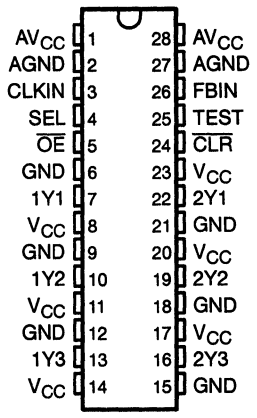


Figure 2. Phase Error and Skew Calculations

- **Low-Output Skew for Clock-Distribution and Clock-Generation Applications**
- **Operates at 3.3-V V_{CC}**
- **Distributes One Clock Input to Six Outputs**
- **One Select Input Configures Three Outputs to Operate at One-Half or Double the Input Frequency**
- **No External RC Network Required**
- **External Feedback Pin (FBIN) Is Used to Synchronize the Outputs to the Clock Input**
- **Application for Synchronous DRAM, High-Speed Microprocessor**
- **Negative-Edge-Triggered Clear for Half-Frequency Outputs**
- **TTL-Compatible Inputs and Outputs**
- **Outputs Drive 50-Ω Parallel-Terminated Transmission Lines**
- **State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **Packaged in Plastic 28-Pin Shrink Small Outline Package**

DL PACKAGE
(TOP VIEW)



description

The CDC536 is a high-performance, low-skew, low-jitter clock driver. It uses a phase-lock loop (PLL) to precisely align, in both frequency and phase, the clock output signals to the clock input (CLKIN) signal. It is specifically designed for use with synchronous DRAMs and popular microprocessors operating at speeds from 50 MHz to 100 MHz or down to 25 MHz on outputs configured as half-frequency outputs. The CDC536 operates at 3.3-V V_{CC} and is designed to drive a properly terminated 50-Ω transmission line.

The feedback input (FBIN) is used to synchronize the output clocks in frequency and phase to the input clock (CLKIN). One of the six output clocks must be fed back to FBIN for the PLL to maintain synchronization between CLKIN and the outputs. The output used as the feedback pin is synchronized to the same frequency as CLKIN.

The Y outputs can be configured to switch in phase and at the same frequency as CLKIN. The select (SEL) input configures three Y outputs to operate at one-half or double the CLKIN frequency depending on which pin is fed back to FBIN (see Tables 1 and 2). All output signal duty cycles are adjusted to 50% independent of the duty cycle at the input clock.

Output-enable ($\overline{OE}$) is provided for output control. When $\overline{OE}$ is high, the outputs are in the high-impedance state. When $\overline{OE}$ is low, the outputs are active. $\overline{CLR}$ is negative-edge triggered and can be used to reset the outputs operating at half frequency. TEST is used for factory testing of the device and can be use to bypass the PLL. TEST should be strapped to GND for normal operation.

Unlike many products containing PLLs, the CDC536 does not require external RC networks. The loop filter for the PLL is included on chip, minimizing component count, board space, and cost.

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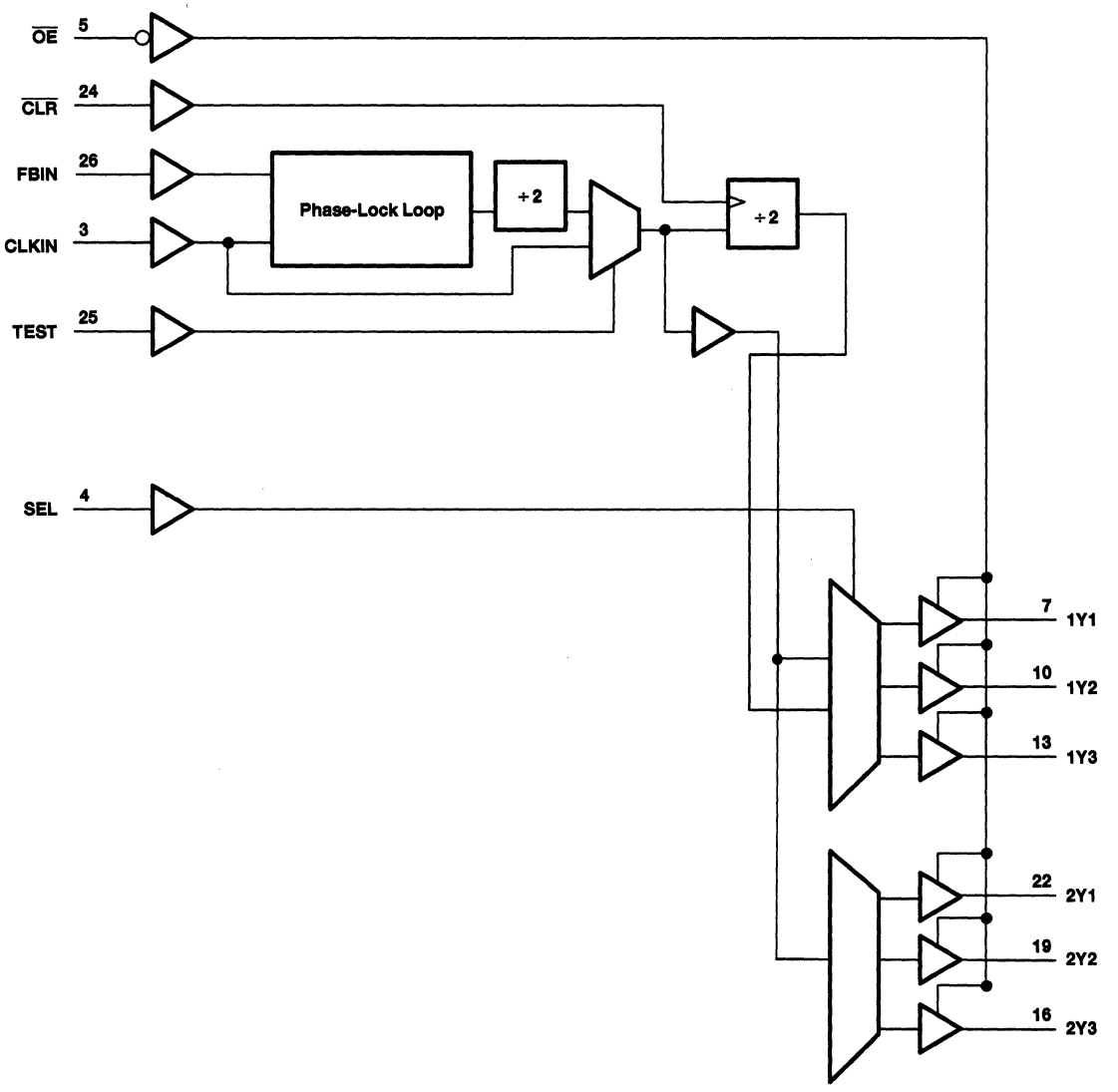
functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) ..... −0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −20 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) ..... 0.7 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		32	mA
T_A	Operating free-air temperature	0	70	°C

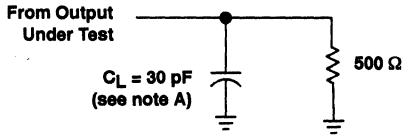
NOTE 3: Unused inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

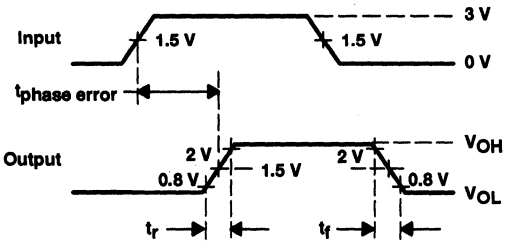
PARAMETER	TEST CONDITIONS			T_A = 25°C MIN	T_A = 25°C MAX	UNIT
V_{IK}	V_{CC} = 3 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA		V_{CC}−0.2		V
	V_{CC} = 3 V,	I_{OH} = −32 mA		2		
V_{OL}	V_{CC} = 3 V,	I_{OL} = 100 µA			0.2	V
	V_{CC} = 3 V,	I_{OL} = 32 mA			0.5	
I_I	V_{CC} = 0 or MAX‡,	V_I = 3.6 V			±10	µA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1	
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			10	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0			−10	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		2	mA
			Outputs low		2	
			Outputs disabled		2	
C_i	V_I = V_{CC} or GND				6	pF
C_o	V_O = V_{CC} or GND				9	pF

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS

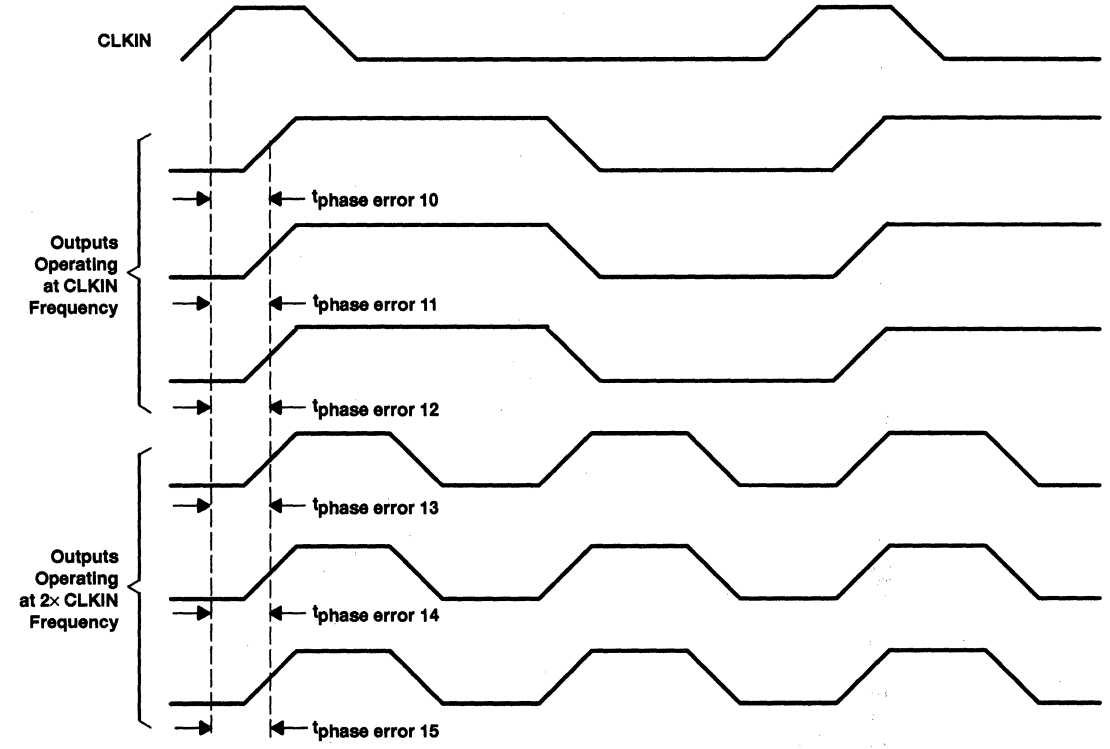


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 100 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



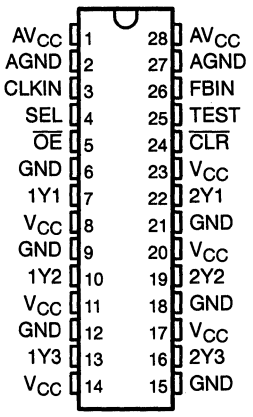
NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 10, 11, . . . 15)

B. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
- The difference between the maximum and minimum $t_{phase\ error\ n}$ (n = 10, 11, . . . 15) across multiple devices under identical operating conditions.

Figure 3. Waveforms for Calculation of $t_{sk(o)}$ and $t_{sk(pr)}$

- **Low Output Skew for Clock-Distribution and Clock-Generation Applications**
- **Operates at 3.3-V V_{CC}**
- **Distributes One Clock Input to Six Outputs**
- **One Select Input Configures Three Outputs to Operate at One-Half or Double the Input Frequency**
- **No External RC Network Required**
- **On-Chip Series Damping Resistors**
- **External Feedback Pin (FBIN) Is Used to Synchronize the Outputs to the Clock Input**
- **Application for Synchronous DRAM, High-Speed Microprocessor**
- **TTL-Compatible Inputs and Outputs**
- **Outputs Drive 50-Ω Parallel-Terminated Transmission Lines**
- **State-of-the-Art *EPIC*-IIB™ BICMOS Design Significantly Reduces Power Dissipation**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **Packaged in Plastic 28-Pin Shrink Small-Outline Package**

DL PACKAGE
(TOP VIEW)



description

The CDC2536 is a high-performance, low-skew, low-jitter clock driver. It uses a phase-lock loop (PLL) to precisely align, in both frequency and phase, the clock output signals to the clock input (CLKIN) signal. It is specifically designed for use with syncronous DRAMs and popular microprocessors operating at speeds from 50 MHz to 100 MHz or down to 25 MHz on outputs configured as half-frequency outputs. The CDC2536 operates at 3.3-V V_{CC} and is designed to drive a properly terminated 50-Ω transmission line. The CDC2536 also provides on-chip series-damping resistors, eliminating the need for external termination components.

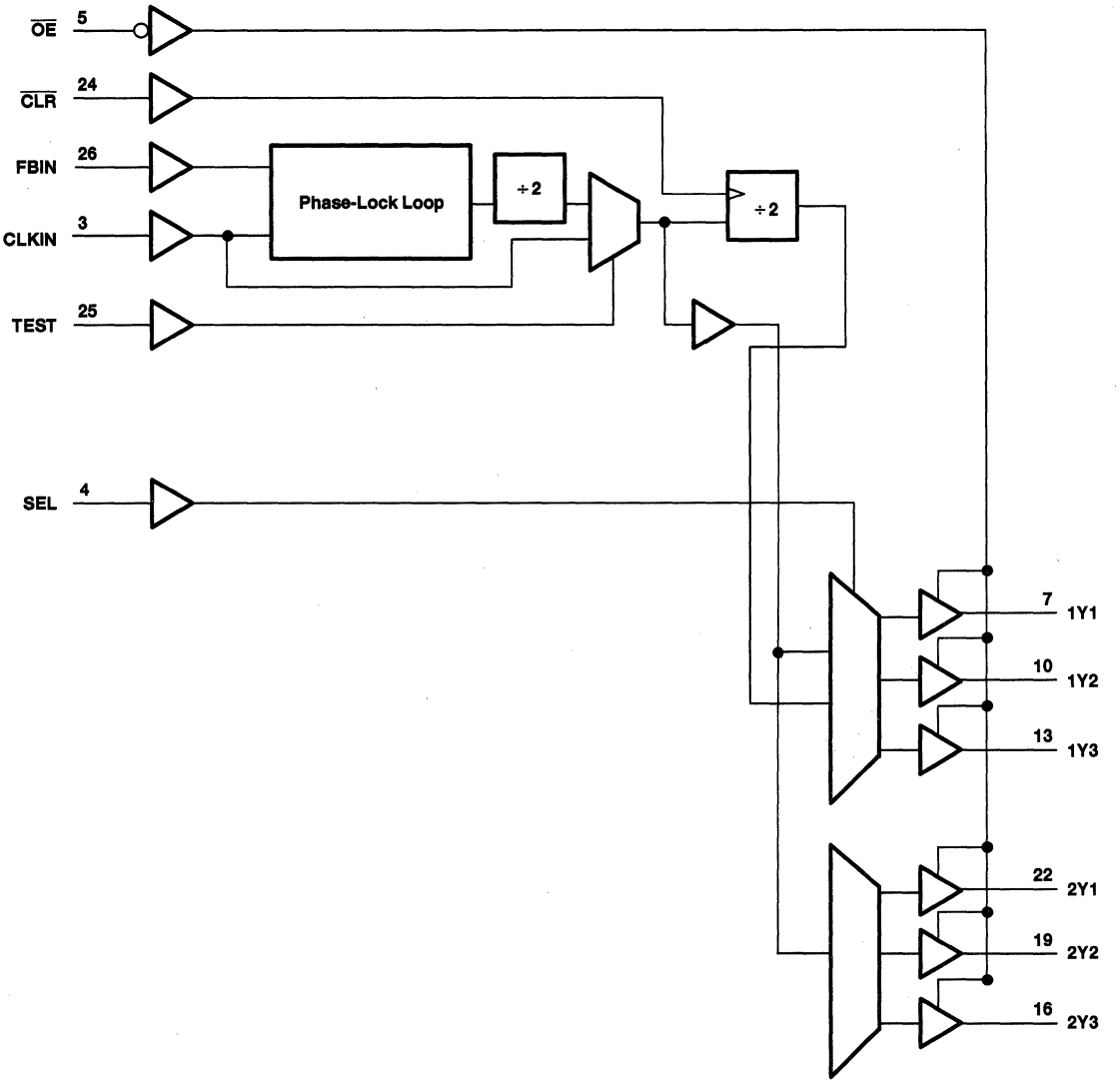
The feedback (FBIN) input is used to synchronize the output clocks in frequency and phase to the input clock (CLKIN). One of the six output clocks must be fed back to FBIN for the PLL to maintain synchronization between CLKIN and the outputs. The output used as the feedback pin is synchronized to the same frequency as CLKIN.

The Y outputs can be configured to switch in phase and at the same frequency as CLKIN. The select (SEL) input configures three Y outputs to operate at one-half or double the CLKIN frequency depending on which pin is fed back to FBIN (see Tables 1 and 2). All output signal duty cycles are adjusted to 50% independent of the duty cycle at the input clock.

Output-enable ($\overline{OE}$) is provided for output control. When $\overline{OE}$ is high, the outputs are in the high-impedance state. When $\overline{OE}$ is low, the outputs are active. $\overline{CLR}$ is negative-edge triggered and can be used to reset the outputs operating at half frequency. TEST is used for factory testing of the device and can be use to bypass the PLL. TEST should be strapped to GND for normal operation.

EPIC-IIB is a trademark of Texas Instruments Incorporated.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) ... −0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 24 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −20 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) ..... 0.7 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
I_{OH}	High-level output current		−12	mA
I_{OL}	Low-level output current		12	mA
T_A	Operating free-air temperature	0	70	°C

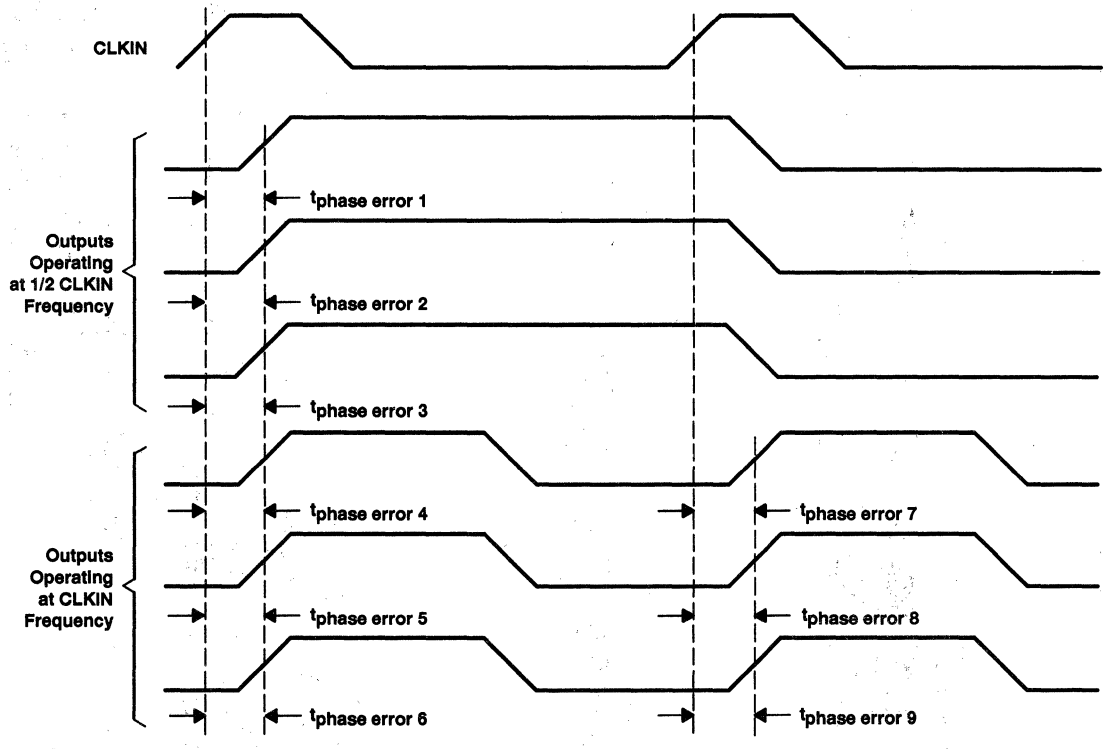
NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C MIN	T_A = 25°C MAX	UNIT
V_{IK}	V_{CC} = 3 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA		V_{CC}−0.2		V
	V_{CC} = 3 V,	I_{OH} = −12 mA		2		
V_{OL}	V_{CC} = 3 V,	I_{OL} = 100 µA			0.2	V
	V_{CC} = 3 V,	I_{OL} = 12 mA			0.8	
I_I	V_{CC} = 0 or MAX‡,	V_I = 3.6 V			±10	µA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1	
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V			10	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0			−10	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		2	mA
			Outputs low		2	
			Outputs disabled		2	
C_i	V_I = V_{CC} or GND				6	pF
C_o	V_O = V_{CC} or GND				9	pF

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION



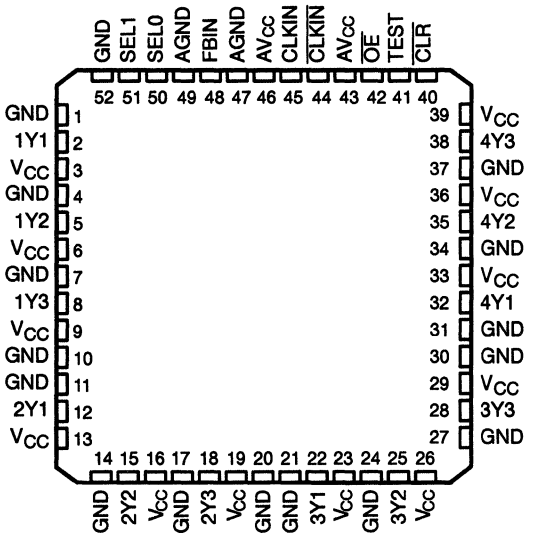
NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 1, 2, . . . 6)
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 7, 8, 9)

B. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
- The difference between the maximum and minimum $t_{phase\ error\ n}$ (n = 1, 2, . . . 6) across multiple devices under identical operating conditions
- The difference between the maximum and minimum $t_{phase\ error\ n}$ (n = 7, 8, 9) across multiple devices under identical operating conditions

Figure 2. Waveforms for Calculations of $t_{sk(o)}$ and $t_{sk(pr)}$

- Low Output Skew for Clock-Distribution and Clock-Generation Applications
- Operates at 3.3-V V_{CC}
- Distributes Differential LVPECL Clock Inputs to 12 TTL-Compatible Outputs
- Two Select Inputs Configure Up to Nine Outputs to Operate at One-Half or Double the Input Frequency
- No External RC Network Required
- State-of-the-Art *EPIC*-IIB™ BICMOS Design Significantly Reduces Power Dissipation
- External Feedback Input (FBIN) Is Used to Synchronize the Outputs With the Clock Inputs
- Application for Synchronous DRAMs
- Distributed V_{CC} and Ground Pins Reduce Switching Noise
- Packaged in 52-Pin Quad Flatpack

PAH PACKAGE
(TOP VIEW)



description

The CDC582 is a high-performance, low-skew, low-jitter clock driver. It uses a phase-lock loop (PLL) to precisely align the frequency and phase of the clock output signals to the differential LVPECL clock (CLKIN, $\overline{\text{CLKIN}}$) input signals. It is specifically designed to operate at speeds from 50 MHz to 100 MHz or down to 25 MHz on outputs configured as half-frequency outputs. The CDC582 operates at 3.3-V V_{CC}.

The feedback input (FBIN) synchronizes the frequency of the output clocks with the input clock (CLKIN, $\overline{\text{CLKIN}}$) signals. One of the twelve output clocks must be fed back to FBIN for the PLL to maintain synchronization between the differential CLKIN and $\overline{\text{CLKIN}}$ inputs and the outputs. The output used as feedback is synchronized to the same frequency as the clock (CLKIN and $\overline{\text{CLKIN}}$) inputs.

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output configuration B

Output configuration B is valid when any output configured as a 1× frequency output in Table 2 is fed back to FBIN. The frequency range for the differential clock inputs is 25 MHz to 50 MHz when using output configuration B. Outputs configured as 1× outputs operate at the input clock frequency, while outputs configured as 2× outputs operate at double the frequency of the differential clock inputs.

Table 2. Output Configuration B

INPUTS		OUTPUTS	
SEL1	SEL0	1× FREQUENCY	2× FREQUENCY
L	L	All	None
L	H	1Yn	2Yn, 3Yn, 4Yn
H	L	1Yn, 2Yn	3Yn, 4Yn
H	H	1Yn, 2Yn, 3Yn	4Yn

NOTE: n = 1, 2, 3

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLKIN $\overline{\text{CLKIN}}$	44, 45	I	Clock input. CLKIN and $\overline{\text{CLKIN}}$ are the differential clock signals to be distributed by the CDC582 clock-driver circuit. These inputs are used to provide the reference signal to the integrated PLL that generates the clock output signals. CLKIN and $\overline{\text{CLKIN}}$ must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and valid CLKIN and $\overline{\text{CLKIN}}$ signals are applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
$\overline{\text{CLR}}$	40	I	Clear. $\overline{\text{CLR}}$ is used to reset the VCO/4 reference frequency. $\overline{\text{CLR}}$ is negative-edge triggered and should be strapped to V_{CC} or GND for normal operation.
FBIN	48	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hardwired to one of the twelve clock outputs to provide frequency and phase lock. The internal PLL adjusts the output clocks to obtain zero phase delay between the FBIN and the differential clock input (CLKIN and $\overline{\text{CLKIN}}$).
$\overline{\text{OE}}$	42	I	Output enable. $\overline{\text{OE}}$ is the output enable for all outputs. When $\overline{\text{OE}}$ is low, all outputs are enabled. When $\overline{\text{OE}}$ is high, all outputs are driven to the low state. Since the feedback signal for the PLL is taken directly from an output terminal, placing the outputs in the logic low state interrupts the feedback loop; therefore, when a high-to-low transition occurs at $\overline{\text{OE}}$, enabling the output buffers, a stabilization time is required before the PLL obtains phase lock.
SEL1, SEL0	51, 50	I	Output configuration select. SEL0 and SEL1 select the output configuration for each output bank (e.g., 1×, 1/2×, or 2×) (see Tables 1 and 2).
TEST	41	I	TEST is used to bypass the PLL circuitry for factory testing of the device. When TEST is low, all outputs operate using the PLL circuitry. When TEST is high, the outputs are placed in a test mode that bypasses the PLL circuitry. TEST should be strapped to GND for normal operation.
1Y1–1Y3 2Y1–2Y3 3Y1–3Y3	2, 5, 8 12, 15, 18 22, 25, 28	O	These outputs are configured by SEL1 and SEL0 to transmit one-half or one-fourth the frequency of the VCO. The relationship between the input clock frequency and the output frequency is dependent on SEL1 and SEL0 and the frequency of the output being fed back to FBIN. The duty cycle of the Y outputs is nominally 50% independent of the duty cycle of the input clock signals.
4Y1–4Y3	32, 35, 38	O	These outputs transmit one-half the frequency of the VCO. The relationship between the input clock frequency and the output frequency is dependent on the frequency of the output being fed back to FBIN. The duty cycle of the Y outputs is nominally 50% independent of the duty cycle of CLKIN.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) ... −0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −20 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipationat T_A = 55°C (in still air) (see Note 2) ..... 1.2 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency	VCO is operating at four times the CLKIN/$\overline{\text{CLKIN}}$ frequency	25	50	MHz
		VCO is operating at double the CLKIN/$\overline{\text{CLKIN}}$ frequency	50	100	
	Input clock duty cycle		40%	60%	
	Stabilization time†	After SEL1, SEL0		50	µs
		After $\overline{\text{OE}}\downarrow$		50	
		After power up		50	

† Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLKIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

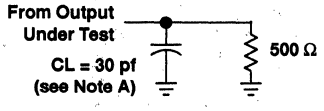
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 15 pF (see Note 4 and Figures 1, 2, and 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
Duty cycle		Y	45%	55%	
f_{max}			100		MHz
$Jitter_{(pk-pk)}$	CLKIN↑	Y↑		200	ps
$t_{phase\ error}$‡	CLKIN↑	Y↑	–500	500	ps
$t_{sk(o)}$‡		Y		0.5	ns
$t_{sk(pr)}$‡		Y		1	ns
t_r				1.4	ns
t_f				1.4	ns

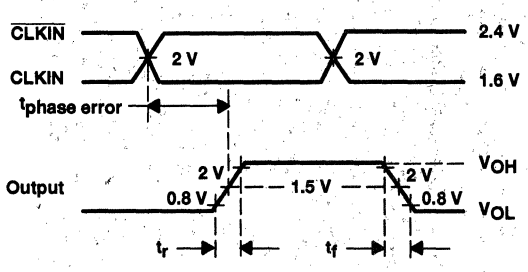
‡ The propagation delay, $t_{phase\ error}$, is dependent on the feedback path from any output to the FBIN. The $t_{phase\ error}$, $t_{sk(o)}$, and $t_{sk(pr)}$ specifications are only valid for equal loading of all outputs.

NOTE 4: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS

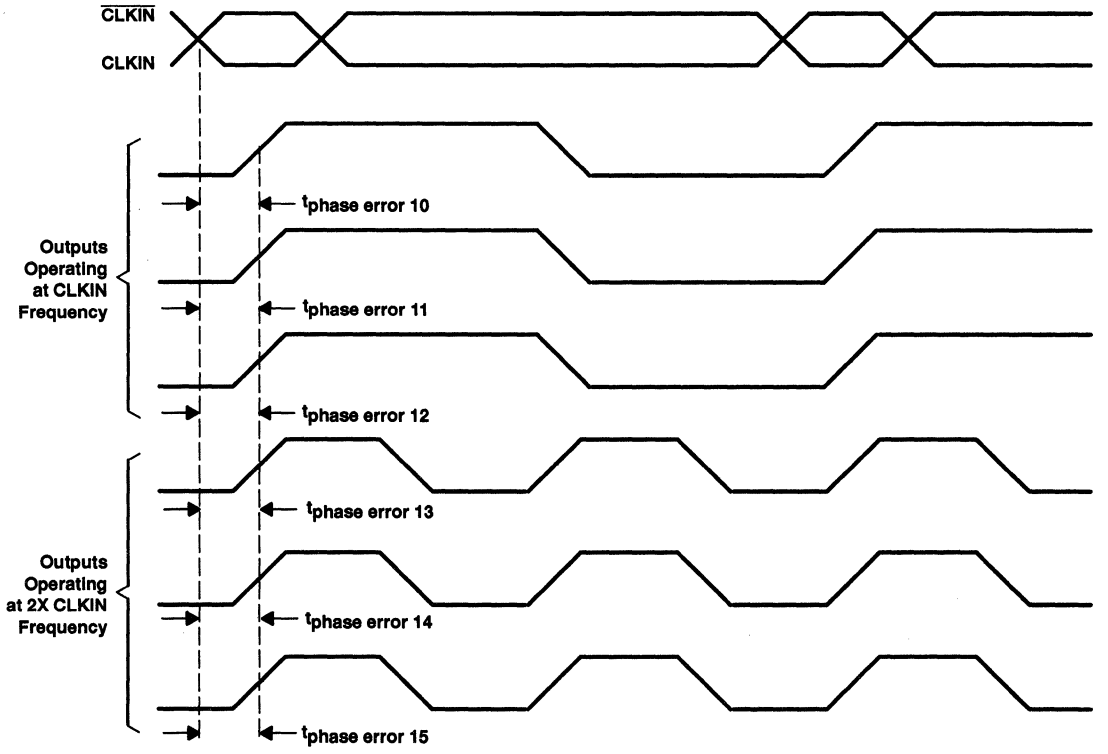


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. The outputs are measured one at a time with one transition per measurement.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



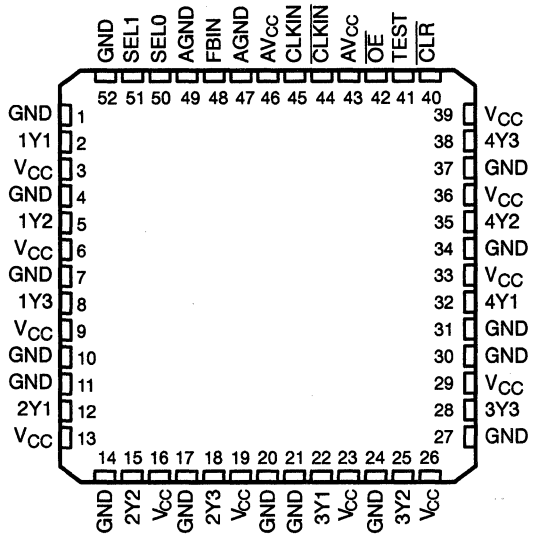
NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 10, 11, . . . 15)

B. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
- The difference between the maximum and minimum $t_{phase\ error\ n}$ (n = 10, 11, . . . 15) across multiple devices under identical operating conditions

Figure 3. Waveforms for Calculation of $t_{sk(o)}$

- **Low Output Skew for Clock-Distribution and Clock-Generation Applications**
- **Operates at 3.3-V V_{CC}**
- **Distributes Differential LVPECL Clock Inputs to 12 TTL-Compatible Outputs**
- **Two Select Inputs Configure Up to Nine Outputs to Operate at One-Half or Double the Input Frequency**
- **No External RC Network Required**
- **External Feedback Input (FBIN) Is Used to Synchronize the Outputs With the Clock Inputs**
- **Application for Synchronous DRAMs**
- **Outputs Have Internal 26-Ω Series Resistors to Dampen Transmission-Line Effects**
- **State-of-the-Art *EPIC*-IIB™ BICMOS Design Significantly Reduces Power Dissipation**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **Packaged in 52-Pin Quad Flatpack**

PAH PACKAGE
(TOP VIEW)



description

The CDC2582 is a high-performance, low-skew, low-jitter clock driver. It uses a phase-lock loop (PLL) to precisely align the frequency and phase of the clock output signals to the differential LVPECL clock (CLKIN, $\overline{\text{CLKIN}}$) input signals. It is specifically designed to operate at speeds from 50 MHz to 100 MHz or down to 25 MHz on outputs configured as half-frequency outputs. Each output has an internal 26-Ω series resistor that improves the signal integrity at the load. The CDC2582 operates at 3.3-V V_{CC}.

The feedback input (FBIN) synchronizes the frequency of the output clocks with the input clock (CLKIN, $\overline{\text{CLKIN}}$) signals. One of the twelve output clocks must be fed back to FBIN for the PLL to maintain synchronization between the differential CLKIN and $\overline{\text{CLKIN}}$ inputs and the outputs. The output used as feedback is synchronized to the same frequency as the clock (CLKIN and $\overline{\text{CLKIN}}$) inputs.

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output configuration B

Output configuration B is valid when any output configured as a 1× frequency output in Table 2 is fed back to FBIN. The frequency range for the differential clock inputs is 25 MHz to 50 MHz when using output configuration B. Outputs configured as 1× outputs operate at the input clock frequency, while outputs configured as 2× outputs operate at double the frequency of the differential clock inputs.

Table 2. Output Configuration B

INPUTS		OUTPUTS	
SEL1	SEL0	1× FREQUENCY	2× FREQUENCY
L	L	All	None
L	H	1Yn	2Yn, 3Yn, 4Yn
H	L	1Yn, 2Yn	3Yn, 4Yn
H	H	1Yn, 2Yn, 3Yn	4Yn

NOTE: n = 1, 2, 3

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLKIN $\overline{\text{CLKIN}}$	44, 45	I	Clock input. CLKIN and $\overline{\text{CLKIN}}$ are the differential clock signals to be distributed by the CDC2582 clock-driver circuit. These inputs are used to provide the reference signal to the integrated PLL that generates the clock-output signals. CLKIN and $\overline{\text{CLKIN}}$ must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and valid CLKIN and $\overline{\text{CLKIN}}$ signals are applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
$\overline{\text{CLR}}$	40	I	Clear. $\overline{\text{CLR}}$ is used to reset the VCO/4 reference frequency. $\overline{\text{CLR}}$ is negative-edge triggered and should be strapped to V_{CC} or GND for normal operation.
FBIN	48	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hardwired to one of the twelve clock outputs to provide frequency and phase lock. The internal PLL adjusts the output clocks to obtain zero-phase delay between the FBIN and the differential clock input (CLKIN and $\overline{\text{CLKIN}}$).
$\overline{\text{OE}}$	42	I	Output enable. $\overline{\text{OE}}$ is the output enable for all outputs. When $\overline{\text{OE}}$ is low, all outputs are enabled. When $\overline{\text{OE}}$ is high, all outputs are in the high-impedance state. Since the feedback signal for the PLL is taken directly from an output terminal, placing the outputs in the high-impedance state interrupts the feedback loop; therefore, when a high-to-low transition occurs at $\overline{\text{OE}}$, enabling the output buffers, a stabilization time is required before the PLL obtains phase lock.
SEL1, SEL0	51, 50	I	Output configuration select. SEL0 and SEL1 select the output configuration for each output bank (e.g., 1×, 1/2×, or 2×) (see Tables 1 and 2).
TEST	41	I	TEST is used to bypass the PLL circuitry for factory testing of the device. When TEST is low, all outputs operate using the PLL circuitry. When TEST is high, the outputs are placed in a test mode that bypasses the PLL circuitry. TEST should be strapped to GND for normal operation.
1Y1–1Y3 2Y1–2Y3 3Y1–3Y3	2, 5, 8 12, 15, 18 22, 25, 28	O	These outputs are configured by SEL1 and SEL0 to transmit one-half or one-fourth the frequency of the VCO. The relationship between the input clock frequency and the output frequency is dependent on SEL1 and SEL0 and the frequency of the output being fed back to FBIN. The duty cycle of the Y outputs is nominally 50% independent of the duty cycle of the input clock signals. Each output has an internal series resistor to dampen transmission-line effects and improve the signal integrity at the load.
4Y1–4Y3	32, 35, 38	O	These outputs transmit one-half the frequency of the VCO. The relationship between the input clock frequency and the output frequency is dependent on the frequency of the output being fed back to FBIN. The duty cycle of the Y outputs is nominally 50% independent of the duty cycle of CLKIN. Each output has an internal series resistor to dampen transmission-line effects and improve the signal integrity at the load.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) ... –0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 24 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) ..... 1.2 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency	VCO is operating at four times the CLKIN/$\overline{\text{CLKIN}}$ frequency	25	50	MHz
		VCO is operating at double the CLKIN/$\overline{\text{CLKIN}}$ frequency	50	100	
	Input clock duty cycle		40%	60%	
	Stabilization time†	After SEL1, SEL0		50	µs
		After $\overline{\text{OE}}\downarrow$		50	
		After power up		50	

† Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLKIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

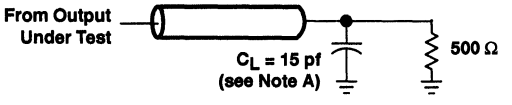
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 15 pF (see Note 4 and Figures 1, 2, and 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
Duty cycle		Y	45%	55%	
f_{max}			100		MHz
$Jitter_{(pk-pk)}$	CLKIN↑	Y↑		200	ps
$t_{phase\ error}$‡	CLKIN↑	Y	–500	500	ps
$t_{sk(o)}$‡		Y		0.5	ns
$t_{sk(pr)}$‡		Y		1	ns
t_r				1.4	ns
t_f				1.4	ns

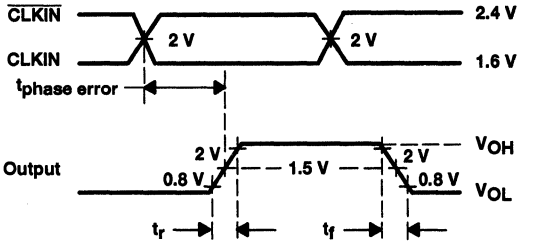
‡ The propagation delay, $t_{phase\ error}$, is dependent on the feedback path from any output to FBIN. The $t_{phase\ error}$, $t_{sk(o)}$, and $t_{sk(pr)}$ specifications are only valid for equal loading of all outputs.

NOTE 4: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS

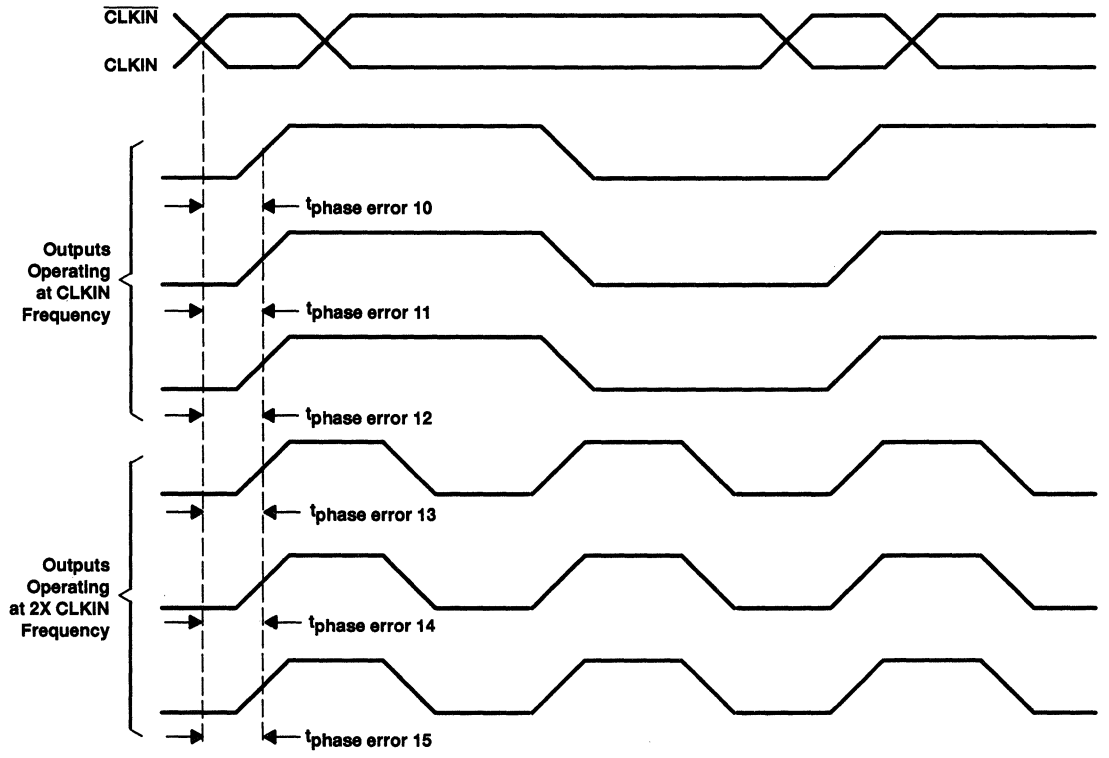


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. The outputs are measured one at a time with one transition per measurement.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



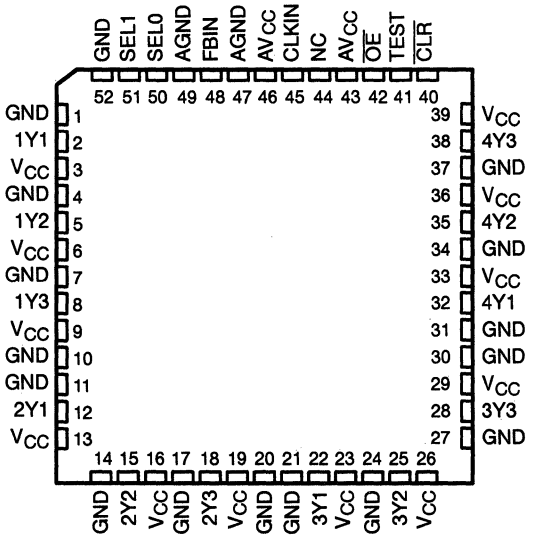
NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 10, 11, . . . 15)

B. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
- The difference between the maximum and minimum $t_{phase\ error\ n}$ (n = 10, 11, . . . 15) across multiple devices under identical operating conditions

Figure 3. Waveforms for Calculation of $t_{sk(o)}$ and $t_{sk(pr)}$

- Low Output Skew for Clock-Distribution and Clock-Generation Applications
- Operates at 3.3-V V_{CC}
- Distributes One Clock Input to Twelve Outputs
- Two Select Inputs Configure Up to Nine Outputs to Operate at One-Half or Double the Input Frequency
- No External RC Network Required
- External Feedback Pin (FBIN) Is Used to Synchronize the Outputs to the Clock Input
- Application for Synchronous DRAM, High-Speed Microprocessor
- TTL-Compatible Inputs and Outputs
- Outputs Drive Parallel 50-Ω Terminated Transmission Lines
- State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- Distributed V_{CC} and Ground Pins Reduce Switching Noise
- Packaged in 52-Pin Thin Quad Flat Package

PAH PACKAGE
(TOP VIEW)



NC – No internal connection

description

The CDC586 is a high-performance, low-skew, low-jitter clock driver. It uses a phase-lock loop (PLL) to precisely align, in both frequency and phase, the clock output signals to the clock input (CLKIN) signal. It is specifically designed for use with popular microprocessors operating at speeds from 50 MHz to 100 MHz or down to 25 MHz on outputs configured as half-frequency outputs. The CDC586 operates at 3.3-V V_{CC} and is designed to drive a properly terminated 50-Ω transmission line.

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output configuration A

Output configuration A is valid when any output configured as a 1x frequency output in Table 1 is fed back to FBIN. The input frequency range for CLKIN is 50 MHz to 100 MHz when using output configuration A. Outputs configured as 1/2x outputs operate at half the CLKIN frequency, while outputs configured as 1x outputs operate at the same frequency as CLKIN.

Table 1. Output Configuration A

INPUTS		OUTPUTS	
SEL1	SEL0	1/2x FREQUENCY	1x FREQUENCY
L	L	None	All
L	H	1Yn	2Yn, 3Yn, 4Yn
H	L	1Yn, 2Yn	3Yn, 4Yn
H	H	1Yn, 2Yn, 3Yn	4Yn

NOTE: n = 1, 2, 3

output configuration B

Output configuration B is valid when any output configured as a 1x frequency output in Table 2 is fed back to FBIN. The input frequency range for CLKIN is 25 MHz to 50 MHz when using output configuration B. Outputs configured as 1x outputs operate at the CLKIN frequency, while outputs configured as 2x outputs operate at double the frequency of CLKIN.

Table 2. Output Configuration B

INPUTS		OUTPUTS	
SEL1	SEL0	1x FREQUENCY	2x FREQUENCY
L	L	All	None
L	H	1Yn	2Yn, 3Yn, 4Yn
H	L	1Yn, 2Yn	3Yn, 4Yn
H	H	1Yn, 2Yn, 3Yn	4Yn

NOTE: n = 1, 2, 3

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLKIN	45	I	Clock input. CLKIN is the clock signal distributed by the CDC586 clock-driver circuit. CLKIN provides the reference signal to the integrated PLL that generates the clock output signals. CLKIN must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLKIN signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
$\overline{CLR}$	40	I	Clear. $\overline{CLR}$ resets the VCO/4 reference frequency. $\overline{CLR}$ is negative edge triggered and should be strapped to GND or V_{CC} for normal operation.
FBIN	48	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hardwired to one of the twelve clock outputs to provide frequency and phase lock. The internal PLL adjusts the output clocks to obtain zero phase delay between FBIN and CLKIN.
$\overline{OE}$	42	I	Output enable. $\overline{OE}$ is the output enable for all outputs. When $\overline{OE}$ is low, all outputs are enabled. When $\overline{OE}$ is high, all outputs are in the high-impedance state. Since the feedback signal for the PLL is taken directly from an output terminal, placing the outputs in the high-impedance state interrupts the feedback loop; therefore, when a high-to-low transition occurs at $\overline{OE}$, enabling the output buffers, a stabilization time is required before the PLL obtains phase lock.
SEL1, SEL0	51, 50	I	Output configuration select. SEL0 and SEL1 select the output configuration for each output bank (e.g. 1×, 1/2×, or 2×). (see Tables 1 and 2).
TEST	41	I	TEST is used to bypass the PLL circuitry for factory testing of the device. When TEST is low, all outputs operate using the PLL circuitry. When TEST is high, the outputs are placed in a test mode that bypasses the PLL circuitry. TEST should be strapped to GND for normal operation.
1Y1–1Y3 2Y1–2Y3 3Y1–3Y3	2, 5, 8 12, 15, 18 22, 25, 28	O	Output ports. These outputs are configured by SEL1 and SEL0 to transmit one-half or one-fourth the frequency of the VCO. The relationship between the CLKIN frequency and the output frequency is dependent on SEL1 and SEL0 and the frequency of the output being fed back to FBIN. The duty cycle of the Y output signals is nominally 50% independent of the duty cycle of CLKIN.
4Y1–4Y3	32, 35, 38	O	Output ports. 4Y1–4Y3 transmit one-half the frequency of the VCO regardless of the state of SEL1 and SEL0. The relationship between the CLKIN frequency and the output frequency is dependent on the frequency of the output being fed back to FBIN. The duty cycle of the Y output signals is nominally 50% independent of the duty cycle of CLKIN.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... –0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state,
V_O (see Note 1) ..... –0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... –20 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... –50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) ..... 1.2 W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency	VCO is operating at four times the CLKIN frequency	25	50	MHz
		VCO is operating at double the CLKIN frequency	50	100	
	Input clock duty cycle		40%	60%	
	Stabilization time†	After SEL1, SEL0		50	µs
		After $\overline{OE}\downarrow$		50	
		After power up		50	
		After CLKIN		50	

† Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLKIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

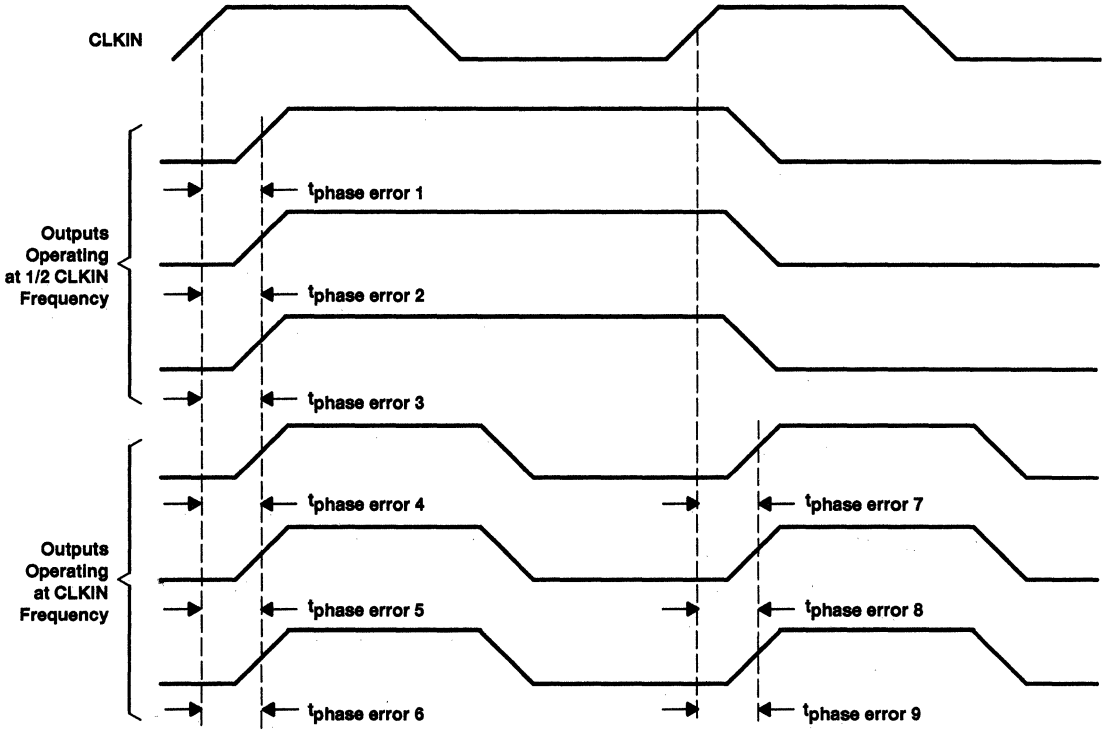
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (see Note 4 and Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}			100		MHz
Duty cycle		Y	45%	55%	
$t_{phase\ error}$‡	CLKIN↑	Y	–500	+500	ps
$Jitter_{(pk\text{-}pk)}$	CLKIN↑	Y		200	ps
$t_{sk(o)}$‡				0.5	ns
$t_{sk(pr)}$‡				1	ns
t_r				1.4	ns
t_f				1.4	ns

‡ The propagation delay, $t_{phase\ error}$, is dependent on the feedback path from any output to FBIN. The $t_{phase\ error}$, $t_{sk(o)}$, and $t_{sk(pr)}$ specifications are valid only for equal loading of all outputs.

NOTE 4: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

PARAMETER MEASUREMENT INFORMATION



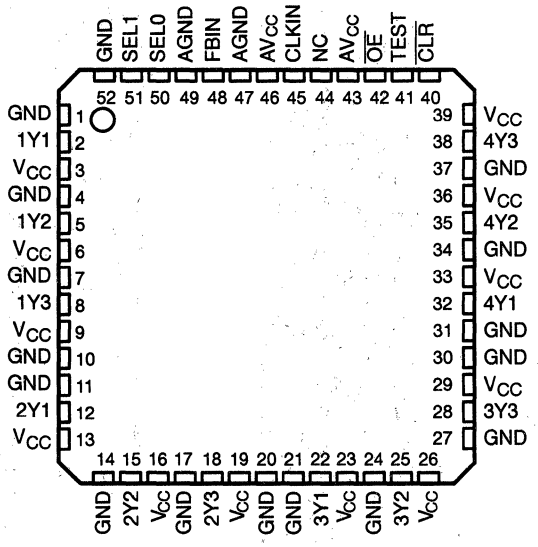
NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 1, 2, . . . 6)
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 7, 8, 9)

B. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
- The difference between the maximum and minimum $t_{phase\ error\ n}$ (n = 1, 2, . . . 6) across multiple devices under identical operating conditions.
- The difference between the maximum and minimum $t_{phase\ error\ n}$ (n = 7, 8, 9) across multiple devices under identical operating conditions.

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

- Low Output Skew for Clock-Distribution and Clock-Generation Applications
- Operates at 3.3-V V_{CC}
- Distributes One Clock Input to Twelve Outputs
- Two Select Inputs Configure Up to Nine Outputs to Operate at One-Half or Double the Input Frequency
- No External RC Network Required
- External Feedback (FBIN) Synchronizes the Outputs to the Clock Input
- Application for Synchronous DRAM, High-Speed Microprocessor
- TTL-Compatible Inputs and Outputs
- Outputs Have Internal 26-Ω Series Resistors to Dampen Transmission-Line Effects
- State-of-the-Art *EPIC*-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- Distributed V_{CC} and Ground Pins Reduce Switching Noise
- Packaged in 52-Pin Thin Quad Flat Package

PAH PACKAGE
(TOP VIEW)



NC – No internal connection

description

The CDC2586 is a high-performance, low-skew, low-jitter clock driver. It uses a phase-lock loop (PLL) to precisely align, in both frequency and phase, the clock output signals to the clock input (CLKIN) signal. It is specifically designed for use with popular microprocessors operating at speeds from 50 MHz to 100 MHz or down to 25 MHz on outputs configured for half-frequency operation. Each output has an internal 26-Ω series resistor that improves the signal integrity at the load. The CDC2586 operates at nominal 3.3-V V_{CC}.

The feedback input (FBIN) synchronizes the output clocks in frequency and phase to CLKIN. One of the twelve output clocks must be fed back to FBIN for the PLL to maintain synchronization between CLKIN and the outputs. The output used as feedback is synchronized to the same frequency as CLKIN.

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output configuration A

Output configuration A is valid when any output configured as a 1 × frequency output in Table 1 is fed back to FBIN. The input frequency range for CLKIN is 50 MHz to 100 MHz when using output configuration A. Outputs configured as 1/2 × outputs operate at half the CLKIN frequency, while outputs configured as 1 × outputs operate at the same frequency as CLKIN.

Table 1. Output Configuration A

INPUTS		OUTPUTS	
SEL1	SEL0	1/2× FREQUENCY	1× FREQUENCY
L	L	None	All
L	H	1Yn	2Yn, 3Yn, 4Yn
H	L	1Yn, 2Yn	3Yn, 4Yn
H	H	1Yn, 2Yn, 3Yn	4Yn

NOTE: n = 1, 2, 3

output configuration B

Output configuration B is valid when any output configured as a 1 × frequency output in Table 2 is fed back to FBIN. The input frequency range for CLKIN is 25 MHz to 50 MHz when using output configuration B. Outputs configured as 1 × outputs operate at the CLKIN frequency, while outputs configured as 2 × outputs operate at double the frequency of CLKIN.

Table 2. Output Configuration B

INPUTS		OUTPUTS	
SEL1	SEL0	1× FREQUENCY	2× FREQUENCY
L	L	All	None
L	H	1Yn	2Yn, 3Yn, 4Yn
H	L	1Yn, 2Yn	3Yn, 4Yn
H	H	1Yn, 2Yn, 3Yn	4Yn

NOTE: n = 1, 2, 3

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLKIN	45	I	Clock input. CLKIN is the clock signal to be distributed by the CDC2586 clock-driver circuit. CLKIN provides the reference signal to the integrated PLL that generates the clock output signals. CLKIN must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLKIN signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
$\overline{CLR}$	40	I	Clear. $\overline{CLR}$ resets the VCO/4 reference frequency. $\overline{CLR}$ is negative-edge triggered and should be strapped to GND or V_{CC} for normal operation.
FBIN	48	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard wired to one of the twelve clock outputs to provide frequency and phase lock. The internal PLL adjusts the output clocks to obtain zero phase delay between FBIN and CLKIN.
$\overline{OE}$	42	I	Output enable. $\overline{OE}$ is the output enable for all outputs. When $\overline{OE}$ is low, all outputs are enabled. When $\overline{OE}$ is high, all outputs are in the high-impedance state. Since the feedback signal for the PLL is taken directly from an output, placing the outputs in the high-impedance state interrupts the feedback loop; therefore, when a high-to-low transition occurs at $\overline{OE}$, enabling the output buffers, a stabilization time is required before the PLL obtains phase lock.
SEL1, SEL0	51, 50	I	Output configuration select. SEL0 and SEL1 select the output configuration for each output bank (e.g., 1/2×, 1×, or 2×) (see Tables 1 and 2).
TEST	41	I	TEST is used to bypass the PLL circuitry for factory testing of the device. When TEST is low, all outputs operate using the PLL circuitry. When TEST is high, the outputs are placed in a test mode that bypasses the PLL circuitry. TEST should be strapped to GND for normal operation.
1Y1–1Y3 2Y1–2Y3 3Y1–3Y3	2, 5, 8 12, 15, 18 22, 25, 28	O	Output ports. These outputs are configured by the select inputs (SEL1, SEL0) to transmit one-half or one-fourth the frequency of the VCO. The relationship between the CLKIN frequency and the output frequency is dependent on the select inputs and the frequency of the output being fed back to FBIN (see Tables 1 and 2). The duty cycle of the Y output signals is nominally 50%, independent of the duty cycle of CLKIN. Each output has an internal series resistor to dampen transmission-line effects and improve the signal integrity at the load.
4Y1–4Y3	32, 35, 38	O	Output ports. 4Y1–4Y3 transmit one-half the frequency of the VCO regardless of the state of the select inputs. The relationship between the CLKIN frequency and the output frequency is dependent on the frequency of the output being fed back to FBIN (see Tables 1 and 2). The duty cycle of the Y output signals is nominally 50%, independent of the duty cycle of CLKIN. Each output has an internal series resistor to dampen transmission-line effects and improve the signal integrity at the load.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) ... −0.5 V to 5.5 V
Current into any output in the low state, I_O ..... 24 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −20 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) ..... 1.2 W
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 75 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

			MIN	MAX	UNIT
f_{clock}	Clock frequency	VCO operating at four times the CLKIN frequency	25	50	MHz
		VCO operating at double the CLKIN frequency	50	100	
	Input clock duty cycle		40%	60%	
	Stabilization time†	After SEL1, SEL0		50	µs
		After $\overline{OE}\downarrow$		50	
		After power up		50	
		After CLKIN		50	

† Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLKIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

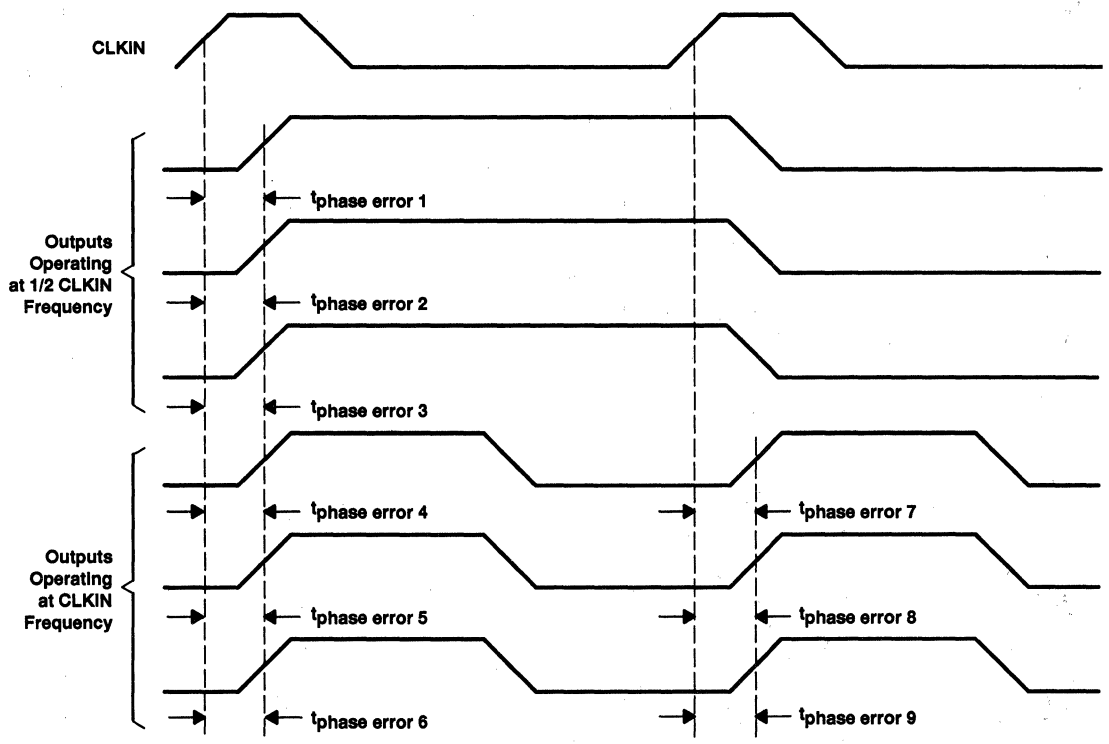
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 15 pF (see Note 4 and Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}			100		MHz
Duty cycle		Y	45%	55%	
$t_{phase\ error}$‡	CLKIN↑	Y↑	−500	+500	ps
jitter	CLKIN↑	Y↑		200	ps
$t_{sk(o)}$‡				0.5	ns
$t_{sk(pr)}$‡				1	ns
t_r				1.4	ns
t_f				1.4	ns

‡ The propagation delay, $t_{phase\ error}$, is dependent on the feedback path from any output to FBIN. The $t_{phase\ error}$, $t_{sk(o)}$, and $t_{sk(pr)}$ specifications are valid only for equal loading of all outputs.

NOTE 4: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 1, 2, . . . 6)
- The difference between the fastest and slowest of $t_{phase\ error\ n}$ (n = 7, 8, 9)

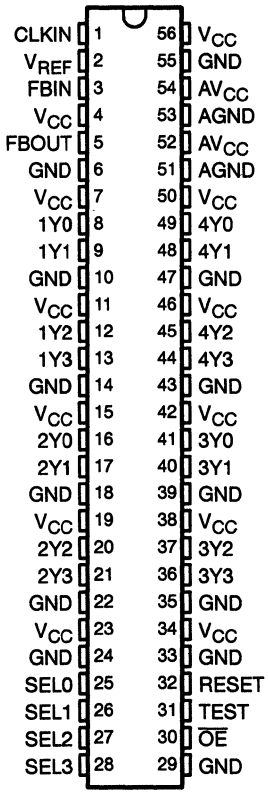
B. Process skew, $t_{sk(pr)}$, is calculated as the greater of:
- The difference between the maximum and minimum $t_{phase\ error\ n}$ (n = 1, 2, . . . 6) across multiple devices under identical operating conditions
- The difference between the maximum and minimum $t_{phase\ error\ n}$ (n = 7, 8, 9) across multiple devices under identical operating conditions

C. For configuration A, see Table 1

Figure 2. Waveforms for Calculation of $t_{sk(o)}$ for Configuration A

- **Low-Output Skew and Jitter for Clock Distribution and Synchronization**
- **Operates at 3.3-V V_{CC}**
- **Distributes One Clock Input to 16 Outputs**
- **Four Select Inputs Configure Output Frequency**
- **Internal Loop Filter Eliminates the Need for External RC Network**
- **Dedicated External Feedback Output and Input for Phase Synchronization With the Clock Input**
- **Applications for Synchronous DRAM, High-Speed Microprocessors, and SSTL_3 Applications**
- **LVTTL- or SSTL_3-Compatible Inputs and Outputs**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **Meets SSTL_3 Class 1 and 2 Specifications**
- **Packaged in Plastic Small-Outline Package**

DGG PACKAGE
(TOP VIEW)



description

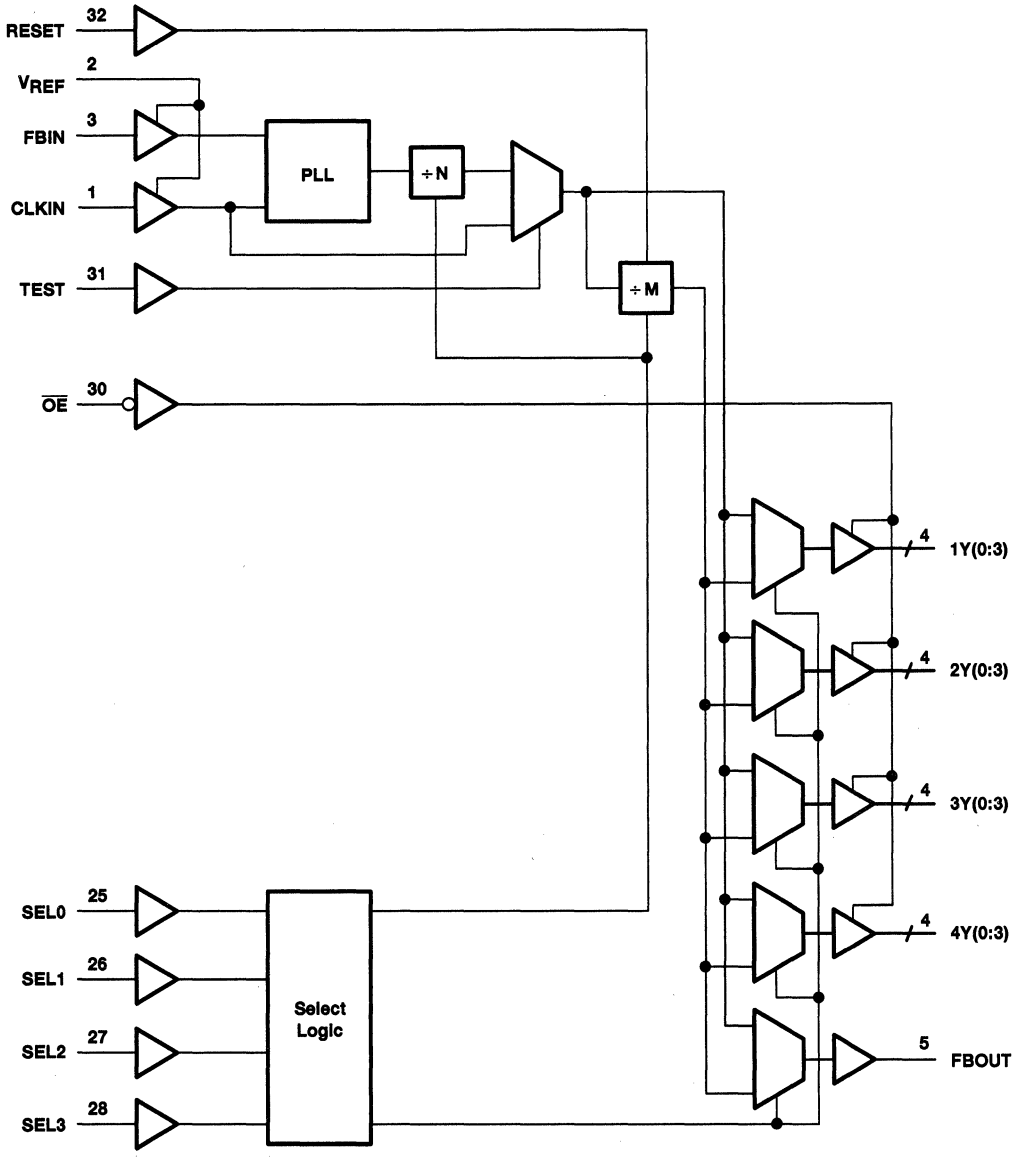
The CDC587 is a high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the clock output signals to the clock input (CLKIN) signal. The CDC587 operates at 3.3-V V_{CC} and provides LVTTL- or SSTL_3-compatible inputs and outputs. The CDC587 operates at frequencies from 16.67 MHz up to 150 MHz, and is ideally suited for high-speed microprocessor and synchronous DRAM applications.

A dedicated feedback output (FBOUT) is used to synchronize the output clocks in frequency and phase to the CLKIN reference. Four banks of four outputs (1Yn, 2Yn, 3Yn, 4Yn) are configured to operate at specified ratios of the input frequency by four select (SELn) inputs. Selectable ratios of the input frequency are 1X, 2X, 3X, 1/2X, and 1/3X.

The output-enable ($\overline{OE}$) input provides control for the Y output banks. When $\overline{OE}$ is high, the outputs are in a high-impedance state. When $\overline{OE}$ is low, the outputs switch in accordance with the select inputs. In addition, RESET provides a master reset for the CDC587 counter circuitry. This allows the outputs to be reset to a known state. TEST provides a bypass of the integrated PLL and divider circuitry. When TEST is high, the input clock bypasses the PLL and is buffered directly to the outputs.

PRODUCT PREVIEW

functional block diagram



PRODUCT PREVIEW

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		3.6	V
V_{REF}	SSTL reference voltage		1.3	1.5	1.7	V
V_I	Input voltage		0		5.5	V
V_{IH}	High-level input voltage	CLK, FBIN	V_{REF}+100 mV			V
		CLK, FBIN (V_{REF} = GND)	2			
		Other inputs	2			
V_{IL}	Low-level input voltage	CLK, FBIN			V_{REF}–100 mV	V
		CLK, FBIN (V_{REF} = GND)			0.8	
		Other inputs			0.8	
I_{OH}	High-level output current				–20	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature		0		70	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

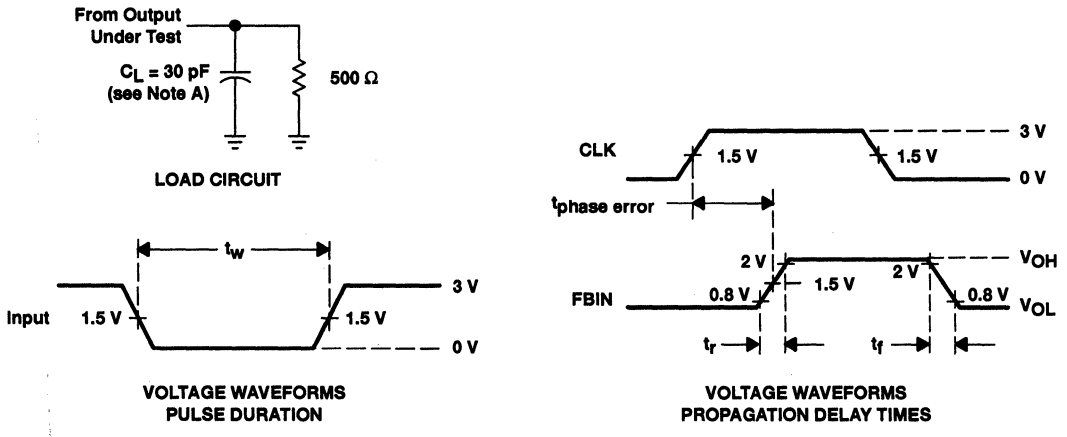
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 3 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V
	V_{CC} = 3 V	I_{OH} = –16 mA		2.2			
		I_{OH} = –20 mA		2.1			
V_{OL}	V_{CC} = 3 V	I_{OL} = 100 µA				0.2	V
		I_{OL} = 16 mA				0.5	
		I_{OL} = 20 mA				0.5	
I_I	V_{CC} = 0 or MAX‡,	V_I = 3.6 V,	V_{REF} = GND			±10	µA
	V_{CC} = 3.6 V	V_I = V_{CC} or GND,	V_{REF} = GND			±1	
		V_I = 2.1 V or 0.9 V,	V_{REF} = 1.5			±1	
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				10	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0				–10	µA
I_{CC}	V_{CC} = 3.6 V, I_O = 0	V_I = V_{CC} or GND,	V_{REF} = GND			1	mA
		V_I = 2.1 V or 0.9 V,	V_{REF} = 1.5 V			6	
C_i	V_I = V_{CC} or GND,	V_{REF} = GND			3		pF
	V_I = 2.1 V or 0.9 V,	V_{REF} = 1.5 V			3		
C_o	V_O = 3 V or 0,	V_{REF} = GND			6		pF
	V_O = 2.1 V or 0.9 V,	V_{REF} = 1.5 V			6		

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

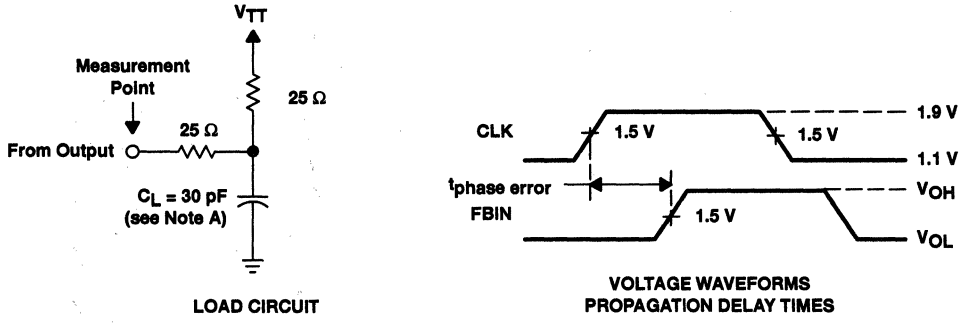
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 150 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms for LVTTL



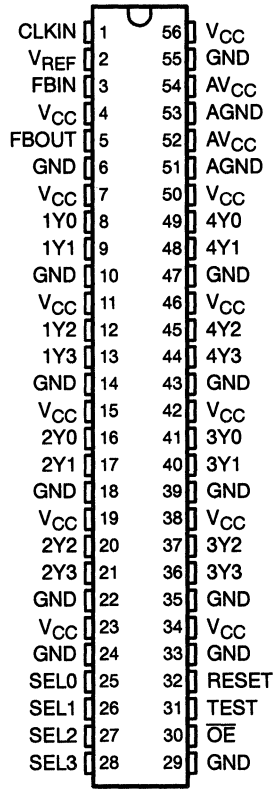
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 150 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. The outputs are measured one at a time with one transition per measurement.
D. $V_{TT} = V_{REF} = V_{CC} \times 0.45$

Figure 2. Load Circuit and Voltage Waveforms for SSTL_3

PRODUCT PREVIEW

- **Low-Output Skew and Jitter for Clock Distribution and Synchronization**
- **Operates at 3.3-V V_{CC}**
- **Distributes One Clock Input to 16 Outputs**
- **Four Select Inputs Configure Output Frequency**
- **Internal Loop Filter Eliminates the Need for External RC Network**
- **Dedicated External Feedback Output and Input for Phase Synchronization With the Clock Input**
- **Applications for Synchronous DRAM, High-Speed Microprocessors, and SSTL_3 Applications**
- **LVTTL- or SSTL_3-Compatible Inputs and Outputs**
- **Distributed V_{CC} and GND Pin Configuration Minimize High-Speed Switching Noise**
- **Meets SSTL_3 Class 1 and 2 Specifications**
- **Packaged in 56-Pin Plastic Small-Outline Package**

DGG PACKAGE
(TOP VIEW)



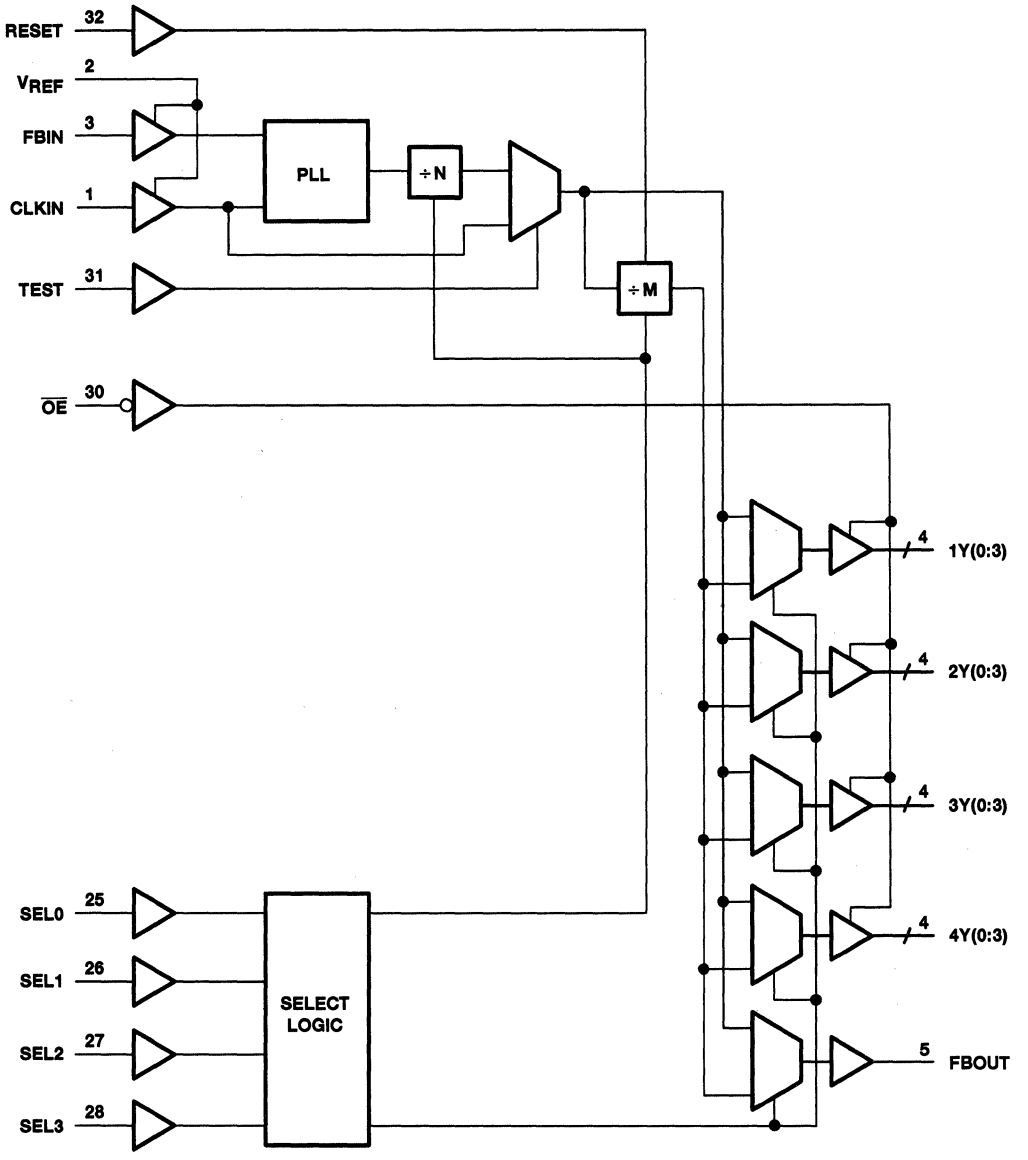
description

The CDC2587 is a high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the clock output signals to the clock input (CLKIN) signal. The CDC2587 operates at 3.3-V V_{CC} and provides LVTTL- or SSTL_3-compatible inputs and outputs. The CDC2587 operates at frequencies from 16.67 MHz to 150 MHz, and is ideally suited for high-speed microprocessor and synchronous DRAM applications. The CDC2587 provides integrated 25-Ω series damping resistors to improve signal integrity.

A dedicated feedback output (FBOUT) is used to synchronize the output clocks in frequency and phase to the CLKIN reference. Four banks of four outputs (1Yn, 2Yn, 3Yn, 4Yn) are configured to operate at specified ratios of the input frequency by four select (SELn) inputs . Selectable ratios of the input frequency are 1X, 2X, 3X, 1/2X, and 1/3X.

PRODUCT PREVIEW

functional block diagram



PRODUCT PREVIEW

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		3.6	V
V_{REF}	SSTL reference voltage		1.3	1.5	1.7	V
V_I	Input voltage		0		5.5	V
V_{IH}	High-level input voltage	CLKIN, FBIN	V_{REF}+100 mV			V
		CLKIN, FBIN (V_{REF} = GND)	2			
		Other inputs	2			
V_{IL}	Low-level input voltage	CLKIN, FBIN			V_{REF}–100 mV	V
		CLKIN, FBIN (V_{REF} = GND)			0.8	
		Other inputs			0.8	
I_{OH}	High-level output current				–12	mA
I_{OL}	Low-level output current				12	mA
T_A	Operating free-air temperature		0		70	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

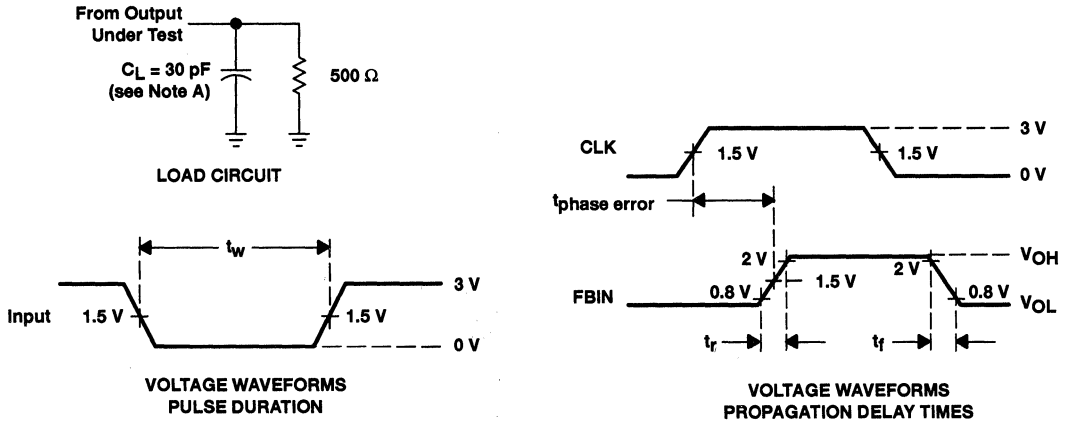
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 3 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V
	V_{CC} = 3 V,	I_{OH} = – 12 mA		2.4			
V_{OL}	V_{CC} = 3 V	I_{OL} = 100 µA				0.2	V
		I_{OL} = 12 mA				0.4	
I_I	V_{CC} = 0 or MAX‡,	V_I = 3.6 V,	V_{REF} = GND			±10	µA
	V_{CC} = 3.6 V	V_I = V_{CC} or GND,	V_{REF} = GND			±1	
		V_I = 2.1 V or 0.9 V,	V_{REF} = 1.5 V			±1	
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				10	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0				–10	µA
I_{CC}	V_{CC} = 3.6 V, I_O = 0,	V_I = V_{CC} or GND,	V_{REF} = GND			1	mA
		V_I = 2.1 V or 0.9 V,	V_{REF} = 1.5 V			1	
C_i	V_I = V_{CC} or GND,	V_{REF} = GND			3		pF
	V_I = 2.1 V or 0.9 V,	V_{REF} = 1.5 V			3		
C_o	V_O = 3 V or 0,	V_{REF} = GND			6		pF
	V_O = 2.1 V or 0.9 V,	V_{REF} = 1.5 V			6		

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

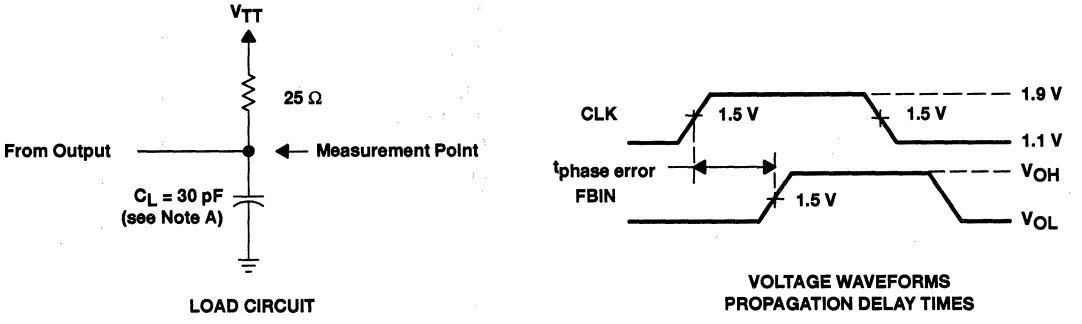
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 150 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 150 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. The outputs are measured one at a time with one transition per measurement.
D. $V_{TT} = V_{REF} = V_{CC} \times 0.4$

Figure 2. Load Circuit and Voltage Waveforms for SSTL_3 Class 1

PRODUCT PREVIEW

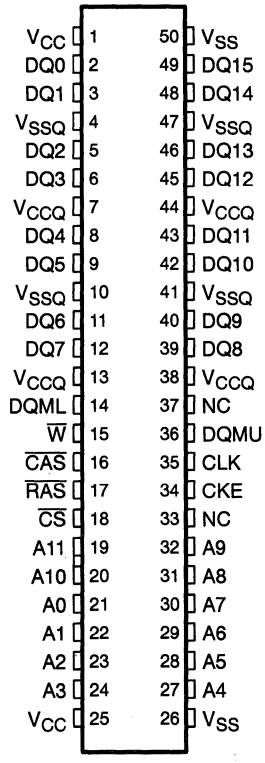
- **Organization . . . 512K × 16 × 2 Banks**
- **3.3-V Power Supply (±10% Tolerance)**
- **Two Banks for On-Chip Interleaving (Gapless Accesses)**
- **High Bandwidth – Up to 83-MHz Data Rates**
- **Read Latency Programmable to 1, 2, or 3 Cycles From Column-Address Entry**
- **Burst Sequence Programmable to Serial or Interleave**
- **Burst Length Programmable to 1, 2, 4, 8, or Full Page**
- **Chip Select and Clock Enable for Enhanced-System Interfacing**
- **Cycle-by-Cycle DQ-Bus Mask Capability With Upper and Lower Byte Control**
- **Auto-Refresh and Self-Refresh Capability**
- **4K Refresh (Total for Both Banks)**
- **High-Speed, Low-Noise, Low-Voltage TTL (LVTTL) Interface**
- **Power-Down Mode**
- **Compatible With JEDEC Standards**
- **Pipeline Architecture**
- **Employs Enhanced Performance Implanted CMOS (EPIC™) Technology Fabricated by Texas Instruments (TI™)**
- **Temperature Ranges:**
  Operating, 0°C to 70°C
  Storage, – 55°C to 150°C
- **Performance Ranges:**

	SYNCHRONOUS CLOCK CYCLE TIME	ACTV COMMAND TO READ OR WRT COMMAND	REFRESH TIME INTERVAL
	t_{CK} (MIN)	t_{RCD} (MIN)	t_{REF} (MAX)
'626162-12A	12 ns	30 ns	64 ms
'626162-12	12 ns	30 ns	64 ms
'626162-15	15 ns	30 ns	64 ms

description

The TMS626162 series of devices are high-speed 16777216-bit synchronous dynamic random-access memories (SDRAMs) organized as two banks of 524288 words with sixteen bits per word.

DGE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A10	Address Inputs A0–A10 Row Addresses A0–A7 Column Addresses A10 Automatic-Precharge Select
A11	Bank Select
$\overline{CAS}$	Column-Address Strobe
CKE	Clock Enable
CLK	System Clock
$\overline{CS}$	Chip Select
DQ0–DQ15	SDRAM Data Input/Data Output
DQML, DQMU	Data/Output Mask Enables
NC	No Connect
$\overline{RAS}$	Row-Address Strobe
V_{CC}	Power Supply (3.3 V Typ)
V_{CCQ}	Power Supply for Output Drivers (3.3 V Typ)
V_{SS}	Ground
V_{SSQ}	Ground for Output Drivers
$\overline{W}$	Write Enable

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operation (continued)

Table 1. Basic Command Truth Table†

COMMAND	STATE OF BANK(S)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	A11	A10	A9–A0	MNEMONIC
Mode register set	T = deac B = deac	L	L	L	L	X	X	A9 = V A8 – A7 = 0 A6 – A0 = V	MRS
Bank deactivate (precharge)	X	L	L	H	L	BS	L	X	DEAC
Deactivate all banks	X	L	L	H	L	X	H	X	DCAB
Bank activate/row-address entry	SB = deac	L	L	H	H	BS	V	V	ACTV
Column-address entry/write operation	SB = actv	L	H	L	L	BS	L	V	WRT
Column-address entry/write operation with auto-deactivate	SB = actv	L	H	L	L	BS	H	V	WRT-P
Column-address entry/read operation	SB = actv	L	H	L	H	BS	L	V	READ
Column-address entry/read operation with auto-deactivate	SB = actv	L	H	L	H	BS	H	V	READ-P
Burst stop	SB = actv	L	H	H	L	X	X	X	STOP
No operation	X	L	H	H	H	X	X	X	NOOP
Control-input inhibit/no operation	X	H	X	X	X	X	X	X	DESL
Auto refresh‡	T = deac B = deac	L	L	L	H	X	X	X	REFR

† For execution of these commands on cycle n:
- CKE (n–1) must be high, or
- t_{CESP} must be satisfied for power-down exit, or
- t_{CESP} and t_{RC} must be satisfied for self-refresh exit, or
- t_{CES} and nCLE must be satisfied for clock-suspend exit.

DQMx(n) is a don't care.

‡ Auto-refresh or self-refresh entry requires that all banks be deactivated or in an idle state prior to the command entry.

Legend:

n = CLK cycle number
L = Logic low
H = Logic high
X = Don't care, either logic low or logic high
V = Valid
T = Bank T
B = Bank B
actv = Activated
deac = Deactivated
BS = Logic high to select bank T; logic low to select bank B
SB = Bank selected by A11 at cycle n

operation (continued)

Table 3. DQM-Use Command Truth Table†

COMMAND	STATE OF BANK(S)	DQML DQMU‡ (n)	DATA IN (n)	DATA OUT (n + 2)	MNEMONIC
—	T = deac and B = deac	X	N/A	Hi-Z	—
—	T = actv and B = actv (no access operation)§	X	N/A	Hi-Z	—
Data-in enable	T = write or B = write	L	V	N/A	ENBL
Data-in mask	T = write or B = write	H	M	N/A	MASK
Data-out enable	T = read or B = read	L	N/A	V	ENBL
Data-out mask	T = read or B = read	H	N/A	Hi-Z	MASK

† For execution of these commands on cycle n:
- CKE (n) must be high, or
- t_{CESP} must be satisfied for power-down exit, or
- t_{CESP} and t_{RC} must be satisfied for self-refresh exit, or
- t_{CES} and n_{CLE} must be satisfied for clock suspend exit.

$\overline{CS}$(n), $\overline{RAS}$(n), $\overline{CAS}$(n), $\overline{W}$(n), and A0–A11 are don't cares.

‡ DQML controls D0–D7 and Q0–Q7
DQMU controls D8–D15 and Q8–Q15

§ A bank is no longer in an access operation one cycle after the last data-out cycle of a read operation, and two cycles after the last data-in cycle of a write operation. Neither the PDE nor the HOLD command is allowed on the cycle immediately following the last data-in cycle of a write operation.

Legend:

n	=	CLK cycle number
L	=	Logic low
H	=	Logic high
X	=	Don't care, either logic low or logic high
V	=	Valid
M	=	Masked input data
N/A	=	Not applicable
T	=	Bank T
B	=	Bank B
actv	=	Activated
deac	=	Deactivated
write	=	Activated and accepting data in on cycle n
read	=	Activated and delivering data out on cycle (n + 2)

burst sequence (continued)

Table 6. 8-Bit Burst Sequences

	INTERNAL COLUMN ADDRESS A2–A0															
	DECIMAL								BINARY							
	START	2ND	3RD	4TH	5TH	6TH	7TH	8TH	START	2ND	3RD	4TH	5TH	6TH	7TH	8TH
Serial	0	1	2	3	4	5	6	7	000	001	010	011	100	101	110	111
	1	2	3	4	5	6	7	0	001	010	011	100	101	110	111	000
	2	3	4	5	6	7	0	1	010	011	100	101	110	111	000	001
	3	4	5	6	7	0	1	2	011	100	101	110	111	000	001	010
	4	5	6	7	0	1	2	3	100	101	110	111	000	001	010	011
	5	6	7	0	1	2	3	4	101	110	111	000	001	010	011	100
	6	7	0	1	2	3	4	5	110	111	000	001	010	011	100	101
	7	0	1	2	3	4	5	6	111	000	001	010	011	100	101	110
Interleave	0	1	2	3	4	5	6	7	000	001	010	011	100	101	110	111
	1	0	3	2	5	4	7	6	001	000	011	010	101	100	111	110
	2	3	0	1	6	7	4	5	010	011	000	001	110	111	100	101
	3	2	1	0	7	6	5	4	011	010	001	000	111	110	101	100
	4	5	6	7	0	1	2	3	100	101	110	111	000	001	010	011
	5	4	7	6	1	0	3	2	101	100	111	110	001	000	011	010
	6	7	4	5	2	3	0	1	110	111	100	101	010	011	000	001
	7	6	5	4	3	2	1	0	111	110	101	100	011	010	001	000

latency

The beginning data-out cycle of a read burst can be programmed to occur 1, 2, or 3 CLK cycles after the read command (see the section on setting the mode register, page 5–11). This feature allows the user to adjust the '626162 to operate in accordance with the system's capability to latch the data output from the '626162. The delay between the READ command and the beginning of the output burst is known as *read latency* (also known as $\overline{\text{CAS}}$ latency). After the initial output cycle begins, the data burst occurs at the CLK frequency without any intervening gaps. Use of minimum read latencies is restricted based on the particular maximum frequency rating of the '626162.

There is no latency for data-in cycles (write latency). The first data-in cycle of a write burst is entered at the same rising edge of CLK on which the WRT command is entered. The write latency is fixed and is not determined by the mode-register contents.

two-bank operation

The '626162 contains two independent banks that can be accessed individually or in an interleaved fashion. Each bank must be activated with a row address before it can be accessed. Each bank then must be deactivated before it can be activated again with a new row address. The bank-activate/row-address-entry command (ACTV) is entered by holding $\overline{\text{RAS}}$ low, $\overline{\text{CAS}}$ high, $\overline{\text{W}}$ high, and A11 valid on the rising edge of CLK. A bank can be deactivated either automatically during a READ-P or a WRT-P command or by use of the deactivate-bank (DEAC) command. Both banks can be deactivated at once by use of the DCAB command (see Table 1 and the section on bank deactivation, page 5–10).

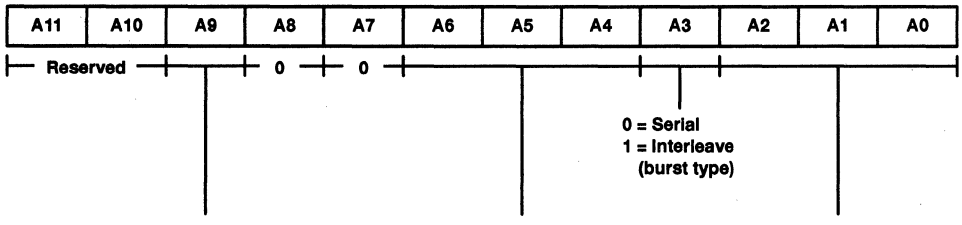
CLK-suspend/power-down mode

For normal device operation, CKE should be held high to enable CLK. If CKE goes low during the execution of a READ (READ-P) or WRT (WRT-P) operation, the state of the DQ bus occurring at the immediate next rising edge of CLK is frozen at its current state, and no further inputs are accepted until CKE returns high. This is known as a CLK-suspend operation, and its execution is denoted as a HOLD command. The device resumes operation from the point at which it was placed in suspension, beginning with the second rising edge of CLK after CKE returns high.

If CKE is brought low when no read or write command is in progress, the device enters power-down mode. If both banks are deactivated when power-down mode is entered, power consumption is reduced to the minimum. Power-down mode can be used during row-active or auto-refresh periods to reduce input-buffer power. After power-down mode is entered, no further inputs are accepted until CKE returns high. To ensure that data in the device remains valid during the power-down mode, the self-refresh command (SLFR) must be executed concurrently with the power-down entry (PDE) command. When exiting power-down mode, new commands can be entered on the first CLK edge after CKE returns high, provided that the setup time (t_{CESP}) is satisfied. Table 2 shows the command configuration for a CLK-suspend/power-down operation; Figure 19, Figure 20, and Figure 38 show examples of the procedure.

setting the mode register

The '626162 contains a mode register that must be programmed with the read latency, the burst type, and the burst length. This is accomplished by executing a mode-register set (MRS) command with the information entered on the address lines A0–A9. A logic 0 must be entered on A7 and A8, but A10 and A11 are don't-care entries for the '626162. When A9 = 1, the write-burst length is always 1. When A9 = 0, the write-burst length is defined by A0–A2. Figure 1 shows the valid combinations for a successful MRS command. Only valid addresses allow the mode register to be changed. If the addresses are not valid, the previous contents of the mode register remain unaffected. The MRS command is executed by holding $\overline{RAS}$, $\overline{CAS}$, and $\overline{W}$ low and the input mode word valid on A0–A9 on the rising edge of CLK (see Table 1). The MRS command can be executed only when both banks are deactivated.



REGISTER BIT A9	Write Burst Length
0	A2–A0
1	1

REGISTER BITS†			READ LATENCY‡
A6	A5	A4	
0	0	1	1
0	1	0	2
0	1	1	3

† All other combinations are reserved.
‡ Refer to timing requirements for minimum valid read latencies based on maximum frequency rating.

REGISTER BITS§			BURST LENGTH
A2	A1	A0	
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	1	1	256

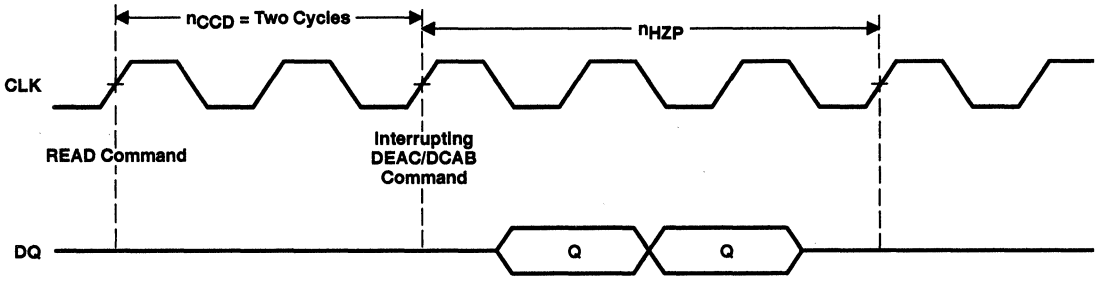
§ All other combinations are reserved.

Figure 1. Mode-Register Programming

Table 7. Read-Burst Interruption

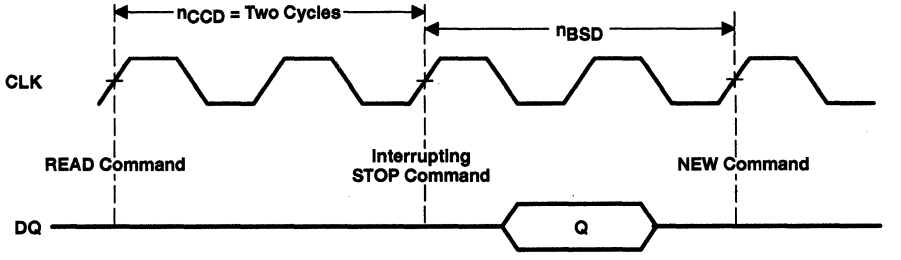
INTERRUPTING COMMAND	EFFECT OR NOTE ON USE DURING READ BURST
READ, READ-P	Current output cycles continue until the programmed latency from the superseding-READ (READ-P) command is met and new output cycles begin (see Figure 2).
WRT, WRT-P	The WRT (WRT-P) command immediately supersedes the read burst in progress. To avoid data contention, DQMx must be held high before the WRT (WRT-P) command to mask output of the read burst on cycles (n_{CCD}-1), n_{CCD}, and (n_{CCD}+1), assuming that there is any output on these cycles. For read latency = 1, read burst interruption by a WRT (WRT-P) command is not allowed at n_{CCD} = 1, 2 (see Figure 3).
DEAC, DCAB	The DQ bus is in the high-impedance state when n_{HZP} cycles are satisfied or when the read burst completes, whichever occurs first (see Figure 4).
STOP	The DQ bus is in the high-impedance state when n_{BSD} cycles are satisfied or when the read burst completes, whichever occurs first. The bank remains active. A new read or write command cannot be entered for at least two cycles after the STOP command (see Figure 5).

interrupted bursts (continued)



NOTE A: For this example, assume read latency = 3 and burst length = 4.

Figure 4. Read Burst Interrupted by DEAC Command



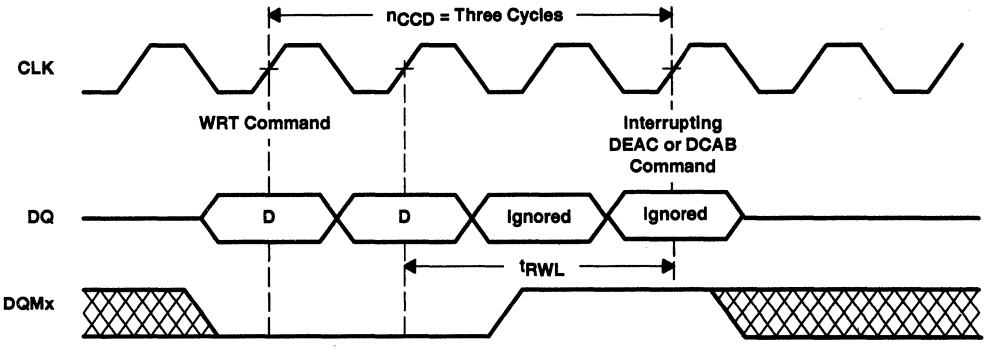
NOTE A: For this example, assume read latency = 3 and burst length = 4.

Figure 5. Read Burst Interrupt by STOP Command

Table 8. Write-Burst Interruption

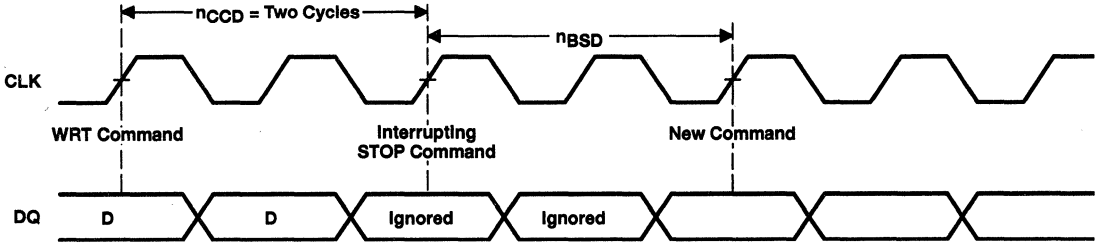
INTERRUPTING COMMAND	EFFECT OR NOTE ON USE DURING WRITE BURST
READ, READ-P	Data in on previous cycle is written. No further data in is accepted (see Figure 6).
WRT, WRT-P	The new WRT (WRT-P) command and data in immediately supersede the write burst in progress (see Figure 7).
DEAC, DCAB	The DEAC/DCAB command immediately supersedes the write burst in progress. DQMx must be used to mask the DQ bus such that the write recovery specification (t_{RWL}) is not violated by the interrupt (see Figure 8).
STOP	The data on the input pins at the time of the burst-STOP command is not written; no further data is accepted. The bank remains active. A new read or write command cannot be entered for at least n_{BSD} cycles after the STOP command (see Figure 9).

interrupted bursts (continued)



NOTE A: For this example, assume burst length = 4.

Figure 8. Write Burst Interrupted by DEAC/DCAB Command



NOTE A: For this example, assume burst length = 4.

Figure 9. Write Burst Interrupted by STOP Command

power up

Device initialization should be performed after a power up to the full V_{CC} level. After power is established, a 200-µs interval is required (with no inputs other than CLK). After this interval, both banks of the device must be deactivated. Eight REFR commands must be performed, and the mode register must be set to complete the device initialization.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	– 0.5 V to 4.6 V
Supply voltage range for output drivers, V_{CCQ}	– 0.5 V to 4.6 V
Voltage range on any pin (see Note 1)	– 0.5 V to 4.6 V
Short-circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	– 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (see Note 2)

PARAMETER		TEST CONDITIONS			'626162-12A MIN	'626162-12A MAX	'626162-12 MIN	'626162-12 MAX	'626162-15 MIN	'626162-15 MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −2 mA			2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA				0.4		0.4		0.4	V
I_I	Input current (leakage)	0 V ≤ V_I ≤ V_{CC} + 0.3 V, All other pins = 0 V to V_{CC}				±10		±10		±10	µA
I_O	Output current (leakage)	0 V ≤ V_O ≤ V_{CC} + 0.3 V, Output disabled				±10		±10		±10	µA
I_{CC1}	Average read or write current	t_{RC} = MIN, t_{CK} = MIN, Read latency = 3	1 bank active	Burst length = 1 or 2		90		90		80	mA
				Burst length = 4 or 8		115		115		100	
			2 banks active, interleaving	Burst length = 1 or 2		150		150		120	
				Burst length = 4 or 8		190		190		150	
I_{CC2}	Standby current	Both banks deactivated	CKE = V_{IH}			25		25		20	mA
			CKE = V_{IL}			2		2		2	
			CKE = 0 V (CMOS)			1		1		1	
		1 or 2 banks active	CKE = V_{IH}			30		30		25	mA
			CKE = V_{IL}			8		8		8	
I_{CC3}	Consecutive CBR commands	t_{RC} = MIN				90		90		80	mA
I_{CC4}	Burst current, gapless burst	ACTV not allowed, t_{CK} = MIN, 2-bank interleaved		Read latency = 1		80		80		70	mA
				Read latency = 2		140		120		110	
				Read latency = 3		160		160		140	
I_{CC6}	Self-refresh current	CKE = V_{IL}				2		2		2	mA
		CKE = 0 V (CMOS)				1		1		1	

NOTES: 2. All specifications apply to the device after power-up initialization. All control and address inputs must be stable and valid.

ac timing requirements over recommended ranges of supply voltage and operating free-air temperature†‡

			'626162-12A		'626162-12		'626162-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{CK}	Cycle time, CLK (system clock)	Read latency = 1	36		36		40		ns
		Read latency = 2	15		18		20		
		Read latency = 3	12		12		15		
t_{CKH}	Pulse duration, CLK (system clock) high		4		4		4		ns
t_{CKL}	Pulse duration, CLK (system clock) low		4		4		4		ns
t_{AC}	Access time, CLK ↑ to data out (see Note 4)	Read latency = 1		31		31		35	ns
		Read latency = 2		9		13		15	
		Read latency = 3		9		9		9	
t_{LZ}	Delay time, CLK to DQ in the low-impedance state (see Note 5)		0		0		0		ns
t_{HZ}	Delay time, CLK to DQ in the high-impedance state (see Note 6)	Read latency = 1		20		20		20	ns
		Read latency = 2		13		13		14	
		Read latency = 3		10		10		11	
t_{DS}	Setup time, data input		3		3		3		ns
t_{AS}	Setup time, address		3		3		3		ns
t_{CS}	Setup time, control input ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, DQMx)		3		3		3		ns
t_{CES}	Setup time, CKE (suspend entry/exit, power-down entry)		3		3		3		ns
t_{CESP}	Setup time, CKE (power-down/self-refresh exit) (see Note 7)		10		10		10		ns
t_{OH}	Hold time, CLK ↑ to data out		3		3		3		ns
t_{DH}	Hold time, data input		1		1.5		1.5		ns
t_{AH}	Hold time, address		1		1.5		1.5		ns
t_{CH}	Hold time, control input ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, DQMx)		1		1.5		1.5		ns
t_{CEH}	Hold time, CKE		1		1.5		1.5		ns
t_{RC}	REFR command to ACTV, MRS, REFR, or SLFR command; ACTV command to ACTV, MRS, REFR, or SLFR command; Self-refresh exit to ACTV, MRS, REFR, or SLFR command		96		108		120		ns
t_{RAS}	ACTV command to DEAC or DCAB command		60	100 000	72	100 000	75	100 000	ns
t_{RCD}	ACTV command to READ or WRT command (see Note 8)		30		30		30		ns
t_{RP}	DEAC or DCAB command to ACTV, MRS, SLFR, or REFR command		36		36		45		ns

† See Parameter Measurement Information, page 5–24, for load circuits.
‡ All references are made to the rising transition of CLK, unless otherwise noted.

NOTES: 4. t_{AC} is referenced from the rising transition of CLK that is previous to the data-out cycle. For example, the first data out t_{AC} is referenced from the rising transition of CLK that is read latency – one cycle after the READ command. An access time is measured at output reference level 1.4 V.
5. t_{LZ} is measured from the rising transition of CLK that is read latency – one cycle after the READ command.
6. t_{HZ} (max) defines the time at which the outputs are no longer driven and is not referenced to output voltage levels.
7. See Figure 20 and Figure 21
8. For read or write operations with automatic deactivate, t_{RCD} must be set to satisfy minimum t_{RAS}.

Table 9. Number of Cycles Required to Meet Minimum Specification for Key Timing Parameters†

			TMS626802-12A			TMS626802-12			TMS626802-15			UNITS
	Operating frequency		83	66	50	83	66	50	66	50	33	MHz
t_{CK}	Cycle time, CLK (system clock)		12	15	20	12	15	20	15	20	30	ns
	KEY PARAMETER		**NUMBER OF CYCLES REQUIRED**									
	Read latency, minimum programmed value		3	2	2	3	3	2	3	2	2	cycles
t_{RCD}	ACTV command to READ or WRT command		3	2	2	3	2	2	2	2	1	cycles
t_{RAS}	ACTV command to DEAC or DCAB command		5	4	3	6	5	4	5	4	3	cycles
t_{RP}	DEAC or DCAB command to ACTV, MRS, SLFR, or REFR command		3	3	2	3	3	2	3	3	2	cycles
t_{RC}	REFR command to ACTV, MRS, or REFR command; self-refresh exit to ACTV, MRS, SLFR, or REFR command		8	7	5	9	8	6	8	6	4	cycles
t_{RWL}	Final data in to DEAC or DCAB command		2	2	1	3	2	1	2	2	1	cycles
t_{RRD}	ACTV command for one bank to ACTV command for the other bank		2	2	2	2	2	2	2	2	1	cycles
t_{APR}	Final data out of READ-P operation to ACTV, MRS, SLFR, or REFR command	Read latency = 1	—	—	—	—	—	—	—	—	—	cycles
		Read latency = 2	—	2	1	—	—	1	—	2	1	cycles
		Read latency = 3	1	1	0	1	1	0	1	1	0	cycles
t_{APW}	Final data in of WRT-P operation to ACTV, MRS, SLFR, or REFR command		5	4	3	5	4	3	5	4	3	cycles

† All references are made to the rising transition of CLK, unless otherwise noted.

PARAMETER MEASUREMENT INFORMATION

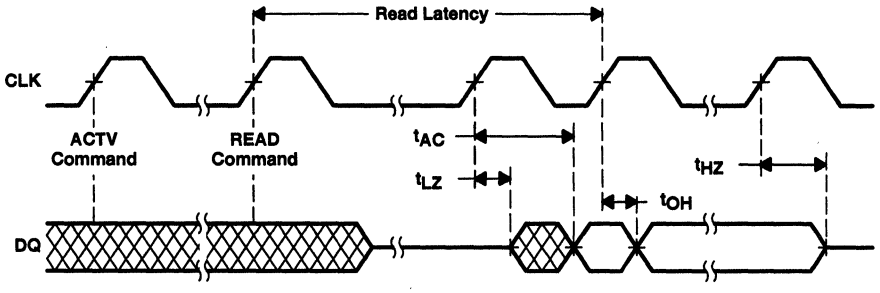


Figure 12. Output Parameters

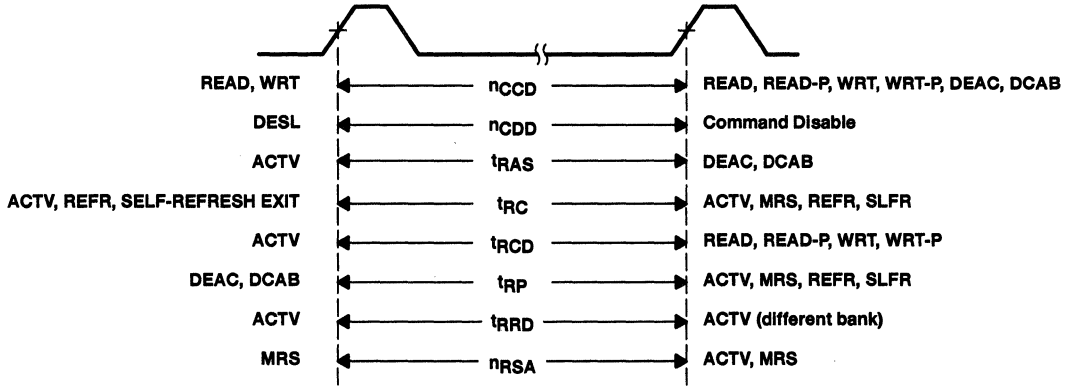


Figure 13. Command-to-Command Parameters

PARAMETER MEASUREMENT INFORMATION

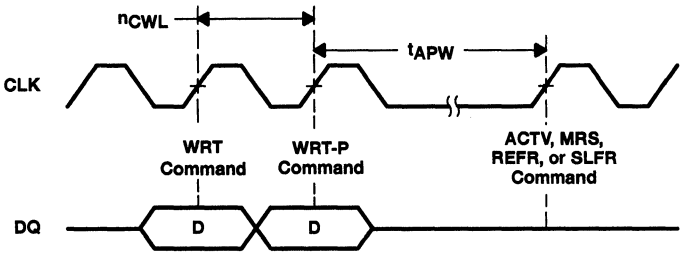
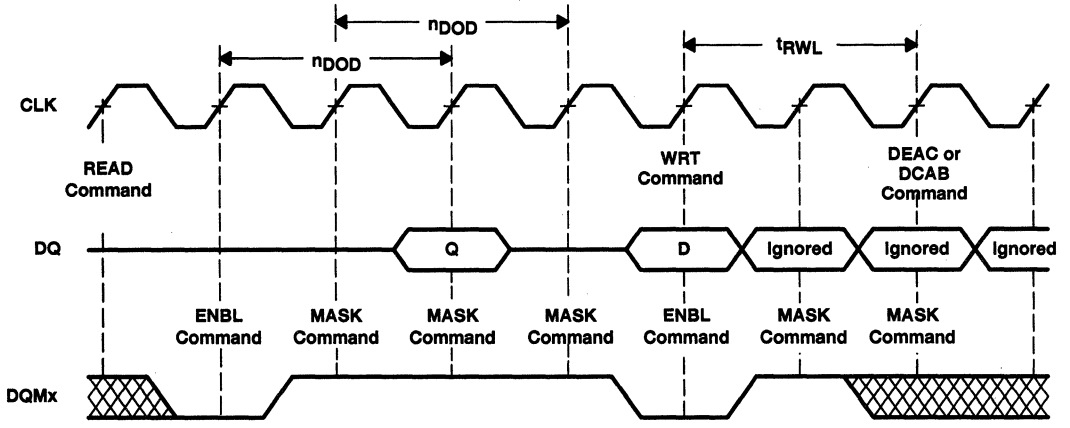


Figure 17. Write With Auto-Deactivate



NOTE A: For this example, assume read latency = 3, and burst length = 4.

Figure 18. DQ Masking

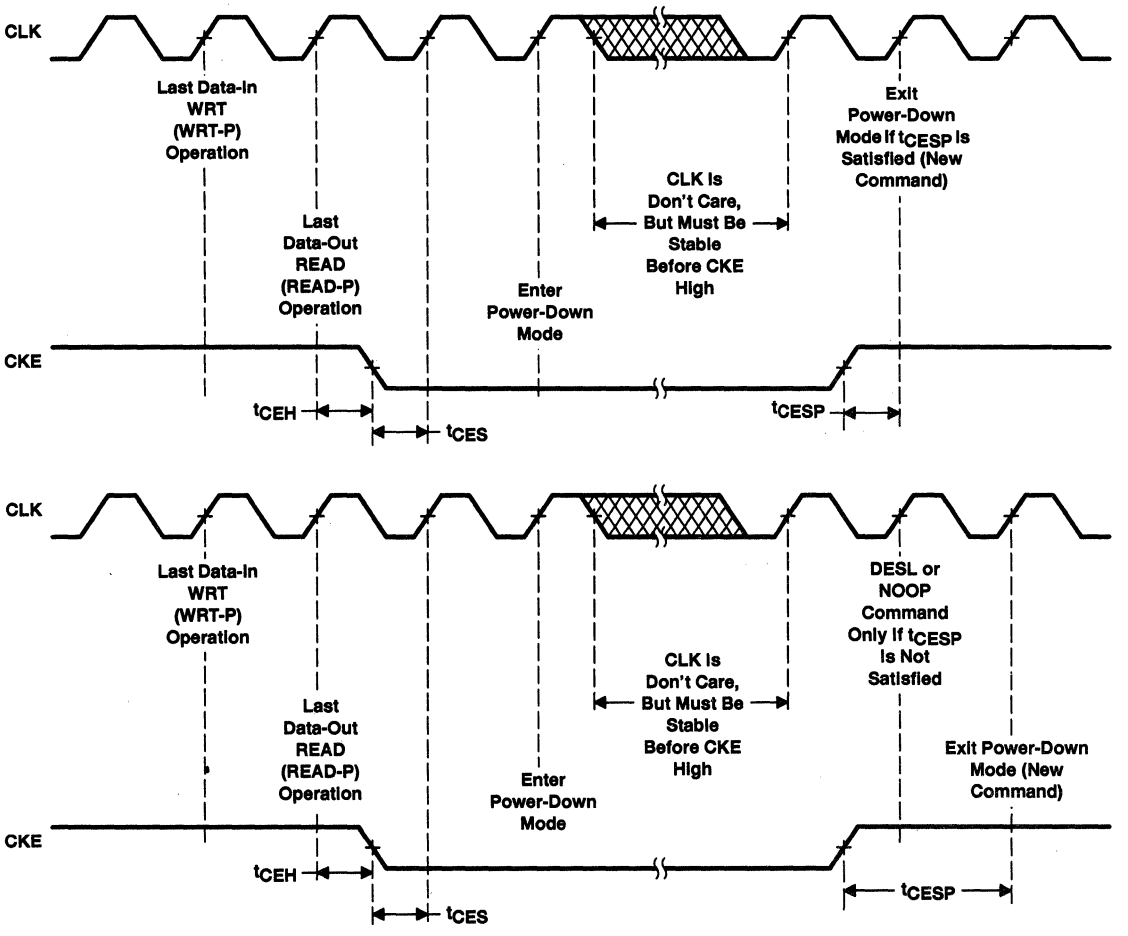
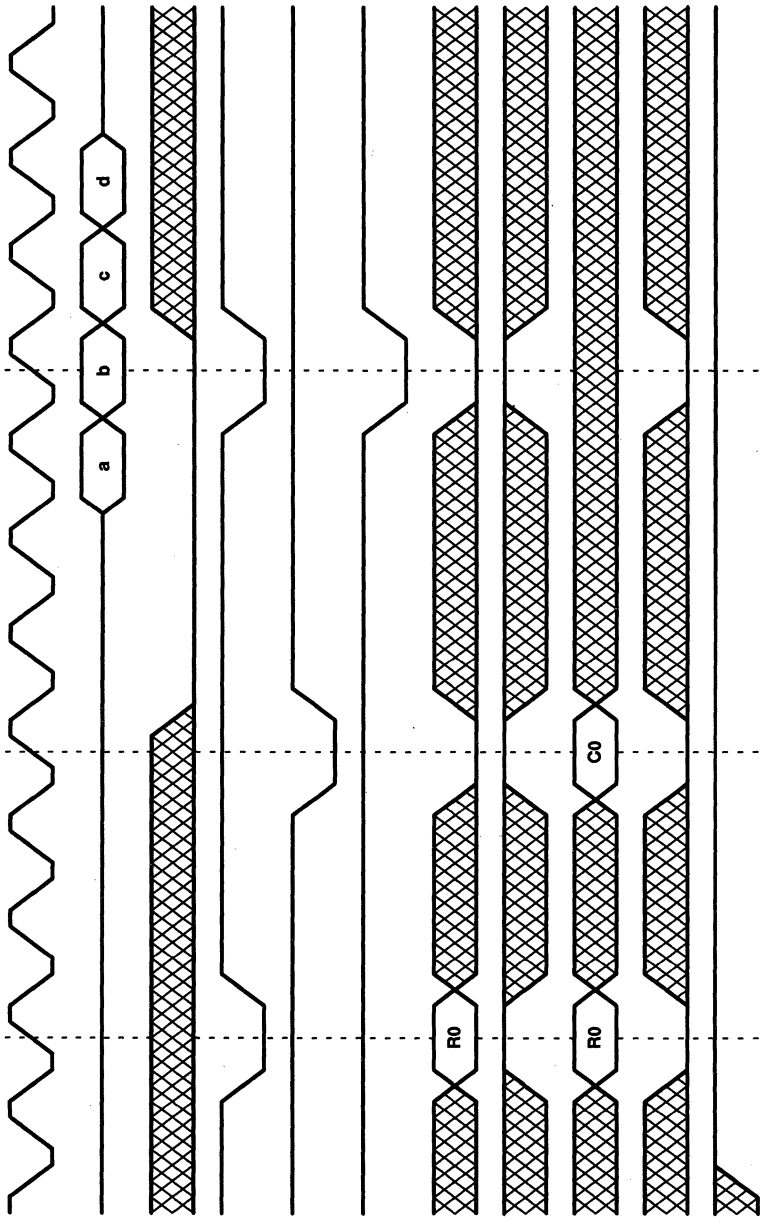


Figure 20. Power-Down Operation

PARAMETER MEASUREMENT INFORMATION



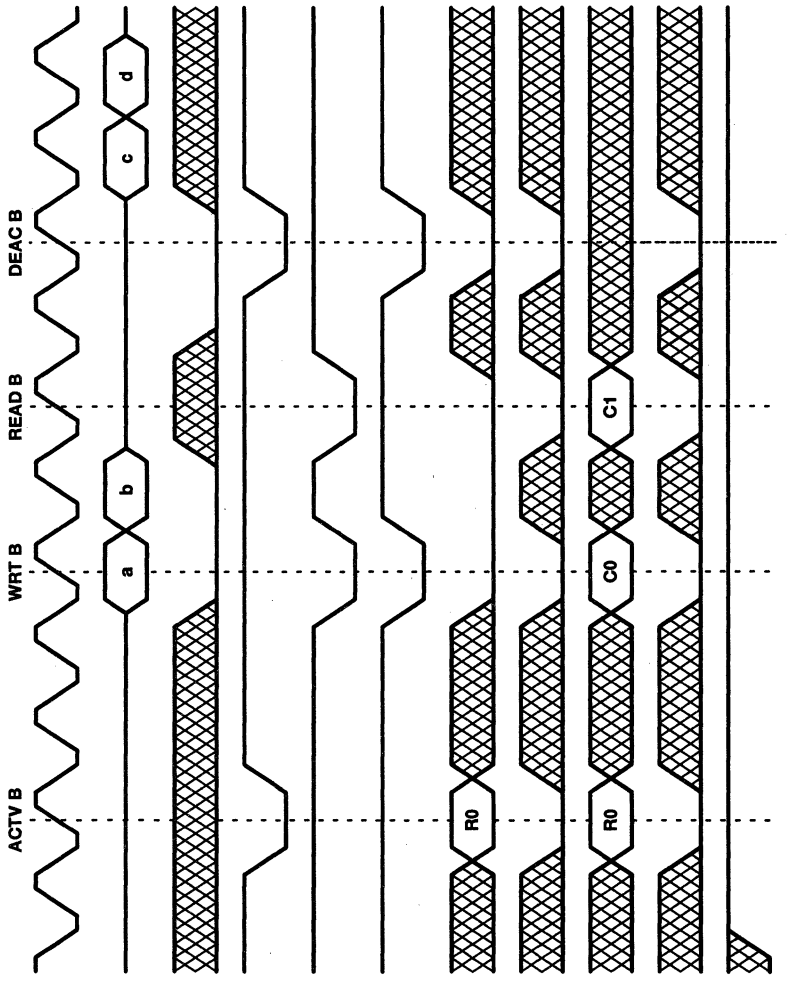
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d
Q	T	R0	C0	C0 + 1	C0 + 2	C0 + 3

† Column-address sequence depends on programmed burst type and starting column address C0 (see Table 5).

NOTE A: This example illustrates minimum t_{RCD} and n_{EP} for the '626162-12 at 83 MHz.

Figure 22. Read Burst (read latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION

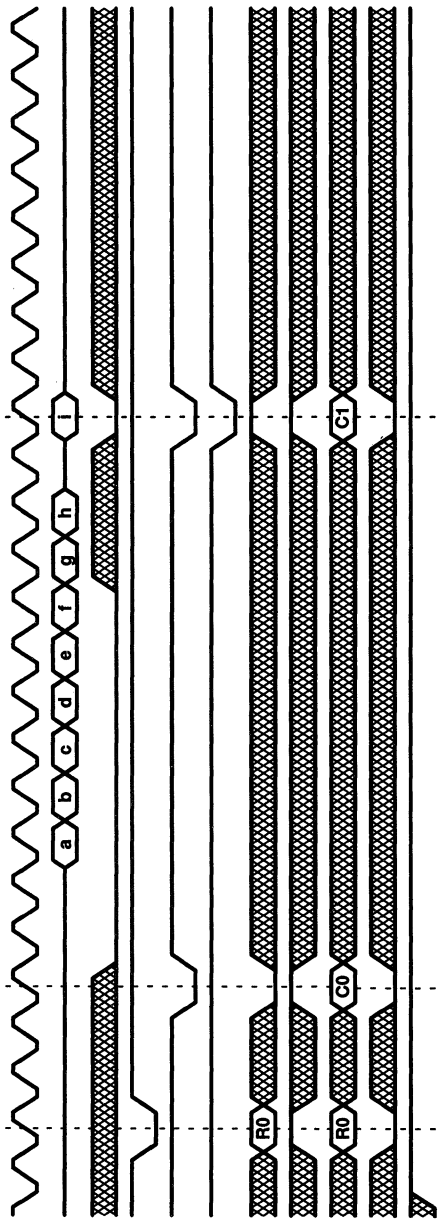


BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d
D	B	R0	C0	C0 + 1		
Q	B	R0			C1‡	C1 + 1

† Column-address sequence depends on programmed burst type and starting column address C0 and C1 (see Table 4).
NOTE A: This example illustrates minimum t_{RCD} and n_{EP} for the '626162-12 at 83 MHz.

Figure 24. Write-Read Burst (read latency = 3, burst length = 2)

PARAMETER MEASUREMENT INFORMATION

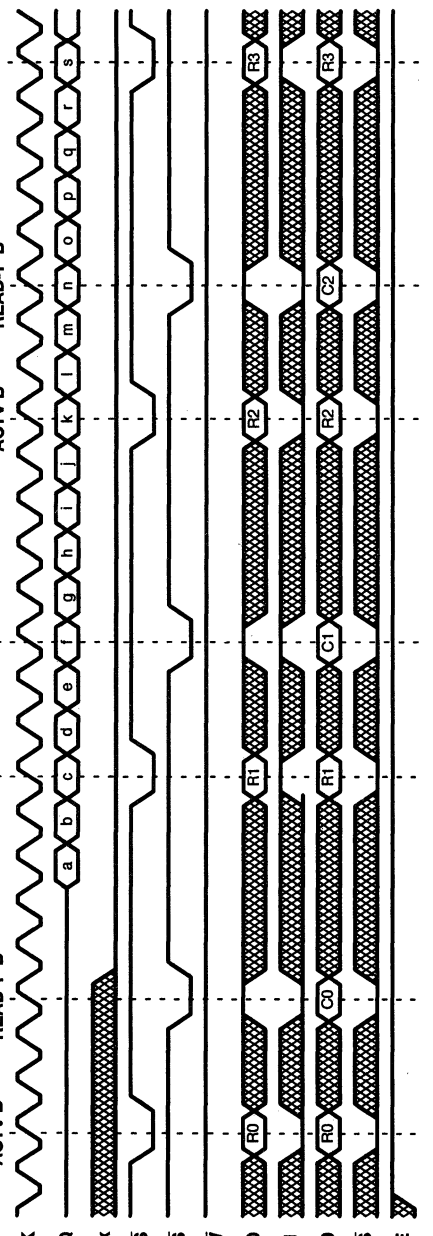


BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d	e	f	g	h	i
Q	T	R0	C0	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7	
D	T	R0									C1

† Column-address sequence depends on programmed burst type and starting column address C0 and C1 (see Table 6).
NOTE A: This example illustrates minimum t_{RCD} for the '626162-12 at 83 MHz.

Figure 26. Read Burst – Single Write With Automatic Deactivate (read latency = 3, burst length = 8)

PARAMETER MEASUREMENT INFORMATION

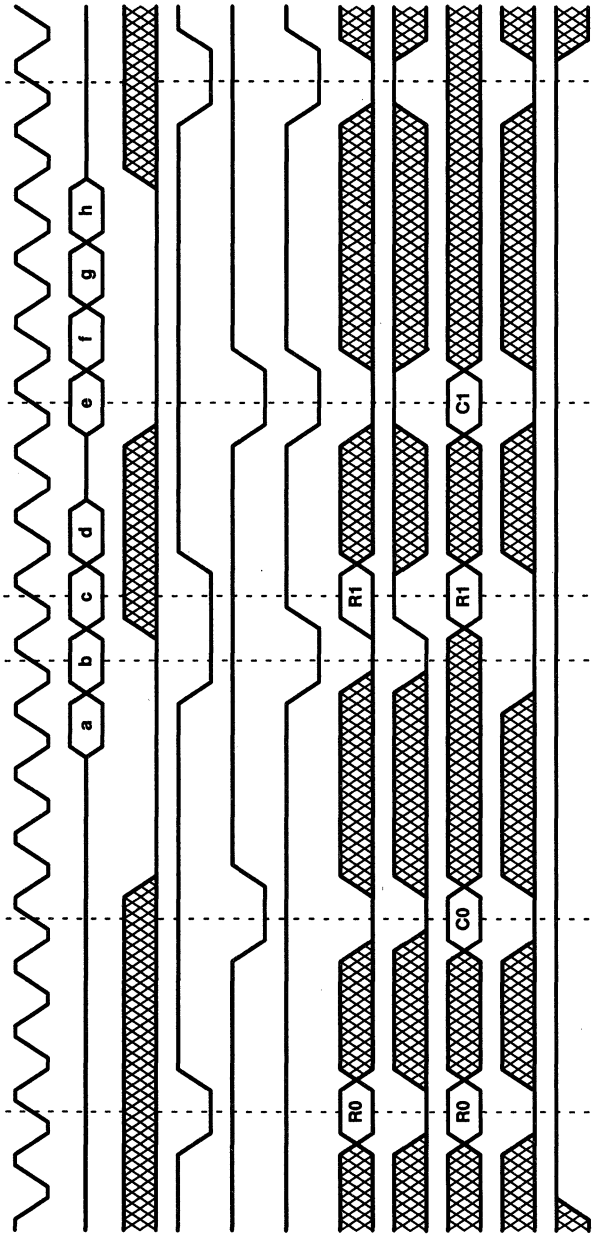


BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	. .
Q	B	R0	C0	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7												
Q	T	R1									C1	C1+1	C1+2	C1+3	C1+4	C1+5	C1+6	C1+7				
Q	B	R2																	C2	C2+1	C2+2	. .

† Column-address sequence depends on programmed burst type and starting column address C0, C1, and C2 (see Table 6).
NOTE A: This example illustrates minimum t_{RCD} for the '626162-12 at 83 MHz.

Figure 28. Two-Bank Row-Interleaving Read Bursts With Automatic Deactivate (read latency = 3, burst length = 8)

PARAMETER MEASUREMENT INFORMATION

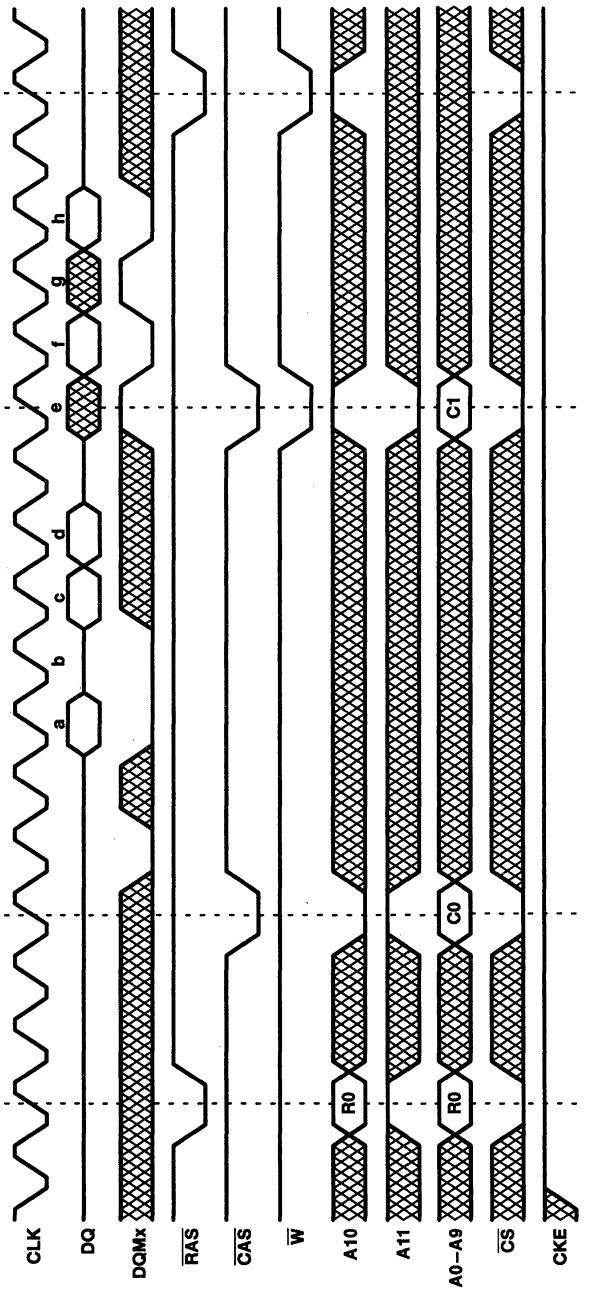


BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d	e	f	g	h
Q	B	R0	C0	C0 + 1	C0 + 2	C0 + 3				
D	T	R1					C1	C1 + 1	C1 + 2	C1 + 3

† Column-address sequence depends on programmed burst type and starting column address C0 and C1. (Refer to Table 5.)
NOTE A: This example illustrates minimum t_{RCD}, n_{EP}, and t_{RWL} for the '626162-12 at 83 MHz.

Figure 30. Read-Burst Bank B, Write-Burst Bank T (read latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION

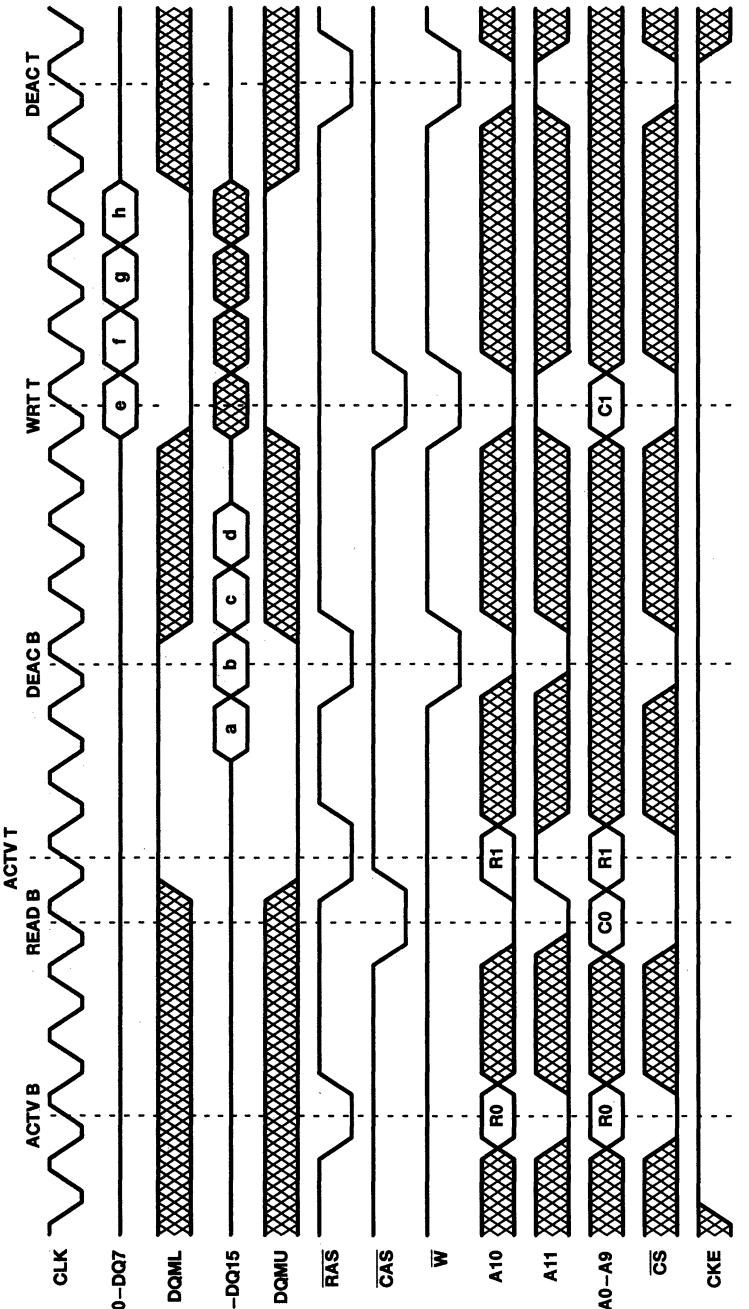


BURST TYPE	BANK	ROW	BURST CYCLE†							
(D/Q)	(B/T)	ADDR	a	b	c	d	e	f	g	h
Q	T	R0	C0	C0+1	C0+2	C0+3	C1	C1+1	C1+2	C1+3
D	T	R1								

† Column-address sequence depends on programmed burst type and starting column address C0 and C1 (see Table 5).
NOTE A: This example illustrates minimum t_{RCD} for the '626162-12 at 83 MHz.

Figure 32. Data Mask (read latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION



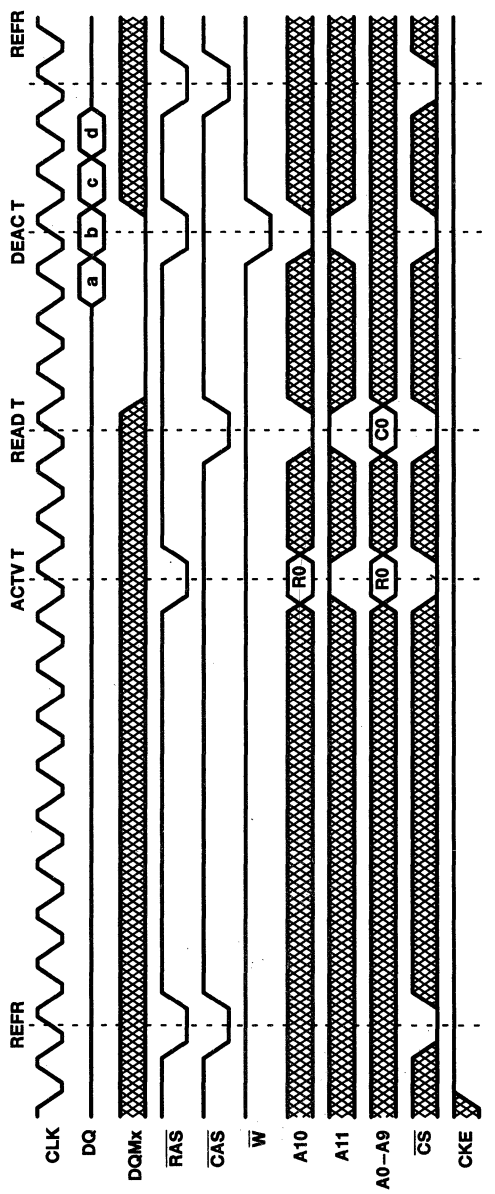
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d	e	f	g	h
Q	T	R0	C0	C0+1	C0+2	C0+3				
D	B	R1					C1	C1+1	C1+2	C1+3

† Column-address sequence depends on programmed burst type and starting column address C0 and C1 (see Table 5).

NOTE A: This example illustrates minimum t_{RCD} and n_{EP} read burst, and a minimum t_{RWL} write burst for the '626162-12 at 83 MHz

Figure 34. Data Mask With Byte Control (read latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION

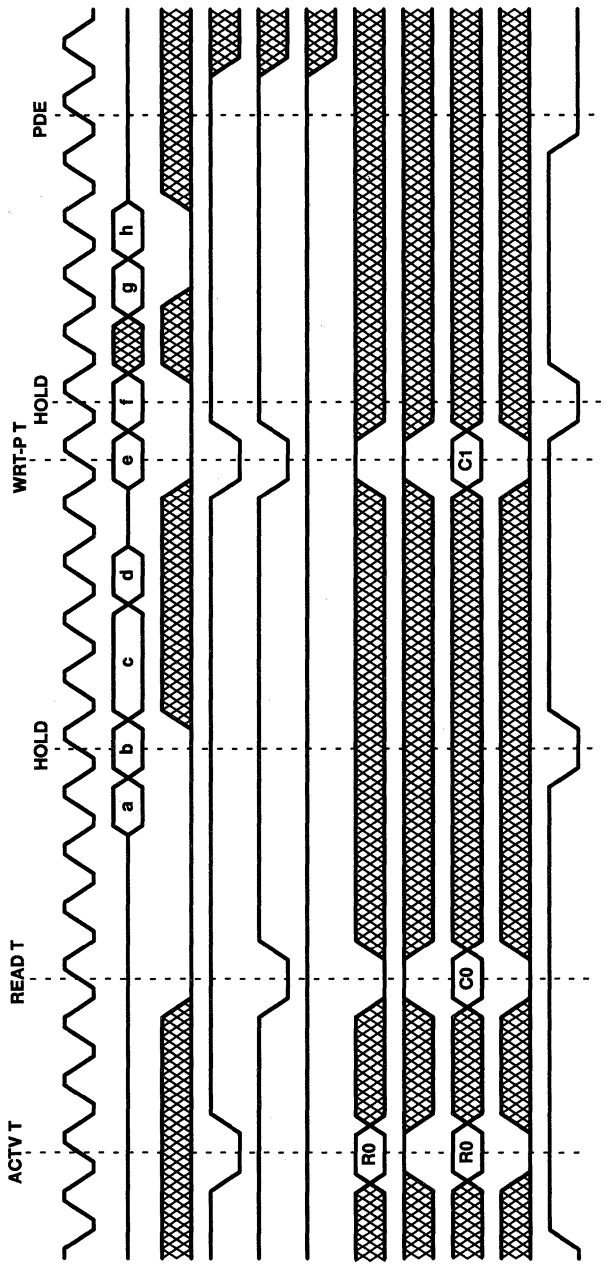


BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d
Q	T	R0	C0	C0+1	C0+2	C0+3

† Column-address sequence depends on programmed burst type and starting column address C0 (see 5).
NOTE A: This example illustrates minimuim t_{RC}, t_{RCD}, and n_{EP} for the '626162-12 at 83 MHz.

Figure 36. Refresh Cycles (read latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION

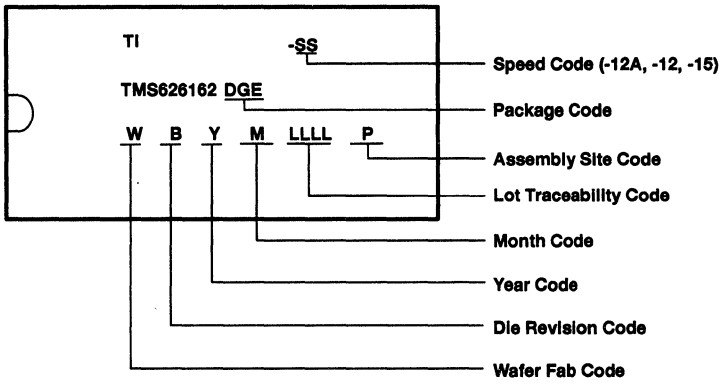


BURST-TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d	e	f	g	h
Q	T	R0	C0	C0+1	C0+2	C0+3				
D	T	R1					C1	C1+1	C1+2	C1+3

† Column-address sequence depends on programmed burst type and starting column address C0 and C1 (see 5).

Figure 38. CLK Suspend (HOLD) During Read Burst and Write Burst (read Latency = 3, burst length = 4)

device symbolization



- Organization . . . 1M × 8 × 2 Banks
- 3.3-V Power Supply (±10% Tolerance)
- Two Banks for On-Chip Interleaving (Gapless Accesses)
- High Bandwidth – Up to 83-MHz Data Rates
- Read Latency Programmable to 1, 2, or 3 Cycles From Column-Address Entry
- Burst Sequence Programmable to Serial or Interleave
- Burst Length Programmable to 1, 2, 4, or 8
- Chip Select and Clock Enable for Enhanced-System Interfacing
- Cycle-by-Cycle DQ-Bus Mask Capability
- Auto-Refresh and Self-Refresh Capability
- 4K Refresh (Total for Both Banks)
- High-Speed, Low-Noise Low-Voltage TTL (LVTTL) Interface
- Power-Down Mode
- Compatible With JEDEC Standards
- Pipeline Architecture
- Employs Enhanced Performance Implanted CMOS (EPIC™) Technology Fabricated by Texas Instruments (TI™)
- Temperature Ranges
  Operating, 0°C to 70°C
  Storage, – 55°C to 150°C
- Performance Ranges:

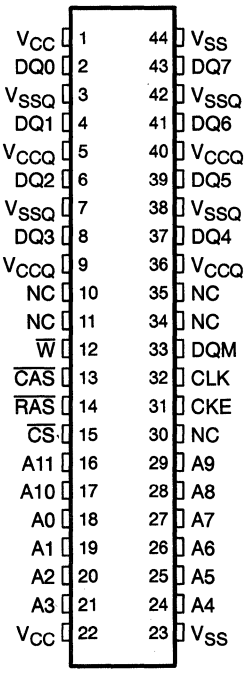
	SYNCHRONOUS CLOCK CYCLE TIME	ACTV COMMAND TO READ OR WRITE COMMAND	REFRESH TIME INTERVAL
	t_{CK} (MIN)	t_{RCD} (MIN)	t_{REF} (MAX)
'626812-12A	12 ns	30 ns	64 ms
'626812-12	12 ns	30 ns	64 ms
'626812-15	15 ns	30 ns	64 ms

description

The TMS626812 series of devices are high-speed 16777216-bit synchronous dynamic random-access memories (SDRAMs) organized as two banks of 1048576 words with eight bits per word.

All inputs and outputs of the TMS626812 series are compatible with the LVTTL interface.

DGE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A10	Address Inputs A0–A10 Row Addresses A0–A8 Column Addresses A10 Automatic-Precharge Select
A11	Bank Select
$\overline{CAS}$	Column-Address Strobe
CKE	Clock Enable
CLK	System Clock
$\overline{CS}$	Chip Select
DQ0–DQ7	SDRAM Data Input/Data Output
DQM	Data/Output Mask Enable
NC	No External Connect
$\overline{RAS}$	Row-Address Strobe
V_{CC}	Power Supply (3.3 V Typ)
V_{CCQ}	Power Supply for Output Drivers (3.3 V Typ)
V_{SS}	Ground
V_{SSQ}	Ground for Output Drivers
$\overline{W}$	Write Enable

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operation (continued)

Table 1. Basic-Command Truth Table†

COMMAND	STATE OF BANK(S)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	A11	A10	A9–A0	MNEMONIC
Mode register set	T = deac B = deac	L	L	L	L	X	X	A9 = V A8–A7 = 0 A6–A0 = V	MRS
Bank deactivate (precharge)	X	L	L	H	L	BS	L	X	DEAC
Deactivate all banks	X	L	L	H	L	X	H	X	DCAB
Bank activate/row-address entry	SB = deac	L	L	H	H	BS	V	V	ACTV
Column-address entry/write operation	SB = actv	L	H	L	L	BS	L	V	WRT
Column-address entry/write operation with automatic deactivate	SB = actv	L	H	L	L	BS	H	V	WRT-P
Column-address entry/read operation	SB = actv	L	H	L	H	BS	L	V	READ
Column-address entry/read operation with automatic deactivate	SB = actv	L	H	L	H	BS	H	V	READ-P
Burst stop	SB = actv	L	H	H	L	X	X	X	STOP
No operation	X	L	H	H	H	X	X	X	NOOP
Control-input inhibit / no operation	X	H	X	X	X	X	X	X	DESL
Auto-refresh‡	T = deac B = deac	L	L	L	H	X	X	X	REFR

† For exception of these commands on cycle n:
– CKE(n–1) must be high, or
– t_{CESP} must be satisfied for power-down exit, or
– t_{CESP} and t_{RC} must be satisfied for self-refresh exit, or
– t_{CES} and n_{CLE} must be satisfied for clock-suspend exit.
DQM(n) is a don't care.

‡ Auto-refresh or self-refresh entry requires that all banks be deactivated or in an idle state prior to the command entry.

Legend:

n	=	CLK cycle number
L	=	Logic low
H	=	Logic high
X	=	Don't care, either logic low or logic high
V	=	Valid
T	=	Bank T
B	=	Bank B
actv	=	Activated
deac	=	Deactivated
BS	=	Logic high to select bank T; logic low to select bank B
SB	=	Bank selected by A11 at cycle n

operation (continued)

Table 3. DQM-Use Command Truth Table†

COMMAND	STATE OF BANK(S)	DQM (n)	DATA IN (n)	DATA OUT (n+2)	MNEMONIC
—	T = deac and B = deac	X	N/A	Hi-Z	—
—	T = actv and B = actv (no access operation)‡	X	N/A	Hi-Z	—
Data-in enable	T = write or B = write	L	V	N/A	ENBL
Data-in mask	T = write or B = write	H	M	N/A	MASK
Data-out enable	T = read or B = read	L	N/A	V	ENBL
Data-out mask	T = read or B = read	H	N/A	Hi-Z	MASK

† For exception of these commands on cycle n:
– CKE(n–1) must be high, or
– t_{CESP} must be satisfied for power-down exit, or
– t_{CESP} and t_{RC} must be satisfied for self-refresh exit, or
– t_{CES} and n_{CLE} must be satisfied for clock-suspend exit.
$\overline{CS}$(n), $\overline{RAS}$(n), $\overline{CAS}$(n), $\overline{W}$(n), and A0–A11(n) are don't cares

‡ A bank is no longer in an access operation one cycle after the last data-out cycle of a read operation, and two cycles after the last data-in cycle of a write operation. Neither the PDE nor the HOLD command is allowed on the cycle immediately following the last data-in cycle of a write operation.

Legend:

n	=	CLK cycle number
L	=	Logic low
H	=	Logic high
X	=	Don't care, either logic low or logic high
V	=	Valid
M	=	Masked input data
N/A	=	Not applicable
T	=	Bank T
B	=	Bank B
actv	=	Activated
deac	=	Deactivated
write	=	Activated and accepting data in on cycle n
read	=	Activated and delivering data out on cycle (n + 2)

burst sequence (continued)

Table 6. 8-Bit Burst Sequences

	INTERNAL COLUMN ADDRESS A2–A0															
	DECIMAL								BINARY							
	START	2ND	3RD	4TH	5TH	6TH	7TH	8TH	START	2ND	3RD	4TH	5TH	6TH	7TH	8TH
Serial	0	1	2	3	4	5	6	7	000	001	010	011	100	101	110	111
	1	2	3	4	5	6	7	0	001	010	011	100	101	110	111	000
	2	3	4	5	6	7	0	1	010	011	100	101	110	111	000	001
	3	4	5	6	7	0	1	2	011	100	101	110	111	000	001	010
	4	5	6	7	0	1	2	3	100	101	110	111	000	001	010	011
	5	6	7	0	1	2	3	4	101	110	111	000	001	010	011	100
	6	7	0	1	2	3	4	5	110	111	000	001	010	011	100	101
	7	0	1	2	3	4	5	6	111	000	001	010	011	100	101	110
Interleave	0	1	2	3	4	5	6	7	000	001	010	011	100	101	110	111
	1	0	3	2	5	4	7	6	001	000	011	010	101	100	111	110
	2	3	0	1	6	7	4	5	010	011	000	001	110	111	100	101
	3	2	1	0	7	6	5	4	011	010	001	000	111	110	101	100
	4	5	6	7	0	1	2	3	100	101	110	111	000	001	010	011
	5	4	7	6	1	0	3	2	101	100	111	110	001	000	011	010
	6	7	4	5	2	3	0	1	110	111	100	101	010	011	000	001
	7	6	5	4	3	2	1	0	111	110	101	100	011	010	001	000

latency

The beginning data-out cycle of a read burst can be programmed to occur 1, 2, or 3 CLK cycles after the read command (see the section on setting the mode register, page 5–59). This feature allows the user to adjust the '626812 to operate in accordance with the system's capability to latch the data output from the '626812. The delay between the READ command and the beginning of the output burst is known as read latency (also known as $\overline{CAS}$ latency). After the initial output cycle begins, the data burst occurs at the CLK frequency without any intervening gaps. Use of minimum read latencies is restricted based on the particular maximum frequency rating of the '626812.

There is no latency for data-in cycles (write latency). The first data-in cycle of a write burst is entered at the same rising edge of CLK on which the WRT command is entered. The write latency is fixed and is not determined by the mode-register contents.

two-bank operation

The '626812 contains two independent banks that can be accessed individually or in an interleaved fashion. Each bank must be activated with a row address before it can be accessed. Each bank must then be deactivated before it can be activated again with a new row address. The bank-activate/row-address-entry command (ACTV) is entered by holding $\overline{RAS}$ low, $\overline{CAS}$ high, $\overline{W}$ high, and A11 valid on the rising edge of CLK. A bank can be deactivated either automatically during a READ-P or a WRT-P command or by use of the deactivate-bank (DEAC) command. Both banks can be deactivated at once by use of the DCAB command (see Table 1 and the section on bank deactivation description, page 5–58).

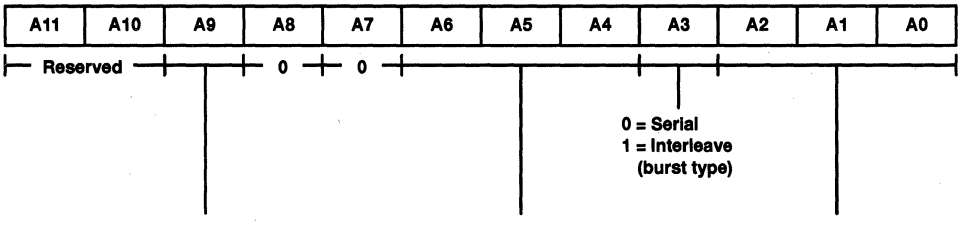
CLK suspend/power-down mode (continued)

as a CLK-suspend operation, and its execution is denoted as a HOLD command. The device resumes operation from the point at which it was placed in suspension, beginning with the second rising edge of CLK after CKE returns high.

If CKE is brought low when no read or write command is in progress, the device enters power-down mode. If both banks are deactivated when power-down mode is entered, power consumption is reduced to the minimum. Power-down mode can be used during row-active or auto-refresh periods to reduce input buffer power. After power-down mode is entered, no further inputs are accepted until CKE returns high. To ensure that data in the device remains valid during the power-down mode, the self-refresh command (SLFR) must be executed concurrently with the power-down entry (PDE) command. When exiting power-down mode, new commands can be entered on the first CLK edge after CKE returns high, provided that the setup time (t_{CESP}) is satisfied. Table 2 shows the command configuration for a CLK suspend/power-down operation, and Figure 19, Figure 20, and Figure 38 show an example of the procedure.

setting the mode register

The '626812 contains a mode register that must be programmed with the read latency, the burst type, and the burst length. This is accomplished by executing a mode-register set (MRS) command with the information entered on address lines A0–A9. A logic 0 must be entered on A7 and A8, but A10 and A11 are don't-care entries for the '626812. When A9=1, the write-burst length is always 1. When A9=0, the write-burst length is defined by A0–A2. Figure 1 shows the valid combinations for a successful MRS command. Only valid addresses allow the mode register to be changed. If the addresses are not valid, the previous contents of the mode register remain unaffected. The MRS command is executed by holding $\overline{RAS}$, $\overline{CAS}$, and $\overline{W}$ low, and the input-mode word valid on A0–A9 on the rising edge of CLK (see Table 1). The MRS command can be executed only when both banks are deactivated.



REGISTER BIT A9	WRITE-BURST LENGTH
0	A2–A0
1	1

REGISTER BITS†			READ LATENCY‡
A6	A5	A4	
0	0	1	1
0	1	0	2
0	1	1	3

† All other combinations are reserved.
‡ Refer to timing requirements for minimum valid-read latencies based on maximum frequency rating.

REGISTER BITS§			BURST LENGTH
A2	A1	A0	
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8

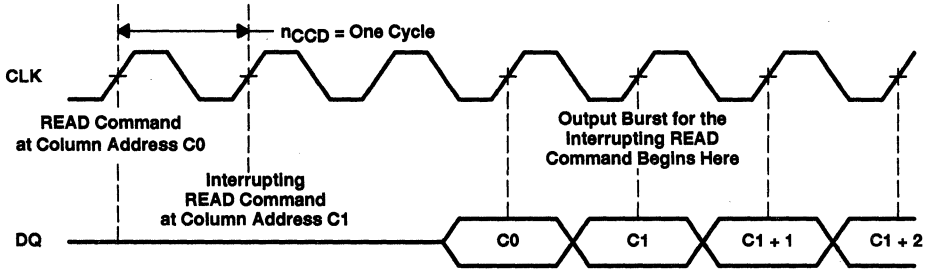
§ All other combinations are reserved.

Figure 1. Mode-Register Programming

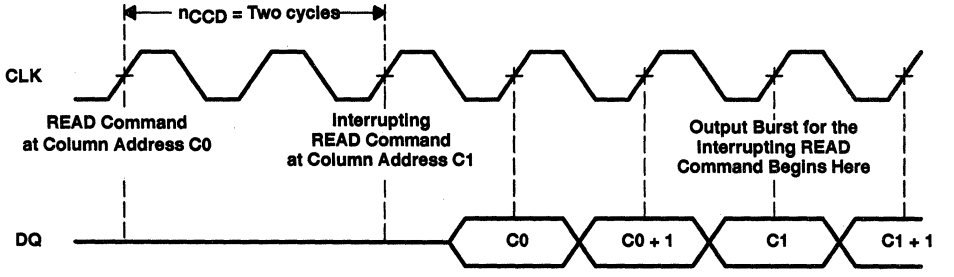
interrupted bursts (continued)

Table 7. Read-Burst Interruption

INTERRUPTING COMMAND	EFFECT OR NOTE ON USE DURING READ BURST
READ, READ-P	Current output cycles continue until the programmed latency from the superseding READ (READ-P) command is met and new output cycles begin (see Figure 2).
WRT, WRT-P	The WRT (WRT-P) command immediately supersedes the read burst in progress. To avoid data contention, DQM must be high before the WRT (WRT-P) command to mask output of the read burst on cycles (n_{CCD}–1), n_{CCD}, and (n_{CCD}+1) assuming that there is any output on these cycles. For read latency = 1, read burst interruption by WRT (WRT-P) command is not allowed at n_{CCD} = 1, 2 (see Figure 3).
DEAC, DCAB	The DQ bus is in the high-impedance state when n_{HZP} cycles are satisfied or when the read burst completes, whichever occurs first (see Figure 4).
STOP	The DQ bus is in the high-impedance state when n_{BSD} cycles are satisfied or when the read burst completes, whichever occurs first. The bank remains active. A new read or write command cannot be entered for at least two cycles after the STOP command (see Figure 5).



a) INTERRUPTED ON ODD CYCLES



b) INTERRUPTED ON EVEN CYCLES

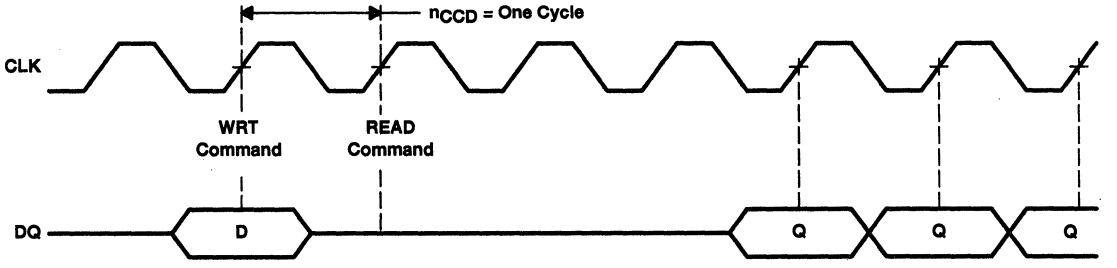
NOTE A: For these examples assume read latency = 3, and burst length = 4.

Figure 2. Read Burst Interrupted by Read Command

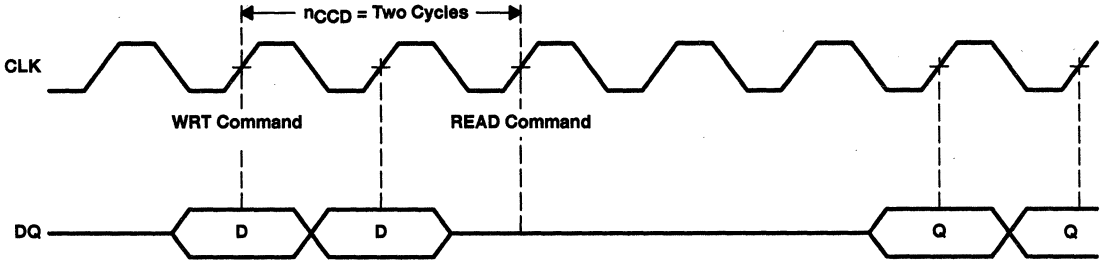
interrupted bursts (continued)

Table 8. Write-Burst Interruption

INTERRUPTING COMMAND	EFFECT OR NOTE ON USE DURING WRITE BURST
READ, READ-P	Data in on previous cycle is written. No further data in is accepted (see Figure 6).
WRT, WRT-P	The new WRT (WRT-P) command and data in immediately supersede the write burst in progress (see Figure 7).
DEAC, DCAB	The DEAC/DCAB command immediately supersedes the write burst in progress. DQM must be used to mask the DQ bus such that the write recovery specification (t_{RWL}) is not violated by the interrupt (see Figure 8).
STOP	The data on the input pins at the time of the burst STOP command is not written, and no further data is accepted. The bank remains active. A new read or write command cannot be entered for at least n_{BSD} cycles after the STOP command (see Figure 9).



a) INTERRUPTED ON ODD CYCLES

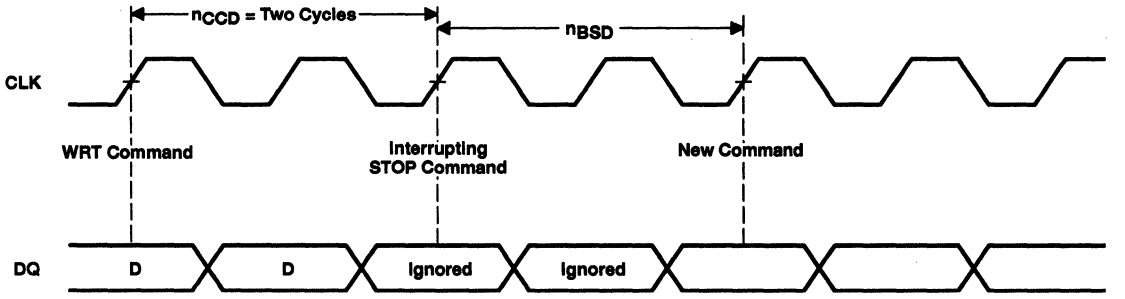


b) INTERRUPTED ON EVEN CYCLES

NOTE A: For these examples assume read latency = 3, burst length = 4.

Figure 6. Write Burst Interrupted by Read Command

interrupted bursts (continued)



NOTE A: For this example assume burst length = 4.

Figure 9. Write Burst Interrupted by STOP Command

power up

Device initialization should be performed after a power up to the full V_{CC} level. After power is established, a 200-µs interval is required (with no inputs other than CLK). After this interval, both banks of the device must be deactivated. Eight REFR commands must be performed, and the mode register must be set to complete the device initialization.

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (see Note 2)

PARAMETER		TEST CONDITIONS			'626812-12A		'626812-12		'626812-15		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = –2 mA			2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA				0.4		0.4		0.4	V
I_I	Input current (leakage)	0 V ≤ V_I ≤ V_{CC} + 0.3 V, All other pins = 0 V to V_{CC}				±10		±10		±10	µA
I_O	Output current (leakage)	0 V ≤ V_O ≤ V_{CC} + 0.3 V, Output disabled				±10		±10		±10	µA
I_{CC1}	Average read or write current	t_{RC} = MIN, t_{CK} = MIN, Read latency = 3	One bank active	Burst length = 1 or 2		85		85		75	mA
				Burst length = 4 or 8		105		105		90	
			Two banks active interleaving	Burst length = 1 or 2		140		140		120	
				Burst length = 4 or 8		165		165		135	
I_{CC2}	Standby current	Both banks deactivated	CKE = V_{IH}			25		25		20	mA
			CKE = V_{IL}			2		2		2	
			CKE = 0 V (CMOS)			1		1		1	
		1 or 2 banks active	CKE = V_{IH}			30		30		25	mA
			CKE = V_{IL}			8		8		8	
I_{CC3}	Consecutive CBR commands	t_{RC} = MIN				80		80		70	mA
I_{CC4}	Burst current, gapless burst	ACTV not allowed, Two bank interleaved, t_{CK} = MIN,		Read latency = 1		60		60		50	mA
				Read latency = 2		120		100		90	
				Read latency = 3		140		140		120	
I_{CC6}	Self-refresh current	CKE = V_{IL}				2		2		2	mA
		CKE = 0 V (CMOS)				1		1		1	

NOTE 2: All specifications apply to the device after power-up initialization. All control and address inputs must be stable and valid.

ac timing requirements over recommended ranges of supply voltage and operating free-air temperature†‡

		'626812-12A		'626812-12		'626812-15		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RAS}	ACTV command to DEAC or DCAB command	60	100 000	72	100 000	75	100 000	ns
t_{RCD}	ACTV command to READ or WRT command (see Note 8)	30		30		30		ns
t_{RP}	DEAC or DCAB command to ACTV, MRS, SLFR, or REFR command	36		36		45		ns
t_{APR}	Final data out of READ-P operation to ACTV, MRS, SLFR, or REFR command	$t_{RP} + (n_{EP} + t_{CK})$						ns
t_{APW}	Final data in of WRT-P operation to ACTV, MRS, SLFR, or REFR command	60		60		75		ns
t_{RWL}	Final data in to DEAC or DCAB command	18		20		30		ns
t_{RRD}	ACTV command for one bank to ACTV command for the other bank	24		24		30		ns
t_T	Transition time, all inputs (see Note 9)	1	5	1	5	1	5	ns
t_{REF}	Refresh interval		64		64		64	ms

† See Parameter Measurement Information for load circuits.
‡ All references are made to the rising transition of CLK, unless otherwise noted.
NOTES: 8. For read or write operations with automatic deactivate, t_{RCD} must be set to satisfy minimum t_{RAS}.
9. Transition time, t_T, is measured between V_{IH} and V_{IL}.

Table 9. Number of Cycles Required to Meet Minimum Specification for Key Timing Parameters

			TMS626812-12A			TMS626812-12			TMS626812-15			UNITS
	Operating frequency		83	66	50	83	66	50	66	50	33	MHz
t_{CK}	Cycle time, CLK (system clock)		12	15	20	12	15	20	15	20	30	ns
	KEY PARAMETER		**NUMBER OF CYCLES REQUIRED**									
	Read latency, minimum programmed value		3	2	2	3	3	2	3	2	2	cycles
t_{RCD}	ACTV command to READ or WRT command		3	2	2	3	2	2	2	2	1	cycles
t_{RAS}	ACTV command to DEAC or DCAB command		5	4	3	6	5	4	5	4	3	cycles
t_{RP}	DEAC or DCAB command to ACTV, MRS, SLFR, or REFR command		3	3	2	3	3	2	3	3	2	cycles
t_{RC}	REFR command to ACTV, MRS, or REFR command; self-refresh exit to ACTV, MRS, SLFR, or REFR command		8	7	5	9	8	6	8	6	4	cycles
t_{RWL}	Final data in to DEAC or DCAB command		2	2	1	3	2	1	2	2	1	cycles
t_{RRD}	ACTV command for one bank to ACTV command for the other bank		2	2	2	2	2	2	2	2	1	cycles
t_{APR}	Final data out of READ-P operation to ACTV, MRS, SLFR, or REFR command	Read latency = 1	—	—	—	—	—	—	—	—	—	cycles
		Read latency = 2	—	2	1	—	—	1	—	2	1	cycles
		Read latency = 3	1	1	0	1	1	0	1	1	0	cycles
t_{APW}	Final data in of WRT-P operation to ACTV, MRS, SLFR, or REFR command		5	4	3	5	4	3	5	4	3	cycles

† All references are made to the rising transition of CLK, unless otherwise noted.

PARAMETER MEASUREMENT INFORMATION

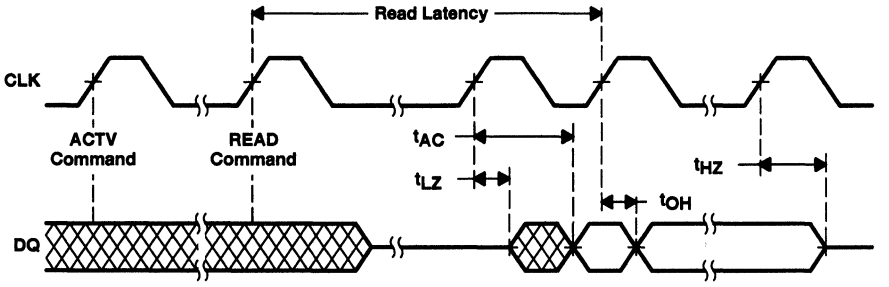


Figure 12. Output Parameters

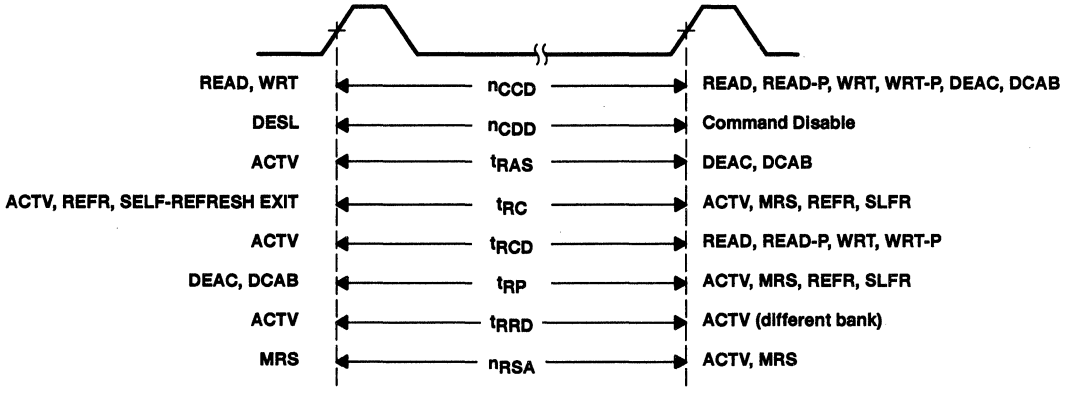


Figure 13. Command-to-Command Parameters

PARAMETER MEASUREMENT INFORMATION

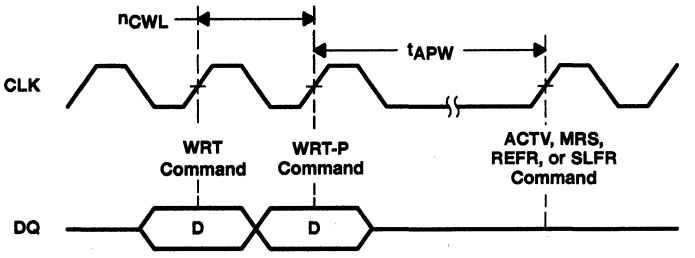
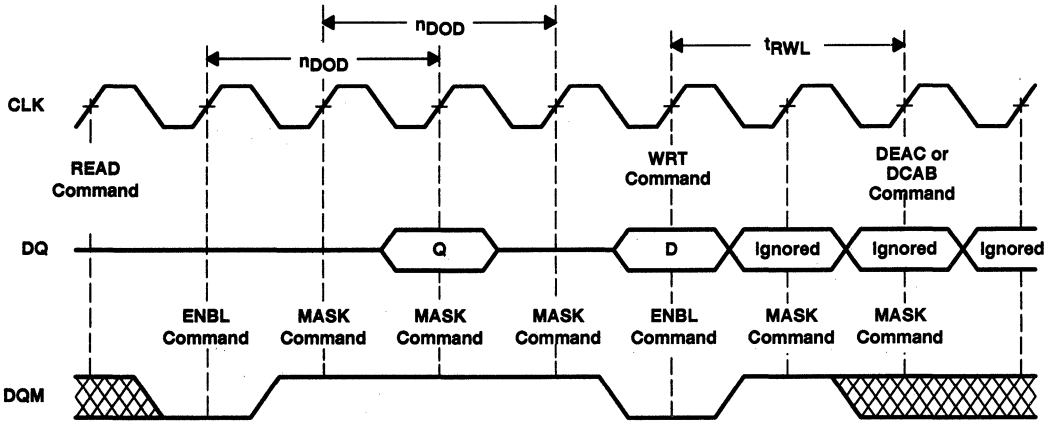


Figure 17. Write With Auto-Deactivate



NOTE A: For this example assume read latency = 3, and burst length = 4.

Figure 18. DQ Masking

PARAMETER MEASUREMENT INFORMATION

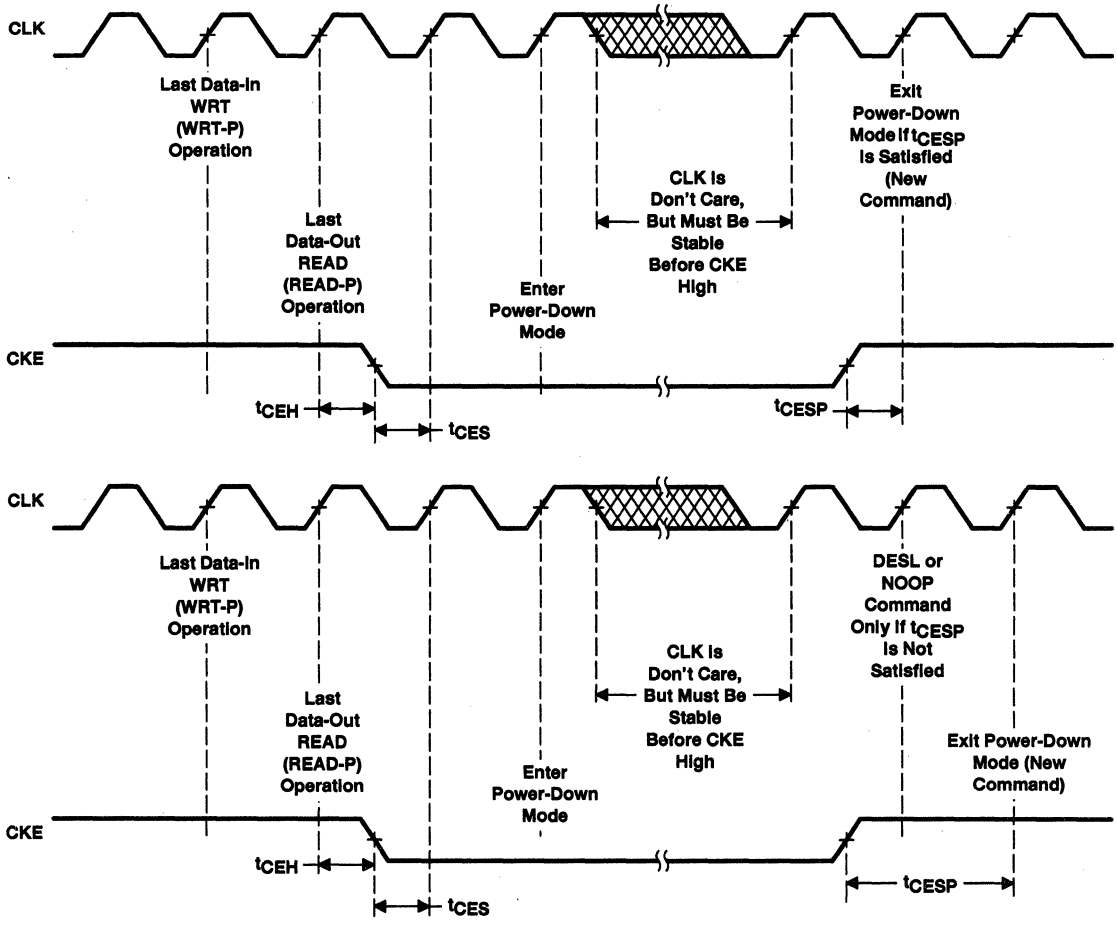
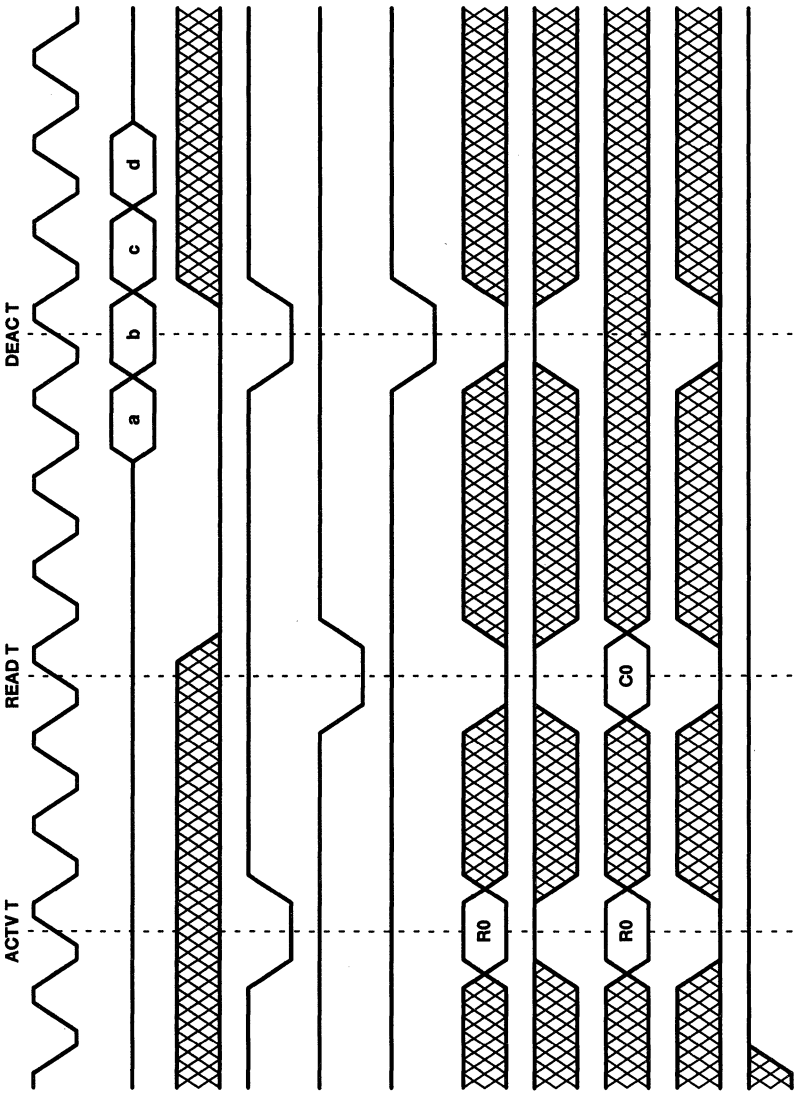


Figure 20. Power-Down Operation

PARAMETER MEASUREMENT INFORMATION

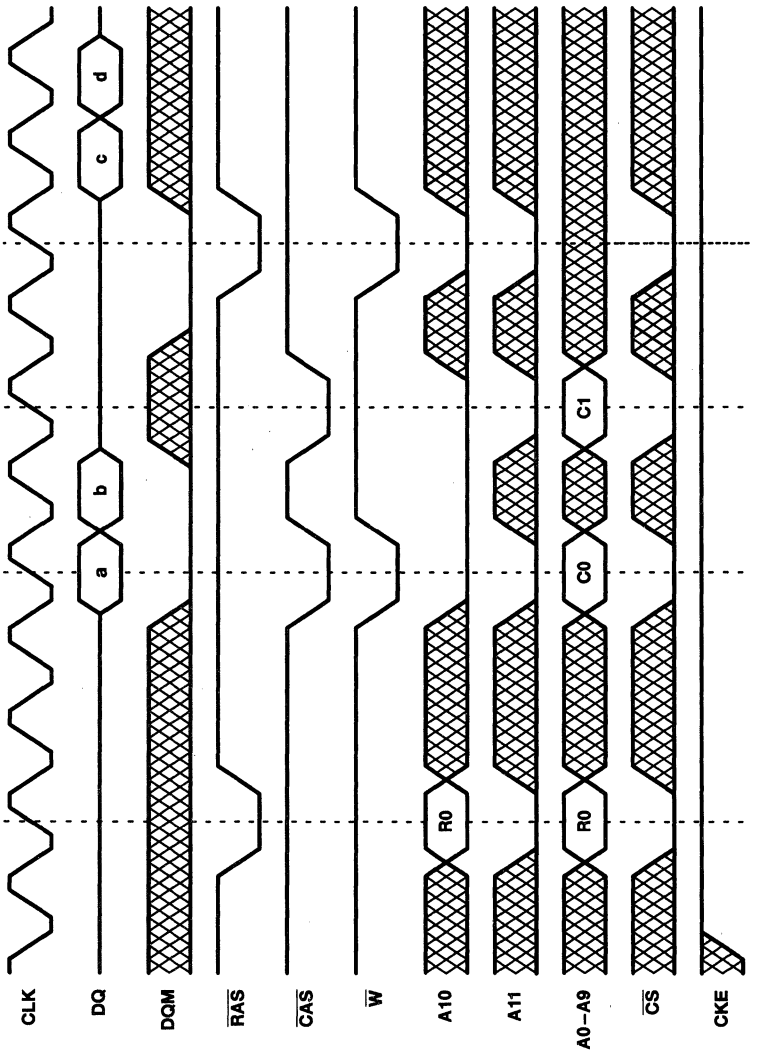


BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d
Q	T	R0	C0	C0 + 1	C0 + 2	C0 + 3

† Column-address sequence depends on programmed burst type and starting column address C0 (see Table 5).
NOTE A: This example illustrates minimum t_{RCD} and n_{EP} for the '626812-12 at 83 MHz.

Figure 22. Read Burst (read latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION

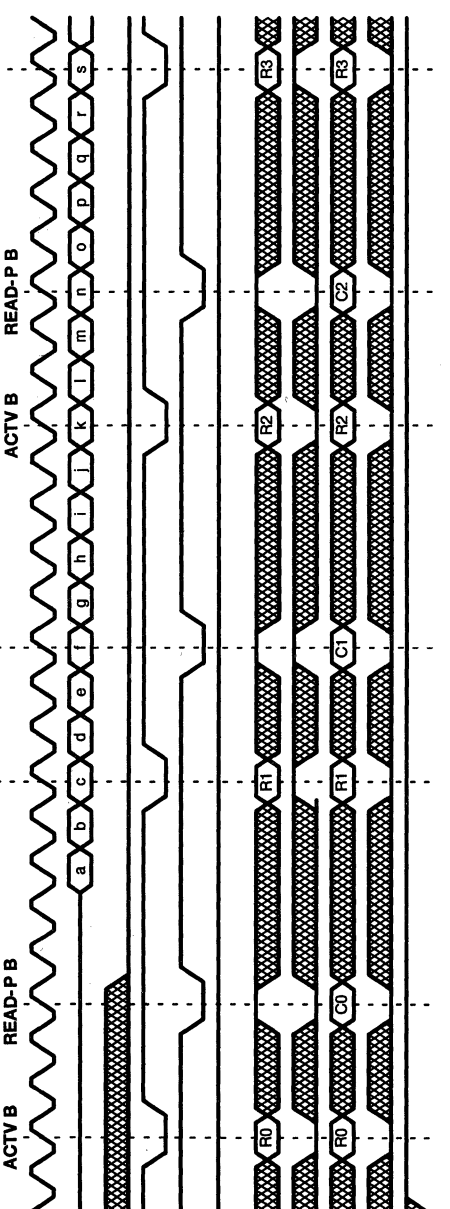


BURST TYPE	BANK	ROW	BURST CYCLE†			
(D/Q)	(B/T)	ADDR	a	b	c	d
D	B	R0	C0	C0 + 1		
Q	B	R0			C1‡	C1 + 1

† Column-address sequence depends on programmed burst type and starting column address C0 and C1 (see Table 4).
NOTE A: This example illustrates minimum t_{RCD}, n_{CWL}, and n_{EP} for the '626812-12 at 83 MHz.

Figure 24. Write-Read Burst (read latency = 3, burst length = 2)

PARAMETER MEASUREMENT INFORMATION

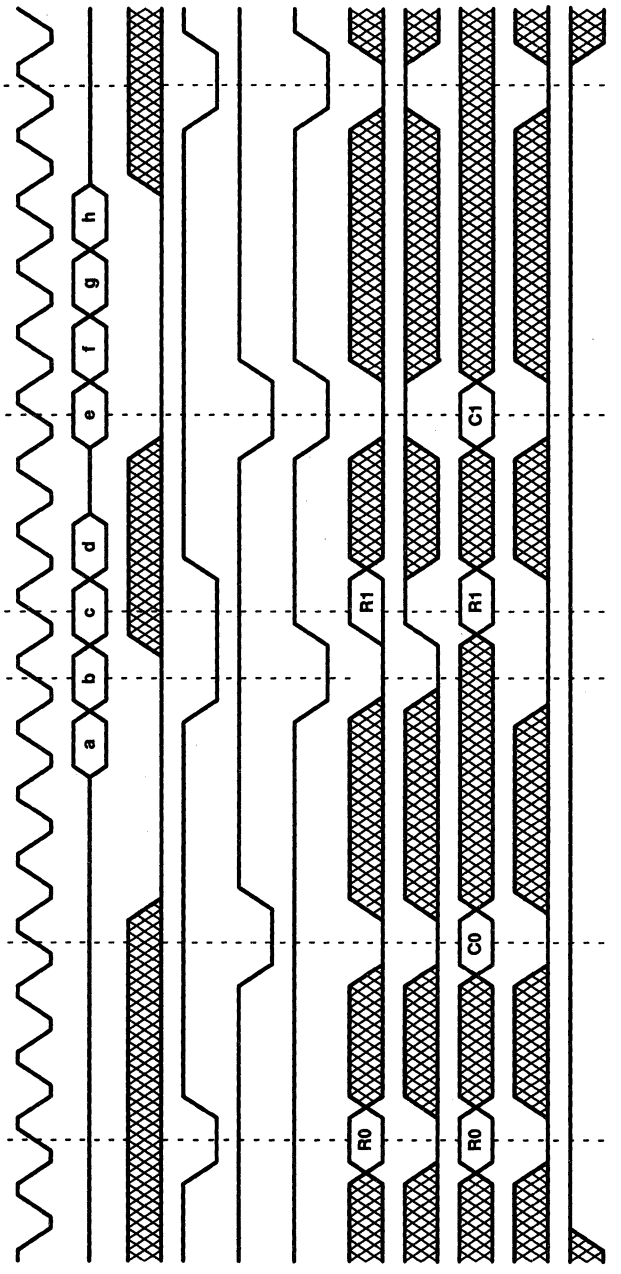


BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	. .
Q	B	R0	C0	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7												
Q	T	R1									C1	C1+1	C1+2	C1+3	C1+4	C1+5	C1+6	C1+7				
Q	B	R2																	C2	C2+1	C2+2	. .

† Column-address sequence depends on programmed burst type and starting column address C0, C1, and C2 (see Table 6).
NOTE A: This example illustrates minimum t_{RCD} for the '626812-12 at 83 MHz.

Figure 26. Two-Bank Row-Interleaving Read Bursts With Automatic Deactivate (read latency = 3, burst length = 8)

PARAMETER MEASUREMENT INFORMATION



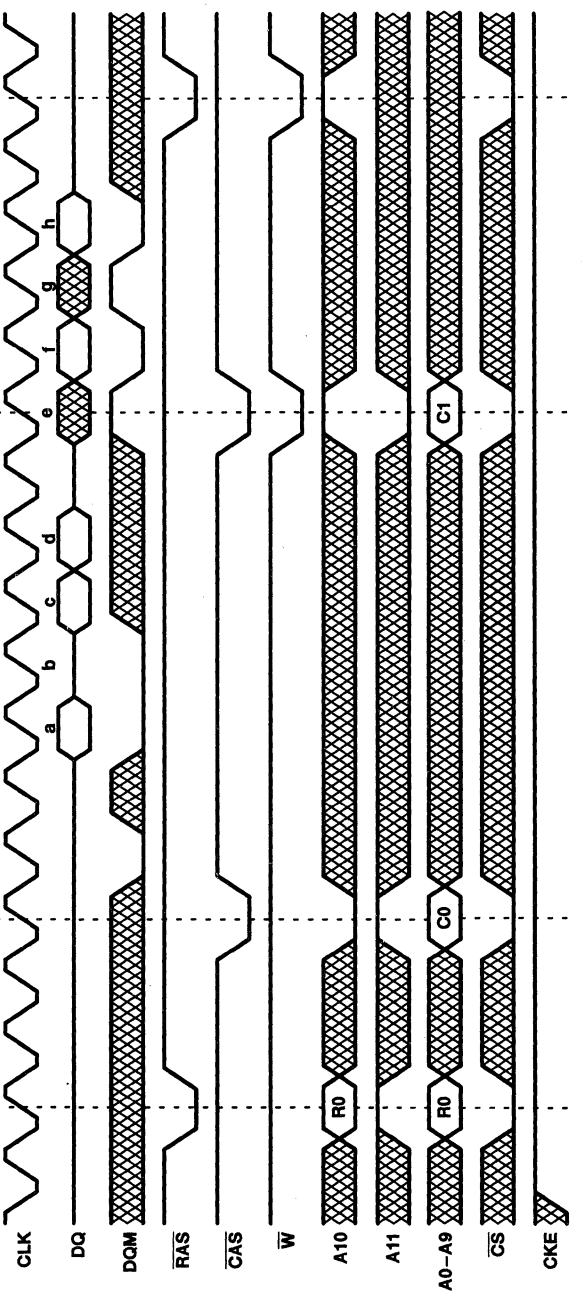
BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d	e	f	g	h
Q	B	R0	C0	C0 + 1	C0 + 2	C0 + 3				
D	T	R1					C1	C1 + 1	C1 + 2	C1 + 3

† Column-address sequence depends on programmed burst type and starting column addresses C0 and C1. (see Table 5).

NOTE A: This example illustrates a minimum t_{RCD}, n_{EP}, and t_{RWL} for the '626812-12 at 83 MHz.

Figure 28. Read-Burst Bank B, Write-Burst Bank T (read latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION

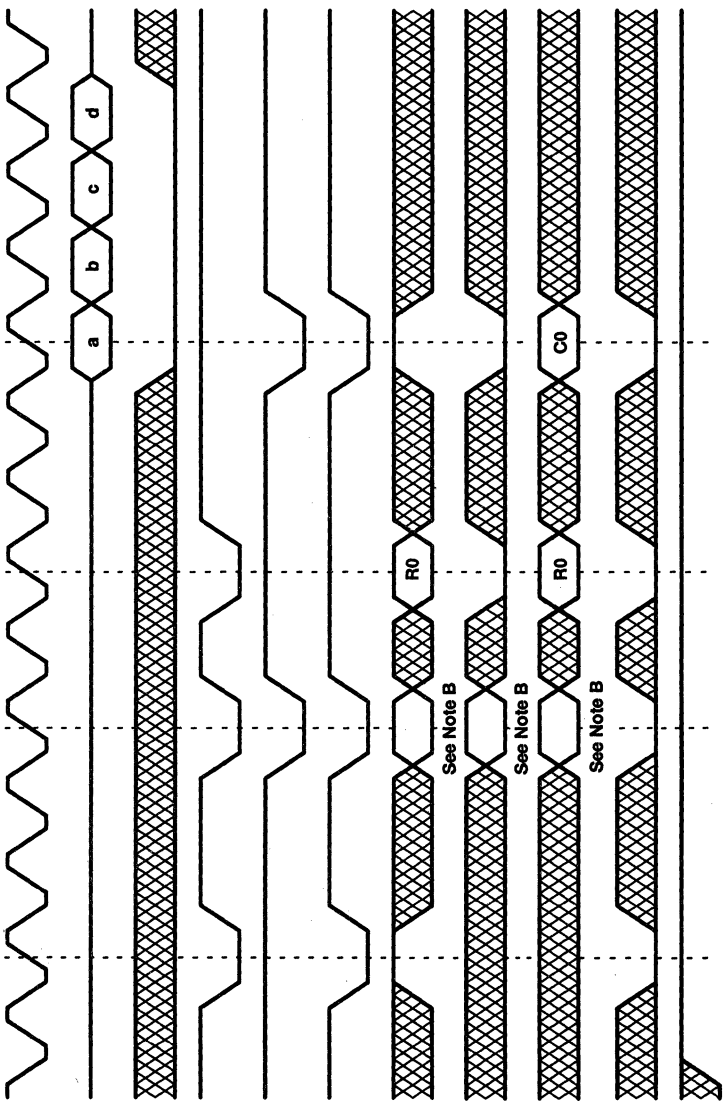


BURST TYPE	BANK	ROW	BURST CYCLE†							
(D/Q)	(B/T)	ADDR	a	b	c	d	e	f	g	h
Q	T	R0	C0	C0+1	C0+2	C0+3				
D	T	R1					C1	C1+1	C1+2	C1+3

† Column-address sequence depends on programmed burst type and starting column address C0 and C1 (see Table 5).
NOTE A: This example illustrates minimum t_{RCD} for the '626812-12 at 83 MHz.

Figure 30. Data Mask (read latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION



BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE† a	b	c	d
D	B	R0	C0	C0+1	C0+2	C0+3

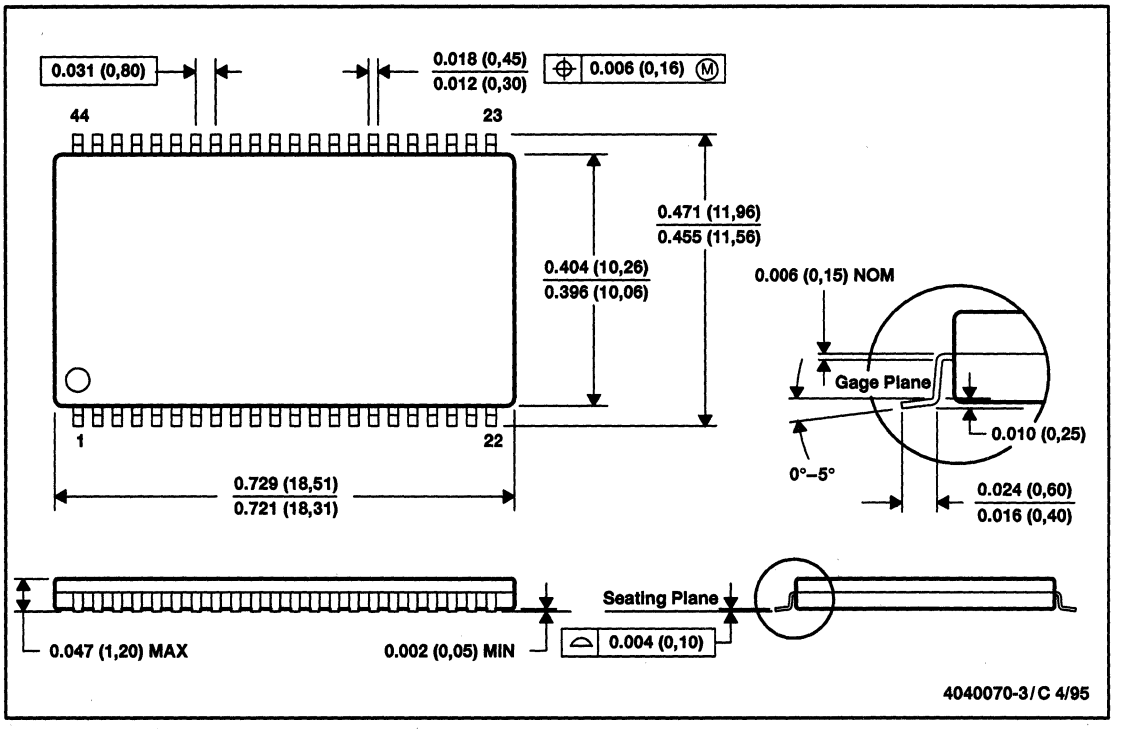
† Column-address sequence depends on programmed burst type and starting column address C0 (see Table 5).

NOTES: A. This example illustrates minimum t_{RP}, n_{RSA}, and t_{RCD} for the 626812-12 at 83 MHz.
B. Refer to Figure 1

Figure 32. Set Mode Register (deactivate all, set mode register, write burst with automatic deactivate) (burst length = 4)

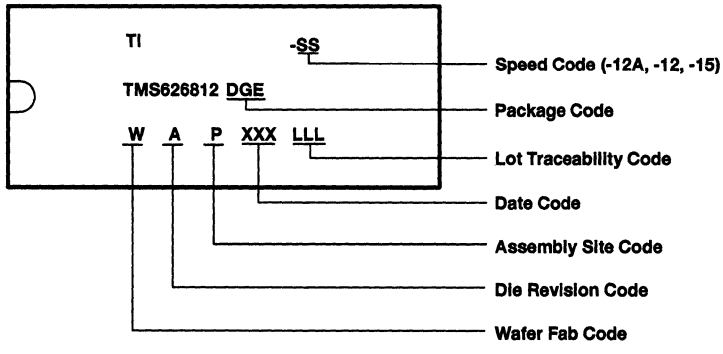
MECHANICAL DATA

DGE (R-PDSO-G44) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

device symbolization



- Organization . . . 1M x 16 x 4 Banks
  2M x 8 x 4 Banks
  4M x 4 x 4 Banks
- 3.3-V Power Supply (±10% Tolerance)
- Four Banks for On-Chip Interleaving for x4/x8/x16 (Gapless Access) Depending on Organizations
- High Bandwidth – Up to 100-MHz Data Rates
- Burst Length Programmable to 1, 2, 4, 8, or Full Page
- Programmable Output Sequence – Serial or Interleave
- Chip Select and Clock Enable for Enhanced-System Interfacing
- Cycle-by-Cycle DQ Bus Mask Capability
- Only x16 SDRAM Configuration Supports Upper-/Lower-Byte Masking Control
- Programmable Read Latency From Column Address
- Pipeline Architecture (Single-Cycle Architecture)
- Single Write/Read Burst
- Self-Refresh Capability (every 16 μs)
- High-Speed, Low-Noise Low-Voltage Transistor-Transistor Logic (LVTTL) Interface
- Power-Down Mode
- Compatible With JEDEC Standards
- 16K $\overline{\text{RAS}}$-Only Refresh (Total for All Banks)
- 4K Auto Refresh (Total for All Banks)/64 ms
- Automatic Precharge and Controlled Precharge
- Burst Interruptions Supported
  - Read Interruption
  - Write Interruption
  - Stop Interruption
  - Precharge Interruption
- Support Clock-Suspend Operation (Hold Command)
- Performance Ranges:

	SYNCHRONOUS CLOCK CYCLE TIME	ACTV COMMAND TO READ OR WRT COMMAND	REFRESH TIME INTERVAL
	t_{CK} (MIN)	t_{RCD} (MIN)	t_{REF} (MAX)
'664xx4-10	10 ns	30 ns	64 ms
'664xx4-12	12 ns	35 ns	64 ms

PRODUCT PREVIEW

description

The TMS664xx4 series are high-speed, 67 108 864-bit synchronous dynamic random-access memories (SDRAMs), which are organized as follows:

- Four banks of 1 048 576 words with 16 bits per word
- Four banks of 2 097 152 words with 8 bits per word
- Four banks of 4 194 304 words with 4 bits per word

All inputs and outputs of the TMS664xx4 series are compatible with the LVTTL interface.

The SDRAM employs state-of-the-art enhanced performance implanted CMOS (EPIC™) technology for high-performance, reliability, and low power. All inputs and outputs are synchonized with the CLK input to simplify system design and to enhance use with high-speed microprocessors and caches.

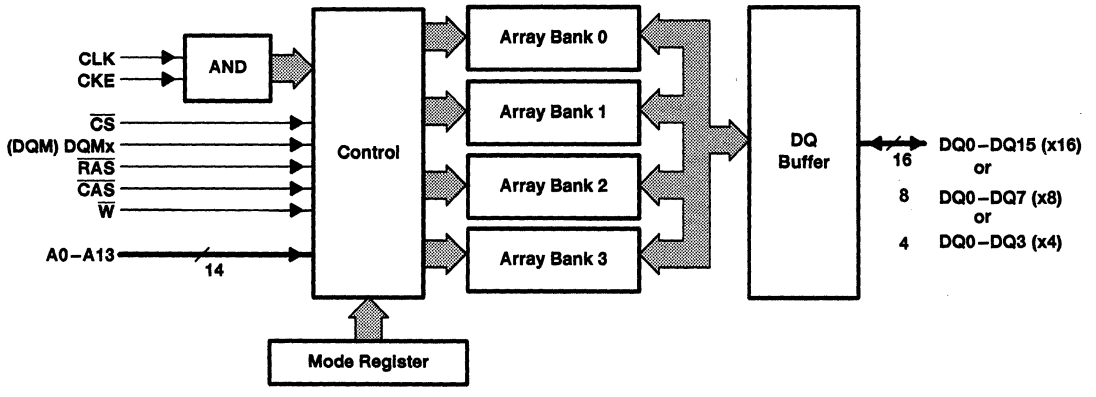
The TMS664xx4 SDRAM is available in a 400-mil, 54-pin surface-mount thin small-outline package (TSOP) (II) (DGE suffix).

EPIC is a trademark of Texas Instruments Incorporated.

PIN NOMENCLATURE

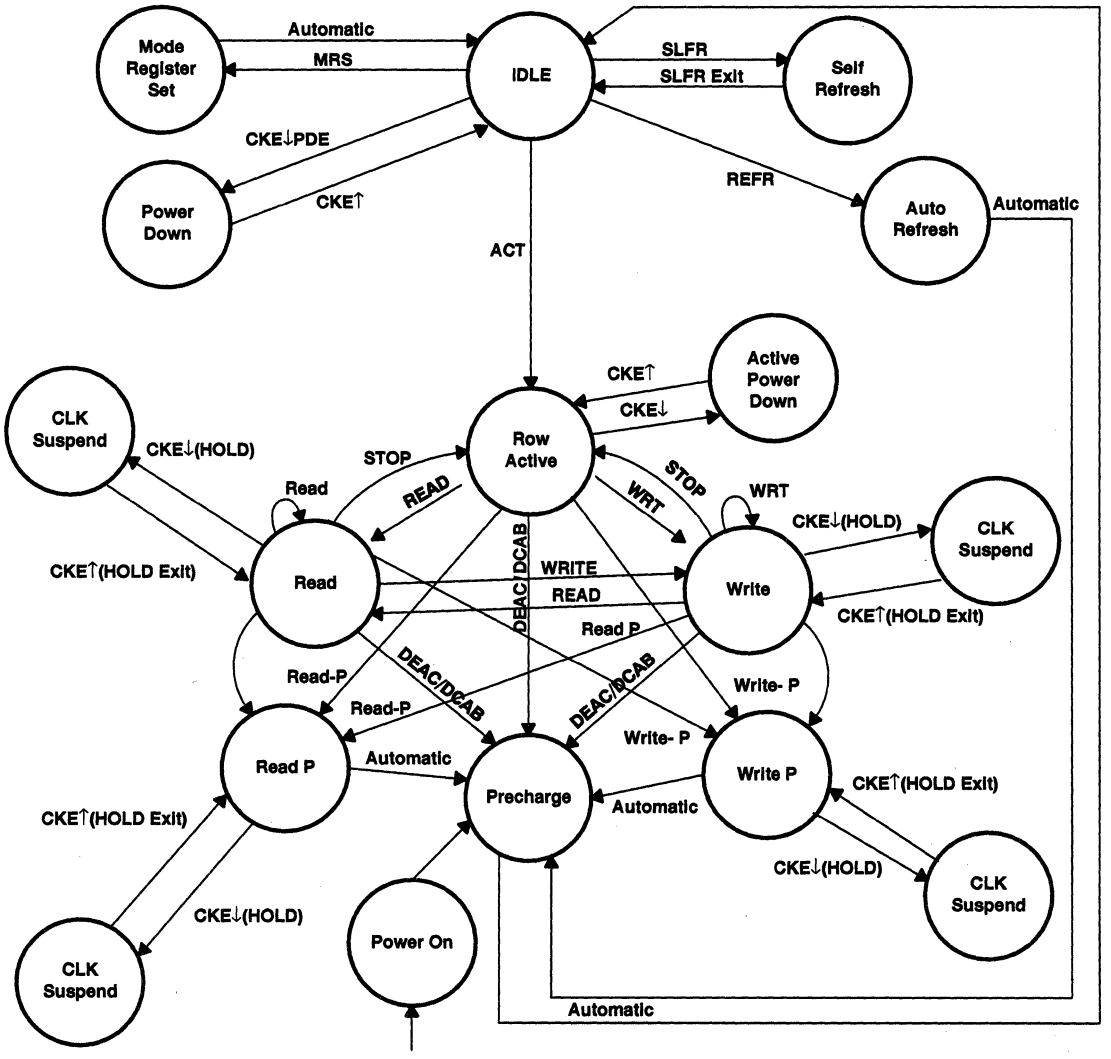
A0 – A13	Address Inputs Four Banks Column A0 –A9 Column Addr (x4) A0 –A8 Column Addr (x8) A0 –A7 Column Addr (x16) A10 Auto Precharge A12 – A13 Bank Select Row A0 – A11 Row Addrs A12 – A13 Bank Select
$\overline{CAS}$	Column-Address Strobe
CKE	Clock Enable
CLK	System Clock
$\overline{CS}$	Chip Select
DQ0–DQ3	SDRAM Data Input/Data Output (x4)
DQ0–DQ7	SDRAM Data Input/Data Output (x8)
DQ0–DQ15	SDRAM Data Input/Data Output (x16)
DQMU/DQML	Data/Output Mask Enables for x16
DQM	Data/Output Mask Enables for x4 and x8
NC	No External Connect
$\overline{RAS}$	Row-Address Strobe
V_{CC}	Power Supply (3.3 V Typ)
V_{CCQ}	Power Supply for Output Drivers (3.3 V Typ)
V_{SS}	Ground
V_{SSQ}	Ground for Output Drivers
$\overline{W}$	Write Enable

functional block diagram (four banks)



PRODUCT PREVIEW

state diagram



PRODUCT PREVIEW

operation (continued)

Table 2. CKE-Use Command Truth Table†

COMMAND	STATE OF BANK(S)	CKE (n−1)	CKE (n)	$\overline{CS}$ (n)	$\overline{RAS}$ (n)	$\overline{CAS}$ (n)	$\overline{W}$ (n)	MNEMONIC
Self-refresh entry	All Banks = deac	H	L	L	L	L	H	SLFR
Power-down entry at n + 1‡	All Banks = no access operation§	H	L	X	X	X	X	PDE
Self-refresh exit	All Banks = self-refresh	L	H	L	H	H	H	—
		L	H	H	X	X	X	—
Power-down exit¶	All Banks = power down	L	H	X	X	X	X	—
CLK suspend at n+1	All Banks = access operation§	H	L	X	X	X	X	HOLD
CLK suspend exit at n+1	All Banks = access operation§	L	H	X	X	X	X	—

† For execution of these commands, A0–A13 (n) and DQMx (n) are don't cares.
‡ On cycle n, the device executes the respective command (listed in Table 1). On cycle (n+1), the device enters the power-down mode.
§ A bank is no longer in an access operation one cycle after the last data-out cycle of a READ (READ-P) operation, and two cycles after the last data-in cycle of a WRT (WRT-P) operation. Neither the PDE nor the HOLD command is allowed on the cycle immediately following the last data-in cycle of a WRT (WRT-P) operation.
¶ If setup time from CKE high to the next CLK high satisfies t_{CESP}, the device executes the respective command (listed in Table 1). Otherwise, either DESL or NOOP command must be applied before any other command.

Legend:
n = CLK cycle number
L = Logic low
H = Logic high
X = Don't care (either logic high or logic low)
deac = Deactivated

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burst sequence

All data for the '664xx4 is written or read in a *burst* fashion. That is, a single starting address is entered into the device and then the '664xx4 internally accesses a sequence of locations based on that starting address. Some of the subsequent accesses after the first one can be at preceding, as well as succeeding, column addresses, depending on the starting address entered. This sequence can be programmed to follow either a serial burst or an interleave burst (see Table 4 through Table 6). The length of the burst sequence can be user-programmed to be 1, 2, 4, 8, or full page [256 (x16), 512 (x8), 1024 (x4)] accesses. After a read burst is completed (as determined by the programmed burst length), the outputs are in the high-impedance state until the next read access is initiated.

Table 4. 2-Bit Burst Sequences

	INTERNAL COLUMN ADDRESS A0			
	DECIMAL		BINARY	
	START	2ND	START	2ND
Serial	0	1	0	1
	1	0	1	0
Interleave	0	1	0	1
	1	0	1	0

Table 5. 4-Bit Burst Sequences

	INTERNAL COLUMN ADDRESS A1–A0							
	DECIMAL				BINARY			
	START	2ND	3RD	4TH	START	2ND	3RD	4TH
Serial	0	1	2	3	00	01	10	11
	1	2	3	0	01	10	11	00
	2	3	0	1	10	11	00	01
	3	0	1	2	11	00	01	10
Interleave	0	1	2	3	00	01	10	11
	1	0	3	2	01	00	11	10
	2	3	0	1	10	11	00	01
	3	2	1	0	11	10	01	00

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four-bank row-access operation

One of the features of the four-bank operation is access to information on random rows at a higher rate of operation than is possible with a standard DRAM. This can be accomplished by activating one of the banks with a row address and, while the data stream is being accessed to/from that bank, activating one of the other banks with other row addresses. When the data stream to/from the first activated bank is complete, the data stream to/from the second activated bank can begin without interruption. After the second bank is activated, the first bank can be deactivated to allow the entry of a new row address for the next round of accesses or the entry of new row addresses for other banks which currently are deactivated. In this manner, operation can continue in an interleaved fashion. Figure 30 is an example of four-bank row-interleaving read bursts with automatic deactivate with a read latency of 3 and a burst length of 8.

four-bank column-access operation

The availability of four banks allows the access of data from random starting columns between banks at a higher rate of operation. After activating each bank with a row address (ACTV command), A12–A13 for the four-bank column-access operation can be used to alternate READ or WRT commands between the banks to provide gapless accesses at the CLK frequency, provided all specified timing requirements are met. Figure 31 is an example of four-bank column-interleaving read bursts with a read latency of 3 and a burst length of 2.

bank deactivation (precharge)

All banks can be deactivated simultaneously (placed in precharge) by using the DCAB command. A single bank can be deactivated by using the DEAC command. The DEAC command is entered identically to the DCAB command except that A10 must be low and A12–A13 selects the bank to be precharged as shown in Table 1. Figure 26 and Figure 34 provide examples. A bank also can be deactivated automatically by using A10 during a READ or WRT command. If A10 is held high during the entry of a READ or WRT command, the accessed bank, selected by A12–A13 for the 4-bank option, is automatically deactivated upon completion of the access burst. If A10 is held low during READ- or WRT-command entry, that bank remains active following the burst. The READ and WRT commands with automatic deactivation are denoted as READ-P and WRT-P. See Figure 29 for an example.

chip select

$\overline{CS}$ (chip select) can be used to select or deselect the '664xx4 for command entry which might be required for multiple-memory-device decoding. If $\overline{CS}$ is held high on the rising edge of CLK (DESL command), the device does not respond to $\overline{RAS}$, $\overline{CAS}$, or $\overline{W}$ until the device is selected again. Device select is accomplished by holding $\overline{CS}$ low on the rising edge of CLK. Any other valid command can be entered simultaneously on the same rising CLK edge of the select operation. The device can be selected/deselected on a cycle-by-cycle basis (see Table 1 and Table 2). Using $\overline{CS}$ does not affect an access burst that is in progress; the DESL command can restrict only $\overline{RAS}$, $\overline{CAS}$, and $\overline{W}$ input to the '664xx4.

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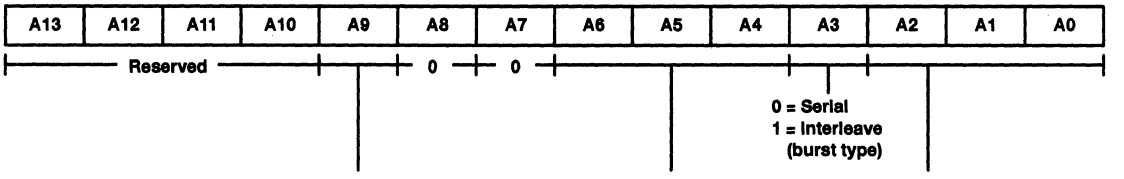
setting the mode register

The '664xx4 contains a mode register that should be user-programmed with the read latency, the burst type, and the burst length. This is accomplished by executing an MRS command with the information entered on address lines A0–A9. A logic 0 must be entered on A7 and A8, but A10–A13 are don't care entries for the '664xx4. When A9 = 1, the write burst length is always 1. When A9 = 0, the write burst length is defined by A2–A0. Figure 1 shows the valid combinations for a successful MRS command. Only valid addresses allow the mode register to be changed. If the addresses are not valid, the previous contents of the mode register remain unaffected. The MRS command is executed by holding $\overline{RAS}$, $\overline{CAS}$, and $\overline{W}$ low and the input-mode word valid on A0–A9 on the rising edge of CLK (see Table 1). The MRS command can be executed only when all banks are deactivated. See Figure 22 and Figure 36 for examples.



REGISTER BIT A9	Write Burst Length
0	A2–A0
1	1

REGISTER BITS†			READ LATENCY‡
A6	A5	A4	
0	1	0	2
0	1	1	3

† All other combinations are reserved.
‡ Refer to timing requirements for minimum valid read latencies based on maximum frequency rating.

REGISTER BITS§			BURST LENGTH
A2	A1	A0	
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	1	1	256 (x16), 512 (x8), 1024 (x4)

§ All other combinations are reserved.

Figure 1. Mode-Register Programming

refresh

The '664xx4 must be refreshed at intervals not exceeding t_{REF} (see timing requirements) or data cannot be retained. Refresh can be accomplished by performing an ACTV command ($\overline{RAS}$-only refresh) to every row in all banks, by performing 4096 auto-refresh (REFR) commands, or by placing the device in self refresh. Regardless of the method used, refresh must be accomplished before t_{REF} has expired. See Figure 35 for an example.

auto refresh

Before performing an auto refresh, all banks must be deactivated (placed in precharge). To enter a REFR command, $\overline{RAS}$ and $\overline{CAS}$ must be low and $\overline{W}$ must be high upon the rising edge of CLK (see Table 1). The refresh address is generated internally such that after 4096 REFR commands, all banks of the '664xx4 are refreshed. The external address and bank select A12–A13 are ignored. The execution of a REFR command automatically deactivates all banks upon completion of the internal auto-refresh cycle. This allows consecutive REFR-only commands to be executed, if desired, without any intervening DEAC commands. The REFR commands do not necessarily have to be consecutive, but all 4096 must be completed before t_{REF} expires.

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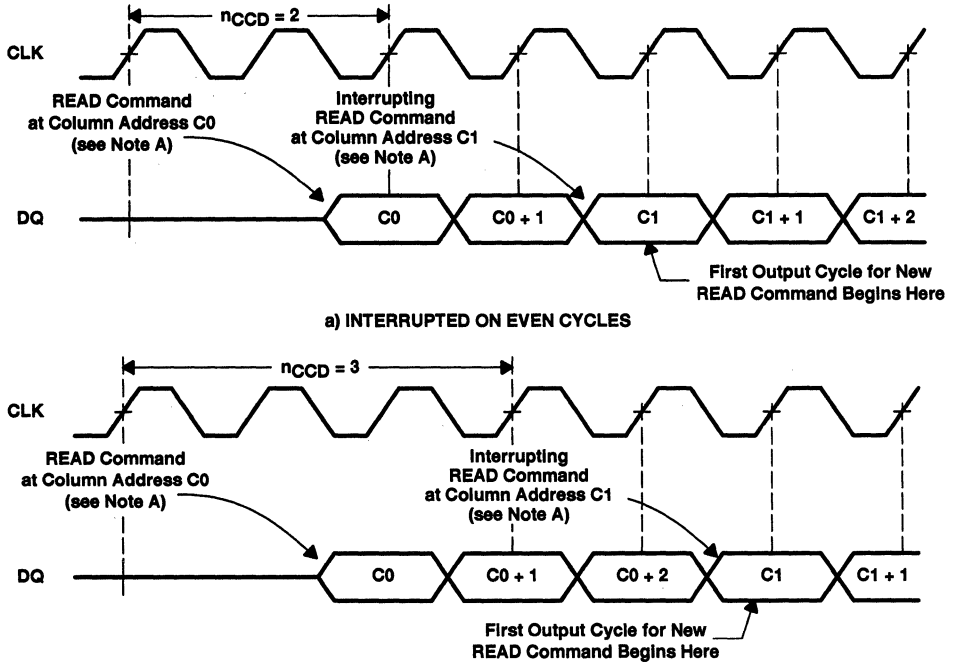
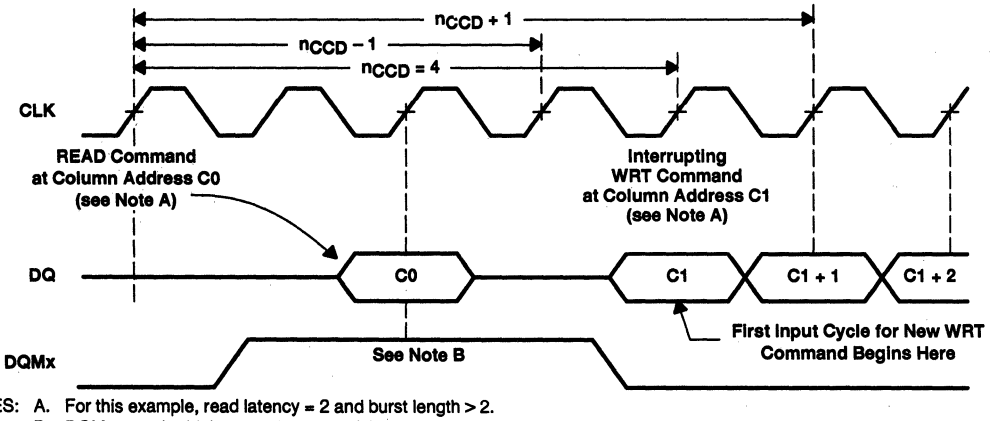
interrupted bursts (continued)



NOTE A: For this example, assume read latency = 2 and burst length > 2.

Figure 2. Read Burst Interrupted by Read Command



NOTES: A. For this example, read latency = 2 and burst length > 2.
B. DQMx must be high to mask output of the read burst on cycles (n_{CCD}–1), (n_{CCD}) and (n_{CCD}+1).

Figure 3. Read Burst Interrupted by Write Command

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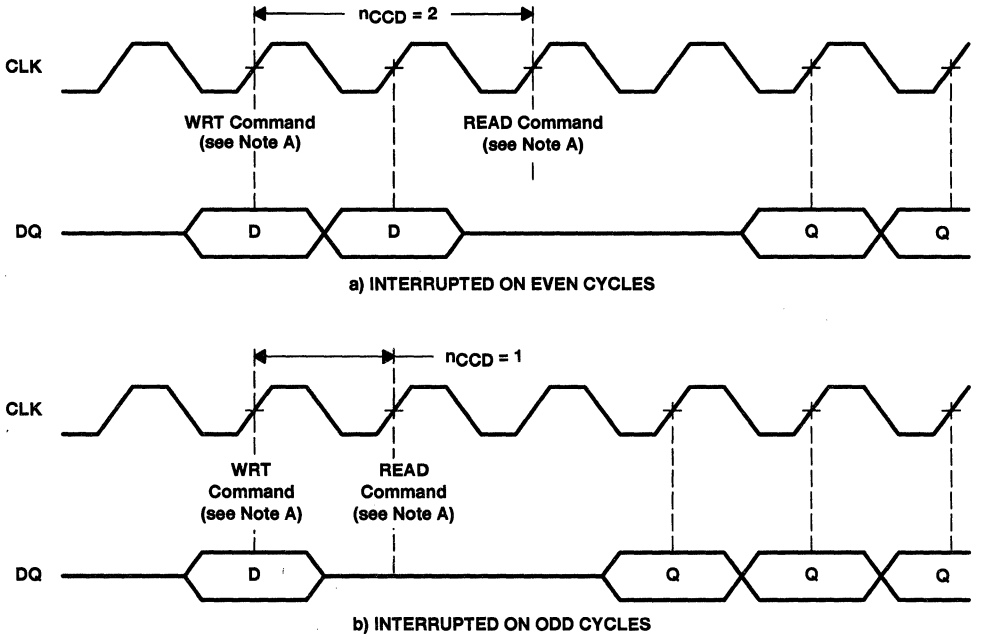
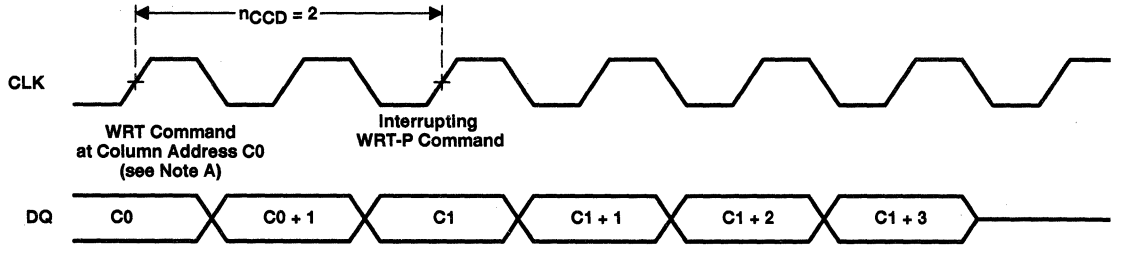
interrupted bursts (continued)



NOTE A: For this example, assume read latency = 2, burst length > 2.

Figure 6. Write Burst Interrupted by Read Command



NOTE A: For this example, burst length > 2.

Figure 7. Write Burst Interrupted by Write Command

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... – 0.5 V to 4.6 V
Supply voltage range for output drivers, V_{CCQ} ..... – 0.5 V to 4.6 V
Voltage range on any input pin (see Note 1) ..... – 0.5 V to 4.6 V
Voltage range on any output pin (see Note 1) ..... – 0.5 V to V_{CC} + 0.5 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... – 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{CCQ}	Supply voltage for output drivers‡	3	3.3	3.6	V
V_{SS}	Supply voltage		0		V
V_{SSQ}	Supply voltage for output drivers		0		V
V_{IH}	High-level input voltage	2		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage	– 0.3		0.8	V
T_A	Operating free-air temperature	0		70	°C

‡ $V_{CCQ} \leq V_{CC}$ + 0.3 V

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capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

		MIN	MAX	UNIT
$C_{i(S)}$	Input capacitance, CLK input		5	pF
$C_{i(AC)}$	Input capacitance, address and control inputs: A0–A13, $\overline{CS}$, DQMx, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		5	pF
$C_{i(E)}$	Input capacitance, CKE input		5	pF
C_o	Output capacitance		7	pF

NOTE 4: V_{CC} = 3.3 ± 0.3 V and bias on pins under test is 0 V.

ac timing requirements over recommended ranges of supply voltage and operating free-air temperature†‡

			'664xx4-10		'664xx4-12		UNIT
			MIN	MAX	MIN	MAX	
t_{CK}	Cycle time, CLK (system clock)	Read latency = 2	15		18		ns
		Read latency = 3	10		12		
t_{CKH}	Pulse duration, CLK (system clock) high		3		4		ns
t_{CKL}	Pulse duration, CLK (system clock) low		3		4		ns
t_{AC}	Access time, CLK ↑ to data out (see Note 4)	Read latency = 2		12		15	ns
		Read latency = 3		8		10	
t_{LZ}	Delay time, CLK to DQ in the low-impedance state (see Note 5)		0		0		ns
t_{HZ}	Delay time, CLK to DQ in the high-impedance state (see Note 6)	Read latency = 2		7		9	ns
		Read latency = 3		7		9	
t_{DS}	Setup time, data input		2		3		ns
t_{AS}	Setup time, address		2		3		ns
t_{CS}	Setup time, control input ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, DQMx)		2		3		ns
t_{CES}	Setup time, CKE (suspend entry/exit, power-down entry)		2		3		ns
t_{CESP}	Setup time, CKE (power-down/self-refresh exit) (see Note 7)		8		10		ns
t_{OH}	Hold time, CLK ↑ to data out		3		3		ns
t_{DH}	Hold time, data input		1		1		ns
t_{AH}	Hold time, address		1		1		ns
t_{CH}	Hold time, control input ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, DQMx)		1		1		ns
t_{CEH}	Hold time, CKE		1		1		ns
t_{RC}	REFR command to ACTV, MRS, REFR, or SLFR command; ACTV command to ACTV, MRS, REFR, or SLFR command; Self-refresh exit to ACTV, MRS, REFR, or SLFR command		90		110		ns
t_{RAS}	ACTV command to DEAC or DCAB command (see Note 9)		60	120 000	70	120 000	ns
t_{RCD}	ACTV command to READ or WRT command (see Note 9)		30		35		ns
t_{RP}	DEAC or DCAB command to ACTV, MRS, SLFR, or REFR command		30		40		ns

† See Figure 10 for load circuits.

‡ All references are made to the rising transition of CLK, unless otherwise noted.

NOTES: 5. t_{AC} is referenced from the rising transition of CLK that is previous to the data-out cycle. For example, the first data out t_{AC} is referenced from the rising transition of CLK that is read latency – one cycle after the READ command. An access time is measured at output reference level 1.4 V.

6. t_{LZ} is measured from the rising transition of CLK that is read latency – one cycle after the READ command.
7. t_{HZ} (max) defines the time at which the outputs are no longer driven and is not referenced to output voltage levels.
8. See Figures 19 and 20.
9. In case of WRITE with auto precharge (WRT_P), the t_{RCD} parameter must be relaxed to satisfy t_{RAS} parameter. For example, – t_{RCD} = 40 ns, for BL = 1 in order to satisfy t_{RAS} = 60 ns in – 10 spec.

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Table 9. Number of Cycles Required to Meet Minimum Specification for Key Timing Parameters†

			'664xx4-10		'664xx4-12		UNITS
	Operating frequency		100	66.6	83.3	55.5	MHz
t_{CK}	Cycle time, CLK (system clock)		10	15	12	18	ns
	KEY PARAMETER		**NUMBER OF CYCLES REQUIRED**				
	Read latency, minimum programmed value		3	2	3	2	cycles
t_{RCD}	ACTV command to READ or WRT command		3	2	3	2	cycles
t_{RAS}	ACTV command to DEAC or DCAB command		6	4	6	4	cycles
t_{RP}	DEAC or DCAB command to ACTV, MRS, SLFR, or REFR command		3	2	3	2	cycles
t_{RC}	REFR command to ACTV, MRS, or REFR command; self-refresh exit to ACTV, MRS, SLFR, or REFR command		9	6	10	7	cycles
t_{RWL}	Final data in to DEAC or DCAB command		2	1	2	1	cycles
t_{RRD}	ACTV command for one bank to ACTV command for the other bank		2	2	2	2	cycles
t_{APR}	Final data out of READ-P operation to ACTV, MRS, SLFR, or REFR command	Read latency = 2 (n_{EP} = –1)	—	2	—	2	cycles
		Read latency = 3 (n_{EP} = –2)	2	1	2	1	cycles
t_{APW}	Final data in of WRT-P operation to ACTV, MRS, SLFR, or REFR command		4	3	5	3	cycles

† All references are made to the rising transition of CLK, unless otherwise noted.

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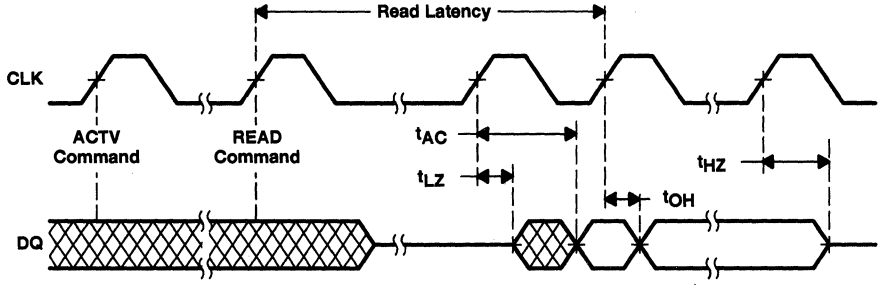
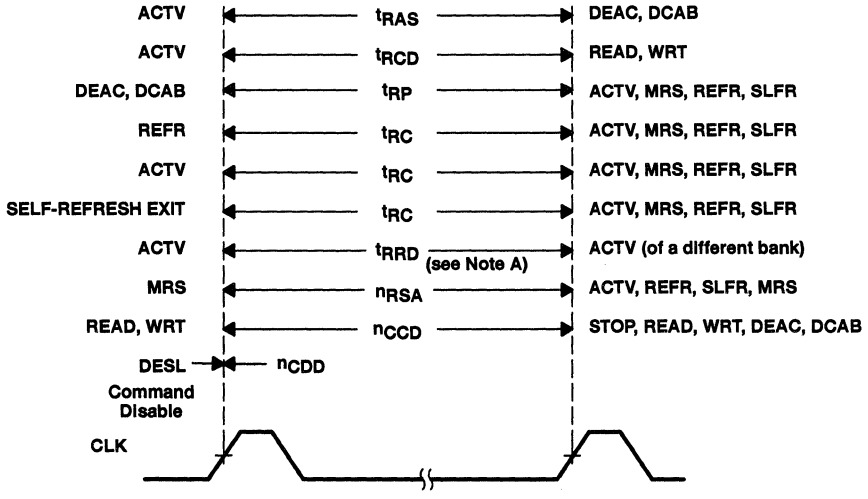


Figure 12. Output Parameters



NOTE A: t_{RRD} is specified for command execution in one bank to command execution in the other bank.

Figure 13. Command-to-Command Parameters

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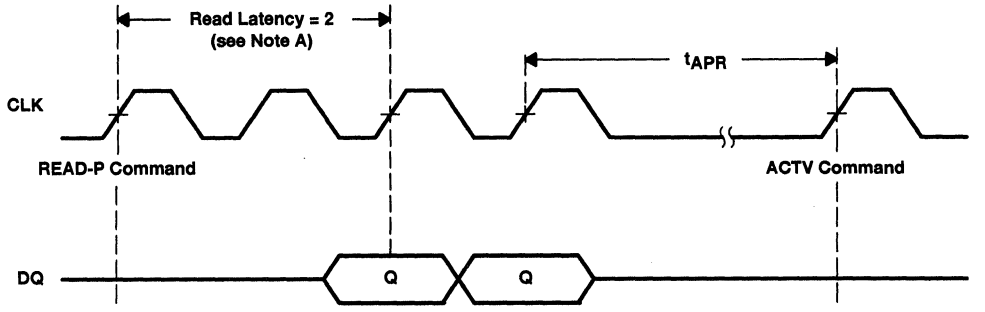
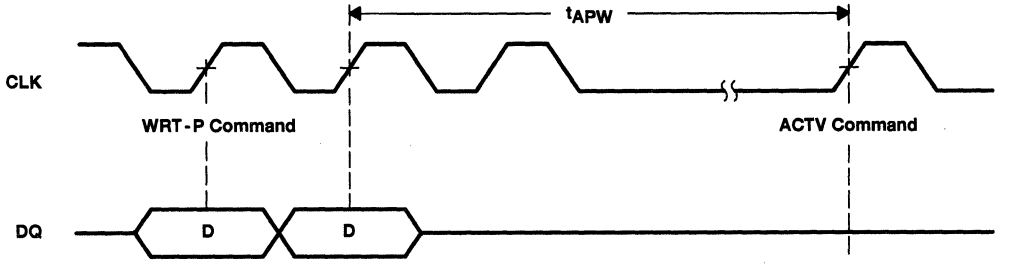


NOTE A: For this example, assume read latency = 2 and burst length = 2.

Figure 16. Read-Automatic Deactivate (Autoprecharge)



NOTE A: For this example, the burst length = 2.

Figure 17. Write-Automatic Deactivate (Autoprecharge)

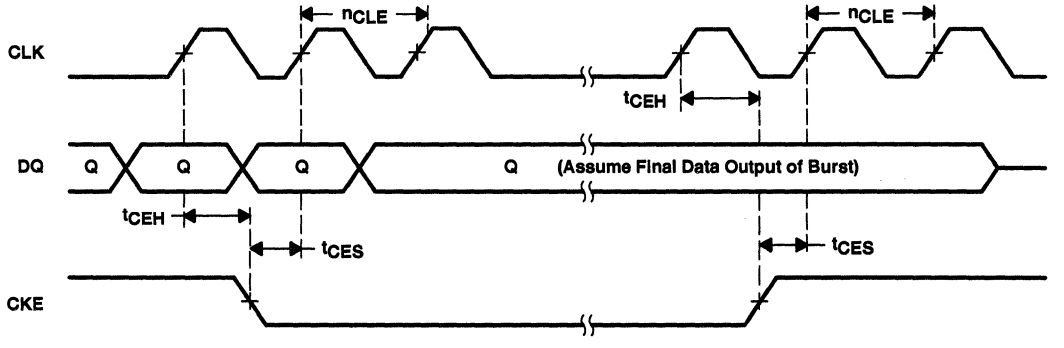


Figure 18. CLK-Suspend Operation (Assume BL = 4)

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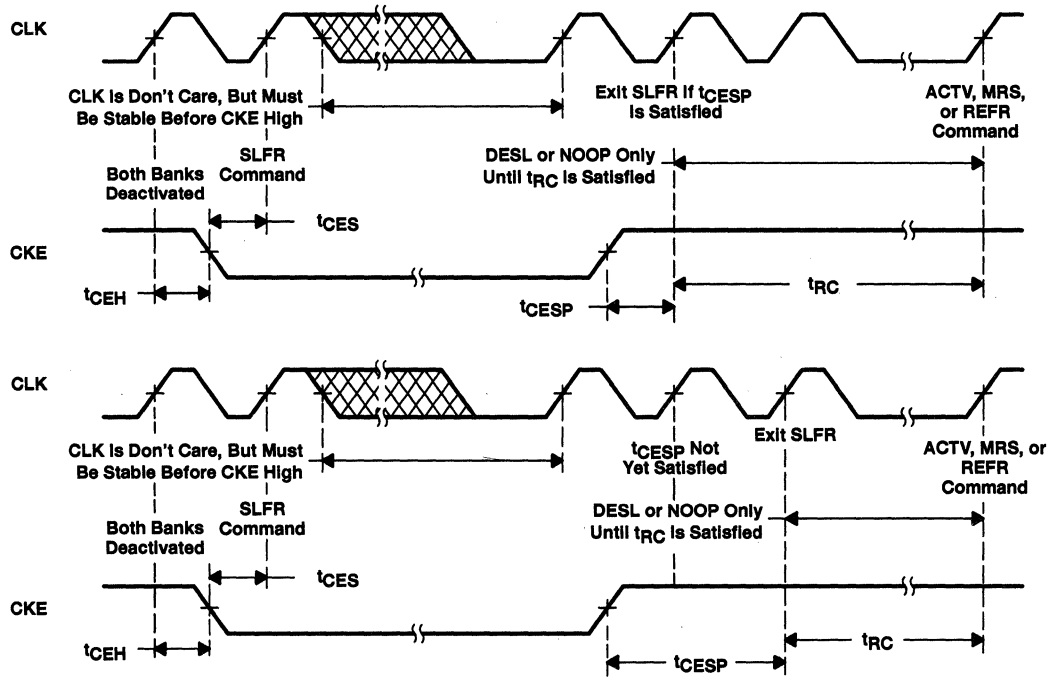

NOTES: A. Assume both banks are deactivated before the execution of SLFR.
B. Before/after self-refresh mode, 4K burst auto refresh cycles are recommended to ensure the SDRAM is fully refreshed.

Figure 20. Self-Refresh Entry/Exit

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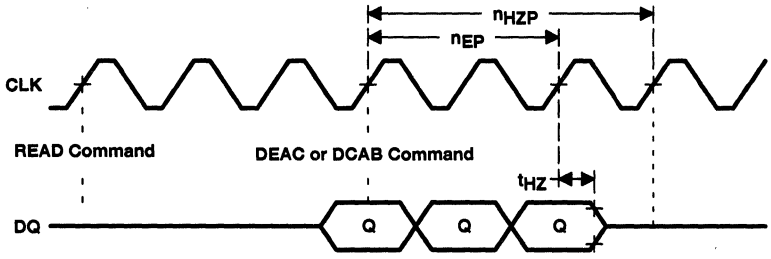
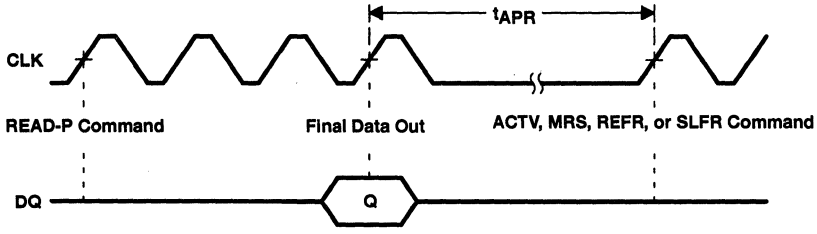


NOTE A: For this example, assume read latency = 3, and burst length = 4.

Figure 23. Read Followed by Deactivate



NOTE A: For this example, assume read latency = 3, and burst length = 1.

Figure 24. Read With Auto-Deactivate

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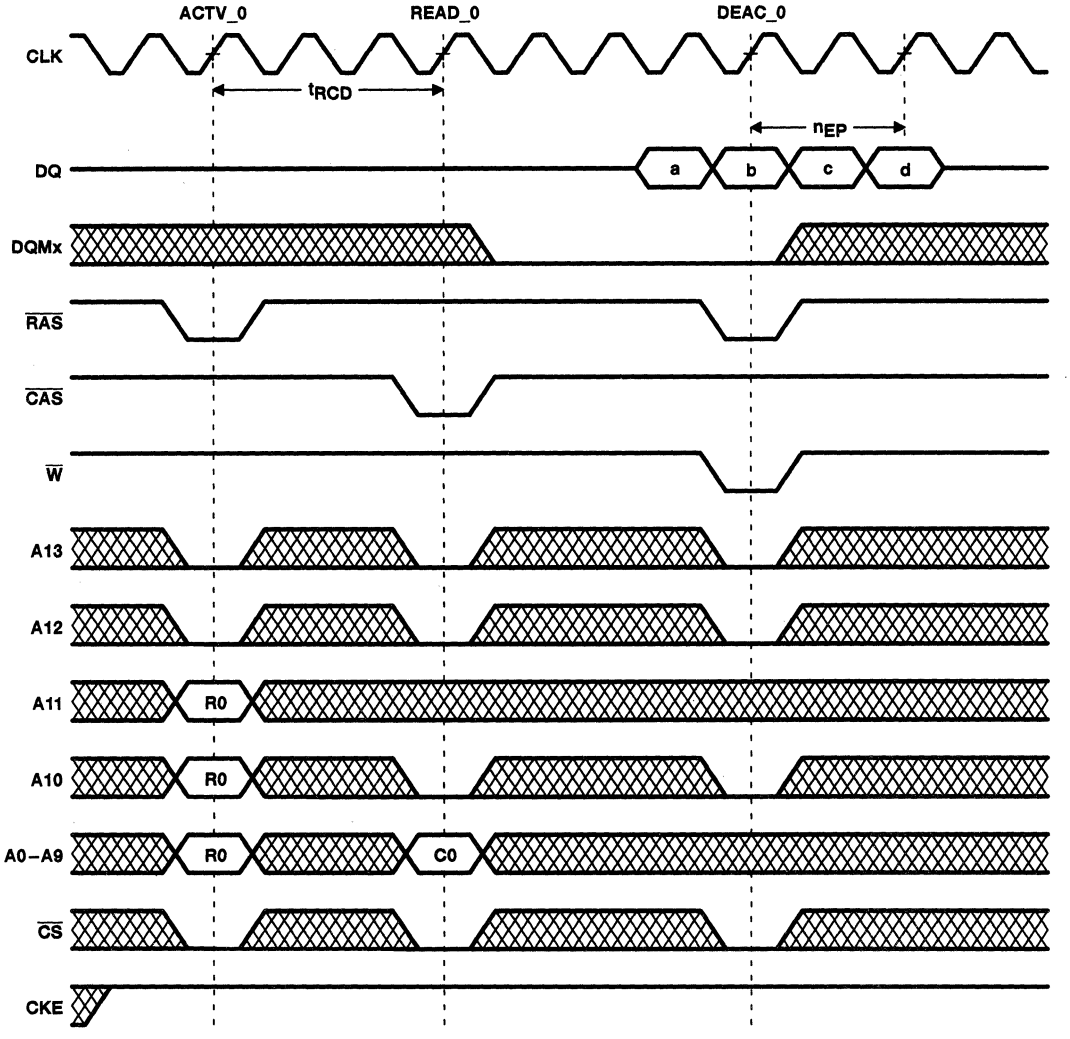

BURST TYPE	BANK	ROW	BURST CYCLE			
(D/Q)	(0–3)	ADDR	a	b	c	d
Q	0	R0	C0†	C0 + 1	C0 + 2	C0 + 3

† Column-address sequence depends on programmed burst type and starting address C0 (see Table 5).
NOTE A: This example illustrates minimum t_{RCD} and n_{EP} for the '664xx4 at 100 MHz.

Figure 26. Read Burst (read latency = 3, burst length = 4)

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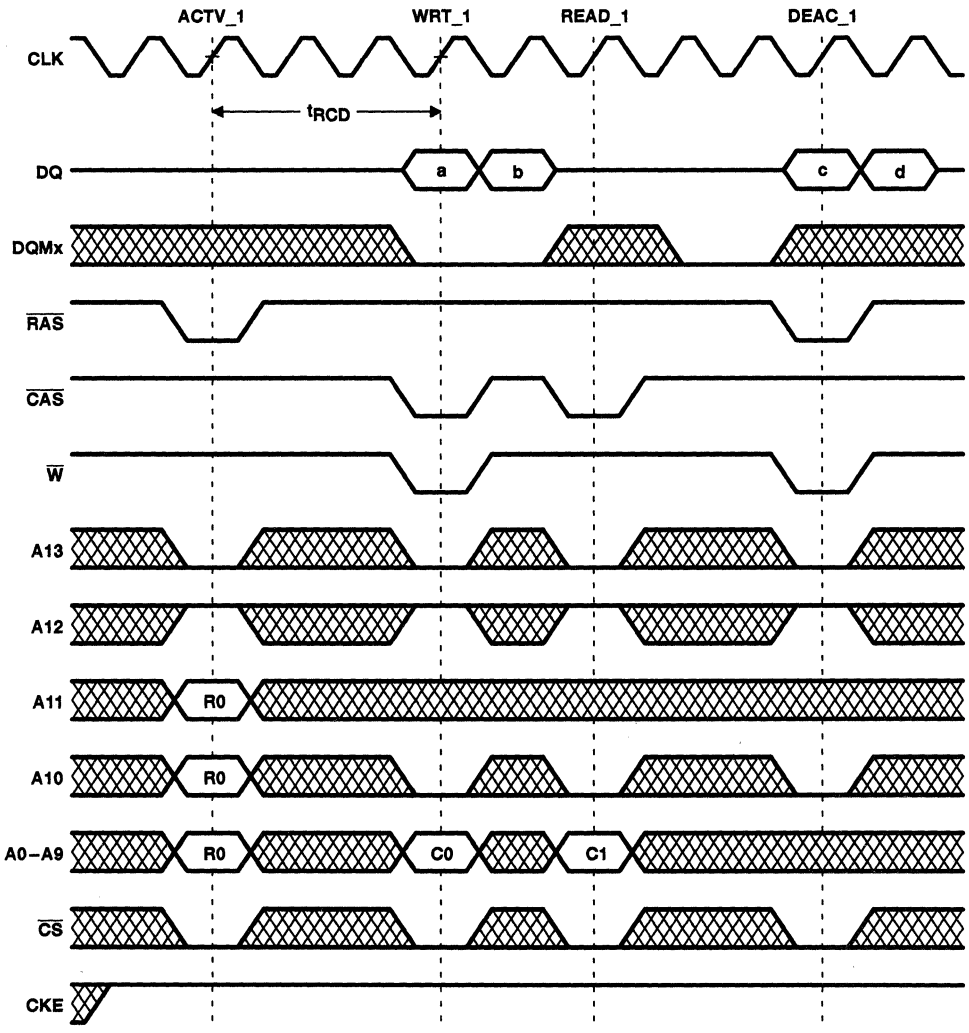

BURST TYPE	BANK	ROW	BURST CYCLE			
(D/Q)	(0–3)	ADDR	a	b	c	d
D	1	R0	C0†	C0+1		
Q	1	R0			C1	C1+1

† Column-address sequence depends on programmed burst type and starting addresses C0 and C1 (see Table 4).
NOTE A: This example illustrates minimum t_{RCD} for the '664xx4 at 100 MHz.

Figure 28. Write-Read Burst (read latency = 3, burst length = 2)

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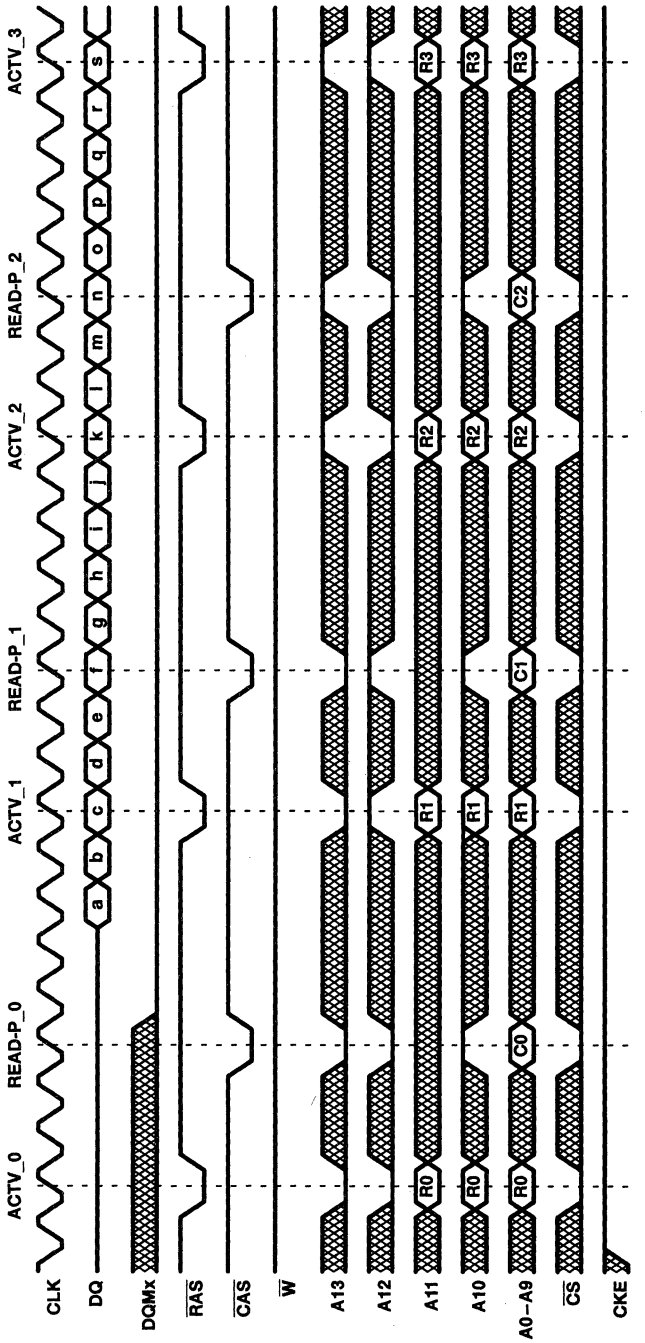


BURST TYPE	BANK	ROW	BURST CYCLE																	
(D/Q)	(0–3)	ADDR	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	...
Q	0	R0	C0†	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7												
Q	1	R1									C1	C1+1	C1+2	C1+3	C1+4	C1+5	C1+6	C1+7				
Q	2	R2																	C2	C2+1	C2+2	...

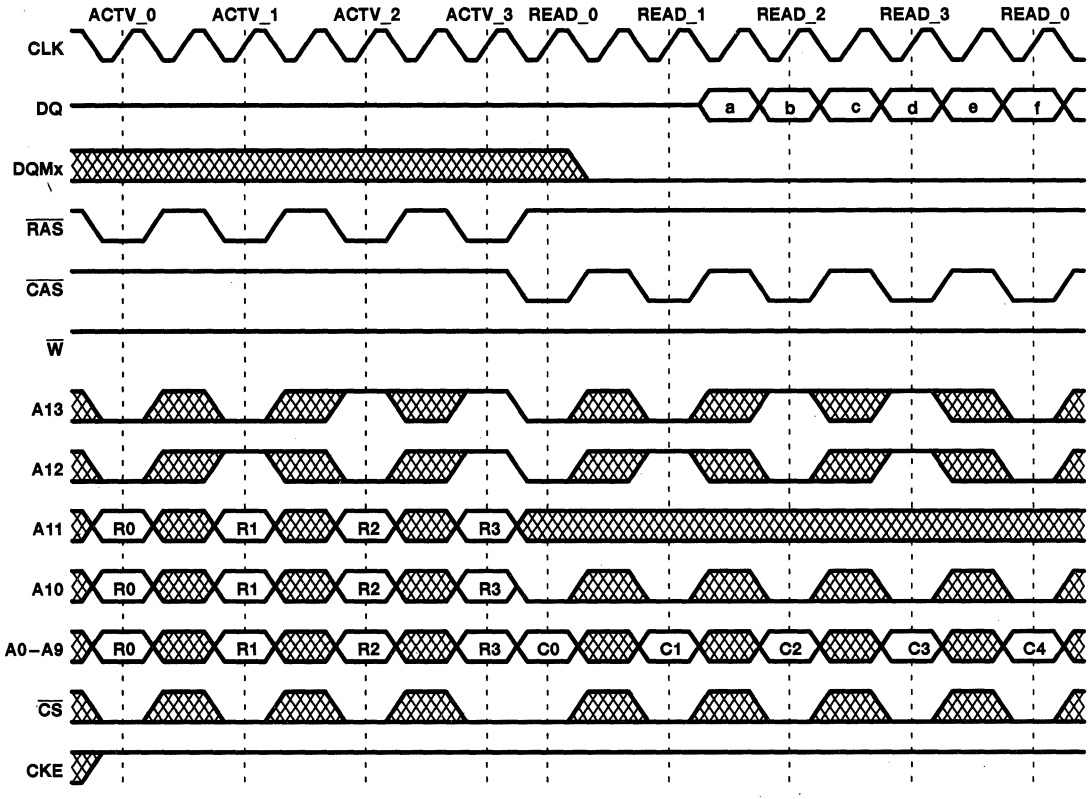
† Column-address sequence depends on programmed burst type and starting addresses C0, C1, and C2 (see Table 6).
NOTE A: This example illustrates minimum t_{RCD} for the '664xx4 at 100 MHz.

(a)

Figure 30. Four-Bank Row-Interleaving Read Bursts With Automatic Deactivate (read latency = 3, burst length = 8)

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



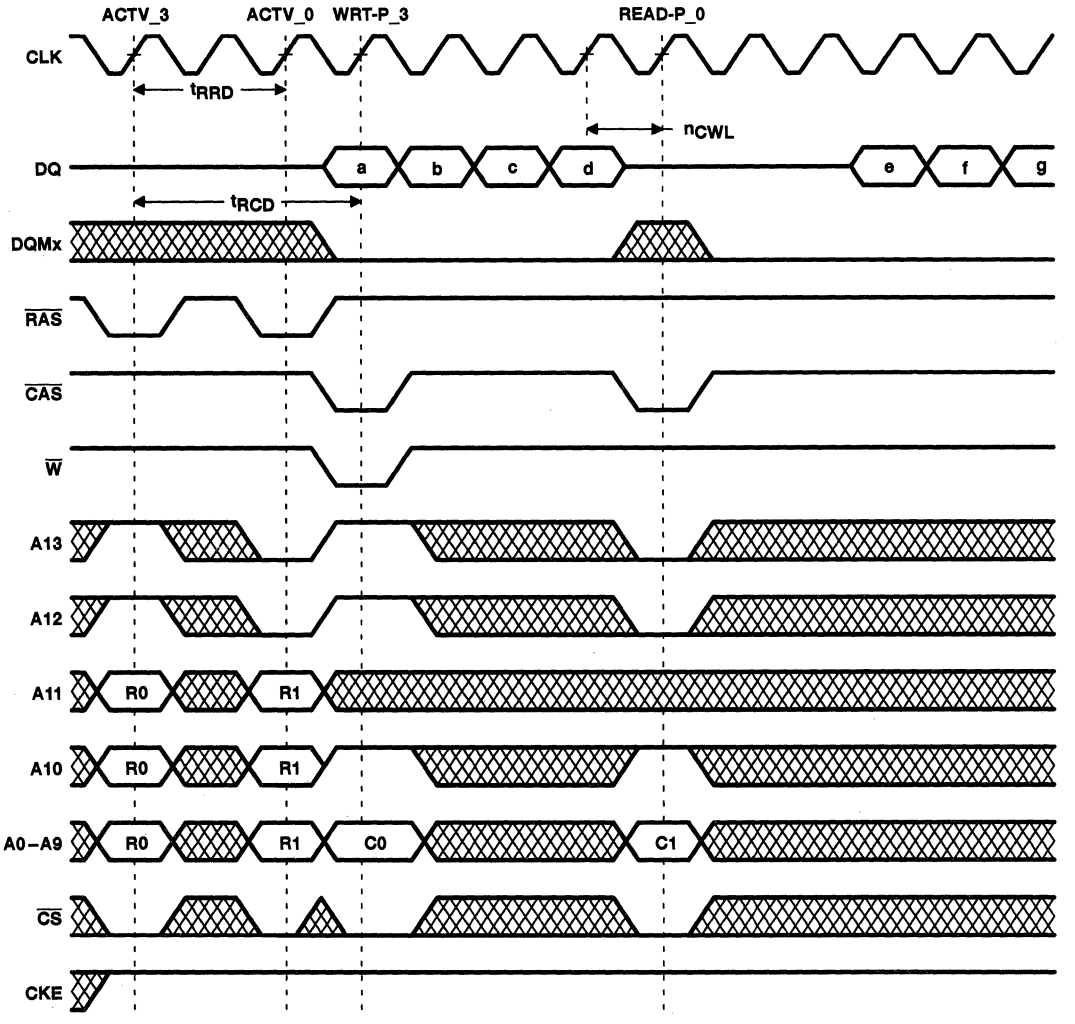
BURST TYPE (D/Q)	BANK (0–3)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h	...	...
Q	0	R0	C0†	C0+1								
Q	1	R1			C1	C1+1						
Q	2	R2					C2	C2+1				
Q	3	R3							C3	C3+1		
...	...	...									...	...

† Column-address sequence depends on programmed burst type and starting addresses C0, C1, and C2 (see Table 4).

Figure 31. Four-Bank Column-Interleaving Read Bursts (read latency = 3, burst length = 2)

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



BURST TYPE	BANK	ROW	BURST CYCLE							
(D/Q)	(0–3)	ADDR	a	b	c	d	e	f	g	h
D	3	R0	C0†	C0+1	C0+2	C0+3				
Q	0	R1					C1	C1+1	C1+2	C1+3

† Column-address sequence depends on programmed burst type and starting addresses C0 and C1 (see Table 5).
NOTE A: This example illustrates minimum n_{CWL} and t_{RRD} for the '664xx4 at 100 MHz.

Figure 33. Write-Burst Bank 3, Read-Burst Bank 0 With Automatic Deactivate (read latency = 3, burst length = 4)

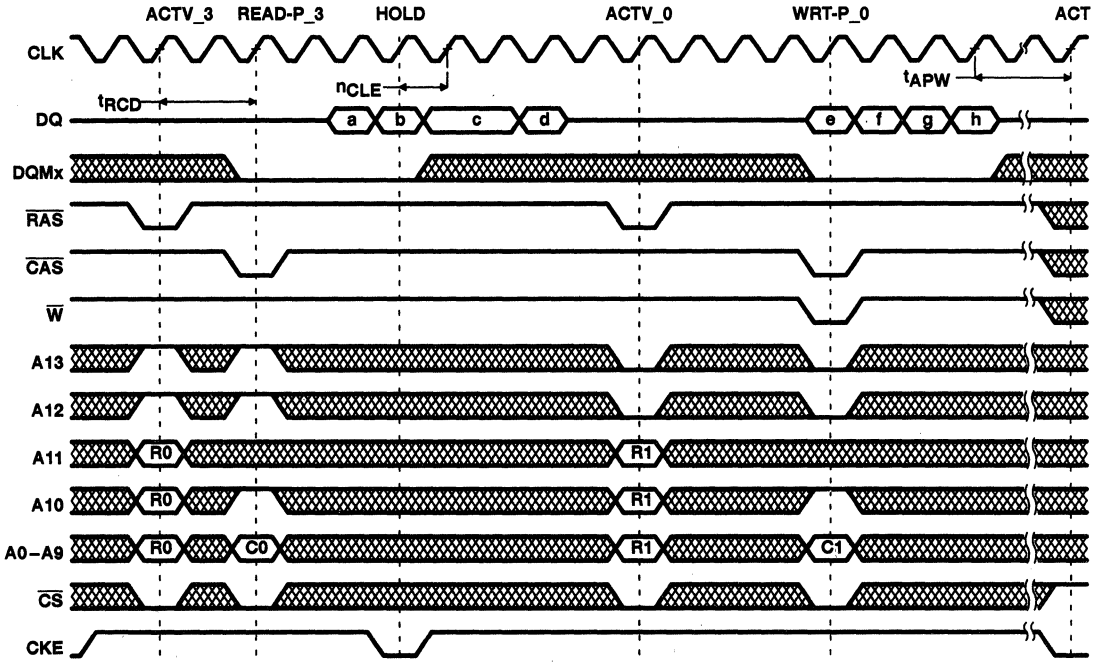
PRODUCT PREVIEW

BURST TYPE	BANK	ROW	BURST CYCLE							
(D/Q)	(0–3)	ADDR	a	b	c	d	e	f	g	h
Q	3	R0	C0†	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7

† Column-address sequence depends on programmed burst type and starting address C0 (see Table 6).
NOTE A: This example illustrates minimum t_{RC}, t_{RCD}, n_{EP}, and t_{RP} for the '664xx4-10 at 66.6 MHz.

**Figure 35. Refresh Cycles (Refreshes Followed by Read Burst, Followed by Refresh)
(read latency = 2, burst length = 8)**

PARAMETER MEASUREMENT INFORMATION



BURST TYPE	BANK	ROW	BURST CYCLE							
(D/Q)	(0–3)	ADDR	a	b	c	d	e	f	g	h
Q	3	R0	C0†	C0+1	C0+2	C0+3				
D	0	R1					C1†	C1+1	C1+2	C1+3

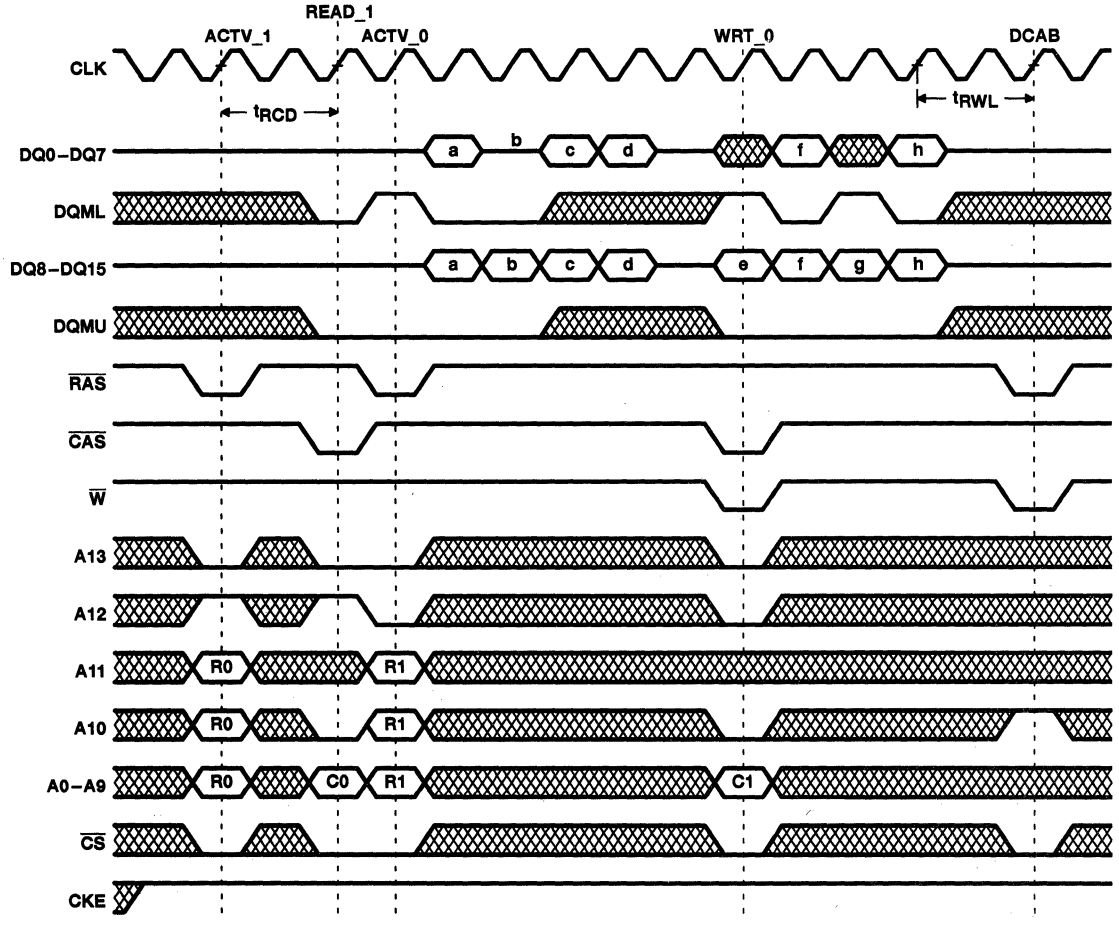
† Column-address sequence depends on programmed burst type and starting addresses C0 and C1 (see Table 5).

NOTES: A. This example illustrates minimum t_{RCD} and t_{APW} for the '664xx4-10 at 66.6 MHz.
B. If entering the PDE command with violation of short t_{APW}, the device still is entering the power-down mode and then both banks are deactivated (still in power-down mode).

Figure 37. Use of CKE for Clock Gating (Hold) and Standby Mode (Read-Burst Bank 3 With Hold, Write-Burst Bank 0, Standby Mode) (read latency = 2, burst length = 4)

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



BURST TYPE (D/Q)	BANK (0–3)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h
Q	1	R0	C0†	C0+1	C0+2	C0+3				
D	0	R1					C1†	C1+1	C1+2	C1+3

† Column-address sequence depends on programmed burst type and starting addresses C0 and C1 (see Table 5).
NOTE A: This example illustrates minimum t_{RCD} and a minimum t_{RWL} write burst for the '664xx4-10 at 66.6 MHz.

Figure 39. Use of DQM for Output and Data-In Cycle Masking (Read-Burst Bank 1, Write-Burst Bank 0, Deactivate All Banks) [Only Masked Out the Lower Bytes (Random Bits)] for x16 (read latency = 2, burst length = 4)

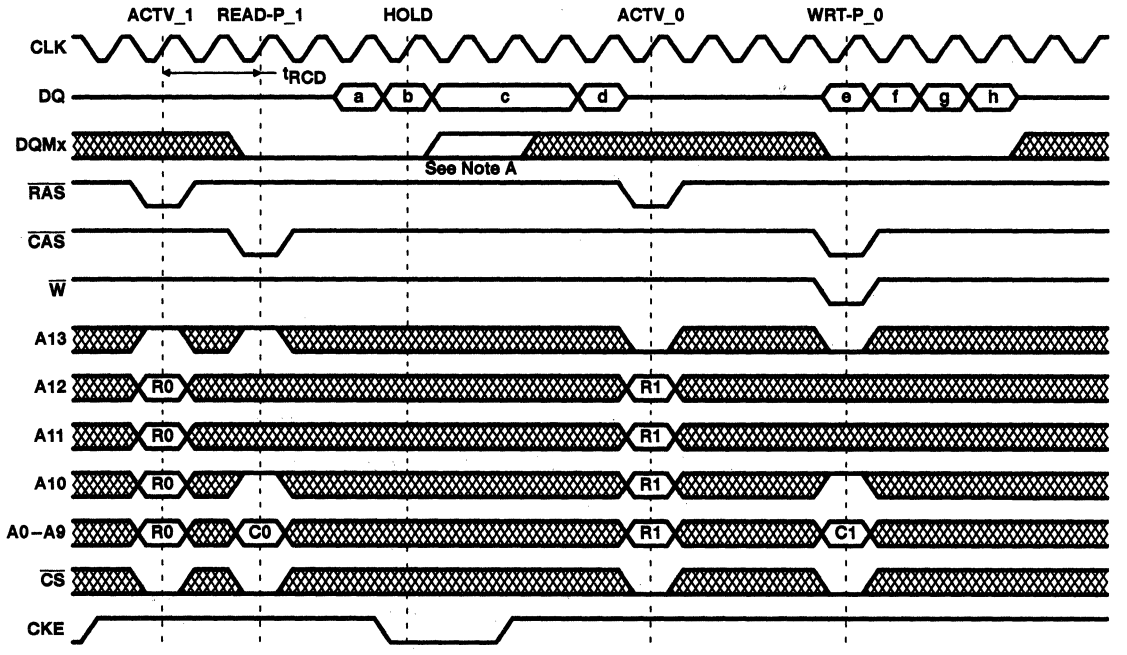
PRODUCT PREVIEW

BURST TYPE	BANK	ROW	BURST CYCLE								
(D/Q)	(0–3)	ADDR	a	b	c	d	e	f	g	h	i
Q	1	R0	C0†	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7	
D	1	R0									C1

† Column-address sequence depends on programmed burst type and starting addresses C0 and C1 (see Table 6).
NOTE A: This example illustrates minimum t_{RCD} for the '664xx4-10 at 100 MHz.

Figure 41. Read Burst — Single Write With Automatic Deactivate (read latency = 3, burst length = 8)

PARAMETER MEASUREMENT INFORMATION



BURST TYPE (D/Q)	BANK (0–1)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h
Q	1	R0	C0†	C0 + 1	C0 + 2	C0 + 3				
D	0	R1					C1	C1 + 1	C1 + 2	C1 + 3

† Column-address sequence depends on programmed burst type and starting addresses C0 and C1 (see Table 5).

NOTES: A. These rising clocks during output "c" with DQMx = Hi would not mask out the output "d" due to CKE insert low to suspend those rising clocks at cycle DQMx = Hi.

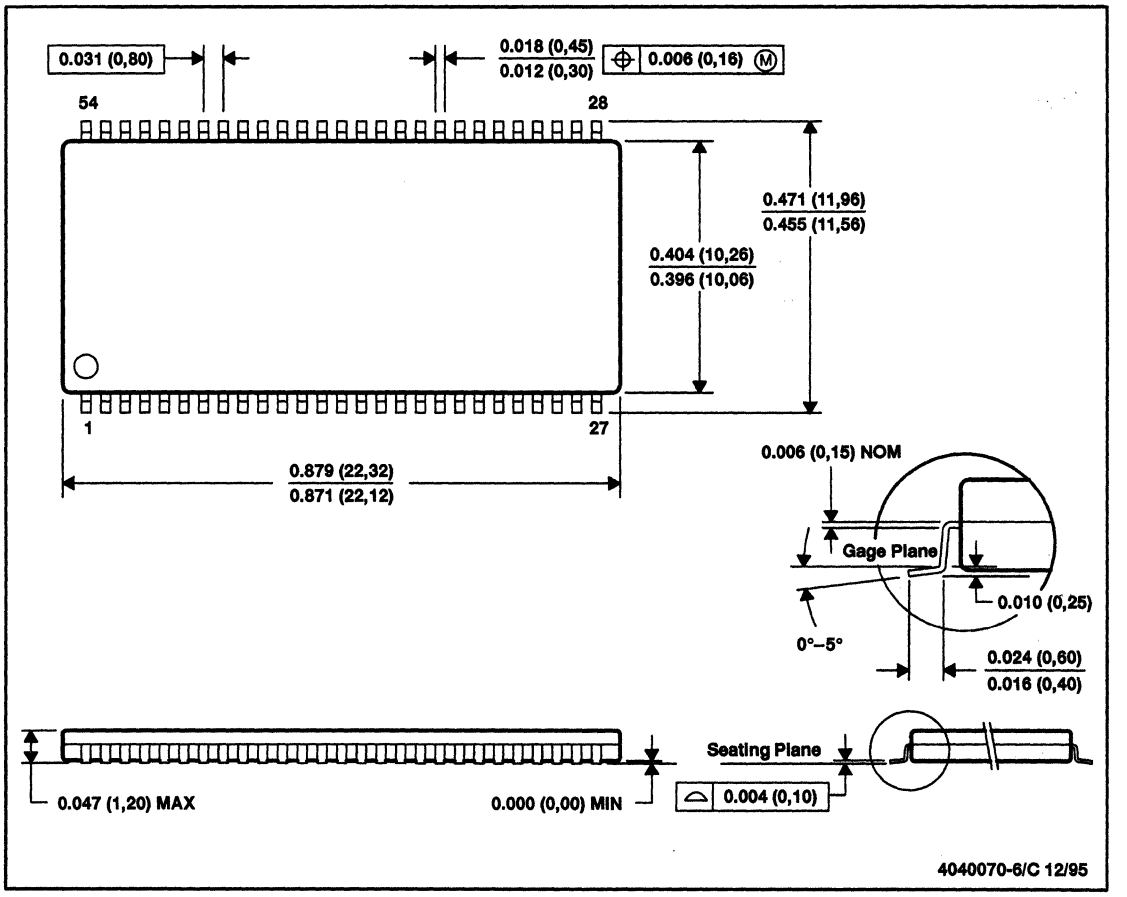
B. This example illustrates minimum t_{RCD} for the '664xx4-10 at 66.6 MHz.

Figure 43. Use of CKE for Clock Gating (Hold/Suspend) and DQM = Hi Showed No Effect (read latency = 2, burst length = 4, two banks)

PRODUCT PREVIEW

MECHANICAL DATA

DGE (R-PDSO-G54) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

PRODUCT PREVIEW

Timing Differences of 10-pF Versus 50-pF Loading

SCEA004
November 1996

TEXAS INSTRUMENTS

Introduction

This application report provides a data analysis of Texas Instruments (TI) 'ALVCH16244, which is an advanced low-voltage CMOS (ALVC) 16-bit unidirectional driver. The 'ALVCH16244, 'ALVCH16721, 'ALVCH162827, and 'ALVCH16835 are unidirectional drivers that are commonly used in personal computers and workstations for memory addressing in dual in-line memory modules (DIMMs). Typical DIMM applications, however, require loads of approximately 10 pF and a temperature range from 0°C to 70°C. Since the data sheet values for t_{pd}, t_{en}, and t_{dis} are characterized under a 50-pF load and a temperature range of –40°C to 85°C, designers may find the difference in typical values to be beneficial. The purpose of this application report is to provide design engineers with the difference in typical values for t_{pd}, t_{en}, and t_{dis} using a load of 10 pF, as opposed to 50 pF, and a temperature range of 0°C to 70°C, as opposed to –40°C to 85°C.

Laboratory Testing Technique

Due to its widespread use, the 'ALVCH16244 was selected as the device for actual laboratory data. The data measures propagation delay time, enable time, and disable time. The values presented are the averages of three different outputs. The data presented is indicative of the 'ALVCH16721, the 'ALVCH162827, and the 'ALVCH16835, since the size of their output transistors are the same as those on the 'ALVCH16244. All values provided are typical values. Unique testing specifications are shown in the top, left portion of each graph.

Figure 1 shows the difference in propagation delay time, enable time, and disable time for V_{CC} = 2.7 V and temperature values of 0°C and 70°C. The impact of a 10-pF versus a 50-pF loading results in decreases of approximately 20% in propagation delay time, approximately 25% in enable time, and approximately 10% in disable time.

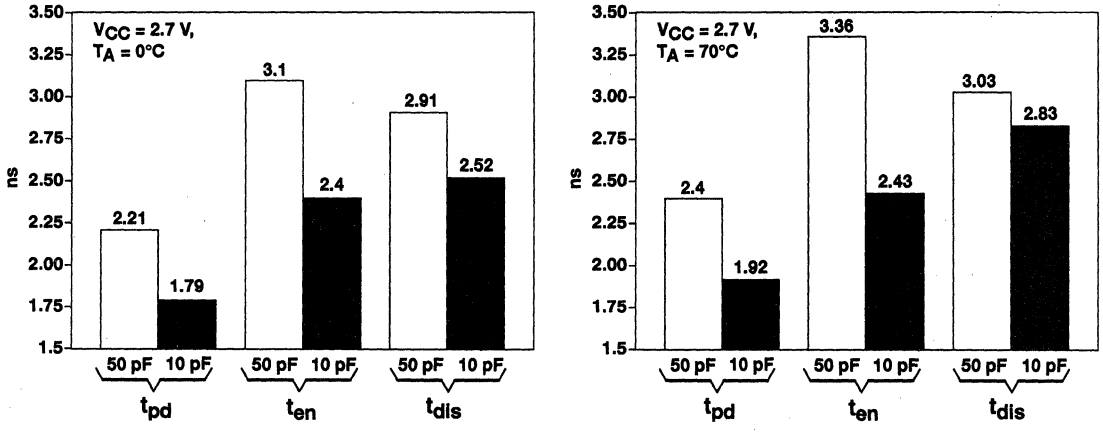


Figure 1. 'ALVCH16244 10-pF Versus 50-pF Switching-Time Differences for V_{CC} = 2.7 V

Figure 2 shows the difference in propagation delay time, enable time, and disable time for V_{CC} = 3 V and temperature values of 0°C and 70°C. The impact of a 10-pF versus a 50-pF loading results in decreases of approximately 25% in propagation delay time and enable time, and approximately 8% in disable time.

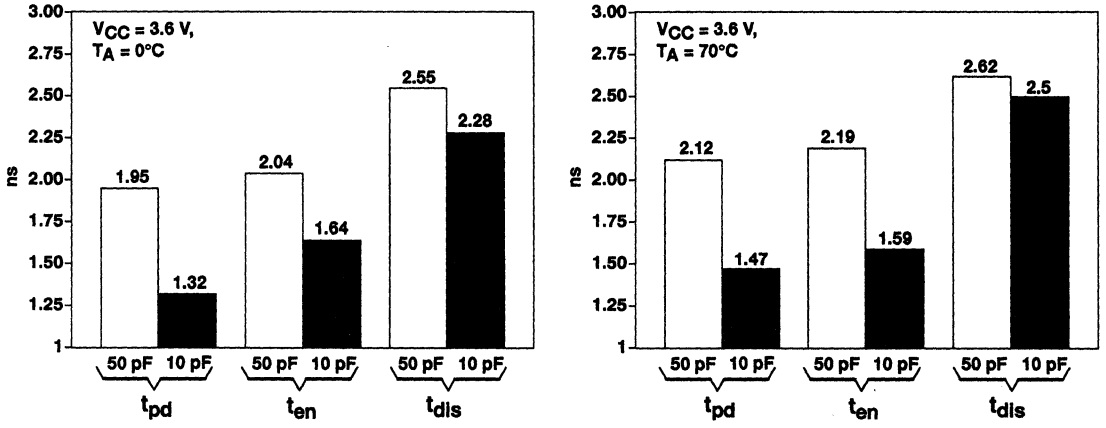


Figure 4. 'ALVCH16244 10-pF Versus 50-pF Switching-Time Differences for V_{CC} = 3.6 V

Conclusion

There is a noticeable difference in propagation delay time, enable time, and disable time when a 10-pF load versus a 50-pF load is used, and when an operating temperature range of 0°C to 70°C, as opposed to –40°C to 85°C, is used. The propagation delay time decreased an average of 26%, the enable time decreased an average of 24%, and the disable time decreased an average of 8%.

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a three-part type number as explained in the following example.

EXAMPLE: SN 74ALVCH16721 DGG R

Prefix

MUST CONTAIN TWO TO FOUR LETTERS

SN = Standard prefix
SNJ = MIL-STD-883 processed and screened per JEDEC Standard 101

Unique Circuit Description

MUST CONTAIN SIX TO TWELVE CHARACTERS

Examples: 74ALVCH16244
74SSTL16837
CDC587

Package

MUST CONTAIN ONE TO THREE LETTERS

DBB, DGV = plastic thin very small-outline package (TVSOP)
DGE, DGG, PW = plastic thin shrink small-outline package (TSSOP)
DL = plastic shrink small-outline package (SSOP)
PAH = plastic thin quad flat package

Tape and Reel Packaging

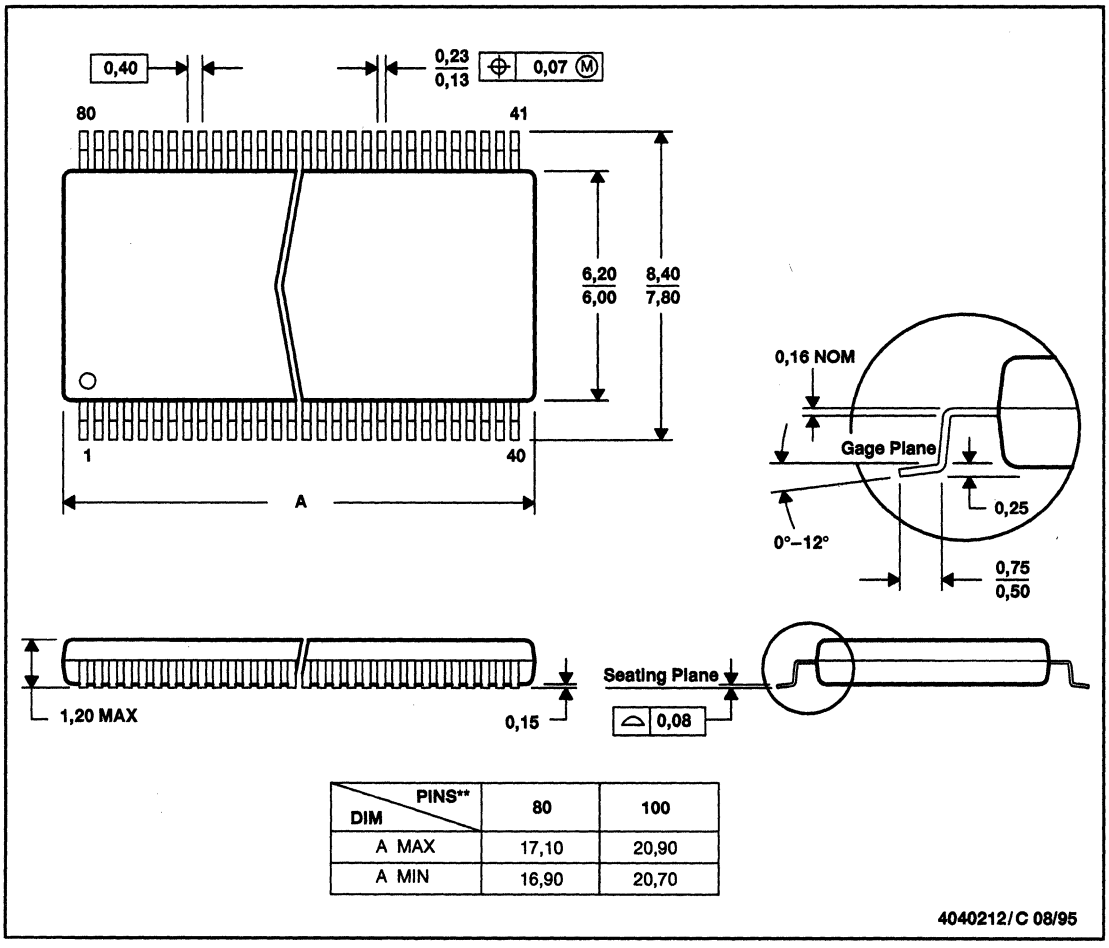
Valid for surface-mount packages only. All orders for tape and reel must be for whole reels.

MUST CONTAIN ONE OR TWO LETTERS

LE = Left embossed tape and reel (required for PW package)
R = Standard tape and reel (required for DBB, DGG, DGV; optional for DGE and DL packages)

DBB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

80 PIN SHOWN



DIM \ PINS**	80	100
A MAX	17,10	20,90
A MIN	16,90	20,70

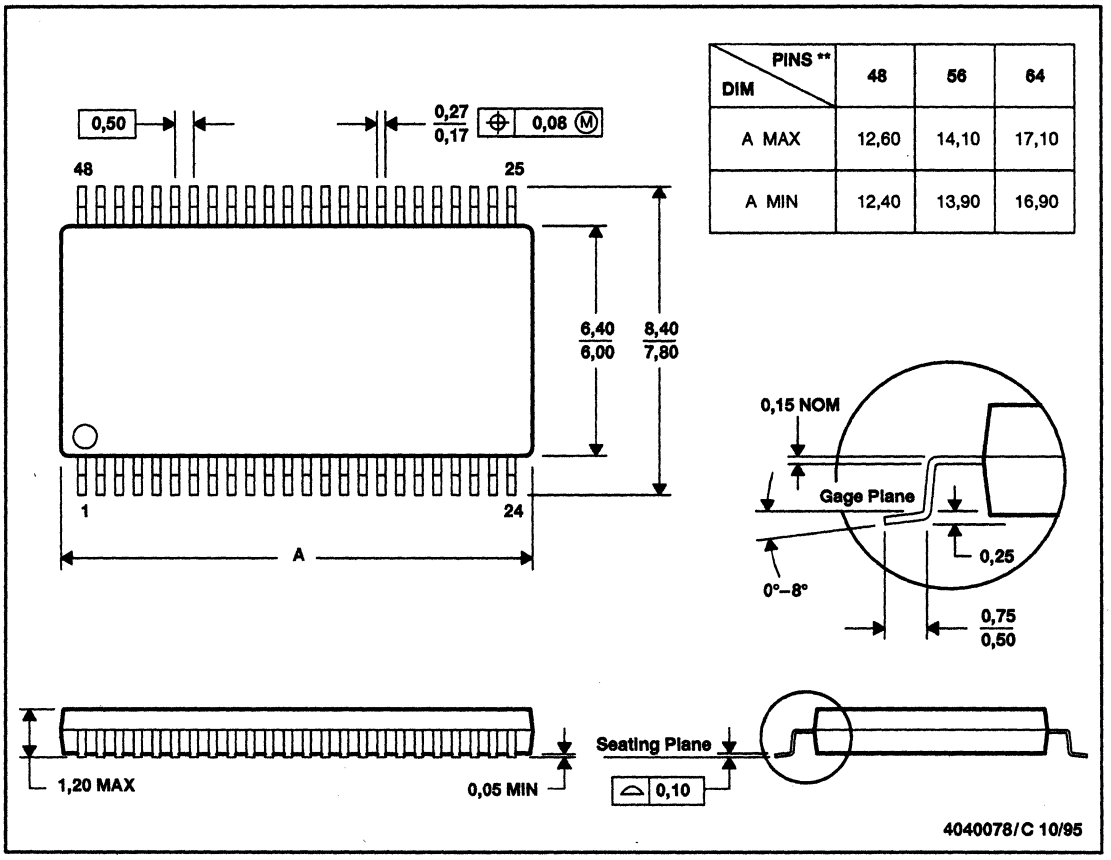
4040212/C 08/95

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PIN SHOWN

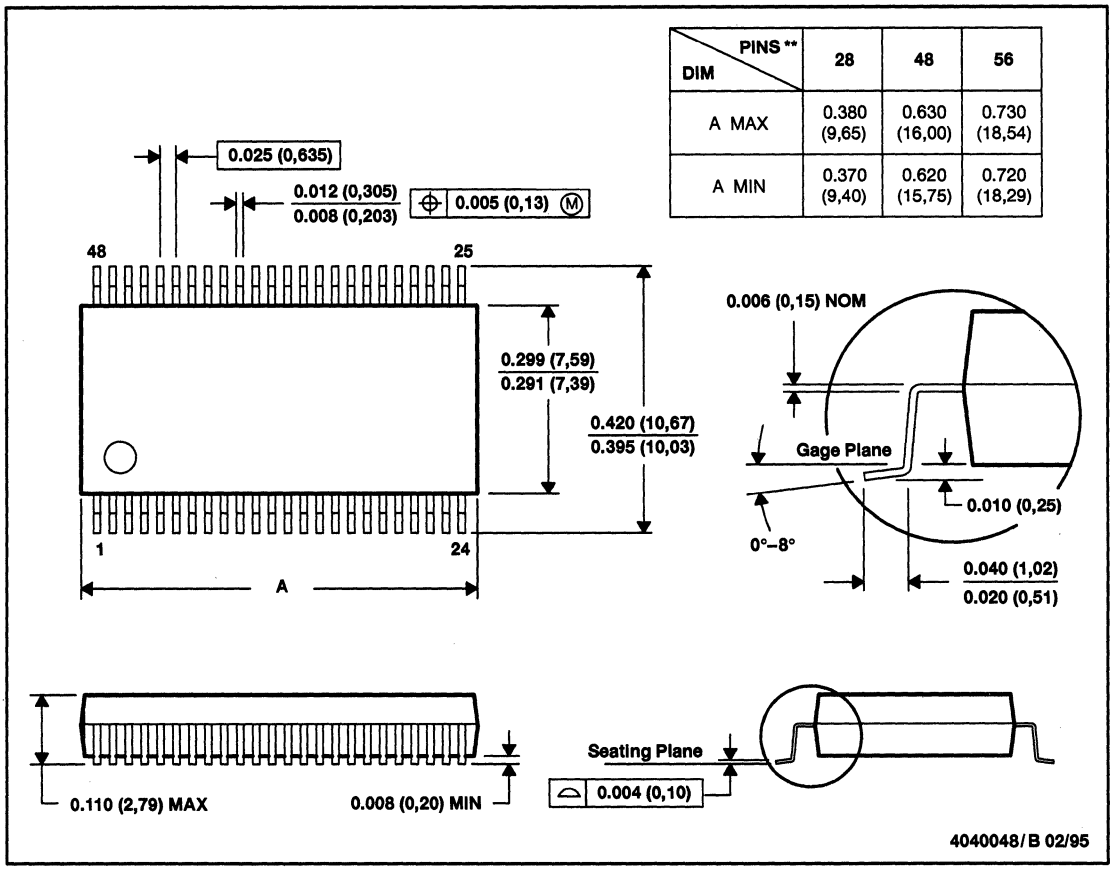


DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-153

DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

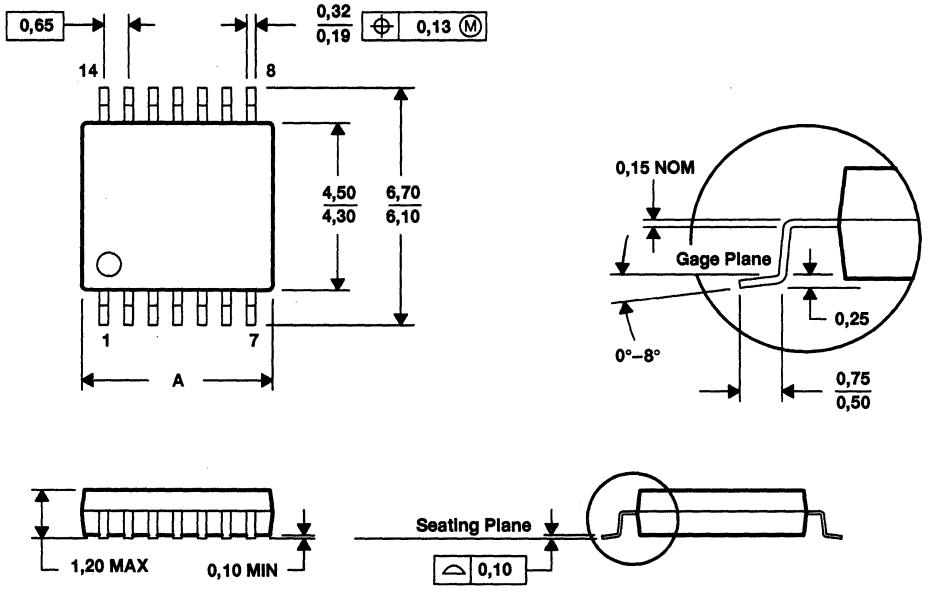
48 PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/D 10/95

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

NOTES