Data Book

Portable Products (PP)

2000

TEXAS INSTRUMENTS

Benchmarq Products from Texas Instruments

Portable Products (PP)

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2000

Analog and Mixed-Signal

On October 15, 1999, Texas Instruments strengthened its ability to provide you with truly premier Power Management solutions. We are proud to announce the acquisition of Power Management expert Unitrode and Battery Management expert Benchmarq.

As you may know, Unitrode has a 40-year history of designing and supplying Power Management components and subsystems. Benchmarq, based in Dallas and acquired by Unitrode last year, has won multiple awards for its industry-leading Battery Management solutions.

TI's commitment to the Power Management marketplace is already evident in its growing portfolio of industry-leading low dropout regulators, supply voltage supervisors, low-power DC-DC converters, power distribution switches and processor power products. Now, with the combination of TI's and Unitrode's high-performance products and TI's leading-edge process technologies and packaging expertise, we are positioned to provide you with easy-to-use, high-performance Power Management solutions.

Unitrode brings a family of products that complements TI's existing portfolio. TI's worldwide network of service and support increases access to and support for the Unitrode and Benchmarq portfolios. Most important, Unitrode brings to this union hundreds of experienced employees dedicated to the Power Management market.

What's in this for you? TI and Unitrode designers are working together right now to develop next-generation Power and Battery Management solutions. Maybe you're looking for easy-to-design-in, turn-key solutions. Or perhaps you need high-performance products, and complete systems and applications knowledge so you can put a power system together yourself. Either way, TI is dedicated to satisfying all of your Power Management needs today and in the future.

The combined TI and Unitrode Power Management offering comprises a rich portfolio that we intend to build upon together. To find out more, including ordering samples, you can visit our website at **www.ti.com/sc/powerleader**, complete the enclosed reply card, or call us for more information, using the TI contact information found on the back cover of this book.

Using Unitrode Data Books

Data sheets and other information about Unitrode's products are organized, by business line, into four volumes: Interface (IF), Portable Power (PP), Power Supply Control (PP), and Nonvolatile SRAMs and Real-Time Clocks (NV).

Each book contains general information as well as sections devoted to the specific business line. Information in these books is referenced in several ways.

Information Source	Volume/ Page Location			
	IF	NV	PP	PS
Data Sheet Types	v	v	v	v
Table of Contents	vi	vi	vi	vi
Master Part Number Index	1-1	1-3	1-3	1-1
Master Application Note Index by Part Number	1-19	1-19	1-19	1-20
Master Application Note Index by Publication Number	1-24	1-24	1-24	1-25
Master Application Note Index by Subject	1-28	1-28	1-28	1-29
Unitrode Product Portfolio	7-1	10-1	6-1	10-1
Product Cross-Reference Tables (NV Book Only)	–	3-2 4-2 5-2	–	–
Ordering Information	2-1	2-1	2-1	2-1

Reading the Indices

The master indices, contained in all four data books, list the location of all data sheets. Each entry is preceded by one of the following 2-letter abbreviations:

- **IF** Interface
- **NV** Nonvolatile SRAMs and Real-Time Clocks
- **PP** Portable Power
- **PS** Power Supply Control

Unitrode's Products

Unitrode Corporation is a world leader in the design and manufacture of innovative, high-performance linear and mixed-signal ICs and modules. This data book introduces the Company's products designed for commercial, industrial, consumer, and military/aerospace applications.

Focused on power management, battery management, and high-speed data communications, products include:

- Off-line power management
- DC/DC power management
- Protection/supervisory circuits
- Portable power management
- Motion/motor controls
- High-speed interface
- Nonvolatile controllers and NVSRAMs
- Real-time clocks

Unitrode also offers an assortment of special function ICs, including fiber-to-curb ringers, CAN transceivers, IrDA transceivers, cellular power-management products and pager/PDA power controllers.

All Unitrode products are backed by design and applications teams that understand the interaction between the Company's products and rest of the power system/subsystem. Unitrode designs technically advanced products in response to customer needs and in anticipation of market trends.

Whatever the application—Power Management, Battery Management, or Ultrafast Data Communications—Unitrode is an innovative, dependable, and customer-driven source for catalog, semi-custom, and custom linear/mixed-signal ICs and modules.

Worldwide Service

Unitrode serves its customers around the world from many locations:

- Design centers in New Hampshire, Texas, California, and North Carolina
- A facility in Dallas for assembly and manufacturing
- A facility in Singapore for testing, assembly subcontractor coordination, and customer service
- A worldwide network of manufacturers' representatives and distributors

Process Capabilities

Unitrode's bipolar process, optimized for both precision-analog and power functions, is constantly updated with the latest process options, such as:

- Operating-voltage ranges from 4–65V
- Schottky and integrated injection logic
- Ion implant
- Thin-film resistors for high accuracy
- Double-level metallization for high-density, high-current layouts and buried zener reference

The Company's BiCMOS process is ideal for high-density linear and mixed-mode designs, especially where speed and low power-consumption are of primary importance.

Options include:

- 3-, 2.5-, and 1-micron processes
- Up to 15V operation
- High-current, double-level metallization
- 125 fully isolated, vertical NPN transistors
- Thin-film resistors

This year, a new BCDMOS process offers all the options available with BiCMOS, as well as a lateral DMOS device with up to 35V operation for added power-handling capability.

An ISO9001 and 9002 Firm

Unitrode was one of the first U.S. linear/analog manufacturers to achieve IS/ISO 9001/EN29001 registration, and in 1998, the registrars completed recertification of the Merrimack and Singapore facilities and renewed the Company's registration to ISO 9001/9002-1994, respectively.

To be registered, the Company passed a rigorous examination of its quality systems—from product design through shipment. These registrations thus assure customers all over the world that Unitrode is adhering to very high, precisely defined standards.

Listening To Customers

To develop custom and semi-custom parts, Unitrode design engineers work very closely with customers, so all requirements are accurately understood, all possibilities are fully explored, and all products meet or exceed specified needs.

Unitrode also pays careful attention to customers and markets to help guide its development of catalog parts. Continuing close contact makes it possible to anticipate industry requirements, and to create devices that satisfy them.

Important Notice

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

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Product Production Status

The table below defines three types of data sheets issued at various stages of product development. Unitrode reserves the right to change products without notice to improve design performance, reliability, or manufacturability.

CLASSIFICATION	PRODUCT STAGE	DESCRIPTION
Advance Information Data Sheet	Formative or Design	This document contains the design specifications for product under development. Specifications may be changed in any manner without notice.
Preliminary Data Sheets	First Production	Supplementary data may be published at a later date. Unitrode reserves the right to make changes at any time without notice, in order to improve design and supply the best product possible.
No Classification Noted	Full Production	Product is in full production.


UNITRODE

Table of Contents

INDEX

Master Part Number and Application Indices

Numeric Master Part Index

Part numbers are listed numerically, not by prefix (bq, DV, EV, UC, UCC).
*Products included in this book are listed in **bold**.*

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Application/Design Notes by Publication Number

Pub.	Title	IC Featured	Volume/Page
DN-19	A Simple Isolation Amplifier using the UC1901	UC3901	PS/7-64
DN-26	UC3842A - Low Cost Startup and Fault Protection Circuit	UC3842A/3A/4A/5A	PS/3-464
DN-27	UC1842/UC1842A Summary of Functional Differences	UC3842/3/4/5	PS/3-466
DN-28	UC3840/UC3841/UC3851 PWM Controllers - Summary of Functional Differences	UC3841	PS/3-467
DN-29	UC3842A Family Frequency Foldback Technique Provides Protection	UC3842A/3A/4A/5A	PS/3-468
DN-30	Programmable Electronic Circuit Breaker	UC3842A/3A/4A/5A	PS/3-469
DN-32	Optocoupler Feedback Drive Techniques	UC3832/3	PS/5-41
DN-33	Optocoupler Feedback Drive Techniques Using the UC3901 and UC3903	UC3903	PS/7-65
DN-35	IGBT Drive Using MOSFET Gate Drivers	UC3708	PS/6-85
DN-36	UC1525B/1527B Devices - Comparison Summary to UC1525A/1527A Devices	UC3525A/27A	PS/3-470
DN-38	Unique Converter for Low Power Bias Supplies	UC494/5A&C	PS/3-471
DN-39E	Optimizing Performance in UC3854 Power Factor Correction Applications	UCC3857	PS/4-76
DN-40	The Effects of Oscillator Discharge Current Variations on Maximum Duty Cycle and Frequency in UC3842 and UC3842A PWM ICs	UC3842/3/4/5	PS/3-473
DN-41	Extend Current Transformer Range	UC3854	PS/4-81
DN-42A	Design Considerations for Transitioning from UC3842 to the New UCC3802 Family	UCC3800/1/2/3/4/5	PS/3-476
DN-43	Simple Techniques to Generate a Negative Voltage Bias Supply from a Positive Input Voltage	UCC3800/1/2/3/4/5	PS/3-479
DN-44	UC3854A and UC3854B Advanced Power Factor Correction Control ICs	UC3854A/B	PS/4-83
DN-45	UC3846, UC3856 and UCC3806 Push-Pull PWM Current Mode Control ICs	UCC3806	PS/3-480
DN-45	UC3846, UC3856 and UCC3806 Push-Pull PWM Current Mode Control ICs	UC3856	PS/3-480
DN-46	Highly Efficient Low Power DC to DC Inverter Converts +5V Input to -3V Output	UCC3813	PS/3-482
DN-48	Versatile Low Power SEPIC Converter Accepts Wide Input Voltage Range	UCC3813	PS/3-484
DN-49	Easy Switcher Controls SEPIC Converter for Automotive Applications	UC2577	PS/3-487
DN-50	Simple Techniques for Isolating and Correcting Common Application Problems with UC3625 Brushless DC Motor Drives	UC3625	PS/8-111
DN-51	Programming the UCC3806 Features	UCC3806	PS/3-489
DN-52	Adjustable Electronic Load for Low Voltage DC Applications	UC39432	PS/7-76
DN-53A	Design Considerations for Synchronizing Multiple UC3637 PWMs	UC3637	PS/8-115
DN-54	Innovative Buck Regulator Uses High Side N-Channel Switch without Complex Gate Drive	UCC3813	PS/3-492
DN-56A	Single Switch Flyback Circuit Converts +5VDC to +/-12VDC for RS-232 and RS-422 Applications	UCC3800/1/2/3/4/5	PS/3-492
DN-57	Power Dissipation Considerations for the UC3726N/UC3727N IGBT Driver Pair	UC3726	PS/6-87
DN-58	UCC3912 Programmable Electronic Circuit Breaker - Performance Evaluation and Programming Information	UCC3912	IF/5-102
DN-59A	UCC3889 Bias Supply Controller Evaluation Kit - Schematic and List of Materials	UCC3888	PS/3-494
DN-60	UC3726/UC3727 IGBT Driver Pair Evaluation Kit Testing Procedure	UC3726	PS/6-90
DN-61	A High Performance Linear Regulator for Low Dropout Applications	UC3832/3	PS/5-42
DN-62	Switching Power Supply Topology: Voltage Mode vs. Current Mode	UCC35701	PS/3-496
DN-63	The Current-Doubler Rectifier: An Alternative Rectification Technique for Push-Pull and Bridge Converters	UC3875/6/7/8	PS/3-499

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Application/Design Notes by Publication Number

Pub.	Title	IC Featured	Volume/Page
DN-97	UCC39411 Low Power Synchronous Boost Converter Evaluation Kit, Schematic and Bill of Materials	UCC39411/2/3	**PP/7-106**
DN-98	UCC3917 Positive Floating Hot Swap Power Manager Evaluation Kit, Schematic and Bill of Materials	UCC3917	IF/5-120
DN-99	Pulse Edge Transmission (PET) circuit	UCC3961	PS/8-102
DN-501	Using RAM Clear Function with bq3285/bq3287A RTCs	bq3285/bq3287	NV/4-321
DN-502	High-Side Current Sensing with Benchmarq Portable Power Fast-Charge Control IC		**PP/3-307**
U-100A	UC3842/3/4/5 Provides Low-Cost Current-Mode Control	UC3842/3/4/5	PS/3-532
U-102	UC1637/2637/3637 Switched Mode Controller for DC Motor Drive	UC3637	PS/8-126
U-104	Improved Charging Methods for Lead-Acid Batteries using the UC3906	UC3906	**PP/3-388**
U-110	1.5MHz Current Mode IC Controlled 50W Power Supply	UC3825	PS/3-546
U-111	Practical Considerations in Current Mode Power Supplies	UC3709	PS/3-558
U-112	A High Precision PWM Transconductance Amplifier for Microstepping using Unitrode's UC3637	UC3637	PS/8-137
U-113	Design Notes on Precision Phase Locked Speed Control for DC Motors	UC3634	PS/8-145
U-115	New Integrated Circuit Produces Robust, Noise Immune System for Brushless DC Motors	UC3625	PS/8-155
U-118	New Driver ICs Optimize High Speed Power MOSFET Switching Characterisitics	UC3709	PS/6-92
U-120	A Simplified Approach to DC Motor Modeling for Dynamic Stability Analysis	UC3638	PS/8-162
U-122	A New Family of Integrated Circuits Controls Resonant Mode Power Converters	UC3861-8	PS/3-576
U-127	Unique Chip Pair Simplifies High Side Switch Drive	UC3725	PS/6-107
U-128	The UC3823A,B & UC3825A,B Enhanced Generation of PWM Controllers	UC3823/5A/B/3	PS/3-585
U-129	UC3907 Load Share IC Simplifies Parallels Power Supply Design	UC3907	PS/7-84
U-130	Dedicated ICs Simplify Brushless DC Servo Amplifier Design	UC3625	PS/8-166
U-131	Simple Switchmode Lead-Acid Battery Charger	UC3906	**PP/3-417**
U-132	Power Factor Correction Using the UC3852 Controlled ON-Time Zero Current Switching Technique	UC3852	PS/4-98
U-133A	UCC3800/1/2/3/4/5 BiCMOS Current Mode Control ICs	UCC3800/1/2/3/4/5	PS/3-594
U-134	UC3854 Controlled Power Factor Correction Circuit Design	UC3854	PS/4-114
U-135	The UC3848 Average Current Mode Controller Squeezes Maximum Performance from Single Switch Converters	UC3848	PS/3-612
U-136A	Phase Shifted, Zero Voltage Transition Design Considerations and the UC3875 PWM Controller	UC3875/6/7/8	PS/3-623
U-137	Practical Considerations in High Performance MOSFET, IGBT & MCT Gate Drive Circuits	UC3709	PS/6-122
U-138	Zero Voltage Switching Resonant Power Conversion	UC3861-8	PS/3-637
U-140	Average Current Mode Control of Switching Power Supplies	UC3849	PS/3-664
U-141	Resonant Fluorescent Lamp Converter Provides Efficient and Compact Solution	UC3871	**PP/8-27**
U-143C	New Chip Pair Provides Isolated Drive for High Voltage IGBTs	UC3727	PS/6-137
U-144	UCC3806 BiCMOS Current Mode Control IC	UCC3806	PS/3-678
U-148	Dimmable Cold-Cathode Fluorescent Lamp Ballast Design Using the UC3871	UC3871	**PP/8-35**
U-149A	Simple Off-Line Bias Supply for Very Low Power Applications	UCC3888	PS/3-685

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INTERFACE (IF)

Hot Swap Power Managers

SCSI

NONVOLATILE SRAMs AND REAL-TIME CLOCKS (NV)

Real-Time Clocks

PORTABLE POWER (PP)

Battery Charging

Publications included in this book are listed in ***bold.***

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Charge Pumps

Class-D Amplifiers

Control Techniques

Average Current Mode

Peak Current Mode

Voltage Mode

Current Sensing

Distributed Power

Electronic Loads

Feedback Techniques

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Microprocessor Voltage Regulators

Linear Regulators

Switching Regulators

Motor Control

Brush DC Motors

Brushless DC Motors

Phase Locked Loops

Power H-Bridge Design

Small Signal Modeling

Stepper Motors

Optocoupler Isolation

Post Regulation

Power Device Drivers

Publications included in this book are listed in ***bold****.*

Power Factor Correction

PWM Oscillators

Rectification

Resonant Converters

Ring Generator Controllers

Publications included in this book are listed in ***bold.***

Secondary Side Regulation

Small Signal Analysis

Subharmonic Oscillation

Supervisory Functions

Switching Regulators - Reference Designs

Flyback Converters

Forward Converters

Non-Isolated Buck, Boost, Flyback and SEPIC Converters

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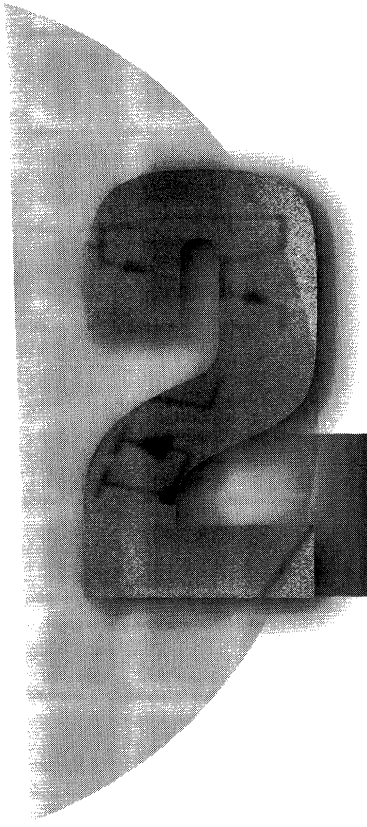
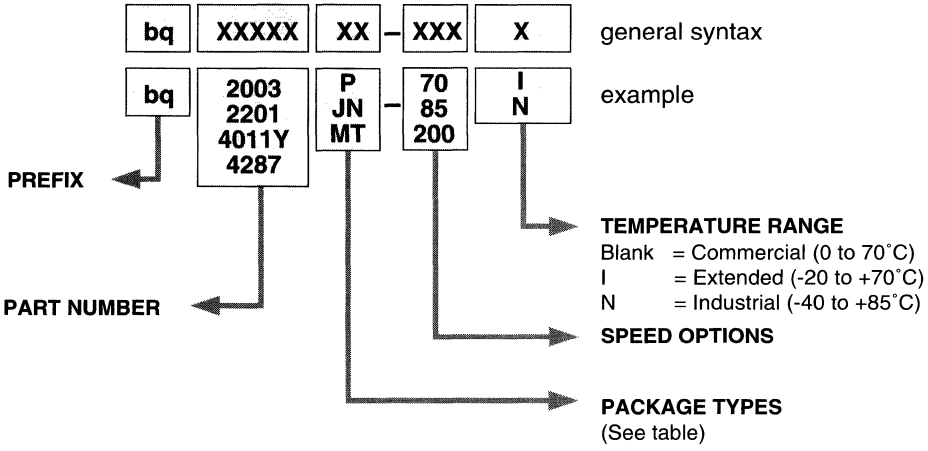


General Information

(see Unitrode ordering information page for "UC" and "UCC" prefix products)



Letter Designator	Package Type
MA	A-Type Module
MB	B-Type Module
MC	C-Type Module
MS	Leaded Chip Carrier for LIFETIME LITHIUM Module
MS	LIFETIME LITHIUM Module Housing
MT	T-Type Module
P	Plastic DIP (600 mil)
PN	Plastic Narrow DIP (300 mil)
S	SOIC (300 mil)
SH	SOH for SNAPHAT Module
SH	SNAPHAT Housing for SOH-28 SNAPHAT Module
SN	Narrow SOIC (150 mil)
SS	SSOP (150 mil)
TS	TSSOP (172 mil)

Ordering Information

(see Benchmarq ordering information page for "bq" prefix products)

UC	XXXXX	XX	XX	XXXX	general syntax
UC	17131 27131 37131	A	J	883B	example

PREFIX
"UC" ~ Linear Integrated Circuits
"UCC" ~ BiCMOS

PART NUMBER
First digit "1" ~ Military Temperature Range*
First digit "2" ~ Industrial Temperature Range*
First digit "3" ~ Commercial Temperature Range*
(*consult individual data sheets for specific temperature ranges on each part)

SCREEN/PROCESSING OPTIONS
"883" ~ MIL-STD-883
Class Q of MIL-PRF-38535

PACKAGE OPTIONS

OPTIONAL GRADES
A or B ~ Improved Version

Letter Designator	Package Type
D	Plastic Narrow Body (150 mil) SOIC
DW	Plastic Wide Body (300 mil) SOIC
DP	Plastic Narrow Body Power SOIC
DS	Plastic Narrow Body (150 mil) SOIC with Shunt Current Sense
DWP	Plastic Wide Body Power SOIC
FP	Power Plastic Metric Quad Flatpack (MQFP)
FQ	Power Low Profile Quad Flatpack (LQFP)
FQP	Power Plastic Low Profile Quad Flatpack (LQFP)
J	Ceramic Dual-in-Line (300 mil and 600 mil)
L	Ceramic Leadless Chip Carrier
LP	Power LCC
M	Quasi Shrink Small Outline (150 mil body, 0.635mm pitch)
MWP	Power Quasi Shrink Small Outline (300 mil body, 0.88mm pitch)
N	Plastic Dual-in-Line (300mil and 600 mil)
P	Mini SOIC
PW	Thin Shrink Small Outline (TSSOP)
PWP	Power TSSOP
Q	Plastic Leadless Chip Carrier (PLCC)
QP	Power (PLCC)
SP	Power Ceramic Dual-in-Line
T	Plastic TO-220
TD	Plastic TO-263 Power Surface Mount
Z	Zig-Zag In-Line Power Package

Quality and innovation characterize our products!

Our commitment begins with our Quality Assurance System. In October 1992, Unitrode Corporation became one of the first in our industry to achieve IS/ISO 9001/EN 29001 Registration. Currently, Unitrode's quality-assurance system exceeds the rigorous requirements of ISO 9001-1994 and MIL-PRF-38535. Quality Management Institute (QMI) has awarded Unitrode a Certificate of Registration (Number 003889) indicating compliance with ISO 9001, for the design and manufacture of analog integrated circuits. For its Singapore branch, Unitrode also holds an ISO 9002 Certificate of Registration (Number 93-2-0148) from the Singapore Productivity and Standards Board, for semiconductor IC manufacturing, factory inspection and testing, and wafer-probe testing.

In August 1996, the Defense Supply Center-Columbus (DSCC) granted Unitrode full Q-Level certification to MIL-PRF-38535 for listing on the Qualified Manufacturers List (QML). In addition, DSCC continued Unitrode's laboratory suitability by certifying that our test methods accord with MIL-STD-883.

All Unitrode products and manufacturing processes meet extensive qualification requirements. Qualification ensures that

- Customer and/or design requirements are translated efficiently into manufacturing requirements
- All groups are integrated, coordinated, and capable
- Our processes are manufacturable
- Our products meet or exceed the reliability requirements of our customers

Process Qualification

When a process qualification is required, Quality Assurance organizes a cross-functional team that prepares and completes a formal qualification plan according to QP 2515. Key requirements for major processes include

- Documented design rules and process specifications; process and device simulation with full SPICE models
- Completed process control plan with identified critical, significant, and non-critical characteristics
- Implemented process-control charts
- Demonstrated Cp, and Cpk for significant and critical characteristics
- Documented out-of-control action plans (OCAPs)
- Completed quality audit
- Process-acceptance criteria
- Gage R&R studies
- Construction analyses

Reliability Testing

Our extensive reliability requirements ensure that our new processes demonstrate, for commercial products under typical use conditions, a 200 FIT rate or better (failures in time calculated at 70°C, 0.7eV activation energy, 60% confidence) at the time of qualification, using a minimum of three wafer lots. Figure 1, on page 2-6, lists typical reliability tests performed for new major processes.

Package Qualification

Whenever a new package is introduced, in addition to qualifying the manufacturing process using requirements appropriate to assembly processing, Unitrode performs a complete battery of reliability tests.

Figure 2, on page 2-7, depicts typical requirements for plastic packages. Figure 3, on page 2-8, presents the requirements for hermetic packages.

Product Qualification

New products must be manufactured using qualified processes and packages. Unitrode's new product qualification consists of 2 major milestones: Release For Introduction (RFI) and Release to Production (RTP).

RFI is the term Unitrode uses to describe devices that

- Are built on a qualified process
- Meet the preliminary data sheet over the specified temperature range
- Demonstrate no infant mortality
- Have been verified in the appropriate application
- Have had ESD measured and classified
- Have a released preliminary test program

Devices that achieve RTP meet all the RFI requirements (plus additional requirements) and complete Unitrode's product qualification. Typical RTP requirements include

- Bench and temperature characterization
- Demonstrated compliance to all data-sheet parameters
- Cp, Cpk targets met for all untrimmed parameters in data sheet
- Test program complete and released to production
- Machine capability less than 5% of the device specification range
- Test schematic(s), test program(s), bonding diagram(s), and burn-in diagrams approved and released
- ESD measured and classified (human body model)
- Passed latch-up and HTOL test to 1000 hours
- Final data sheet approved and released.

Results

As a result of our comprehensive qualification procedures, we are able to report long-term device reliability of 4.0 FIT or lower for combined functional families. This figure is estimated from millions of hours of life-testing at accelerated temperatures.

Failure Analysis

If we do experience a failure during pre-production qualification, we have an extensive failure-analysis lab to determine and fix the root cause before the products reach our customers. We begin by verifying the failure to published specifications. We provide written failure-verification to our customers within 72 hours.

This notification is followed by failure-mode identification through laboratory analyses such as electrical measurements, optical and electron microscopy, radiography, device deprocessing, microsectioning, spectrometry, and cholesteric liquid-crystal analysis. Unitrode maintains a ten-day cycle to identify moderately complex failures from receipt of failed units.

If needed, closed-loop corrective action is managed through our Corrective Action Continuous Improvement Team using the 8D approach.

Customer Notification

Our continuous improvement requires an occasional product or process change. Unitrode notifies the customer (a 90-day notification whenever possible) when

- A waiver to a customer's or Unitrode's specification is required before shipment of material deemed suitable by Unitrode or our customer
- Any product, process or mask change requires a change to Unitrode's data sheet, SCD, Purchase Order, or customer specification
- Any product, process or mask change reduces ESD rating
- A change occurs in manufacturing location, including wafer fabrication, assembly, and test
- There is a change in wafer starting material, dieletric, passivation or metalization materials and certain assembly materials
- A major change occurs in manufacturing process on a critical or significant characteristic, according to our process control plan(s)
- A manufacturing process changes a characteristic that is a reliability concern
- Unitrode's operating procedures or quality systems change significantly

Total Business Excellence

Unitrode's policy of Total Business Excellence (TBE) goes well beyond the scope of Quality Assurance. A company demonstrating Total Business Excellence must have more rigorous business practices than industry standards and a supporting culture to enable and improve these practices.

TBE requires continuous improvement. It is a never-ending search for ways to improve everything we do, and a pledge to ultimately translate improvements into better products and services for our customers.

Our goals include improved designs that meet the broadest spectrum of application needs, improved translation of customer requirements into actual product performance characteristics, improved understanding of process capabilities to improve the product introduction process, higher productivity, less scrap and rework, and lower production costs.

For example, Unitrode internal qualification procedures now include rigorous qualification of our suppliers, subcontractors, and the wafer fabrication (both major new processes and unit processes). Each qualification is managed by a cross-functional quality team. Qualification requirements include detailed and advanced process control plans, out-of-control action plans (OCAPs), demonstrated process-capability, advance statistical process-control techniques, and Gage R&R studies.

We've improved many of our internal practices: for example, shop floor control, document management, customer notification, and corrective action. We've replaced our old hardcopy system with electronically based systems using the best software systems and relational databases.

Total Business Excellence affects every department, activity, and product, from initial concept to end-user installation and operation.

For all of these reasons we deliver high-quality, reliable products. Our continuing quest to improve everything we do yields better and more reliable products and services for our customers. That is what earns customer loyalty!

Figure 1. Typical Reliability Tests for New Processes

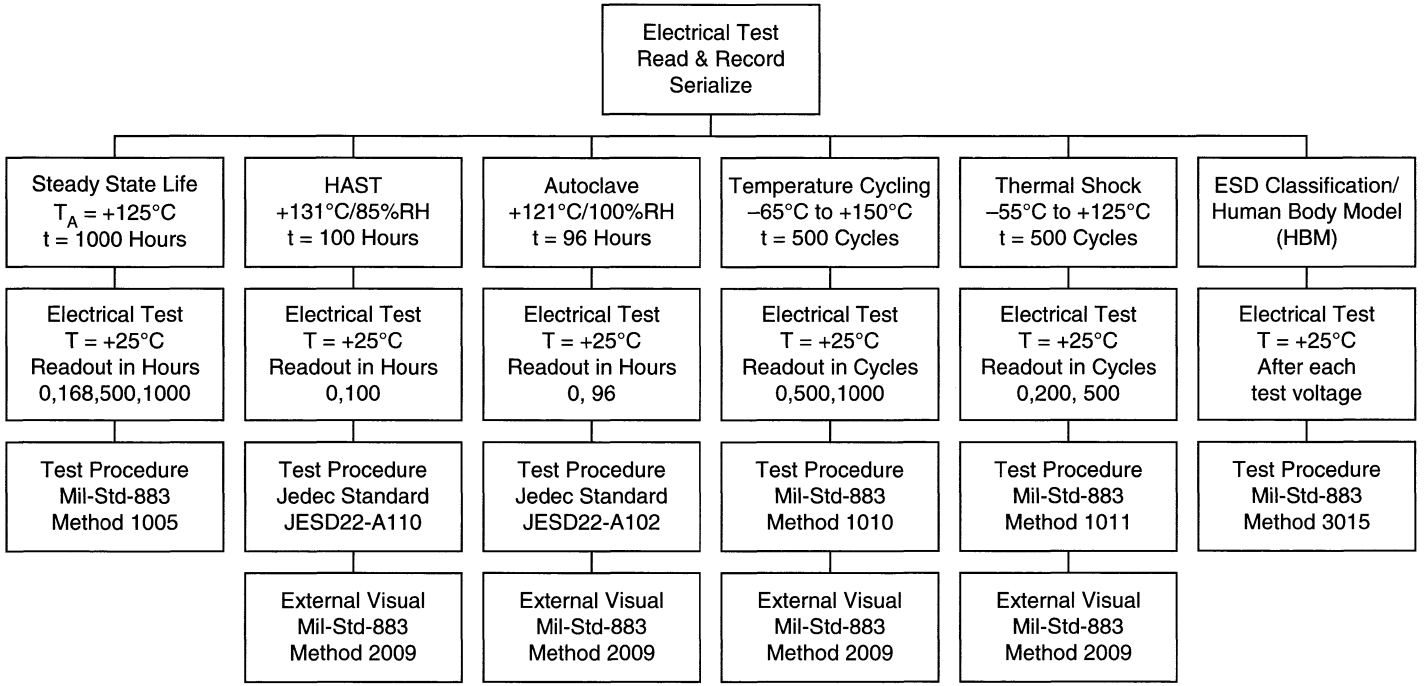
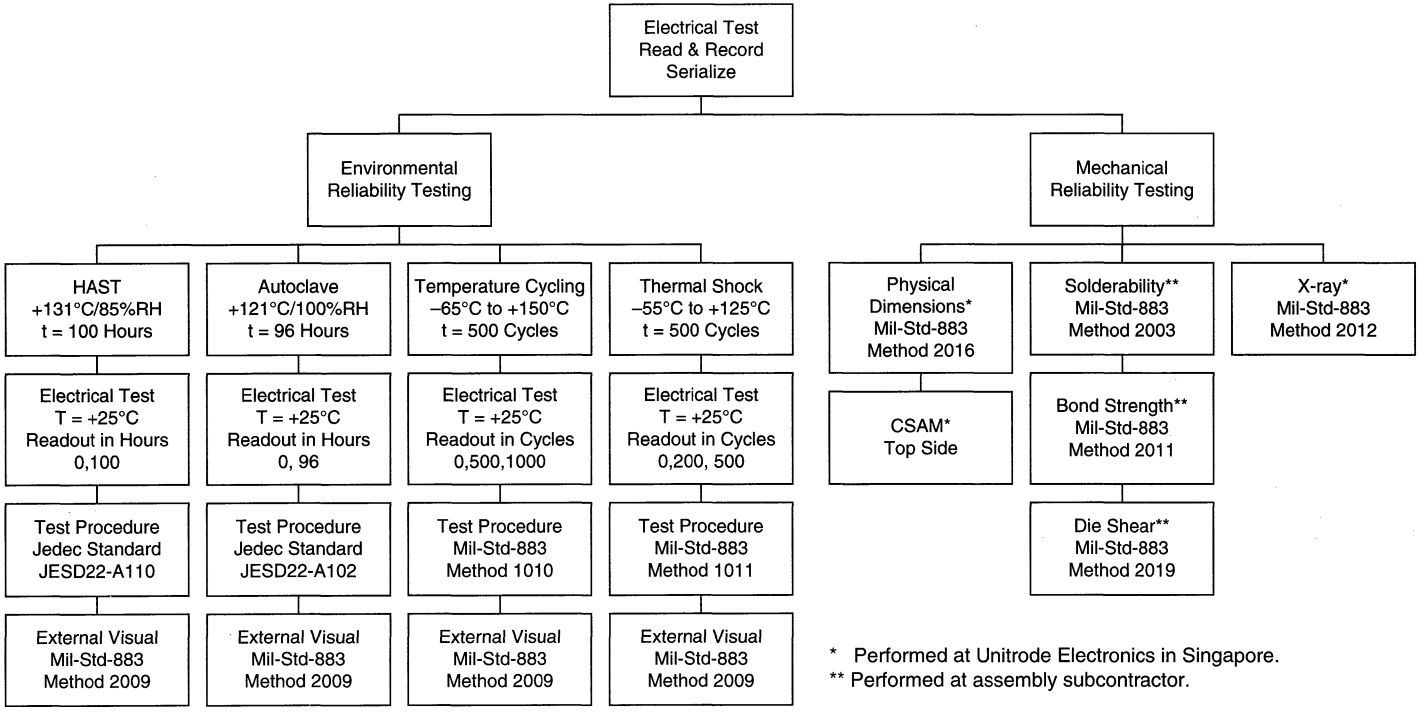
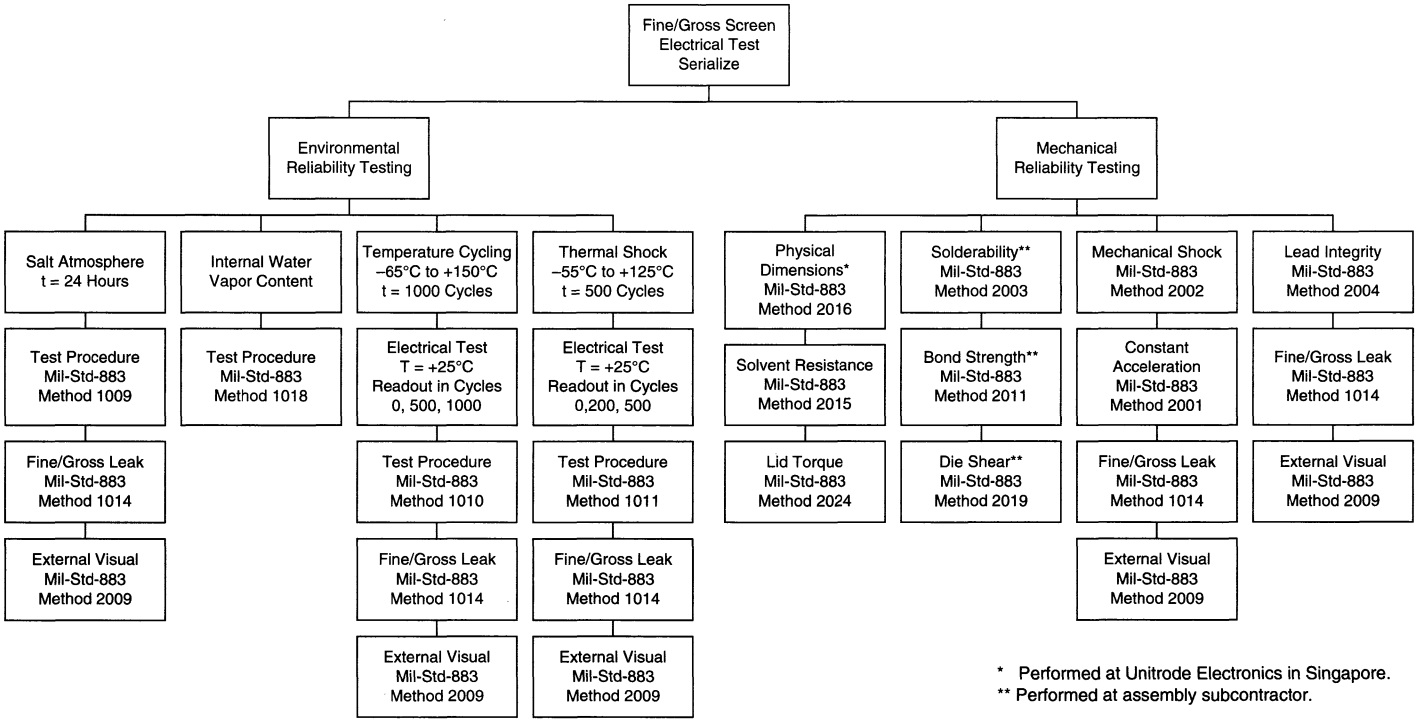


Figure 2. Typical Reliability Requirements for Plastic Packages



* Performed at Unitrode Electronics in Singapore.
** Performed at assembly subcontractor.

Figure 3. Typical Reliability Requirements for Hermetic Packages



* Performed at Unitrode Electronics in Singapore.
** Performed at assembly subcontractor.

Description

Unitrode offers most of our products in die and/or wafer form through our die distributors. Unitrode's die utilize either linear bipolar or BiCMOS process technology featuring tight beta controls and resistor matching techniques.Die thickness is either 12 mils or 15 mils, +/- 1 mil. Interconnects are an alloy of copper and aluminum (to reduce the possibility of electromigration). Most product's backside material is pure silicon.

Testing

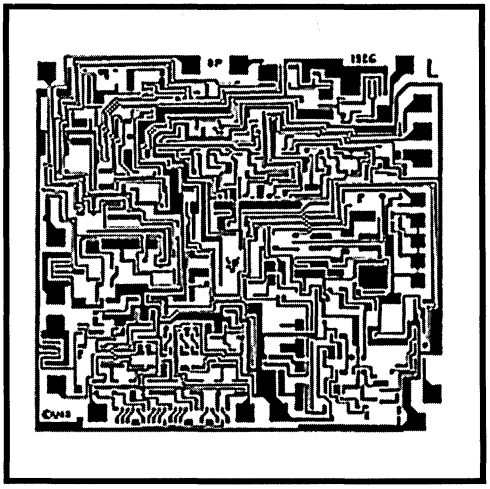
All products are tested at two separate points: (1) wafer process parameter in-line probing and (2) ambient electrical test probing. Die are tested to full data sheet specifications, with the exception of some high power or high speed devices where production probe equipment limit the test environment.

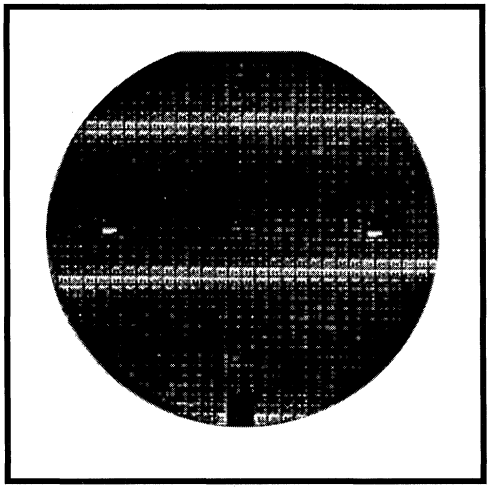
Inspection

Unitrode performs visual inspections on military grade die to MIL-STD-883, Method 2010, conditions A or B, or to individual customer specifications. Die is supplied in "waffle pack" or single wafer form. Standard wafers are 100 mils, generic 4- or 6-inch diameter.

Ordering

Product is available from Unitrode's authorized die distributors, and part numbers end with the suffix "c" for chip form or "chipwfr" for wafer form.



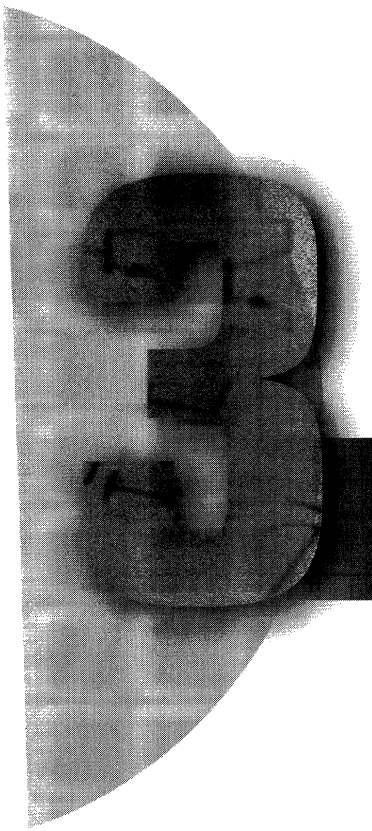


Battery Charge-Management ICs

Power-Management ICs

Pack Protection and Supervisory ICs


UNITRODE



Battery Charge-Management ICs

Battery Charge-Management ICs Selection Guide

Unitrode battery charge-management ICs provide full-function, safe charge control for all types of rechargeable chemistries. Functions include pre-charge qualification and conditioning, charge regulation, and termination.

- ➤ Fast charging and conditioning of nickel cadmium, nickel metal hydride, lead acid, lithium ion, or rechargeable alkaline batteries
- ➤ Flexible charge regulation support:
  - – Linear
  - – Switch-mode
  - – Gating control (external regulator)
- ➤ Easily integrated into systems or as a stand-alone charger
- ➤ Direct LED outputs display battery and charge status
- ➤ Fast, safe, and reliable chemistry-specific charge-termination methods, including rate of temperature rise ($\Delta T/\Delta t$), negative delta voltage ($-\Delta V$), peak voltage detect (PVD), minimum current, maximum temperature, maximum voltage, and maximum time
- ➤ Optional top-off and maintenance charging
- ➤ Discharge-before-charge option for NiCd

Battery Charge-Management Selection Guide

Battery Technology	Key Features	Fast-Charge Termination Method	Pins / Package	Part Number	Page Number
Multi-Chemistry	Complete change management with integrated switching controller	PVD, minimum current, maximum temperature, maximum time	8/0.300" DIP, 8/0.150" SOIC	bq2000+	3-7
		$\Delta T/\Delta$, minimum current, maximum temperature, maximum time	8/0.300" DIP, 8/0.150" SOIC	bq2000T+	3-20
NiMH, NiCd	Gating control of an external regulator	$-\Delta V$, PVD, maximum temperature, maximum time	8/0.300" DIP, 8/0.150" SOIC	bq2002/C/E/F/G	3-3
		$\Delta T/\Delta t$, maximum temperature, maximum time	8/0.300" DIP, 8/0.150" SOIC	bq2002D/T	3-3
	PWM Controller	$-\Delta V$, $\Delta T/\Delta t$, maximum temperature, maximum time	16/0.300" DIP, 16/0.300" SOIC	bq2003	3-73
	PWM controller, enhanced display mode	$-\Delta V$, PVD, $\Delta T/\Delta t$, maximum temperature, maximum time	16/0.300" DIP, 16/0.150" SOIC	bq2004/E/H	3-5
	Dual sequential charge-controller for 2-bay chargers	$-\Delta V$, $\Delta T/\Delta t$, maximum temperature, maximum time	20/0.300" DIP, 20/0.300" SOIC	bq2005	3-119
Lithium Ion	PWM controller	Minimum current, maximum time	16/0.300" DIP, 16/0.150" SOIC	bq2054	3-6
	Low-dropout linear with AutoComp™ feature	-	8/0.150" SOIC	bq2056/T/V	3-186
	PWM controller, enhanced display mode	Minimum current, maximum time	16/0.300" DIP, 16/0.150" SOIC	bq2954+	3-6
	PWM controller, differential current sense	Minimum current, maximum time	20/0.300" DIP, 20/0.300" SOIC	UCC3956	3-6

+ New Product

Continued on next page

Battery Charge-Management Selection Guide (Continued)

Battery Technology	Key Features	Fast-Charge Termination Method	Pins/ Package	Part Number	Page Number
Lead Acid	PWM controller, 3 charge algorithms	Maximum voltage, $-\Delta^2V$, minimum current, maximum time	16/0.300" DIP, 16/0.150" SOIC	bq2031	3-154
	Linear controller	Maximum voltage, minimum current	16/0.300" DIP 16/0.300"SOIC	UC3906	3-237
	PWM controller, differential current sense	Maximum voltage, minimum current	20/0.300" DIP 20/0.300"SOIC	UC3909	3-244
Rechargeable Alkaline	2-cell charging	Maximum voltage	8/0.300"DIP, 8/0.150" SOIC	bq2902	3-194
	3- or 4-cell charging	Maximum voltage	14/0.300" DIP, 14/0.150" SOIC	bq2903	3-204

bq2002 Family Selection Guide

The bq2002 fast-charge control ICs are low-cost CMOS battery charge-control ICs providing reliable charge termination for both NiCd and NiMH battery applications. Controlling a current-limited or constant-current supply allows the ICs to be the basis for a cost-effective stand-alone or system-integrated charger. The bq2002 family includes options that integrate fast charge, top-off, and pulse-trickle charge control in a single IC for charging one or more NiCd or NiMH batteries.

A new charge cycle is started by the application of a charging supply or by replacement of the battery. For safety, fast charge is inhibited if the battery voltage or temperature is outside of configured limits. Fast charge may be inhibited using the INH input. In some versions, this input may be used to synchronize voltage sampling. A low-power standby mode reduces system power consumption.

- Fast-charge control of nickel cadmium or nickel-metal hydride batteries
- Fast-charge terminations available:
  - $-\Delta V$
  - Peak Voltage Detection (PVD)
  - $\Delta T/\Delta t$
- Direct LED output displays charge status
- Backup safety termination on maximum voltage, maximum temperature, and maximum time
- Top-off and pulse-trickle charge rates available
- Synchronized voltage sampling available
- Low-power mode
- 8-pin 300-mil DIP or 150-mil SOIC packaging

	Part Number						
	$-\Delta V$ or PVD Termination					$\Delta T/\Delta t$ Termination	
Feature	bq2002	bq2002F	bq2002C	bq2002E	bq2002G	bq2002T	bq2002D
Fast charge time limit options (minutes)	160/80/40	160/100/40	160/80/40	200/80/40	160/80/40	320/80/40	440/110/55
Hold-off period options (seconds)	600/300/10	600/300/10	300/150/75	300/150/75	300/150/75	none	none
Top-off options	C/32,C/16,0	C/32,C/16,0	none	C/16,0	C/16,0	C/64,C/16,0	none
Top-off period	4.6ms	4.6ms	n/a	1.17s	1.17s	4.6ms	n/a
Pulse-trickle options	C/64,C/32	C/64,C/32	C/32	C/32	C/32	C/256,C/128	none
Pulse-trickle period	9 or 18ms	9 or 18ms	1.17s	1.17s	1.17s	18 or 73ms	n/a
Synchronized voltage sampling	no	no	yes	yes	yes	no	no
Minimum voltage pre-charge qualification	no	no	yes	yes	yes	no	no

Continued on next page

bq2002 Family Selection Guide (Continued)

	Part Number						
	-ΔV or PVD Termination					ΔT/Δt Termination	
Feature	bq2002	bq2002F	bq2002C	bq2002E	bq2002G	bq2002T	bq2002D
Hysteresis on high-temperature cut-off	no	no	no	no	no	yes	yes
LED in "charge pending" phase	n/a	n/a	flashes	flashes	flashes	on	off
Page number	3-35	3-35	3-43	3-61	3-61	3-51	3-51

bq2004 Family Selection Guide

The bq2004 fast-charge control ICs are low-cost CMOS battery charge control ICs providing reliable charge termination for both NiCd and NiMH battery applications. Integration of PWM current control circuitry allows the ICs to be the basis for a cost-effective stand-alone or system-integrated charger. The bq2004 family includes options that integrate fast charge, top-off, and pulse-trickle charge control in a single IC for charging one or more NiCd or NiMH batteries.

A new charge cycle is started by the application of a charging supply, replacement of the battery, or a logic-level pulse. For safety, fast charge is inhibited if the battery voltage or temperature is outside of configured limits. Fast charge may be inhibited using the INH input, which also puts the IC into a low-power standby mode, reducing system power consumption.

- Fast-charge control of nickel cadmium or nickel-metal hydride batteries
- Integrated PWM closed-loop current control
- Configurable, direct LED output displays charge status
- Low-power mode
- Top-off and pulse-trickle charging available
- Fast-charge terminations available:
  - $-\Delta V$
  - Peak Voltage Detection (PVD)
  - $\Delta T/\Delta t$
- Backup safety termination on maximum voltage, maximum temperature, and maximum time
- 16-pin 300-mil DIP or 150-mil SOIC packaging

Feature	Part Number bq2004	bq2004E	bq2004H
Maximum time-out selections (minutes)	360/180/90/45/23	325/154/77/39/19	650/325/154/77/39
Hold-off period selections (seconds)	137/820/410/200/100	137/546/273/137/68	273/546/546/273/137
Charge rate during hold-off period	full fast-charge rate	1/8*fast-charge rate	1/8*fast-charge rate
Top-off options	C/2,C/4,C/8,C/16,0	C/2,C/4,C/8,C/16,0	C/4,C/8,C/16,C/32,0
Top-off pulse width/period (seconds)	260/2080	260/2080	260/2080
Top-off duration	MTO	0.235*MTO	0.235*MTO
Pulse-trickle selections	C/32,C/64,0	C/512,0	C/512,0
Pulse-trickle period (ms)	4.17/8.3/16.7/33.3/66.7	66.7/133/267/532	33.3/66.7/133/267
Pulse-trickle pulse width (seconds)	260	260	260
DSEL floating disables pulse-trickle	no	yes	yes
VSEL high disables low-temperature fault threshold	yes	no	no
High-temperature fault threshold	1/4LTF + 3/4 TCO	1/3LTF + 2/3 TCO	1/3LTF + 2/3 TCO
Page number	3-91	3-105	3-105

Li-Ion PWM Charge IC Selection Guide

Feature	Part Number bq2054	bq2954	UCC3956
Charge algorithm	During pre-qualification, the bq2054 charges using a low trickle current if the battery voltage is low. Then it charges using constant current followed by constant volatge. After fast-charge termination, charge is re-initiated by resetting the power to the IC or by inserting a new battery.	Performs similar to the bq2054, but the bq2954 also re-initiates a recharge if the battery voltage falls below a threshold level. This allows the bq2954 to maintain a full charge in the battery at all times.	Uses a 4-step charge algorithm: low-current trickle charge (when the cell voltage is below a user-programmable level); high-current bulk charge; constant-voltage overcharge; optional top-off with user-programmable timer
Current-sensing technique	Low-side current sensing	Low-side and high-side current sensing	Fully differential high-side current sensing can be used up to 20V common mode without the need for external level shifting.
Charge initiation	Application of power or detection of battery insertion	Application of power or detection of battery insertion	One-shot charge initiates charging, or a simple comparator initiates charging on battery insertion.
Detection of deeply discharged (bad) cells	Minimum cell voltage required for fast charge: 2V/cell Trickle-charge period: 1 * MTO	Minimum cell voltage required for fast charge: 3V/cell Trickle-charge period: 0.25 * MTO (for faster detection of bad cells)	User-programmable threshold limits charge current when battery cells are deeply discharged and provides short-circuit protection.
Charge termination based on minimum current	User-programmable minimum current is a ratio of the charging current: 1/10, 1/20, 1/30. A safety charge timer is also available.	User-programmable minimum current is a ratio of the charging current: 1/10, 1/15, 1/20. A safety charge timer is also available.	User-programmable minimum current or user-programmable overcharge timer
Temperature monitoring	Measured using an external thermistor. Fast charge is inhibited if the battery temperature is outside user-configured limits.	Measured using an external thermistor. Fast charge is inhibited if the battery temperature is outside user-configured limits.	No
Status display	3 LEDs for state of charge	2 LEDs or one bi-color LED optimize state of charge	2 LEDs for state of charge including end of charge
Full-charge indication	LEDs indicate full charge after charge termination	LEDs indicate full charge just before charge termination	LEDs indicate full charge on charge termination
Input voltage range	4.5V to 5.5V	4.5V to 5.5V	6.5V to 20V
Typical supply current	2mA	2mA	5mA
Voltage regulation accuracy	±1% at 25°C	±1% at 25°C	±1% at 25°C
Wakeup feature for battery pack protectors	No	Yes	No
Integrated PWM controller	Yes	Yes	Yes
Pins/package	16-pin narrow PDIP or SOIC	16-pin narrow PDIP or SOIC	20-pin SOIC or DIP
Page number	3-170	3-217	3-253

Programmable Multi-Chemistry Fast-Charge Management IC

Features

- Safe management of fast charge for NiCd, NiMH, or Li-Ion battery packs
- High-frequency switching controller for efficient and simple charger design
- Pre-charge qualification for detecting shorted, damaged, or overheated cells
- Fast-charge termination by peak voltage (PVD), minimum current (Li-Ion), maximum temperature, and maximum charge time
- Selectable top-off mode for achieving maximum capacity in NiMH batteries
- Programmable trickle-charge mode for reviving deeply discharged batteries and for post-charge maintenance
- Built-in battery removal and insertion detection
- Sleep mode for low power consumption

General Description

The bq2000 is a programmable, monolithic IC for fast-charge management of nickel cadmium (NiCd), nickel metal-hydride (NiMH), or lithium-ion (Li-Ion) batteries in single- or multi-chemistry applications. The bq2000 detects the battery chemistry and proceeds with the optimal charging and termination algorithms. This process eliminates undesirable undercharged or overcharged conditions and allows accurate and safe termination of fast charge.

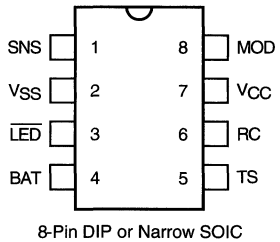
Depending on the chemistry, the bq2000 provides a number of charge termination criteria:

- Peak voltage, PVD (for NiCd and NiMH)
- Minimum charging current (f or Li-Ion)
- Maximum temperature
- Maximum charge time

For safety, the bq2000 inhibits fast charge until the battery voltage and temperature are within user-defined limits. If the battery voltage is below the low-voltage threshold, the bq2000 uses trickle-charge to condition the battery. For NiMH batteries, the bq2000 provides an optional top-off charge to maximize the battery capacity.

The integrated high-frequency comparator allows the bq2000 to be the basis for a complete, high-efficiency power-conversion circuit for both nickel-based and lithium-based chemistries.

Pin Connections



8-Pin DIP or Narrow SOIC or TSSOP

PN-2000.eps

Pin Names

SNS	Current-sense input	TS	Temperature-sense input
V_{SS}	System ground	RC	Timer-program input
$\overline{LED}$	Charge-status output	V_{CC}	Supply-voltage input
BAT	Battery-voltage input	MOD	Modulation-control output

Pin Descriptions

SNS **Current-sense input**

Enables the bq2000 to sense the battery current via the voltage developed on this pin by an external sense-resistor connected in series with the battery pack

V_{SS} **System Ground**

$\overline{LED}$ **Charge-status output**

Open-drain output that indicates the charging status by turning on, turning off, or flashing an external LED

BAT **Battery-voltage input**

Battery-voltage sense input. A simple resistive divider, across the battery terminals, generates this input.

TS **Temperature-sense input**

Input for an external battery-temperature monitoring circuit. An external resistive divider network with a negative temperature-coefficient thermistor sets the lower and upper temperature thresholds.

RC **Timer-program input**

RC input used to program the maximum charge-time, hold-off period, and trickle rate during the charge cycle, and to disable or enable top-off charge

V_{CC} **Supply-voltage input**

MOD **Modulation-control output**

Push-pull output that controls the charging current to the battery. MOD switches high to enable charging current to flow and low to inhibit charging- current flow.

Functional Description

The bq2000 is a versatile, multi-chemistry battery-charge control device. See Figure 1 for a functional block diagram and Figure 2 for a state diagram.

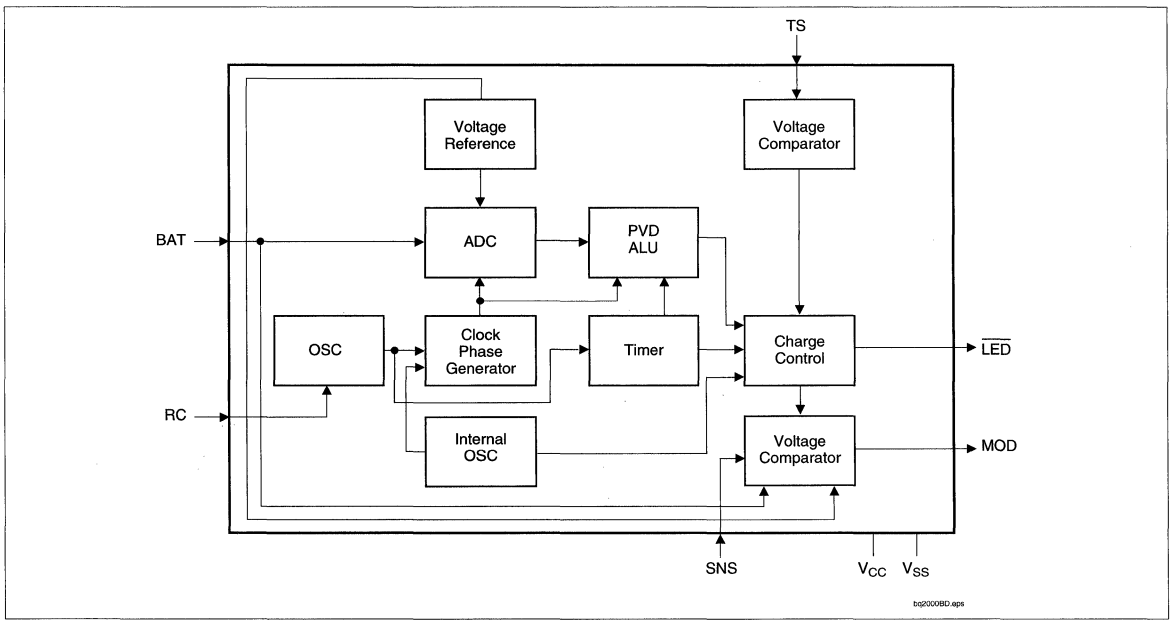


Figure 1. Functional Block Diagram

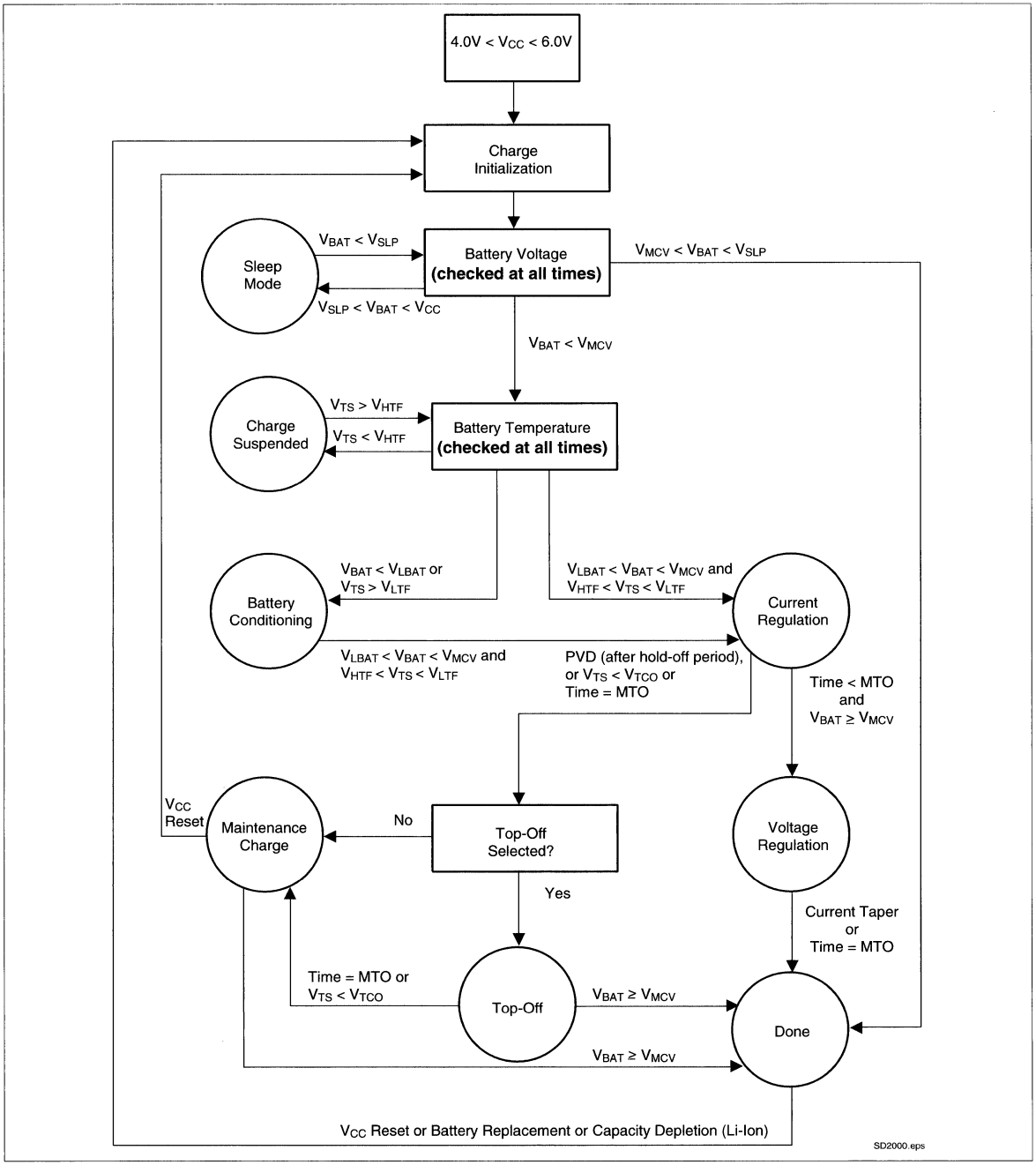


Figure 2. State Diagram

Initiation and Charge Qualification

The bq2000 initiates a charge cycle when it detects

- Application of power to V_{CC}
- Battery replacement
- Exit from sleep mode
- Capacity depletion (Li-Ion only)

Immediately following initiation, the IC enters a charge-qualification mode. The bq2000 charge qualification is based on battery voltage and temperature. If voltage on pin BAT is less than the internal threshold, V_{LBAT}, the bq2000 enters the charge-pending state. This condition indicates the possiblility of a defective or shorted battery pack. In an attempt to revive a fully depleted pack, the bq2000 enables the MOD pin to trickle-charge at a rate of once every 1.0s. As explained in the section "Top-Off and Pulse-Trickle Charge," the trickle pulse-width is user-selectable and is set by the value of the resistance connected to pin RC.

During this period, the $\overline{LED}$ pin blinks at a 1Hz rate, indicating the pending status of the charger.

Similarly, the bq2000 suspends fast charge if the battery temperature is outside the V_{LTF} to V_{HTF} range. (See Table 4.) For safety reasons, however, it disables the pulse trickle, in the case of a battery over-temperature condition (i.e., $V_{TS} < V_{HTF}$). Fast charge begins when the battery temperature and voltage are valid.

Battery Chemistry

The bq2000 detects the battery chemistry by monitoring the battery-voltage profile during the initial stage of the fast charge. If the voltage on BAT input rises to the internal V_{MCV} reference, the IC assumes a Li-Ion battery. Otherwise the bq2000 assumes NiCd/NiMH chemistry.

As shown in Figure 6, a resistor voltage-divider between the battery pack's positive terminal and V_{SS} scales the battery voltage measured at pin BAT. In a mixed-chemistry design, a common voltage-divider is used as long as the maximum charge voltage of the nickel-based pack is below that of the Li-Ion pack. Otherwise, different scaling is required.

Once the chemistry is determined, the bq2000 completes the fast charge with the appropriate charge algorithm (Table 1). The user can customize the algorithm by programming the device using an external resistor and a capacitor connected to the RC pin, as discussed in later sections.

NiCd and NiMH Batteries

Following qualification, the bq2000 fast-charges NiCd or NiMH batteries using a current-limited algorithm. During the fast-charge period, it monitors charge time, temperature, and voltage for adherence to the termination criteria. This monitoring is further explained in later sections. Following fast charge, the battery is topped off, if top-off is selected. The charging cycle ends with a trickle maintenance-charge that continues as long as the voltage on pin BAT remains below V_{MCV}.

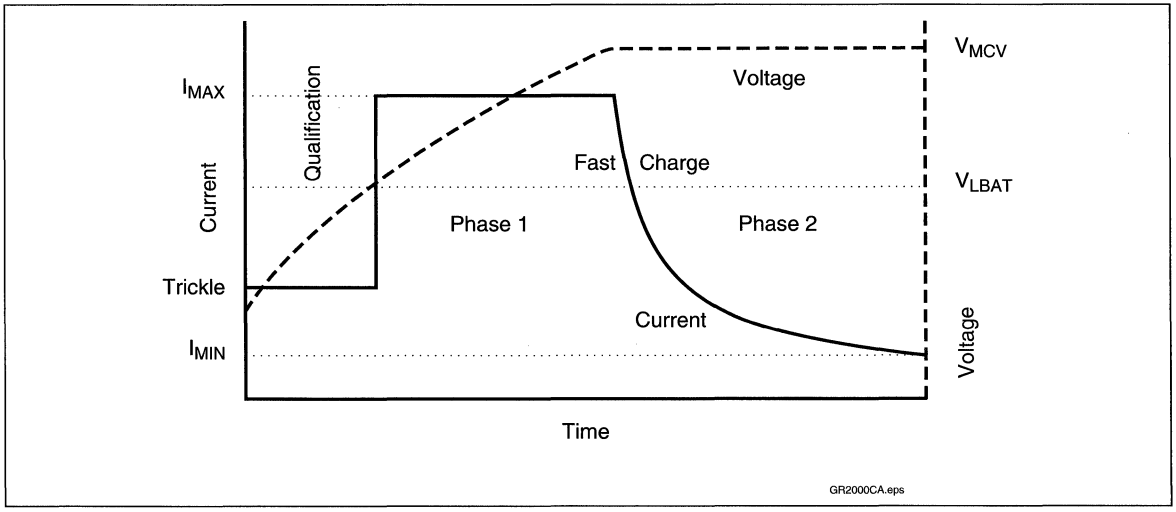


Figure 3. Lithium-Ion Charge Algorithm

Table 1. Charge Algorithm

Battery Chemistry	Charge Algorithm
NiCd or NiMH	1. Charge qualification 2. Trickle charge, if required 3. Fast charge (constant current) 4. Charge termination (peak voltage, maximum charge time) 5. Top-off (optional) 6. Trickle charge
Li-Ion	1. Charge qualification 2. Trickle charge, if required 3. Two-step fast charge (constant current followed by constant voltage) 4. Charge termination (minimum current, maximum charge time)

Lithium-Ion Batteries

The bq2000 uses a two-phase fast-charge algorithm for Li-Ion batteries (Figure 3). In phase one, the bq2000 regulates constant current until V_{BAT} rises to V_{MCV}. The bq2000 then moves to phase two, regulates the battery with constant voltage of V_{MCV}, and terminates when the charging current falls below the I_{MIN} threshold. A new charge cycle is started if the cell voltage falls below the V_{RCH} threshold.

During the current-regulation phase, the bq2000 monitors charge time, battery temperature, and battery voltage for adherence to the termination criteria. During the final constant-voltage stage, in addition to the charge time and temperature, it monitors the charge current as a termination criterion. There is no post-charge maintenance mode for Li-Ion batteries.

Charge Termination

Maximum Charge Time (NiCD, NiMH, and Li-Ion)

The bq2000 sets the maximum charge-time through pin RC. With the proper selection of external resistor and capacitor, various time-out values may be achieved. Figure 4 shows a typical connection.

The following equation shows the relationship between the R_{MTO} and C_{MTO} values and the maximum charge time (MTO) for the bq2000:

$$MTO = R_{MTO} * C_{MTO} * 35{,}988$$

MTO is measured in minutes, R_{MTO} in ohms, and C_{MTO} in farads. (**Note:** R_{MTO} and C_{MTO} values also determine other features of the device. See Tables 2 and 3 for details.)

For Li-Ion cells, the bq2000 resets the MTO when the battery reaches the constant-voltage phase of the charge. This feature provides the additional charge time required for Li-Ion cells.

Maximum Temperature (NiCd, NiMH, Li-Ion)

A negative-coefficient thermistor, referenced to V_{SS} and placed in thermal contact with the battery, may be used as a temperature-sensing device. Figure 5 shows a typical temperature-sensing circuit.

During fast charge, the bq2000 compares the battery temperature to an internal high-temperature cutoff threshold, V_{TCO}. As shown in Table 4, high-temperature termination occurs when voltage at pin TS is less than this threshold.

Peak Voltage (NiCd, NiMH)

The bq2000 uses a peak-voltage detection (PVD) scheme to terminate fast charge for NiCd and NiMH batteries. The bq2000 continuously samples the voltage on the BAT pin, representing the battery voltage, and triggers the peak detection feature if this value falls below the maximum sampled value by as much as 3.8mV (PVD). As shown in Figure 6, a resistor voltage-divider between the battery pack's positive terminal and V_{SS} scales the battery voltage measured at pin BAT.

For Li-Ion battery packs, the resistor values R_{B1} and R_{B2} are calculated by the following equation:

$$\frac{R_{B1}}{R_{B2}} = \left(N * \frac{V_{CELL}}{V_{MCV}}\right) - 1$$

where N is the number of cells in series and V_{CELL} is the manufacturer-specified charging voltage. The end-to-end input impedance of this resistive divider network should be at least 200kΩ and no more than 1MΩ.

A NiCd or NiMH battery pack consisting of N series-cells may benefit by the selection of the R_{B1} value to be N-1 times larger than the R_{B2} value.

In a mixed-chemistry design, a common voltage-divider is used as long as the maximum charge voltage of the

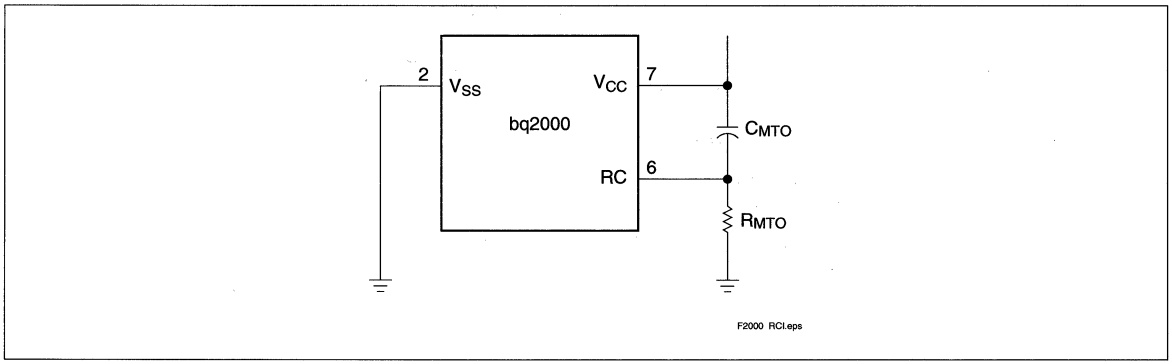


Figure 4. Typical Connection for the RC Input

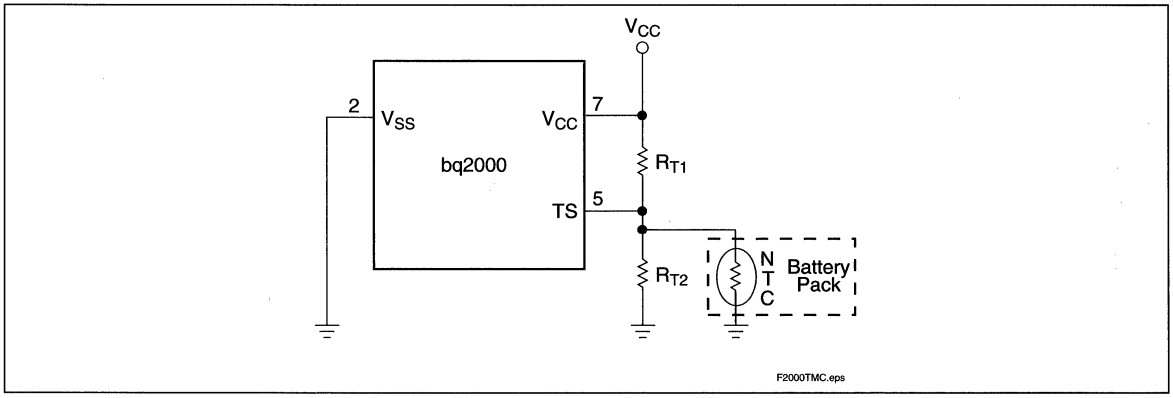


Figure 5. Temperature Monitoring Configuration

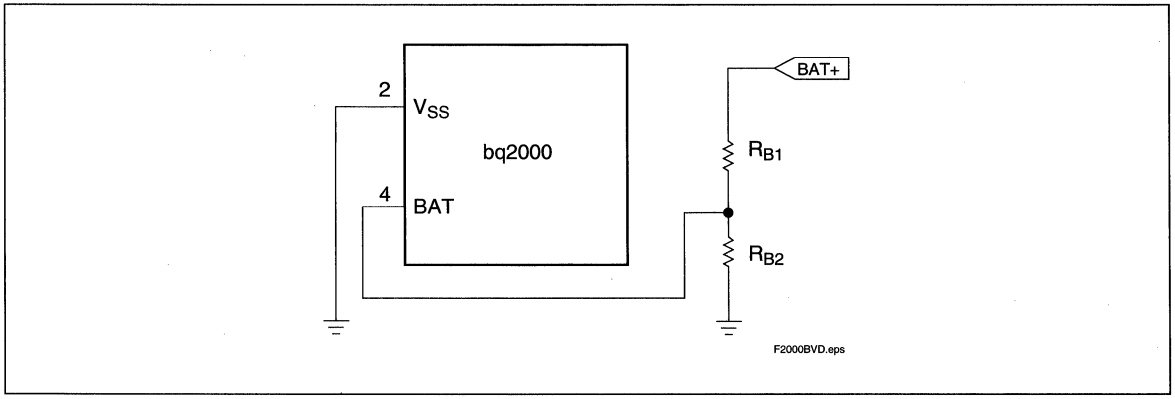


Figure 6. Battery Voltage Divider

6/13

nickel-based pack is below that of the Li-Ion pack. Otherwise, different scaling is required.

Minimum Current (Li-Ion Only)

The bq2000 monitors the charging current during the voltage-regulation phase of Li-Ion batteries. Fast charge is terminated when the current is tapered off to 14% of the maximum charging current.

Initial Hold-Off Period

The values of the external resistor and capacitor connected to pin RC set the initial hold-off period. During this period, the bq2000 avoids early termination due to an initial rise in the battery voltage by disabling the peak voltage-detection feature. This period is fixed at the programmed value of the maximum charge time divided by 32.

$$\text{hold-off period} = \frac{\text{maximum time - out}}{32}$$

Top-Off and Pulse-Trickle Charge

An optional top-off charge is available for NiCd or NiMH batteries. Top-off may be desirable on batteries that have a tendency to terminate charge before reaching full capacity. To enable this option, the capacitance value of C_{MTO} connected to pin RC (Figure 4) should be greater than 0.13µF, and the value of the resistor connected to this pin should be less than 15kΩ. To disable top-off, the capacitance value should be less than 0.07µF. The tolerance of the capacitor needs to be taken into account in component selection.

Once enabled, the top-off is performed over a period equal to the maximum charge time at a rate of $\frac{1}{16}$ that of fast charge.

Following top-off, the bq2000 trickle-charges the battery by enabling the MOD to charge at a rate of once every 1.0 second. The trickle pulse-width is user-selectable and is set by the value of the resistor R_{MTO}, connected to pin RC. Figure 7 shows the relationship between the trickle pulse-width and the value of R_{MTO}. The typical tolerance of the pulsewidth below 150kΩ is ±10%.

During top-off and trickle-charge, the bq2000 monitors battery voltage and temperature. These charging functions are suspended if the battery voltage rises above the maximum cell voltage (V_{MCV}) or if the temperature exceeds the high-temperature fault threshold (V_{HTF}).

Charge Current Control

The bq2000 controls the charge current through the MOD output pin. The current-control circuit supports a switching-current regulator with frequencies up to 500kHz. The bq2000 monitors charge current at the SNS input by the voltage drop across a sense-resistor, R_{SNS}, in series with the battery pack. See Figure 9 for a typical current-sensing circuit. R_{SNS} is sized to provide the desired fast-charge current (I_{MAX}):

$$I_{MAX} = \frac{0.05}{R_{SNS}}$$

If the voltage at the SNS pin is greater than V_{SNSLO} or less than V_{SNSHI}, the bq2000 switches the MOD output high to pass charge current to the battery. When the

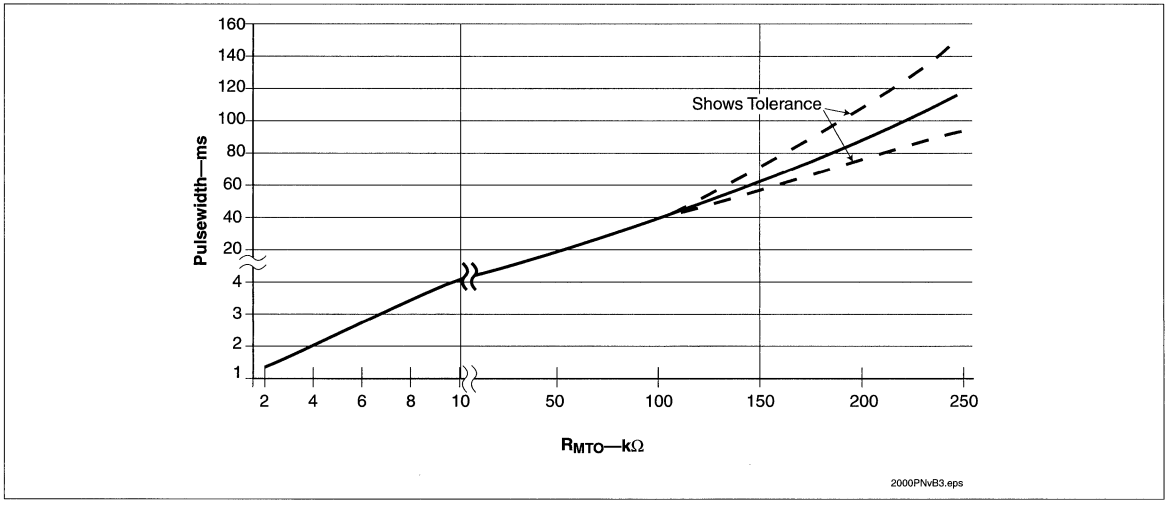
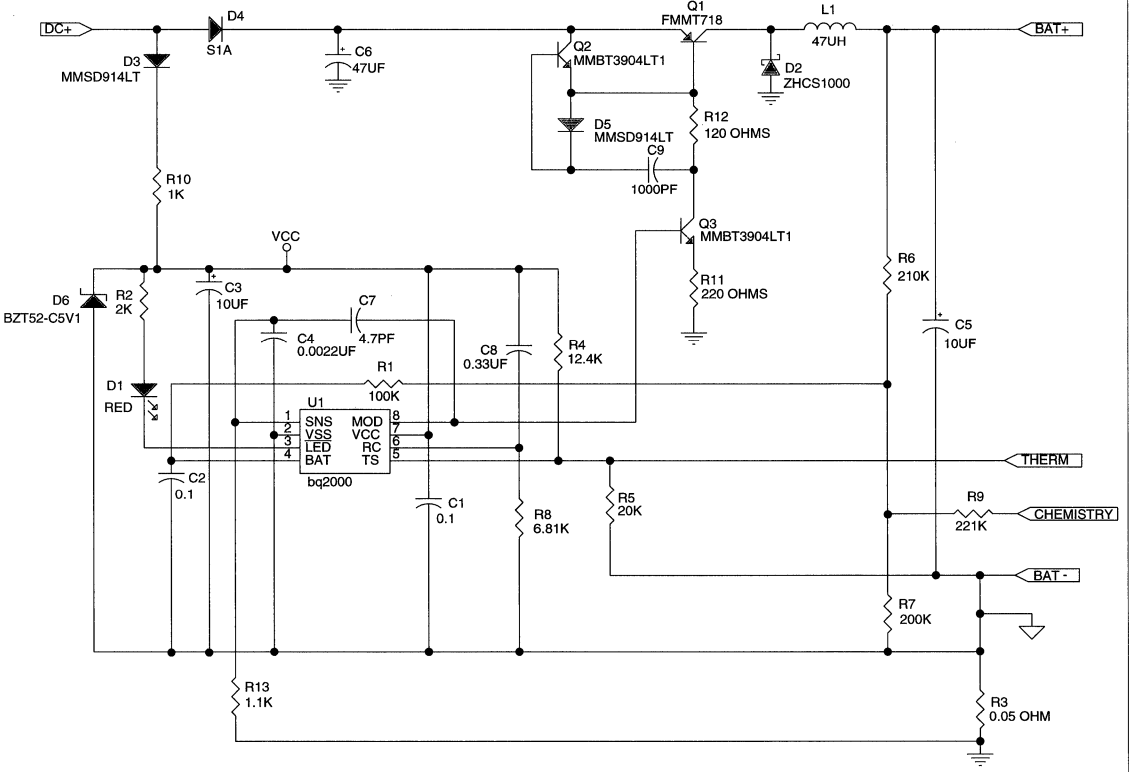


Figure 7. Relationship Between Trickle Pulse-Width and Value of R_{MTO}



NOTES: 1. For Li-Ion, the CHEMISTRY is left floating.
For NiCd/NiMH, the CHEMISTRY is tied to BAT-

2. DC input voltage: 9–16V

3. Charge current: 1A

4. L1: 3L Global P/N PKSMD-1005-470K-1A

Figure 8. Single-Cell Li-Ion, Three-Cell NiCd/NiMH 1A Charger

Table 2. Summary of NiCd or NiMH Charging Characteristics

Parameter	Value*
Maximum cell voltage (V_{MCV})	2V
Minimum pre-charge qualification voltage (V_{LBAT})	950mV
High-temperature cutoff voltage (V_{TCO})	0.225 * V_{CC}
High-temperature fault voltage (V_{HTF})	0.25 * V_{CC}
Low-temperature fault voltage (V_{LTF})	0.5 * V_{CC}
bq2000 fast-charge maximum time out (MTO)	R_{MTO} * C_{MTO} * 35,988
Fast-charge charging current (I_{MAX})	0.05/R_{SNS}
Hold-off period	MTO/32
Top-off charging current (optional)	I_{MAX}/16
Top-off period (optional)	MTO
Trickle-charge frequency	1Hz
Trickle-charge pulse-width	See Figure 7

*Please refer to DC Thresholds Specification for details.

SNS voltage is less than V_{SNSLO} or greater than V_{SNSHI}, the bq2000 switches the MOD output low to shut off charging current to the battery. Figure 8 shows a typical multi-chemistry charge circuit.

Temperature Monitoring

The bq2000 measures the temperature by the voltage at the TS pin. This voltage is typically generated by a negative-temperature-coefficient thermistor. The bq2000 compares this voltage against its internal threshold voltages to determine if charging is safe. These thresholds are the following:

- High-temperature cutoff voltage: V_{TCO} = 0.225 * V_{CC} This voltage corresponds to the maximum temperature (TCO) at which fast charging is allowed. The bq2000 terminates fast charge if the voltage on pin TS falls below V_{TCO}.

Table 3. Summary of Li-Ion Charging Characteristics

Parameter	Value*
Maximum cell voltage (V_{MCV})	2V
Minimum pre-charge qualification voltage (V_{LBAT})	950mV
High-temperature cutoff voltage (V_{TCO})	0.225 * V_{CC}
High-temperature fault voltage (V_{HTF})	0.25 * V_{CC}
Low-temperature fault voltage (V_{LTF})	0.5 * V_{CC}
bq2000 fast-charge maximum time-out (MTO)	2 * R_{MTO} * C_{MTO} * 35,988
Fast-charge charging current (I_{MAX})	0.05/R_{SNS}
Hold-off period	MTO/32
Minimum current (for fast-charge termination)	I_{MAX}/7
Trickle-charge frequency (before fast charge only)	1Hz
Trickle-charge pulse-width (before fast charge only)	See Figure 7

*Please refer to DC Thresholds Specification for details.

Table 4. Temperature-Monitoring Conditions

Temperature	Condition	Action
$V_{TS} > V_{LTF}$	Cold battery—checked at all times	Suspends fast charge or top-off and timer Allows trickle charge—LED flashes at 1Hz rate during pre-charge qualification and fast charge
$V_{HTF} < V_{TS} < V_{LTF}$	Optimal operating range	Allows charging
$V_{TS} < V_{HTF}$	Hot battery—checked during charge qualification and top-off and trickle-charge	Suspends fast-charge initiation, does not allow trickle charge—LED flashes at 1Hz rate during pre-charge qualification and fast charge
$V_{TS} < V_{TCO}$	Battery exceeding maximum allowable temperature—checked at all times	Terminates fast charge or top-off

- High-temperature fault voltage: $V_{HTF} = 0.25 * V_{CC}$ This voltage corresponds to the temperature (HTF) at which fast charging is allowed to begin.
- Low-temperature fault voltage: $V_{LTF} = 0.5 * V_{CC}$ This voltage corresponds to the minimum temperature (LTF) at which fast charging or top-off is allowed. If the voltage on pin TS rises above V_{LTF}, the bq2000 suspends fast charge or top-off but does not terminate charge. When the voltage falls back below V_{LTF}, fast charge or top-off resumes from the point where suspended. Trickle-charge is allowed during this condition.

Table 4 summarizes these various conditions.

Charge Status Display

The charge status is indicated by open-drain output LED. Table 5 summarizes the display output of the bq2000.

Table 5. Charge Status Display

Charge Action State	$\overline{\text{LED}}$ Status
Battery absent	High impedance
Pre-charge qualification	1Hz flash
Trickle charge (before fast charge)	1Hz flash
Fast charging	Low
Top-off or trickle (after fast charge, NiCd, NiMH only)	High impedance
Charge complete	High impedance
Sleep mode	High impedance
Charge suspended ($V_{TS} > V_{LTF}$)	1Hz flash

Sleep Mode

The bq2000 features a sleep mode for low power consumption. This mode is enabled when the voltage at pin BAT is above the low-power-mode threshold, V_{SLP}. During sleep mode, the bq2000 shuts down all internal circuits, drives the LED output to high-impedance state, and drives pin MOD to low. Restoring BAT below the V_{MCV} threshold initiates the IC and starts a fast-charge cycle.

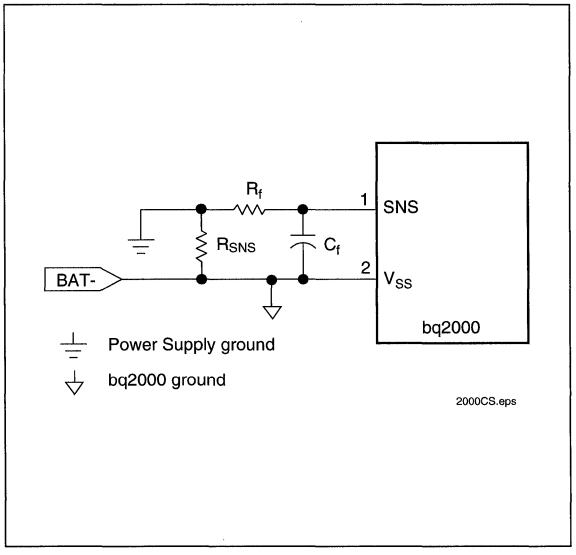


Figure 9. Current-Sensing Circuit

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin, excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	-20	+70	°C	
T_{STG}	Storage temperature	-40	+125	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10s max.

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds ($T_A = T_{OPR}$; V_{CC} = 5V ±20% unless otherwise specified)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{TCO}	Temperature cutoff	0.225 * V_{CC}	±5%	V	Voltage at pin TS
V_{HTF}	High-temperature fault	0.25 * V_{CC}	±5%	V	Voltage at pin TS
V_{LTF}	Low-temperature fault	0.5 * V_{CC}	±5%	V	Voltage at pin TS
V_{MCV}	Maximum cell voltage	2.00	±0.75%	V	$V_{BAT} > V_{MCV}$ inhibits fast charge
V_{LBAT}	Minimum cell voltage	950	±5%	mV	Voltage at pin BAT
PVD	BAT input change for PVD detection	3.8	±20%	mV	
V_{SNSHI}	High threshold at SNS, resulting in MOD-low	50	±10	mV	Voltage at pin SNS
V_{SNSLO}	Low threshold at SNS, resulting in MOD-high	-50	±10	mV	Voltage at pin SNS
V_{SLP}	Sleep-mode input threshold	V_{CC} - 1	±0.5	V	Applied to pin BAT
V_{RCH}	Recharge threshold	V_{MCV} - 0.1	±0.02	V	At pin BAT

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.0	5.0	6.0	V	
I_{CC}	Supply current	-	0.5	1	mA	Exclusive of external loads
I_{CCS}	Sleep current	-	-	5	µA	$V_{BAT} = V_{SLP}$
V_{TS}	Thermistor input	0.5	-	V_{CC}	V	$V_{TS} < 0.5V$ prohibited
V_{OH}	Output high	V_{CC} - 0.2	-	-	V	MOD, I_{OH} = 20mA
V_{OL}	Output low	-	-	0.2	V	MOD, LED, I_{OL} = 20mA
I_{OZ}	High-impedance leakage current	-	-	5	µA	LED
I_{snk}	Sink current	-	-	20	mA	MOD, LED
R_{MTO}	Charge timer resistor	2	-	250	kΩ	
C_{MTO}	Charge timer capacitor	0.001	-	1.0	µF	

Note: All voltages relative to V_{SS} except as noted.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
R_{BAT}	Battery input impedance	10	-	-	MΩ
R_{TS}	TS input impedance	10	-	-	MΩ
R_{SNS}	SNS input impedance	10	-	-	MΩ

Timing ($T_A = T_{OPR}$; V_{CC} = 5V ±20% unless otherwise specified)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
d_{MTO}	MTO time-base variation	-5	-	+5	%
f_{TRKL}	Pulse-trickle frequency	0.9	1.0	1.1	Hz

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	4	MTO equation	Was: MTO = R * C * 71,976 Is: MTO = R_{MTO} * C_{MTO} * 35,988
1	6	Trickle-pulse width equation	Replaced equation with Figure 6
1	7	Figure 7	Schematic updated
1	10	V_{TCO}, V_{HTF}, V_{LTF}	Tolerance updated
1	11	R_{MTO}, C_{MTO}	Values updated
2	8	V_{LBAT}	Corrected values in Tables 2 and 3
3	1, 13	Package option	Added TSSOP
3	3	State diagram	Added
3	8	Schematic updated	
3	11	V_{TSO}, V_{HTF},V_{LTF}	Tolerance updated
3	7	Top-off charge	Updated requirement for enabling top-off

Note: Change 1 = Jan. 1999 B changes to Final from Sept. 1998 Preliminary data sheet.

Change 2 = Mar. 1999 C changes from Jan. 1999 B.

Change 3 = May 1999 D changes from Mar. 1999 C.

Ordering Information

bq2000 _ _

Package Option:
PN = 8-pin narrow plastic DIP
SN = 8-pin narrow SOIC
TS = 8-pin TSSOP

Device:
bq2000 Multi-Chemistry Fast-Charge IC with Peak Voltage Detection

13/13

UNITRODE

bq2000T

Programmable Multi-Chemistry Fast-Charge Management IC

Features

- Safe management of fast charge for NiCd, NiMH, or Li-Ion battery packs
- High-frequency switching controller for efficient and simple charger design
- Pre-charge qualification for detecting shorted, damaged, or overheated cells
- Fast-charge termination by $\Delta T/\Delta t$ minimum current (Li-Ion), maximum temperature, and maximum charge time
- Selectable top-off mode for achieving maximum capacity in NiMH batteries
- Programmable trickle-charge mode for reviving deeply discharged batteries and for post-charge maintenance
- Built-in battery removal and insertion detection
- Sleep mode for low power consumption

General Description

The bq2000T is a programmable, monolithic IC for fast-charge management of nickel cadmium (NiCd), nickel metal-hydride (NiMH), or lithium-ion (Li-Ion) batteries in single- or multi-chemistry applications. The bq2000T detects the battery chemistry and proceeds with the optimal charging and termination algorithms. This process eliminates undesirable undercharged or overcharged conditions and allows accurate and safe termination of fast charge.

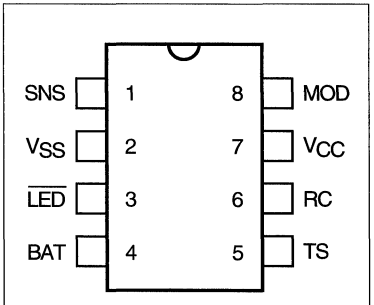
Depending on the chemistry, the bq2000T provides a number of charge termination criteria:

- Rate of temperature rise, $\Delta T/\Delta t$ (for NiCd and NiMH)
- Minimum charging current (for Li-Ion)
- Maximum temperature
- Maximum charge time

For safety, the bq2000T inhibits fast charge until the battery voltage and temperature are within user-defined limits. If the battery voltage is below the low-voltage threshold, the bq2000T uses trickle-charge to condition the battery. For NiMH batteries, the bq2000T provides an optional top-off charge to maximize the battery capacity.

The integrated high-frequency comparator allows the bq2000T to be the basis for a complete, high-efficiency power-conversion circuit for both nickel-based and lithium-based chemistries.

Pin Connections



8-Pin DIP or Narrow SOIC or TSSOP

PN-2000.eps

Pin Names

SNS	Current-sense input	TS	Temperature-sense input
V_{SS}	System ground	RC	Timer-program input
$\overline{LED}$	Charge-status output	V_{CC}	Supply-voltage input
BAT	Battery-voltage input	MOD	Modulation-control output

Pin Descriptions

SNS **Current-sense input**

Enables the bq2000T to sense the battery current via the voltage developed on this pin by an external sense-resistor connected in series with the battery pack

V_{SS} **System Ground**

$\overline{LED}$ **Charge-status output**

Open-drain output that indicates the charging status by turning on, turning off, or flashing an external LED

BAT **Battery-voltage input**

Battery-voltage sense input. A simple resistive divider, across the battery terminals, generates this input.

TS **Temperature-sense input**

Input for an external battery-temperature monitoring circuit. An external resistive divider network with a negative temperature-coefficient thermistor sets the lower and upper temperature thresholds.

RC **Timer-program input**

RC input used to program the maximum charge-time, hold-off period, and trickle rate during the charge cycle, and to disable or enable top-off charge

V_{CC} **Supply-voltage input**

MOD **Modulation-control output**

Push-pull output that controls the charging current to the battery. MOD switches high to enable charging current to flow and low to inhibit charging- current flow.

Functional Description

The bq2000T is a versatile, multi-chemistry battery-charge control device. See Figure 1 for a functional block diagram and Figure 2 for the state diagram.

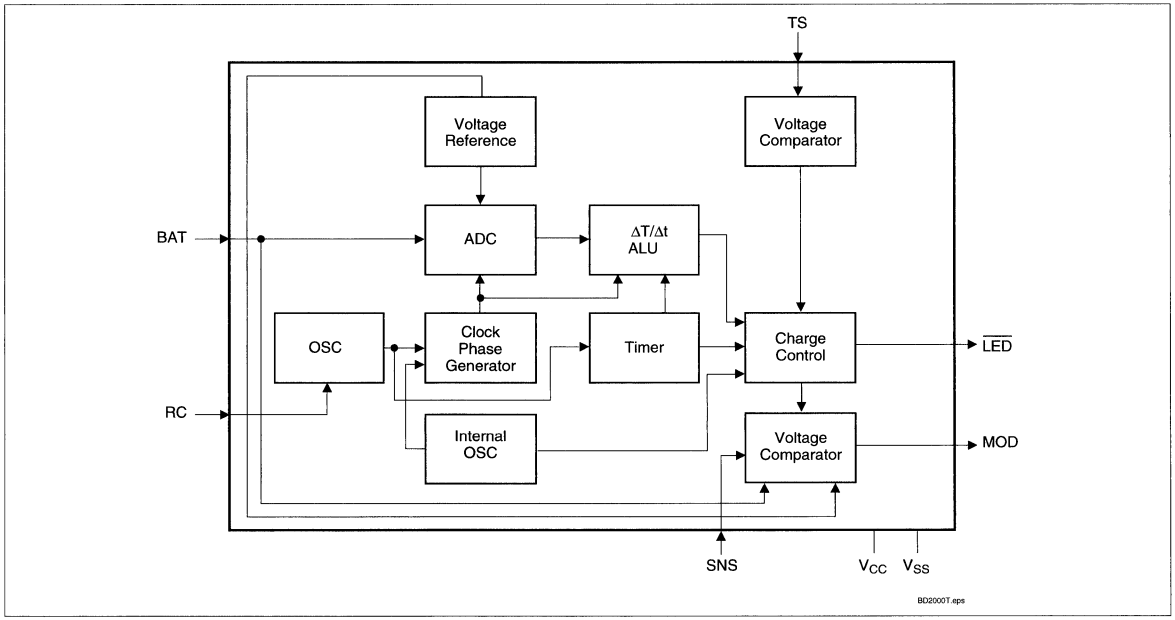


Figure 1. Functional Block Diagram

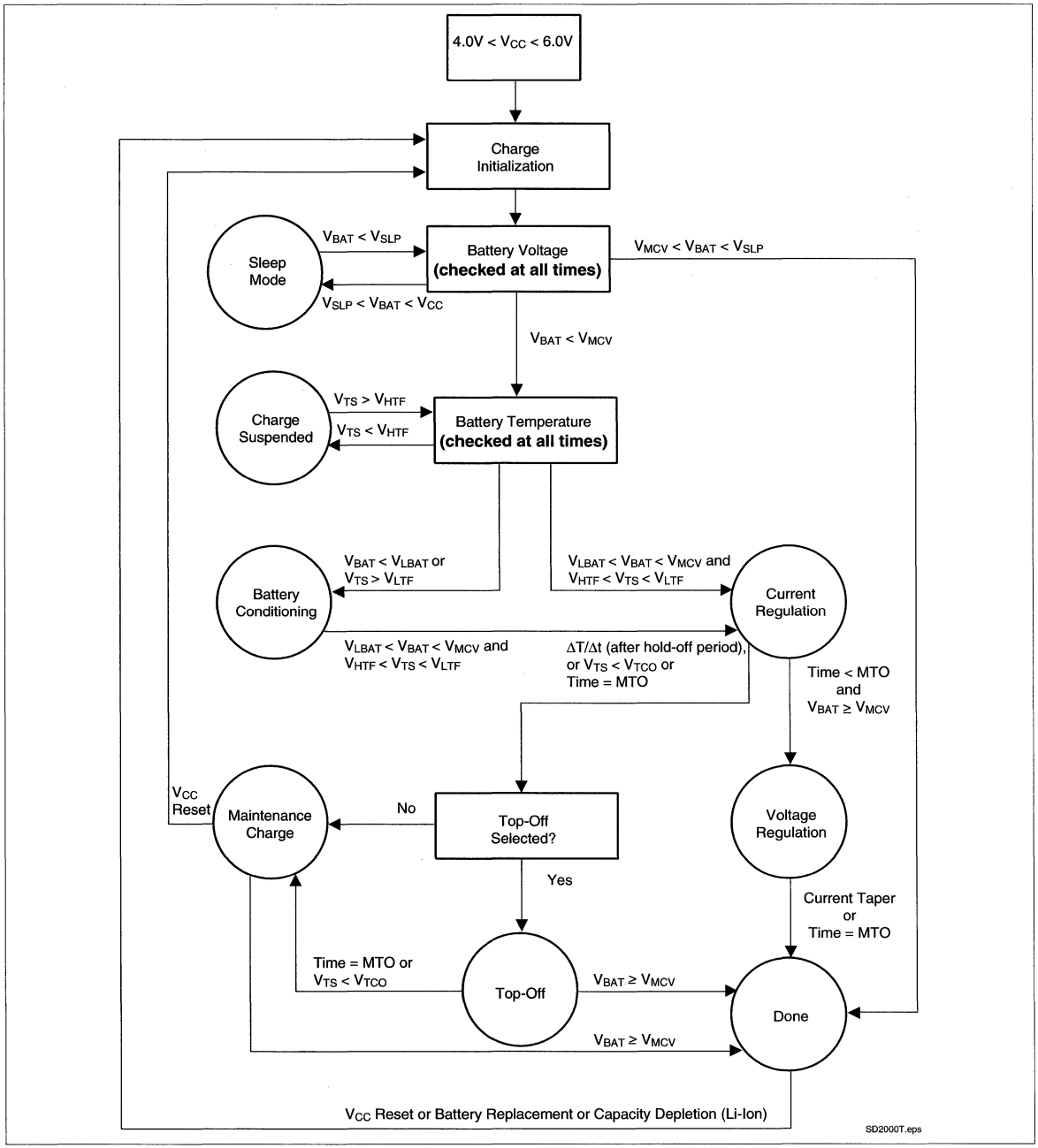


Figure 2. State Diagram

Initiation and Charge Qualification

The bq2000T initiates a charge cycle when it detects

- Application of power to V_{CC}
- Battery replacement
- Exit from sleep mode
- Capacity depletion (Li-Ion only)

Immediately following initiation, the IC enters a charge-qualification mode. The bq2000T charge qualification is based on battery voltage and temperature. If voltage on pin BAT is less than the internal threshold, V_{LBAT}, the bq2000T enters the charge-pending state. This condition indicates the possiblility of a defective or shorted battery pack. In an attempt to revive a fully depleted pack, the bq2000T enables the MOD pin to trickle-charge at a rate of once every 1.0s. As explained in the section "Top-Off and Pulse-Trickle Charge," the trickle pulse-width is user-selectable and is set by the value of the resistance connected to pin RC.

During this period, the $\overline{LED}$ pin blinks at a 1Hz rate, indicating the pending status of the charger.

Similarly, the bq2000T suspends fast charge if the battery temperature is outside the V_{LTF} to V_{HTF} range. (See Table 4.) For safety reasons, however, it disables the pulse trickle, in the case of a battery over-temperature condition (i.e., $V_{TS} < V_{HTF}$). Fast charge begins when the battery temperature and voltage are valid.

Battery Chemistry

The bq2000T detects the battery chemistry by monitoring the battery-voltage profile during fast charge. If the voltage on BAT input rises to the internal V_{MCV} reference, the IC assumes a Li-Ion battery. Otherwise the bq2000T assumes NiCd/NiMH chemistry.

As shown in Figure 6, a resistor voltage-divider between the battery pack's positive terminal and V_{SS} scales the battery voltage measured at pin BAT. In a mixed-chemistry design, a common voltage-divider is used as long as the maximum charge voltage of the nickel-based pack is below that of the Li-Ion pack. Otherwise, different scaling is required.

Once the chemistry is determined, the bq2000T completes the fast charge with the appropriate charge algorithm (Table 1). The user can customize the algorithm by programming the device using an external resistor and a capacitor connected to the RC pin, as discussed in later sections.

NiCd and NiMH Batteries

Following qualification, the bq2000T fast-charges NiCd or NiMH batteries using a current-limited algorithm. During the fast-charge period, it monitors charge time, temperature, and voltage for adherence to the termination criteria. This monitoring is further explained in later sections. Following fast charge, the battery is topped off, if top-off is selected. The charging cycle ends

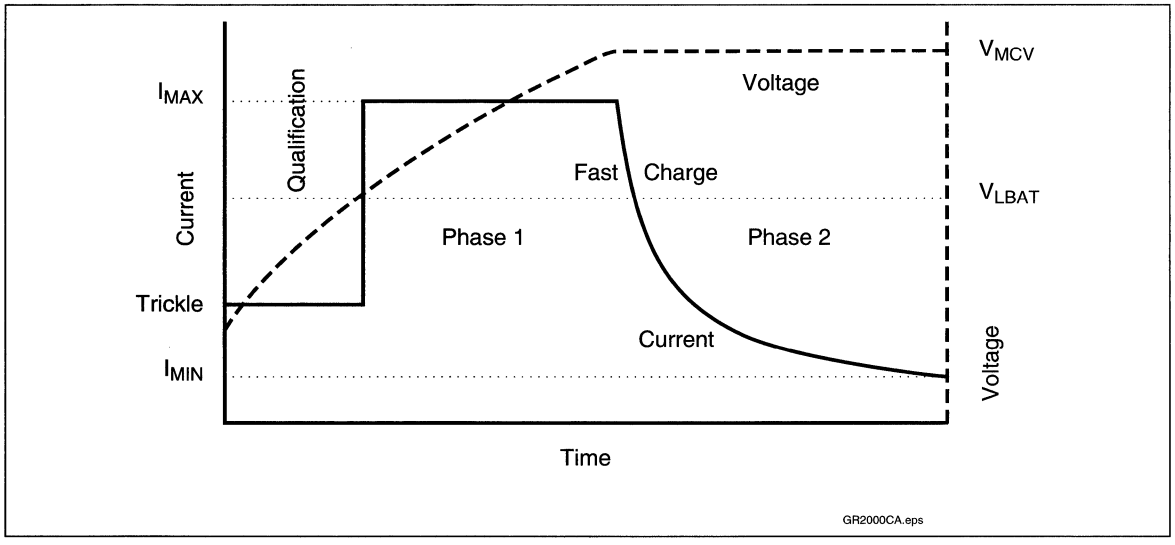


Figure 3. Lithium-Ion Charge Algorithm

4/13

Table 1. Charge Algorithm

Battery Chemistry	Charge Algorithm
NiCd or NiMH	1. Charge qualification 2. Trickle charge, if required 3. Fast charge (constant current) 4. Charge termination (ΔT/Δt, time) 5. Top-off (optional) 6. Trickle charge
Li-Ion	1. Charge qualification 2. Trickle charge, if required 3. Two-step fast charge (constant current followed by constant voltage) 4. Charge termination (minimum current, time)

with a trickle maintenance-charge that continues as long as the voltage on pin BAT remains below V_{MCV}.

Lithium-Ion Batteries

The bq2000T uses a two-phase fast-charge algorithm for Li-Ion batteries (Figure 3). In phase one, the bq2000T regulates constant current until V_{BAT} rises to V_{MCV}. The bq2000T then moves to phase two, regulates the battery with constant voltage of V_{MCV}, and terminates when the charging current falls below the I_{MIN} threshold. A new charge cycle is started if the cell voltage falls below the V_{RCH} threshold.

During the current-regulation phase, the bq2000T monitors charge time, battery temperature, and battery voltage for adherence to the termination criteria. During the final constant-voltage stage, in addition to the charge time and temperature, it monitors the charge current as a termination criterion. There is no post-charge maintenance mode for Li-Ion batteries.

Charge Termination

Maximum Charge Time (NiCD, NiMH, and Li-Ion)

The bq2000T sets the maximum charge-time through pin RC. With the proper selection of external resistor and capacitor, various time-out values may be achieved. Figure 4 shows a typical connection.

The following equation shows the relationship between the R_{MTO} and C_{MTO} values and the maximum charge time (MTO) for the bq2000T:

$$MTO = R_{MTO} * C_{MTO} * 35{,}988$$

MTO is measured in minutes, R_{MTO} in ohms, and C_{MTO} in farads. (**Note:** R_{MTO} and C_{MTO} values also determine other features of the device. See Tables 2 and 3 for details.)

For Li-Ion cells, the bq2000T resets the MTO when the battery reaches the constant-voltage phase of the charge. This feature provides the additional charge time required for Li-Ion cells.

Maximum Temperature (NiCd, NiMH, Li-Ion)

A negative-coefficient thermistor, referenced to V_{SS} and placed in thermal contact with the battery, may be used as a temperature-sensing device. Figure 5 shows a typical temperature-sensing circuit.

During fast charge, the bq2000T compares the battery temperature to an internal high-temperature cutoff threshold, V_{TCO}. As shown in Table 4, high-temperature termination occurs when voltage at pin TS is less than this threshold.

ΔT/Δt (NiCd, NiMH)

When fast charging, the bq2000T monitors the voltage at pin TS for rate of temperature change detection, ΔT/Δt. The bq2000T samples the voltage at the TS pin every 16s and compares it to the value measured 2 samples earlier. This feature terminates fast charge if this voltage declines at a rate of

$$\frac{V_{CC}}{161}\left(\frac{V}{Min}\right)$$

Figure 5 shows a typical connection diagram.

Minimum Current (Li-Ion Only)

The bq2000T monitors the charging current during the voltage-regulation phase of Li-Ion batteries. Fast charge is terminated when the current is tapered off to 7% of the maximum charging current. **Please note that this threshold is different for the bq2000.**

Initial Hold-Off Period

The values of the external resistor and capacitor connected to pin RC set the initial hold-off period. During this period, the bq2000T avoids early termination by disabling the ΔT/Δt feature. This period is fixed at the

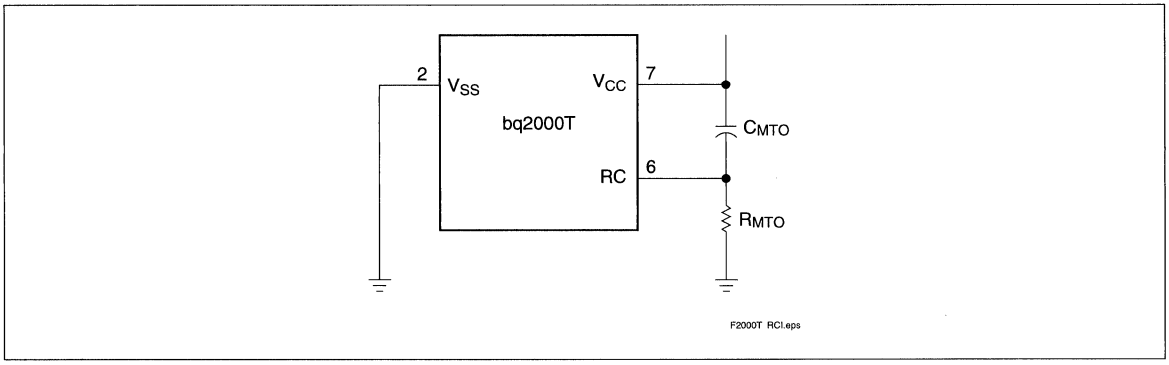


Figure 4. Typical Connection for the RC Input

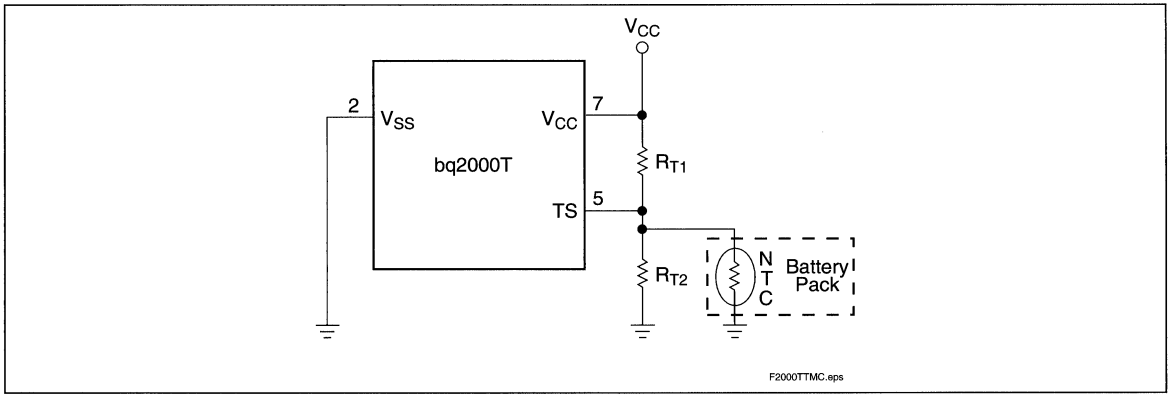


Figure 5. Temperature Monitoring Configuration

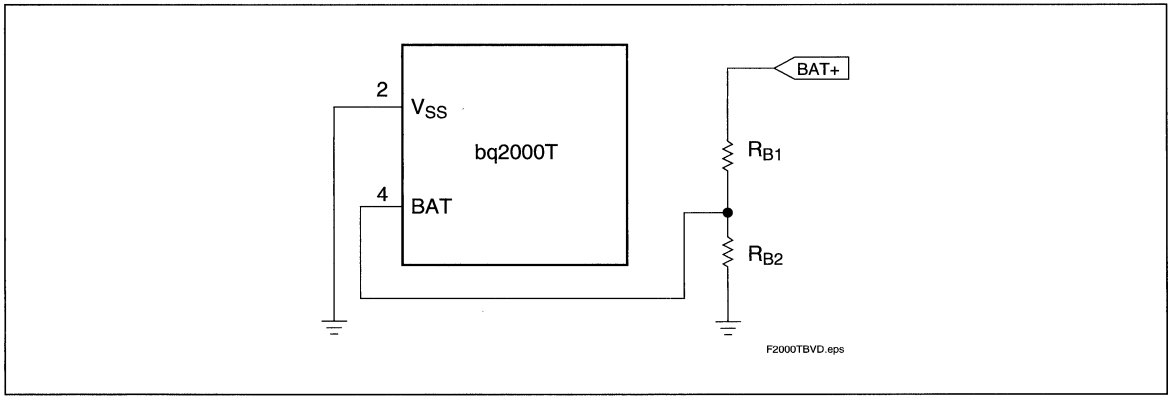


Figure 6. Battery Voltage Divider

6/13

programmed value of the maximum charge time divided by 32.

$$\text{hold-off period} = \frac{\text{maximum time - out}}{32}$$

Top-Off and Pulse-Trickle Charge

An optional top-off charge is available for NiCd or NiMH batteries. Top-off may be desirable on batteries that have a tendency to terminate charge before reaching full capacity. To enable this option, the capacitance value of C_{MTO} connected to pin RC (Figure 4) should be greater than 0.13µF, and the value of the resistor connected to this pin should be less than 15kΩ. To disable top-off, the capacitance value should be less than 0.07µF. The tolerance of the capacitor needs to be taken into account in component selection.

Once enabled, the top-off is performed over a period equal to the maximum charge time at a rate of $\frac{1}{16}$ that of fast charge.

Following top-off, the bq2000T trickle-charges the battery by enabling the MOD to charge at a rate of once every 1.0 second. The trickle pulse-width is user-selectable and is set by the value of the resistor R_{MTO}, which is on pin RC. Figure 7 shows the relationship between the trickle pulse-width and the value of R_{MTO}. The typical tolerance of the pulsewidth below 150kΩ is ±10%.

During top-off and trickle-charge, the bq2000T monitors battery voltage and temperature. These functions are suspended if the battery voltage rises above the maximum cell voltage (V_{MCV}) or if the temperature exceeds the high-temperature fault threshold (V_{HTF}).

Charge Current Control

The bq2000T controls the charge current through the MOD output pin. The current-control circuit supports a switching-current regulator with frequencies up to 500kHz. The bq2000T monitors charge current at the SNS input by the voltage drop across a sense-resistor, R_{SNS}, in series with the battery pack. See Figure 9 for a typical current-sensing circuit. R_{SNS} is sized to provide the desired fast-charge current (I_{MAX}):

$$I_{MAX} = \frac{0.05}{R_{SNS}}$$

If the voltage at the SNS pin is greater than V_{SNSLO} or less than V_{SNSHI}, the bq2000T switches the MOD output high to pass charge current to the battery. When the SNS voltage is less than V_{SNSLO} or greater than V_{SNSHI}, the bq2000T switches the MOD output low to shut off charging current to the battery. Figure 8 shows a typical multi-chemistry charge circuit.

Voltage Input

As shown in Figure 6, a resistor voltage-divider between the battery pack's positive terminal and V_{SS} scales the battery voltage measured at pin BAT.

For Li-Ion battery packs, the resistor values R_{B1} and R_{B2} are calculated by the following equation:

$$\frac{R_{B1}}{R_{B2}} = \left(N * \frac{V_{CELL}}{V_{MCV}}\right) - 1$$

where N is the number of cells in series and V_{CELL} is the manufacturer-specified charging voltage. The end-to-end input impedance of this resistive divider network should be at least 200kΩ and no more than 1MΩ.

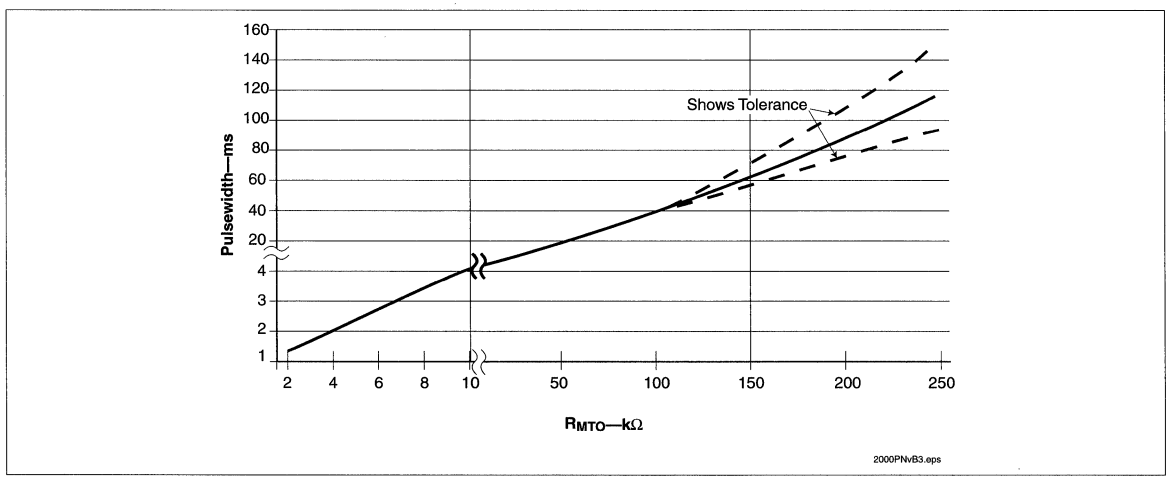
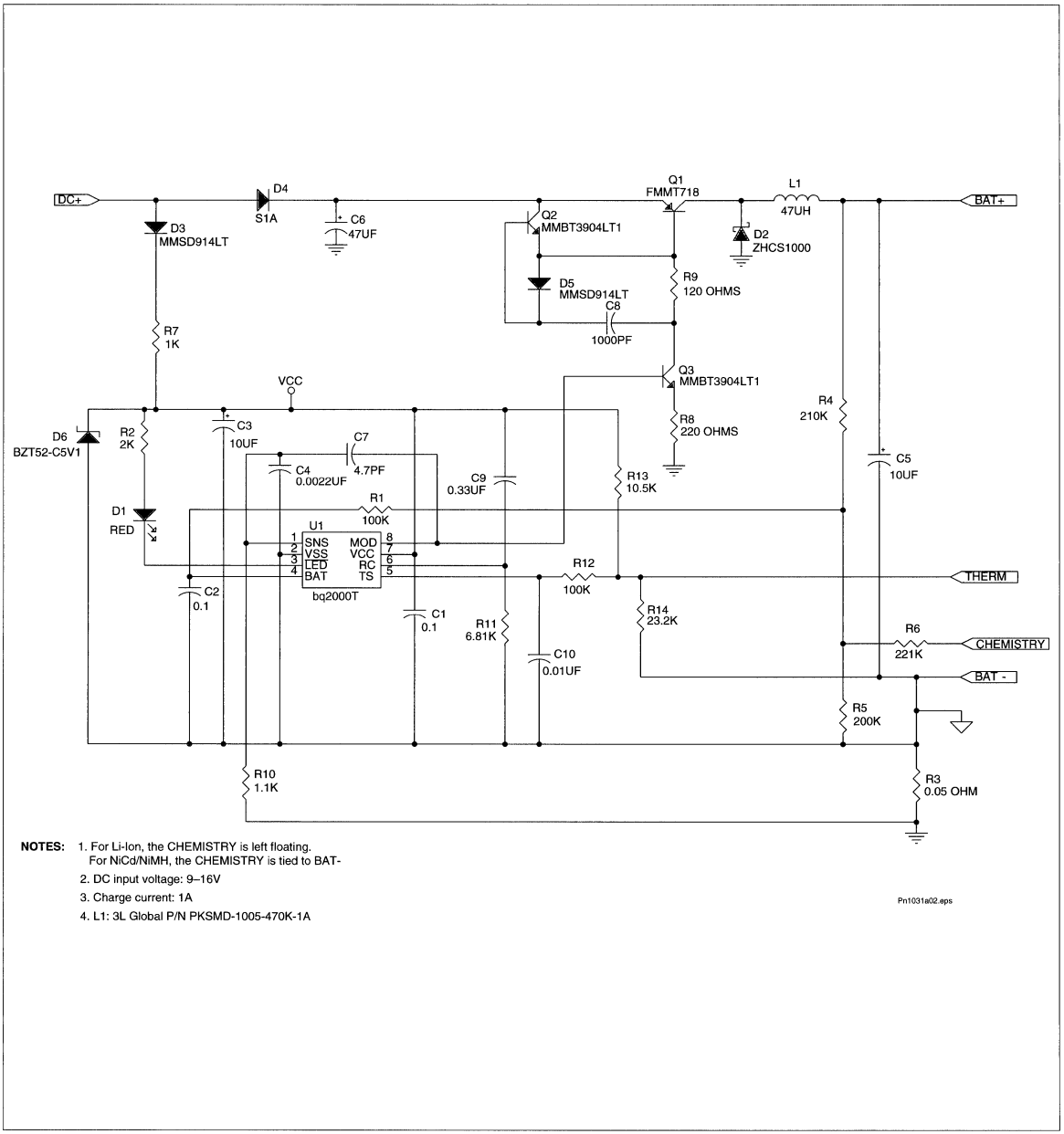


Figure 7. Relationship Between Trickle Pulse-Width and Value of R_{MTO}



NOTES: 1. For Li-Ion, the CHEMISTRY is left floating.
For NiCd/NiMH, the CHEMISTRY is tied to BAT-
2. DC input voltage: 9–16V
3. Charge current: 1A
4. L1: 3L Global P/N PKSMD-1005-470K-1A

Figure 8. Single-Cell Li-Ion, Three-Cell NiCd/NiMH 1A Charger

8/13

Table 2. Summary of NiCd or NiMH Charging Characteristics

Parameter	Value
Maximum cell voltage (V_{MCV})	2V
Minimum pre-charge qualification voltage (V_{LBAT})	950mV
High-temperature cutoff voltage (V_{TCO})	0.225 * V_{CC}
High-temperature fault voltage (V_{HTF})	0.25 * V_{CC}
Low-temperature fault voltage (V_{LTF})	0.5 * V_{CC}
bq2000T fast-charge maximum time out (MTO)	R_{MTO} * C_{MTO} * 35,988
Fast-charge charging current (I_{MAX})	0.05/R_{SNS}
Hold-off period	MTO/32
Top-off charging current (optional)	I_{MAX}/16
Top-off period (optional)	MTO
Trickle-charge frequency	1Hz
Trickle-charge pulse-width	See Figure 7

A NiCd or NiMH battery pack consisting of N series-cells may benefit by the selection of the R_{B1} value to be N-1 times larger than the R_{B2} value.

In a mixed-chemistry design, a common voltage-divider is used as long as the maximum charge voltage of the nickel-based pack is below that of the Li-Ion pack. Otherwise, different scaling is required.

Temperature Monitoring

The bq2000T measures the temperature by the voltage at the TS pin. This voltage is typically generated by a negative-temperature-coefficient thermistor. The bq2000T compares this voltage against its internal threshold voltages to determine if charging is safe. These thresholds are the following:

- High-temperature cutoff voltage: V_{TCO} = 0.225 * V_{CC} This voltage corresponds to the maximum temperature (TCO) at which fast charging is allowed. The bq2000T terminates fast charge if the voltage on pin TS falls below V_{TCO}.
- High-temperature fault voltage: V_{HTF} = 0.25 * V_{CC} This voltage corresponds to the temperature (HTF) at which fast charging is allowed to begin.
- Low-temperature fault voltage: V_{LTF} = 0.5 * V_{CC} This voltage corresponds to the minimum temperature

Table 3. Summary of Li-Ion Charging Characteristics

Parameter	Value
Maximum cell voltage (V_{MCV})	2V
Minimum pre-charge qualification voltage (V_{LBAT})	950mV
High-temperature cutoff voltage (V_{TCO})	0.225 * V_{CC}
High-temperature fault voltage (V_{HTF})	0.25 * V_{CC}
Low-temperature fault voltage (V_{LTF})	0.5 * V_{CC}
bq2000T fast-charge maximum time-out (MTO)	2 * R_{MTO} * C_{MTO} * 35,988
Fast-charge charging current (I_{MAX})	0.05/R_{SNS}
Hold-off period	MTO/32
Minimum current (for fast-charge termination)	I_{MAX}/7
Trickle-charge frequency (before fast charge only)	1Hz
Trickle-charge pulse-width (before fast charge only)	See Figure 7

Table 4. Temperature-Monitoring Conditions

Temperature	Condition	Action
$V_{TS} > V_{LTF}$	Cold battery—checked at all times	Suspends fast charge or top-off and timer Allows trickle charge—LED flashes at 1Hz rate during pre-charge qualification and fast charge
$V_{HTF} < V_{TS} < V_{LTF}$	Optimal operating range	Allows charging
$V_{TS} < V_{HTF}$	Hot battery—checked during charge qualification and top-off and trickle-charge	Suspends fast-charge initiation, does not allow trickle charge—LED flashes at 1Hz rate during pre-charge qualification
$V_{TS} < V_{TCO}$	Battery exceeding maximum allowable temperature—checked at all times	Terminates fast charge or top-off

(LTF) at which fast charging or top-off is allowed. If the voltage on pin TS rises above V_{LTF}, the bq2000T suspends fast charge or top-off but does not terminate charge. When the voltage falls back below V_{LTF}, fast charge or top-off resumes from the point where suspended. Trickle-charge is allowed during this condition.

Table 4 summarizes these various conditions.

Charge Status Display

The charge status is indicated by open-drain output LED. Table 5 summarizes the display output of the bq2000T.

Table 5. Charge Status Display

Charge Action State	$\overline{\text{LED}}$ Status
Battery absent	High impedance
Pre-charge qualification	1Hz flash
Trickle charge (before fast charge)	1Hz flash
Fast charging	Low
Top-off or trickle (after fast charge, NiCd, NiMH only)	High impedance
Charge complete	High impedance
Sleep mode	High impedance
Charge suspended ($V_{TS} > V_{LTF}$)	1Hz flash

Sleep Mode

The bq2000T features a sleep mode for low power consumption. This mode is enabled when the voltage at pin BAT is above the low-power-mode threshold, V_{SLP}. During sleep mode, the bq2000T shuts down all internal circuits, drives the LED output to high-impedance state, and drives pin MOD to low. Restoring BAT below the V_{MCV} threshold initiates the IC and starts a fast-charge cycle.

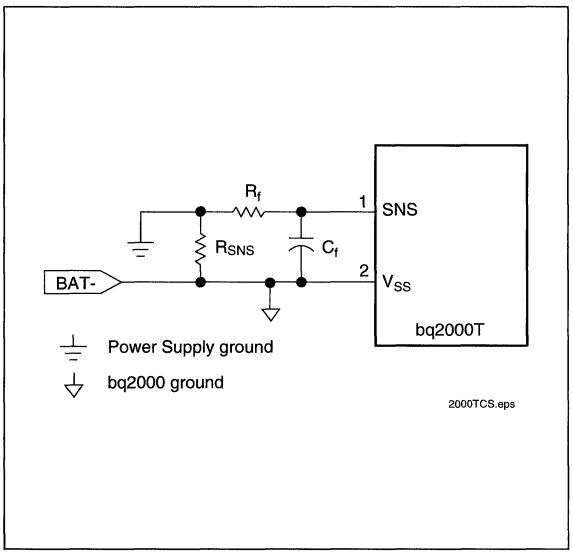


Figure 9. Current-Sensing Circuit

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin, excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	-20	+70	°C	
T_{STG}	Storage temperature	-40	+125	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10s max.

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds ($T_A = T_{OPR}$; V_{CC} = 5V ±20% unless otherwise specified)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{TCO}	Temperature cutoff	0.225 * V_{CC}	±5%	V	Voltage at pin TS
V_{HTF}	High-temperature fault	0.25 * V_{CC}	±5%	V	Voltage at pin TS
V_{LTF}	Low-temperature fault	0.5 * V_{CC}	±5%	V	Voltage at pin TS
V_{MCV}	Maximum cell voltage	2.00	±0.75%	V	$V_{BAT} > V_{MCV}$ inhibits fast charge
V_{LBAT}	Minimum cell voltage	950	±5%	mV	Voltage at pin BAT
V_{THERM}	TS input change for $\Delta T/\Delta t$ detection	$-\frac{V_{CC}}{161}$	±25%	V/Min	
V_{SNSHI}	High threshold at SNS, resulting in MOD-low	50	±10	mV	Voltage at pin SNS
V_{SNSLO}	Low threshold at SNS, resulting in MOD-high	-50	±10	mV	Voltage at pin SNS
V_{SLP}	Sleep-mode input threshold	V_{CC} - 1	±0.5	V	Applied to pin BAT
V_{RCH}	Recharge threshold	V_{MCV} - 0.1	±0.02	V	At pin BAT

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.0	5.0	6.0	V	
I_{CC}	Supply current	-	0.5	1	mA	Exclusive of external loads
I_{CCS}	Sleep current	-	-	5	µA	$V_{BAT} = V_{SLP}$
V_{TS}	Thermistor input	0.5	-	V_{CC}	V	$V_{TS} < 0.5V$ prohibited
V_{OH}	Output high	V_{CC} - 0.2	-	-	V	MOD, $I_{OH} = 20mA$
V_{OL}	Output low	-	-	0.2	V	MOD, LED, $I_{OL} = 20mA$
I_{OZ}	High-impedance leakage current	-	-	5	µA	LED
I_{snk}	Sink current	-	-	20	mA	MOD, LED
R_{MTO}	Charge timer resistor	2	-	250	kΩ	
C_{MTO}	Charge timer capacitor	0.001	-	1.0	µF	

Note: All voltages relative to V_{SS} except as noted.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
R_{BAT}	Battery input impedance	10	-	-	MΩ
R_{TS}	TS input impedance	10	-	-	MΩ
R_{SNS}	SNS input impedance	10	-	-	MΩ

Timing ($T_A = T_{OPR}$; V_{CC} = 5V ±20% unless otherwise specified)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
d_{MTO}	MTO time-base variation	-5	-	+5	%
f_{TRKL}	Pulse-trickle frequency	0.9	1.0	1.1	Hz

12/13

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	5	Minimum current termination	Was: 14% Is: 7%
1	3	Added state diagram	
1	7	Changed capacitor value for enabling top-off	Was: 0.13µF Is: 0.26µF
1	8	Figure 8	Schematic updated
1	10	V_{TCO}, V_{HTF}, V_{LTF}	Tolerance updated

Note: Change 1 = May 1999 B changes to Final from Jan. 1999 Preliminary data sheet.

Ordering Information

bq2000T _

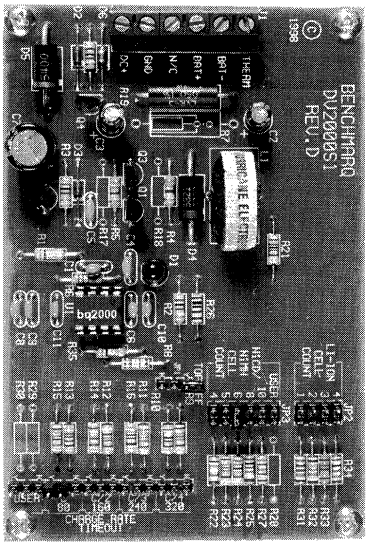
Package Option:
PN = 8-pin narrow plastic DIP
SN = 8-pin narrow SOIC
TS = 8-pin TSSOP

Device:
bq2000T Multi-Chemistry Fast-Charge IC with ΔT/Δt Detection

Multi-Chemistry Switching Charger Development System

Features

- Safe management of fast charge for NiCd, NiMH, or Li-Ion battery packs
- On-board switching regulation for up to 3A charge current (set to 1A for shipment)
- Fast-charge termination by peak voltage (bq2000), ΔT/Δt(bq2000T), minimum current (Li-Ion), maximum temperature, or maximum charge time
- Programmable charge rate and time-out
- Programmable top-off option for NiMH packs
- Trickle charge for conditioning deeply discharged batteries
- Charge-status LED
- Direct battery connection



General Description

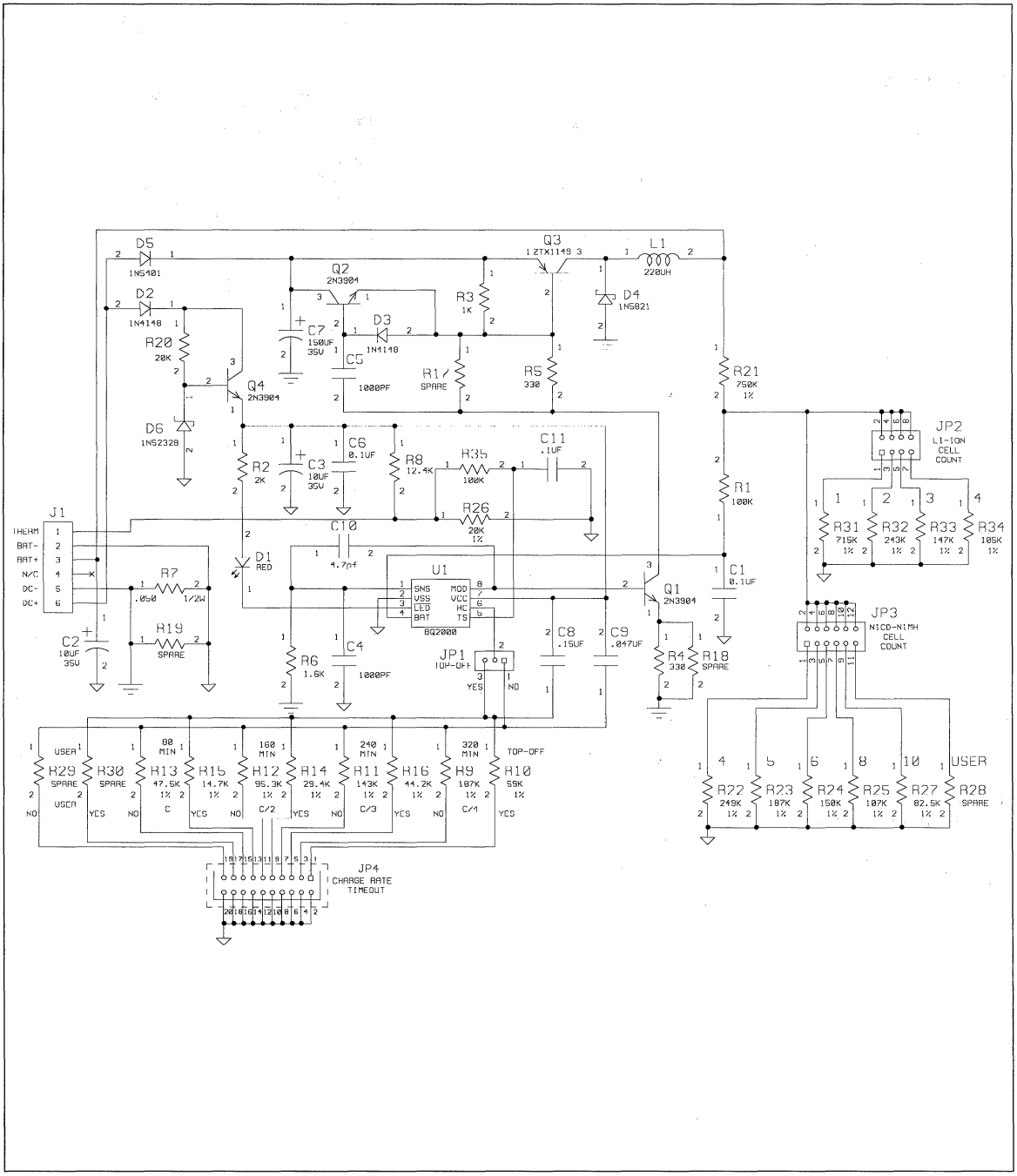
The DV2000S1 is a complete development and evaluation environment for bq2000 and bq2000T multi-chemistry charge- control ICs. The DV2000S1 supports up to 4 Li-Ion or 10 NiCd/NiMH cells and can be user-programmed for other cell counts.

Charge qualification precedes fast charge. During qualification, full-charge current is inhibited if the battery voltage or temperature is outside predetermined and user-defined thresholds, indicating a battery pack that is deeply discharged, shorted, hot, or cold. During the qualification interval, the LED flashes at a 1Hz rate. In the case of a low battery voltage, the IC applies a low-current trickle charge in an attempt to revive the battery or to close the pack protector's discharge switch. When battery voltage and temperature reach the required thresholds, full charge begins.

The bq2000/T completes the fast charge with the appropriate charge algorithm. If the voltage on BAT input rises to the internal V_{MCV} threshold, the IC assumes a Li-Ion battery. Otherwise, the bq2000 assumes NiCd/NiMH chemistry. The user can further customize the algorithm by programming the device for top-off option (NiCd/NiMH only) and time-out period.

Please review the bq2000 and bq2000T data sheets before using the DV2000S1 board.

DV2000S1 Board Schematic



Rev. D Board

UNITRODE

bq2002/F

NiCd/NiMH Fast-Charge Management ICs

Features

- Fast charge of nickel cadmium or nickel-metal hydride batteries
- Direct LED output displays charge status
- Fast-charge termination by -ΔV, maximum voltage, maximum temperature, and maximum time
- Internal band-gap voltage reference
- Optional top-off charge
- Selectable pulse trickle charge rates
- Low-power mode
- 8-pin 300-mil DIP or 150-mil SOIC

General Description

The bq2002 and bq2002/F Fast-Charge ICs are low-cost CMOS battery-charge controllers providing reliable charge termination for both NiCd and NiMH battery applications. Controlling a current-limited or constant-current supply allows the bq2002/F to be the basis for a cost-effective stand-alone or system-integrated charger. The bq2002/F integrates fast charge with optional top-off and pulsed-trickle control in a single IC for charging one or more NiCd or NiMH battery cells.

Fast charge is initiated on application of the charging supply or battery replacement. For safety, fast charge is inhibited if the battery temperature and voltage are outside configured limits.

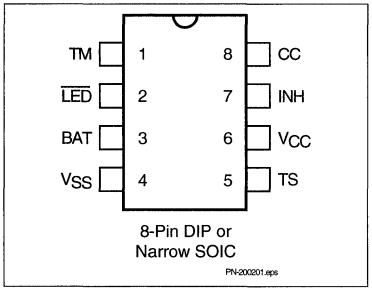
Fast charge is terminated by any of the following:

- Peak voltage detection (PVD)
- Negative delta voltage (-ΔV)
- Maximum voltage
- Maximum temperature
- Maximum time

After fast charge, the bq2002/F optionally tops-off and pulse-trickles the battery per the pre-configured limits. Fast charge may be inhibited using the INH pin. The bq2002/F may also be placed in low-standby-power mode to reduce system power consumption.

The bq2002F differs from the bq2002 only in that a slightly different set of fast-charge and top-off time limits is available. All differences between the two ICs are illustrated in Table 1.

Pin Connections



Pin Names

TM	Timer mode select input	TS	Temperature sense input
$\overline{LED}$	Charging status output	V_{CC}	Supply voltage input
BAT	Battery voltage input	INH	Charge inhibit input
V_{SS}	System ground	CC	Charge control output

bq2002/F Selection Guide

Part No.	TCO	HTF	LTF	-ΔV	PVD	Fast Charge	t_{MTO}	Top-Off	Maintenance
bq2002	0.5 * V_{CC}	None	None		✔	C/2	160	C/32	C/64
					✔	1C	80	C/16	C/64
				✔		2C	40	None	C/32
bq2002F	0.5 * V_{CC}	None	None		✔	C/2	160	C/32	C/64
					✔	1C	100	C/16	C/64
				✔		2C	55	None	C/32

Pin Descriptions

TM **Timer mode input**

A three-level input that controls the settings for the fast charge safety timer, voltage termination mode, top-off, pulse-trickle, and voltage hold-off time.

$\overline{\text{LED}}$ **Charging output status**

Open-drain output that indicates the charging status.

BAT **Battery input voltage**

The battery voltage sense input. The input to this pin is created by a high-impedance resistor divider network connected between the positive and negative terminals of the battery.

V_{SS} **System ground**

TS **Temperature sense input**

Input for an external battery temperature monitoring thermistor.

V_{CC} **Supply voltage input**

5.0V ±20% power input.

INH **Charge inhibit input**

When high, INH suspends the fast charge in progress. When returned low, the IC resumes operation at the point where initially suspended.

CC **Charge control output**

An open-drain output used to control the charging current to the battery. CC switching to high impedance (Z) enables charging current to flow, and low to inhibit charging current. CC is modulated to provide top-off, if enabled, and pulse trickle.

Functional Description

Figure 2 shows a state diagram and Figure 3 shows a block diagram of the bq2002/F.

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum allowable values. The voltage presented on the battery sense input, BAT, should represent a single-cell potential for the battery under charge. A resistor-divider ratio of

$$\frac{RB1}{RB2} = N - 1$$

is recommended to maintain the battery voltage within the valid range, where N is the number of cells, RB1 is the resistor connected to the positive battery terminal, and RB2 is the resistor connected to the negative battery terminal. See Figure 1.

Note: This resistor-divider network input impedance to end-to-end should be at least 200kΩ and less than 1 MΩ.

A ground-referenced negative temperature coefficient thermistor placed near the battery may be used as a low-cost temperature-to-voltage transducer. The temperature sense voltage input at TS is developed using a resistor-thermistor network between V_{CC} and V_{SS}. See Figure 1.

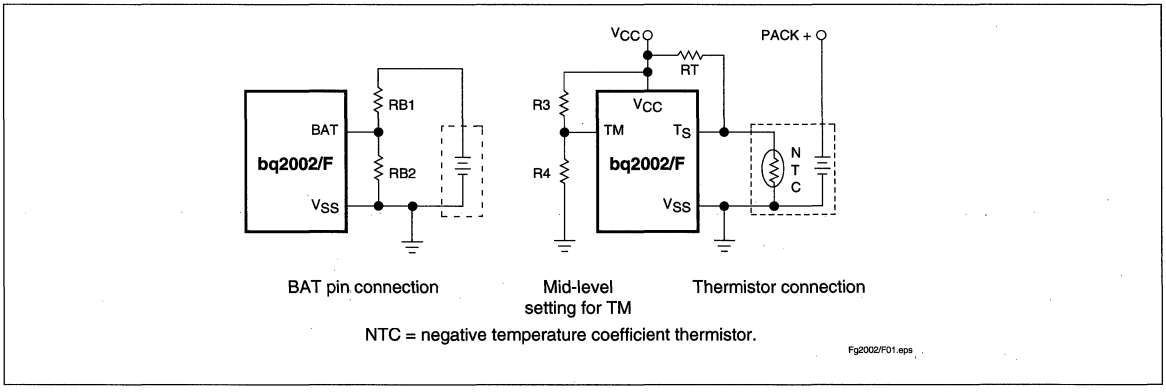


Figure 1. Voltage and Temperature Monitoring and TM Pin Configuration

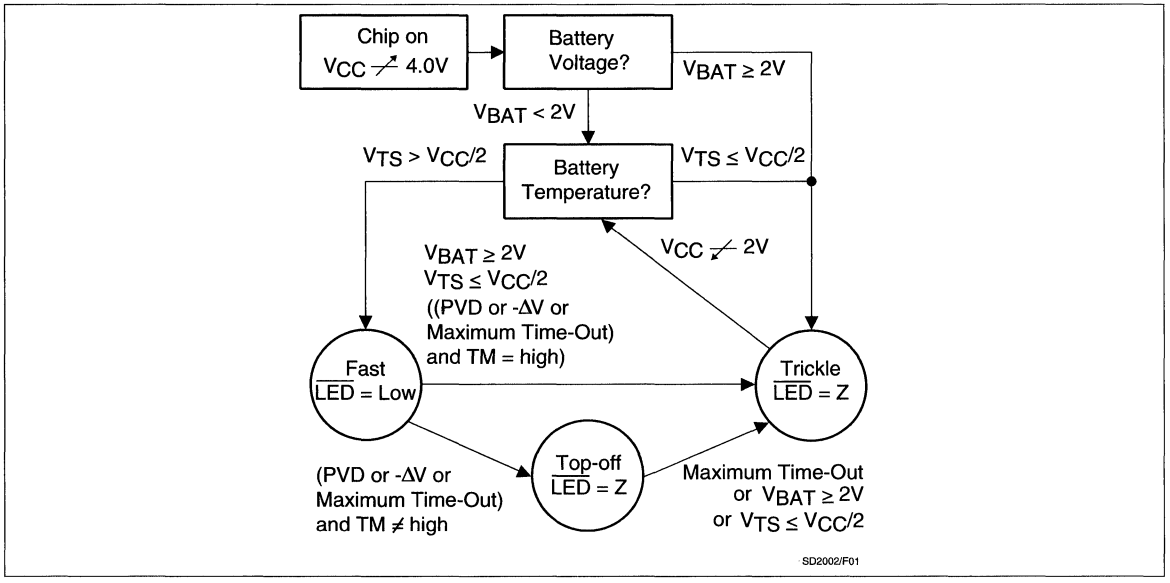


Figure 2. State Diagram

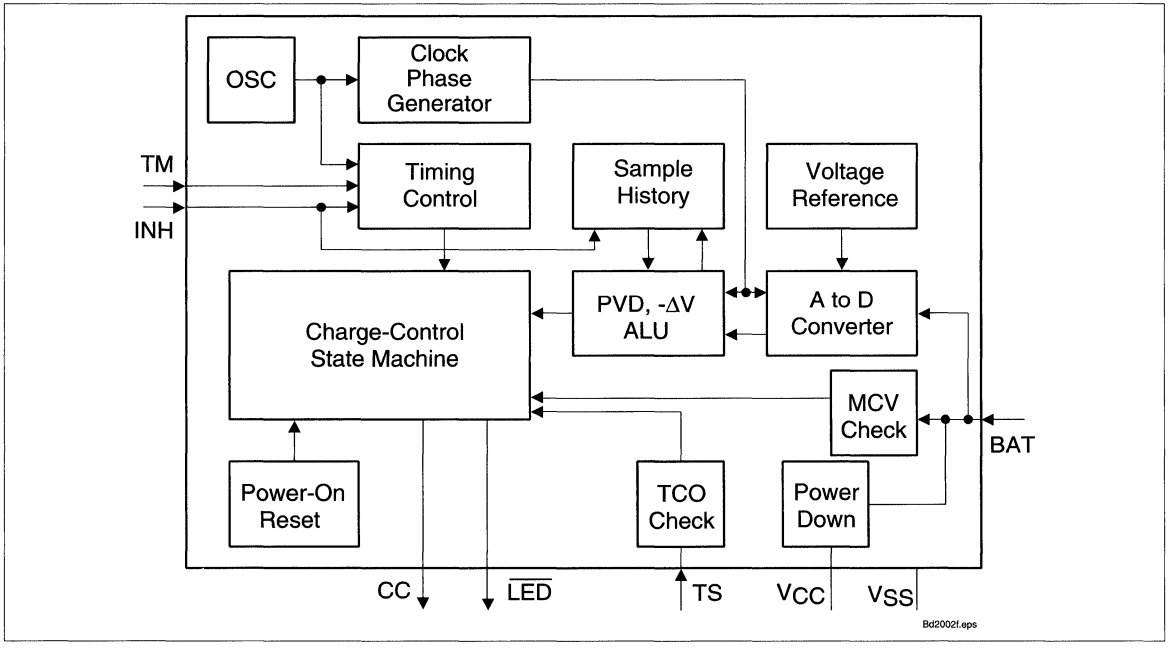


Figure 3. Block Diagram

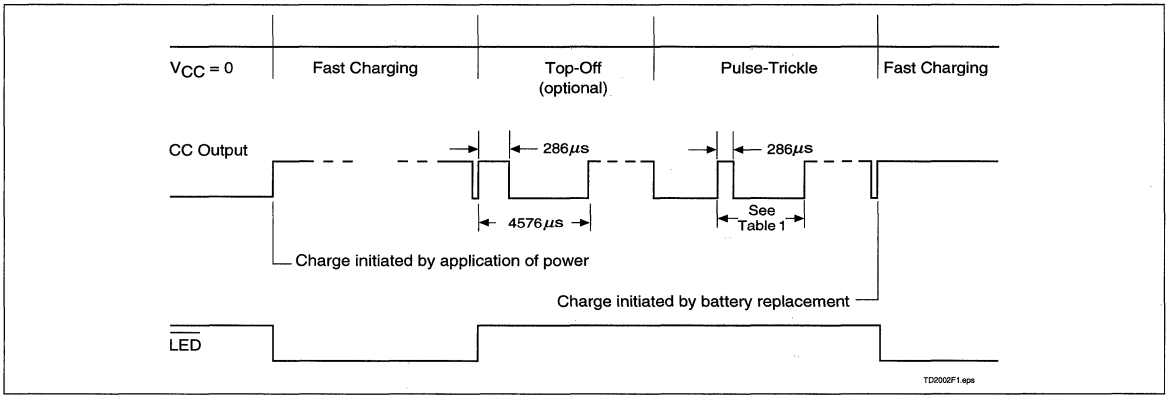


Figure 4. Charge Cycle Phases

Starting A Charge Cycle

Either of two events starts a charge cycle (see Figure 4):

1. Application of power to V_{CC} or

2. Voltage at the BAT pin falling through the maximum cell voltage V_{MCV} where

$$V_{MCV} = 2V \pm 5\%.$$

If the battery is within the configured temperature and voltage limits, the IC begins fast charge. The valid battery voltage range is $V_{BAT} < V_{MCV}$. The valid temperature range is $V_{TS} > V_{TCO}$ where

$$V_{TCO} = 0.5 * V_{CC} \pm 5\%.$$

If the battery voltage or temperature is outside of these limits, the IC pulse-trickle charges until the next new charge cycle begins.

Fast charge continues until termination by one or more of the five possible termination conditions:

- Peak voltage detection (PVD)
- Negative delta voltage (-ΔV)
- Maximum voltage
- Maximum temperature
- Maximum time

Table 1. Fast-Charge Safety Time/Hold-Off Table

Corresponding Fast-Charge Rate	TM	Termination	Typical Fast-Charge and Top-Off Time Limits (minutes)		Typical PVD and -ΔV Hold-Off Time (seconds)	Top-Off Rate	Pulse-Trickle Rate	Pulse-Trickle Period (ms)
			bq2002	bq2002F				
C/2	Mid	PVD	160	160	600	C/32	C/64	9.15
1C	Low	PVD	80	100	300	C/16	C/64	18.3
2C	High	-ΔV	40	40	150	Disabled	C/32	18.3

Notes: Typical conditions = 25°C, V_{CC} = 5.0V.
Mid = $0.5 * V_{CC} \pm 5V$
Tolerance on all timing is ±20%.

PVD and -ΔV Termination

There are two modes for voltage termination depending on the state of TM. For -ΔV (TM = high), if V_{BAT} is lower than any previously measured value by 12mV ±3mV, fast charge is terminated. For PVD (TM = low or mid), a decrease of 2.5mV ±2.5mV terminates fast charge. The PVD and -ΔV tests are valid in the range $1V < V_{BAT} < 2V$.

Voltage Sampling

Voltage is sampled at the BAT pin for PVD and -ΔV termination once every 17s. The sample is an average of voltage measurements taken 57µs apart. The IC takes 32 measurements in PVD mode and 16 measurements in -ΔV mode. The resulting sample periods (9.17 and 18.18ms, respectively) filter out harmonics centered around 55 and 109Hz. This technique minimizes the effect of any AC line ripple that may feed through the power supply from either 50 or 60Hz AC sources. Tolerance on all timing is ±20%.

Voltage Termination Hold-off

A hold-off period occurs at the start of fast charging. During the hold-off time, the PVD and -ΔV terminations are disabled. This avoids premature termination on the voltage spikes sometimes produced by older batteries when fast-charge current is first applied. Maximum voltage and temperature terminations are not affected by the hold-off period.

Maximum Voltage, Temperature, and Time

Any time the voltage on the BAT pin exceeds the maximum cell voltage,V_{MCV}, fast charge or optional top-off charge is terminated.

Maximum temperature termination occurs anytime the voltage on the TS pin falls below the temperature cut-off threshold V_{TCO}.

Maximum charge time is configured using the TM pin. Time settings are available for corresponding charge rates of C/2, 1C, and 2C. Maximum time-out termination is enforced on the fast-charge phase, then reset, and enforced again on the top-off phase, if selected. There is no time limit on the trickle-charge phase.

Top-off Charge

An optional top-off charge phase may be selected to follow fast charge termination for 1C and C/2 rates. This phase may be necessary on NiMH or other battery chemistries that have a tendency to terminate charge prior to reaching full capacity. With top-off enabled, charging continues at a reduced rate after fast-charge termination for a period of time selected by the TM pin. (See Table 1.) During top-off, the CC pin is modulated at a duty cycle of 286µs active for every 4290µs inactive. This modulation results in an average rate 1/16th that of the fast charge rate. Maximum voltage, time, and temperature are the only termination methods enabled during top-off.

Pulse-Trickle Charge

Pulse-trickle is used to compensate for self-discharge while the battery is idle in the charger. The battery is pulse-trickle charged by driving the CC pin active for a period of 286µs for every 18.0ms of inactivity for 1C and 2C selections, and 286µs for every 8.86ms of inactivity for C/2 selection. This results in a trickle rate of C/64 for the top-off enabled mode and C/32 otherwise.

TM Pin

The TM pin is a three-level pin used to select the charge timer, top-off, voltage termination mode, trickle rate, and voltage hold-off period options. Table 1 describes the states selected by the TM pin. The mid-level selection input is developed by a resistor divider between V_{CC} and ground that fixes the voltage on TM at $V_{CC}/2 \pm 0.5V$. See Figure 4.

Charge Status Indication

A fast charge in progress is uniquely indicated when the $\overline{LED}$ pin goes low. The $\overline{LED}$ pin is driven to the high-Z state for all conditions other than fast charge. Figure 2 outlines the state of the $\overline{LED}$ pin during charge.

Charge Inhibit

Fast charge and top-off may be inhibited by using the INH pin. When high, INH suspends all fast charge and top-off activity and the internal charge timer. INH freezes the current state of $\overline{LED}$ until inhibit is removed. Temperature monitoring is not affected by the INH pin. During charge inhibit, the bq2002/F continues to pulse-trickle charge the battery per the TM selection. When INH returns low, charge control and the charge timer resume from the point where INH became active.

Low-Power Mode

The IC enters a low-power state when V_{BAT} is driven above the power-down threshold (V_{PD}) where

$$V_{PD} = V_{CC} - (1V \pm 0.5V)$$

Both the CC pin and the $\overline{LED}$ pin are driven to the high-Z state. The operating current is reduced to less than 1µA in this mode. When V_{BAT} returns to a value below V_{PD}, the IC pulse-trickle charges until the next new charge cycle begins.

5/8

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	0	+70	°C	Commercial
T_{STG}	Storage temperature	-40	+85	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10 sec max.
T_{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds (T_A = 0 to 70°C; V_{CC} ±20%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{TCO}	Temperature cutoff	0.5 * V_{CC}	±5%	V	$V_{TS} \le V_{TCO}$ inhibits/terminates fast charge and top-off
V_{MCV}	Maximum cell voltage	2	±5%	V	$V_{BAT} \ge V_{MCV}$ inhibits/terminates fast charge and top-off
-ΔV	BAT input change for -ΔV detection	-12	±3	mV	
PVD	BAT input change for PVD detection	-2.5	±2.5	mV	

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.0	5.0	6.0	V	
V_{DET}	-ΔV, PVD detect voltage	1	-	2	V	
V_{BAT}	Battery input	0	-	V_{CC}	V	
V_{TS}	Thermistor input	0.5	-	V_{CC}	V	V_{TS} < 0.5V prohibited
V_{IH}	Logic input high	0.5	-	-	V	INH
	Logic input high	V_{CC} - 0.5	-	-	V	TM
V_{IM}	Logic input mid	$\frac{V_{CC}}{2}$ - 0.5	-	$\frac{V_{CC}}{2}$ + 0.5	V	TM
V_{IL}	Logic input low	-	-	0.1	V	INH
	Logic input low	-	-	0.5	V	TM
V_{OL}	Logic output low	-	-	0.8	V	$\overline{LED}$, CC, I_{OL} = 10mA
V_{PD}	Power down	V_{CC} - 1.5	-	V_{CC} - 0.5	V	$V_{BAT} \geq V_{PD}$ max. powers down bq2002/F; $V_{BAT} < V_{PD}$ min. = normal operation.
I_{CC}	Supply current	-	-	250	µA	Outputs unloaded, V_{CC} = 5.1V
I_{SB}	Standby current	-	-	1	µA	V_{CC} = 5.1V, V_{BAT} = V_{PD}
I_{OL}	$\overline{LED}$, CC sink	10	-	-	mA	@V_{OL} = V_{SS} + 0.8V
I_L	Input leakage	-	-	±1	µA	INH, CC, V = V_{SS} to V_{CC}
I_{OZ}	Output leakage in high-Z state	-5	-	-	µA	$\overline{LED}$, CC

Note: All voltages relative to V_{SS}.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
R_{BAT}	Battery input impedance	50	-	-	MΩ
R_{TS}	TS input impedance	50	-	-	MΩ

Timing (T_A = 0 to +70°C; V_{CC} ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
d_{FCV}	Time-base variation	-20	-	20	%	

Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	3	Was: Table 1 gave the bq2002/F Operational Summary. Is: Figure 2 gives the bq2002/F Operational Summary.	Changed table to figure.
1	5	Added Termination column to table and Top-off values.	Added column and values.
2	All	Revised and expanded this data sheet to include bq2002F	
3	1	Addition of selection guide	

Notes: Change 1 = Sept. 1996 B changes from July 1994.
Change 2 = Aug. 1997 C changes from Sept. 1996 B.
Change 3 = Jan. 1999 D changes from Aug. 1997 C.

Ordering Information

bq2002/F _

Package Option:
PN = 8-pin plastic DIP
SN = 8-pin narrow SOIC

Device:
bq2002 Fast-Charge IC
bq2002F Fast-Charge IC

8/8

UNITRODE

bq2002C

NiCd/NiMH Fast-Charge Management IC

Features

- Fast charge of nickel cadmium or nickel-metal hydride batteries
- Direct LED output displays charge status
- Fast-charge termination by -ΔV, maximum voltage, maximum temperature, and maximum time
- Internal band-gap voltage reference
- Selectable pulse-trickle charge rates
- Low-power mode
- 8-pin 300-mil DIP or 150-mil SOIC

General Description

The bq2002C Fast-Charge IC is a low-cost CMOS battery-charge controller providing reliable charge termination for both NiCd and NiMH battery applications. Controlling a current-limited or constant-current supply allows the bq2002C to be the basis for a cost-effective stand-alone or system-integrated charger. The bq2002C integrates fast charge with pulsed-trickle control in a single IC for charging one or more NiCd or NiMH battery cells.

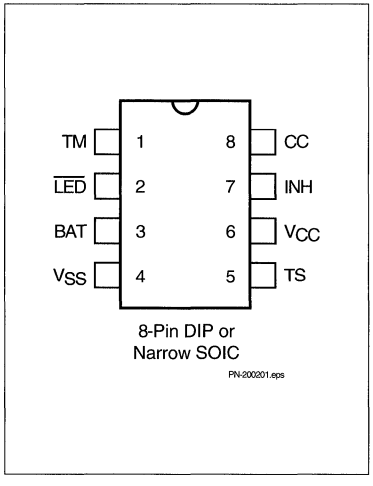
Fast charge is initiated on application of the charging supply or battery replacement. For safety, fast charge is inhibited if the battery temperature and voltage are outside configured limits.

Fast charge is terminated by any of the following:

- Peak voltage detection (PVD)
- Negative delta voltage (-ΔV)
- Maximum voltage
- Maximum temperature
- Maximum time

After fast charge, the bq2002C pulse-trickles the battery per the pre-configured limits. Fast charge may be inhibited using the INH pin. The bq2002C may also be placed in low-standby-power mode to reduce system power consumption.

Pin Connections



Pin Names

TM	Timer mode select input	TS	Temperature sense input
$\overline{LED}$	Charging status output	V_{CC}	Supply voltage input
BAT	Battery voltage input	INH	Charge inhibit input
V_{SS}	System ground	CC	Charge control output

Pin Descriptions

TM **Timer mode input**

A three-level input that controls the settings for the fast charge safety timer, voltage termination mode, pulse-trickle, and voltage hold-off time.

$\overline{LED}$ **Charging output status**

Open-drain output that indicates the charging status.

BAT **Battery input voltage**

The battery voltage sense input. The input to this pin is created by a high-impedance resistor divider network connected between the positive and negative terminals of the battery.

V_{SS} **System ground**

TS **Temperature sense input**

Input for an external battery temperature monitoring thermistor.

V_{CC} **Supply voltage input**

5.0V ±20% power input.

INH **Charge inhibit input**

When high, INH suspends the fast charge in progress. When returned low, the IC resumes operation at the point where initially suspended.

CC **Charge control output**

An open-drain output used to control the charging current to the battery. CC switching to high impedance (Z) enables charging current to flow, and low to inhibit charging current. CC is modulated to provide pulse trickle.

Functional Description

Figure 2 shows a state diagram and Figure 3 shows a block diagram of the bq2002C.

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum allowable values. The voltage presented on the battery sense input, BAT, should represent a single-cell potential for the battery under charge. A resistor-divider ratio of

$$\frac{RB1}{RB2} = N - 1$$

is recommended to maintain the battery voltage within the valid range, where N is the number of cells, RB1 is the resistor connected to the positive battery terminal, and RB2 is the resistor connected to the negative battery terminal. See Figure 1.

Note: This resistor-divider network input impedance to end-to-end should be at least 200kΩ and less than 1 MΩ.

A ground-referenced negative temperature coefficient thermistor placed near the battery may be used as a low-cost temperature-to-voltage transducer. The temperature sense voltage input at TS is developed using a resistor-thermistor network between V_{CC} and V_{SS}. See Figure 1.

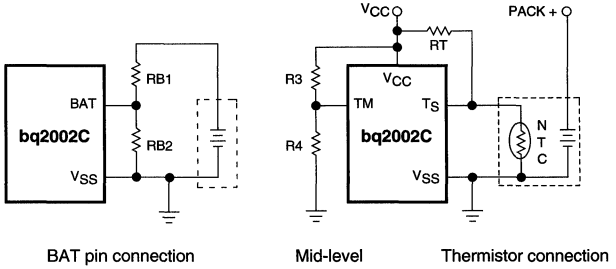


Figure 1. Voltage and Temperature Monitoring and TM Pin Configuration

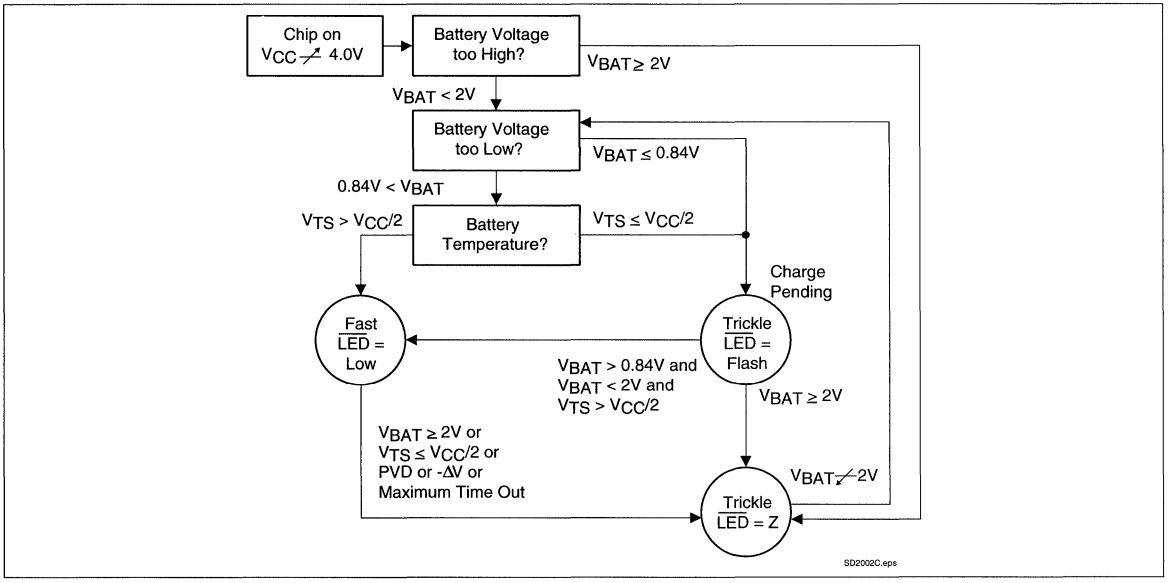


Figure 2. State Diagram

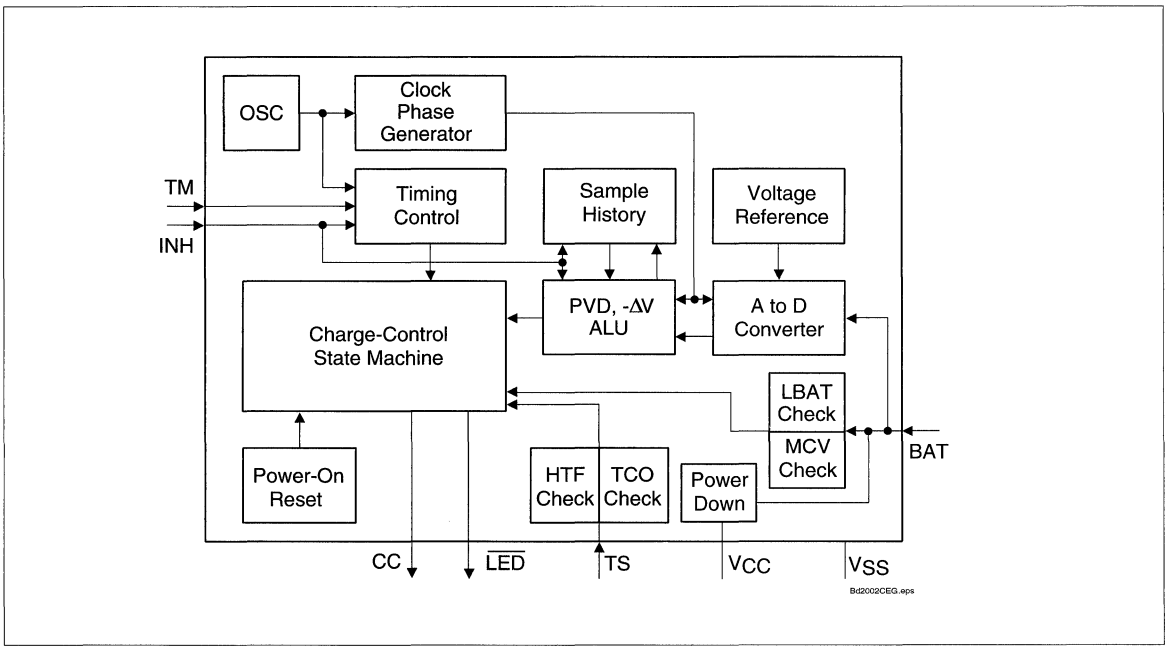


Figure 3. Block Diagram

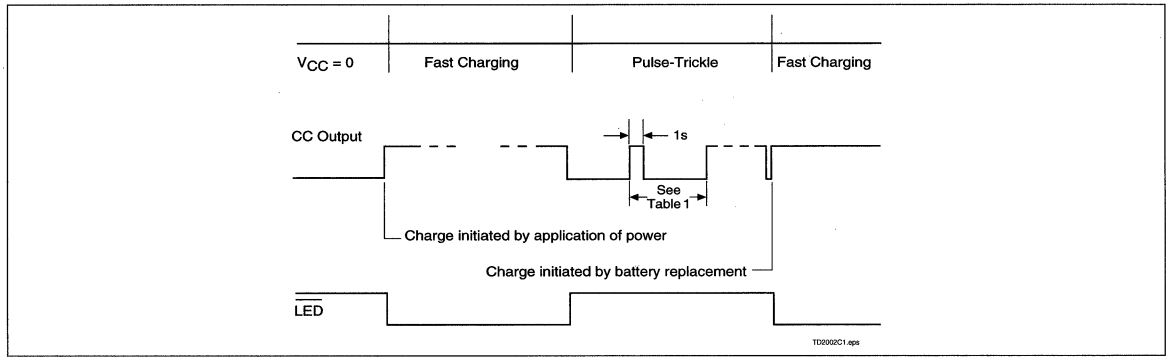


Figure 4. Charge Cycle Phases

Starting A Charge Cycle

Either of two events starts a charge cycle (see Figure 4):

1. Application of power to V_{CC} or

2. Voltage at the BAT pin falling through the maximum cell voltage V_{MCV} where

$$V_{MCV} = 2V \pm 5\%.$$

If the battery is within the configured temperature and voltage limits, the IC begins fast charge. The valid battery voltage range is $V_{LBAT} < V_{BAT} < V_{MCV}$, where

$$V_{LBAT} = 0.175 * V_{CC} \pm 20\%$$

The valid temperature range is $V_{TS} > V_{HTF}$ where

$$V_{HTF} = 0.6 * V_{CC} \pm 5\%.$$

If $V_{BAT} \leq V_{LBAT}$ or $V_{TS} \leq V_{HTF}$, the IC enters the charge-pending state. In this state pulse trickle charge is applied to the battery and the LED flashes until the voltage and temperature come into the allowed fast charge range or V_{BAT} rises above V_{MCV}. Anytime $V_{BAT} \geq V_{MCV}$, the IC enters the Charge Complete/Battery Absent state. In this state the LED is off and trickle charge is applied to the battery until the next new charge cycle begins.

Fast charge continues until termination by one or more of the five possible termination conditions:

- Peak voltage detection (PVD)
- Negative delta voltage (-ΔV)
- Maximum voltage
- Maximum temperature
- Maximum time

Table 1. Fast-Charge Safety Time/Hold-Off Table

Corresponding Fast-Charge Rate	TM	Termination	Typical Fast-Charge Time Limits (minutes)	Typical PVD and -ΔV Hold-Off Time (seconds)	Pulse-Trickle Rate	Pulse-Trickle Pulse Width (ms)	Maximum Synchronized Sampling Period (seconds)
C/2	Mid	PVD	160	300	C/32	73	18.7
1C	Low	PVD	80	150	C/32	37	18.7
2C	High	-ΔV	40	75	C/32	18	9.4

Notes: Typical conditions = 25°C, V_{CC} = 5.0V
Mid = $0.5 * V_{CC} \pm 0.5V$
Tolerance on all timing is ±12%.

4/8

PVD and -ΔV Termination

There are two modes for voltage termination, depending on the state of TM. For -ΔV (TM = high), if V_{BAT} is lower than any previously measured value by 12mV ±3mV, fast charge is terminated. For PVD (TM = low or mid), a decrease of 2.5mV ±2.5mV terminates fast charge. The PVD and -ΔV tests are valid in the range $1V < V_{BAT} < 2V$.

Synchronized Voltage Sampling

Voltage sampling at the BAT pin for PVD and -ΔV termination may be synchronized to an external stimulus using the INH input. Low-high-low input pulses between 100ns and 3.5ms in width must be applied at the INH pin with a frequency greater than the "maximum synchronized sampling period" set by the state of the TM pin as shown in Table 1. Voltage is sampled on the falling edge of such pulses. If the time between pulses is greater than the synchronizing period, voltage sampling "free-runs" at once every 17 seconds. A sample is taken by averaging together voltage measurements taken 57µs apart. The IC takes 32 measurements in PVD mode and 16 measurements in -ΔV mode. The resulting sample periods (9.17 and 18.18ms, respectively) filter out harmonics centered around 55 and 109Hz. This technique minimizes the effect of any AC line ripple that may feed through the power supply from either 50 or 60Hz AC sources. If the INH input remains high for more than 12ms, the voltage sample history kept by the IC and used for PVD and -ΔV termination decisions is erased and a new history is started. Such a reset is required when transitioning from free-running to synchronized voltage sampling. The response of the IC to pulses less than 100ns in width or between 3.5ms and 12ms is indeterminate. The tolerance on all timing is ±12%.

Voltage Termination Hold-off

A hold-off period occurs at the start of fast charging. During the hold-off time, the PVD and -ΔV terminations are disabled. This avoids premature termination on the voltage spikes sometimes produced by older batteries when fast-charge current is first applied. Maximum voltage and temperature terminations are not affected by the hold-off period.

Maximum Voltage, Temperature, and Time

Any time the voltage on the BAT pin exceeds the maximum cell voltage, V_{MCV}, fast charge is terminated.

Maximum temperature termination occurs anytime the voltage on the TS pin falls below the temperature cut-off threshold V_{TCO}, where

$$V_{TCO} = 0.5 * V_{CC} \pm 5\%.$$

Maximum charge time is configured using the TM pin. Time settings are available for corresponding charge rates of C/2, 1C, and 2C. Maximum time-out termination is enforced on the fast-charge phase, then reset, and enforced again on the top-off phase, if selected. There is no time limit on the trickle-charge phase.

Pulse-Trickle Charge

Pulse-trickle is used to compensate for self-discharge while the battery is idle in the charger. The battery is pulse-trickle charged by driving the CC pin active once per second for the period specified in Table 1. This results in a trickle rate of C/32.

TM Pin

The TM pin is a three-level pin used to select the charge timer, top-off, voltage termination mode, trickle rate, and voltage hold-off period options. Table 1 describes the states selected by the TM pin. The mid-level selection input is developed by a resistor divider between V_{CC} and ground that fixes the voltage on TM at $V_{CC}/2 \pm 0.5V$. See Figure 4.

Charge Status Indication

A fast charge in progress is uniquely indicated when the $\overline{LED}$ pin goes low. In the charge pending state, the $\overline{LED}$ pin is driven low for 500ms, then to high-Z for 500ms. The $\overline{LED}$ pin is driven to the high-Z state for all other conditions. Figure 2 outlines the state of the $\overline{LED}$ pin during charge.

Charge Inhibit

Fast charge and top-off may be inhibited by using the INH pin. When high, INH suspends all fast charge and top-off activity and the internal charge timer. INH freezes the current state of $\overline{LED}$ until inhibit is removed. Temperature monitoring is not affected by the INH pin. During charge inhibit, the bq2002C continues to pulse-trickle charge the battery per the TM selection. When INH returns low, charge control and the charge timer resume from the point where INH became active.

Low-Power Mode

The IC enters a low-power state when V_{BAT} is driven above the power-down threshold (V_{PD}) where

$$V_{PD} = V_{CC} - (1V \pm 0.5V)$$

Both the CC pin and the $\overline{LED}$ pin are driven to the high-Z state. The operating current is reduced to less than 1µA in this mode. When V_{BAT} returns to a value below V_{PD}, the IC pulse-trickle charges until the next new charge cycle begins.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	0	+70	°C	Commercial
T_{STG}	Storage temperature	-40	+85	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10 sec max.
T_{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds (T_A = 0 to 70°C; V_{CC} ±20%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{TCO}	Temperature cutoff	0.5 * V_{CC}	±5%	V	$V_{TS} \leq V_{TCO}$ inhibits/terminates fast charge
V_{HTF}	High-temperature fault	0.6 * V_{CC}	±5%	V	$V_{TS} \leq V_{HTF}$ inhibits fast charge start
V_{MCV}	Maximum cell voltage	2	±5%	V	$V_{BAT} \geq V_{MCV}$ inhibits/terminates fast charge
V_{LBAT}	Minimum cell voltage	0.175 * V_{CC}	±20%	V	$V_{BAT} \leq V_{LBAT}$ inhibits fast charge
-ΔV	BAT input change for -ΔV detection	-12	±3	mV	
PVD	BAT input change for PVD detection	-2.5	±2.5	mV	

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.0	5.0	6.0	V	
V_{DET}	-ΔV, PVD detect voltage	1	-	2	V	
V_{BAT}	Battery input	0	-	V_{CC}	V	
V_{TS}	Thermistor input	0.5	-	V_{CC}	V	V_{TS} < 0.5V prohibited
V_{IH}	Logic input high	0.5	-	-	V	INH
	Logic input high	V_{CC} - 0.5	-	-	V	TM
V_{IM}	Logic input mid	$\frac{V_{CC}}{2}$ - 0.5	-	$\frac{V_{CC}}{2}$ + 0.5	V	TM
V_{IL}	Logic input low	-	-	0.1	V	INH
	Logic input low	-	-	0.5	V	TM
V_{OL}	Logic output low	-	-	0.8	V	$\overline{LED}$, CC, I_{OL} = 10mA
V_{PD}	Power down	V_{CC} - 1.5	-	V_{CC} - 0.5	V	$V_{BAT} \geq V_{PD}$ max. powers down bq2002C; $V_{BAT} < V_{PD}$ min. = normal operation.
I_{CC}	Supply current	-	-	500	µA	Outputs unloaded, V_{CC} = 5.1V
I_{SB}	Standby current	-	-	1	µA	V_{CC} = 5.1V, V_{BAT} = V_{PD}
I_{OL}	$\overline{LED}$, CC sink	10	-	-	mA	@V_{OL} = V_{SS} + 0.8V
I_L	Input leakage	-	-	±1	µA	INH, CC, V = V_{SS} to V_{CC}
I_{OZ}	Output leakage in high-Z state	-5	-	-	µA	$\overline{LED}$, CC

Note: All voltages relative to V_{SS}.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
R_{BAT}	Battery input impedance	50	-	-	MΩ
R_{TS}	TS input impedance	50	-	-	MΩ

Timing (T_A = 0 to +70°C; V_{CC} ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
d_{FCV}	Time-base variation	-12	-	12	%	

Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

Data Sheet Revision History

Change No.	Page No.	Description
1	All	Revised format and outline of this data sheet

Note: Change 1 = Sept. 1997 B changes from Dec. 1995.

Ordering Information

bq2002C _

Package Option:
PN = 8-pin plastic DIP
SN = 8-pin narrow SOIC

Device:
bq2002C Fast-Charge IC

UNITRODE

bq2002D/T

NiCd/NiMH Fast-Charge Management ICs

Features

- Fast charge of nickel cadmium or nickel-metal hydride batteries
- Direct LED output displays charge status
- Fast-charge termination by rate of rise of temperature, maximum voltage, maximum temperature, and maximum time
- Internal band-gap voltage reference
- Optional top-off charge (bq2002T only)
- Selectable pulse-trickle charge rates (bq2002T only)
- Low-power mode
- 8-pin 300-mil DIP or 150-mil SOIC

General Description

The bq2002D/T Fast-Charge IC are low-cost CMOS battery-charge controllers able to provide reliable charge termination for both NiCd and NiMH battery applications. Controlling a current-limited or constant-current supply allows the bq2002D/T to be the basis for a cost-effective stand-alone or system-integrated charger. The bq2002D/T integrates fast charge with optional top-off and pulsed-trickle control in a single IC for charging one or more NiCd or NiMH battery cells.

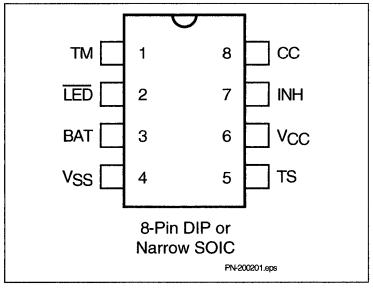
Fast charge is initiated on application of the charging supply or battery replacement. For safety, fast charge is inhibited if the battery temperature and voltage are outside configured limits.

Fast charge is terminated by any of the following:

- Rate of temperature rise
- Maximum voltage
- Maximum temperature
- Maximum time

After fast charge, the bq2002T optionally tops-off and pulse-trickles the battery per the pre-configured limits. Fast charge may be inhibited using the INH pin. The bq2002D/T may be placed in low-standby-power mode to reduce system power consumption.

Pin Connections



Pin Names

TM	Timer mode select input	TS	Temperature sense input
$\overline{LED}$	Charging status output	V_{CC}	Supply voltage input
BAT	Battery voltage input	INH	Charge inhibit input
V_{SS}	System ground	CC	Charge control output

bq2002D/T Selection Guide

Part No.	TCO	HTF	LTF	Fast Charge	Time-Out	Top-Off	Maintenance
bq2002D	0.225 * V_{CC}	0.25 * V_{CC}	0.4 * V_{CC}	C/4	320 min	C/64	C/256
				1C	80 min	C/16	C/256
				2C	40 min	None	C/128
bq2002T	0.225 * V_{CC}	0.25 * V_{CC}	None	C/4	440 min	None	None
				1C	110 min	None	None
				2C	55 min	None	None

Pin Descriptions

TM **Timer mode input**

A three-level input that controls the settings for the fast charge safety timer, voltage termination mode, top-off, pulse-trickle, and voltage hold-off time.

$\overline{LED}$ **Charging output status**

Open-drain output that indicates the charging status.

BAT **Battery input voltage**

The battery voltage sense input. The input to this pin is created by a high-impedance resistor divider network connected between the positive and negative terminals of the battery.

V_{SS} **System ground**

TS **Temperature sense input**

Input for an external battery temperature monitoring thermistor.

V_{CC} **Supply voltage input**

5.0V ±20% power input.

INH **Charge inhibit input**

When high, INH suspends the fast charge in progress. When returned low, the IC resumes operation at the point where initially suspended.

CC **Charge control output**

An open-drain output used to control the charging current to the battery. CC switching to high impedance (Z) enables charging current to flow, and low to inhibit charging current. CC is modulated to provide top-off, if enabled, and pulse trickle.

Functional Description

Figures 2 and 3 show state diagrams of bq2002D/T and Figure 4 shows the block diagram of the bq2002D/T

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum allowable values. The voltage presented on the battery sense input, BAT, should represent a single-cell potential for the battery under charge. A resistor-divider ratio of:

$$\frac{RB1}{RB2} = N - 1$$

is recommended to maintain the battery voltage within the valid range, where N is the number of cells, RB1 is the resistor connected to the positive battery terminal, and RB2 is the resistor connected to the negative battery terminal. See Figure 1.

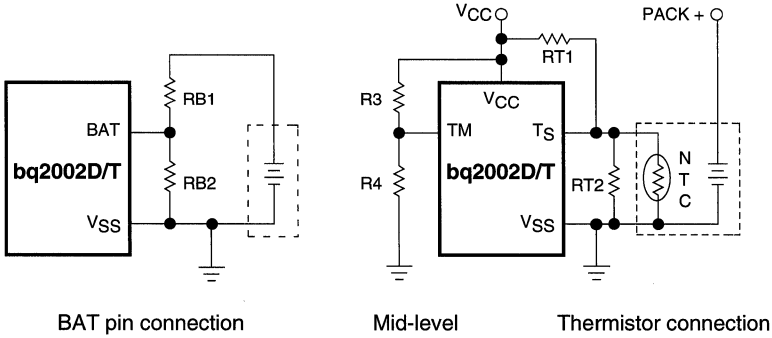


Figure 1. Voltage and Temperature Monitoring and TM Pin Configuration

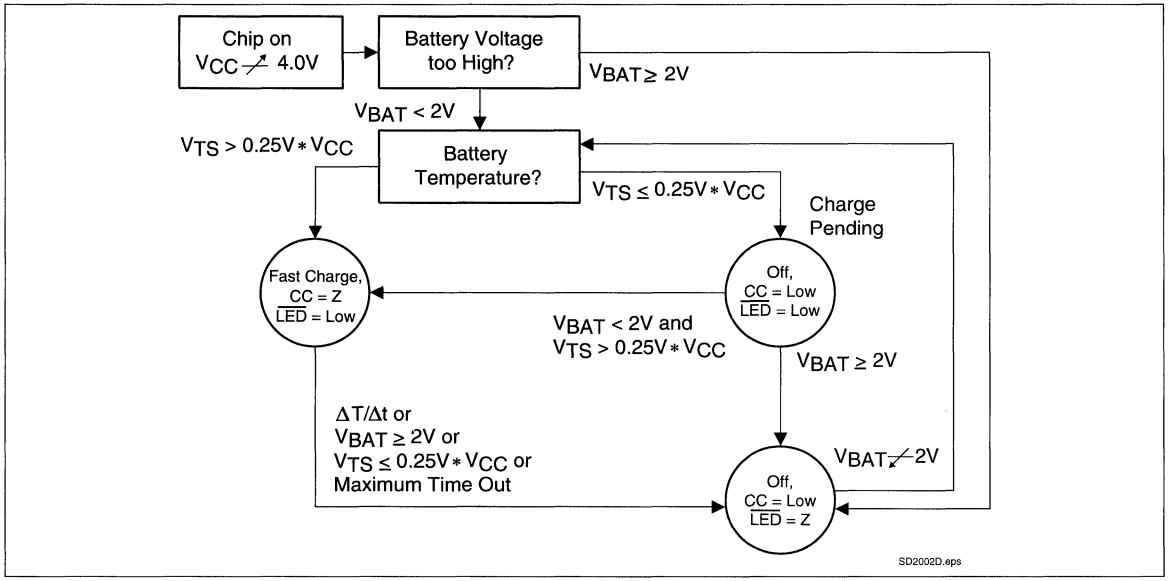


Figure 2. bq2002D State Diagram

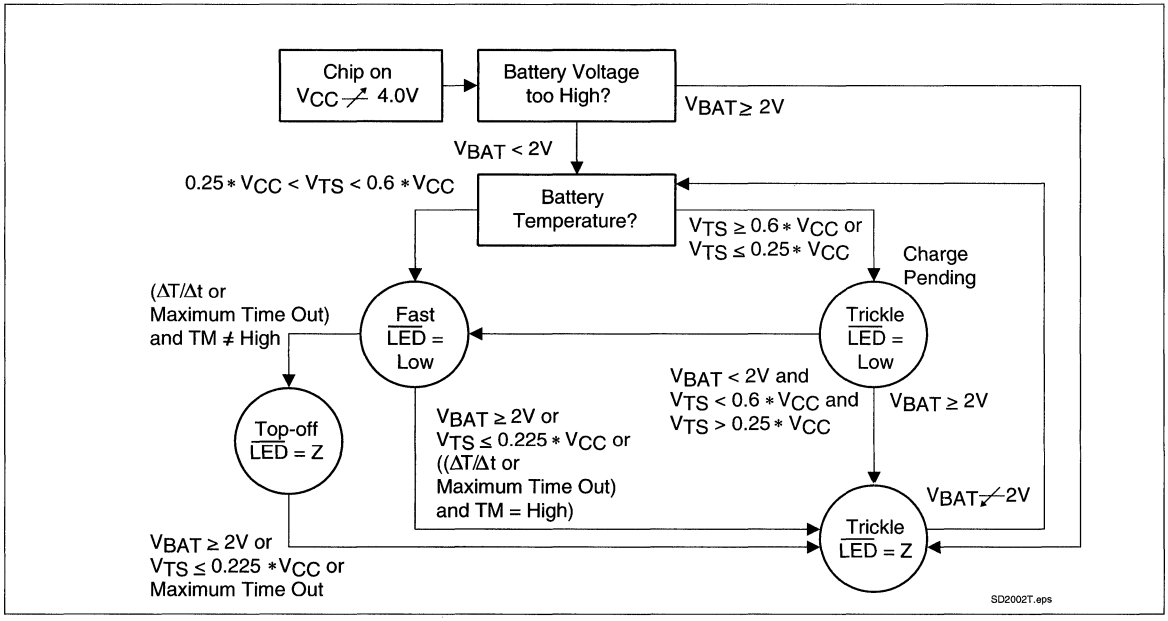


Figure 3. bq2002T State Diagram

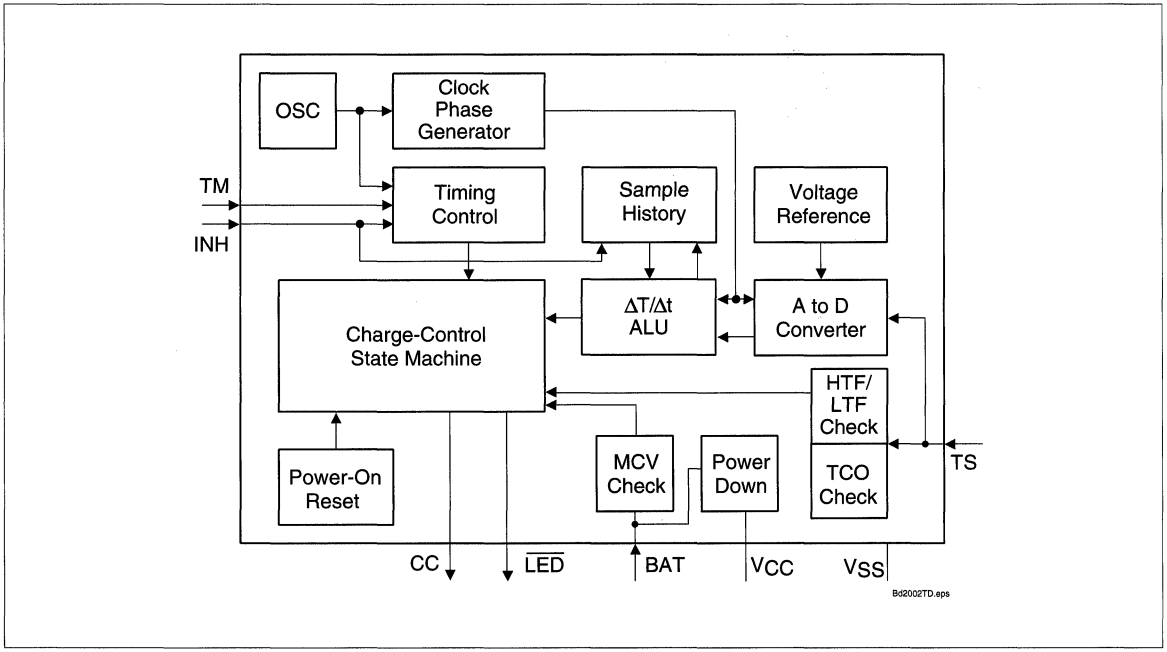


Figure 4. Block Diagram

Note: This resistor-divider network input impedance to end-to-end should be at least 200kΩ and less than 1 MΩ.

A ground-referenced negative temperature coefficient thermistor placed in proximity to the battery may be used as a low-cost temperature-to-voltage transducer. The temperature sense voltage input at TS is developed using a resistor-thermistor network between V_{CC} and V_{SS}. See Figure 1.

Starting A Charge Cycle

Either of two events starts a charge cycle (see Figure 5):

1. Application of power to V_{CC} or

2. Voltage at the BAT pin falling through the maximum cell voltage where:

$$V_{MCV} = 2V \pm 5\%.$$

If the battery is within the configured temperature and voltage limits, the IC begins fast charge. The valid battery voltage range is $V_{BAT} < V_{MCV}$. The valid temperature range is $V_{HTF} < V_{TS} < V_{LTF}$ for the bq2002T and $V_{HTF} < V_{TS}$ for the bq2002D where:

$$V_{LTF} = 0.4 * V_{CC} \pm 5\%.$$

$$V_{HTF} = 0.25 * V_{CC} \pm 5\% \text{ (bq2002T only).}$$

If the battery voltage or temperature is outside of these limits, the IC pulse-trickle charges until the temperature falls within the allowed fast charge range or a new charge cycle is started.

Fast charge continues until termination by one or more of the four possible termination conditions:

- Rate of temperature rise
- Maximum voltage
- Maximum temperature
- Maximum time

ΔT/Δt Termination

The bq2002D/T samples at the voltage at the TS pin every 19s and compares it to the value measured three samples earlier. If the voltage has fallen 25.6mV or more, fast charge is terminated. The ΔT/Δt termination test is valid only when $V_{TCO} < V_{TS} < V_{LTF}$ for the bq2002T and $V_{TCO} < V_{TS}$ for the bq2002D.

Temperature Sampling

A sample is taken by averaging together 16 measurements taken 57µs apart. The resulting sample period (18.18ms) filters out harmonics around 55Hz. This tech-

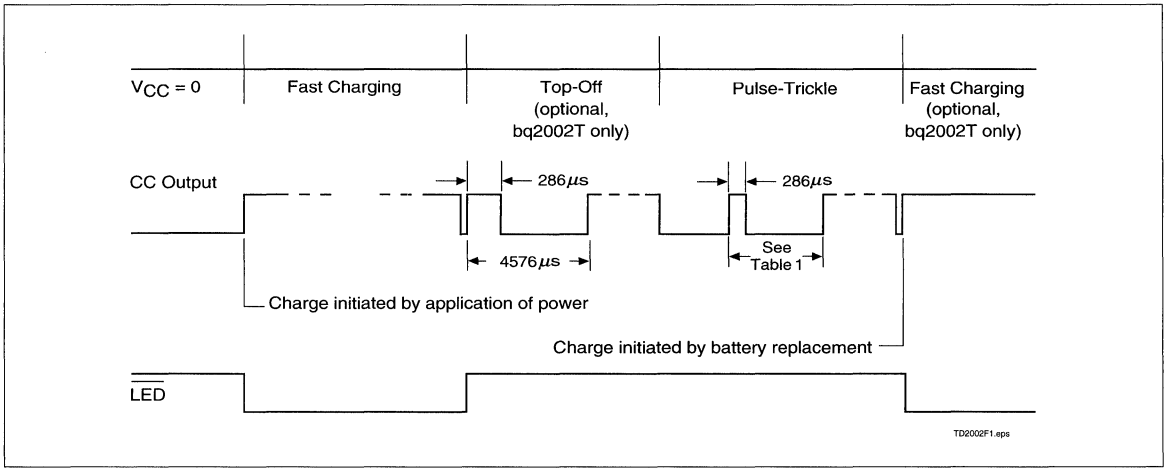


Figure 5. Charge Cycle Phases

nique minimizes the effect of any AC line ripple that may feed through the power supply from either 50Hz or 60Hz AC sources. Tolerance on all timing is ±20%.

Maximum Voltage, Temperature, and Time

Any time the voltage on the BAT pin exceeds the maximum cell voltage, V_{MCV}, fast charge or optional top-off charge is terminated.

Maximum temperature termination occurs anytime the voltage on the TS pin falls below the temperature cut-off threshold V_{TCO} where:

$$V_{TCO} = 0.225 * V_{CC} \pm 5\%$$

Maximum charge time is configured using the TM pin. Time settings are available for corresponding charge rates of C/4, 1C, and 2C. Maximum time-out termination is enforced on the fast-charge phase, then reset, and

Table 1. Fast-Charge Safety Time/Top-Off Table

	Corresponding Fast-Charge Rate	TM	Typical Fast-Charge and Top-Off Time Limits (minutes)	Top-Off Rate	Pulse-Trickle Rate	Pulse-Trickle Period (ms)
bq2002D	C/4	Mid	440	NA	NA	NA
	1C	Low	110	NA	NA	NA
	2C	High	55	NA	NA	NA
bq2002T	C/4	Mid	320	C/64	C/256	18.3
	1C	Low	80	C/16	C/256	73.1
	2C	High	40	Disabled	C/128	73.1

Notes: Typical conditions = 25°C, V_{CC} = 5.0V.
Mid = 0.5 * V_{CC} ±0.5V
Tolerance on all timing is ±20%

5/10

enforced again on the top-off phase, if selected (bq2002T only). There is no time limit on the trickle-charge phase.

Top-off Charge—bq2002T Only

An optional top-off charge phase may be selected to follow fast charge termination for 1C and C/4 rates. This phase may be necessary on NiMH or other battery chemistries that have a tendency to terminate charge prior to reaching full capacity. With top-off enabled, charging continues at a reduced rate after fast-charge termination for a period of time selected by the TM pin. (See Table 1.) During top-off, the CC pin is modulated at a duty cycle of 286µs active for every 4290µs inactive. This modulation results in an average rate 1/16th that of the fast charge rate. Maximum voltage, time, and temperature are the only termination methods enabled during top-off.

Pulse-Trickle Charge—bq2002T Only

Pulse-trickle is used to compensate for self-discharge while the battery is idle in the charger. The battery is pulse-trickle charged by driving the CC pin active for a period of 286µs for every 72.9ms of inactivity for 1C and 2C selections, and 286µs for every 17.9ms of inactivity for C/4 selection. This results in a trickle rate of C/256 for the top-off enabled mode and C/128 otherwise.

TM Pin

The TM pin is a three-level pin used to select the charge timer, top-off, voltage termination mode, trickle rate, and voltage hold-off period options. Table 1 describes the states selected by the TM pin. The mid-level selection input is developed by a resistor divider between V_{CC} and ground that fixes the voltage on TM at $V_{CC}/2 \pm 0.5V$. See Figure 5.

Charge Status Indication

In the fast charge and charge pending states, and whenever the inhibit pin is active, the $\overline{LED}$ pin goes low. The $\overline{LED}$ pin is driven to the high-Z state for all other conditions. Figure 3 outlines the state of the $\overline{LED}$ pin during charge.

Charge Inhibit

Fast charge and top-off may be inhibited by using the INH pin. When high, INH suspends all fast charge and top-off activity and the internal charge timer. INH freezes the current state of $\overline{LED}$ until inhibit is removed. Temperature monitoring is not affected by the INH pin. During charge inhibit, the bq2002D/T continues to pulse-trickle charge the battery per the TM selection. When INH returns low, charge control and the charge timer resume from the point where INH became active. The V_{TS} sample history is cleared by INH.

Low-Power Mode

The IC enters a low-power state when V_{BAT} is driven above the power-down threshold (V_{PD}) where:

$$V_{PD} = V_{CC} - (1V \pm 0.5V)$$

Both the CC pin and the $\overline{LED}$ pin are driven to the high-Z state. The operating current is reduced to less than 1µA in this mode. When V_{BAT} returns to a value below V_{PD}, the IC pulse-trickle charges until the next new charge cycle begins.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	0	+70	°C	Commercial
T_{STG}	Storage temperature	-40	+85	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10 sec max.
T_{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds (T_A = 0 to 70°C; V_{CC} ±20%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{TCO}	Temperature cutoff	0.225 * V_{CC}	±5%	V	$V_{TS} \le V_{TCO}$ terminates fast charge and top-off
V_{HTF}	High-temperature fault	0.25 * V_{CC}	±5%	V	$V_{TS} \le V_{HTF}$ inhibits fast charge start
V_{LTF}	Low-temperature fault	0.4 * V_{CC}	±5%	V	$V_{TS} \ge V_{LTF}$ inhibits fast charge start (bq2002T only)
V_{MCV}	Maximum cell voltage	2	±5%	V	$V_{BAT} \ge V_{MCV}$ inhibits/terminates fast charge

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.0	5.0	6.0	V	
V_{BAT}	Battery input	0	-	V_{CC}	V	
V_{TS}	Thermistor input	0.5	-	V_{CC}	V	V_{TS} < 0.5V prohibited
V_{IH}	Logic input high	0.5	-	-	V	INH
	Logic input high	V_{CC} - 0.5	-	-	V	TM
V_{IM}	Logic input mid	$\frac{V_{CC}}{2}$ - 0.5	-	$\frac{V_{CC}}{2}$ + 0.5	V	TM
V_{IL}	Logic input low	-	-	0.1	V	INH
	Logic input low	-	-	0.5	V	TM
V_{OL}	Logic output low	-	-	0.8	V	$\overline{LED}$, CC, I_{OL} = 10mA
V_{PD}	Power down	V_{CC} - 1.5	-	V_{CC} - 0.5	V	$V_{BAT} \geq V_{PD}$ max. powers down bq2002D/T; $V_{BAT} < V_{PD}$ min. = normal operation.
I_{CC}	Supply current	-	-	500	µA	Outputs unloaded, V_{CC} = 5.1V
I_{SB}	Standby current	-	-	1	µA	V_{CC} = 5.1V, V_{BAT} = V_{PD}
I_{OL}	$\overline{LED}$, CC sink	10	-	-	mA	@V_{OL} = V_{SS} + 0.8V
I_L	Input leakage	-	-	±1	µA	INH, CC, V = V_{SS} to V_{CC}
I_{OZ}	Output leakage in high-Z state	-5	-	-	µA	$\overline{LED}$, CC

Note: All voltages relative to V_{SS}.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
R_{BAT}	Battery input impedance	50	-	-	MΩ
R_{TS}	TS input impedance	50	-	-	MΩ

Timing (T_A = 0 to +70°C; V_{CC} ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
d_{FCV}	Time-base variation	-20	-	20	%	

Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

Data Sheet Revision History

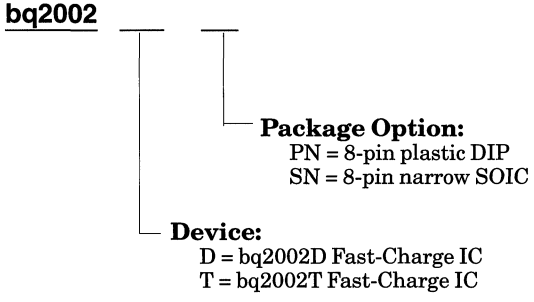
Change No.	Page No.	Description	Nature of Change
1	3	Was: Table 1 gave the bq2002D/T Operational Summary. Is: Figure 2 gives the bq2002D/T Operational Summary.	Changed table to figure.
1	5	Added top-off values.	Added column and values.
2	All	Revised and expanded this data sheet	
3	All	Revised and included bq2002D	Addition of device

Notes: Change 1 = Sept. 1996 B changes from Aug. 1994.

Change 2 = Aug. 1997 C changes from Sept. 1996 B.

Change 3 = Jan. 1999 D changes from Aug. 1997 C.

Ordering Information



UNITRODE

bq2002E/G

NiCd/NiMH Fast-Charge Management ICs

Features

- Fast charge of nickel cadmium or nickel-metal hydride batteries
- Direct LED output displays charge status
- Fast-charge termination by -ΔV, maximum voltage, maximum temperature, and maximum time
- Internal band-gap voltage reference
- Optional top-off charge
- Selectable pulse trickle charge rates
- Low-power mode
- 8-pin 300-mil DIP or 150-mil SOIC

General Description

The bq2002E and bq2002G Fast-Charge ICs are low-cost CMOS battery-charge controllers providing reliable charge termination for both NiCd and NiMH battery applications. Controlling a current-limited or constant-current supply allows the bq2002E/G to be the basis for a cost-effective stand-alone or system-integrated charger. The bq2002E/G integrates fast charge with optional top-off and pulsed- trickle control in a single IC for charging one or more NiCd or NiMH battery cells.

Fast charge is initiated on application of the charging supply or battery replacement. For safety, fast charge is inhibited if the battery temperature and voltage are outside configured limits.

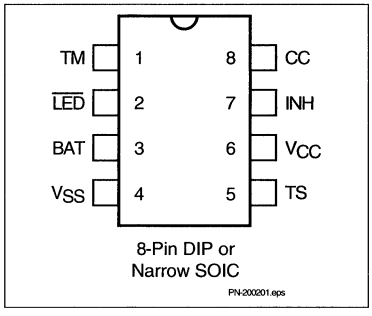
Fast charge is terminated by any of the following:

- Peak voltage detection (PVD)
- Negative delta voltage (-ΔV)
- Maximum voltage
- Maximum temperature
- Maximum time

After fast charge, the bq2002E/G optionally tops-off and pulse-trickles the battery per the pre-configured limits. Fast charge may be inhibited using the INH pin. The bq2002E/G may also be placed in low-standby-power mode to reduce system power consumption.

The bq2002E differs from the bq2002G only in that a slightly different set of fast-charge and top-off time limits is available. All differences between the two ICs are illustrated in Table 1.

Pin Connections



Pin Names

TM	Timer mode select input	TS	Temperature sense input
$\overline{LED}$	Charging status output	V_{CC}	Supply voltage input
BAT	Battery voltage input	INH	Charge inhibit input
V_{SS}	System ground	CC	Charge control output

bq2002E/G Selection Guide

Part No.	LBAT	TCO	HTF	LTF	-ΔV	PVD	Fast Charge	t_{MTO}	Top-Off	Maintenance
bq2002E	0.175 * V_{CC}	0.5 * V_{CC}	0.6 * V_{CC}	None		✔	C/2	200	None	C/32
						✔	1C	80	C/16	C/32
					✔		2C	40	None	C/32
bq2002G	0.175 * V_{CC}	0.5 * V_{CC}	0.6 * V_{CC}	None		✔	C/2	160	None	C/32
						✔	1C	80	C/16	C/32
					✔		2C	40	None	C/32

Pin Descriptions

TM **Timer mode input**

A three-level input that controls the settings for the fast charge safety timer, voltage termination mode, top-off, pulse-trickle, and voltage hold-off time.

$\overline{\text{LED}}$ **Charging output status**

Open-drain output that indicates the charging status.

BAT **Battery input voltage**

The battery voltage sense input. The input to this pin is created by a high-impedance resistor divider network connected between the positive and negative terminals of the battery.

V_{SS} **System ground**

TS **Temperature sense input**

Input for an external battery temperature monitoring thermistor.

V_{CC} **Supply voltage input**

5.0V ±20% power input.

INH **Charge inhibit input**

When high, INH suspends the fast charge in progress. When returned low, the IC resumes operation at the point where initially suspended.

CC **Charge control output**

An open-drain output used to control the charging current to the battery. CC switching to high impedance (Z) enables charging current to flow, and low to inhibit charging current. CC is modulated to provide top-off, if enabled, and pulse trickle.

Functional Description

Figure 2 shows a state diagram and Figure 3 shows a block diagram of the bq2002E/G.

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum allowable values. The voltage presented on the battery sense input, BAT, should represent a single-cell potential for the battery under charge. A resistor-divider ratio of

$$\frac{RB1}{RB2} = N - 1$$

is recommended to maintain the battery voltage within the valid range, where N is the number of cells, RB1 is the resistor connected to the positive battery terminal, and RB2 is the resistor connected to the negative battery terminal. See Figure 1.

Note: This resistor-divider network input impedance to end-to-end should be at least 200kΩ and less than 1 MΩ.

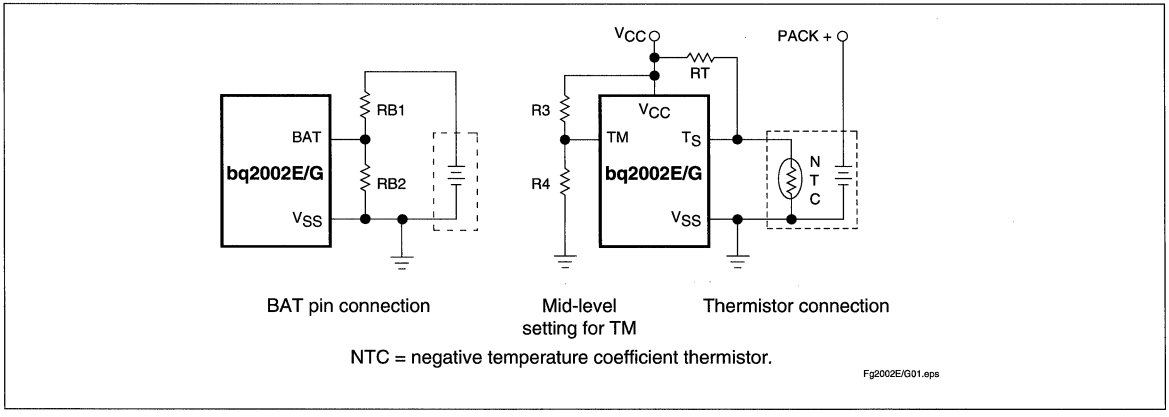


Figure 1. Voltage and Temperature Monitoring and TM Pin Configuration

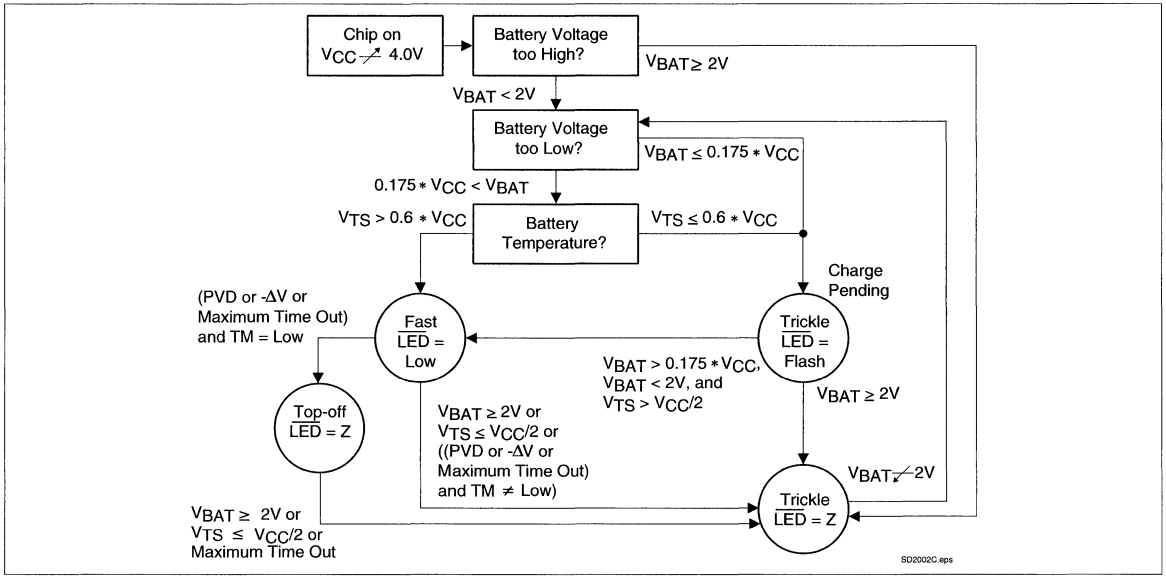


Figure 2. State Diagram

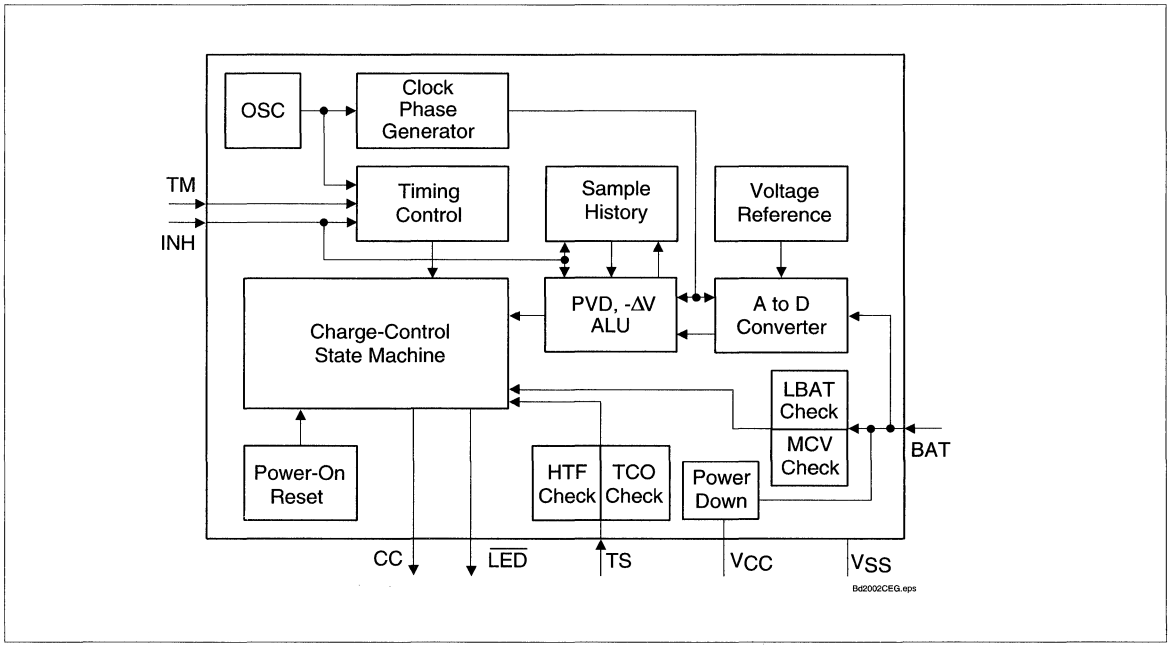


Figure 3. Block Diagram

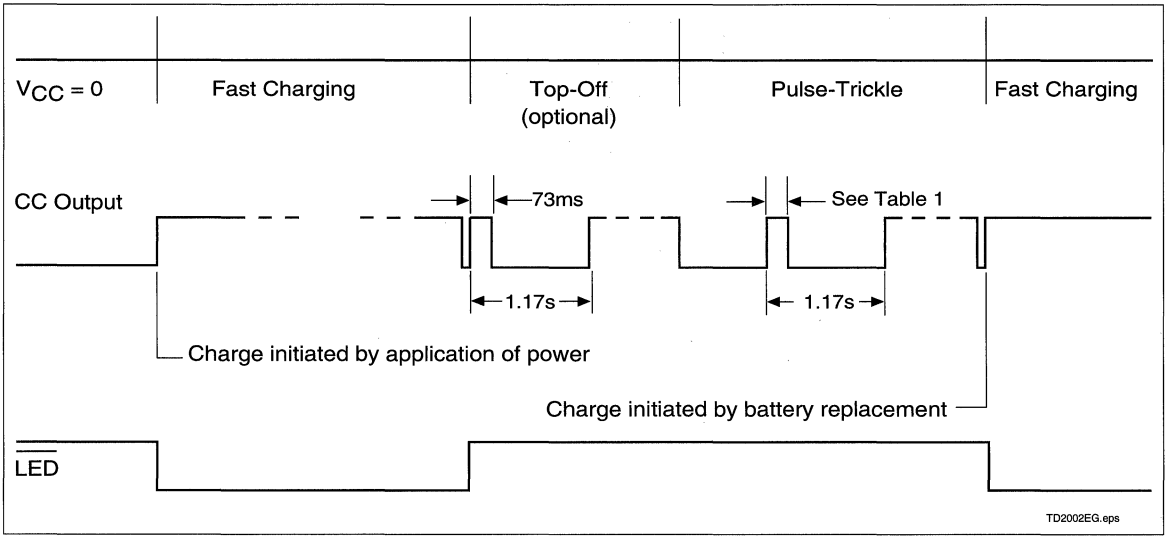


Figure 4. Charge Cycle Phases

A ground-referenced negative temperature coefficient thermistor placed near the battery may be used as a low-cost temperature-to-voltage transducer. The temperature sense voltage input at TS is developed using a resistor-thermistor network between V_{CC} and V_{SS}. See Figure 1.

Starting A Charge Cycle

Either of two events starts a charge cycle (see Figure 4):

1. Application of power to V_{CC} or

2. Voltage at the BAT pin falling through the maximum cell voltage V_{MCV} where

$$V_{MCV} = 2V \pm 5\%.$$

If the battery is within the configured temperature and voltage limits, the IC begins fast charge. The valid battery voltage range is $V_{LBAT} < V_{BAT} < V_{MCV}$, where

Table 1. Fast-Charge Safety Time/Hold-Off/Top-Off Table

Corresponding Fast-Charge Rate	TM	Termination	Typical Fast-Charge and Top-Off Time Limits (minutes)		Typical PVD and -ΔV Hold-Off Time (seconds)	Top-Off Rate	Pulse-Trickle Rate	Pulse-Trickle Width (ms)	Maximum Synchronized Sampling Period (seconds)
			bq2002E	bq2002G					
C/2	Mid	PVD	200	160	300	Disabled	C/32	73	18.7
1C	Low	PVD	80	80	150	C/16	C/32	37	18.7
2C	High	-ΔV	40	40	75	Disabled	C/32	18	9.4

Notes: Typical conditions = 25°C, V_{CC} = 5.0V
Mid = 0.5 * V_{CC} ±0.5V
Tolerance on all timing is ±12%.

4/9

$$V_{LBAT} = 0.175 * V_{CC} \pm 20\%$$

The valid temperature range is $V_{TS} > V_{HTF}$ where

$$V_{HTF} = 0.6 * V_{CC} \pm 5\%.$$

If the battery voltage or temperature is outside of these limits, the IC pulse-trickle charges until the next new charge cycle begins.

If $V_{MCV} < V_{BAT} < V_{PD}$ (see "Low-Power Mode") when a new battery is inserted, a delay of 0.35 to 0.9s is imposed before the new charge cycle begins.

Fast charge continues until termination by one or more of the five possible termination conditions:

- Peak voltage detection (PVD)
- Negative delta voltage (-ΔV)
- Maximum voltage
- Maximum temperature
- Maximum time

PVD and -ΔV Termination

There are two modes for voltage termination, depending on the state of TM. For -ΔV (TM = high), if V_{BAT} is lower than any previously measured value by 12mV ±3mV, fast charge is terminated. For PVD (TM = low or mid), a decrease of 2.5mV ±2.5mV terminates fast charge. The PVD and -ΔV tests are valid in the range $1V < V_{BAT} < 2V$.

Synchronized Voltage Sampling

Voltage sampling at the BAT pin for PVD and -ΔV termination may be synchronized to an external stimulus using the INH input. Low-high-low input pulses between 100ns and 3.5ms in width must be applied at the INH pin with a frequency greater than the "maximum synchronized sampling period" set by the state of the TM pin as shown in Table 1. Voltage is sampled on the falling edge of such pulses.

If the time between pulses is greater than the synchronizing period, voltage sampling "free-runs" at once every 17 seconds. A sample is taken by averaging together voltage measurements taken 57µs apart. The IC takes 32 measurements in PVD mode and 16 measurements in -ΔV mode. The resulting sample periods (9.17 and 18.18ms, respectively) filter out harmonics centered around 55 and 109Hz. This technique minimizes the effect of any AC line ripple that may feed through the power supply from either 50 or 60Hz AC sources.

If the INH input remains high for more than 12ms, the voltage sample history kept by the IC and used for PVD and -ΔV termination decisions is erased and a new history is started. Such a reset is required when transitioning from free-running to synchronized voltage sampling. The response of the IC to pulses less than 100ns in width or between 3.5ms and 12ms is indeterminate. Tolerance on all timing is ±12%.

Voltage Termination Hold-off

A hold-off period occurs at the start of fast charging. During the hold-off time, the PVD and -ΔV terminations are disabled. This avoids premature termination on the voltage spikes sometimes produced by older batteries when fast-charge current is first applied. Maximum voltage and temperature terminations are not affected by the hold-off period.

Maximum Voltage, Temperature, and Time

Any time the voltage on the BAT pin exceeds the maximum cell voltage,V_{MCV}, fast charge or optional top-off charge is terminated.

Maximum temperature termination occurs anytime the voltage on the TS pin falls below the temperature cut-off threshold V_{TCO} where

$$V_{TCO} = 0.5 * V_{CC} \pm 5\%.$$

Maximum charge time is configured using the TM pin. Time settings are available for corresponding charge rates of C/2, 1C, and 2C. Maximum time-out termination is enforced on the fast-charge phase, then reset, and enforced again on the top-off phase, if selected. There is no time limit on the trickle-charge phase.

Top-off Charge

An optional top-off charge phase may be selected to follow fast charge termination for 1C and C/2 rates. This phase may be necessary on NiMH or other battery chemistries that have a tendency to terminate charge before reaching full capacity. With top-off enabled, charging continues at a reduced rate after fast-charge termination for a period of time selected by the TM pin. (See Table 1.) During top-off, the CC pin is modulated at a duty cycle of 73ms active for every 1097ms inactive. This modulation results in an average rate 1/16th that of the fast charge rate. Maximum voltage, time, and temperature are the only termination methods enabled during top-off.

Pulse-Trickle Charge

Pulse-trickle is used to compensate for self-discharge while the battery is idle in the charger. The battery is pulse-trickle charged by driving the CC pin active once every 1.17s for the period specified in Table 1. This results in a trickle rate of C/32.

TM Pin

The TM pin is a three-level pin used to select the charge timer, top-off, voltage termination mode, trickle

rate, and voltage hold-off period options. Table 1 describes the states selected by the TM pin. The mid-level selection input is developed by a resistor divider between V_{CC} and ground that fixes the voltage on TM at $V_{CC}/2 \pm 0.5V$. See Figure 4.

Charge Status Indication

A fast charge in progress is uniquely indicated when the $\overline{LED}$ pin goes low. The $\overline{LED}$ pin is driven to the high-Z state for all conditions other than fast charge. Figure 2 outlines the state of the $\overline{LED}$ pin during charge.

Charge Inhibit

Fast charge and top-off may be inhibited by using the INH pin. When high, INH suspends all fast charge and top-off activity and the internal charge timer. INH freezes the current state of $\overline{LED}$ until inhibit is removed. Temperature monitoring is not affected by the INH pin. During charge inhibit, the bq2002E/G continues to pulse-trickle charge the battery per the TM selection. When INH returns low, charge control and the charge timer resume from the point where INH became active.

Low-Power Mode

The IC enters a low-power state when V_{BAT} is driven above the power-down threshold (V_{PD}) where

$$V_{PD} = V_{CC} - (1V \pm 0.5V)$$

Both the CC pin and the $\overline{LED}$ pin are driven to the high-Z state. The operating current is reduced to less than 1µA in this mode. When V_{BAT} returns to a value below V_{PD}, the IC pulse-trickle charges until the next new charge cycle begins.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	0	+70	°C	Commercial
T_{STG}	Storage temperature	-40	+85	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10 sec max.
T_{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds (T_A = 0 to 70°C; V_{CC} ±20%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{TCO}	Temperature cutoff	0.5 * V_{CC}	±5%	V	$V_{TS} \leq V_{TCO}$ inhibits/terminates fast charge and top-off
V_{HTF}	High temperature fault	0.6 * VCC	±5%	V	$V_{TS} < V_{HTF}$ inhibits fast charge start
V_{MCV}	Maximum cell voltage	2	±5%	V	$V_{BAT} \geq V_{MCV}$ inhibits/terminates fast charge and top-off
V_{LBAT}	Minimum cell voltage	0.175 * V_{CC}	±20%	V	$V_{BAT} < V_{LBAT}$ inhibits fast charge start
-ΔV	BAT input change for -ΔV detection	-12	±3	mV	
PVD	BAT input change for PVD detection	-2.5	±2.5	mV	

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.0	5.0	6.0	V	
V_{DET}	-ΔV, PVD detect voltage	1	-	2	V	
V_{BAT}	Battery input	0	-	V_{CC}	V	
V_{TS}	Thermistor input	0.5	-	V_{CC}	V	V_{TS} < 0.5V prohibited
V_{IH}	Logic input high	0.5	-	-	V	INH
	Logic input high	V_{CC} - 0.5	-	-	V	TM
V_{IM}	Logic input mid	$\frac{V_{CC}}{2}$ - 0.5	-	$\frac{V_{CC}}{2}$ + 0.5	V	TM
V_{IL}	Logic input low	-	-	0.1	V	INH
	Logic input low	-	-	0.5	V	TM
V_{OL}	Logic output low	-	-	0.8	V	$\overline{LED}$, CC, I_{OL} = 10mA
V_{PD}	Power down	V_{CC} - 1.5	-	V_{CC} - 0.5	V	$V_{BAT} \geq V_{PD}$ max. powers down bq2002E/G; $V_{BAT} < V_{PD}$ min. = normal operation.
I_{CC}	Supply current	-	-	500	µA	Outputs unloaded, V_{CC} = 5.1V
I_{SB}	Standby current	-	-	1	µA	V_{CC} = 5.1V, V_{BAT} = V_{PD}
I_{OL}	$\overline{LED}$, CC sink	10	-	-	mA	@V_{OL} = V_{SS} + 0.8V
I_L	Input leakage	-	-	±1	µA	INH, CC, V = V_{SS} to V_{CC}
I_{OZ}	Output leakage in high-Z state	-5	-	-	µA	$\overline{LED}$, CC

Note: All voltages relative to V_{SS}.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
R_{BAT}	Battery input impedance	50	-	-	MΩ
R_{TS}	TS input impedance	50	-	-	MΩ

Timing (TA = 0 to +70°C; VCC ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
d_{FCV}	Time base variation	-12	-	12	%	
t_{DLY}	Start-up delay	0.35	-	0.9	s	Starting from $V_{MCV} < V_{BAT} < V_{PD}$

Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	1	Added selection guide	

Notes: Change 1 = Feb. 1999 B changes from Sept. 1997.

Ordering Information

bq2002E/G _

Package Option:
PN = 8-pin plastic DIP
SN = 8-pin narrow SOIC

Device:
bq2002E Fast-Charge IC
bq2002G Fast-Charge IC

9/9

UNITRODE

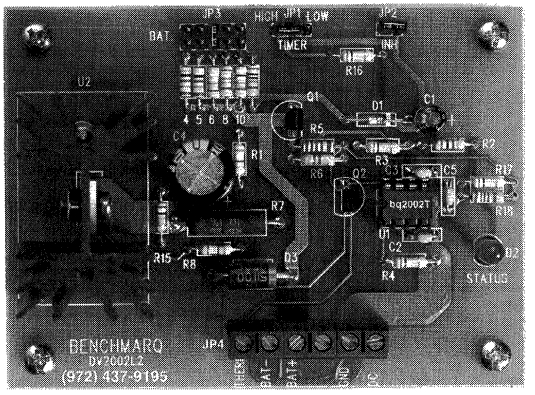
Product Brief **DV2002L2/TL2**

Fast-Charge Development Systems

Control of LM317 Linear Regulator

Features

- bq2002/T fast-charge control evaluation and development
- Charge current sourced from an on-board linear regulator (up to 1.5A)
- Fast charge of 4, 5, 6, 8, and 10 NiCd or NiMH cells (contact Unitrode for other cell counts)
- Fast-charge termination by negative delta voltage (-ΔV) or peak voltage detect (bq2002) or ΔT/Δt (bq2002T)
- Maximum temperature and maximum time safety terminations
- -ΔV/peak voltage detect, hold-off, top-off, maximum time, and number of cells are jumper-configurable
- Inhibit fast charge by a logic-level input



General Description

The DV2002L2/TL2 Development System provides a development environment for the bq2002 and bq2002T Fast-Charge ICs. The DV2002L2/TL2 incorporates a bq2002/T and a linear regulator to provide fast charge control for 4 to 10 NiCd or NiMH cells.

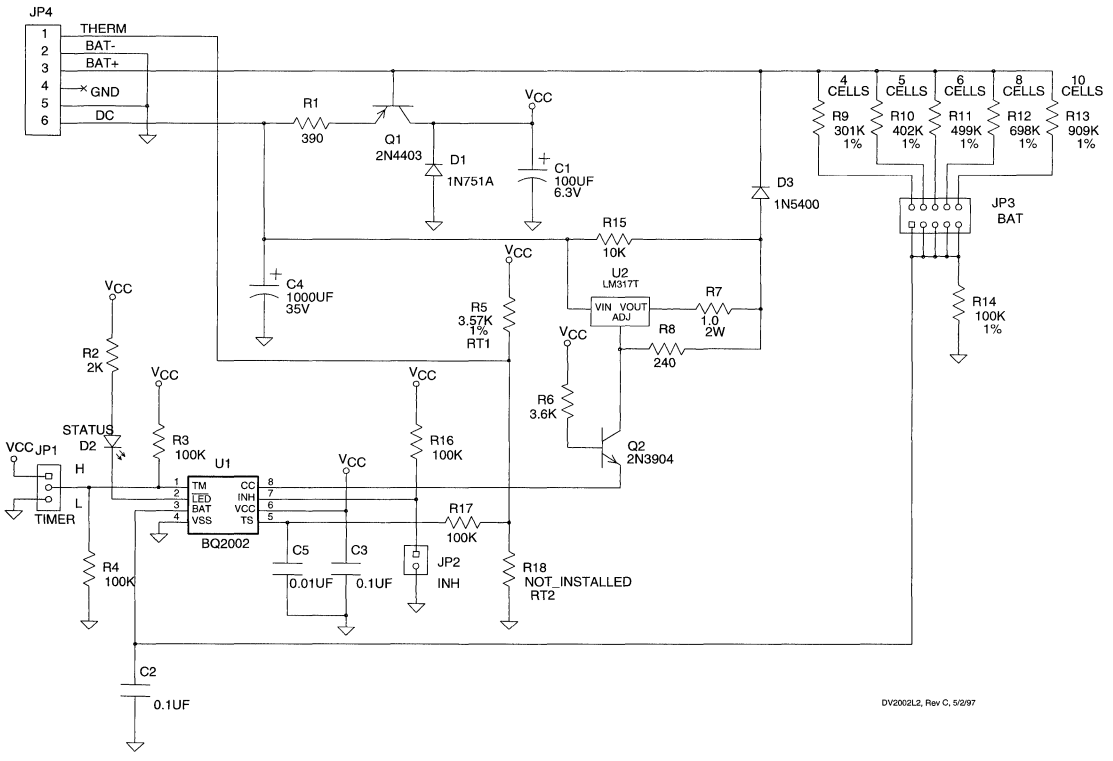
The fast charge is terminated by any of the following: ΔT/Δt, maximum temperature, maximum time, or an inhibit command for the bq2002T; or -ΔV/peak voltage, maximum temperature, maximum time, and inhibit command for the bq2002. Jumper settings select the top-off and maximum time limits.

The user provides a power supply and batteries. The user configures the DV2002L2/TL2 for the number of cells and maximum charge time (with or without top-off).

Please review the bq2002T or bq2002 data sheet before using the DV2002L2/TL2 board.

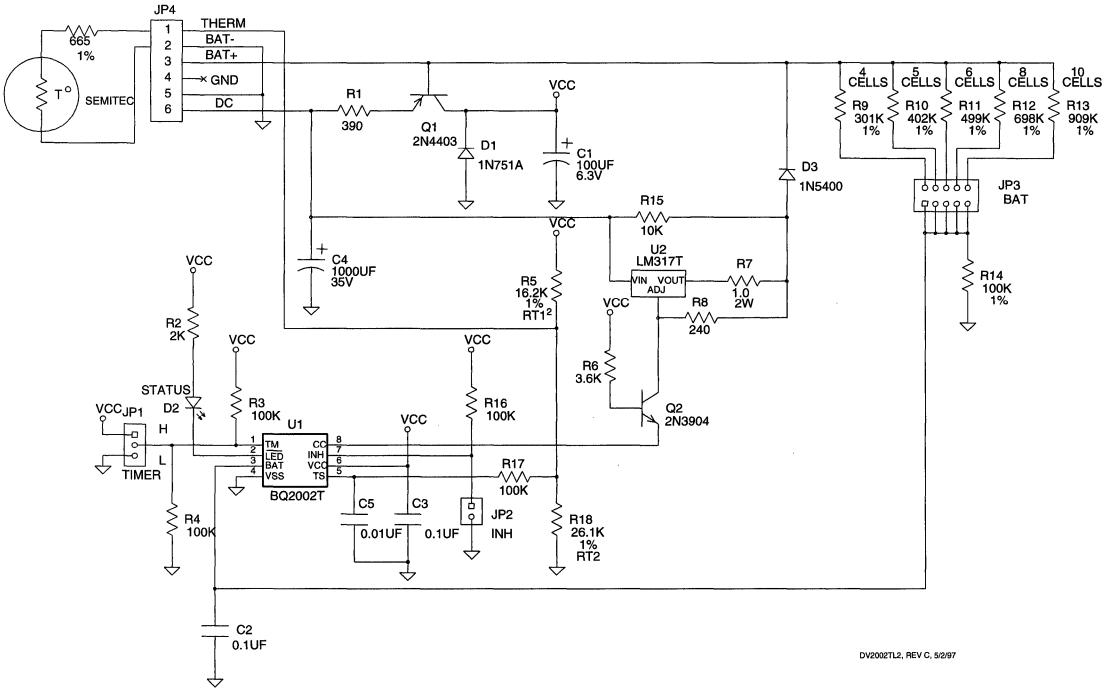
Full data sheets for these products are available from the Unitrode web site or from the factory

DV2002L2 Board Schematic



Rev. C Board

DV2002TL2 Board Schematic (Continued)



Rev. C Board

UNITRODE

bq2003

Fast-Charge IC

Features

- Fast charge and conditioning of nickel cadmium or nickel-metal hydride batteries
- Hysteretic PWM switch-mode current regulation or gated control of an external regulator
- Easily integrated into systems or used as a stand-alone charger
- Pre-charge qualification of temperature and voltage
- Direct LED outputs display battery and charge status
- Fast-charge termination by Δ temperature/Δ time, -ΔV, maximum voltage, maximum temperature, and maximum time
- Optional top-off charge

General Description

The bq2003 Fast Charge IC provides comprehensive fast charge control functions together with high-speed switching power control circuitry on a monolithic CMOS device.

Integration of closed-loop current control circuitry allows the bq2003 to be the basis of a cost-effective solution for stand-alone and system-integrated chargers for batteries of one or more cells.

Switch-activated discharge-before-charge allows bq2003-based chargers to support battery conditioning and capacity determination.

High-efficiency power conversion is accomplished using the bq2003 as a hysteretic PWM controller for switch-mode regulation of the charging current. The bq2003 may alternatively be used to gate an externally regulated charging current.

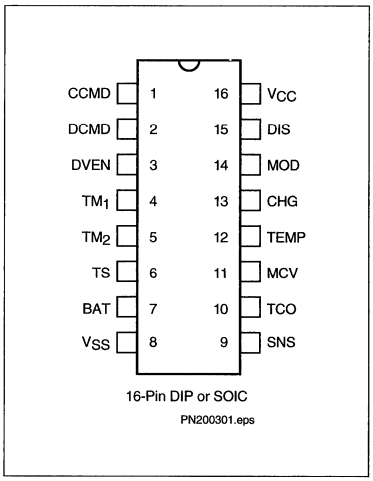
Fast charge may begin on application of the charging supply, replacement of the battery, or switch depression. For safety, fast charge is inhibited unless/until the battery temperature and voltage are within configured limits.

Temperature, voltage, and time are monitored throughout fast charge. Fast charge is terminated by any of the following:

- Rate of temperature rise (ΔT/Δt)
- Negative delta voltage (-ΔV)
- Maximum voltage
- Maximum temperature
- Maximum time

After fast charge, an optional top-off phase is available. Constant-current maintenence charge is provided by an external trickle resistor.

Pin Connections



16-Pin DIP or SOIC

PN200301.eps

Pin Names

CCMD	Charge command/select
DCMD	Discharge command
DVEN	-ΔV enable/disable
TM_1	Timer mode select 1
TM_2	Timer mode select 2
TS	Temperature sense
BAT	Battery voltage
V_{SS}	System ground
SNS	Sense resistor input
TCO	Temperature cutoff
MCV	Maximum voltage
TEMP	Temperature status output
CHG	Charging status output
MOD	Charge current control
DIS	Discharge control
V_{CC}	5.0V ±10% power

Pin Descriptions

CCMD, DCMD **Charge initiation and discharge-before-charge control inputs**

These two inputs control the conditions that begin a new charge cycle and enable discharge-before-charge. See Table 1.

DVEN **-ΔV enable input**

This input enales/disables -ΔV charge termination. If DVEN is high, the -ΔV test is enabled. If DVEN is low, -ΔV test is disabled. The state of DVEN may be changed at any time.

TM_1–TM_2 **Timer mode inputs**

TM_1 and TM_2 are three-state inputs that configure the fast charge safety timer, -ΔV hold-off time, and that enhance/disable top-off. See Table 2.

TS **Temperature sense input**

Input, referenced to SNS, for an external thermistor monitoring battery temperature.

BAT **Single-cell voltage input**

The battery voltage sense input, referenced to SNS. This is created by a high-impedance resistor divider network connected between the positive and the negative terminals of the battery.

Vss **Ground**

SNS **Charging current sense input**

SNS controls the switching of MOD based on the voltage across an external sense resistor in the current path of the battery. SNS is the reference potential for the TS and BAT pins. If SNS is connected to V_{SS}, MOD switches high at the beginning of charge and low at the end of charge.

TCO **Temperature cutoff threshold input**

Input to set maximum allowable battery temperature. If the potential between TS and SNS is less than the voltage at the TCO input, then fast charge or top-off charge is terminated.

MCV **Maximum-Cell-Voltage threshold input**

Input to set maximum single-cell equivalent voltage. If the voltage between BAT and SNS is greater than or equal to the voltage at the MCV input, then fast charge or top-off charge is inhibited.

Note: For valid device operation, the voltage level on MCV must not exceed 0.6 * V_{CC}.

TEMP **Temperature status output**

Push-pull output indicating temperature status. TEMP is low if the voltage at the TS pin is not within the allowed range to start fast charge.

CHG **Charging status output**

Push-pull output indicating charging status. See Figure 1.

MOD **Current-switching control output**

MOD is a push/pull output that is used to control the charging current to the battery. MOD switches high to enable charging current flow and low to inhibit charging current flow.

DIS **Discharge FET control output**

Push-pull output used to control an external transistor to discharge the battery before charging.

V_{CC} **V_{CC} supply input**

5.0 V, ±10% power input.

Functional Description

Figure 3 shows a state diagram and Figure 4 shows a block diagram of the bq2003.

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum allowable values. The voltage presented on the battery sense input, BAT, should represent a single-cell potential for the battery under charge. A resistor-divider ratio of:

$$\frac{RB1}{RB2} = N - 1$$

is recommended to maintain the battery voltage within the valid range, where N is the number of cells, RB1 is the resistor connected to the positive battery terminal, and RB2 is the resistor connected to the negative battery terminal. See Figure 1.

Note: This resistor-divider network input impedance to end-to-end should be at least 200kΩ and less than 1MΩ.

A ground-referenced negative temperature coefficient thermistor placed in proximity to the battery may be used as a low-cost temperature-to-voltage transducer. The temperature sense voltage input at TS is developed using a resistor-thermistor network between V_{CC} and V_{SS}. See Figure 1. Both the BAT and TS inputs are referenced to SNS, so the signals used inside the IC are:

$$V_{BAT} - V_{SNS} = V_{CELL}$$

and

$$V_{TS} - V_{SNS} = V_{TEMP}$$

Table 1. New Charge Cycle and Discharge Stimulus

CCMD Pulled Up/Down to:	DCMD Pulled Up/Down to:	New Charge Cycle Started by:	Discharge-Before-Charge Started by:
V_{SS}	V_{SS}	V_{CC} rising to valid level	A rising edge on DCMD
		Battery replacement (V_{CELL} falling through V_{MCV})	
		A rising edge on CCMD	
V_{CC}	V_{CC}	V_{CC} rising to valid level	A falling edge on DCMD
		Battery replacement (V_{CELL} falling through V_{MCV})	
		A falling edge on CCMD	
V_{CC}	V_{SS}	A rising edge on CCMD	A falling edge on DCMD
V_{SS}	V_{CC}	A falling edge on CCMD	A rising edge on DCMD

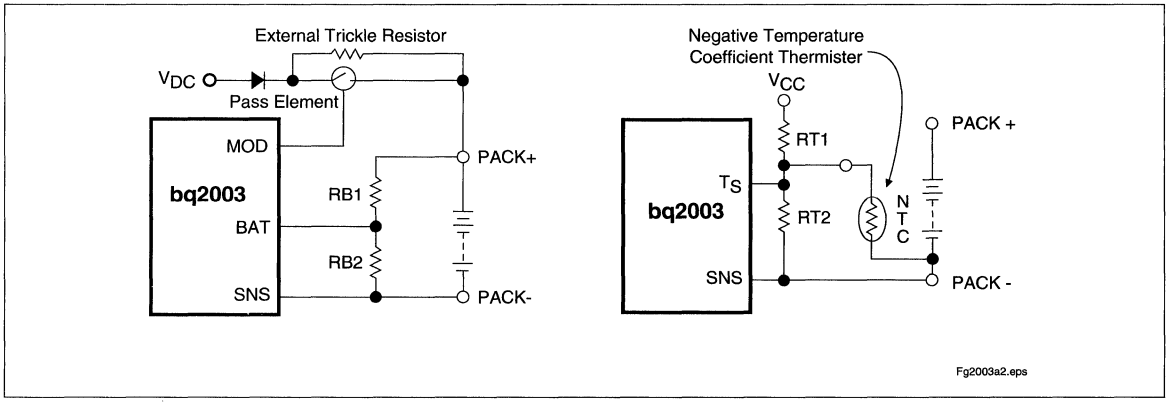


Figure 1. Voltage and Temperature Monitoring and Trickle Resistor

3/12

Discharge-Before-Charge

The DCMD input is used to command discharge-before-charge via the DIS output. Once activated, DIS becomes active (high) until V_{CELL} falls below V_{EDV}, at which time DIS goes low and a new fast charge cycle begins. See Table 1 for the conditions that initiate discharge-before-charge. Discharge-before-charge is qualified by the same voltage and temperature conditions that qualify a new charge cycle start (see below). If a discharge is initiated but the pack voltage or temperature is out of range, the chip enters the charge pending mode and trickle charges the battery until the voltage and temperature qualification conditions are met, and then starts to discharge.

Starting A Charge Cycle

The stimulus required to start a new charge cycle is determined by the configuration of the CCMD and DCMD inputs. If CCMD and DCMD are both pulled up or pulled down, then a new charge cycle is started by (see Figure 2):

1. V_{CC} rising above 4.5V
2. V_{CELL} falling through the maximum cell voltage, V_{MCV}. V_{MCV} is the voltage presented at the MCV input pin, and is configured by the user with a resistor divider between V_{CC} and ground. The allowed range is 0.2 to 0.4 * V_{CC}.
3. A rising edge on CCMD of it is pulled down, or a falling edge on CCMD if it is pulled up.

Starting a new charge cycle may be limited to a push-button or logical pulse input only by pulling one member of the DCMD and CCMD pair up while pulling the other input down. In this configuration a new charge cycle will be started only by a falling edge on CCMD if it is pulled up, and by a falling edge on CCMD if it is pulled down. See Table 1.

If the battery is within the configured temperature and voltage limits, the IC begins fast charge. The valid battery voltage range is $V_{EDV} < V_{BAT} < V_{MCV}$ where:

$$V_{EDV} = 0.2 * V_{CC} \pm 30mV$$

The valid temperature range is $V_{HTF} < V_{TEMP} < V_{LTF}$, where:

$$V_{LTF} = 0.4 * V_{CC} \pm 30mV$$

$$V_{HTF} = [(1/8 * V_{LTF}) + (7/8 * V_{TCO})] \pm 30mV$$

V_{TCO} is the voltage presented at the TCO input pin, and is configured by the user with a resistor divider between V_{CC} and ground. The allowed range is 0.2 to 0.4 * V_{CC}.

If the temperature of the battery is out of range, or the voltage is too low, the chip enters the charge pending state and waits for both conditions to fall within their allowed limits. There is no time limit on the charge pending state; the charger remains in this state as long as the voltage or temperature conditons are outside of

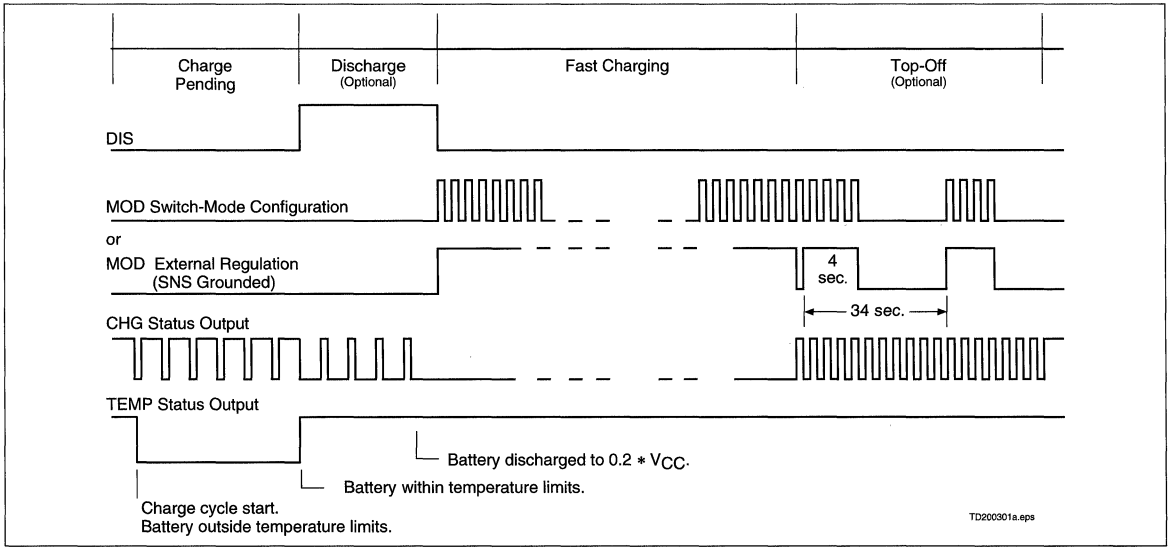


Figure 2. Charge Cycle Phases

Table 2. Fast-Charge Safety Time/Hold-Off/Top-Off Table

Corresponding Fast-Charge Rate	TM1	TM2	Typical Fast Charge and Top-Off Time Limits	Typical -ΔV/MCV Hold-Off Time (seconds)	Top-Off Rate
C/4	Low	Low	360	137	Disabled
C/2	Float	Low	180	820	Disabled
1C	High	Low	90	410	Disabled
2C	Low	Float	45	200	Disabled
4C	Float	Float	23	100	Disabled
C/2	High	Float	180	820	C/16
1C	Low	High	90	410	C/8
2C	Float	High	45	200	C/4
4C	High	High	23	100	C/2

Note: Typical conditions = 25°C, V_{CC} = 5.0V.

the allowed limits. If the voltage is too high, the chip goes to the battery absent state and waits until a new charge cycle is started.

Fast charge continues until termination by one or more of the five possible termination conditions:

- Delta temperature/delta time (ΔT/Δt)
- Negative delta voltage (-ΔV)
- Maximum voltage
- Maximum temperature
- Maximum time

-ΔV Termination

If the DVEN input is high, the bq2003 samples the voltage at the BAT pin once every 34s. If V_{CELL} is lower than any previously measured value by 12mV ±4mV, fast charge is terminated. The -ΔV test is valid in the range V_{MCV} - (0.2 * V_{CC}) < V_{CELL} < V_{MCV}.

Voltage Sampling

Each sample is an average of 16 voltage measurements taken 57µs apart. The resulting sample period (18.18ms) filters out harmonics around 55Hz. This technique minimizes the effect of any AC line ripple that may feed through the power supply from either 50Hz or 60Hz AC sources. Tolerance on all timing is ±16%.

Voltage Termination Hold-off

A hold-off period occurs at the start of fast charging. During the hold-off period, -ΔV termination is disabled. This avoids premature termination on the voltage spikes sometimes produced by older batteries when fast-charge current is first applied. ΔT/Δt, maximum voltage and maximum temperature terminations are not affected by the hold-off period.

ΔT/Δt Termination

The bq2003 samples at the voltage at the TS pin every 34s, and compares it to the value measured two samples earlier. If V_{TEMP} has fallen 16mV ±4mV or more, fast charge is terminated. The ΔT/Δt termination test is valid only when V_{TCO} < V_{TEMP} < V_{LTF}.

Temperature Sampling

Each sample is an average of 16 voltage measurements taken 57µs apart. The resulting sample period (18.18ms) filters out harmonics around 55Hz. This technique minimizes the effect of any AC line ripple that may feed through the power supply from either 50Hz or 60Hz AC sources. Tolerance on all timing is ±16%.

Maximum Voltage, Temperature, and Time

Anytime V_{CELL} rises above V_{MCV}, CHG goes high (the LED goes off) immediately. If the bq2003 is not in the voltage hold-off period, fast charging also ceases immediately. If V_{CELL} then falls back below V_{MCV} before t_{MCV} = 250ms ±50ms, the chip transitions to the Charge Complete state (maximum voltage termination). If V_{CELL} remains above V_{MCV} at the expiration of t_{MCV}, the bq2003 transitions to the Battery Absent state (battery removal). See Figure 3.

If the bq2003 is in the voltage hold-off period when V_{CELL} rises above V_{MCV}, the LED goes out but fast charging continues until the expiration of the hold-off period. Temperature sampling continues until the end of the hold-off period as well. If a new battery is inserted before the hold-off period expires, it continues in the fast charge cycle started by its predecessor. No precharge qualification is performed, and a temperature sample taken on the new battery is compared to ones

taken before the original battery was removed and any that may have been taken while no battery was present. If the IC is configured for $\Delta T/\Delta t$ termination, this may result in a premature fast-charge termination on the newly inserted battery.

Maximum temperature termination occurs anytime the voltage on the TS pin falls below the temperature cut-off threshold V_{TCO}. Charge is also terminated if V_{TEMP} rises above the minimum temperature fault threshold, V_{LTF}, after fast charge begins.

Maximum charge time is configured using the TM pin. Time settings are available for corresponding charge rates of C/4, C/2, 1C, and 2C. Maximum time-out termination is enforced on the fast-charge phase, then reset, and enforced again on the top-off phase, if selected. There is no time limit on the trickle-charge phase.

Top-off Charge

An optional top-off charge phase may be selected to follow fast charge termination for the C/2 through 4C rates. This phase may be necessary on NiMH or other battery chemistries that have a tendency to terminate charge prior to reaching full capacity. With top-off enabled, charging continues at a reduced rate after fast-charge termination for a period of time selected by the TM_1 and TM_2 input pins. (See Table 2.) During top-off, the MOD pin is enabled at a duty cycle of 4s active for every 30s inactive. This modulation results in an average rate 1/8th that of the fast charge rate. Maximum voltage, time, and temperature are the only termination methods enabled during top-off.

External Trickle Resistor

Maintenance charging is provided by the use of an external trickle resistor between the high side of the battery pack and V_{DC}, the input charging supply voltage. (See Figure 2.) This resistor is sized to meet two criteria.

- With the battery removed, the resistor must pull the voltage at the BAT input above MCV for battery insertion and removal detection.
- With the battery at its fully charged voltage, the trickle current should be approximately equal to the self-discharge rate of the battery.

Charge Status Indication

Charge status is indicated by the CHG output. The state of the CHG output in the various charge cycle phases is shown in Figure 3 and illustrated in Figure 1.

Temperature status is indicated by the TEMP output. TEMP is in the high state whenever V_{TEMP} is within the temperature window defined by the V_{LTF} and V_{HTF} temperature limits, and is low when the battery temperature is outside these limits.

In all cases, if V_{CELL} exceeds the voltage at the MCV pin, both CHG and TEMP outputs are held high regardless of other conditions. CHG and TEMP may both be used to directly drive an LED.

Charge Current Control

The bq2003 controls charge current through the MOD output pin. The current control circuitry is designed to support implementation of a constant-current switching regulator or to gate an externally regulated current source.

When used in switch-mode configuration, the nominal regulated current is:

$$I_{REG} = 0.235V/R_{SNS}$$

Charge current is monitored at the SNS input by the voltage drop across a sense resistor, R_{SNS}, between the low side of the battery pack and ground. R_{SNS} is sized to provide the desired fast-charge current.

If the voltage at the SNS pin is less than V_{SNSLO}, the MOD output is switched high to pass charge current to the battery.

When the SNS voltage is greater than V_{SNSHI}, the MOD output is switched low—shutting off charging current to the battery.

$$V_{SNSLO} = 0.044 * V_{CC} \pm 25mV$$

$$V_{SNSHI} = 0.05 * V_{CC} \pm 25mV$$

When used to gate an externally regulated current source, the SNS pin is connected to V_{SS}, and no sense resisitor is required.

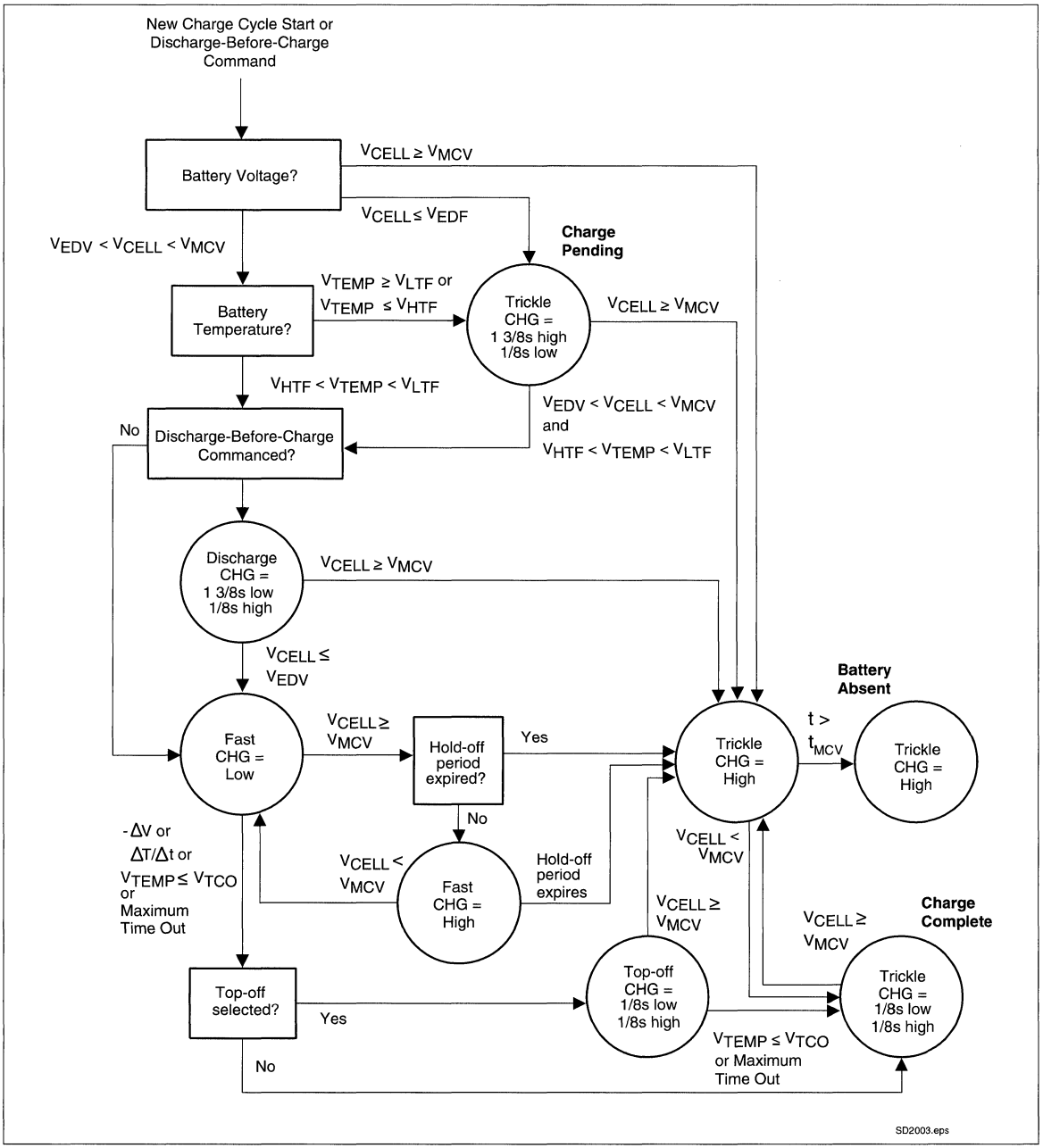


Figure 3. State Diagram

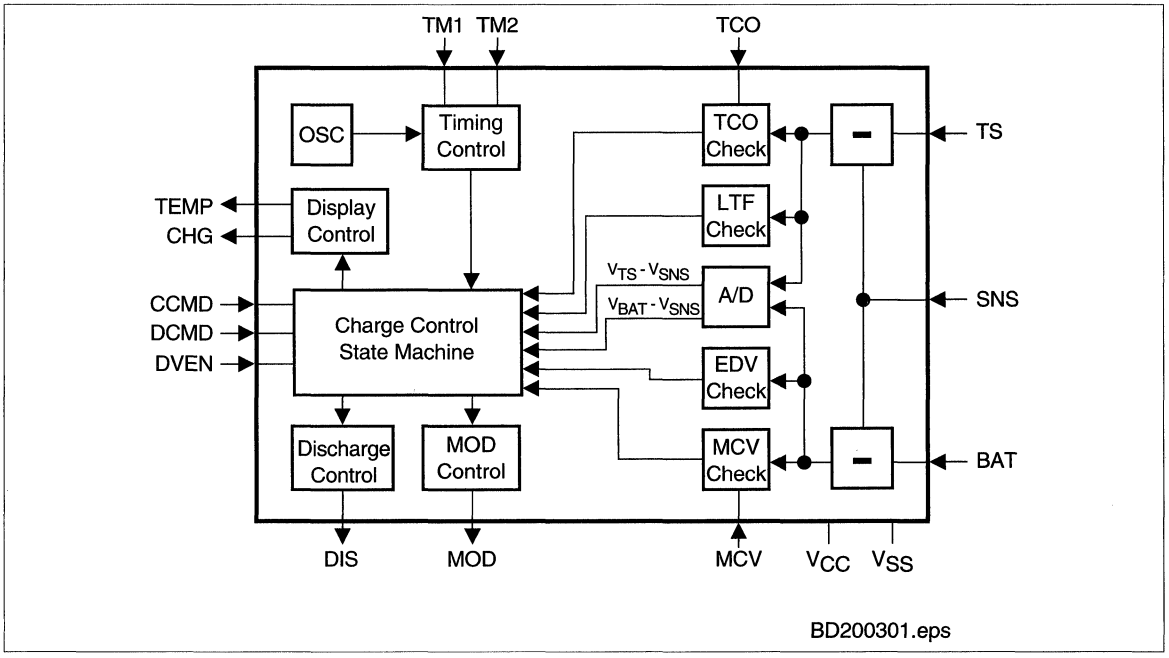


Figure 4. Block Diagram

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	0	+70	°C	Commercial
T_{STG}	Storage temperature	-55	+125	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10 sec max.
T_{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds ($T_A = T_{OPR}$; V_{CC} ±10%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{SNSHI}	High threshold at SNS resulting in MOD = Low	0.05 * V_{CC}	±0.025	V	Tolerance is common mode deviation.
V_{SNSLO}	Low threshold at SNS resulting in MOD = High	0.044 * V_{CC}	±0.025	V	Tolerance is common mode deviation.
V_{LTF}	Low-temperature fault	0.4 * V_{CC}	±0.030	V	$V_{TEMP} \geq V_{LTF}$ inhibits/ terminates charge
V_{HTF}	High-temperature fault	(1/8 * V_{LTF}) + (7/8 * V_{TCO})	±0.030	V	$V_{TEMP} \leq V_{HTF}$ inhibits fast charge
V_{EDV}	End-of-discharge voltage	0.2 * V_{CC}	±0.030	V	$V_{CELL} < V_{EDV}$ inhibits fast charge
V_{THERM}	TS input change for $\Delta T/\Delta t$ detection	-16	±4	mV	V_{CC} = 5V, T_A = 25°C
$-\Delta V$	BAT input change for $-\Delta V$ detection	-12	±4	mV	V_{CC} = 5V, T_A = 25°C

Recommended DC Operating Conditions (T_A = 0 to +70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{BAT}	Battery input	0	-	V_{CC}	V	
V_{CELL}	BAT voltage potential	0	-	V_{CC}	V	V_{BAT} - V_{SNS}
V_{TS}	Thermistor input	0	-	V_{CC}	V	
V_{TEMP}	TS voltage potential	0	-	V_{CC}	V	V_{TS} - V_{SNS}
V_{MCV}	Maximum cell voltage	0.2 * V_{CC}	-	0.4 * V_{CC}	V	
V_{TCO}	Temperature cutoff	0.2 * V_{CC}	-	0.4 * V_{CC}	V	
V_{IH}	Logic input high	V_{CC} - 1.0	-	-	V	CCMD, DCMD, DVEN
	Logic input high	V_{CC} - 0.3	-	-	V	TM_1, TM_2
V_{IL}	Logic input low	-	-	1.0	V	CCMD, DCMD, DVEN
	Logic input low	-	-	0.3	V	TM_1, TM_2
V_{OH}	Logic output high	V_{CC} - 0.5	-	-	V	DIS, TEMP, CHG, MOD, $I_{OH} \leq$ -5mA
V_{OL}	Logic output low	-	-	0.5	V	DIS, TEMP, CHG, MOD, $I_{OL} \leq$ 5mA
I_{CC}	Supply current	-	0.75	2.2	mA	Outputs unloaded
I_{OH}	DIS, TEMP, MOD, CHG source	-5.0	-	-	mA	@V_{OH} = V_{CC} - 0.5V
I_{OL}	DIS, TEMP, MOD, CHG sink	5.0	-	-	mA	@V_{OL} = V_{SS} + 0.5V
I_{IL}	Input leakage	-	-	±1	µA	CCMD, DCMD, DVEN, V = V_{SS} to V_{CC}
	Logic input low source	-	-	70	µA	TM_1, TM_2, V = V_{SS} to V_{SS} + 0.3V
I_{IH}	Logic input high source	-70	-	-	µA	TM_1, TM_2, V = V_{CC} - 0.3V to V_{CC}
I_{IZ}	TM_1, TM_2 tri-state open detection	-2.0	-	2.0	µA	TM_1, TM_2 may be left disconnected (floating) for Z logic input state

Note: All voltages relative to V_{SS} except as noted.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
R_{BAT}	Battery input impedance	50	-	-	MΩ
R_{MCV}	MCV input impedance	50	-	-	MΩ
R_{TCO}	TCO input impedance	50	-	-	MΩ
R_{SNS}	SNS input impedance	50	-	-	MΩ
R_{TS}	TS input impedance	50	-	-	MΩ

Timing (T_A = 0 to +70°C; V_{CC} ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{PW}	Pulse width for CCMD, DCMD pulse commands	1	-	-	µs	Pulse start for charge or discharge-before-charge
d_{FCV}	Time base variation	-16	-	16	%	V_{CC} = 4.5V to 5.5V
f_{REG}	MOD output regulation frequency	-	-	300	kHz	
t_{MCV}	Maximum voltage termination time limit	200	250	300	ms	Time limit to distinguish battery removed from charge complete

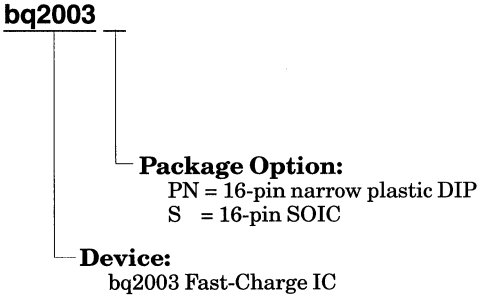
Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
5	2	Changed block diagram	Changed diagram.
5	8	Added top-off values to Table 2.	Added values.
6	All	Revised and expanded format of this data sheet	Clarification
7	9	T_{OPR}	Deleted industrial temperature range.

Notes: Changes 1–4: Please refer to the *1997 Data Book*.
Change 5 = Sept. 1996 F changes from Oct. 1993 E.
Change 6 = Oct. 1997 G changes from Sept. 1996 F.
Change 7 = June 1999 H changes from Oct. 1997 G.

Ordering Information



UNITRODE

Product Brief **DV2003L1**

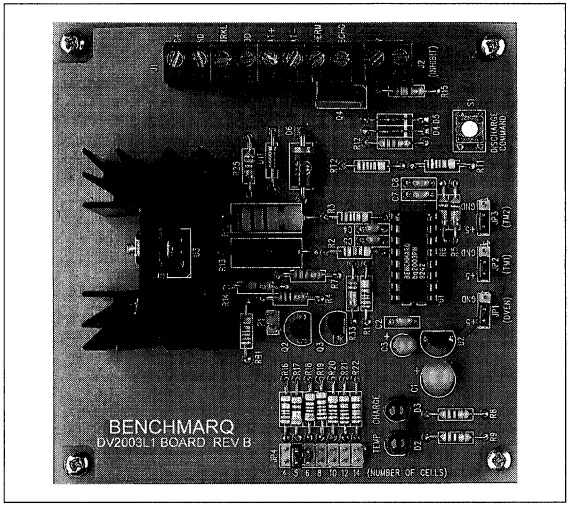
Fast-Charge Development System

Control of On-Board Linear Current Regulator or External Current Source

3

Features

- bq2003 fast-charge control evaluation and development
- Charge current sourced from an on-board linear regulator (1.25A, modifiable for 0.1 to 1.5 A) or an external current source
- Fast charge of 4 to 14 NiCd or NiMH cells
- Fast-charge termination by $\Delta T/\Delta t$, $-\Delta V$, maximum temperature, time, and voltage
- $-\Delta V$ enable, hold-off, top-off, maximum time, number of cells, and off-board current source control are jumper-configurable
- Charging status displayed on charge and temperature LEDs
- Discharge-before-charge control with push-button switch
- Inhibit fast charge by external logic-level input



General Description

The DV2003L1 Development System provides a development environment for the bq2003 Fast-Charge IC. The DV2003L1 incorporates a bq2003 and an LM317 linear regulator to provide fast charge control for 4 to 14 NiCd or NiMH cells. The DV2003L1 also supports on/off control of an external current source.

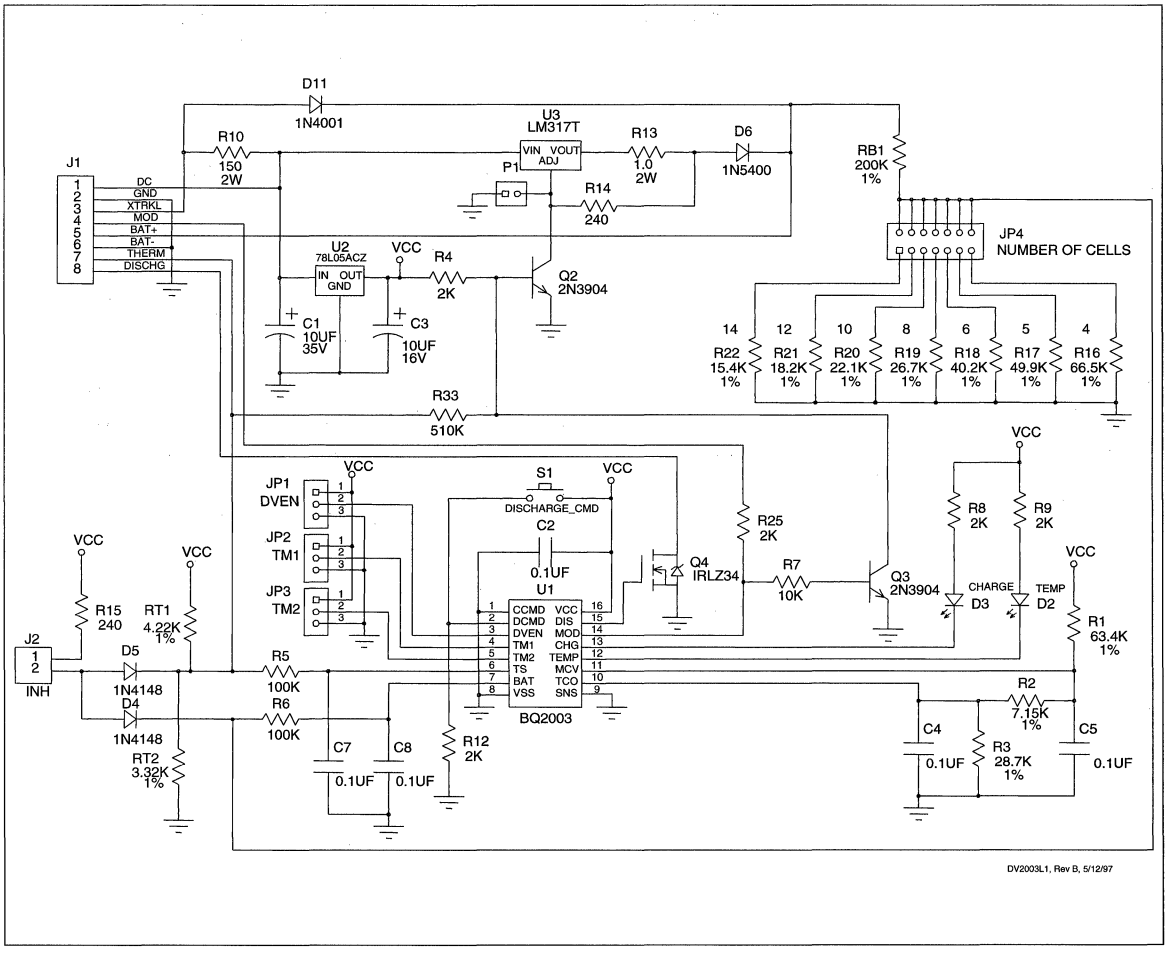
The fast charge is terminated by any of the following: $\Delta T/\Delta t$, $-\Delta V$, maximum temperature, maximum time, maximum voltage, or an external inhibit command.

Jumper settings select the $-\Delta V$ enabled state, the hold-off, top-off, and maximum time limits, and enable the use of an external current source.

The user provides a power supply and batteries. If the on-board 1.25A linear regulator is disabled, the external current source must have an appropriate digitally controlled switch (active high). The user configures the DV2003L1 for the number of cells, charge termination, maximum charge time (with or without top-off), and commands the discharge-before-charge option with the push-button switch S1.

A full data sheet for this product is available on the Unitrode web site, or you may contact the factory for one.

DV2003L1 Board Schematic



Rev. B Board

UNITRODE

Product Brief **DV2003S1**

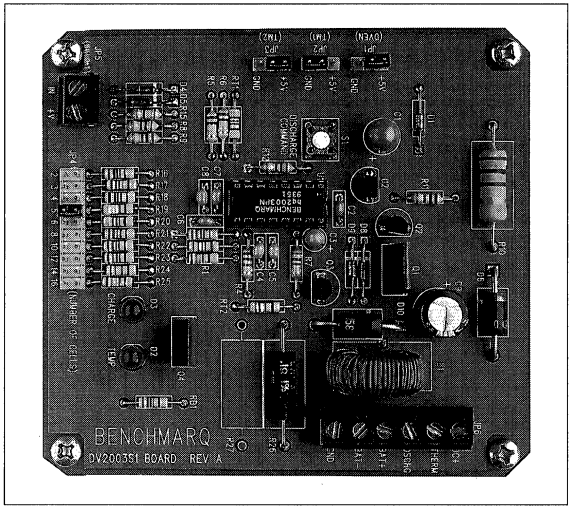
Fast-Charge Development System

Control of On-Board P-FET Switch-Mode Regulator

3

Features

- bq2003 fast-charge control evaluation and development
- Charge current sourced from an on-board switch-mode regulator (up to 3.0 A)
- Fast charge of 2 to 16 NiCd or NiMH cells
- Fast-charge termination by delta temperature/delta time ($\Delta T/\Delta t$), negative delta voltage ($-\Delta V$), maximum temperature, maximum time, and maximum voltage
- $-\Delta V$ enable, hold-off, top-off, maximum time, and number of cells are jumper-configurable
- Charging status displayed on charge and temperature LEDs
- Discharge-before-charge control with push-button switch
- Inhibit fast charge by external logic-level input



General Description

The DV2003S1 Development System provides a development environment for the bq2003 Fast-Charge IC. The DV2003S1 incorporates a bq2003 and a buck-type switch-mode regulator to provide fast charge control for 2 to 16 NiCd or NiMH cells.

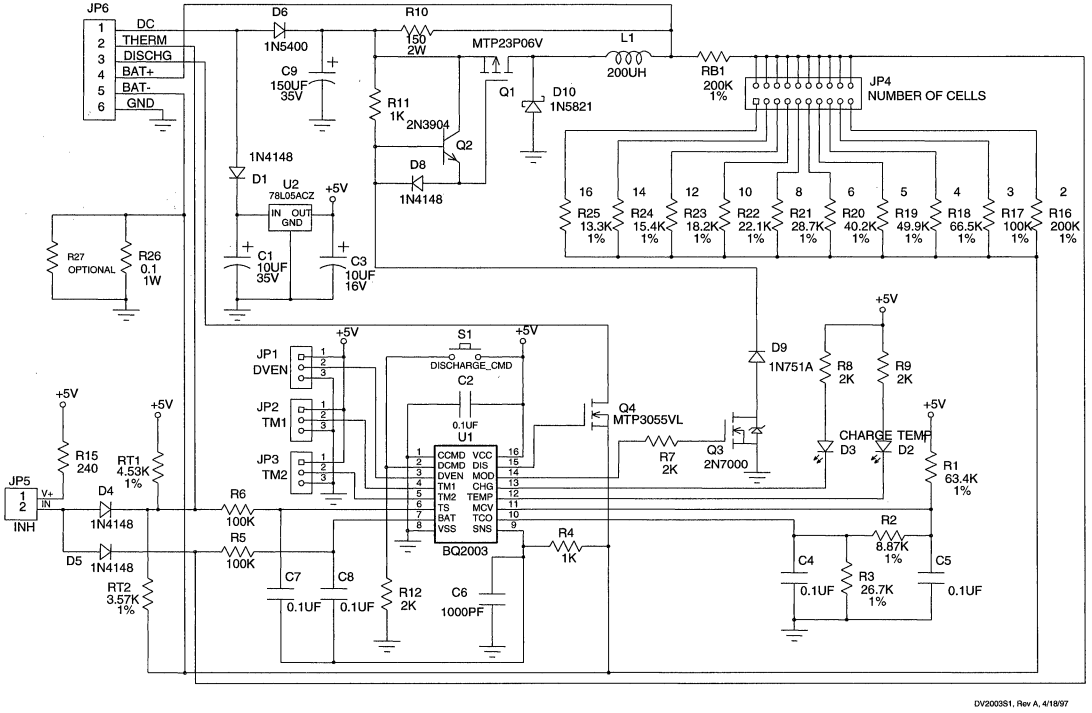
Review the bq2003 data sheet and the application note, "Using the bq2003 to Control Fast Charge," before using the DV2003S1 board.

The fast charge is terminated by any of the following: $\Delta T/\Delta t$, $-\Delta V$, maximum temperature, maximum time, maximum voltage, or an external inhibit command. Jumper settings select the $-\Delta V$ enabled state, and the hold-off, top-off, and maximum time limits.

The user provides a power supply and batteries. The user configures the DV2003S1 for the number of cells, $-\Delta V$ charge termination and maximum charge time (with or without top-off), and commands the discharge-before-charge option with the push-button switch S1.

A full data sheet of this product is available on the Unitrode web site, or you may contact the factory for one.

DV2003S1 Board Schematic



Rev. A Board

UNITRODE

Product Brief **DV2003S2**

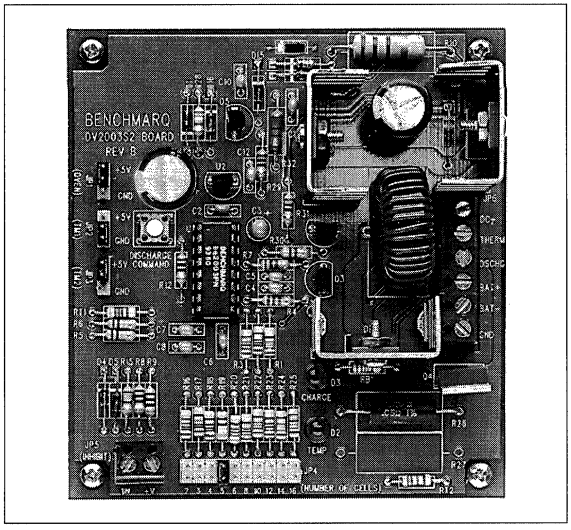
Fast-Charge Development System

Control of On-Board N-FET Switch-Mode Regulator

3

Features

- bq2003 fast-charge control evaluation and development
- Charge current sourced from an on-board switch-mode regulator (up to 6.0 A)
- Fast charge of 2 to 16 NiCd or NiMH cells
- Fast-charge termination by delta temperature/delta time ($\Delta T/\Delta t$), negative delta voltage ($-\Delta V$), maximum temperature, maximum time, and maximum voltage
- $-\Delta V$ enable, hold-off, top-off, maximum time, and number of cells are jumper-configurable
- Charging status displayed on charge and temperature LEDs
- Discharge-before-charge control with push-button switch
- Inhibit fast charge by external logic-level input



General Description

The DV2003S2 Development System provides a development environment for the bq2003 Fast-Charge IC. The DV2003S2 incorporates a bq2003 and an n-FET buck-type switch-mode regulator to provide fast charge control for 2 to 16 NiCd or NiMH cells. The primary difference between the DV2003S2 and the DV2003S1 is in the switching FET Q1. The DV2003S1 uses a p-FET for battery charge currents of 3.0A or less, whereas the DV2003S2 uses an n-FET to support charge currents up to 6.0A.

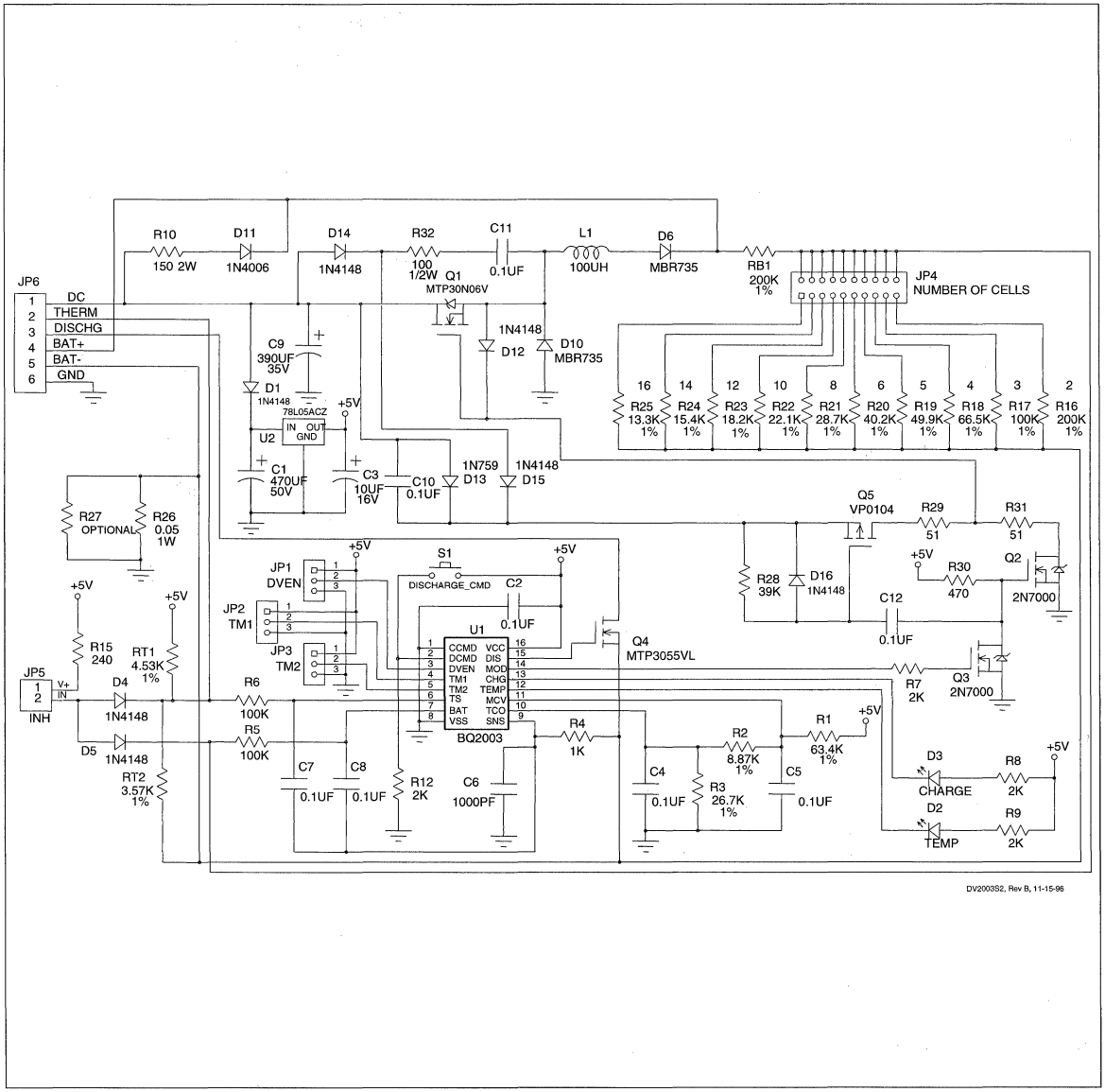
Review the bq2003 data sheet and the application note, "Using the bq2003 to Control Fast Charge," before using the DV2003S2 board. Also review the application note, "Step-Down Switching Current Regulation Using the bq2003," for information concerning trade-offs between using P-FET and N-FET transistors for Q1.

The fast charge is terminated by any of the following: $\Delta T/\Delta t$, $-\Delta V$, maximum temperature, maximum time, maximum voltage, or an external inhibit command. Jumper settings select the $-\Delta V$ enabled state, and the hold-off, top-off, and maximum time limits.

The user provides a power supply and batteries. The user configures the DV2003S2 for the number of cells, $-\Delta V$ charge termination, and maximum charge time (with or without top-off), and commands the discharge-before-charge option with the push-button switch S1.

A full data sheet for this product is available on the Unitrode web site, or you may contact the factory for one.

DV2003S2 Board Schematic



Rev B Board

UNITRODE

bq2004

Fast-Charge IC

3

Features

- ➤ Fast charge and conditioning of nickel cadmium or nickel-metal hydride batteries
- ➤ Hysteretic PWM switch-mode current regulation or gated control of an external regulator
- ➤ Easily integrated into systems or used as a stand-alone charger
- ➤ Pre-charge qualification of temperature and voltage
- ➤ Configurable, direct LED outputs display battery and charge status
- ➤ Fast-charge termination by Δ temperature/Δ time, peak volume detection, -ΔV, maximum voltage, maximum temperature, and maximum time
- ➤ Optional top-off charge and pulsed current maintenance charging
- ➤ Logic-level controlled low-power mode (< 5μA standby current)

General Description

The bq2004 Fast Charge IC provides comprehensive fast charge control functions together with high-speed switching power control circuitry on a monolithic CMOS device.

Integration of closed-loop current control circuitry allows the bq2004 to be the basis of a cost-effective solution for stand-alone and system-integrated chargers for batteries of one or more cells.

Switch-activated discharge-before-charge allows bq2004-based chargers to support battery conditioning and capacity determination.

High-efficiency power conversion is accomplished using the bq2004 as a hysteretic PWM controller for switch-mode regulation of the charging current. The bq2004 may alternatively be used to gate an externally regulated charging current.

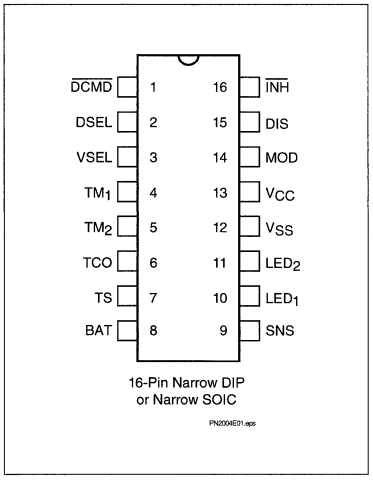
Fast charge may begin on application of the charging supply, replacement of the battery, or switch depression. For safety, fast charge is inhibited unless/until the battery temperature and voltage are within configured limits.

Temperature, voltage, and time are monitored throughout fast charge. Fast charge is terminated by any of the following:

- Rate of temperature time (ΔT/Δt)
- Peak voltage detection (PVD)
- Negative delta voltage (-ΔV)
- Maximum voltage
- Maximum temperature
- Maximum time

After fast charge, optional top-off and pulsed current maintenance phases are available.

Pin Connections



16-Pin Narrow DIP
or Narrow SOIC

Pin Names

$\overline{DCMD}$	Discharge command
DSEL	Display select
VSEL	Voltage termination select
TM_1	Timer mode select 1
TM_2	Timer mode select 2
TCO	Temperature cutoff
TS	Temperature sense
BAT	Battery voltage
SNS	Sense resistor input
LED_1	Charge status output 1
LED_2	Charge status output 2
V_{SS}	System ground
V_{CC}	5.0V ±10% power
MOD	Charge current control
DIS	Discharge control output
$\overline{INH}$	Charge inhibit input

Pin Descriptions

$\overline{DCMD}$ **Discharge-before-charge control input**

The $\overline{DCMD}$ input controls the conditions that enable discharge-before-charge. $\overline{DCMD}$ is pulled up internally. A negative-going pulse on $\overline{DCMD}$ initiates a discharge to end-of-discharge voltage (EDV) on the BAT pin, followed by a new charge cycle start. Tying $\overline{DCMD}$ to ground enables automatic discharge-before-charge on every new charge cycle start.

DSEL **Display select input**

This three-state input configures the charge status display mode of the LED_1 and LED_2 outputs. See Table 2.

VSEL **Voltage termination select input**

This three-state input controls the voltage-termination technique used by the bq2004. When high, PVD is active. When floating, -ΔV is used. When pulled low, both PVD and -ΔV are disabled.

TM_1–TM_2 **Timer mode inputs**

TM_1 and TM_2 are three-state inputs that configure the fast charge safety timer, voltage termination hold-off time, "top-off", and trickle charge control. See Table 1.

TCO **Temperature cut-off threshold input**

Input to set maximum allowable battery temperature. If the potential between TS and SNS is less than the voltage at the TCO input, then fast charge or top-off charge is terminated.

TS **Temperature sense input**

Input, referenced to SNS, for an external thermister monitoring battery temperature.

BAT **Battery voltage input**

BAT is the battery voltage sense input, referenced to SNS. This is created by a high-impedance resistor-divider network connected between the positive and the negative terminals of the battery.

SNS **Charging current sense input**

SNS controls the switching of MOD based on an external sense resistor in the current path of the battery. SNS is the reference potential for both the TS and BAT pins. If SNS is connected to V_{SS}, then MOD switches high at the beginning of charge and low at the end of charge.

LED_1–LED_2 **Charge status outputs**

Push-pull outputs indicating charging status. See Table 2.

V_{SS} **Ground**

V_{CC} **V_{CC} supply input**

5.0V, ±10% power input.

MOD **Charge current control output**

MOD is a push-pull output that is used to control the charging current to the battery. MOD switches high to enable charging current to flow and low to inhibit charging current flow.

DIS **Discharge control output**

Push-pull output used to control an external transistor to discharge the battery before charging.

$\overline{INH}$ **Charge inhibit input**

When low, the bq2004 suspends all charge actions, drives all outputs to high impedance, and assumes a low-power operational state. When transitioning from low to high, a new charge cycle is started.

Functional Description

Figure 3 shows a block diagram and Figure 4 shows a state diagram of the bq2004.

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum allowable values. The voltage presented on the battery sense input, BAT, should represent a two-cell potential for the battery under charge. A resistor-divider ratio of:

$$\frac{RB1}{RB2} = \frac{N}{2} - 1$$

is recommended to maintain the battery voltage within the valid range, where N is the number of cells, RB1 is the resistor connected to the positive battery terminal, and RB2 is the resistor connected to the negative battery terminal. See Figure 1.

Note: This resistor-divider network input impedance to end-to-end should be at least 200kΩ and less than 1MΩ.

A ground-referenced negative temperature coefficient thermistor placed in proximity to the battery may be used as a low-cost temperature-to-voltage transducer. The temperature sense voltage input at TS is developed using a resistor-thermistor network between V_{CC} and V_{SS}. See Figure 1. Both the BAT and TS inputs are referenced to SNS, so the signals used inside the IC are:

$$V_{BAT} - V_{SNS} = V_{CELL}$$

and

$$V_{TS} - V_{SNS} = V_{TEMP}$$

Discharge-Before-Charge

The $\overline{DCMD}$ input is used to command discharge-before-charge via the DIS output. Once activated, DIS becomes active (high) until V_{CELL} falls below V_{EDV}, at which time DIS goes low and a new fast charge cycle begins.

The $\overline{DCMD}$ input is internally pulled up to V_{CC} (its inactive state). Leaving the input unconnected, therefore, results in disabling discharge-before-charge. A negative going pulse on $\overline{DCMD}$ initiates discharge-before-charge at any time regardless of the current state of the bq2004. If $\overline{DCMD}$ is tied to V_{SS}, discharge-before-charge will be the first step in all newly started charge cycles.

Starting a Charge Cycle

A new charge cycle (see Figure 2) is started by:

1. V_{CC} rising above 4.5V
2. V_{CELL} falling through the maximum cell voltage, V_{MCV} where:

$$V_{MCV} = 0.8 * V_{CC} \pm 30mV$$

3. A transition on the $\overline{INH}$ input from low to high.

If $\overline{DCMD}$ is tied low, a discharge-before-charge is executed as the first step of the new charge cycle. Otherwise, pre-charge qualification testing is the first step.

The battery must be within the configured temperature and voltage limits before fast charging begins.

The valid battery voltage range is $V_{EDV} < V_{BAT} < V_{MCV}$ where:

$$V_{EDV} = 0.4 * V_{CC} \pm 30mV$$

The valid temperature range is $V_{HTF} < V_{TEMP} < V_{LTF}$, where:

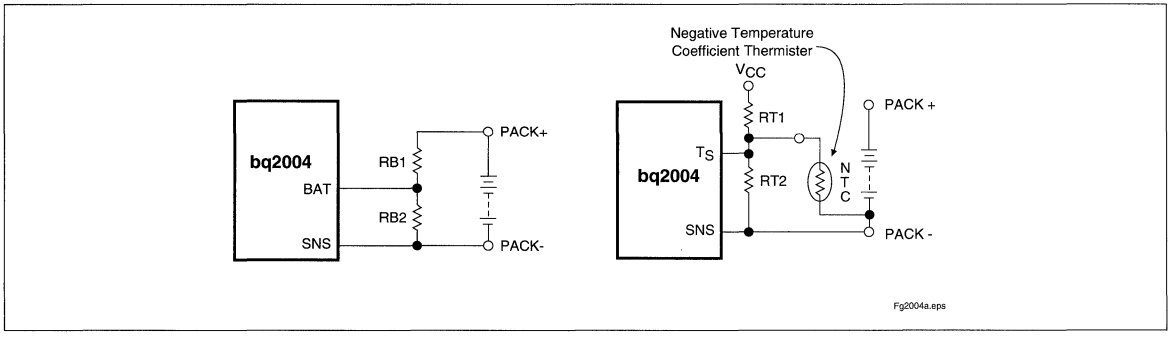


Figure 1. Voltage and Temperature Monitoring

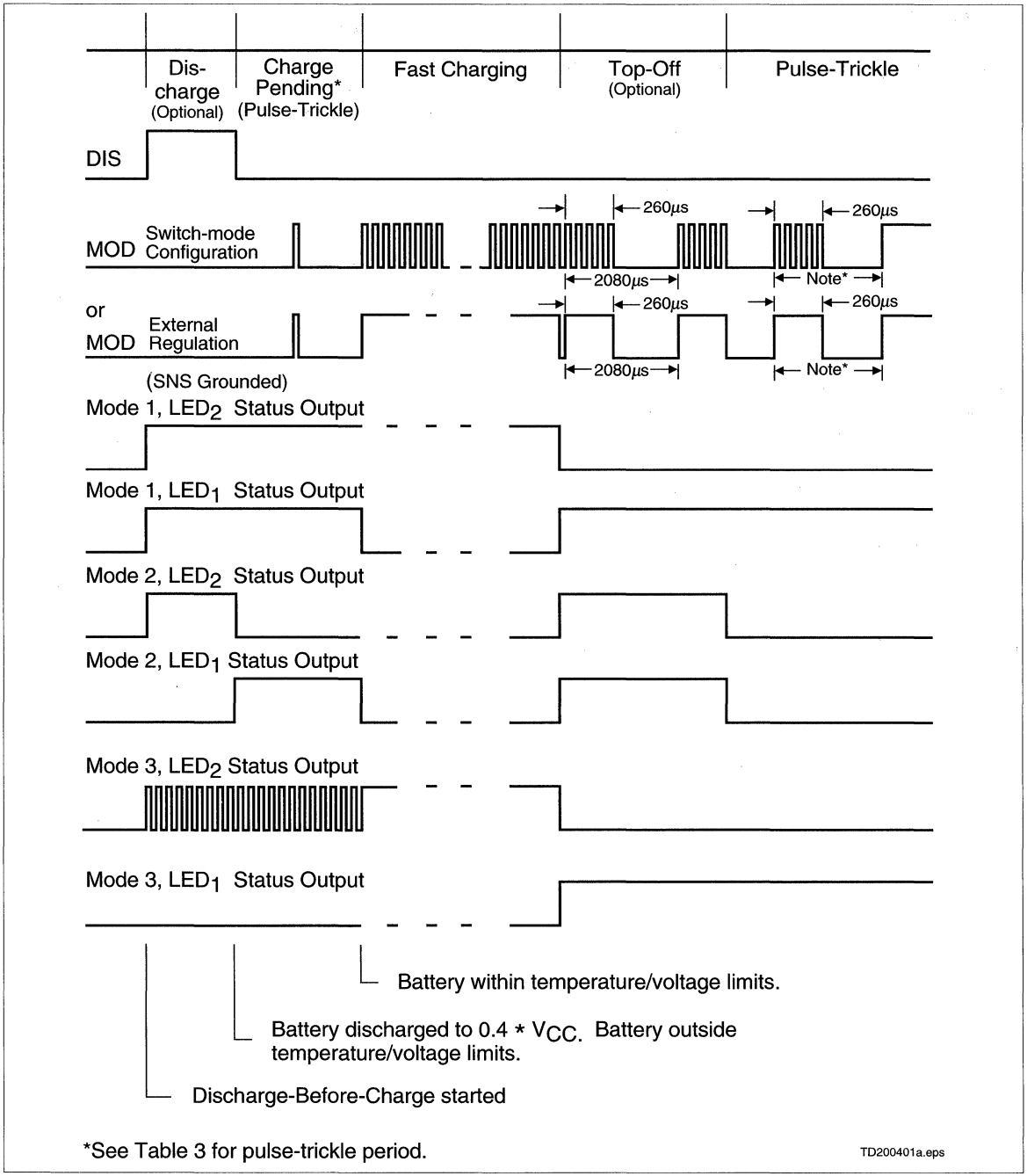


Figure 2. Charge Cycle Phases

4/12

$$V_{LTF} = 0.4 * V_{CC} \pm 30mV$$

$$V_{HTF} = [(1/4 * V_{LTF}) + (3/4 * V_{TCO})] \pm 30mV$$

Note: The low temperature fault (LTF) threshold is not enforced if the IC is configured for PVD termination (VSEL = high).

V_{TCO} is the voltage presented at the TCO input pin, and is configured by the user with a resistor divider between V_{CC} and ground. The allowed range is 0.2 to 0.4 * V_{CC}.

If the temperature of the battery is out of range, or the voltage is too low, the chip enters the charge pending state and waits for both conditions to fall within their allowed limits. The MOD output is modulated to provide the configured trickle charge rate in the charge pending state. There is no time limit on the charge pending state; the charger remains in this state as long as the voltage or temperature conditons are outside of the allowed limits. If the voltage is too high, the chip goes to the battery absent state and waits until a new charge cycle is started.

Fast charge continues until termination by one or more of the six possible termination conditions:

- Delta temperature/delta time ($\Delta T/\Delta t$)
- Peak voltage detection (PVD)
- Negative delta voltage ($-\Delta V$)
- Maximum voltage
- Maximum temperature
- Maximum time

PVD and -ΔV Termination

The bq2004 samples the voltage at the BAT pin once every 34s. When $-\Delta V$ termination is selected, if V_{CELL} is lower than any previously measured value by 12mV ±4mV (6mV/cell), fast charge is terminated. When PVD termination is selected, if V_{CELL} is lower than any previously measured value by 6mV ±2mV (3mV/cell), fast charge is terminated. The PVD and $-\Delta V$ tests are valid in the range 0.4 * V_{CC} < V_{CELL} < 0.8 * V_{CC}.

VSEL Input	Voltage Termination
Low	Disabled
Float	-ΔV
High	PVD

Voltage Sampling

Each sample is an average of voltage measurements taken 57µs apart. The IC takes 32 measurements in PVD mode and 16 measurements in $-\Delta V$ mode. The resulting sample periods (9.17ms and 18.18ms, respectively) filter out harmonics centered around 55Hz and 109Hz. This technique minimizes the effect of any AC line ripple that may feed through the power supply from either 50Hz or 60Hz AC sources. Tolerance on all timing is ±16%.

Voltage Termination Hold-off

A hold-off period occurs at the start of fast charging. During the hold-off period, $-\Delta V$ termination is disabled. This avoids premature termination on the voltage spikes sometimes produced by older batteries when fast-charge current is first applied. $\Delta T/\Delta t$, maximum voltage and maximum temperature terminations are not affected by the hold-off period.

ΔT/Δt Termination

The bq2004 samples at the voltage at the TS pin every 34s, and compares it to the value measured two samples earlier. If V_{TEMP} has fallen 16mV ±4mV or more, fast charge is terminated. If VSEL = high, the $\Delta T/\Delta t$ termination test is valid only when V_{TCO} < V_{TEMP} < V_{TCO} + 0.2 * V_{CC}. Otherwise the $\Delta T/\Delta t$ termination test is valid only when V_{TCO} < V_{TEMP} < V_{LTF}.

Temperature Sampling

Each sample is an average of 16 voltage measurements taken 57µs apart. The resulting sample period (18.18ms) filters out harmonics around 55Hz. This technique minimizes the effect of any AC line ripple that may feed through the power supply from either 50Hz or 60Hz AC sources. Tolerance on all timing is ±16%.

Maximum Voltage, Temperature, and Time

Anytime V_{CELL} rises above V_{MCV}, the LEDs go off and charging ceases immediately. If V_{CELL} then falls back below V_{MCV} before t_{MCV} = 1.5s ±0.5s, the chip transitions to the Charge Complete state (maximum voltage termination). If V_{CELL} remains above V_{MCV} at the expiration of t_{MCV}, the bq2004 transitions to the Battery Absent state (battery removal). See Figure 4.

Maximum temperature termination occurs anytime V_{TEMP} falls below the temperature cutoff threshold V_{TCO}. Unless PVD termination is enabled (VSEL = high), charge will also be terminated if V_{TEMP} rises above the low temperature fault threshold, V_{LTF}, after fast charge begins. The V_{LTF} threshold is not enforced when the IC is configured for PVD termination.

Maximum charge time is configured using the TM pin. Time settings are available for corresponding charge rates of C/4, C/2, 1C, and 2C. Maximum time-out termination is enforced on the fast-charge phase, then reset, and enforced again on the top-off phase, if selected. There is no time limit on the trickle-charge phase.

5/12

Top-off Charge

An optional top-off charge phase may be selected to follow fast charge termination for the C/2 through 4C rates. This phase may be necessary on NiMH or other battery chemistries that have a tendency to terminate charge prior to reaching full capacity. With top-off enabled, charging continues at a reduced rate after fast-charge termination for a period of time equal to the fast-charge safety time (See Table 1.) During top-off, the MOD pin is enabled at a duty cycle of 260µs active for every 1820µs inactive. This modulation results in an average rate 1/8th that of the fast charge rate. Maximum voltage, time, and temperature are the only termination methods enabled during top-off.

Pulse-Trickle Charge

Pulse-trickle charging follows the fast charge and optional top-off charge phases to compensate for self-discharge of the battery while it is idle in the charger. The configured pulse-trickle rate is also applied in the charge pending state to raise the voltage of an over-discharged battery up to the minimum required before fast charge can begin.

In the pulse-trickle mode, MOD is active for 260µs of a period specified by the settings of TM1 and TM2. See Table 1. The resulting trickle-charge rate is C/64 when top-off is enabled and C/32 when top-off is disabled. Both pulse trickle and top-off may be disabled by tying TM1 and TM2 to V_{SS}.

Charge Status Indication

Charge status is indicated by the LED_1 and LED_2 outputs. The state of these outputs in the various charge cycle phases is given in Table 2 and illustrated in Figure 2.

In all cases, if V_{CELL} exceeds the voltage at the MCV pin, both LED_1 and LED_2 outputs are held low regardless of other conditions. Both can be used to directly drive an LED.

Charge Current Control

The bq2004 controls charge current through the MOD output pin. The current control circuitry is designed to support implementation of a constant-current switching regulator or to gate an externally regulated current source.

When used in switch mode configuration, the nominal regulated current is:

$$I_{REG} = 0.225V/R_{SNS}$$

Charge current is monitored at the SNS input by the voltage drop across a sense resistor, R_{SNS}, between the low side of the battery pack and ground. R_{SNS} is sized to provide the desired fast charge current.

If the voltage at the SNS pin is less than V_{SNSLO}, the MOD output is switched high to pass charge current to the battery.

Table 1. Fast-Charge Safety Time/Hold-Off/Top-Off Table

Corresponding Fast-Charge Rate	TM1	TM2	Typical Fast-Charge Safety Time (minutes)	Typical PVD, -ΔV Hold-Off Time (seconds)	Top-Off Rate	Pulse-Trickle Rate	Pulse-Trickle Period (Hz)
C/4	Low	Low	360	137	Disabled	Disabled	Disabled
C/2	Float	Low	180	820	Disabled	C/32	240
1C	High	Low	90	410	Disabled	C/32	120
2C	Low	Float	45	200	Disabled	C/32	60
4C	Float	Float	23	100	Disabled	C/32	30
C/2	High	Float	180	820	C/16	C/64	120
1C	Low	High	90	410	C/8	C/64	60
2C	Float	High	45	200	C/4	C/64	30
4C	High	High	23	100	C/2	C/64	15

Note: Typical conditions = 25°C, V_{CC} = 5.0V.

When the SNS voltage is greater than V_{SNSHI}, the MOD output is switched low—shutting off charging current to the battery.

$$V_{SNSLO} = 0.04 * V_{CC} \pm 25mV$$

$$V_{SNSHI} = 0.05 * V_{CC} \pm 25mV$$

When used to gate an externally regulated current source, the SNS pin is connected to V_{SS}, and no sense resisitor is required.

Table 2. bq2004 LED Status Display Options

Mode 1	Charge Status	LED_1	LED_2
DSEL = V_{SS}	Battery absent	Low	Low
	Fast charge pending or discharge-before-charge in progress	High	High
	Fast charge in progress	Low	High
	Charge complete, top-off, and/or trickle	High	Low
Mode 2	**Charge Status**	**LED_1**	**LED_2**
DSEL = Floating	Battery absent, fast charge in progress or complete	Low	Low
	Fast charge pending	High	Low
	Discharge in progress	Low	High
	Top-off in progress	High	High
Mode 3	**Charge Status**	**LED_1**	**LED_2**
DSEL = V_{CC}	Battery absent	Low	Low
	Fast charge pending or discharge-before-charge in progress	Low	1/8s high 1/8s low
	Fast charge in progress	Low	High
	Fast charge complete, top-off, and/or trickle	High	Low

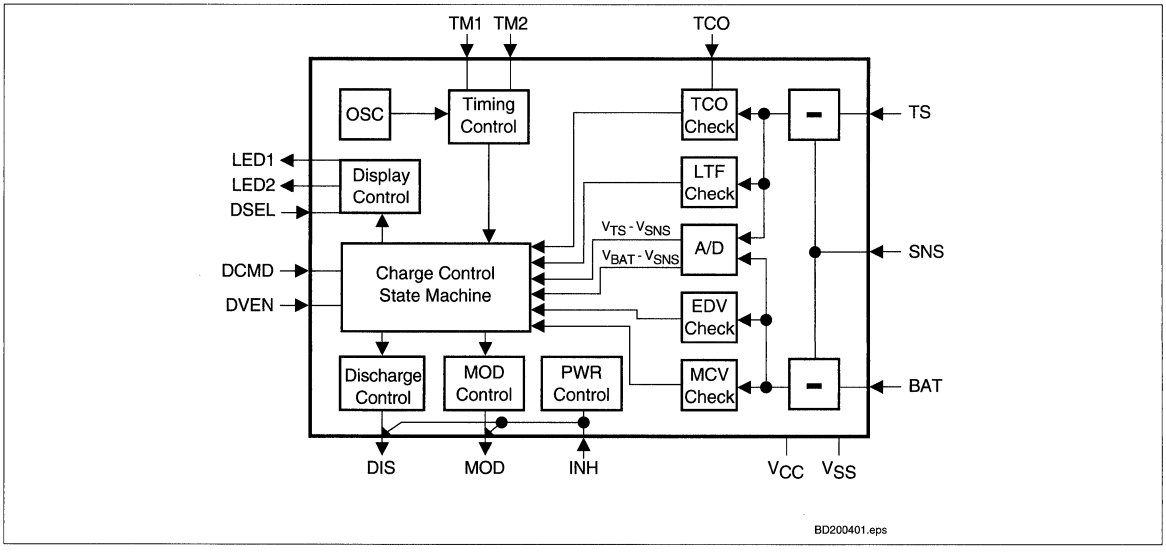


Figure 3. Block Diagram

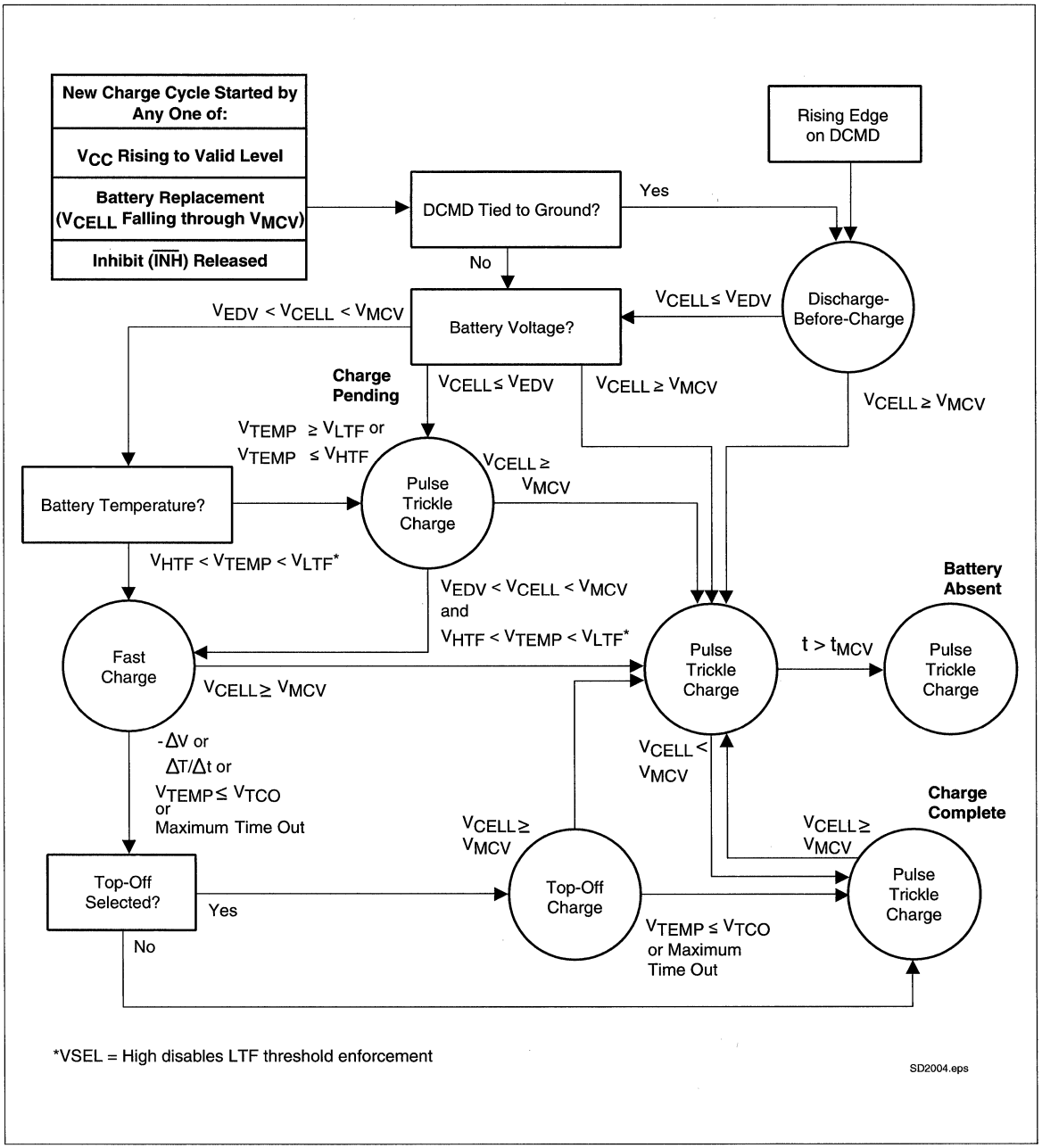


Figure 4. State Diagram

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	-20	+70	°C	Commercial
T_{STG}	Storage temperature	-55	+125	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10 sec max.
T_{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds ($T_A = T_{OPR}$; V_{CC} ±10%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{SNSHI}	High threshold at SNS resulting in MOD = Low	0.05 * V_{CC}	±0.025	V	
V_{SNSLO}	Low threshold at SNS resulting in MOD = High	0.04 * V_{CC}	±0.010	V	
V_{LTF}	Low-temperature fault	0.4 * V_{CC}	±0.030	V	$V_{TEMP} \geq V_{LTF}$ inhibits/terminates charge
V_{HTF}	High-temperature fault	(1/4 * V_{LTF}) + (2/3 * V_{TCO})	±0.030	V	$V_{TEMP} \leq V_{HTF}$ inhibits charge
V_{EDV}	End-of-discharge voltage	0.4 * V_{CC}	±0.030	V	$V_{CELL} < V_{EDV}$ inhibits fast charge
V_{MCV}	Maximum cell voltage	0.8 * V_{CC}	±0.030	V	$V_{CELL} > V_{MCV}$ inhibits/terminates charge
V_{THERM}	TS input change for$\Delta T/\Delta t$ detection	-16	±4	mV	V_{CC} = 5V, T_A = 25°C
-ΔV	BAT input change for -ΔV detection	-12	±4	mV	V_{CC} = 5V, T_A = 25°C
PVD	BAT input change for PVD detection	-6	±2	mV	V_{CC} = 5V, T_A = 25°C

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{BAT}	Battery input	0	-	V_{CC}	V	
V_{CELL}	BAT voltage potential	0	-	V_{CC}	V	V_{BAT} - V_{SNS}
V_{TS}	Thermistor input	0	-	V_{CC}	V	
V_{TEMP}	TS voltage potential	0	-	V_{CC}	V	V_{TS} - V_{SNS}
V_{TCO}	Temperature cutoff	0.2 * V_{CC}	-	0.4 * V_{CC}	V	Valid $\Delta T/\Delta t$ range
V_{IH}	Logic input high	2.0	-	-	V	$\overline{DCMD}$, $\overline{INH}$
	Logic input high	V_{CC} - 0.3	-	-	V	TM_1, TM_2, DSEL, VSEL
V_{IL}	Logic input low	-	-	0.8	V	$\overline{DCMD}$, $\overline{INH}$
	Logic input low	-	-	0.3	V	TM_1, TM_2, DSEL, VSEL
V_{OH}	Logic output high	V_{CC} - 0.8	-	-	V	DIS, MOD, LED_1, LED_2, $I_{OH} \leq$ -10mA
V_{OL}	Logic output low	-	-	0.8	V	DIS, MOD, LED_1, LED_2, $I_{OL} \leq$ 10mA
I_{CC}	Supply current	-	1	3	mA	Outputs unloaded
I_{SB}	Standby current	-	-	1	µA	$\overline{INH} = V_{IL}$
I_{OH}	DIS, LED_1, LED_2, MOD source	-10	-	-	mA	@$V_{OH} = V_{CC}$ - 0.8V
I_{OL}	DIS, LED_1, LED_2, MOD sink	10	-	-	mA	@$V_{OL} = V_{SS}$ + 0.8V
I_L	Input leakage	-	-	±1	µA	$\overline{INH}$, BAT, V = V_{SS} to V_{CC}
	Input leakage	50	-	400	µA	$\overline{DCMD}$, V = V_{SS} to V_{CC}
I_{IL}	Logic input low source	-	-	70	µA	TM_1, TM_2, DSEL, VSEL, V = V_{SS} to V_{SS} + 0.3V
I_{IH}	Logic input high source	-70	-	-	µA	TM_1, TM_2, DSEL, VSEL, V = V_{CC} - 0.3V to V_{CC}
I_{IZ}	Tri-state	-2	-	2	µA	TM_1, TM_2, DSEL, and VSEL should be left disconnected (floating) for Z logic input state

Note: All voltages relative to V_{SS} except as noted.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
R_{BAT}	Battery input impedance	50	-	-	MΩ
R_{TS}	TS input impedance	50	-	-	MΩ
R_{TCO}	TCO input impedance	50	-	-	MΩ
R_{SNS}	SNS input impedance	50	-	-	MΩ

Timing (T_A = 0 to +70°C; V_{CC} ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{PW}	Pulse width for $\overline{DCMD}$ and $\overline{INH}$ pulse command	1	-	-	µs	Pulse start for charge or discharge before charge
d_{FCV}	Time base variation	-16	-	16	%	V_{CC} = 4.75V to 5.25V
f_{REG}	MOD output regulation frequency	-	-	300	kHz	
t_{MCV}	Maximum voltage termination time limit	1	-	2	s	Time limit to distinguish battery removed from charge complete.

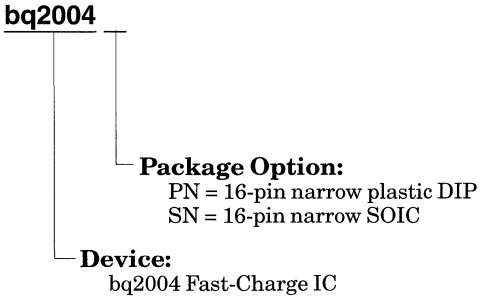
Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	10	Standby current ISB	Was 5 µA max; is 1 µA max
2	9	V_{BSNSLO} Rating	Was: V_{SNSHI} - (0.01 * V_{CC}) Is: 0.04 * V_{CC}
2	7	Correction in Peak Voltage Detect Termination section	Was VCELL; is VBAT
2	3	Added block diagram	Diagram insertion
2	7	Added VSEL/termination table	Table insertion
2	8	Added values to Table 3	Top-off rate values
3	7	VSEL/Termination	Low, High changed
4	All	Revised and expanded format of this data sheet	Clarification
5	9	Corrected V_{HTF} rating	Was: (1/3 * V_{LTF}) + (2/3 * V_{TCO}) Is: (1/4 * V_{LTF}) + (3/4 * V_{TCO})
6	9	T_{OPR}	Deleted industrial temperature range

Notes: Change 1 = Apr. 1994 B "Final" changes from Dec. 1993 A "Preliminary."
Change 2 = Sept. 1996 C changes from Apr. 1994 B.
Change 3 = April 1997 C changes from Sept. 1996 C.
Change 4 = Oct. 1997 D changes from April 1997 C.
Change 5 = Jan. 1998 E changes from Oct. 1997 D.
Change 6 = June 1999 F changes from Jan. 1998 E.

Ordering Information



12/12

Fast-Charge Development System

Control of PNP Power Transistor

Features

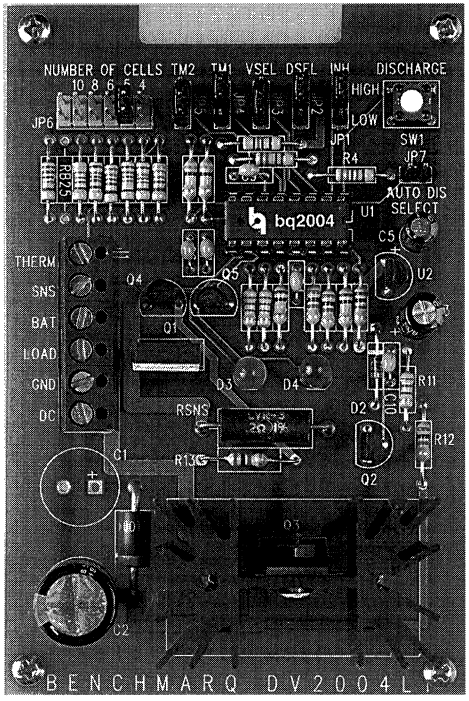
- bq2004 fast-charge control evaluation and development
- Charge current sourced from an on-board frequency-modulated linear regulator (up to 3.0A)
- Fast charge of 4 to 10 NiCd or NiMH cells and one user-defined selection
- Fast-charge termination by delta temperature/delta time ($\Delta T/\Delta t$), negative delta voltage ($-\Delta V$) or peak voltage detect, maximum temperature, maximum time, and maximum voltage
- $-\Delta V$/peak voltage detect, hold-off, top-off, maximum time, and number of cells are jumper-configurable
- Programmable charge status display
- Discharge-before-charge control with push-button switch or auto discharge-before-charge with jumper
- Inhibit fast charge by logic-level input

General Description

The DV2004L1 Development System provides a development environment for the bq2004 Fast-Charge IC. The DV2004L1 incorporates a bq2004 and a frequency-modulated linear regulator to provide fast charge control for 4 to 10 NiCd or NiMH cells.

The fast charge is terminated by any of the following: $\Delta T/\Delta t$, $-\Delta V$ or peak voltage detect, maximum temperature, maximum time, maximum voltage, or an inhibit command. Jumper settings select the voltage termination mode, the hold-off, top-off, and maximum time limits, and automatic discharge-before-charge.

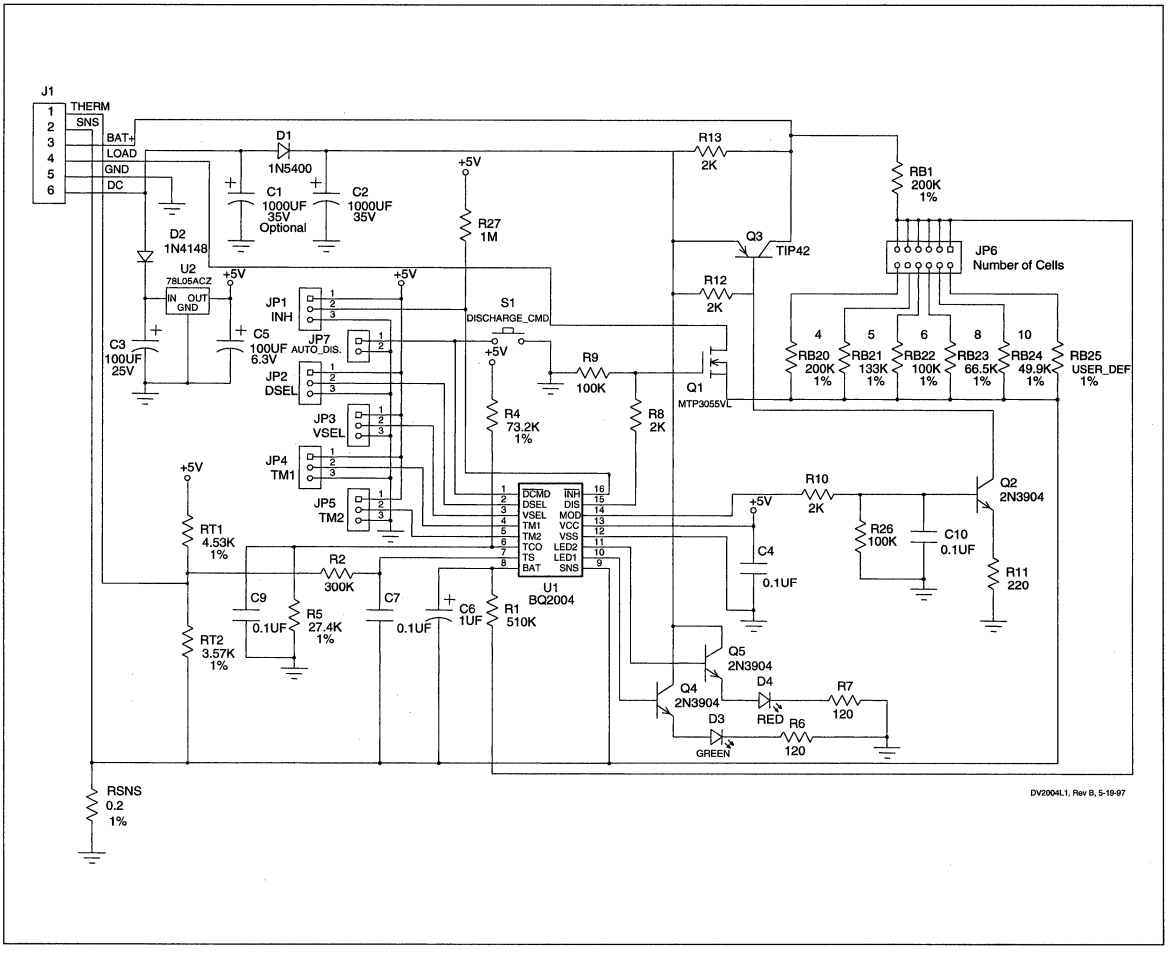
The user provides a power supply and batteries. The user configures the DV2004L1 for the number of cells, voltage, charge termination mode, and maximum charge time (with or without top-off), and commands the discharge-before-charge option with the push-button switch S1.



Please review the bq2004 data sheet before using the DV2004L1 board.

A full data sheet for this product is available on the Unitrode web site, or you may contact the factory for one.

DV2004L1 Board Schematic



Rev. B Board

UNITRODE

bq2004E/H

Fast-Charge ICs

Features

- Fast charge and conditioning of nickel cadmium or nickel-metal hydride batteries
- Hysteretic PWM switch-mode current regulation or gated control of an external regulator
- Easily integrated into systems or used as a stand-alone charger
- Pre-charge qualification of temperature and voltage
- Configurable, direct LED outputs display battery and charge status
- Fast-charge termination by Δ temperature/Δ time, peak volume detection, -ΔV, maximum voltage, maximum temperature, and maximum time
- Optional top-off charge and pulsed current maintenance charging
- Logic-level controlled low-power mode (< 5μA standby current)

General Description

The bq2004E and bq2004H Fast Charge ICs provide comprehensive fast charge control functions together with high-speed switching power control circuitry on a monolithic CMOS device.

Integration of closed-loop current control circuitry allows the bq2004 to be the basis of a cost-effective solution for stand-alone and system-integrated chargers for batteries of one or more cells.

Switch-activated discharge-before-charge allows bq2004E/H-based chargers to support battery conditioning and capacity determination.

High-efficiency power conversion is accomplished using the bq2004E/H as a hysteretic PWM controller for switch-mode regulation of the charging current. The bq2004E/H may alternatively be used to gate an externally regulated charging current.

Fast charge may begin on application of the charging supply, replacement of the battery, or switch depression. For safety, fast charge is inhibited unless/until the battery temperature and voltage are within configured limits.

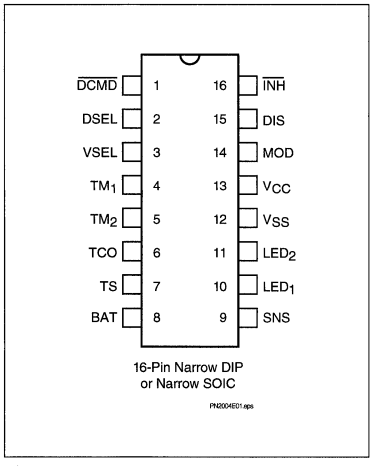
Temperature, voltage, and time are monitored throughout fast charge. Fast charge is terminated by any of the following:

- Rate of temperature rise (ΔT/Δt)
- Peak voltage detection (PVD)
- Negative delta voltage (-ΔV)
- Maximum voltage
- Maximum temperature
- Maximum time

After fast charge, optional top-off and pulsed current maintenance phases with appropriate display mode selections are available.

The bq2004H differs from the bq2004E only in that fast charge, hold-off, and top-off time units have been scaled up by a factor of two, and the bq2004H provides different display selections. Timing differences between the two ICs are illustrated in Table 1. Display differences are shown in Table 2.

Pin Connections



Pin Names

$\overline{DCMD}$	Discharge command
DSEL	Display select
VSEL	Voltage termination select
TM_1	Timer mode select 1
TM_2	Timer mode select 2
TCO	Temperature cutoff
TS	Temperature sense
BAT	Battery voltage
SNS	Sense resistor input
LED_1	Charge status output 1
LED_2	Charge status output 2
V_{SS}	System ground
V_{CC}	5.0V ±10% power
MOD	Charge current control
DIS	Discharge control output
$\overline{INH}$	Charge inhibit input

Pin Descriptions

$\overline{DCMD}$ **Discharge-before-charge control input**

The $\overline{DCMD}$ input controls the conditions that enable discharge-before-charge. $\overline{DCMD}$ is pulled up internally. A negative-going pulse on $\overline{DCMD}$ initiates a discharge to end-of-discharge voltage (EDV) on the BAT pin, followed by a new charge cycle start. Tying $\overline{DCMD}$ to ground enables automatic discharge-before-charge on every new charge cycle start.

DSEL **Display select input**

This three-state input configures the charge status display mode of the LED_1 and LED_2 outputs and can be used to disable top-off and pulsed-trickle. See Table 2.

VSEL **Voltage termination select input**

This three-state input controls the voltage-termination technique used by the bq2004E/H. When high, PVD is active. When floating, -ΔV is used. When pulled low, both PVD and -ΔV are disabled.

TM_1–TM_2 **Timer mode inputs**

TM_1 and TM_2 are three-state inputs that configure the fast charge safety timer, voltage termination hold-off time, "top-off", and trickle charge control. See Table 1.

TCO **Temperature cut-off threshold input**

Input to set maximum allowable battery temperature. If the potential between TS and SNS is less than the voltage at the TCO input, then fast charge or top-off charge is terminated.

TS **Temperature sense input**

Input, referenced to SNS, for an external thermister monitoring battery temperature.

BAT **Battery voltage input**

BAT is the battery voltage sense input, referenced to SNS. This is created by a high-impedance resistor-divider network connected between the positive and the negative terminals of the battery.

SNS **Charging current sense input**

SNS controls the switching of MOD based on an external sense resistor in the current path of the battery. SNS is the reference potential for both the TS and BAT pins. If SNS is connected to V_{SS}, then MOD switches high at the beginning of charge and low at the end of charge.

LED_1–LED_2 **Charge status outputs**

Push-pull outputs indicating charging status. See Table 2.

Vss **Ground**

V_{CC} **V_{CC} supply input**

5.0V, ±10% power input.

MOD **Charge current control output**

MOD is a push-pull output that is used to control the charging current to the battery. MOD switches high to enable charging current to flow and low to inhibit charging current flow.

DIS **Discharge control output**

Push-pull output used to control an external transistor to discharge the battery before charging.

$\overline{INH}$ **Charge inhibit input**

When low, the bq2004E/H suspends all charge actions, drives all outputs to high impedance, and assumes a low-power operational state. When transitioning from low to high, a new charge cycle is started.

Functional Description

Figure 2 shows a block diagram and Figure 3 shows a state diagram of the bq2004E/H.

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum allowable values. The voltage presented on the battery sense input, BAT, should represent a two-cell potential for the battery under charge. A resistor-divider ratio of:

$$\frac{RB1}{RB2} = \frac{N}{2} - 1$$

is recommended to maintain the battery voltage within the valid range, where N is the number of cells, RB1 is the resistor connected to the positive battery terminal, and RB2 is the resistor connected to the negative battery terminal. See Figure 1.

Note: This resistor-divider network input impedance to end-to-end should be at least 200kΩ and less than 1MΩ.

A ground-referenced negative temperature coefficient thermistor placed in proximity to the battery may be used as a low-cost temperature-to-voltage transducer. The temperature sense voltage input at TS is developed using a resistor-thermistor network between V_{CC} and V_{SS}. See Figure 1. Both the BAT and TS inputs are referenced to SNS, so the signals used inside the IC are:

$$V_{BAT} - V_{SNS} = V_{CELL}$$

and

$$V_{TS} - V_{SNS} = V_{TEMP}$$

Discharge-Before-Charge

The $\overline{DCMD}$ input is used to command discharge-before-charge via the DIS output. Once activated, DIS becomes active (high) until V_{CELL} falls below V_{EDV}, at which time DIS goes low and a new fast charge cycle begins.

The $\overline{DCMD}$ input is internally pulled up to V_{CC} (its inactive state). Leaving the input unconnected, therefore, results in disabling discharge-before-charge. A negative going pulse on $\overline{DCMD}$ initiates discharge-before-charge at any time regardless of the current state of the bq2004. If $\overline{DCMD}$ is tied to V_{SS}, discharge-before-charge will be the first step in all newly started charge cycles.

Starting A Charge Cycle

A new charge cycle is started by:

1. Application of V_{CC} power.
2. V_{CELL} falling through the maximum cell voltage, V_{MCV} where:

$$V_{MCV} = 0.8 * V_{CC} \pm 30mV$$

3. A transition on the $\overline{INH}$ input from low to high.

If $\overline{DCMD}$ is tied low, a discharge-before-charge will be executed as the first step of the new charge cycle. Otherwise, pre-charge qualification testing will be the first step.

The battery must be within the configured temperature and voltage limits before fast charging begins.

The valid battery voltage range is $V_{EDV} < V_{BAT} < V_{MCV}$ where:

$$V_{EDV} = 0.4 * V_{CC} \pm 30mV$$

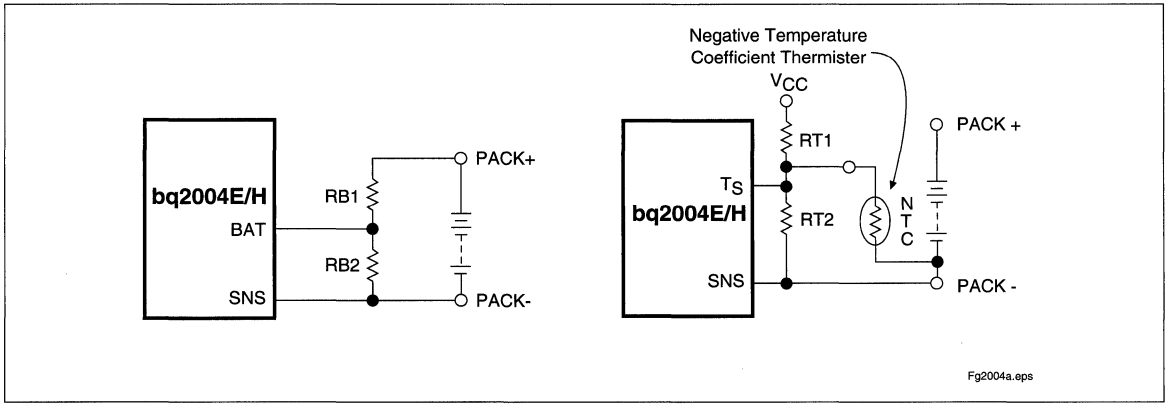


Figure 1. Voltage and Temperature Monitoring

3/12

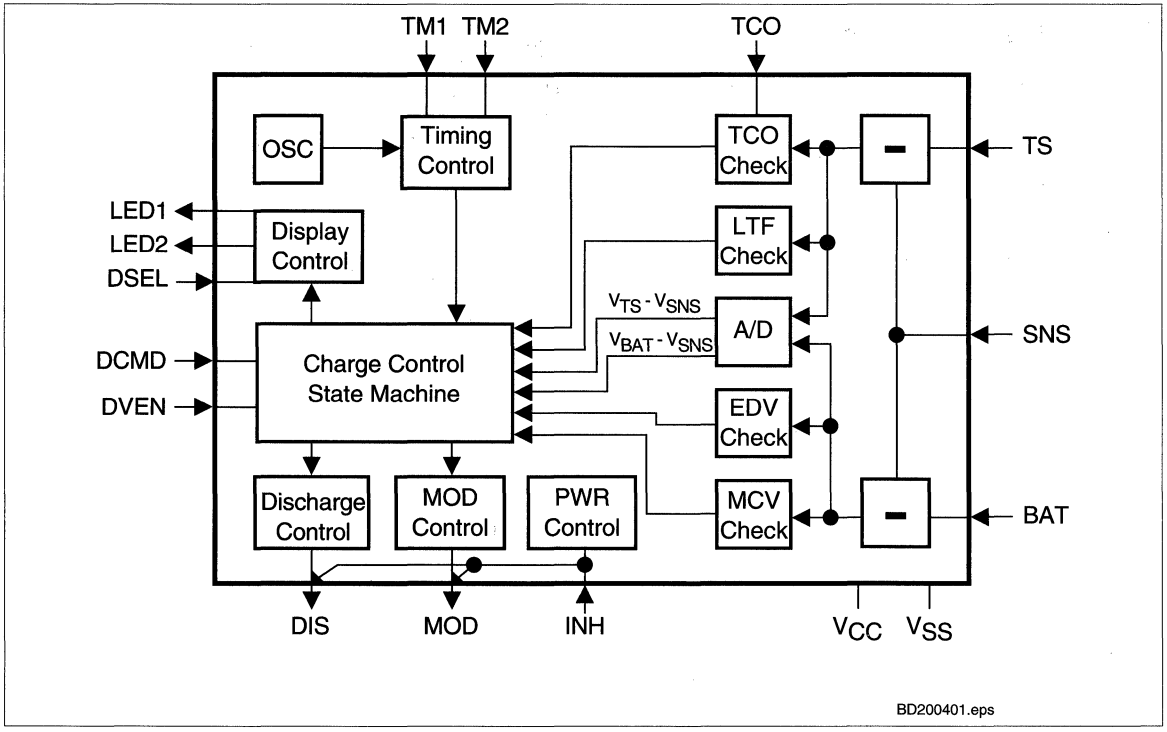


Figure 2. Block Diagram

The valid temperature range is $V_{HTF} < V_{TEMP} < V_{LTF}$, where:

$$V_{LTF} = 0.4 * V_{CC} \pm 30mV$$

$$V_{HTF} = [(1/3 * V_{LTF}) + (2/3 * V_{TCO})] \pm 30mV$$

V_{TCO} is the voltage presented at the TCO input pin, and is configured by the user with a resistor divider between V_{CC} and ground. The allowed range is 0.2 to $0.4 * V_{CC}$.

If the temperature of the battery is out of range, or the voltage is too low, the chip enters the charge pending state and waits for both conditions to fall within their allowed limits. During the charge-pending mode, the IC first applies a top-off charge to the battery.

The top-off charge, at the rate of 1/8 of the fast charge, continues until the fast-charge conditions are met or the top-off time-out period is exceeded. The IC then trickle charges until the fast-charge conditions are met. There is no time limit on the charge pending state; the charger remains in this state as long as the voltage or temperature conditons are outside of the allowed limits. If the voltage is too high, the chip goes to the battery absent state and waits until a new charge cycle is started.

4/12

Fast charge continues until termination by one or more of the six possible termination conditions:

- Delta temperature/delta time ($\Delta T/\Delta t$)
- Peak voltage detection (PVD)
- Negative delta voltage ($-\Delta V$)
- Maximum voltage
- Maximum temperature
- Maximum time

PVD and -ΔV Termination

The bq2004E/H samples the voltage at the BAT pin once every 34s. When $-\Delta V$ termination is selected, if V_{CELL} is lower than any previously measured value by 12mV ±4mV (6mV/cell), fast charge is terminated. When PVD termination is selected, if V_{CELL} is lower than any previously measured value by 6mV ±2mV (3mV/cell), fast charge is terminated. The PVD and $-\Delta V$ tests are valid in the range $0.4 * V_{CC} < V_{CELL} < 0.8 * V_{CC}$.

VSEL Input	Voltage Termination
Low	Disabled
Float	-ΔV
High	PVD

Voltage Sampling

Each sample is an average of voltage measurements. The IC takes 32 measurements in PVD mode and 16 measurements in -ΔV mode. The resulting sample periods (9.17ms and 18.18ms, respectively) filter out harmonics centered around 55Hz and 109Hz. This technique minimizes the effect of any AC line ripple that may feed through the power supply from either 50Hz or 60Hz AC sources. Tolerance on all timing is ±16%.

Temperature and Voltage Termination Hold-off

A hold-off period occurs at the start of fast charging. During the hold-off period, -ΔV and ΔT/Δt termination are disabled. The MOD pin is enabled at a duty cycle of 260µs active for every 1820µs inactive. This modulation results in an average rate 1/8th that of the fast charge rate. This avoids premature termination on the voltage spikes sometimes produced by older batteries when fast-charge current is first applied. Maximum voltage and maximum temperature terminations are not affected by the hold-off period.

ΔT/Δt Termination

The bq2004E/H samples at the voltage at the TS pin every 34s, and compares it to the value measured two samples earlier. If V_{TEMP} has fallen 16mV ±4mV or more, fast charge is terminated. The ΔT/Δt termination test is valid only when $V_{TCO} < V_{TEMP} < V_{LTF}$.

Temperature Sampling

Each sample is an average of 16 voltage measurements. The resulting sample period (18.18ms) filters out harmonics around 55Hz. This technique minimizes the effect of any AC line ripple that may feed through the power supply from either 50Hz or 60Hz AC sources. Tolerance on all timing is ±16%.

Maximum Voltage, Temperature, and Time

Anytime V_{CELL} rises above V_{MCV}, the LEDs go off and current flow into the battery ceases immediately. If V_{CELL} then falls back below V_{MCV} before t_{MCV} = 1.5s ±0.5s, the chip transitions to the Charge Complete state (maximum voltage termination). If V_{CELL} remains above V_{MCV} at the expiration of t_{MCV}, the bq2004E/H transitions to the Battery Absent state (battery removal). See Figure 3.

Maximum temperature termination occurs anytime V_{TEMP} falls below the temperature cutoff threshold V_{TCO}. Charge will also be terminated if V_{TEMP} rises above the low temperature fault threshold, V_{LTF}, after fast charge begins.

Table 1. Fast Charge Safety Time/Hold-Off/Top-Off Table

Corresponding Fast-Charge Rate				Typical Fast-Charge Safety Time (min)		Typical PVD, -ΔV Hold-Off Time (s)		Top-Off Rate		Pulse-Trickle Rate	Pulse-Trickle Period (Hz)	
2004E	2004H	TM1	TM2	2004E	2004H	2004E	2004H	2004E	2004H		2004E	2004H
C/4	C/8	Low	Low	325	650	137	273	Disabled		Disabled	Disabled	
C/2	C/4	Float	Low	154	325	546	546	Disabled		C/512	15	30
1C	C/2	High	Low	77	154	273	546	Disabled		C/512	7.5	15
2C	1C	Low	Float	39	77	137	273	Disabled		C/512	3.75	7.5
4C	2C	Float	Float	19	39	68	137	Disabled		C/512	1.88	3.75
C/2	C/4	High	Float	154	325	546	546	C/16	C/32	C/512	15	30
1C	C/2	Low	High	77	154	273	546	C/8	C/16	C/512	7.5	15
2C	1C	Float	High	39	77	137	273	C/4	C/18	C/512	3.75	7.5
4C	2C	High	High	19	39	68	137	C/2	C/4	C/512	1.88	3.75

Note: Typical conditions = 25°C, V_{CC} = 5.0V.

5/12

Table 2. bq2004E/H LED Output Summary

Mode 1 bq2004E	Charge Action State	LED_1	LED_2
DSEL = V_{SS}	Battery absent	Low	Low
	Fast charge pending or a discharge-before-charge in progress	High	High
	Fast charging	Low	High
	Fast charge complete, top-off, and/or trickle	High	Low
Mode 1 bq2004H	**Charge Action State**	**LED_1**	**LED_2**
DSEL = V_{SS}	Battery absent	Low	Low
	Discharge-before-charge in progress	High	High
	Fast charge pending	Low	1/8 second high 1/8 second low
	Fast charging	Low	High
	Fast charge complete, top-off, and/or trickle	High	Low
Mode 2 bq2004E	**Charge Action State (See note)**	**LED_1**	**LED_2**
DSEL = Floating	Battery absent	Low	Low
	Fast charge pending or discharge-before-charge in progress	High	High
	Fast charging	Low	High
	Fast charge complete, top-off, and/or trickle	High	Low
Mode 2 bq2004H	**Charge Action State (See note)**	**LED_1**	**LED_2**
DSEL = Floating	Battery absent	Low	Low
	Discharge-before-charge in progress	High	High
	Fast charge pending	Low	1/8 second high 1/8 second low
	Fast charging	Low	High
	Fast charge complete, top-off, and/or trickle	High	Low
Mode 3 bq2004E/H	**Charge Action State**	**LED_1**	**LED_2**
DSEL = V_{CC}	Battery absent	Low	Low
	Fast charge pending or discharge-before-charge in progress	Low	1/8 second high 1/8 second low
	Fast charging	Low	High
	Fast charge complete, top-off, and/or trickle	High	Low

Note: Pulse trickle is inhibited in Mode 2.

Maximum charge time is configured using the TM pin. Time settings are available for corresponding charge rates of C/4, C/2, 1C, and 2C. Maximum time-out termination is enforced on the fast-charge phase, then reset, and enforced again on the top-off phase, if selected. There is no time limit on the trickle-charge phase.

Top-off Charge

An optional top-off charge phase may be selected to follow fast charge termination for the C/2 through 4C rates. This phase may be necessary on NiMH or other battery chemistries that have a tendency to terminate charge prior to reaching full capacity. With top-off enabled, charging continues at a reduced rate after fast-charge termination for a period of time equal to 0.235* the fast-charge safety time (See Table 1.) During top-off, the MOD pin is enabled at a duty cycle of 260µs active for every 1820µs inactive. This modulation results in an average rate 1/8th that of the fast charge rate. Maximum voltage, time, and temperature are the only termination methods enabled during top-off.

Pulse-Trickle Charge

Pulse-trickle charging may be configured to follow the fast charge and optional top-off charge phases to compensate for self-discharge of the battery while it is idle in the charger.

In the pulse-trickle mode, MOD is active for 260µs of a period specified by the settings of TM1 and TM2. See Table 1. The resulting trickle-charge rate is C/512. Both pulse trickle and top-off may be disabled by tying TM1 and TM2 to V_{SS} or by selecting Mode 2 in the display.

Charge Status Indication

Charge status is indicated by the LED_1 and LED_2 outputs. The state of these outputs in the various charge cycle phases is given in Table 2 and illustrated in Figure 3.

In all cases, if V_{CELL} exceeds the voltage at the MCV pin, both LED_1 and LED_2 outputs are held low regardless of other conditions. Both can be used to directly drive an LED.

Charge Current Control

The bq2004E/H controls charge current through the MOD output pin. The current control circuitry is designed to support implementation of a constant-current switching regulator or to gate an externally regulated current source.

When used in switch mode configuration, the nominal regulated current is:

$$I_{REG} = 0.225V/R_{SNS}$$

Charge current is monitored at the SNS input by the voltage drop across a sense resistor, R_{SNS}, between the low side of the battery pack and ground. R_{SNS} is sized to provide the desired fast charge current.

If the voltage at the SNS pin is less than V_{SNSLO}, the MOD output is switched high to pass charge current to the battery.

When the SNS voltage is greater than V_{SNSHI}, the MOD output is switched low—shutting off charging current to the battery.

$$V_{SNSLO} = 0.04 * V_{CC} \pm 25mV$$

$$V_{SNSHI} = 0.05 * V_{CC} \pm 25mV$$

When used to gate an externally regulated current source, the SNS pin is connected to V_{SS}, and no sense resisitor is required.

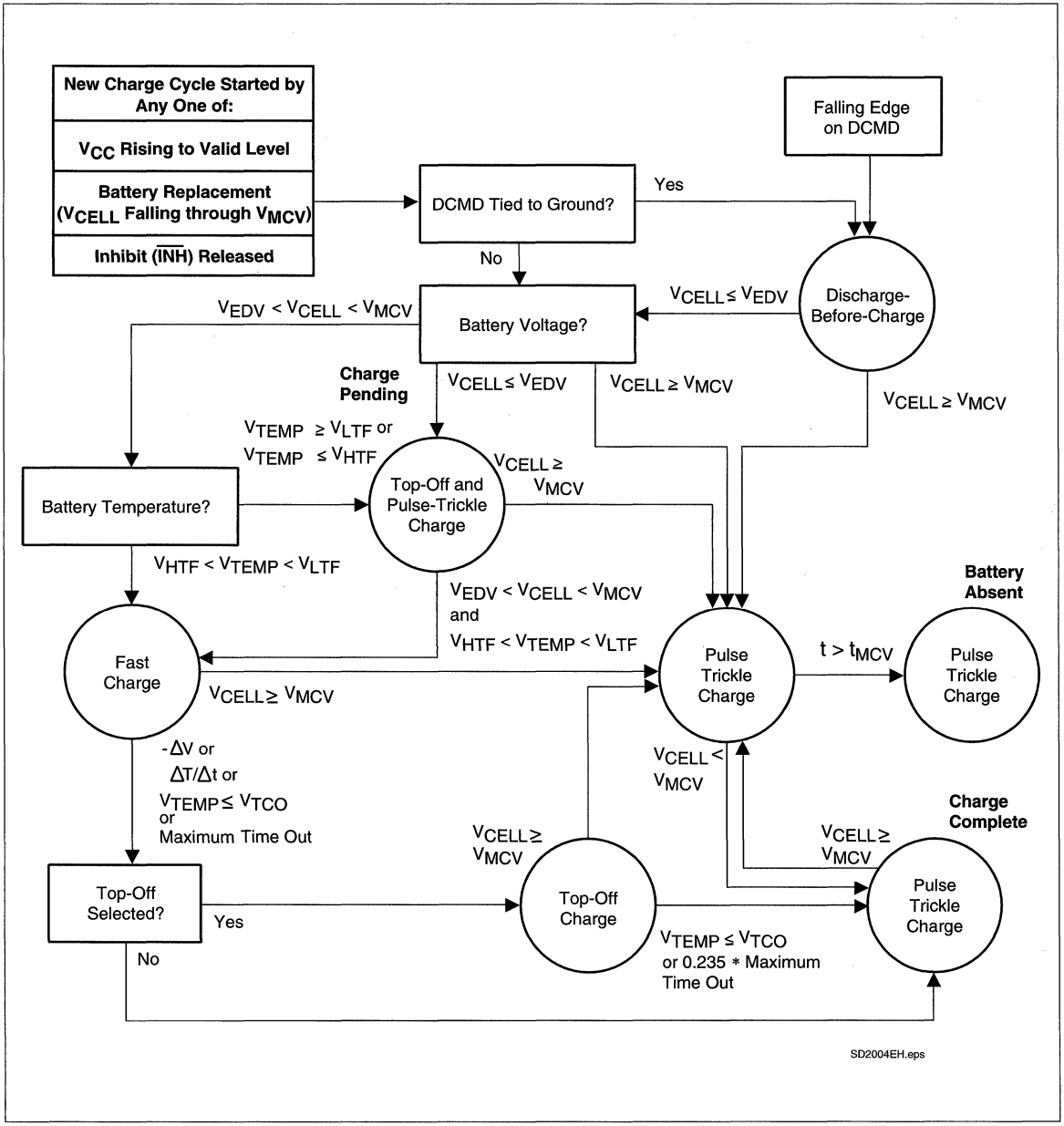


Figure 3. Charge Algorithm State Diagram

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	-20	+70	°C	Commercial
T_{STG}	Storage temperature	-55	+125	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10 sec max.
T_{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds ($T_A = T_{OPR}$; V_{CC} ±10%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{SNSHI}	High threshold at SNS resulting in MOD = Low	0.05 * V_{CC}	±0.025	V	
V_{SNSLO}	Low threshold at SNS resulting in MOD = High	0.04 * V_{CC}	±0.010	V	
V_{LTF}	Low-temperature fault	0.4 * V_{CC}	±0.030	V	$V_{TEMP} \geq V_{LTF}$ inhibits/terminates charge
V_{HTF}	High-temperature fault	(1/3 * V_{LTF}) + (2/3 * V_{TCO})	±0.030	V	$V_{TEMP} \leq V_{HTF}$ inhibits charge
V_{EDV}	End-of-discharge voltage	0.4 * V_{CC}	±0.030	V	$V_{CELL} < V_{EDV}$ inhibits fast charge
V_{MCV}	Maximum cell voltage	0.8 * V_{CC}	±0.030	V	$V_{CELL} > V_{MCV}$ inhibits/terminates charge
V_{THERM}	TS input change for$\Delta T/\Delta t$ detection	-16	±4	mV	V_{CC} = 5V, T_A = 25°C
-ΔV	BAT input change for -ΔV detection	-12	±4	mV	V_{CC} = 5V, T_A = 25°C
PVD	BAT input change for PVD detection	-6	±2	mV	V_{CC} = 5V, T_A = 25°C

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{BAT}	Battery input	0	-	V_{CC}	V	
V_{CELL}	BAT voltage potential	0	-	V_{CC}	V	V_{BAT} - V_{SNS}
V_{TS}	Thermistor input	0	-	V_{CC}	V	
V_{TEMP}	TS voltage potential	0	-	V_{CC}	V	V_{TS} - V_{SNS}
V_{TCO}	Temperature cutoff	0.2 * V_{CC}	-	0.4 * V_{CC}	V	Valid $\Delta T/\Delta t$ range
V_{IH}	Logic input high	2.0	-	-	V	$\overline{DCMD}$, $\overline{INH}$
	Logic input high	V_{CC} - 0.3	-	-	V	TM_1, TM_2, DSEL, VSEL
V_{IL}	Logic input low	-	-	0.8	V	$\overline{DCMD}$, $\overline{INH}$
	Logic input low	-	-	0.3	V	TM_1, TM_2, DSEL, VSEL
V_{OH}	Logic output high	V_{CC} - 0.8	-	-	V	DIS, MOD, LED_1, LED_2, $I_{OH} \leq$ -10mA
V_{OL}	Logic output low	-	-	0.8	V	DIS, MOD, LED_1, LED_2, $I_{OL} \leq$ 10mA
I_{CC}	Supply current	-	1	3	mA	Outputs unloaded
I_{SB}	Standby current	-	-	1	µA	$\overline{INH} = V_{IL}$
I_{OH}	DIS, LED_1, LED_2, MOD source	-10	-	-	mA	@$V_{OH} = V_{CC}$ - 0.8V
I_{OL}	DIS, LED_1, LED_2, MOD sink	10	-	-	mA	@$V_{OL} = V_{SS}$ + 0.8V
I_L	Input leakage	-	-	±1	µA	$\overline{INH}$, BAT, V = V_{SS} to V_{CC}
	Input leakage	50	-	400	µA	$\overline{DCMD}$, V = V_{SS} to V_{CC}
I_{IL}	Logic input low source	-	-	70	µA	TM_1, TM_2, DSEL, VSEL, V = V_{SS} to V_{SS} + 0.3V
I_{IH}	Logic input high source	-70	-	-	µA	TM_1, TM_2, DSEL, VSEL, V = V_{CC} - 0.3V to V_{CC}
I_{IZ}	Tri-state	-2	-	2	µA	TM_1, TM_2, DSEL, and VSEL should be left disconnected (floating) for Z logic input state

Note: All voltages relative to V_{SS} except as noted.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
R_{BAT}	Battery input impedance	50	-	-	MΩ
R_{TS}	TS input impedance	50	-	-	MΩ
R_{TCO}	TCO input impedance	50	-	-	MΩ
R_{SNS}	SNS input impedance	50	-	-	MΩ

Timing (T_A = 0 to +70°C; V_{CC} ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{PW}	Pulse width for $\overline{DCMD}$ and $\overline{INH}$ pulse command	1	-	-	µs	Pulse start for charge or discharge before charge
d_{FCV}	Time base variation	-16	-	16	%	V_{CC} = 4.75V to 5.25V
f_{REG}	MOD output regulation frequency	-	-	300	kHz	
t_{MCV}	Maximum voltage termination time limit	1	-	2	s	Time limit to distinguish battery removed from charge complete.

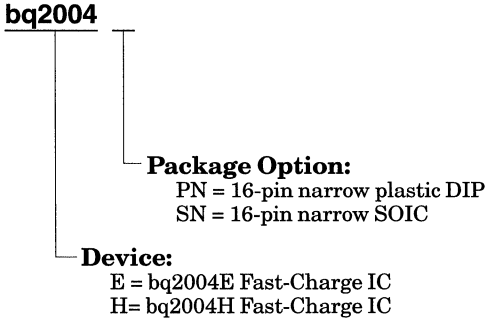
Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	All	Combined bq2004E and bq2004H, revised and expanded format of this data sheet	Clarification
2	7	Separated bq2004E and bq2004H in Table 2, LED Output Summary	Clarification
3	5	Description of charge-pending state	Clarification
4			

Note: Change 1 = Oct. 1997 B changes from Sept. 1996 (bq2004E), Feb. 1997 (bq2004H).
Change 2 = Feb. 1998 C changes from Oct. 1997 B.
Change 3 = Dec. 1998 D changes from Feb. 1998 C.
Change 4 = June 1999 E changes from Dec. 1998 D.

Ordering Information



12/12

UNITRODE

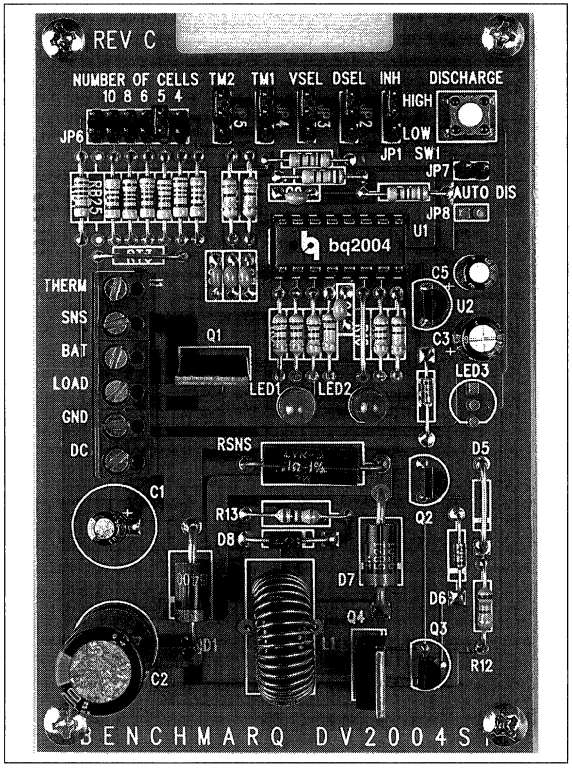
Product Brief DV2004S1/ES1/HS1

Fast-Charge Development Systems

Control of On-Board P-FET Switch-Mode Regulator

Features

- bq2004/E/H fast-charge control evaluation and development
- Charge current sourced from an on-board switch-mode regulator (up to 3.0A)
- Fast charge of 4 to 10 NiCd or NiMH cells and one user-defined selection
- Fast-charge termination by delta temperature/delta time (ΔT/Δt), negative delta voltage (-ΔV) or peak voltage detect, maximum temperature, maximum time, and maximum voltage
- -ΔV/peak voltage detect, hold-off, top-off, maximum time, and number of cells are jumper-configurable
- Programmable charge status display
- Discharge-before-charge control with push-button switch or auto discharge-before-charge with jumper
- Inhibit fast charge by logic-level input



General Description

The DV2004/E/H/S1 Development Systems provide a development environment for the bq2004, bq2004E, or bq2004H Fast-Charge IC. The DV2004/E/H/S1 incorporate a bq2004/E/H and a buck-type switch-mode regulator to provide fast charge controls for 4 to 10 NiCd or NiMH cells.

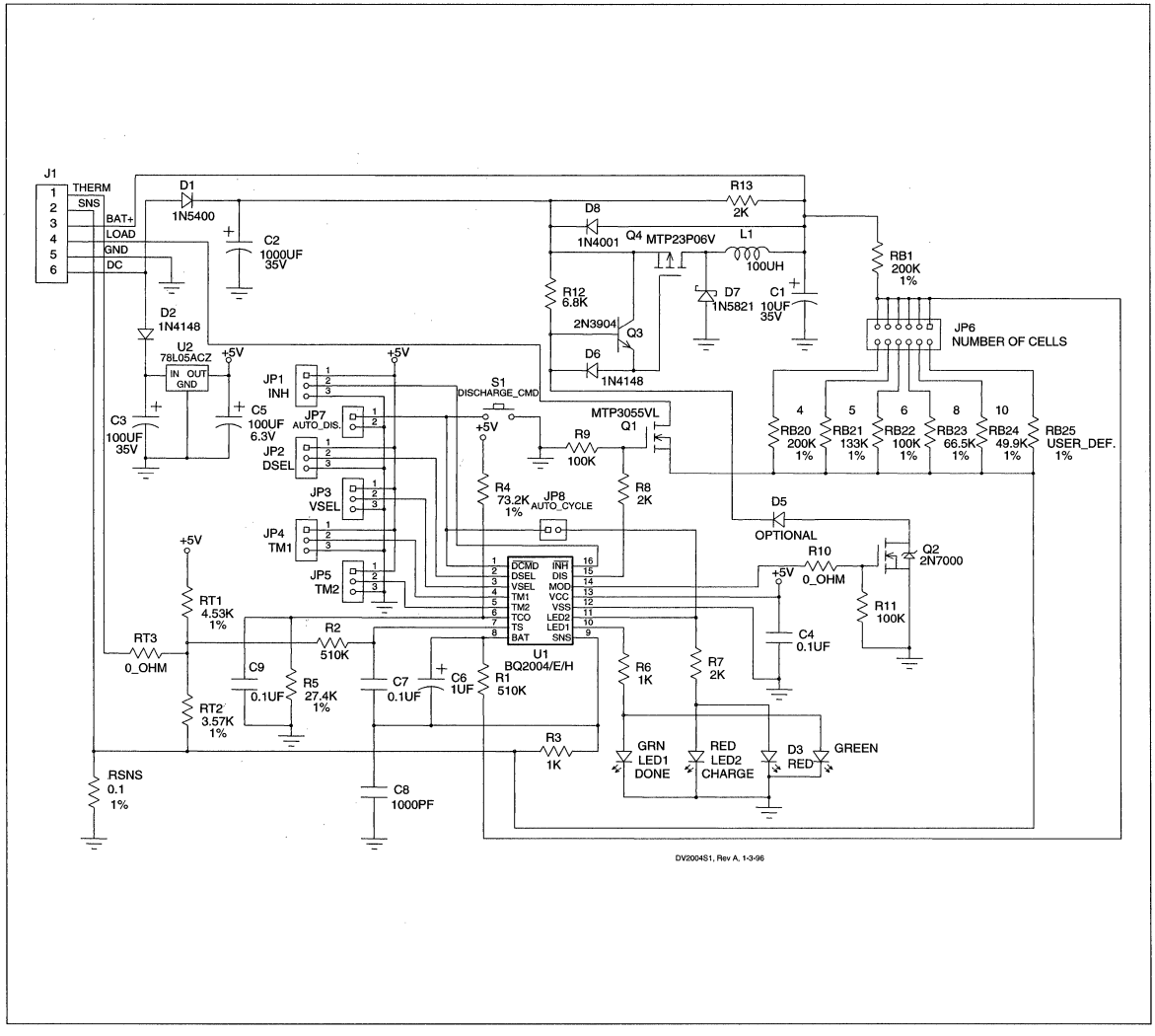
The fast charge is terminated by any of the following: ΔT/Δt, -ΔV or peak voltage detect, maximum temperature, maximum time, maximum voltage, or an inhibit command. Jumper settings select the voltage termination mode, the hold-off, top-off, and maximum time limits, and automatic discharge-before-charge.

The user provides a power supply and batteries. The user configures the DV2004/E/H/S1 for the number of cells, voltage, charge termination mode, and maximum charge time (with or without top-off), and commands the discharge-before-charge option with the push-button switch S1.

Please review the bq2004/E/H data sheets, before using the DV2004/E/H/S1 boards.

Full data sheets for these products are available on the Unitrode web site or from the factory.

DV2004S1 Board Schematic



Rev. C Board

UNITRODE

bq2005

Fast-Charge IC for Dual-Battery Packs

3

Features

- Sequential fast charge and conditioning of two NiCd or NiMH nickel cadmium or nickel-metal hydride battery packs
- Hysteretic PWM switch-mode current regulation or gated control of an external regulator
- Easily integrated into systems or used as a stand-alone charger
- Pre-charge qualification of temperature and voltage
- Direct LED outputs display battery and charge status
- Fast-charge termination by Δ temperature/Δ time, -ΔV, maximum voltage, maximum temperature, and maximum time
- Optional top-off and pulse-trickle charging

General Description

The bq2005 Fast-Charge IC provides comprehensive fast charge control functions together with high-speed switching power control circuitry on a monolithic CMOS device for sequential charge management in dual battery pack applications.

Integration of closed-loop current control circuitry allows the bq2005 to be the basis of a cost-effective solution for stand-alone and system-integrated chargers for batteries of one or more cells.

Switch-activated discharge-before-charge allows bq2005-based chargers to support battery conditioning and capacity determination.

High-efficiency power conversion is accomplished using the bq2005 as a hysteretic PWM controller for switch-mode regulation of the charging current. The bq2005 may alternatively be used to gate an externally regulated charging current.

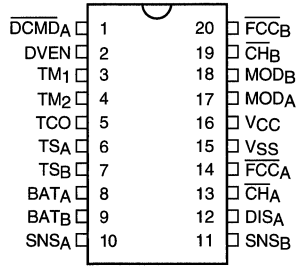
Fast charge may begin on application of the charging supply, replacement of the battery, or switch depression. For safety, fast charge is inhibited unless/until the battery temperature and voltage are within configured limits.

Temperature, voltage, and time are monitored throughout fast charge. Fast charge is terminated by any of the following:

- Rate of temperature rise (ΔT/Δt)
- Negative delta voltage (-ΔV)
- Maximum voltage
- Maximum temperature
- Maximum time

After fast charge, optional top-off and pulsed current maintenance phases are available.

Pin Connections



20-Pin DIP or SOIC

PN200501.eps

Pin Names

$\overline{DCMD}_A$	Discharge command input, battery A
DVEN	-ΔV enable
TM_1	Timer mode select 1
TM_2	Timer mode select 2
TCO	Temperature cut-off
TS_A, TS_B	Temperature sense input, battery A/B
BAT_A, BAT_B	Battery voltage input, battery A/B
SNSA, SNSB	Sense resistor input , battery A/B
DIS_A	Discharge control output, battery A
$\overline{CH}_A$, $\overline{CH}_B$	Charge status output, battery A/B
$\overline{FCC}_A$, $\overline{FCC}_B$	Fast charge complete output, battery A/B
V_{SS}	System ground
V_{CC}	5.0V ±10% power
MOD_A, MOD_B	Charge current control output, battery A/B

Pin Descriptions

$DCMD_A$ **Discharge-before-charge control input, battery A**

$\overline{DCMD_A}$ controls the discharge-before-charge function of the bq2005. A negative-going pulse on $\overline{DCMD_A}$ initiates a discharge to EDV followed by a charge if conditions allow. By tying $\overline{DCMD_A}$ to ground, automatic discharge-before-charge is enabled on every new charge cycle start.

DVEN **-ΔV enable input**

This input enales/disables -ΔV charge termination. If DVEN is high, the -ΔV test is enabled. If DVEN is low, -ΔV test is disabled. The state of DVEN may be changed at any time.

TM_1–TM_2 **Timer mode inputs**

TM_1 and TM_2 are three-state inputs that configure the fast charge safety timer, -ΔV hold-off time, and that enhance/disable top-off. See Table 2.

TCO **Temperature cutoff threshold input**

Input to set maximum allowable battery temperature. If the potential between TS_A and SNS_A or TSB and SNS_B is less than the voltage at the TCO input, then fast charge or top-off charge is terminated for the corresponding battery pack.

TS_A, TS_B **Temperature sense inputs**

Input, referenced to SNS_A or SNS_B, respectively, for an external thermistor monitoring battery temperature.

BAT_A, BAT_B **Voltage inputs**

The battery voltage sense input, referenced to $SNS_{A,B}$, respectively. This is created by a high-impedance resistor divider network connected between the positive and the negative terminals of the battery.

SNS_A, SNS_B **Charging current sense inputs,**

$SNS_{A,B}$ controls the switching of $MOD_{A,B}$ based on the voltage across an external sense resistor in the current path of the battery. SNS is the reference potential for the TS and BAT pins. If SNS is connected to V_{SS}, MOD switches high at the beginning of charge and low at the end of charge.

DIS_A **Discharge control output**

Push-pull output used to control an external transistor to discharge battery A before charging.

$\overline{CH_A}$, $\overline{CH_B}$ **Charge status outputs**

Push-pull outputs indicating charging status for batteries A and B, respectively. See Figure 1 and Table 2.

$\overline{FCC_A}$, $\overline{FCC_B}$ **Fast charge complete outputs**

Open-drain outputs indicating fast charge complete for batteries A and B, respectively. See Figure 1 and Table 2.

MOD_A, MOD_B **Charge current control outputs**

$MOD_{A,B}$ is a push-pull output that is used to control the charging current to the battery. $MOD_{A,B}$ switches high to enable charging current to flow and low to inhibit charging current flow to batteries A and B, respectively.

V_{CC} **V_{CC} supply input**

5.0 V, ±10% power input.

Vss **Ground**

Functional Description

Figure 3 shows a block diagram and Figure 4 shows a state diagram of the bq2005.

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum allowable values. The voltage presented on the battery sense input, $BAT_{A,B}$, must be divided down to between 0.95 * V_{CC} and 0.475 * V_{CC} for proper operation. A resistor-divider ratio of:

$$\frac{RB1}{RB2} = \frac{N}{2.375} - 1$$

is recommended to maintain the battery voltage within the valid range, where N is the number of cells, RB1 is the resistor connected to the positive battery terminal, and RB2 is the resistor connected to the negative battery terminal. See Figure 1.

Note: This resistor-divider network input impedance to end-to-end should be at least 200kΩ and less than 1MΩ.

A ground-referenced negative temperature coefficient thermistor placed in proximity to the battery may be used as a low-cost temperature-to-voltage transducer. The temperature sense voltage input at $TS_{A,B}$ is developed using a resistor-thermistor network between V_{CC} and V_{SS}. See Figure 1. Both the $BAT_{A,B}$ and $TS_{A,B}$ inputs are referenced to $SNS_{A,B}$, so the signals used inside the IC are:

$$V_{BAT(A,B)} - V_{SNS(A,B)} = V_{CELL(A,B)}$$

and

$$V_{TS(A,B)} - V_{SNS(A,B)} = V_{TEMP(A,B)}$$

Discharge-Before-Charge

The $\overline{DCMD}_A$ input is used to command discharge-before-charge via the DIS_A output. Once activated, DIS_A becomes active (high) until V_{CELL} falls below V_{EDV} where:

$$V_{EDV} = 0.475 * V_{CC} \pm 30mV$$

at which time DIS_A goes low and a new fast charge cycle begins.

The $\overline{DCMD}_A$ input is internally pulled up to V_{CC} (its inactive state). Leaving the input unconnected, therefore, results in disabling discharge-before-charge. A negative going pulse on $\overline{DCMD}_A$ initiates discharge-before-charge at any time regardless of the current state of the bq2005. If $\overline{DCMD}_A$ is tied to V_{SS}, discharge-before-charge will be the first step in all newly started charge cycles.

Starting A Charge Cycle

A new charge cycle is started by (see Figure 2):

1. V_{CC} rising above 4.5V
2. V_{CELL} falling through the maximum cell voltage, V_{MCV} where:

$$V_{MCV} = 0.95 * V_{CC} \pm 30mV$$

If $\overline{DCMD}_A$ is tied low, a discharge-before-charge will be executed as the first step of the new charge cycle. Otherwise, pre-charge qualification testing will be the first step.

The battery must be within the configured temperature and voltage limits before fast charging begins.

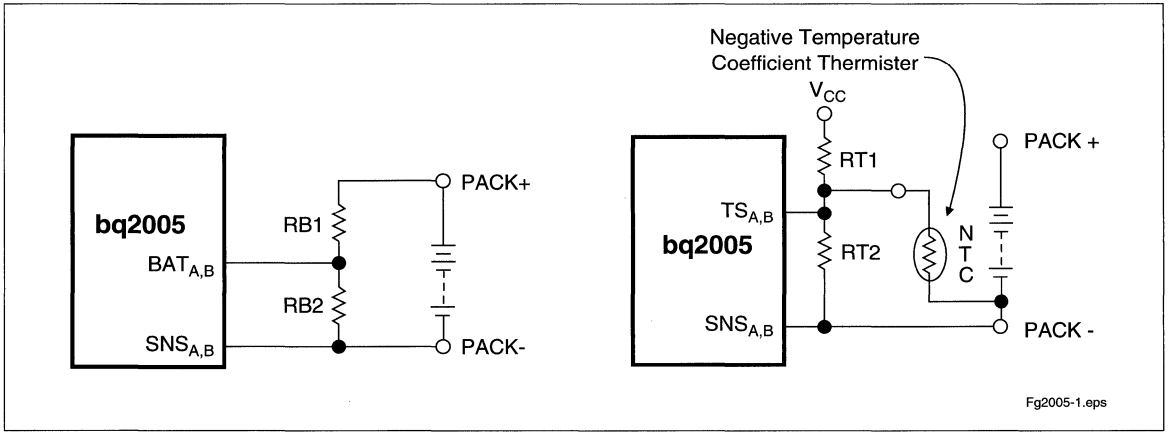


Figure 1. Voltage and Temperature Monitoring

3/12

The valid battery voltage range is $V_{EDV} < V_{BAT} < V_{MCV}$. The valid temperature range is $V_{HTF} < V_{TEMP} < V_{LTF}$, where:

$$V_{LTF} = 0.4 * V_{CC} \pm 30mV$$

$$V_{HTF} = [(1/4 * V_{LTF}) + (3/4 * V_{TCO})] \pm 30mV$$

V_{TCO} is the voltage presented at the TCO input pin, and is configured by the user with a resistor divider between V_{CC} and ground. The allowed range is 0.2 to $0.4 * V_{CC}$.

If the temperature of the battery is out of range, or the voltage is too low, the chip enters the charge pending state and waits for both conditions to fall within their allowed limits. The $MOD_{A,B}$ output is modulated to provide the configured trickle charge rate in the charge pending state. There is no time limit on the charge pending state; the charger remains in this state as long as the voltage or temperature conditons are outside of the allowed limits. If the voltage is too high, the chip goes to the battery absent state and waits until a new charge cycle is started.

Fast charge continues until termination by one or more of the five possible termination conditions:

- Delta temperature/delta time ($\Delta T/\Delta t$)
- Negative delta voltage ($-\Delta V$)
- Maximum voltage
- Maximum temperature
- Maximum time

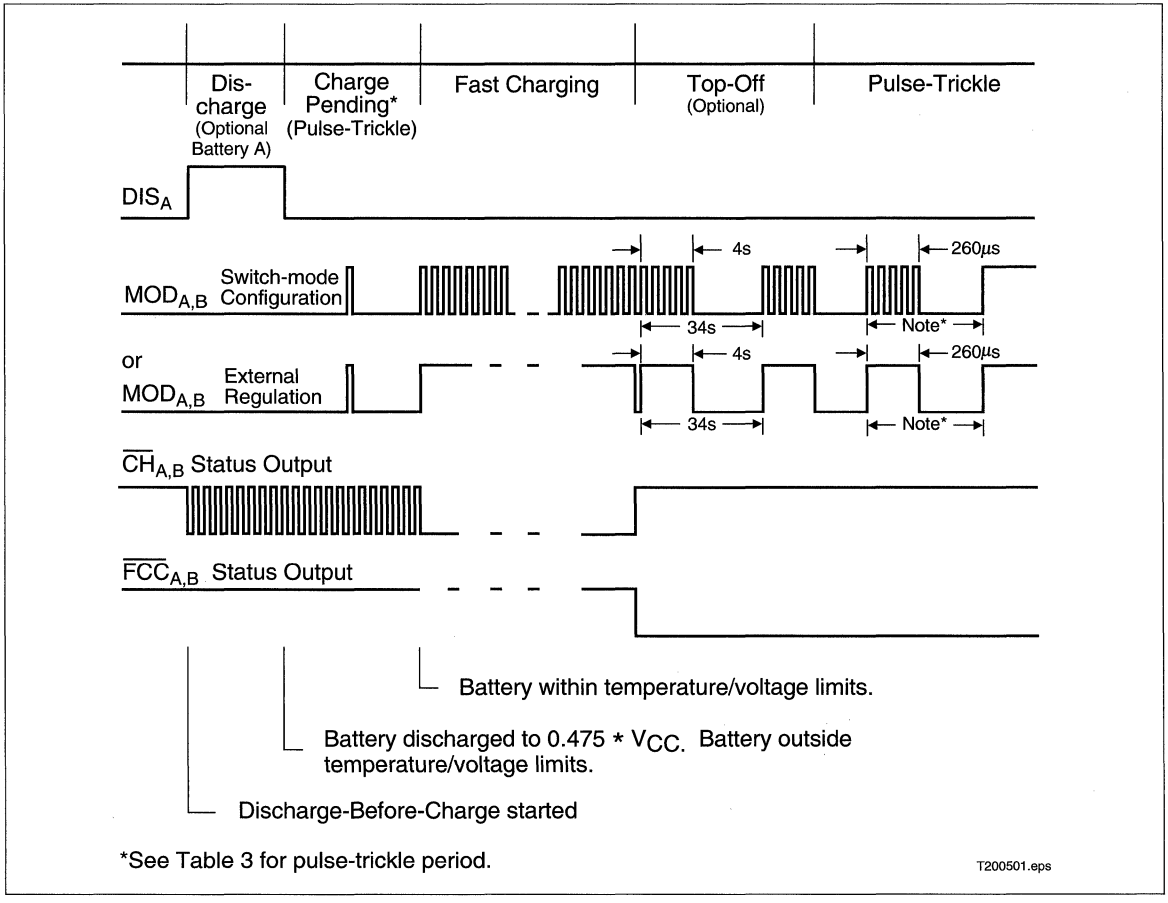


Figure 2. Charge Cycle Phases

Table 1. Fast Charge Safety Time/Hold-Off/Top-Off Table

Corresponding Fast-Charge Rate	TM1	TM2	Typical Fast-Charge and Top-Off Time Limits	Typical -ΔV/MCV Hold-Off Time (seconds)	Top-Off Rate
C/4	Low	Low	360	137	Disabled
C/2	Float	Low	180	820	Disabled
1C	High	Low	90	410	Disabled
2C	Low	Float	45	200	Disabled
4C	Float	Float	23	100	Disabled
C/2	High	Float	180	820	C/16
1C	Low	High	90	410	C/8
2C	Float	High	45	200	C/4
4C	High	High	23	100	C/2

Note: Typical conditions = 25°C, V_{CC} = 5.0V.

-ΔV Termination

If the DVEN input is high, the bq2005 samples the voltage at the BAT pin once every 34s. If V_{CELL} is lower than any previously measured value by 12mV ±4mV, fast charge is terminated. The -ΔV test is valid in the range $V_{MCV} - (0.2 * V_{CC}) < V_{CELL} < V_{MCV}$.

Voltage Sampling

Each sample is an average of 16 voltage measurements taken 57µs apart. The resulting sample period (18.18ms) filters out harmonics around 55Hz. This technique minimizes the effect of any AC line ripple that may feed through the power supply from either 50Hz or 60Hz AC sources. Tolerance on all timing is ±16%.

Voltage Termination Hold-off

A hold-off period occurs at the start of fast charging. During the hold-off period, -ΔV termination is disabled. This avoids premature termination on the voltage spikes sometimes produced by older batteries when fast-charge current is first applied. ΔT/Δt, maximum voltage and maximum temperature terminations are not affected by the hold-off period.

ΔT/Δt Termination

The bq2005 samples at the voltage at the TS pin every 34s, and compares it to the value measured two samples earlier. If V_{TEMP} has fallen 16mV ±4mV or more, fast charge is terminated. The ΔT/Δt termination test is valid only when $V_{TCO} < V_{TEMP} < V_{LTF}$.

Temperature Sampling

Each sample is an average of 16 voltage measurements taken 57µs apart. The resulting sample period (18.18ms) filters out harmonics around 55Hz. This technique minimizes the effect of any AC line ripple that may feed through the power supply from either 50Hz or 60Hz AC sources. Tolerance on all timing is ±16%.

Maximum Voltage, Temperature, and Time

Anytime V_{CELL} rises above V_{MCV}, CHG goes high (the LED goes off) immediately. If the bq2005 is not in the voltage hold-off period, fast charging also ceases immediately. If V_{CELL} then falls back below V_{MCV} before t_{MCV} = 1s (maximum), the chip transitions to the Charge Complete state (maximum voltage termination). If V_{CELL} remains above V_{MCV} at the expiration of t_{MCV}, the bq2005 transitions to the Battery Absent state (battery removal). See Figure 4.

Maximum temperature termination occurs anytime the voltage on the TS pin falls below the temperature cut-off threshold V_{TCO}. Charge will also be terminated if V_{TEMP} rises above the minimum temperature fault threshold, V_{LTF}, after fast charge begins.

Maximum charge time is configured using the TM pin. Time settings are available for corresponding charge rates of C/4, C/2, 1C, and 2C. Maximum time-out termination is enforced on the fast-charge phase, then reset, and enforced again on the top-off phase, if selected. There is no time limit on the trickle-charge phase.

Top-off Charge

An optional top-off charge phase may be selected to follow fast charge termination for the C/2 through 4C rates. This phase may be necessary on NiMH or other

5/12

battery chemistries that have a tendency to terminate charge prior to reaching full capacity. With top-off enabled, charging continues at a reduced rate after fast-charge termination for a period of time selected by the TM_1 and TM_2 input pins. (See Table 2.) During top-off, the CC pin is modulated at a duty cycle of 4s active for every 30s inactive. This modulation results in an average rate 1/8th that of the fast charge rate. Maximum voltage, time, and temperature are the only termination methods enabled during top-off.

Pulse-Trickle Charge

Pulse-trickle charging follows the fast charge and optional top-off charge phases to compensate for self-discharge of the battery while it is idle in the charger. The configured pulse-trickle rate is also applied in the charge pending state to raise the voltage of an over-discharged battery up to the minimum required before fast charge can begin.

In the pulse-trickle mode, MOD is active for 260µs of a period specified by the settings of TM1 and TM2. See Table 1. The resulting trickle-charge rate is C/64 when top-off is enabled and C/32 when top-off is disabled. Both pulse trickle and top-off may be disabled by tying TM1 and TM2 to V_{SS}.

Charge Status Indication

Charge status is indicated by the CHG output. The state of the CHG output in the various charge cycle phases is shown in Figure 4 and illustrated in Figure 2.

Temperature status is indicated by the TEMP output. TEMP is in the high state whenever V_{TEMP} is within the temperature window defined by the V_{LTF} and V_{HTF} temperature limits, and is low when the battery temperature is outside these limits.

In all cases, if V_{CELL} exceeds the voltage at the MCV pin, both CHG and TEMP outputs are held high regardless of other conditions. CHG and TEMP may both be used to directly drive an LED.

Pack Sequencing

If both batteries A and B are present when a new charge cycle is started, the charge cycle starts on battery B and B remains the active channel until fast charge termination. Then battery A will be fast charged, followed by a top-off phase on B (if selected), a top-off phase on A (if selected), and then maintenance charging on both. If only battery A is present, the charge cycle begins on A and continues until fast charge termination even if a battery is inserted in channel B in the meantime. A new battery insertion in channel B while A is in the top-off phase terminates top-off on A and begins a new charge cycle on B. If A is configured for or commanded to discharge-before-charge, the discharge may take place while channel B is the active charging channel. When the discharge is complete, if B is still the active channel battery A enters the Charge Pending state until A becomes the active channel.

Charge Current Control

The bq2005 controls charge current through the $MOD_{A,B}$ output pin. The current control circuitry is designed to support implementation of a constant-current switching regulator or to gate an externally regulated current source.

When used in switch mode configuration, the nominal regulated current is:

$$I_{REG} = 0.225V/R_{SNS}$$

Charge current is monitored at the $SNS_{A,B}$ input by the voltage drop across a sense resistor, R_{SNS}, between the low side of the battery pack and ground. R_{SNS} is sized to provide the desired fast charge current.

If the voltage at the $SNS_{A,B}$ pin is less than V_{SNSLO}, the $MOD_{A,B}$ output is switched high to pass charge current to the battery.

When the $SNS_{A,B}$ voltage is greater than V_{SNSHI}, the $MOD_{A,B}$ output is switched low—shutting off charging current to the battery.

$$V_{SNSLO} = 0.04 * V_{CC} \pm 25mV$$

$$V_{SNSHI} = 0.05 * V_{CC} \pm 25mV$$

When used to gate an externally regulated current source, the $SNS_{A,B}$ pin is connected to V_{SS}, and no sense resisitor is required.

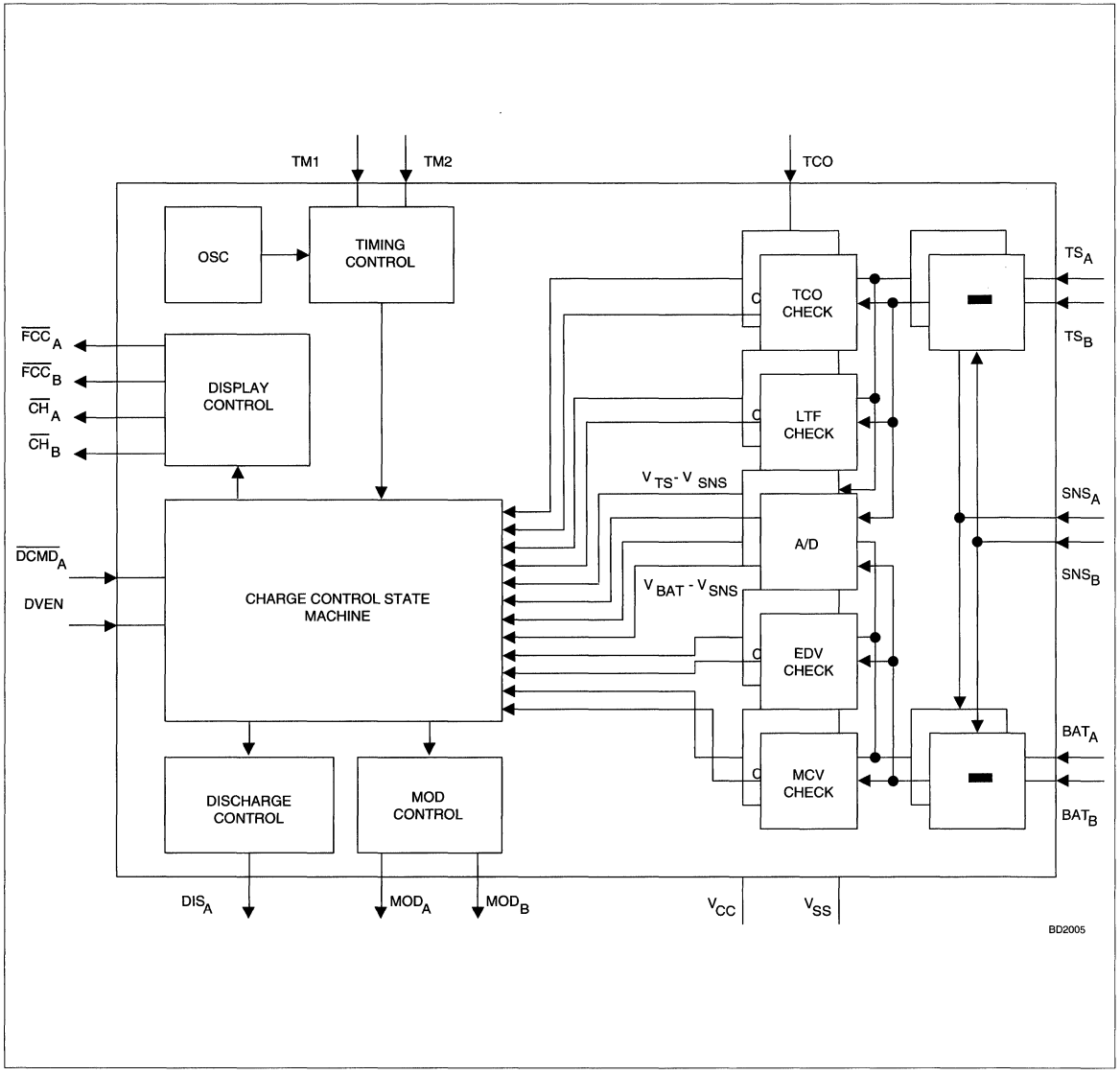


Figure 3. Block Diagram

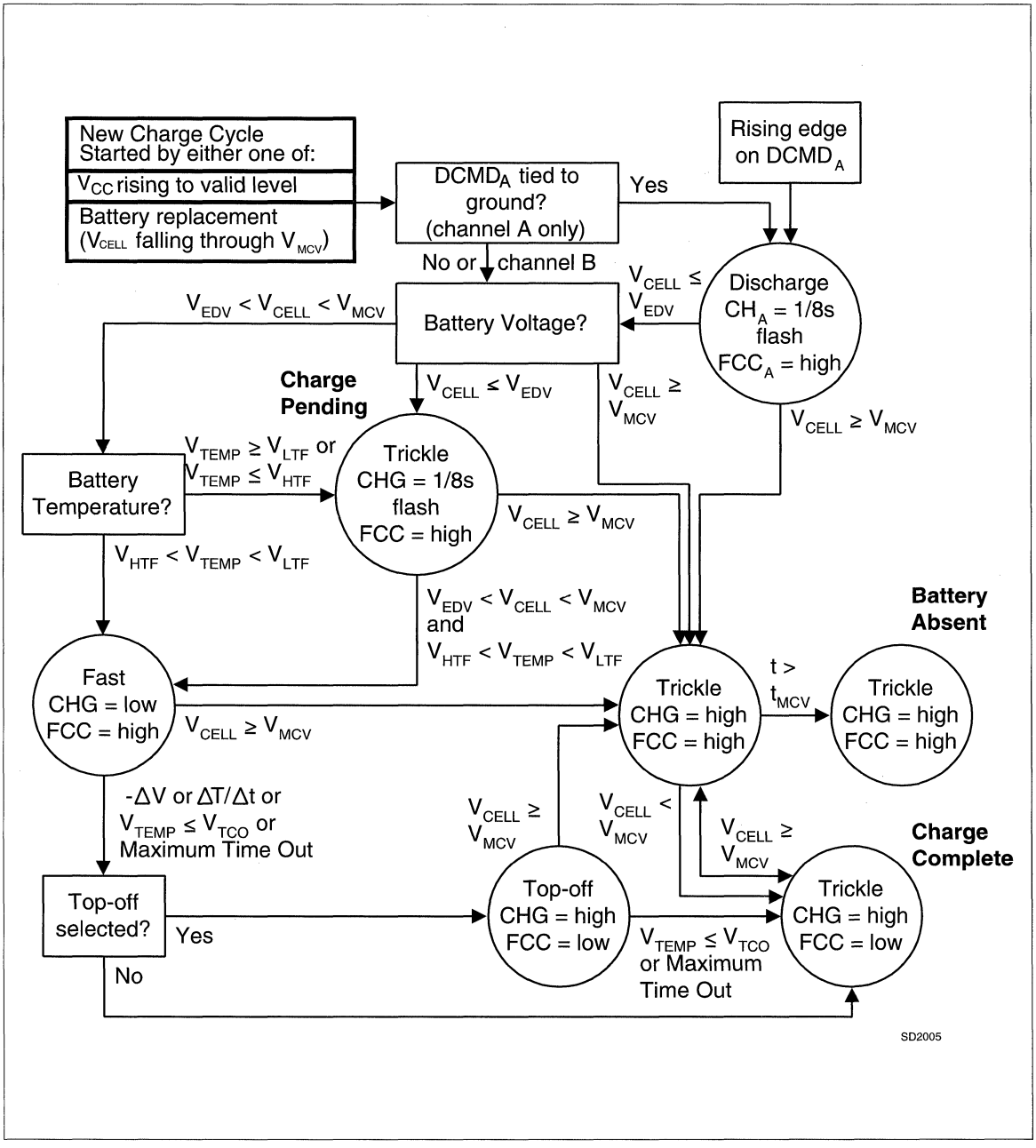


Figure 4. State Diagram

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	-20	+70	°C	Commercial
T_{STG}	Storage temperature	-55	+125	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10 sec max.
T_{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds ($T_A = T_{OPR}$; V_{CC} ±10%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{SNSHI}	High threshold at $SNS_{A,B}$ resulting in $MOD_{A,B}$ = Low	0.05 * V_{CC}	±0.025	V	
V_{SNSLO}	Low threshold at $SNS_{A,B}$ resulting in $MOD_{A,B}$ = High	0.04 * V_{CC}	±0.010	V	
V_{LTF}	Low-temperature fault	0.4 * V_{CC}	±0.030	V	$V_{TEMP} \geq V_{LTF}$ inhibits/ terminates charge
V_{HTF}	High-temperature fault	(1/4 * V_{LTF}) + (3/4 * V_{TCO})	±0.030	V	$V_{TEMP} \leq V_{HTF}$ inhibits charge
V_{EDV}	End-of-discharge voltage	0.475 * V_{CC}	±0.030	V	$V_{CELL} < V_{EDV}$ inhibits fast charge
V_{MCV}	Maximum cell voltage	0.95 * V_{CC}	±0.030	V	$V_{CELL} > V_{MCV}$ inhibits/ terminates charge
V_{THERM}	TS input change for $\Delta T/\Delta t$ detection	16	±4	mV	
$-\Delta V$	BAT input change for $-\Delta V$ detection	12	±4	mV	

Recommended DC Operating Conditions (T_A = 0 to +70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{CELL}	BAT voltage potential	0	-	V_{CC}	V	V_{BAT} - V_{SNS}
V_{BAT}	Battery input	0	-	V_{CC}	V	
V_{TEMP}	TS voltage potential	0	-	V_{CC}	V	V_{TS} - V_{SNS}
V_{TS}	Thermistor input	0	-	V_{CC}	V	
V_{TCO}	Temperature cutoff	0.2 * V_{CC}	-	0.4 * V_{CC}	V	
V_{IH}	Logic input high	2.0	-	-	V	$\overline{DCMD}_A$, DVEN
	Logic input high	V_{CC} - 0.3	-	-	V	TM_1, TM_2
V_{IL}	Logic input low	-	-	0.8	V	$\overline{DCMD}_A$, DVEN
	Logic input low	-	-	0.3	V	TM_1, TM_2
V_{OH}	Logic output high	V_{CC} - 0.5	-	-	V	DIS_A, $MOD_{A,B}$, $I_{OH} \leq$ -5mA
V_{OL}	Logic output low	-	-	0.5	V	DIS_A, $\overline{FCC}_{A,B}$, $\overline{CH}_{A,B}$, $MOD_{A,B}$, $I_{OL} \leq$ 5mA
I_{CC}	Supply current	-	1.0	3.0	mA	Outputs unloaded
I_{OH}	DIS_A, $MOD_{A,B}$ source	-5.0	-	-	mA	@V_{OH} = V_{CC} - 0.5V
I_{OL}	$\overline{DIS}_A$, $\overline{FCC}_{A,B}$, $MOD_{A,B}$, $\overline{CH}_{A,B}$ sink	5.0	-	-	mA	@V_{OL} = V_{SS} + 0.5V
I_L	Input leakage	-	-	±1	µA	DVEN, V = V_{SS} to V_{CC}
		-	-	-400	µA	$\overline{DCMD}_A$, V = V_{SS}
I_{IL}	Logic input low source	-	-	70.0	µA	TM_1, TM_2, V = V_{SS} to V_{SS} + 0.3V
I_{IH}	Logic input high source	-70.0	-	-	µA	TM_1, TM_2, V = V_{CC} - 0.3V to V_{CC}
I_{IZ}	TM_1, TM_2 tri-state open detection	-2.0	-	2.0	µA	TM_1, TM_2 should be left disconnected (floating) for Z logic input state
I_{BAT}	Input current to $BAT_{A,B}$ when battery is removed	-	-	-20	µA	V_{CC} = 5.0V; T_A = 25°C; input should be limited to this current when input exceeds V_{CC}.

Note: All voltages relative to V_{SS}, except as noted.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
$R_{BATA,B}$	Battery A/B input impedance	50	-	-	MΩ
$R_{TSA,B}$	$TS_{A,B}$ input impedance	50	-	-	MΩ
R_{TCO}	TCO input impedance	50	-	-	MΩ
$R_{SNSA,B}$	$SNS_{A,B}$ input impedance	50	-	-	MΩ

Timing (TA = 0 to +70°C; VCC ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{PW}	Pulse width for $\overline{DCMD}_A$, pulse command	1	-	-	µs	Pulse start for discharge-before-charge
d_{FCV}	Time base variation	-16	-	16	%	V_{CC} = 4.5V to 5.5V
t_{REG}	MOD output regulation frequency	-	-	300	kHz	
t_{MCV}	Maximum voltage termination time limit	-	-	1	s	Time limit to distinguish battery removed from charge complete

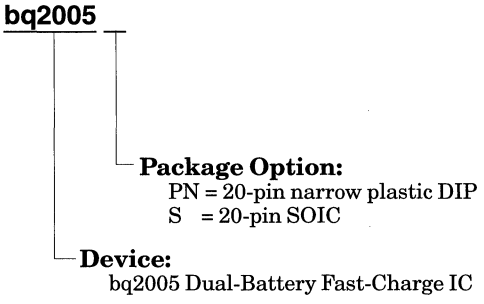
Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
3	9	V_{SNSLO} rating	Was V_{SNSHI} - (0.01 * V_{CC}); is 0.04 * V_{CC}
4	5	Corrected sample period	Was: 32s; Is: 34s
4	5, 9	Corrected -ΔV threshold	Was: 13mV Is: 12mV
4	All	Revised and expanded format of this data sheet	Clarification
5	9	T_{OPR}	Deleted industrial temperature range.

Notes: Change 3 = Sept. 1996 D changes from Nov. 1993 C.
Change 4 = Nov. 1997 E changes from Sept. 1996 D.
Change 5 = June 1999 F changes from Nov. 1997 E.

Ordering Information



Fast-Charge Development System

Control of PNP Power Transistor

Features

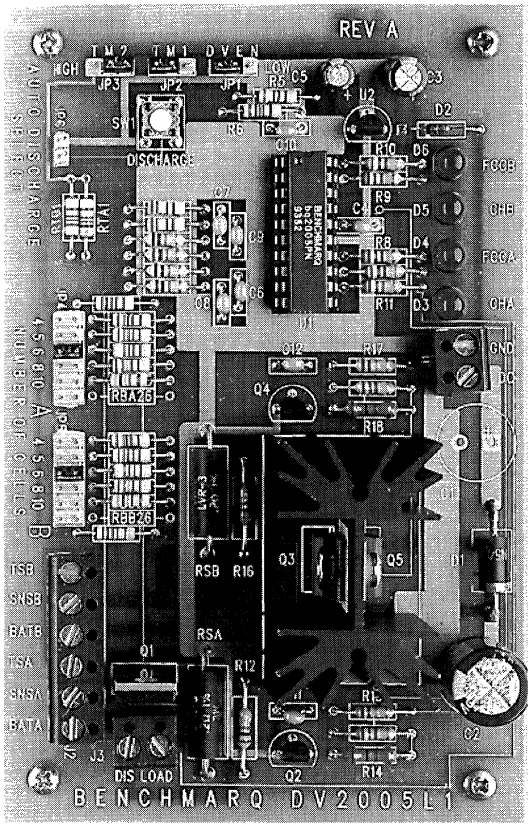
- bq2005 fast-charge control evaluation and development
- Charge current sourced from two on-board linear regulators (up to 3.0 A)
- Fast charge control and conditioning for one or two NiMH and/or NiCd batteries containing 4 to 10 NiCd or NiMH cells; user-configurable for applications that use other numbers of cells
- Sequential charging of two battery packs
- Fast-charge termination by delta temperature/delta time ($\Delta T/\Delta t$), negative delta voltage ($-\Delta V$), maximum temperature, maximum time, and maximum voltage
- $-\Delta V$ enable, hold-off, top-off,trickle rate, maximum charge time, and number of cells are jumper-configurable
- Charging status displayed on LEDs (two for each battery)
- Discharge-before-charge control with push-button switch for battery A
- Selectable pulsed "top-off" charge and trickle charge

General Description

The DV2005L1 Linear Development System provides a development environment for the bq2005 Dual-Battery Fast-Charge IC. The DV2005L1 incorporates a bq2005 and two linear regulators to provide fast charge control for 4 to 10 NiCd or NiMH cells.

Review the bq2005 data sheet and the application note, "Using the bq2005 to Control Fast Charge," before using the DV2005L1 board.

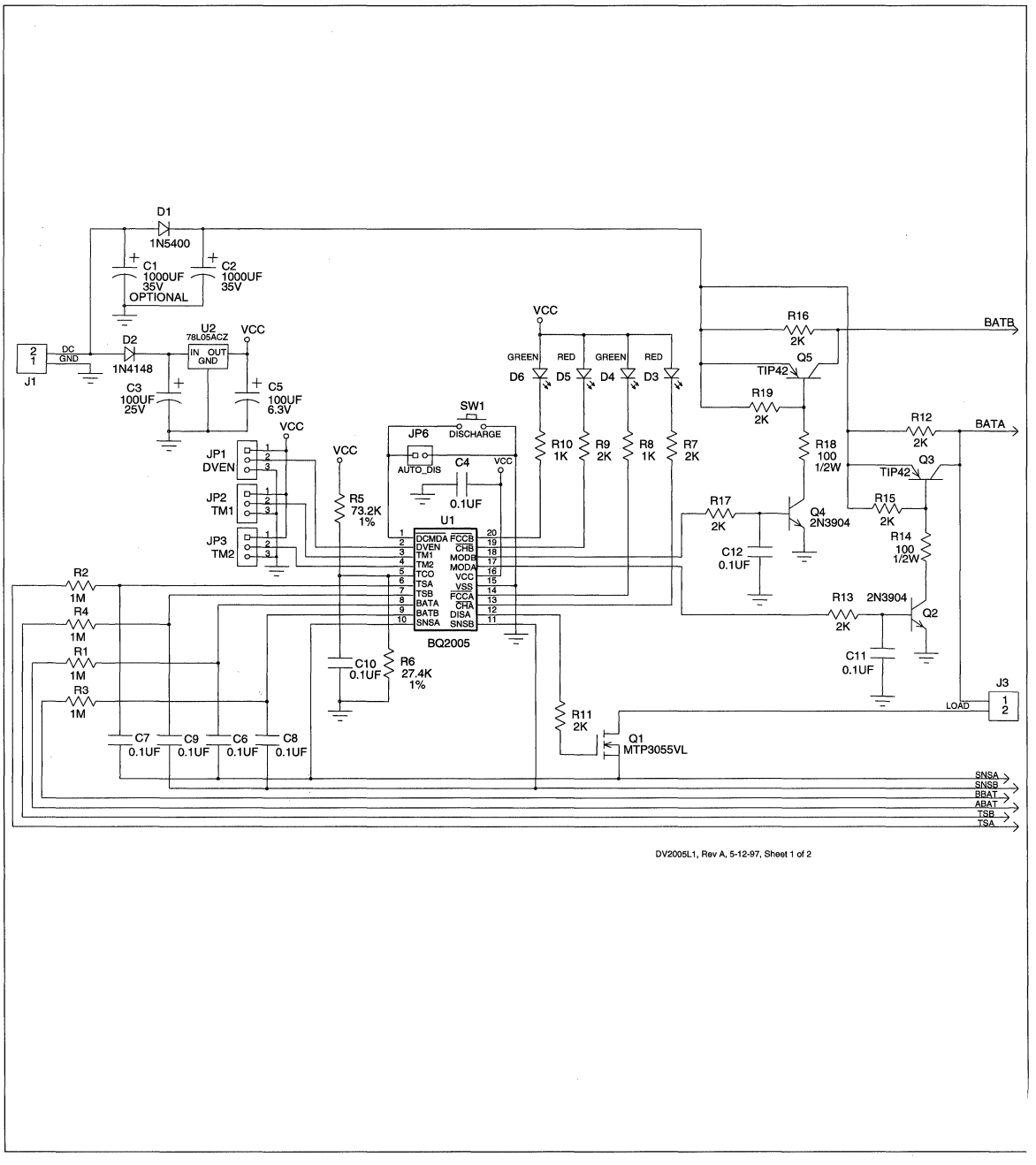
The fast charge is terminated by any of the following: $\Delta T/\Delta t$, $-\Delta V$, maximum temperature, maximum time, and maximum voltage. Jumper settings select the $-\Delta V$ enabled state, and the hold-off, top-off, trickle, and maximum time limits.



The user provides a power supply and batteries. The user configures the DV2005L1 for the number of cells, charge termination, and maximum charge time (with or without top-off), and commands the discharge-before-charge option with the push-button switch SW1.

A full data sheet for this product is available on the Unitrode web site, or you may contact the factory for one.

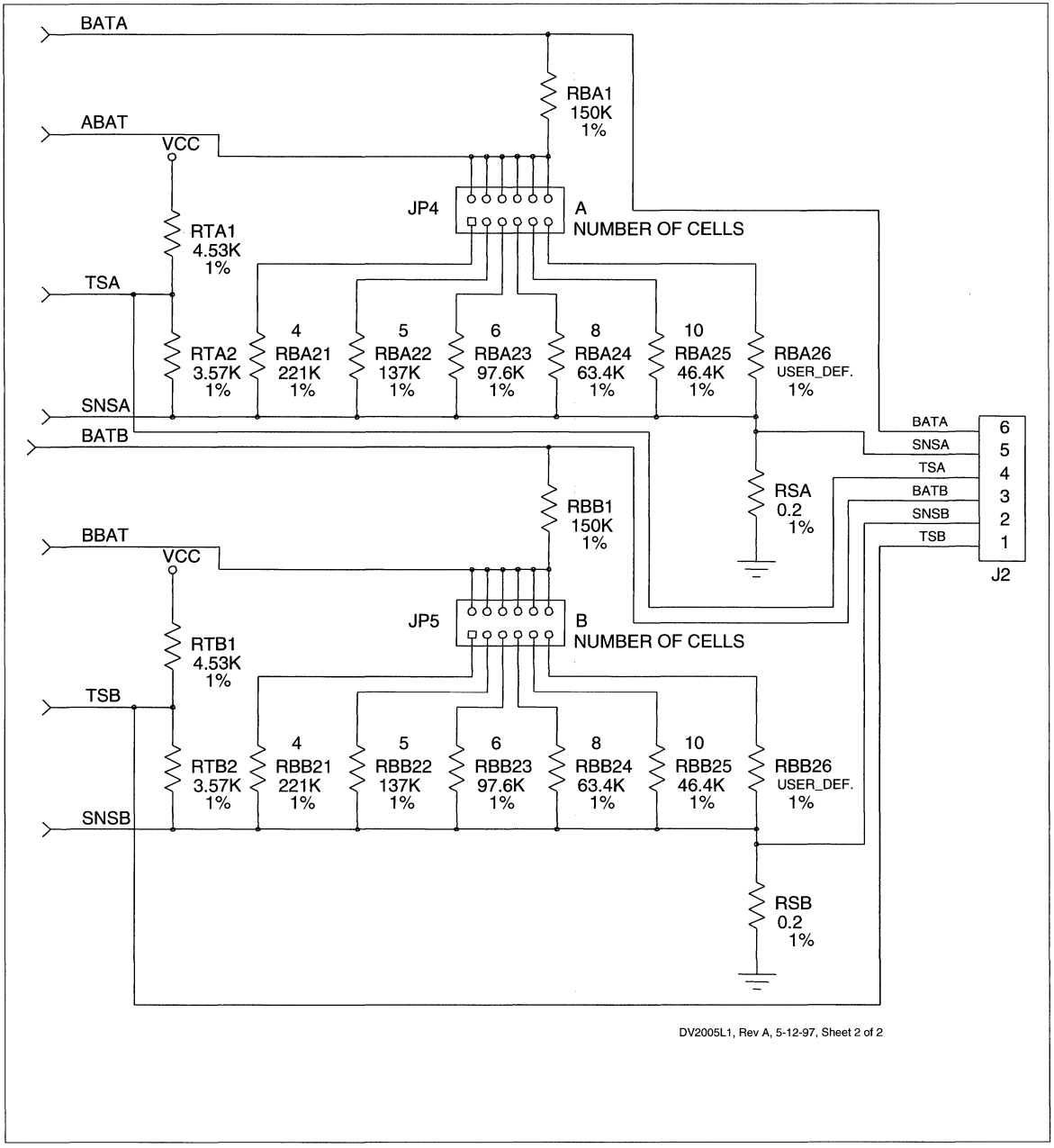
DV2005L1 Board Schematic



DV2005L1, Rev A, 5-12-97, Sheet 1 of 2

Rev. A Board

DV2005L1 Board Schematic (Continued)



Rev. A. Board

UNITRODE

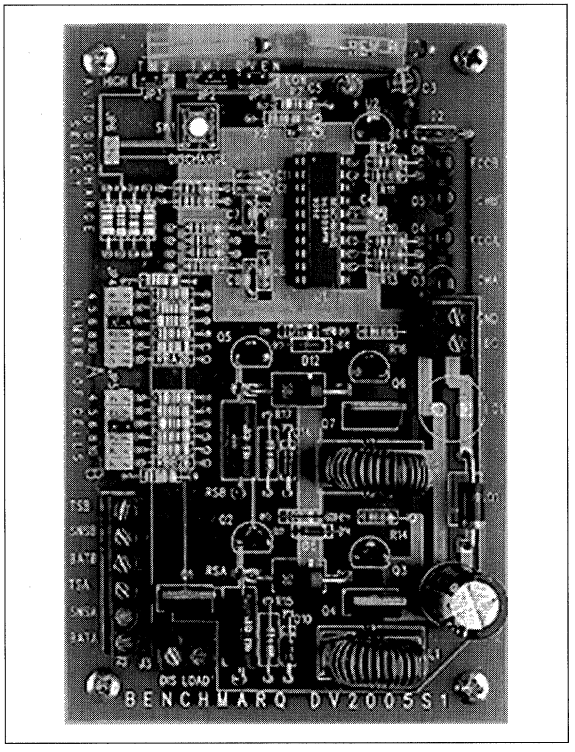
Product Brief **DV2005S1**

Fast-Charge Development System

Control of On-Board P-FET Switch-Mode Regulator

Features

- bq2005 fast-charge control evaluation and development
- Charge current sourced from two on-board switch-mode regulators (up to 3.0 A)
- Fast charge control and conditioning for one or two NiMH and/or NiCd batteries containing 4 to 10 NiCd or NiMH cells; user-configurable for applications that use other numbers of cells
- Sequential charging of two battery packs
- Fast-charge termination by delta temperature/delta time ($\Delta T/\Delta t$), negative delta voltage ($-\Delta V$), maximum temperature, maximum time, and maximum voltage
- $-\Delta V$ enable, hold-off, top-off,trickle rate, maximum charge time, and number of cells are jumper-configurable
- Charging status displayed on LEDs (two for each battery)
- Discharge-before-charge control with push-button switch for battery A
- Integrated switching charge current controller to 300KHz
- Selectable pulsed "top-off" charge and trickle charge



General Description

The DV2005S1 Switching Development System provides a development environment for the bq2005 Dual-Battery Fast-Charge IC. The DV2005S1 incorporates a bq2005 and two buck-type switch-mode regulators to provide fast charge control for 4 to 10 NiCd or NiMH cells.

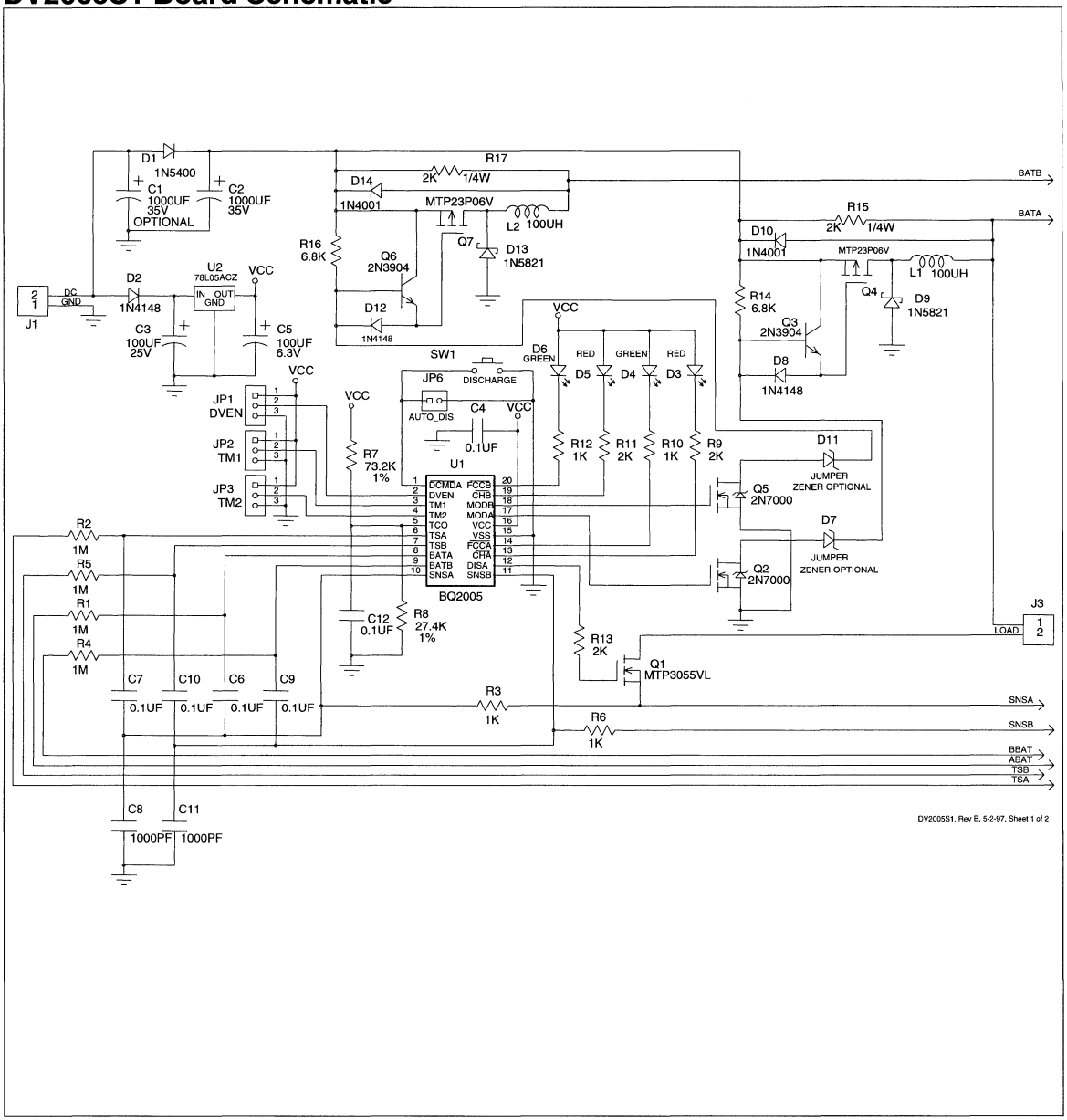
Review the bq2005 data sheet and the application note, "Using the bq2005 to Control Fast Charge," before using the DV2005S1 board.

The fast charge is terminated by any of the following: $\Delta T/\Delta t$, $-\Delta V$, maximum temperature, maximum time, and maximum voltage. Jumper settings select the $-\Delta V$ enabled state, and the hold-off, top-off, trickle, and maximum time limits.

The user provides a power supply and batteries. The user configures the DV2005S1 for the number of cells, charge termination enabled or disabled, and maximum charge time (with or without top-off), and commands the discharge-before-charge option with the push-button switch SW1.

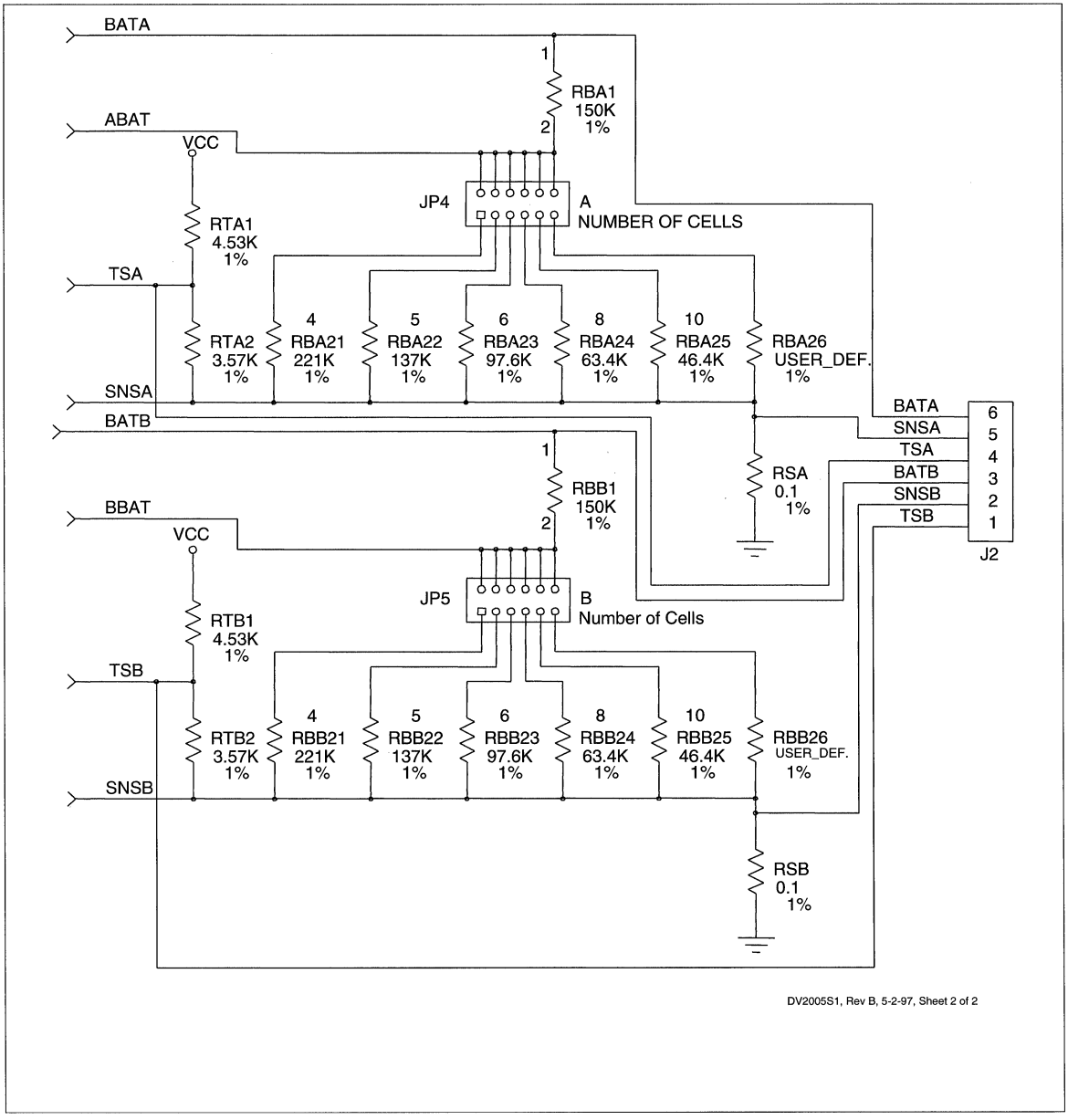
A full data sheet for this product is available on the Unitrode web site, or you may contact the factory for one.

DV2005S1 Board Schematic



Rev. B Board

DV2005S1 Board Schematic (Continued)



Rev. B Board

UNITRODE

bq2007

Fast-Charge IC

Features

- Fast charging and conditioning of NiCd and NiMH batteries
  - Precise charging independent of battery pack number of cells
  - Discharge-before-charge on demand
  - Pulse trickle charge conditioning
  - Battery undervoltage and overvoltage protection
- Built-in 10-step voltage-based charge status monitoring
  - Charge status display options include seven-segment monotonic bargraph and fully decoded BCD digit
  - Display interface options for direct drive of LCD or LED segments
  - Charger state status indicators for pending, discharge, charge, completion, and fault
  - Audible alarm for charge completion and fault conditions
- Charge control flexibility
  - Fast or Standard speed charging
  - Top-off mode for NiMH
  - Charge rates from $\frac{1}{8}$ to 2C (30 minutes to 8 hours)
- Charge termination by:
  - Negative delta voltage ($-\Delta V$)
  - Peak voltage detect (PVD)
  - Maximum voltage
  - Maximum time
  - Maximum temperature
- High-efficiency switch-mode design
  - Ideal for small heat-sensitive enclosures
- 24-pin, 300-mil SOIC or DIP

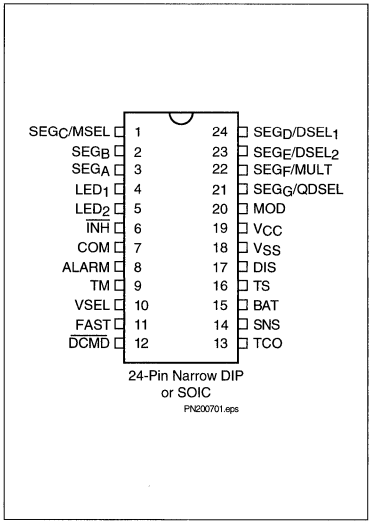
General Description

The bq2007 is a highly integrated monolithic CMOS IC designed to provide intelligent battery charging and charge status monitoring for stand-alone charge systems.

The bq2007 provides a wide variety of charge status display formats. The bq2007 internal charge status monitor supports up to a seven-segment bargraph or a single BCD digit display. The bargraph display indicates up to seven monotonic steps, whereas the BCD digit counts in ten steps of 10% increments. The bq2007 output drivers can direct-drive either an LCD or LED display.

Charge action begins either by application of the charging supply or by replacement of the battery pack. For safety, charging is inhibited until battery temperature and voltage are within configured limits.

Pin Connections



Pin Names

SEG_C/MSEL	Display output segment C/ driver mode select
SEG_B	Display output segment B
SEG_A	Display output segment A
LED_1	Charge status output 1
LED_2	Charge status output 2
$\overline{INH}$	Charge inhibit input
COM	Common LED/LCD output
ALARM	Audio alarm output
TM	Timer mode select
VSEL	Voltage termination select
FAST	Fast charge rate select
$\overline{DCMD}$	Discharge command
TCO	Temperature cutoff
SNS	Sense resistor input
BAT	Battery voltage
TS	Temperature sense
DIS	Discharge control
V_{SS}	System ground
V_{CC}	5.0V ±10% power
MOD	Modulation control
SEG_G/QDSEL	Display output segment G/ charge status display select
SEG_F/MULT	Display output segment F/ multi-cell pack select
SEG_E/$DSEL_2$	Display output segment E/ display select 2
SEG_D/$DSEL_1$	Display output segment D/ display select 1

The acceptable battery temperature range is set by an internal low-temperature threshold and an external high-temperature cutoff threshold. The absolute temperature is monitored as a voltage on the TS pin with the external thermistor network shown in Figure 2.

The bq2007 provides for undervoltage battery protection from high-current charging if the battery voltage is less than the normal end-of-discharge value. In the case of a deeply discharged battery, the bq2007 enters the charge-pending state and attempts trickle-current conditioning of the battery until the voltage increases. Should the battery voltage fail to increase above the discharge value during the undervoltage time-out period, a fault condition is indicated.

Discharge-before-charge may be selected to automatically discharge the battery pack on battery insertion or with a push-button switch. Discharge-before-charge on demand provides conditioning services that are useful to correct or prevent the NiCd voltage depression, or "memory" effect, and also provide a zero capacity reference for accurate capacity monitoring.

After prequalification and any required discharge-before-charge operations, charge action begins until one of the full-charge termination conditions is detected. The bq2007 terminates charging by any of the following methods:

- Negative delta voltage (-ΔV)
- Peak voltage detect (PVD)
- Maximum absolute temperature
- Maximum battery voltage
- Maximum charge time-out

The bq2007 may be programmed for negative delta voltage (-ΔV) or peak voltage detect (PVD) charge termination algorithms. The VSEL input pin selects -ΔV or PVD termination to match the charge rate and battery characteristics.

To provide maximum safety for battery and system, charging terminates based on maximum temperature cutoff (TCO), maximum cutoff voltage (MCV), and maximum time-out (MTO). The TCO threshold is the maximum battery temperature limit for charging. TCO terminates charge action when the temperature sense input voltage on the TS pin drops below the TCO pin voltage threshold. MCV provides battery overvoltage protection by detecting when the battery cell voltage (V_{CELL} = V_{BAT} - V_{SNS}) exceeds the VMCV value and terminates fast charge, standard charge, or top-off charge. The maximum time-out (MTO) termination occurs when the charger safety timer has completed during the active charge state.

The bq2007 indicates charge state status with an audio alarm output option and two dedicated output pins with programmable display options. The DSEL1–2 inputs can select one of the three display modes for the LED1–2 outputs.

Charger status is indicated for:

- Charge pending
- Charge in progress
- Charge complete
- Fault condition

Pin Descriptions

$SEG_{A–G}$ Display output segments A–G

State-of-charge monitoring outputs. QDSEL input selects the bargraph or BCD digit display mode. See Table 3.

MSEL Display driver mode select

Soft-programmed input selects LED or LCD driver configuration at initialization. When MSEL is pulled up to V_{CC}, outputs $SEG_{A–G}$ are LED interface levels; when MSEL is pulled down to V_{SS}, outputs $SEG_{A–G}$ are LCD levels.

$DSEL_1$–$DSEL_2$ Display mode select 1–2

Soft-programmed inputs control the $LED_{1–2}$ charger status display modes at initialization. See Table 2.

MULT Fixed-cell pack select

Soft-programmed input is pulled up to V_{CC} when charging multi-cell packs and is pulled down to V_{SS} for charging packs with a fixed number of cells.

QDSEL State-of-charge display select

The QDSEL input controls the $SEG_{A–G}$ state-of-charge display modes. See Table 3.

LED_1–LED_2 Charger status outputs 1–2

Charger status output drivers for direct drive of LED displays. Display modes are selected by the DSEL input. See Table 2.

$\overline{INH}$ Charge inhibit input

When low, the bq2007 suspends all charge actions, drives all outputs to high impedance, and assumes a low-power operational state. When transitioning from low to high, a charge cycle is initiated. See page 10 for details.

COM **Common LCD/LED output**

Common output for LCD/LED display SEG_{A-G}. Output is high-impedance during initialization to allow reading of soft-programmed inputs $DSEL_1$, $DSEL_2$, MSEL, MULT, and QDSEL.

ALARM **Audio output**

Audio alarm output.

TM **Timer mode select**

TM is a three-level input that controls the settings for charge control functions. See Table 5.

VSEL **Voltage termination select**

This input switches the voltage detect sensitivity. See Table 5.

FAST **Fast charge rate select**

The FAST input switches between Fast and Standard charge rates. See Table 4.

$\overline{DCMD}$ **Discharge command**

The $\overline{DCMD}$ input controls the discharge-before-charge function. A negative-going pulse initiates a discharge action. If $\overline{DCMD}$ is connected to V_{SS}, automatic discharge-before-charge is enabled. See Figure 3.

TCO **Temperature cut-off threshold input**

Minimum allowable battery temperature-sensor voltage. If the potential between TS and SNS is less than the voltage at the TCO input, then any fast charging or top-off charging is terminated.

SNS **Sense resistor input**

SNS controls the switching of MOD output based on an external sense resistor. This provides the lower reference potential for the BAT pin and the TS pin.

BAT **Battery voltage input**

Battery voltage sense input referenced to SNS for the battery pack being charged. This resistor divider network is connected between the positive and the negative terminals of the battery. See Figure 1.

TS **Temperature sense input**

Input referenced to SNS for battery temperature monitoring negative temperature coefficient (NTC) thermistor.

DIS **Discharge control**

DIS is a push-pull output that controls an external transistor to discharge the battery before charging.

V_{SS} **Ground**

V_{CC} **V_{CC} supply input**

MOD **Current-switching control output**

Push/pull output that controls the charging current to the battery. MOD switches high to enable current flow and low to inhibit current flow.

Functional Description

Figure 1 illustrates charge control and display status during a bq2007 charge cycle. Table 1 summarizes the bq2007 operational features. The charge action states and control outputs are given for possible input conditions.

Charge Action Control

The bq2007 charge action is controlled by input pins $\overline{DCMD}$, VSEL, FAST, and TM. When charge action is initiated, the bq2007 enters the charge-pending state, checks for acceptable battery voltage and temperature, and performs any required discharge-before-charge operations. $\overline{DCMD}$ controls the discharge-before-charge function, and VSEL, FAST, and TM select the charger configuration. See Tables 4 and 5.

During charging, the bq2007 continuously tests for charge termination conditions: negative delta voltage, peak voltage detection, maximum time-out, battery over-voltage, and high-temperature cutoff. When the charge state is terminated, a trickle charge continues to compensate for self-discharge and maintain the fully charged condition.

Charge Status Indication

Table 2 summarizes the bq2007 charge status display indications. The charge status indicators include the DIS output, which can be used to indicate the discharge state, the audio ALARM output, which indicates charge completion and fault conditions, and the dedicated status outputs, LED_1 and LED_2.

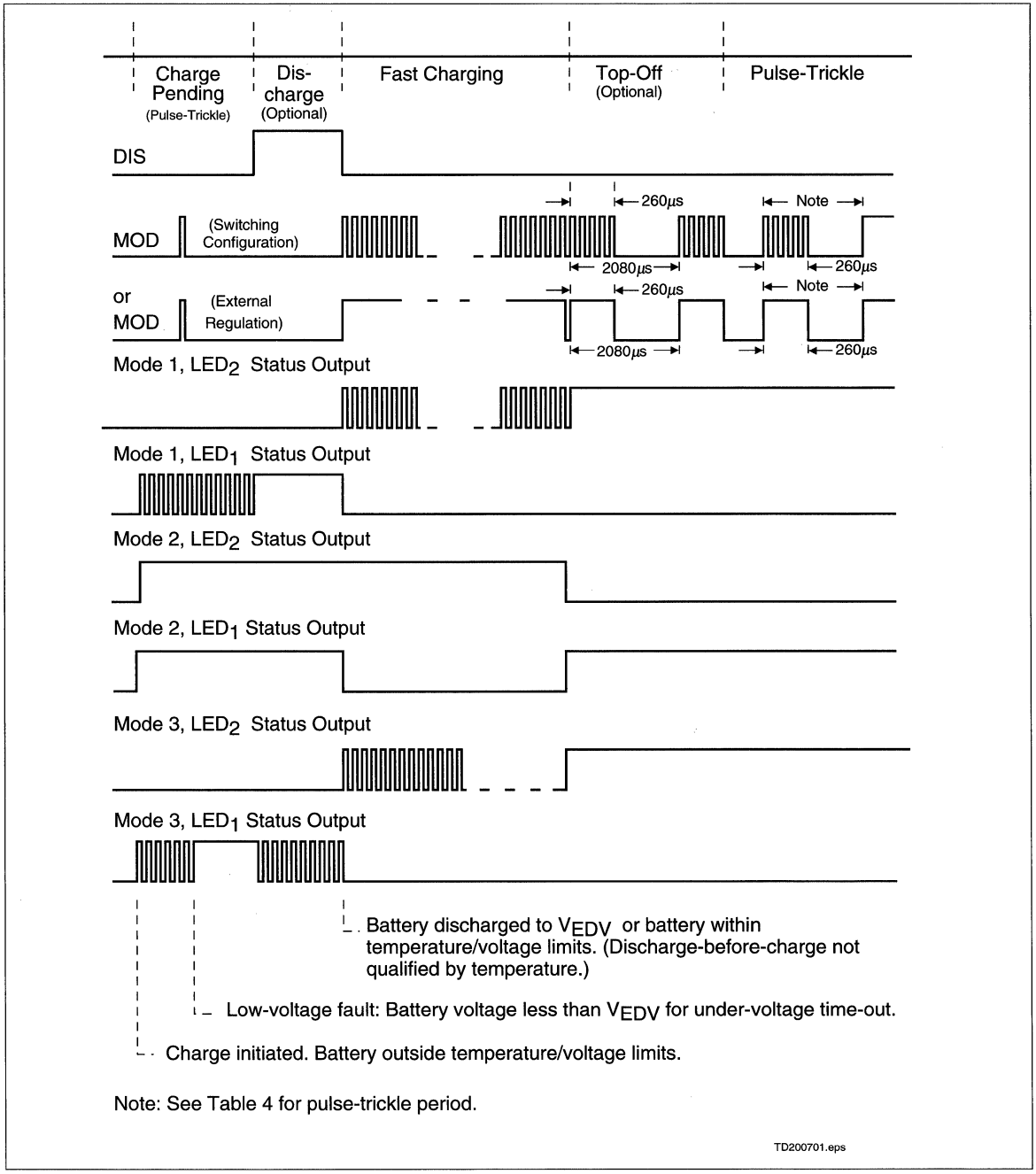


Figure 1. Example Charging Action Events

Outputs LED_{1-2} have three display modes that are selected at initialization by the input pins $DSEL_1$ and $DSEL_2$. The $DSEL_1$ and $DSEL_2$ input pins, when pulled down to V_{SS}, are intended for implementation of a simple two-LED system. LED_2 indicates the precharge status (i.e., charge pending and discharge) and LED_1 indicates the charge status (i.e., charging and completion). $DSEL_1$ pulled up to V_{CC} and $DSEL_2$ pulled down to V_{SS} mode is for implementation of a single tri-color LED such that discharge, charging, and completion each have a unique color. $DSEL_1$ pulled down to V_{SS} and $DSEL_2$ pulled up to V_{CC} allows for fault status information to be displayed.

Audio Output Alarm

The bq2007 audio alarm output generates an audio tone to indicate a charge completion or fault condition. The audio alarm output is a symmetrical duty-cycle AC signal that is compatible with standard piezoelectric alarm elements. A valid battery insertion is indicated by a single high-tone beep of ½-second typical duration. The charge completion and fault conditions are indicated by a 9.5- to 15-second high-tone sequence of ½-second typical duration at a 2-second typical repetition rate.

Charge Status Monitoring

The bq2007 charge status monitor may display the battery voltage or charge safety timer as a percentage of the full-charged condition. These options are selected with the MULT soft-programmed input pin.

When MULT is pulled down to V_{SS}, the battery charge status is displayed as a percentage of the battery voltage, and the single-cell battery voltage at the BAT pin is compared with internal charge voltage reference thresholds. When V_{BAT} is greater than the internal thresholds of V_{20}, V_{40}, V_{60}, or V_{80}, the respective 20%, 40%, 60%, or 80% display outputs are activated. The battery voltage directly indicates 20% charge increments, while the 10% charge increments use a timer that is a function of the charge safety timer.

When MULT is pulled down to V_{SS} and when V_{BAT} exceeds V_{20} during charging, the 20% charge indication is activated and the timer begins counting for a period equal to $\frac{1}{64}$ to $\frac{1}{32}$ of the charge safety time-out period. When the timer count is completed, the 30% charge indication is activated. Should V_{BAT} exceed V_{40} prior to the timer count completion, the charge status monitor activates the 30% and 40% indications. This technique

Table 1. bq2007 Operational Summary

Charge Action State	Conditions	MOD Output	DIS Output
Battery absent	V_{CC} applied and $V_{CELL} \geq V_{MCV}$	Trickle charge per Table 4	Low
Charge initiation	V_{CC} applied or V_{CELL} drops from $\geq V_{MCV}$ to $< V_{MCV}$	-	Low
Discharge-before-charge	$\overline{DCMD}$ high-to-low transition or to V_{SS} on charge initiation and $V_{EDV} < V_{CELL} < V_{MCV}$	Low	High
Charge pending	Charge initiation occurred and $V_{TEMP} \geq V_{LTF}$ or $V_{TEMP} \leq V_{TCO}$ or $V_{CELL} < V_{EDV}$	Trickle charge per Table 4	Low
Fast charging	Charge pending complete and FAST = V_{CC}	Low if $V_{SNS} > 250mV$; high if $V_{SNS} < 200mV$	Low
Standard charging	Charge pending complete and FAST = V_{SS}	Low if $V_{SNS} > 250mV$; high if $V_{SNS} < 200mV$	Low
Charge complete	$-\Delta V$ termination or $V_{TEMP} < V_{TCO}$ or PVD ≥ 0 to -3mV/cell or maximum time-out or $V_{CELL} > V_{MCV}$	-	-
Top-off pending	VSEL = V_{CC}, charge complete and $V_{TEMP} \geq V_{LTF}$ or $V_{TEMP} \leq V_{TCO}$ or $V_{CELL} < V_{EDV}$	Trickle charge per Table 4	Low
Top-off charging	VSEL = V_{CC} and charge complete and time-out not exceeded and $V_{TEMP} > V_{TCO}$ and $V_{CELL} < V_{MCV}$	Activated per V_{SNS} for 73ms of every 585ms	Low
Trickle charging	Charge complete and top-off disabled or top-off complete or pending	Trickle charge per Table 4	Low
Fault	Charge pending state and charge pending time-out (t_{PEND}) complete	Trickle charge per Table 4	Low

Definitions: $V_{CELL} = V_{BAT} - V_{SNS}$; $V_{MCV} = 0.8 * V_{CC}$; $V_{EDV} = 0.262 * V_{CC}$ or $0.4 * V_{CC}$; $V_{TEMP} = V_{TS} - V_{SNS}$; $V_{LTF} = 0.5 * V_{CC}$.

5/14

is used for all the odd percentage charge indications to assure a monotonic charge status display.

When MULT is pulled up to V_{CC}, the bq2007 charge status monitor directly displays $\frac{1}{32}$ of the charge safety timer as a percentage of full charge. This method is recommended over the voltage-based method when charging fixed-cell packs where the battery terminal voltages can vary greatly between packs. This method offers an accurate charge status indication when the battery is fully discharged. When using the timer-based method, discharge-before-charge is recommended.

During discharge with MULT pulled down to V_{SS}, the charge status monitor indicates the percentage of the battery voltage by comparing V_{BAT} to the internal discharge voltage reference thresholds. In BCD format, the discharge thresholds V_{80}, V_{60}, V_{40}, and V_{20} correspond to a battery charge state indication of 90%, 70%, 50%, and 30%, respectively. In bargraph format, the same discharge thresholds correspond to a battery charge state indication of 90%, 60%, 40%, and 30%, respectively. Differences in the battery charge state indications are due to the finer granularity of the BCD versus the bargraph format.

During discharge and when MULT is pulled up to V_{CC}, the state-of-charge monitor BCD format displays the discharge condition, letter "d," whereas the bargraph format has no indication.

The charge status display is blanked during the charge pending state and when the battery pack is removed.

Charge Status Display Modes

The bq2007 charge status monitor can be displayed in two modes summarized in Table 3. The display modes are a seven-segment monotonic bargraph or a seven-segment BCD single-digit format. When QDSEL is pulled down to V_{SS}, pins SEG_{A-G} drive the decoded seven segments of a single BCD digit display, and when QDSEL is pulled up to V_{CC}, pins SEG_{A-G} drive the seven segments of a bargraph display.

In the bargraph display mode, outputs SEG_{A-G} allow options for a three-segment to seven-segment bargraph display. The three-segment charge status display uses outputs SEG_B, SEG_D, and SEG_F for 30%, 60%, and 90% charge indications, respectively. The four-segment charge status display uses outputs SEG_A, SEG_C, SEG_D, and SEG_E for 20%, 40%, 60%, and 80% indications, respectively. The seven-segment charge status monitor uses all segments.

The BCD display mode drives pins SEG_{A-G} with the decoded seven-segment single-digit information. The display indicates in 10% increments from a BCD zero count at charge initiation to a BCD nine count indicating 90% charge capacity. Charge completion is indicated by the letter "F," a fault condition by the letter "E," and the discharge condition by the letter "d." See Table 3.

Table 2. bq2007 Charge Status Display Summary

Mode	Charge Action State	LED_1	LED_2	DIS	ALARM
$DSEL_1$ = L $DSEL_2$ = L (Mode 1)	Battery absent	0	0	0	0
	Charge pending (temp. limit, low voltage)	0	Flashing	0	0
	Discharge in progress	0	1	1	0
	Charging	Flashing	0	0	0
	Charge complete	1	0	0	High tone
	Fault (low-voltage time-out)	0	0	0	High tone
$DSEL_1$ = H $DSEL_2$ = L (Mode 2)	Battery absent	0	0	0	0
	Discharge in progress, pending	1	1	1	0
	Charging	1	0	0	0
	Charge complete	0	1	0	High tone
	Fault (low-voltage time-out)	0	0	0	High tone
$DSEL_1$ = L $DSEL_2$ = H (Mode 3)	Battery absent	0	0	0	0
	Charge pending (temp. limit, low voltage)	0	Flashing	0	0
	Discharge in progress	0	Flashing	1	0
	Charging	Flashing	0	0	0
	Charge complete	1	0	0	High tone
	Fault (low-voltage time-out)	0	1	0	High tone

Note: 1 = on; 0 = off; L = pulled down to V_{SS}; H = pulled up to V_{CC}.

6/14

Display Driver Modes

The bq2007 is designed to interface with LCD or LED type displays. The LED signal levels are driven when the MSEL soft-programmed input is pulled to V_{CC} at initialization. The output pin COM is the common anode connection for LED SEG_{A-G}.

The LCD interface mode is enabled when the MSEL soft-programmed input pin is pulled to V_{SS} at initialization. An internal oscillator generates all the timing signals required for the LCD interface. The output pin COM is the common connection for static direct-driving of the LCD display backplane and is driven with an AC signal at the frame period. When enabled, each of the SEG_{A-G} pins is driven with the correct-phase AC signal to activate the LCD segment. In bargraph or BCD mode, output pins SEG_{A-G} interface to LED or LCD segments.

Battery Voltage and Temperature Measurement

The battery voltage and temperature are monitored within set minimum and maximum limits. When MULT is pulled up to V_{CC}, battery voltage is sensed at the BAT pin by a resistive voltage divider that divides the terminal voltage between 0.262 * V_{CC} (V_{EDV}) and 0.8 * V_{CC} (V_{MCV}). The bq2007 charges multi-cell battery packs from a minimum of N cells, to a maximum of 1.5 * N cells. The battery voltage divider is set to the minimum cell battery pack (N) by the BAT pin voltage divider ratio equation:

$$\frac{R1}{R2} = \left(\frac{N}{1.33}\right) - 1$$

When MULT is pulled down to V_{SS}, tighter charge voltage limits and voltage-based charge status display are selected. This is recommended for charging packs with a fixed number of cells where the battery voltage divider range is between 0.4 * V_{CC} (V_{EDV}) and 0.8 * V_{CC}

Table 3. bq2007 Charge Status Display Summary

Mode	Display Indication	SEG_A	SEG_B	SEG_C	SEG_D	SEG_E	SEG_F	SEG_G
QDSEL = H	20% charge	1	0	0	0	0	0	0
	30% charge	1	1	0	0	0	0	0
	40% charge	1	1	1	0	0	0	0
	60% charge	1	1	1	1	0	0	0
	80% charge	1	1	1	1	1	0	0
	90% charge	1	1	1	1	1	1	0
	Charge complete	1	1	1	1	1	1	1
QDSEL = L	0% charge—digit 0	1	1	1	1	1	1	0
	10% charge—digit 1	0	1	1	0	0	0	0
	20% charge—digit 2	1	1	0	1	1	0	1
	30% charge—digit 3	1	1	1	1	0	0	1
	40% charge—digit 4	0	1	1	0	0	1	1
	50% charge—digit 5	1	0	1	1	0	1	1
	60% charge—digit 6	1	0	1	1	1	1	1
	70% charge—digit 7	1	1	1	0	0	1	0
	80% charge—digit 8	1	1	1	1	1	1	1
	90% charge—digit 9	1	1	1	1	0	1	1
	Charge complete—letter F	1	0	0	0	1	1	1
	Fault condition—letter E	1	0	0	1	1	1	1
	Discharge—letter d	0	1	1	1	1	0	1

Note: 1 = on; 0 = off; L = pulled down to V_{SS}; H = pulled up to V_{CC}.

7/14

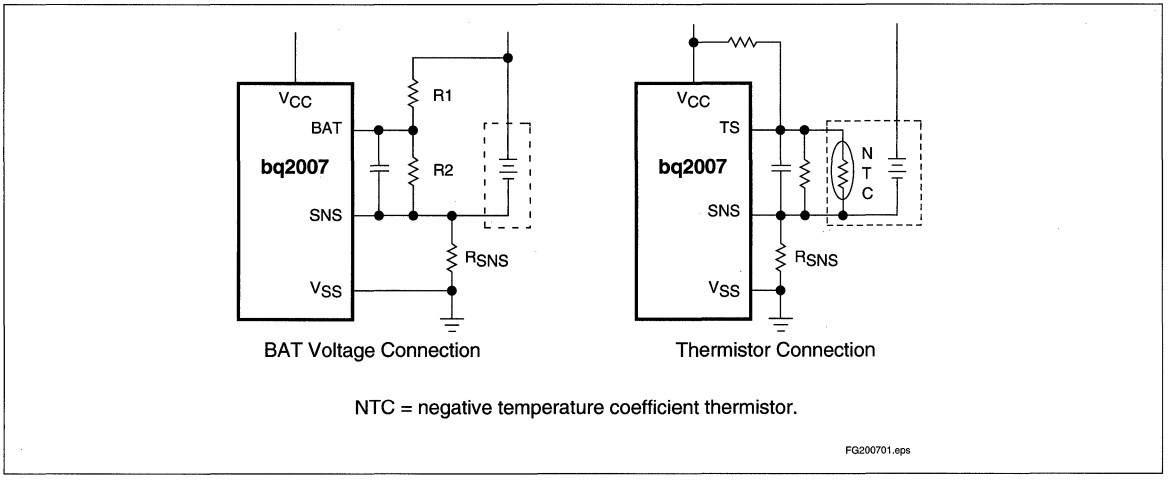


Figure 2. Voltage and Temperature Limit Measurement

(V_{MCV}). The bq2007 charges fixed-cell battery packs of N cells. The battery voltage divider is set by the divider ratio equation:

$$\frac{R1}{R2} = \left(\frac{N}{2}\right) - 1$$

Note: The resistor-divider network impedance should be above 200KΩ to protect the bq2007.

When battery temperature is monitored for maximum and minimum allowable limits, the bq2007 requires that the thermistor used for temperature measurement have a negative temperature coefficient. See Figure 2.

Temperature and Voltage Prequalifications

For charging to be initiated, the battery temperature must fall within predetermined acceptable limits. The voltage on the TS pin (V_{TS}) is compared to an internal low-temperature fault threshold (V_{LTF}) of (0.5 * V_{CC}) and the high temperature cutoff voltage (V_{TCO}) on the TCO pin. For charging to be initiated, V_{TS} must be less than V_{LTF} and greater than V_{TCO}. Since V_{TS} decreases as temperature increases, the TCO threshold should be selected to be lower than 0.5 * V_{CC} for proper operation. If the battery temperature is outside these limits, the bq2007 holds the charge-pending state with a pulse trickle current until the temperature is within limits. Temperature prequalification and termination is disabled if V_{TS} is greater than 0.8 * V_{CC}. See Figure 2.

The bq2007 provides undervoltage battery protection by trickle-current conditioning of a battery that is below the low-voltage threshold (V_{EDV}). The battery voltage (V_{CELL}) is compared to the low-voltage threshold (V_{EDV}) and charge will be inhibited if V_{CELL} < V_{EDV}. The condition trickle current and fault time-out are a percentage of the fast charge rate and maximum time-out (MTO).

Initiating Charge Action and Discharge-Before-Charge

A charge action is initiated under control of: (1) battery insertion or (2) power applied. Battery insertion is detected when the voltage at the BAT pin falls from above V_{MCV} to below V_{MCV}. Power applied is detected by the rising edge of V_{CC} when a battery is inserted.

Discharge-before-charge (see Figure 3) is initiated automatically on application of power or battery insertion when $\overline{DCMD}$ is connected to V_{SS}. Discharge-on-demand is initiated by a negative-going pulse on the $\overline{DCMD}$ pin

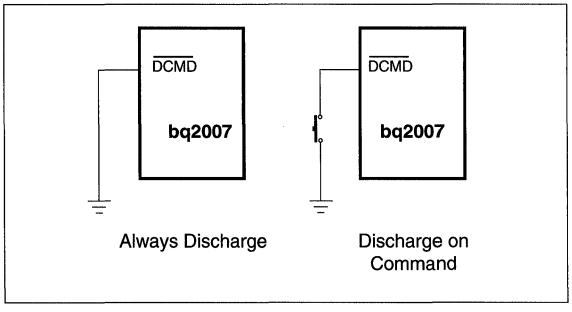


Figure 3. Discharge-Before-Charge

Table 4. bq2007 Charge Action Control Summary

FAST Input State	TM Input State	Time-out Period (min)	MOD Duty Cycle	Hold-off period (sec)	Trickle Rep Rate -ΔV C/32	Trickle Rep Rate PVD C/64
V_{SS}	Float	640 (C/8)	25%	2400	219Hz	109Hz
V_{SS}	V_{SS}	320 (C/4)	25%	1200	109Hz	55Hz
V_{SS}	V_{CC}	160 (C/2)	25%	600	55Hz	27Hz
V_{CC}	Float	160 (C/2)	100%	600	219Hz	109Hz
V_{CC}	V_{SS}	80 (C)	100%	300	109Hz	55Hz
V_{CC}	V_{CC}	40 (2C)	100%	150	55Hz	27Hz

regardless of charging activity. The $\overline{DCMD}$ pin is internally pulled up to V_{CC}; therefore, not connecting this pin results in disabling the discharge-before-charge function. When the discharge begins, the DIS output goes high to activate an external transistor that connects a load to the battery. The bq2007 terminates discharge-before-charge by detecting when the battery cell voltage is less than or equal to the end-of-discharge voltage (V_{EDV}).

Charge State Actions

Once the required discharge is completed and temperature and voltage prequalifications are met, the charge state is initiated. The charge state is configured by the VSEL, FAST, and TM input pins. The FAST input selects between Fast and Standard charge rates. The Standard charge rate is ¼ of the Fast charge rate, which is accomplished by disabling the regulator for a period of 286µs of every 1144µs (25% duty cycle). In addition to throttling back the charge current, time-out and hold-off safety time are increased accordingly. See Table 4.

The VSEL input selects the voltage termination method. The termination mode sets the top-off state and trickle charge current rates. The TM input selects the Fast charge rate, the Standard rate, and the corresponding charge times. Once charging begins at the Fast or Standard rate, it continues until terminated by any of the following conditions:

- Negative delta voltage (-ΔV)
- Peak voltage detect (PVD)
- Maximum temperature cutoff (TCO)
- Maximum time-out (MTO)
- Maximum cutoff voltage (MCV)

Voltage Termination Hold-off

To prevent early termination due to an initial false peak battery voltage, the -ΔV and PVD terminations are disabled during a short "hold-off" period at the start of charge. During the hold-off period when fast charge is selected (FAST = 1), the bq2007 will top off charge to prevent excessive overcharging of a fully charged battery. Once past the initial charge hold-off time, the termination is enabled. TCO and MCV terminations are not affected by the hold-off time.

-ΔV or PVD Termination

Table 5 summarizes the two modes for full-charge voltage termination detection. When $V_{SEL} = V_{SS}$, negative delta voltage detection occurs when the voltage seen on the BAT pin falls 12mV (typical) below the maximum sampled value. $V_{SEL} = V_{CC}$ selects peak voltage detect termination and the top-off charge state. PVD termination occurs when the BAT pin voltage falls 6mV per cell below the maximum sampled value. When charging a battery pack with a fixed number of cells, the -ΔV and PVD termination thresholds are -6mV and 0 to -3mV per cell, respectively. The valid battery voltage range on V_{BAT} for -ΔV or PVD termination is from 0.262 * V_{CC} to 0.8 * V_{CC}.

Table 5. VSEL Configuration

VSEL	Detection Method	Top-Off	Pulse Trickle Rate
V_{SS}	-ΔV	Disabled	C/32
V_{CC}	PVD	Enabled	C/64

Maximum Temperature, Maximum Voltage, and Maximum Time Safety Terminations

The bq2007 also terminates charge action for maximum temperature cutoff (TCO), maximum cutoff voltage (MCV), and maximum time-out (MTO). Temperature is monitored as a voltage on the TS pin (V_{TS}), which is compared to an internal high-temperature cutoff threshold of V_{TCO}. The TCO reference level provides the maximum limit for battery temperature during charging. MCV termination occurs when $V_{CELL} > V_{MCV}$. The maximum time-out (MTO) termination is when the charger safety timer countdown has completed during the active charge state. If the MTO, MCV, or TCO limit is exceeded during Fast charge, Standard charge, or top-off states, charge action is terminated.

Top-Off and Pulse Trickle Charging

The bq2007 provides a post-detection timed charge capability called top-off to accommodate battery chemistries that may have a tendency to terminate charge prior to achieving full capacity. When $V_{SEL} = V_{CC}$, the top-off state is selected; charging continues after Fast charge termination for a period equal to the time-out value. In top-off mode, the Fast charge control cycle is modified so that MOD is activated for a pulse output of 73ms of every 585ms. This results in a rate $\frac{1}{8}$ that of the Fast charge rate. Top-off charge is terminated by maximum temperature cutoff (TCO), maximum cutoff voltage (MCV), or maximum time-out termination.

Pulse trickle is used to compensate for self-discharge while the battery is idle and to condition a depleted low-voltage battery to a valid voltage prior to high-current charging. The battery is pulse trickle charged when Fast, Standard, or top-off charge is not active. The MOD output is active for a period of 286µs of a period specified in Table 4. This results in a trickle rate of $\frac{1}{64}$ for PVD and $\frac{1}{32}$ when -ΔV is enabled.

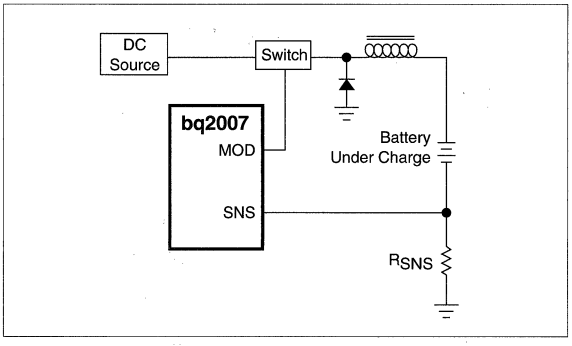


Figure 4. Constant-Current Switching Regulation

Charge Inhibit

Fast charge, top-off, and pulse trickle may be inhibited by using the $\overline{INH}$ input pin. When low, the bq2007 suspends all charge activity, drives all outputs to high impedance, and assumes a low-power operational state. When $\overline{INH}$ returns high, a fast-charge cycle is qualified and begins as soon as conditions allow.

Charge Current Control

The bq2007 controls charge current through the MOD output pin. In a frequency-modulated buck regulator configuration, the control loop senses the voltage at the SNS pin and regulates to maintain it between 0.04 * V_{CC} and 0.05 * V_{CC}. The nominal regulated current is $I_{REG} = 0.225V/R_{SNS}$. See Figure 4.

MOD pin is switched high or low depending on the voltage input to the SNS pin. If the voltage at the SNS pin is less than V_{SNSLO} (0.04 * V_{CC} nominal), the MOD output is switched high to gate charge current through the inductor to the battery. When the SNS voltage is greater than V_{SNSHI} (0.05 * V_{CC} nominal), the MOD output is switched low-shutting off charge current from the supply. The MOD pin can be used to gate an external charging current source. When an external current source is used, no sense resistor is required, and the SNS pin is connected to V_{SS}.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	-20	+70	°C	Commercial
T_{STG}	Storage temperature	-40	+85	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds ($T_A = T_{OPR}$; V_{CC} = 5V ± 10%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{SNSHI}	High threshold at SNS resulting in MOD = Low	0.05 * V_{CC}	±25	mV	
V_{SNSLO}	Low threshold at SNS resulting in MOD = High	0.04 * V_{CC}	±10	mV	
V_{LTF}	TS pin low-temperature threshold	0.5 * V_{CC}	±30	mV	SNS = 0V
V_{HTF}	TS pin high-temperature threshold	V_{TCO}	±30	mV	SNS = 0V
V_{EDV}	End-of-discharge voltage MULT is pulled up to V_{CC}	0.262 * V_{CC}	±30	mV	SNS = 0V
	End-of-discharge voltage MULT is pulled down to V_{SS}	0.4 * V_{CC}	±30	mV	SNS = 0V
V_{MCV}	BAT pin maximum cell voltage threshold	0.8 * V_{CC}	±30	mV	SNS = 0V
V_{20}	20% state-of-charge voltage threshold at the BAT pin	$^{187}/_{320}$ * V_{CC}	±30	mV	Fast or standard charge state; MULT pulled to V_{SS}
V_{40}	40% state-of-charge voltage threshold at the BAT pin	$^{191}/_{320}$ * V_{CC}	±30	mV	Fast or standard charge state; MULT pulled to V_{SS}
V_{60}	60% state-of-charge voltage threshold at the BAT pin	$^{195}/_{320}$ * V_{CC}	±30	mV	Fast or standard charge state; MULT pulled to V_{SS}
V_{80}	80% state-of-charge voltage threshold at the BAT pin	$^{203}/_{320}$ * V_{CC}	±30	mV	Fast or standard charge state; MULT pulled to V_{SS}
V_{20}	20% state-of-charge voltage threshold at the BAT pin	$^{158}/_{320}$ * V_{CC}	±30	mV	Discharge-before-charge state; MULT pulled to V_{SS}; DIS = 1
V_{40}	40% state-of-charge voltage threshold at the BAT pin	$^{163}/_{320}$ * V_{CC}	±30	mV	Discharge-before-charge state; MULT pulled to V_{SS}; DIS = 1
V_{60}	60% state-of-charge voltage threshold at the BAT pin	$^{167}/_{320}$ * V_{CC}	±30	mV	Discharge-before-charge state; MULT pulled to V_{SS}; DIS = 1
V_{80}	80% state-of-charge voltage threshold at the BAT pin	$^{171}/_{320}$ * V_{CC}	±30	mV	Discharge-before-charge state; MULT pulled to V_{SS}; DIS = 1

Recommended DC Operating Conditions (T_A = 0 to +70°C)

Symbol	Parameter	inimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	10%
V_{BAT}	Voltage on BAT pin	0	-	V_{CC}	V	
V_{TS}	Voltage on TS pin	0	-	V_{CC}	V	Thermistor input
V_{TCO}	Temperature cutoff on TCO	0	-	0.5 * V_{CC}	V	Note 2
V_{CELL}	Battery voltage potential	0	-	V_{CC}	V	V_{BAT} - V_{SNS}
V_{TEMP}	Voltage potential on TS	0	-	V_{CC}	V	V_{TS} - V_{SNS}
V_{IH}	Logic input high	2.0	-	-	V	$\overline{DCMD}$, FAST, VSEL, $\overline{INH}$
	Tri-level input high	V_{CC} - 0.3	-	-	V	TM
V_{IL}	Logic input low	-	-	0.8	V	$\overline{DCMD}$, FAST, VSEL, $\overline{INH}$
	Tri-level input low	-	-	0.3	V	TM
V_{OH}	Logic output high	V_{CC} - 0.8	-	-	V	DIS, LED_{1-2}, SEG_{A-G} @ I_{OH} = -10mA; MOD @ I_{OH} = -5mA
V_{OL}	Logic output low	-	-	0.8	V	DIS, LED_{1-2}, SEG_{A-G} @ I_{OL} = 10mA; MOD @ I_{OL} = 5mA
V_{OHCOM}	COM output	V_{CC} - 0.8	-	-	V	@ I_{OHCOM} = -40mA
I_{OHCOM}	COM source	-40	-	-	mA	@ V_{OHCOM} = V_{CC} - 0.8V
I_{CC}	Supply current	-	1	2.5	mA	No output load
I_{OH}	DIS, LED_{1-2}, SEG_{A-G} source	-10	-	-	mA	@V_{OH} = V_{CC} - 0.8V
I_{OH}	MOD	-5	-	-	mA	@V_{OH} = V_{CC} - 0.8V
I_{OL}	DIS, LED_{1-2}, SEG_{A-G} sink	10	-	-	mA	@V_{OL} = V_{SS} + 0.8V
I_{OL}	MOD	5	-	-	mA	@V_{OL} = V_{SS} + 0.8V
I_{IZ}	Tri-state inputs floating for Z state	-2.0	-	2.0	µA	TM
I_L	Input leakage	-	-	±1	µA	$\overline{INH}$, VSEL, V = V_{SS} to V_{CC}
	Input leakage	50	-	400	µA	$\overline{DCMD}$, FAST, V = V_{SS} to V_{CC}
I_{IL}	Logic input low current	-	-	70	µA	TM, V = V_{SS} to V_{SS} + 0.3V
I_{IH}	Logic input high current	-70	-	-	µA	TM, V = V_{CC} - 0.3V to V_{CC}

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
R_I	DC input impedance: pins TS, BAT, SNS, TCO	50	-	-	MΩ	
R_{PROG}	Soft-programmed pull-up resistor	150	-	200	KΩ	MSEL, $DSEL_1$, $DSEL_2$, MULT, QDSEL; resistor value ± 10% tolerance
R_{FLT}	Float state external resistor	-	5	-	MΩ	TM

Timing (TA = 0 to +70°C; VCC ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
d_{FCV}	Deviation of fast charge safety time-out	0.84	1.0	1.16	-	At V_{CC} = ±10%, T_A = 0 to 60°C; see Table 3
t_{REG}	MOD output regulation frequency	-	-	300	kHz	Typical regulation range; V_{CC} = 5.0V
t_{PEND}	Charge pending time-out	-	25	-	%	Ratio of fast charge time-out; see Table 4.
F_{COM}	Common LCD backplane frequency	-	73	-	Hz	LCD segment frame rate
F_{ALARM}	Alarm frequency output	-	3500	-	kHz	High tone
t_{PW}	Pulse width for $\overline{DCMD}$ and $\overline{INH}$ pulse command	1	-	-	µs	Signal valid time
t_{MCV}	Valid period for V_{CELL} > V_{MCV}	0.5	-	1	sec	If $V_{CELL} \geq V_{MCV}$ for t_{MCV} during charge or top-off, then a transition is recognized as a battery replacement.

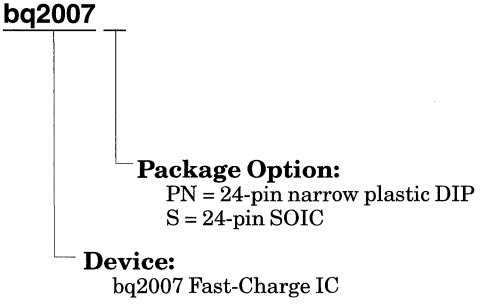
Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	11	V_{SNSLO} Rating	Was V_{SNSHI} - (0.01 * V_{CC}); is 0.04 * V_{CC}

Note: Change 1 = Sept. 1996 B changes from Dec. 1995.

Ordering Information



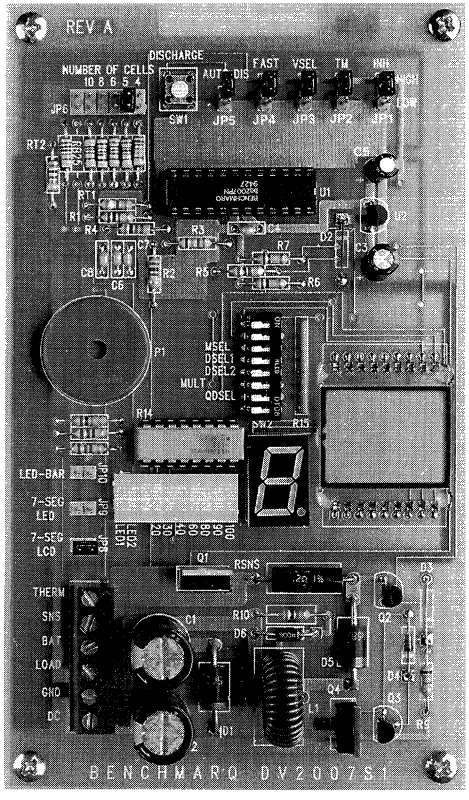
Product Brief DV2007S1

Fast-Charge Development System

Control of On-Board Switch-Mode Regulator

Features

- bq2007 fast-charge control evaluation and development
- Battery charge status display modes and driver interfaces are jumper configurable
  - On-board seven-step LED bargraph or ten-step BCD digit display
  - Charge status monitoring interface option
  - On-board charge status indication LEDs
- Fast-charge termination by -ΔV, peak voltage detect (PVD), maximum voltage, maximum time, and maximum temperature
- Jumper-selectable for 4, 5, 6, 8, or 10 NiCd or NiMH cell pack charging
- Jumper-selectable standard or fast charge rates from 1 to 4 hours
- Discharge-before-charge push-button or automatic control

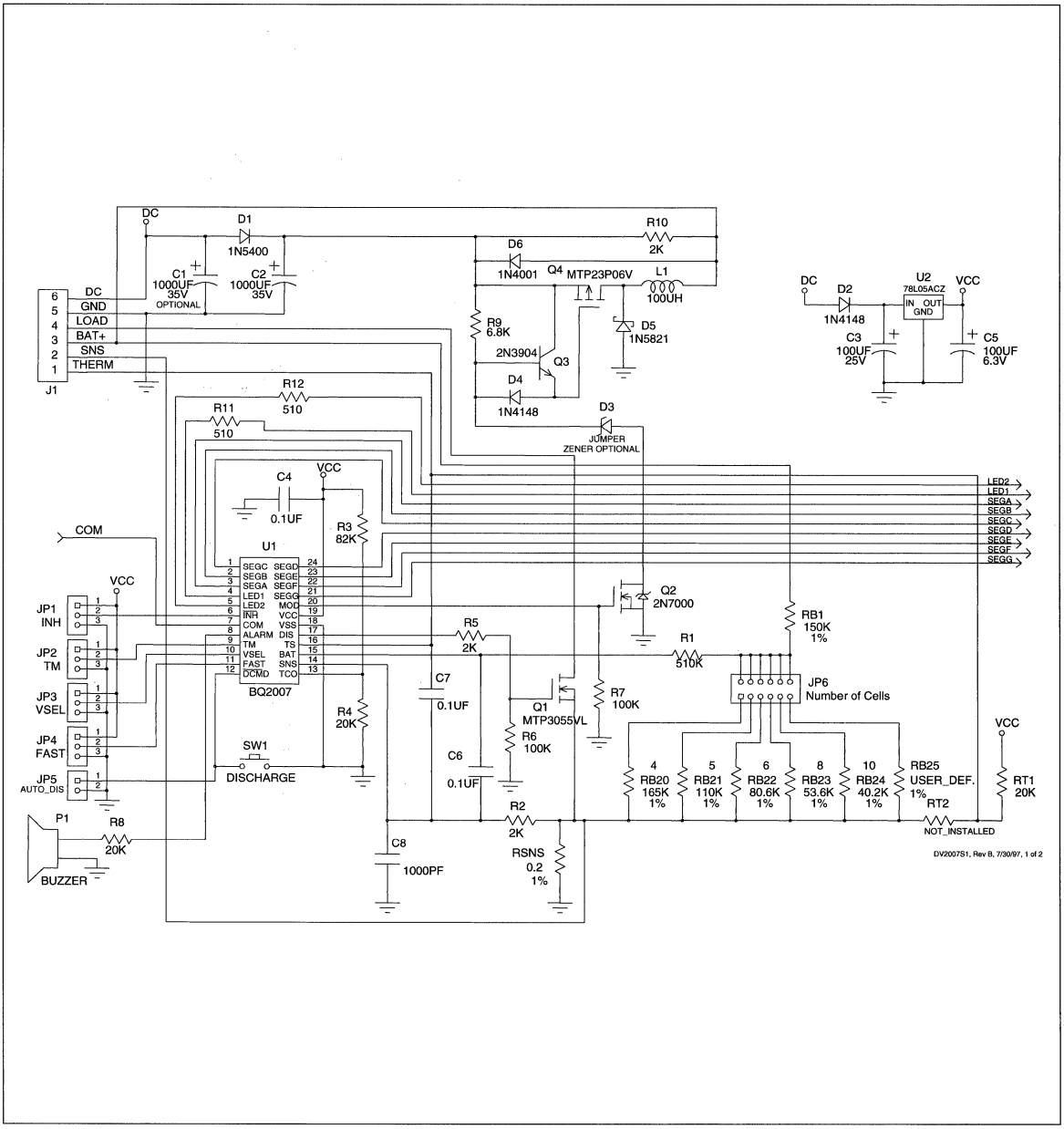


General Description

The DV2007S1 provides the platform for a functional evaluation of the bq2007 features on single PCB. The board contain all the connections required to fully exercise the bq2007 feature sets. See the bq2007 data sheet and application note AB-0019 entitled "Using the bq2007 Display Mode Options."

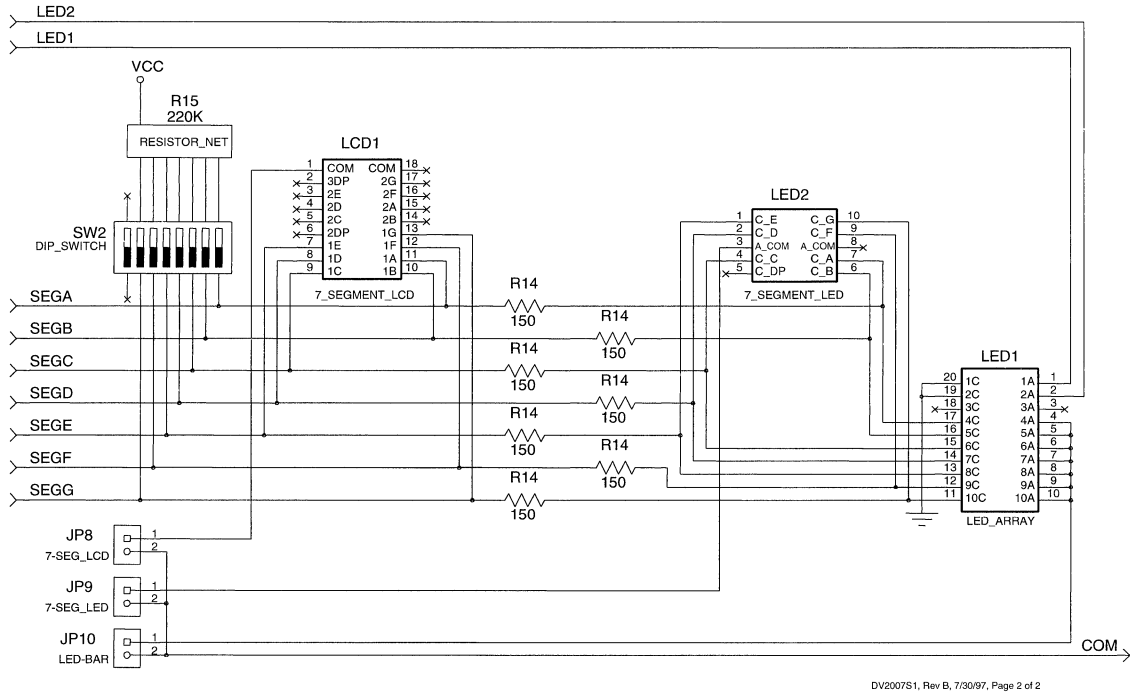
A full data sheet of this product is available on the Unitrode web site, or you may contact the factory for one.

DV2007S1 Board Schematic



Rev A Board

DV2007S1 Board Schematic (Continued)



DV2007S1, Rev B, 7/30/97, Page 2 of 2

Rev. A Board

UNITRODE

bq2031

Lead-Acid Fast-Charge IC

Features

- ➤ Conforms to battery manufacturers' charge recommendations for cyclic and float charge
- ➤ Pin-selectable charge algorithms
  - Two-Step Voltage with temperature-compensated constant-voltage maintenance
  - Two-Step Current with constant-rate pulsed current maintenance
  - Pulsed Current: hysteretic, on-demand pulsed current
- ➤ Pin-selectable charge termination by maximum voltage, Δ^2V, minimum current, and maximum time
- ➤ Pre-charge qualification detects shorted, opened, or damaged cells and conditions battery
- ➤ Charging continuously qualified by temperature and voltage limits
- ➤ Internal temperature-compensated voltage reference
- ➤ Pulse-width modulation control
  - Ideal for high-efficiency switch-mode power conversion
  - Configurable for linear or gated current use
- ➤ Direct LED control outputs display charge status and fault conditions

General Description

The bq2031 Lead-Acid Fast Charge IC is designed to optimize charging of lead-acid chemistry batteries. A flexible pulse-width modulation regulator allows the bq2031 to control constant-voltage, constant-current, or pulsed-current charging. The regulator frequency is set by an external capacitor for design flexibility. The switch-mode design keeps power dissipation to a minimum for high charge current applications.

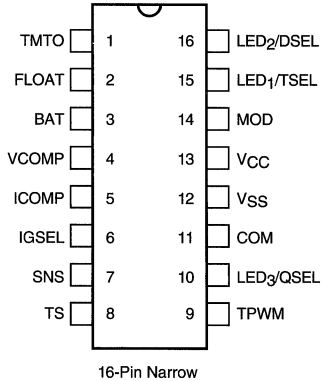
A charge cycle begins when power is applied or the battery is replaced. For safety, charging is inhibited until the battery voltage is within configured limits. If the battery voltage is less than the low-voltage threshold, the bq2031 provides trickle-current charging until the voltage rises into the allowed range or an internal timer runs out and places the bq2031 in a Fault condition. This procedure prevents high-current charging of cells that are possibly damaged or reversed. Charging is inhibited anytime the temperature of the battery is outside the configurable, allowed range. All voltage thresholds are temperature-compensated.

The bq2031 terminates fast (bulk) charging based on the following:

- Maximum voltage
- Second difference of cell voltage (Δ^2V)
- Minimum current (in constant-voltage charging)
- Maximum time-out (MTO)

After bulk charging, the bq2031 provides temperature-compensated maintenance (float) charging to maintain battery capacity.

Pin Connections



16-Pin Narrow
DIP or SOIC

PN203101.eps

Pin Names

TMTO	Time-out timebase input
FLOAT	State control output
BAT	Battery voltage input
VCOMP	Voltage loop comp input
ICOMP	Current loop comp input
IGSEL	Current gain select input
SNS	Sense resistor input
TS	Temperature sense input
TPWM	Regulator timebase input
LED_3/ QSEL	Charge status output 3/ Charge algorithm select input 1
COM	Common LED output
V_{SS}	System ground
V_{CC}	5.0V±10% power
MOD	Modulation control output
LED_1/ TSEL	Charge status output 1/ Charge algorithm select input 2
LED_2/ DSEL	Charge status output 2/ Display select input

Pin Descriptions

TMTO **Time-out timebase input**

This input sets the maximum charge time. The resistor and capacitor values are determined using equation 6. Figure 9 shows the resistor/capacitor connection.

FLOAT **Float state control output**

This open-drain output uses an external resistor divider network to control the BAT input voltage threshold (V_{FLT}) for the float charge regulation. See Figure 1.

BAT **Battery voltage input**

BAT is the battery voltage sense input. This potential is generally developed using a high-impedance resistor divider network connected between the positive and the negative terminals of the battery. See Figure 6 and equation 2.

VCOMP **Voltage loop compensation input**

This input uses an external C or R-C network for voltage loop stability.

IGSEL **Current gain select input**

This three-state input is used to set I_{MIN} for fast charge termination in the Two-Step Voltage algorithm and for maintenance current regulation in the Two-Step Current algorithm. See Tables 3 and 4.

ICOMP **Current loop compensation input**

This input uses an external C or R-C network for current loop stability.

SNS **Charging current sense input**

Battery current is sensed via the voltage developed on this pin by an external sense resistor, R_{SNS}, connected in series with the low side of the battery. See equation 8.

TS **Temperature sense input**

This input is for an external battery temperature monitoring thermistor or probe. An external resistor divider network sets the lower and upper temperature thresholds. See Figures 7 and 8 and equations 4 and 5.

TPWM **Regulation timebase input**

This input uses an external timing capacitor to ground the pulse-width modulation (PWM) frequency. See equation 9.

COM **Common LED output**

Common output for LED_{1-3}. This output is in a high-impedance state during initialization to read program inputs on TSEL, QSEL, and DSEL.

QSEL **Charge regulation select input**

With TSEL, selects the charge algorithm. See Table 1.

MOD **Current-switching control output**

MOD is a pulse-width modulated push/pull output that is used to control the charging current to the battery. MOD switches high to enable current flow and low to inhibit current flow.

LED_{1-3} **Charger display status 1–3 outputs**

These charger status output drivers are for the direct drive of the LED display. Display modes are shown in Table 2. These outputs are tri-stated during initialization so that QSEL, TSEL, and DSEL can be read.

DSEL **Display select input**

This three-level input controls the LED_{1-3} charge display modes. See Table 2.

TSEL **Termination select input**

With QSEL, selects the charge algorithm. See Table 1.

V_{CC} **V_{CC} supply**

5.0V, ± 10% power

V_{SS} **Ground**

Functional Description

The bq2031 functional operation is described in terms of:

- Charge algorithms
- Charge qualification
- Charge status display
- Voltage and current monitoring
- Temperature monitoring

- Fast charge termination
- Maintenance charging
- Charge regulation

Charge Algorithms

Three charge algorithms are available in the bq2031:

- Two-Step Voltage
- Two-Step Current
- Pulsed Current

The state transitions for these algorithms are described in Table 1 and are shown graphically in Figures 2 through 4. The user selects a charge algorithm by configuring pins QSEL and TSEL.

Charge Qualification

The bq2031 starts a charge cycle when power is applied while a battery is present or when a battery is inserted. Figure 1 shows the state diagram for pre-charge qualification and temperature monitoring. The bq2031 first checks that the battery temperature is within the allowed, user-configurable range. If the temperature is out-of-range (or the thermistor is missing), the bq2031 enters the Charge Pending state and waits until the battery temperature is within the allowed range. Charge Pending is annunciated by LED_3 flashing.

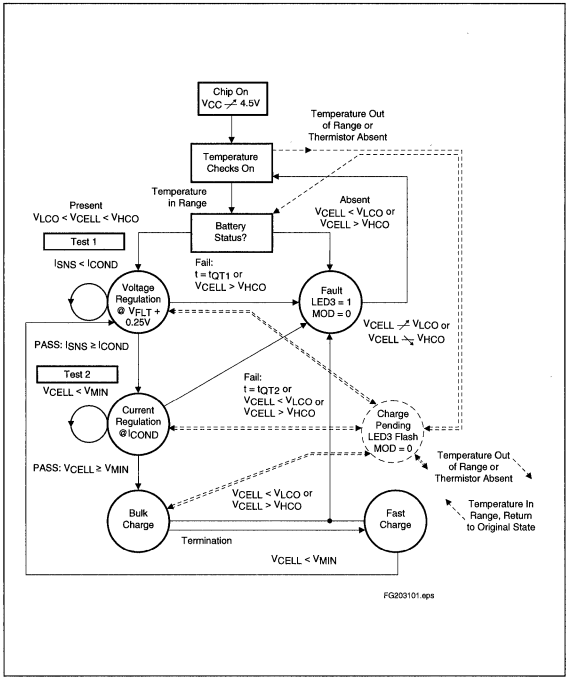


Figure 1. Cycle Start/Battery Qualification State Diagram

Table 1. bq2031 Charging Algorithms

Algorithm/State	QSEL	TSEL	Conditions	MOD Output
Two-Step Voltage	L	H/L[Note 1]	-	-
Fast charge, phase 1			while $V_{BAT} < V_{BLK}$, $I_{SNS} = I_{MAX}$	Current regulation
Fast charge, phase 2			while $I_{SNS} > I_{MIN}$, $V_{BAT} = V_{BLK}$	Voltage regulation
Primary termination			$I_{SNS} = I_{MIN}$	
Maintenance			$V_{BAT} = V_{FLT}$	Voltage regulation
Two-Step Current	H	L	-	-
Fast charge			while $V_{BAT} < V_{BLK}$, $I_{SNS} = I_{MAX}$	Current regulation
Primary termination			$V_{BAT} = V_{BLK}$ or $\Delta^2V < -8mV$[Note 2]	
Maintenance			I_{SNS} pulsed to average I_{FLT}	Fixed pulse current
Pulsed Current	H	H	-	-
Fast charge			while $V_{BAT} < V_{BLK}$, $I_{SNS} = I_{MAX}$	Current regulation
Primary termination			$V_{BAT} = V_{BLK}$	
Maintenance			$I_{SNS} = I_{MAX}$ after $V_{BAT} = V_{FLT}$; $I_{SNS} = 0$ after $V_{BAT} = V_{BLK}$	Hysteretic pulsed current

Notes: 1. May be high or low, but do not float.
2. A Unitrode proprietary algorithm for accumulating successive differences between samples of V_{BAT}.

Thermal monitoring continues throughout the charge cycle, and the bq2031 enters the Charge Pending state anytime the temperature is out of range. (There is one exception; if the bq2031 is in the Fault state—see below—the out-of-range temperature is not recognized until the bq2031 leaves the Fault state.) All timers are suspended (but not reset) while the bq2031 is in Charge Pending. When the temperature comes back into range, the bq2031 returns to the point in the charge cycle where the out-of-range temperature was detected.

When the temperature is valid, the bq2031 performs two tests on the battery. In test 1, the bq2031 regulates a voltage of V_{FLT} + 0.25V across the battery and observes I_{SNS}. If I_{SNS} does not rise to at least I_{COND} within a time-out period (e.g., the cell has failed open), the bq2031 enters the Fault state. If test 1 passes, the bq2031 then regulates current to I_{COND} (= $I_{MAX}/5$) and watches V_{CELL} (= V_{BAT} - V_{SNS}). If V_{CELL} does not rise to at least V_{FLT} within a time-out period (e.g., the cell has failed short), again the bq2031 enters the Fault state. A hold-off period is enforced at the beginning of qualification test 2 before the bq2031 recognizes its "pass" criterion. If this second test passes, the bq2031 begins fast (bulk) charging.

Once in the Fault state, the bq2031 waits until V_{CC} is cycled or a battery insertion is detected. It then starts a new charge cycle and begins the qualification process again.

Charge Status Display

Charge status is annunciated by the LED driver outputs LED_1–LED_3. Three display modes are available in the bq2031; the user selects a display mode by configuring pin DSEL. Table 2 shows the three modes and their programming pins.

The bq2031 does not distinguish between an over-voltage fault and a "battery absent" condition. The bq2031 enters the Fault state, annunciated by turning on LED_3, whenever the battery is absent. The bq2031, therefore, gives an indication that the charger is on even when no battery is in place to be charged.

Table 2. bq2031 Display Output Summary

Mode	Charge Action State	LED_1	LED_2	LED_3
DSEL = 0 (Mode 1)	Battery absent or over-voltage fault	Low	Low	High
	Pre-charge qualification	Flash	Low	Low
	Fast charging	High	Low	Low
	Maintenance charging	Low	High	Low
	Charge pending (temperature out of range)	X	X	Flash
	Charging fault	X	X	High
DSEL = 1 (Mode 2)	Battery absent or over-voltage fault	Low	Low	High
	Pre-charge qualification	High	High	Low
	Fast charge	Low	High	Low
	Maintenance charging	High	Low	Low
	Charge pending (temperature out of range)	X	X	Flash
	Charging fault	X	X	High
DSEL = Float (Mode 3)	Battery absent or over-voltage fault	Low	Low	High
	Pre-charge qualification	Flash	Flash	Low
	Fast charge: current regulation	Low	High	Low
	Fast charge: voltage regulation	High	High	Low
	Maintenance charging	High	Low	Low
	Charge pending (temperature out of range)	X	X	Flash
	Charging fault	X	X	High

Notes: 1 = V_{CC}; 0 = V_{SS}; X = LED state when fault occurred; Flash = $\frac{1}{6}$ s low, $\frac{1}{6}$ s high.
In the Pulsed Current algorithm, the bq2031 annunciates maintenance when charging current is off and fast charge whenever charging current is on.

4/14

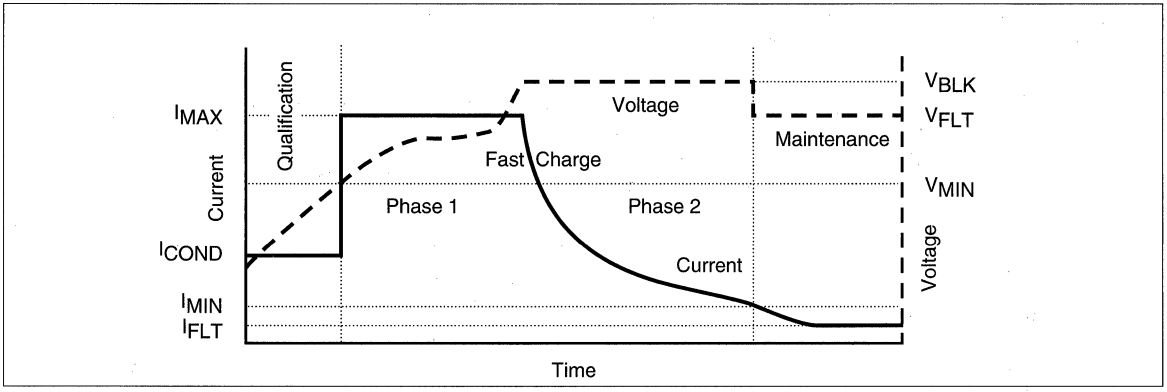


Figure 2. Two-Step Voltage Algorithm

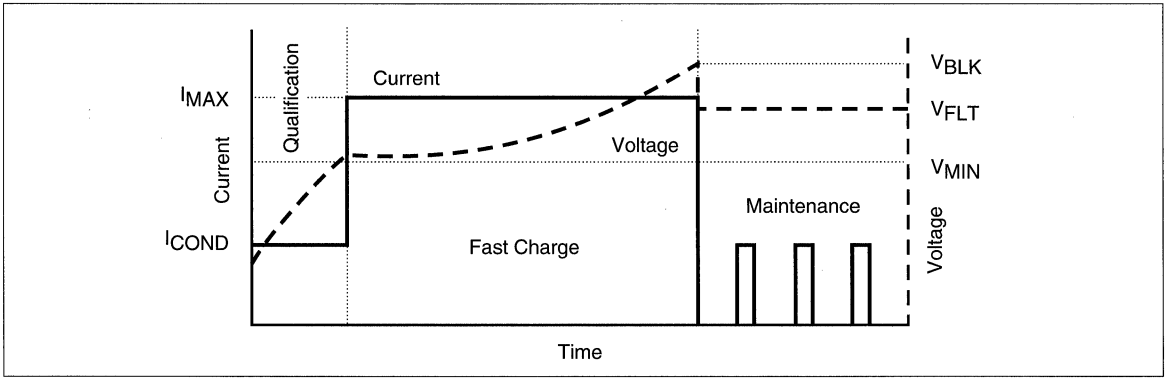


Figure 3. Two-Step Current Algorithm

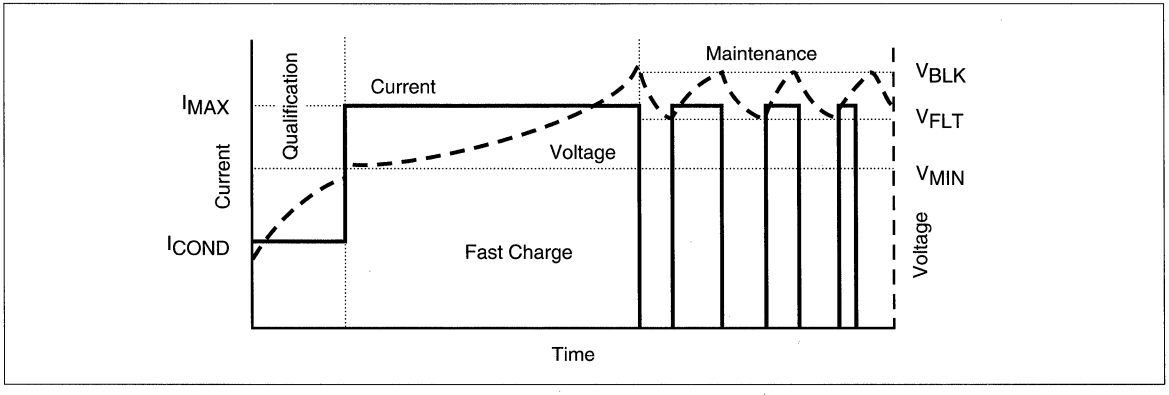


Figure 4. Pulsed Current Algorithm

Configuring Algorithm and Display Modes

$QSEL/LED_3$, $DSEL/LED_2$, and $TSEL/LED_1$ are bi-directional pins with two functions; they are LED driver pins as outputs and programming pins for the bq2031 as inputs. The selection of pull-up, pull-down, or no pull resistor programs the charging algorithm on QSEL and TSEL per Table 1 and the display mode on DSEL per Table 2. The bq2031 latches the program states when any of the following events occurs:

1. V_{CC} rises to a valid level.
2. The bq2031 leaves the Fault state.
3. The bq2031 detects battery insertion.

The LEDs go blank for approximately 750ms (typical) while new programming data is latched.

For example, Figure 5 shows the bq2031 configured for the Pulsed Current algorithm and display mode 2.

Voltage and Current Monitoring

The bq2031 monitors battery pack voltage at the BAT pin. A voltage divider between the positive and negative terminals of the battery pack is used to present a scaled battery pack voltage to the BAT pin and an appropriate value for regulation of float (maintenance) voltage to the FLOAT pin. The bq2031 also uses the voltage across a sense resistor (R_{SNS}) between the negative terminal of the battery pack and ground to monitor current. See Figure 6 for the configuration of this network.

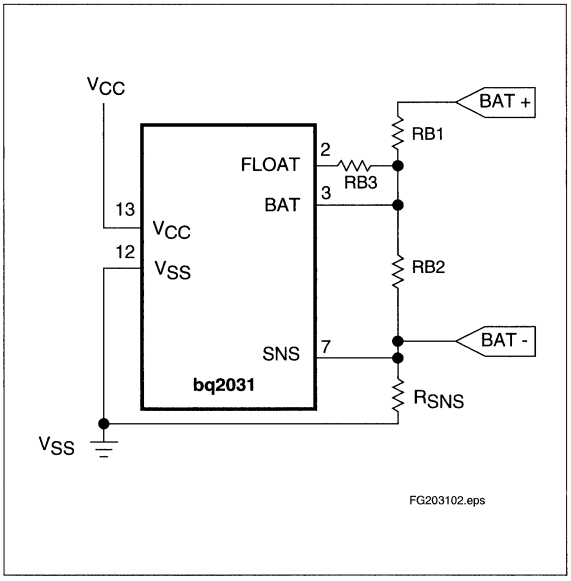


Figure 6. Configuring the Battery Divider

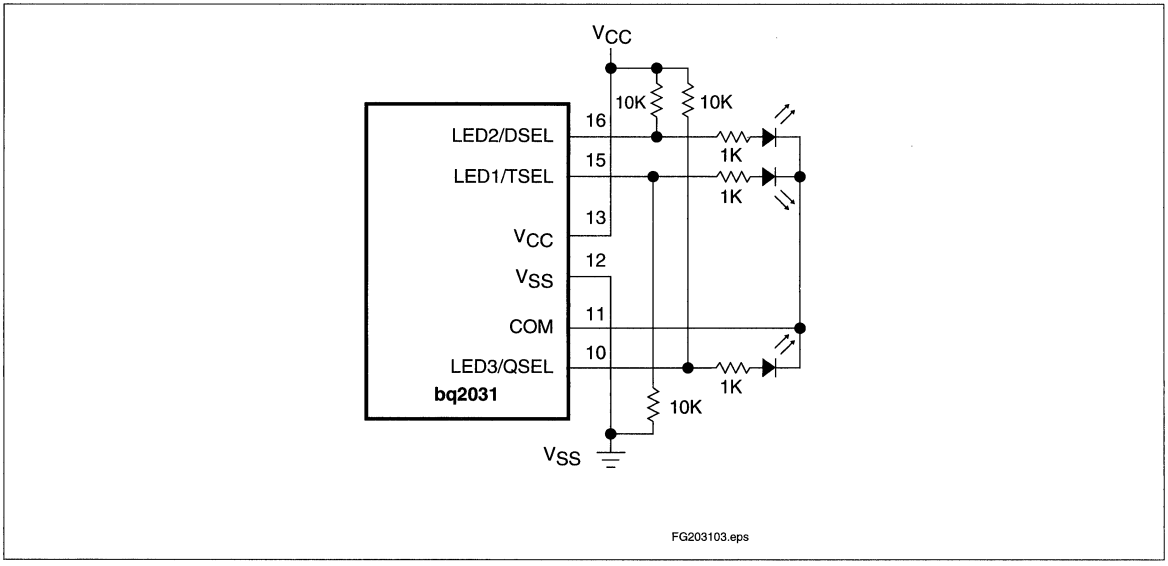


Figure 5. Configuring Charging Algorithm and Display Mode

6/14

The resistor values are calculated from the following:

Equation 1

$$\frac{RB1}{RB2} = \frac{(N * V_{FLT})}{2.2V} - 1$$

Equation 2

$$\frac{RB1}{RB2} + \frac{RB1}{RB3} = (\frac{N * V_{BLK}}{2.2}) - 1$$

Equation 3

$$I_{MAX} = \frac{0.250V}{R_{SNS}}$$

where:

- N = Number of cells
- V_{FLT} = Desired float voltage
- V_{BLK} = Desired bulk charging voltage
- I_{MAX} = Desired maximum charge current

These parameters are typically specified by the battery manufacturer. The total resistance presented across the battery pack by RB1 + RB2 should be between 150kΩ and 1MΩ. The minimum value ensures that the divider network does not drain the battery excessively when the power source is disconnected. Exceeding the maximum value increases the noise susceptibility of the BAT pin.

An empirical procedure for setting the values in the resistor network is as follows:

1. Set RB2 to 49.9 kΩ. (for 3 to 18 series cells)
2. Determine RB1 from equation 1 given V_{FLT}
3. Determine RB3 from equation 2 given V_{BLK}
4. Calculate R_{SNS} from equation 3 given I_{MAX}

Battery Insertion and Removal

The bq2031 uses V_{BAT} to detect the presence or absence of a battery. The bq2031 determines that a battery is present when V_{BAT} is between the High-Voltage Cutoff (V_{HCO} = 0.6 * V_{CC}) and the Low-Voltage Cutoff (V_{LCO} = 0.8V). When V_{BAT} is outside this range, the bq2031 determines that no battery is present and transitions to the Fault state. Transitions into and out of the range between V_{LCO} and V_{HCO} are treated as battery insertions and removals, respectively. Besides being used to detect battery insertion, the V_{HCO} limit implicitly serves as an over-voltage charge termination, because exceeding this limit causes the bq2031 to believe that the battery has been removed.

The user must include a pull-up resistor from the positive terminal of the battery stack to VDC (and a diode to prevent battery discharge through the power supply when the supply is turned off) in order to detect battery removal during periods of voltage regulation. Voltage regulation occurs in pre-charge qualification test 1 prior to all of the fast charge algorithms, and in phase 2 of the Two-Step Voltage fast charge algorithm.

Temperature Monitoring

The bq2031 monitors temperature by examining the voltage presented between the TS and SNS pins (V_{TEMP}) by a resistor network that includes a Negative Temperature Coefficient (NTC) thermistor. Resistance variations around that value are interpreted as being proportional to the battery temperature (see Figure 7).

The temperature thresholds used by the bq2031 and their corresponding TS pin voltage are:

- TCO—Temperature cutoff—Higher limit of the temperature range in which charging is allowed. V_{TCO} = 0.4 * V_{CC}
- HTF—High-temperature fault—Threshold to which temperature must drop after temperature cutoff is exceeded before charging can begin again. V_{HTF} = 0.44 * V_{CC}

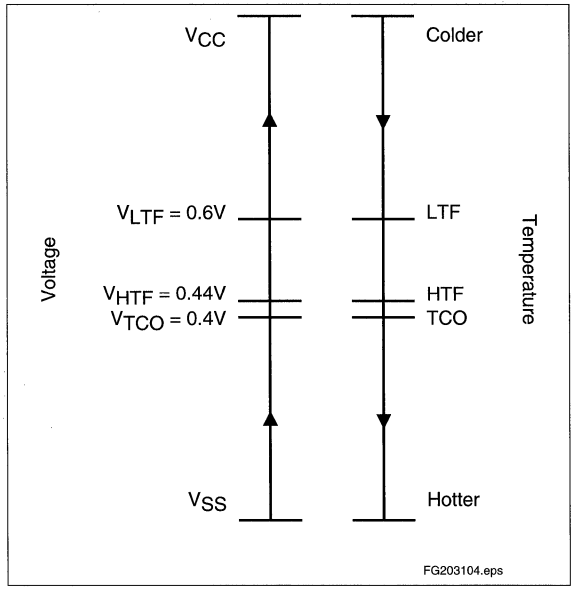


Figure 7. Voltage Equivalent of Temperature Thresholds

- LTF—Low-temperature fault—Lower limit of the temperature range in which charging is allowed. $V_{LTF} = 0.6 * V_{CC}$

A resistor-divider network must be implemented that presents the defined voltage levels to the TS pin at the desired temperatures (see Figure 8).

The equations for determining RT1 and RT2 are:

Equation 4

$$0.6 * V_{CC} = \frac{(V_{CC} - 0.250V)}{1 + \frac{RT1 * (RT2 + R_{LTF})}{(RT2 * R_{LTF})}}$$

Equation 5

$$0.44 = \frac{1}{1 + \frac{RT1 * (RT2 + R_{HTF})}{(RT2 * R_{HTF})}}$$

where:

- R_{LTF} = thermistor resistance at LTF
- R_{HTF} = thermistor resistance at HTF

TCO is determined by the values of RT1 and RT2. 1% resistors are recommended.

Disabling Temperature Sensing

Temperature sensing can be disabled by removing RT and using a 100kΩ resistor for RT1 and RT2.

Temperature Compensation

The internal voltage reference used by the bq2031 for all voltage threshold determinations is compensated for temperature. The temperature coefficient is -3.9mV/°C, normalized to 25°C. Voltage thresholds in the bq2031 vary by this proportion as ambient conditions change.

Fast-Charge Termination

Fast-charge termination criteria are programmed with the fast charge algorithm per Table 1. Note that not all criteria are applied in all algorithms.

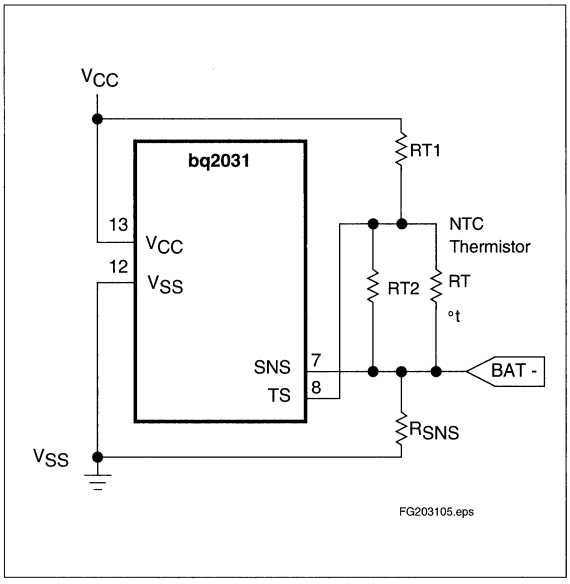


Figure 8. Configuring Temperature Sensing

Minimum Current

Fast charge terminates when the charging current drops below a minimum current threshold programmed by the value of IGSEL (see Table 3). This is used by the Two-Step Voltage algorithm.

Table 3. I_{MIN} Termination Thresholds

IGSEL	I_{MIN}
0	$I_{MAX}/10$
1	$I_{MAX}/20$
Z	$I_{MAX}/30$

Second Difference (Δ^2V)

Second difference is a Unitrode proprietary algorithm that accumulates the difference between successive samples of V_{BAT}. The bq2031 takes a sample and makes a termination decision at a frequency equal to 0.008 * t_{MTO}. Fast charge terminates when the accumulated difference is ≤ -8mV. Second difference is used only in the Two-Step Current algorithm, and is subject to a hold-off period (see below).

Maximum Voltage

Fast charge terminates when $V_{CELL} \geq V_{BLK}$. V_{BLK} is set per equation 2. Maximum voltage is used for fast charge termination in the Two-Step Current and Pulsed Current algorithms, and for transition from phase 1 to phase 2 in the Two-Step Voltage algorithm. This criterion is subject to a hold-off period.

Hold-off Periods

Maximum V and Δ^2V termination criteria are subject to a hold-off period at the start of fast charge equal to 0.15 * t_{MTO}. During this time, these termination criteria are ignored.

Maximum Time-Out

Fast charge terminates if the programmed MTO time is reached without some other termination shutting off fast charge. MTO is programmed from 1 to 24 hours by an R-C network on TMTO (see Figure 9) per the equation:

Equation 6

$$t_{MTO} = 0.5 * R * C$$

where R is in kΩ, C is in µF, and t_{MTO} is in hours. Typically, the maximum value for C of 0.1µF is used.

Fast-charge termination by MTO is a Fault only in the Pulsed Current algorithm; the bq2031 enters the Fault state and waits for a new battery insertion, at which time it begins a new charge cycle. In the Two-Step Voltage and Two-Step Current algorithms, the bq2031 transitions to the maintenance phase on MTO time-out.

The MTO timer starts at the beginning of fast charge. In the Two-Step Voltage algorithm, it is cleared and restarted when the bq2031 transitions from phase 1 (current regulation) to phase 2 (voltage regulation). The MTO timer is suspended (but not reset) during the out-of-range temperature (Charge Pending) state.

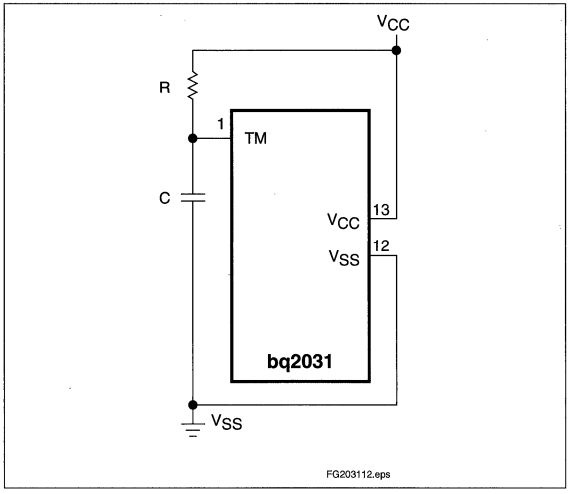


Figure 9. R-C Network for Setting MTO

Maintenance Charging

Three algorithms are used in maintenance charging:

- Two-Step Voltage algorithm
- Two-Step Current algorithm
- Pulsed Current algorithm

Two-Step Voltage Algorithm

In the Two-Step Voltage algorithm, the bq2031 provides charge maintenance by regulating charging voltage to V_{FLT}. Charge current during maintenance is limited to I_{COND}.

Two-Step Current Algorithm

Maintenance charging in the Two-Step Current Algorithm is implemented by varying the period (T_P) of a fixed current (I_{COND} = I_{MAX}/5) and duration (0.2 seconds) pulse to achieve the configured average maintenance current value. See Figure 10.

Maintenance current can be calculated by:

Equation 7

$$\text{Maintenance current} = \frac{((0.2) * I_{COND})}{T_P} = \frac{((0.04) * I_{MAX})}{T_P}$$

where T_P is the period of the waveform in seconds.

Table 4 gives the values of P programmed by IGSEL.

Table 4. Fixed-Pulse Period by IGSEL

IGSEL	T_P (sec.)
L	0.4
H	0.8
Z	1.6

Pulsed Current Algorithm

In the Pulsed Current algorithm, charging current is turned off after the initial fast charge termination until V_{CELL} falls to V_{FLT}. Full fast charge current (I_{MAX}) is then re-enabled to the battery until V_{CELL} rises to V_{BLK}. This cycle repeats indefinitely.

Charge Regulation

The bq2031 controls charging through pulse-width modulation of the MOD output pin, supporting both constant-current and constant-voltage regulation. Charge current is monitored by the voltage at the SNS pin, and charge voltage by voltage at the BAT pin. These voltages are compared to an internal temperature-compensated reference, and the MOD output modulated to maintain the desired value.

Voltage at the SNS pin is determined by the value of resistor R_{SNS}, so nominal regulated current is set by:

Equation 8

$$I_{MAX} = 0.250V/R_{SNS}$$

The switching frequency of the MOD output is determined by an external capacitor (CPWM) between the pin TPWM and ground, per the following:

Equation 9

$$F_{PWM} = 0.1/C_{PWM}$$

where C is in µF and F is in kHz. A typical switching rate is 100kHz, implying C_{PWM} = 0.001µF. MOD pulse width is modulated between 0 and 80% of the switching period.

To prevent oscillation in the voltage and current control loops, frequency compensation networks (C or R-C) are typically required on the VCOMP and ICOMP pins (respectively) to add poles and zeros to the loop control equations. A software program, "CNFG2031," is available to assist in configuring these networks for buck type regulators. For more detail on the control loops in buck topology, see the application note, "Switch-Mode Power Conversion Using the bq2031." For assistance with other power supply topologies, contact the factory.

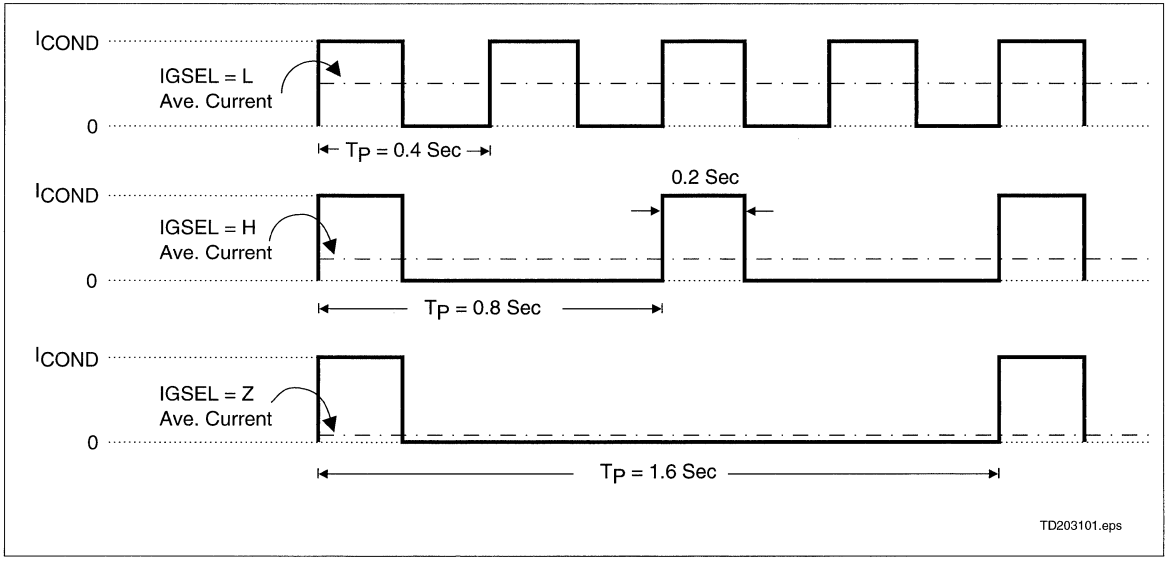


Figure 10. Implementation of Fixed-Pulse Maintenance Charge

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	-20	+70	°C	Commercial
T_{STG}	Storage temperature	-55	+125	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10 s. max.
T_{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds ($T_A = T_{OPR}$; V_{CC} = 5V ±10%)

Symbol	Parameter	Rating	Unit	Tolerance	Notes
V_{REF}	Internal reference voltage	2.20	V	1%	T_A = 25°C
	Temperature coefficient	-3.9	mV/°C	10%	
V_{LTF}	TS maximum threshold	0.6 * V_{CC}	V	±0.03V	Low-temperature fault
V_{HTF}	TS hysteresis threshold	0.44 * V_{CC}	V	±0.03V	High-temperature fault
V_{TCO}	TS minimum threshold	0.4 * V_{CC}	V	±0.03V	Temperature cutoff
V_{HCO}	High cutoff voltage	0.60 * V_{CC}	V	±0.03V	
V_{MIN}	Under-voltage threshold at BAT	0.34 * V_{CC}	V	±0.03V	
V_{LCO}	Low cutoff voltage	0.8	V	±0.03V	
V_{SNS}	Current sense at SNS	0.250	V	10%	I_{MAX}
		0.05	V	10%	I_{COND}

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{TEMP}	TS voltage potential	0	-	V_{CC}	V	V_{TS} - V_{SNS}
V_{CELL}	Battery voltage potential	0	-	V_{CC}	V	V_{BAT} - V_{SNS}
I_{CC}	Supply current	-	2	4	mA	Outputs unloaded
I_{IZ}	DSEL tri-state open detection	-2	-	2	µA	Note 2
	IGSEL tri-state open detection	-2		2	µA	
V_{IH}	Logic input high	V_{CC}-1.0	-	-	V	QSEL,TSEL
		V_{CC}-0.3	-	-	V	DSEL, IGSEL
V_{IL}	Logic input low	-	-	V_{SS}+1.0	V	QSEL,TSEL
		-	-	V_{SS}+0.3	V	DSEL, IGSEL
V_{OH}	LED_1, LED_2, LED_3, output high	V_{CC}-0.8	-	-	V	$I_{OH} \leq 10mA$
	MOD output high	V_{CC}-0.8	-	-	V	$I_{OH} \leq 10mA$
V_{OL}	LED_1, LED_2, LED_3, output low	-	-	V_{SS}+0.8V	V	$I_{OL} \leq 10mA$
	MOD output low	-	-	V_{SS}+0.8V	V	$I_{OL} \leq 10mA$
	FLOAT output low	-	-	V_{SS}+0.8V	V	$I_{OL} \leq 5mA$, Note 3
	COM output low	-	-	V_{SS}+0.5	V	$I_{OL} \leq 30mA$
I_{OH}	LED_1, LED_2, LED_3, source	-10	-	-	mA	$V_{OH} = V_{CC}$-0.5V
	MOD source	-5.0	-	-	mA	$V_{OH} = V_{CC}$-0.5V
I_{OL}	LED_1, LED_2, LED_3, sink	10	-	-	mA	$V_{OL} = V_{SS}$+0.5V
	MOD sink	5	-	-	mA	$V_{OL} = V_{SS}$+0.8V
	FLOAT sink	5	-	-	mA	$V_{OL} = V_{SS}$+0.8V, Note 3
	COM sink	30	-	-	mA	$V_{OL} = V_{SS}$+0.5V
I_{IL}	DSEL logic input low source	-	-	+30	µA	V = V_{SS} to V_{SS}+ 0.3V, Note 2
	IGSEL logic input low source	-	-	+70	µA	V = V_{SS} to V_{SS}+ 0.3V
I_{IH}	DSEL logic input high source	-30	-	-	µA	V = V_{CC} - 0.3V to V_{CC}
	IGSEL logic input high source	-70	-	-	µA	V = V_{CC} - 0.3V to V_{CC}
I_L	Input leakage	-	-	±1	µA	QSEL, TSEL, Note 2

Notes:
1. All voltages relative to V_{SS} except where noted.
2. Conditions during initialization after V_{CC} applied.
3. SNS = 0V.

12/14

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
R_{BATZ}	BAT pin input impedance	50	-	-	MΩ	
R_{SNSZ}	SNS pin input impedance	50	-	-	MΩ	
R_{TSZ}	TS pin input impedance	50	-	-	MΩ	
R_{PROG1}	Soft-programmed pull-up or pull-down resistor value (for programming)	-	-	10	kΩ	DSEL, TSEL, and QSEL
R_{PROG2}	Pull-up or pull-down resistor value	-	-	3	kΩ	IGSEL
R_{MTO}	Charge timer resistor	20	-	480	kΩ	

Timing (TA = TOPR; VCC = 5V ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{MTO}	Charge time-out range	1	-	24	hours	See Figure 9
t_{QT1}	Pre-charge qual test 1 time-out period	-	$0.02t_{MTO}$	-	-	
t_{QT2}	Pre-charge qual test 2 time-out period	-	$0.16t_{MTO}$	-	-	
t_{DV}	Δ^2V termination sample frequency	-	$0.008t_{MTO}$	-	-	
t_{H01}	Pre-charge qual test 2 hold-off period	-	$0.002t_{MTO}$	-	-	
t_{H02}	Bulk charge hold-off period	-	$0.015t_{MTO}$	-	-	
F_{PWM}	PWM regulator frequency range	-	100		kHz	See Equation 9

Capacitance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
C_{MTO}	Charge timer capacitor	-	0.1	0.1	µF
C_{PWM}	PWM R-C capacitance	-	0.001	-	µF

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1		Descriptions	Clarified and consolidated
1		Renamed	Dual-Level Constant Current Mode to Two-Step Current Mode V_{MCV} to V_{HCO} V_{INT} to V_{LCO} t_{UV1} to t_{QT1} t_{UV2} to t_{QT2}
1		Consolidation	Tables 1 and 2
1		Added figures	Start-up states Temperature sense input voltage thresholds Pulsed maintenance current implementation
1		Updated figures	Figures 1 through 6
1		Added equations	Thermistor divider network configuration equations
1		Raised condition	MOD V_{OL} and V_{OH} parameters from ≤5mA to ≤10µA
1		Corrected Conditions	VSNS rating from V_{MAX} and V_{MIN} to I_{MAX} and I_{MIN}
1		Added table	Capacitance table for C_{MTO} and C_{PWM}
2	6	Changed values in Figure 5	Was 51K; is now 10K
3	7, 10	Changed values in Equations 3 and 8	Was: $I_{MAX} = 0.275V/R_{SNS}$; is now $I_{MAX} = 0.250V/R_{SNS}$
3	8	Changed values in Equation 4	Was: $(V_{CC} - 0.275)$; is now $(V_{CC} - 0.250V)$
3	11	Changed rating value for V_{SNS} in DC Thresholds table	Was 0.275; is now 0.250
4	11	T_{OPR}	Deleted industrial temperature range.

Notes: Change 1 = Dec. 1995 B changes from June 1995 A.
Change 2 = Sept. 1996 C changes from Dec. 1995 B.
Change 3 = April 1997 D changes from Sept. 1996 C.
Change 4 = June 1999 E changes from April 1997 D.

Ordering Information

bq2031 _

Package Option:
PN = 16-pin plastic DIP
SN = 16-pin narrow SOIC

Device:
bq2031 Lead Acid Charge IC

14/14

UNITRODE

Product Brief **DV2031S2**

Lead-Acid Charger Development System

Control of On-Board P-FET Switch-Mode Regulator

Features

- ➤ bq2031 fast-charge control evaluation and development
- ➤ Onboard configuration for fast charge of 2, 3, 4 or 6 lead-acid cells; user-defined option allows other configurations
- ➤ Selectable charge algorithms: Two-Step Voltage, Two-Step Current, or Pulsed Current
- ➤ Constant current (up to 2.2A) and constant voltage (up to 15V) provided by on-board switch-mode regulator
- ➤ Charge termination by maximum voltage, second difference of cell voltage, minimum current, or maximum time-out
- ➤ Direct connections for battery, thermistor, and power supply
- ➤ MTO is set for 3.1 hours
- ➤ Jumper-configurable 3-LED display

General Description

The DV2031S2 Development System provides a development environment for the bq2031 Lead-Acid Fast-Charge IC. The DV2031S2 incorporates a bq2031 in a buck-type switch-mode regulation mode to provide fast-charge control for 2, 3, 4, or 6 lead-acid cells.

The DV2031S2 can be configured for three different charge algorithms with jumpers JP1 and JP3. The charge algorithms available are

- Two-step voltage
- Two-step current
- Pulsed current

Each algorithm consists of pre-charge qualification, fast charge, and maintenance charge periods.

Fast charge termination occurs on

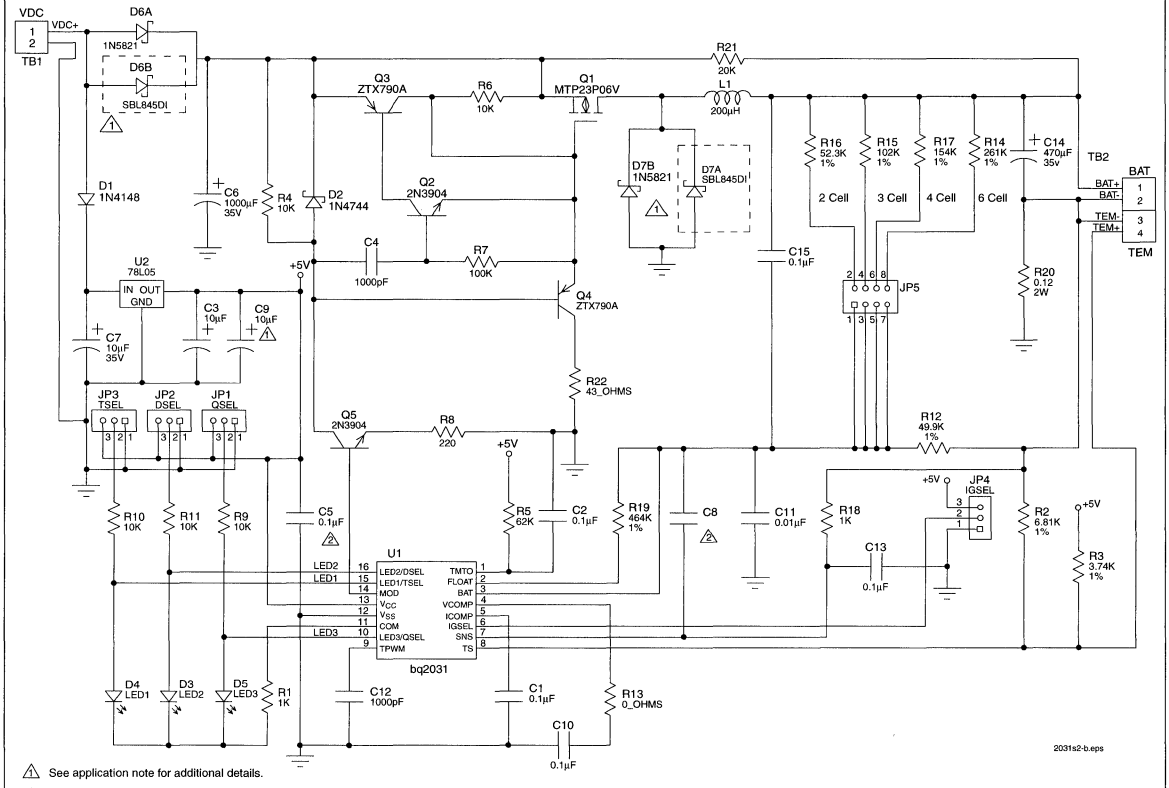
- Maximum voltage
- The second difference of cell voltage (Δ^2V)
- Minimum current
- Maximum time-out

The maintenance charge may be configured for either a regulated float voltage or a pulsed current.

The user provides a DC power supply and batteries and configures the board for the number of cells, the minimum current threshold, and the LED display mode. The board has direct connections for the battery and the provided thermistor.

Before using the DV2031S2 board, please review the bq2031 data sheet and the application note entitled "Using the bq2031 to Charge Lead-Acid Batteries." A full data sheet for this product is available on the Unitrode web site, or you may contact the factory for one.

DV2031S2 Board Schematic



⚠1 See application note for additional details.

⚠2 Not used

Rev. B Board

UNITRODE

bq2054

Lithium Ion Fast-Charge IC

Features

- Safe charge of Lithium Ion battery packs
- Voltage-regulated current-limited charging
- Fast charge terminated by selectable minimum current; safety backup termination on maximum time
- Charging continuously qualified by temperature and voltage limits
- Pulse-width modulation control ideal for high-efficiency switch-mode power conversion
- Direct LED control outputs display charge status and fault conditions

General Description

The bq2054 Lithium Ion Fast-Charge IC is designed to optimize charging of lithium ion (Li-Ion) chemistry batteries. A flexible pulse-width modulation regulator allows the bq2054 to control voltage and current during charging. The regulator frequency is set by an external capacitor for design flexibility. The switch-mode design keeps power dissipation to a minimum.

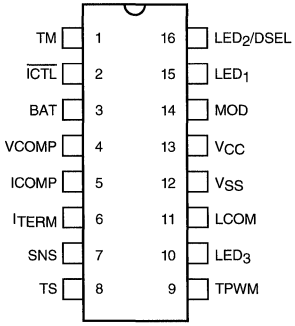
The bq2054 measures battery temperature using an external thermistor for charge qualification. Charging begins when power is applied or on battery insertion.

For safety, the bq2054 inhibits charging until the battery voltage and temperature are within configured limits. If the battery voltage is less than the low-voltage threshold, the bq2054 provides low-current conditioning of the battery.

A constant current-charging phase replenishes up to 70% of the charge capacity, and a voltage-regulated phase returns the battery to full. The charge cycle terminates when the charging current falls below a user-selectable current limit. For safety, charging terminates after maximum time and is suspended if the temperature is outside the preconfigured limits.

The bq2054 provides status indications of all charger states and faults for accurate determination of the battery and charge system conditions.

Pin Connections



16-Pin Narrow DIP or SOIC

PN205401.eps

Pin Names

TM	Time-out programming input	TPWM	Regulator timebase input
$\overline{ICTL}$	Inrush current control output	LED_3	Charge status output 3
BAT	Battery voltage input	LCOM	Common LED output
VCOMP	Voltage loop comp input	V_{SS}	System ground
ICOMP	Current loop comp input	V_{CC}	5.0V±10% power
I_{TERM}	Minimum current termination select input	MOD	Modulation control output
SNS	Sense resistor input	LED_1	Charge status output 1
TS	Temperature sense input	LED_2/DSEL	Charge status output 2/ Display select input

Pin Descriptions

TM **Time-out programming input**

This input sets the maximum charge time. The resistor and capacitor values are determined using Equation 5. Figure 7 shows the resistor/capacitor connection.

$\overline{\text{ICTL}}$ **Inrush current control output**

$\overline{\text{ICTL}}$ is driven low during the fault or charge-complete states of the chip. It is used to disconnect the capacitor across the battery pack terminals, preventing inrush currents from tripping overcurrent protection features in the pack when a new battery is inserted.

BAT **Battery voltage input**

BAT is the battery voltage sense input. This potential is generally developed using a high-impedance resistor divider network connected between the positive and the negative terminals of the battery. See Figure 4 and Equation 1.

VCOMP **Voltage loop compensation input**

This input uses an external R-C network for voltage loop stability.

I_{TERM} **Minimum current termination select**

This three-state input is used to set I_{MIN} for fast charge termination. See Table 2.

ICOMP **Current loop compensation input**

This input uses an external R-C network for current loop stability.

SNS **Charging current sense input**

Battery current is sensed via the voltage developed on this pin by an external sense resistor, R_{SNS}, connected in series with the negative terminal of the battery pack. See Equation 6.

TS **Temperature sense input**

This input is used to monitor battery temperature. An external resistor divider network sets the lower and upper temperature thresholds. See Figure 6 and Equations 3 and 4.

TPWM **Regulation timebase input**

This input uses an external timing capacitor to ground to set the pulse-width modulation (PWM) frequency. See Equation 7.

LCOM **Common LED output**

Common output for LED_{1-3}. This output is in a high-impedance state during initialization to read programming input on DSEL.

MOD **Current-switching control output**

MOD is a pulse-width modulated push/pull output that is used to control the charging current to the battery. MOD switches high to enable current flow and low to inhibit current flow.

LED_1–LED_3 **Charger display status 1–3 outputs**

These charger status output drivers are for the direct drive of the LED display. Display modes are shown in Table 1. These outputs are tri-stated during initialization so that DSEL can be read.

DSEL **Display select input**

This three-level input controls the LED_{1-3} charge display modes. See Table 1.

V_{CC} **V_{CC} supply**

5.0V, ± 10% power

V_{SS} **Ground**

Charge Algorithm

The bq2054 uses a two-phase fast charge algorithm. In phase 1, the bq2054 regulates constant current (I_{SNS} = I_{MAX}) until V_{CELL} (= V_{BAT} - V_{SNS}) rises to V_{REG}. The bq2054 then transitions to phase 2 and regulates constant voltage (V_{CELL} = V_{REG}) until the charging current falls below the programmed I_{MIN} threshold. The charging current must remain below I_{MIN} for 120 ± 40ms before a valid fast charge termination is detected. Fast charge then terminates, and the bq2054 enters the Charge Complete state. See Figures 1 and 2.

Charge Qualification

The bq2054 starts a charge cycle when power is applied while a battery is present or when a battery is inserted. Figure 2 shows the state diagram for pre-charge qualification and temperature monitoring. The bq2054 first checks that the battery temperature is within the allowed, user-configurable range. If the temperature is out of range, the bq2054 enters the Charge Pending state and waits until the battery temperature is within the allowed range. Charge Pending is enunciated by LED_3 flashing.

Thermal monitoring continues throughout the charge cycle, and the bq2054 enters the Charge Pending state when the temperature out of range. (There is one exception; if the bq2054 is in the Fault state—see below—the out-of-range temperature is not recognized until the bq2054 leaves the Fault state.) All timers are suspended (but not reset) while the bq2054 is in Charge Pending. When the temperature comes back into range, the bq2054 returns to the point in the charge cycle where the out-of-range temperature was detected.

When the temperature is valid, the bq2054 then regulates current to I_{COND} (=I_{MAX}/5). After an initial holdoff period t_{HO} (which prevents the chip from reacting to transient voltage spikes that may occur when charge current is first applied), the chip begins monitoring V_{CELL}. If V_{CELL} does not rise to at least V_{MIN} before the expiration of time-out limit t_{MTO} (e.g. the cell has failed short), the bq2054 enters the Fault state. If V_{MIN} is achieved before expiration of the time limit, the chip begins fast charging.

Once in the Fault state, the bq2054 waits until V_{CC} is cycled or a new battery insertion is detected. It then starts a new charge cycle and begins the qualification process again.

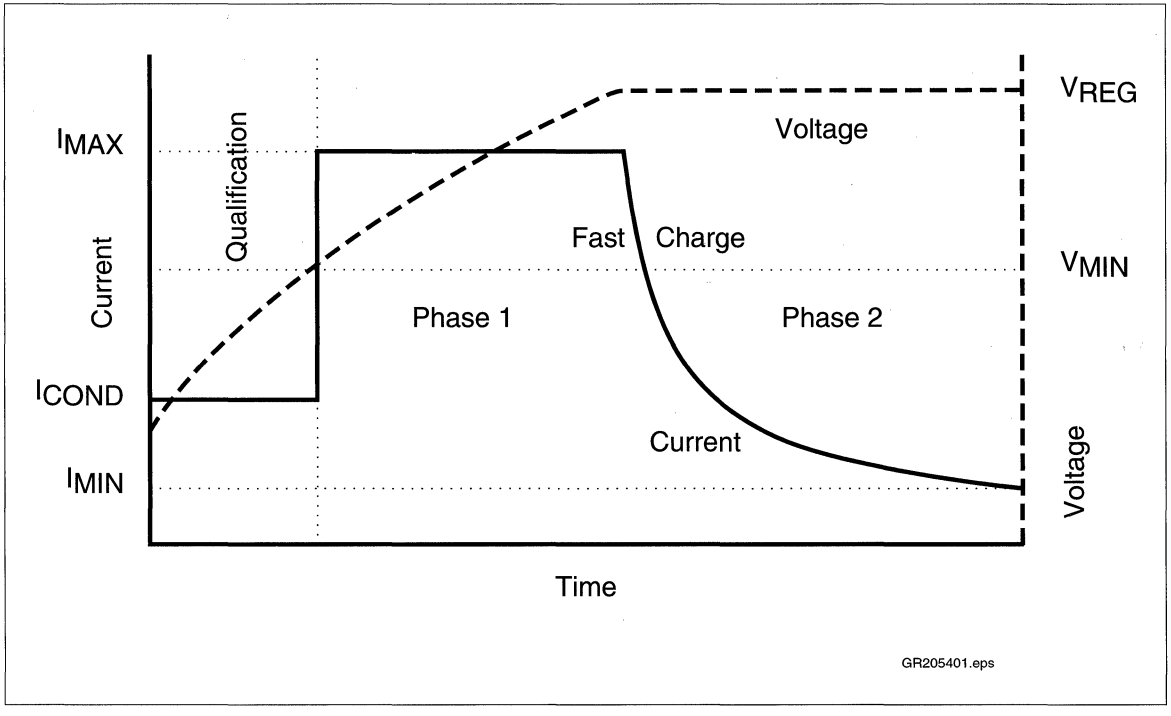


Figure 1. bq2054 Charge Algorithm

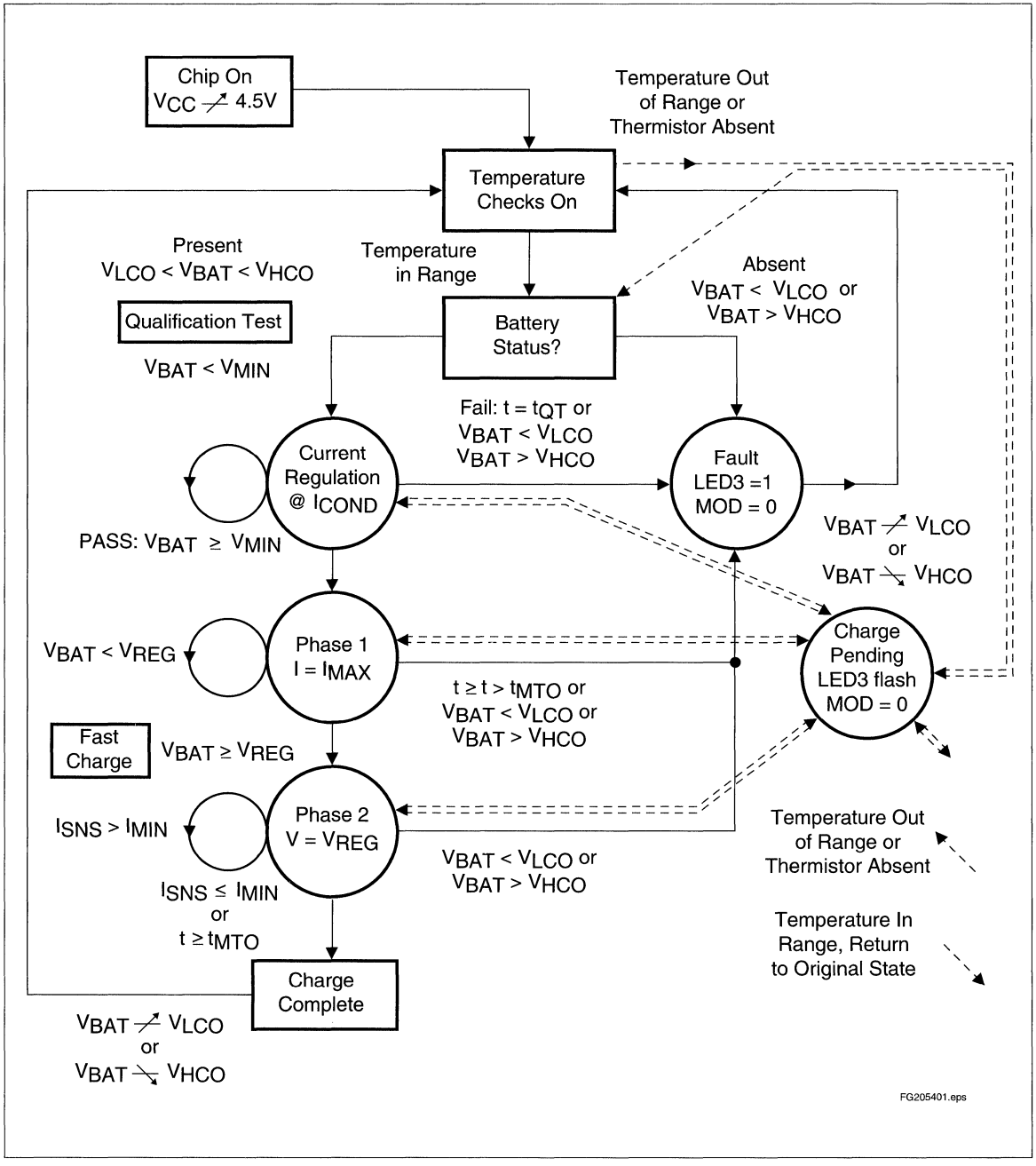


Figure 2. bq2054 State Diagram

4/14

Charge Status Display

Charge status is enunciated by the LED driver outputs LED_1–LED_3. Three display modes are available in the bq2054; the user selects a display mode by configuring pin DSEL. Table 1 shows the three display modes.

The bq2054 does not distinguish between an over-voltage fault and a "battery absent" condition. The bq2054 enters the Fault state, enunciated by turning on LED_3, whenever the battery is absent. The bq2054, therefore, gives an indication that the charger is on even when no battery is in place to be charged.

Configuring the Display Mode and I_{MIN}

DSEL/LED_2 is a bi-directional pin with two functions; it is an LED driver pin as an output and a programming pin as an input. The selection of pull-up, pull-down, or no pull resistor programs the display mode on DSEL per Table 1. The bq2054 latches the programming data sensed on the DSEL input when any one of the following three events occurs:

1. V_{CC} rises to a valid level.
2. The bq2054 leaves the Fault state.
3. The bq2054 detects battery insertion.

The LEDs go blank for approximately 750ms (typical) while new programming data is latched.

Table 1. bq2054 Display Output Summary

Mode	Charge Action State	LED_1	LED_2	LED_3
DSEL = 0 (Mode 1)	Battery absent or over-voltage fault	Low	Low	High
	Pre-charge qualification	Flash	Low	Low
	Fast charging	High	Low	Low
	Charge complete	Low	High	Low
	Charge pending (temperature out of range)	X	X	Flash
	Charging fault	X	X	High
DSEL = 1 (Mode 2)	Battery absent or over-voltage fault	Low	Low	High
	Pre-charge qualification	High	High	Low
	Fast charge	Low	High	Low
	Charge complete	High	Low	Low
	Charge pending (temperature out of range)	X	X	Flash
	Charging fault	X	X	High
DSEL = Float (Mode 3)	Battery absent or over-voltage fault	Low	Low	High
	Pre-charge qualification	Flash	Flash	Low
	Fast charge: current regulation	Low	High	Low
	Fast charge: voltage regulation	High	High	Low
	Charge complete	High	Low	Low
	Charge pending (temperature out of range)	X	X	Flash
	Charging fault	X	X	High

Note: 1 = V_{CC}; 0 = V_{SS}; X = LED state when fault occurred; Flash = ⅙ sec. low, ⅙ sec high.

5/14

Fast charge terminates when the charging current drops below a minimum current threshold programmed by the value of I_{TERM} (see Table 2) and remains below that level for 120 ± 40ms.

Table 2. I_{MIN} Termination Thresholds

I_{TERM}	I_{MIN}
0	$I_{MAX}/10$
1	$I_{MAX}/20$
Float	$I_{MAX}/30$

Figure 3 shows the bq2054 configured for display mode 2 and $I_{MIN} = I_{MAX}/10$.

Voltage and Current Monitoring

The bq2054 monitors battery pack voltage at the BAT pin. The user must implement a voltage divider between the positive and negative terminals of the battery pack to present a scaled battery pack voltage to the BAT pin. The bq2054 also uses the voltage across a sense resistor (R_{SNS}) between the negative terminal of the battery pack and ground to monitor the current into the pack. See Figure 4 for the configuration of this network.

The resistor values are calculated from the following:

Equation 1

$$\frac{RB1}{RB2} = \frac{N * V_{REG}}{2.05V} - 1$$

where:

- N = Number of cells in series
- V_{REG} = Desired fast-charging voltage per cell

These parameters are typically specified by the battery manufacturer. The total resistance presented across the battery pack by RB1 + RB2 should be between 150kΩ and 1MΩ. The minimum value ensures that the divider network does not drain the battery excessively when the power source is disconnected. Exceeding the maximum value increases the noise susceptibility of the BAT pin.

The current sense resistor, R_{SNS} (see Figure 5), determines the fast charge current. The value of R_{SNS} is given by the following:

Equation 2

$$I_{MAX} = \frac{0.250V}{R_{SNS}}$$

where:

- I_{MAX} = Desired maximum charge current

Hold-Off Period

Both V_{HCO} and I_{MIN} terminations are ignored during the first 1.33 ± 0.19 seconds of both the Charge Qualification and Fast Charge phases. This condition prevents premature termination due to voltage spikes that may occur when charge is first applied.

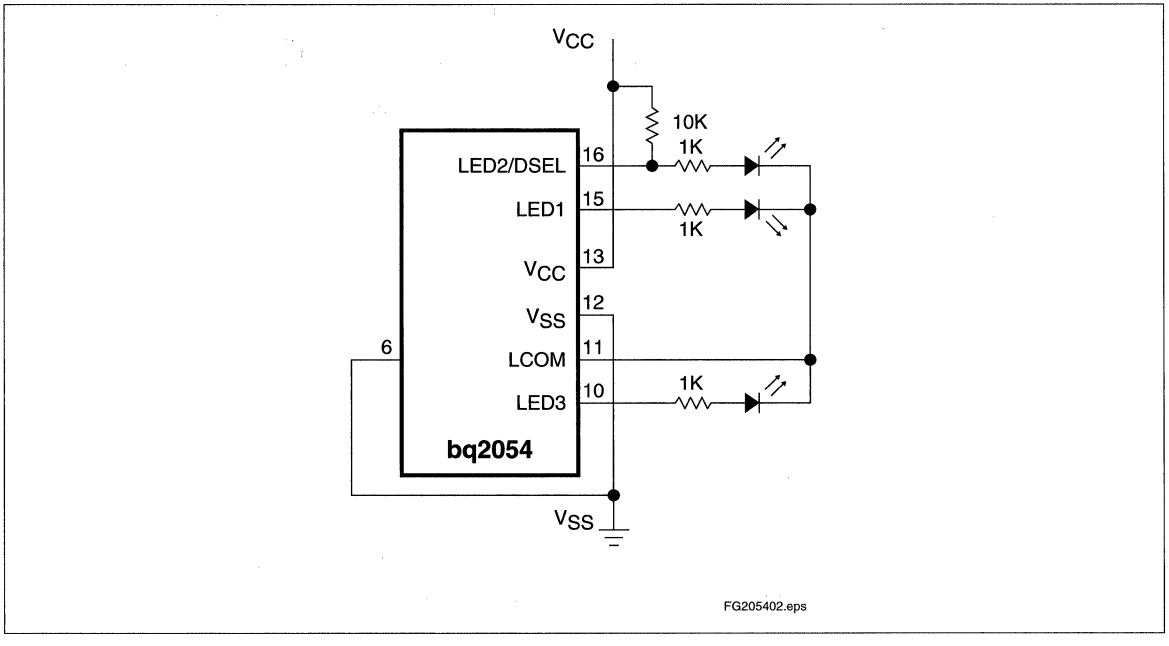


Figure 3. Configured Display Mode/IMIN Threshold

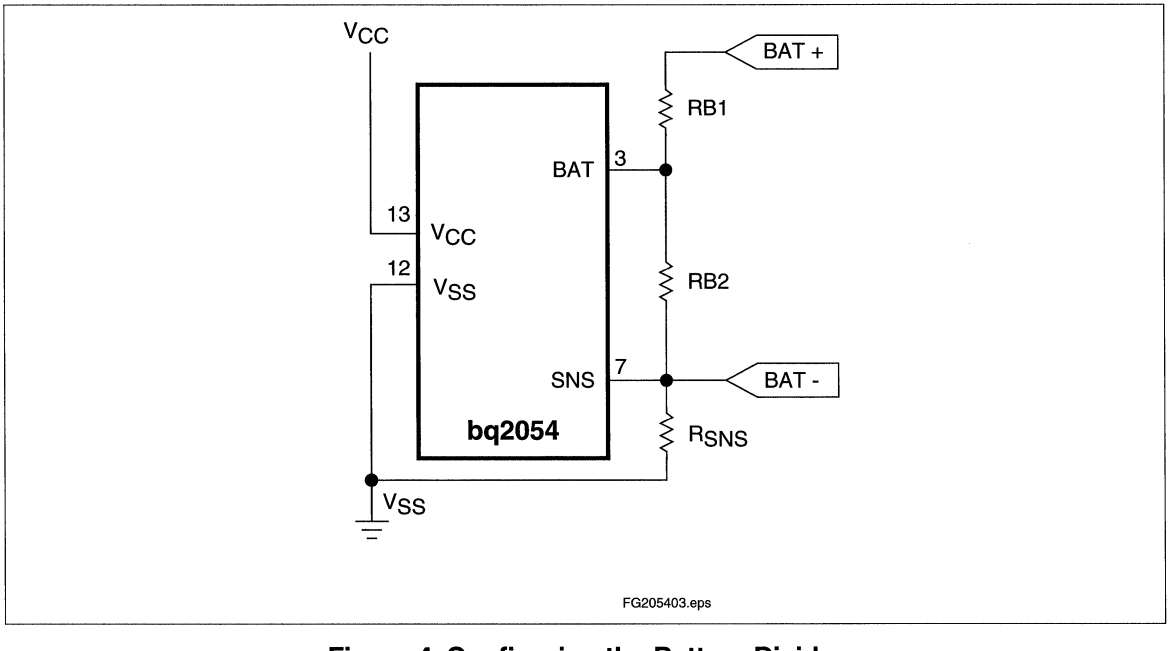


Figure 4. Configuring the Battery Divider

7/14

Battery Insertion and Removal

V_{CELL} is interpreted by the bq2054 to detect the presence or absence of a battery. The bq2054 determines that a battery is present when V_{CELL} is between the High-Voltage Cutoff (V_{HCO} = V_{REG} + 0.25V) and the Low-Voltage Cutoff (V_{LCO} = 0.8V). When V_{CELL} is outside this range, the bq2054 determines that no battery is present and transitions to the Fault state. Transitions into and out of the range between V_{LCO} and V_{HCO} are treated as battery insertions and removals, respectively. The V_{HCO} limit also implicitly serves as an overvoltage charge termination.

Inrush Current Control

Whenever the bq2054 is in the fault or charge-complete state, the $\overline{ICTL}$ output is driven low. This output can be used to disconnect the capacitor usually present in the charger across the positive and negative battery terminals, preventing the cap from supplying large inrush currents to a newly inserted battery. Such inrush currents may trip the overcurrent protection circuitry usually present in Li-Ion battery packs.

Temperature Monitoring

The bq2054 monitors temperature by examining the voltage presented between the TS and SNS pins by a resistor network that includes a Negative Temperature Coefficient (NTC) thermistor. Resistance variations around that value are interpreted as being proportional to the battery temperature (see Figure 6).

The temperature thresholds used by the bq2054 and their corresponding TS pin voltage are:

- TCO (Temperature Cutoff): Higher limit of the temperature range in which charging is allowed. V_{TCO} = 0.4 * V_{CC}
- HTF (High-Temperature Fault): Threshold to which temperature must drop after temperature cutoff is exceeded before charging can begin again. V_{HTF} = 0.44 * V_{CC}
- LTF (Low-Temperature Fault): Lower limit of the temperature range in which charging is allowed. V_{LTF} = 0.6 * V_{CC}

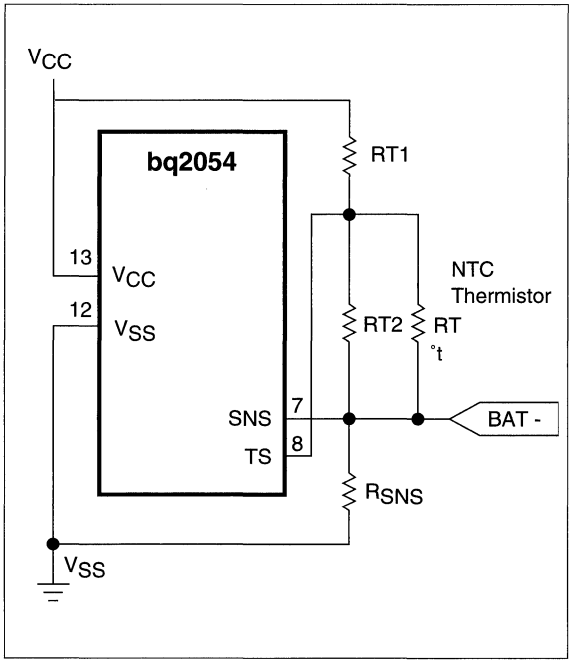


Figure 5. Configuring Temperature Sensing

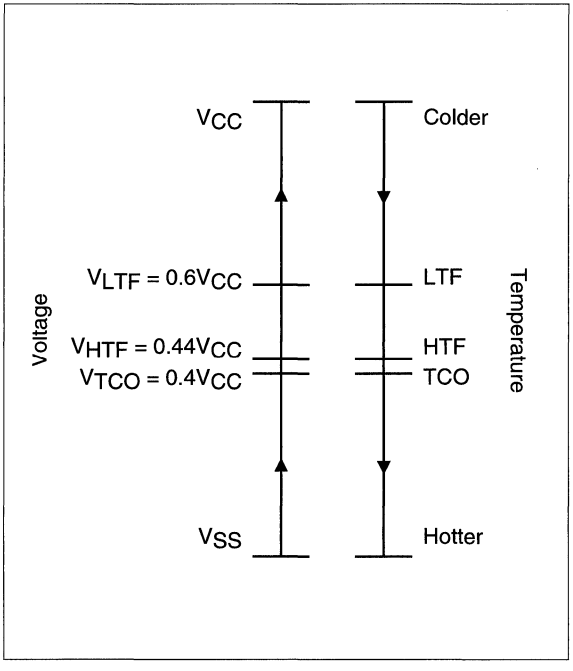


Figure 6. Voltage Equivalent of Temperature

8/14

A resistor-divider network can be implemented that presents the defined voltage levels to the TS pin at the desired temperatures (see Figure 6).

The equations for determining RT1 and RT2 are:

Equation 3

$$0.6 * V_{CC} = \frac{(V_{CC} - 0.250)}{1 + \frac{RT1 * (RT2 + R_{LTF})}{(RT2 * R_{LTF})}}$$

Equation 4

$$0.44 = \frac{1}{1 + \frac{RT1 * (RT2 + R_{HTF})}{(RT2 * R_{HTF})}}$$

where:

- R_{LTF} = thermistor resistance at LTF
- R_{HTF} = thermistor resistance at HTF

TCO is determined by the values of RT1 and RT2. 1% resistors are recommended.

Disabling Temperature Sensing

Temperature sensing can be disabled by placing 10kΩ resistors between TS and SNS and between SNS and V_{CC}.

Maximum Time-Out

MTO is programmed from 1 to 24 hours by an R-C network on the TM pin (see Figure 7) per the equation:

Equation 5

$$t_{MTO} = 0.5 * R * C$$

Where R is in kΩ and C is in μF, t_{MTO} is in hours. The maximum value for C (0.1μF) is typically used.

The MTO timer is reset at the beginning of fast charge and when fast charge transitions from the current regulated to the voltage regulated mode. If MTO expires during the current regulated phase, the bq2054 enters the Fault state and terminates charge. If the MTO timer expires during the voltage regulated phase, fast charging terminates and the bq2054 enters the Charge Complete state.

The MTO timer is suspended (but not reset) during the out-of-range temperature (Charge Pending) state.

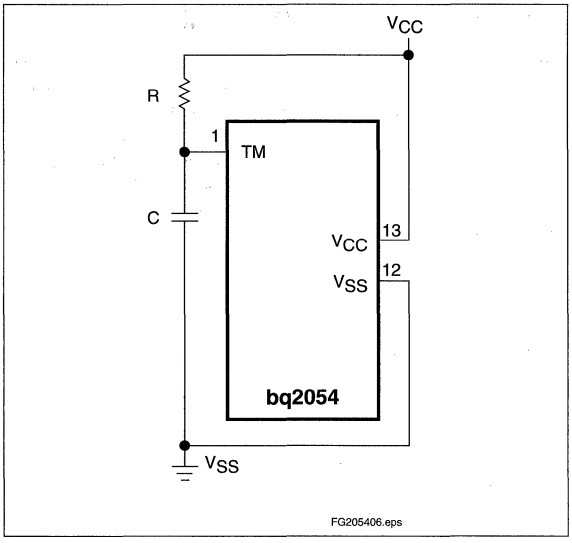


Figure 7. R-C Network for Setting MTO

Charge Regulation

The bq2054 controls charging through pulse-width modulation of the MOD output pin, supporting both constant-current and constant-voltage regulation. Charge current is monitored at the SNS pin, and charge voltage is monitored at the BAT pin. These voltages are compared to an internal reference, and the MOD output modulated to maintain the desired value.

Voltage at the SNS pin is determined by the value of resistor R_{SNS}, so nominal regulated current is set by:

Equation 6

$$I_{MAX} = 0.250V/R_{SNS}$$

The switching frequency of the MOD output is determined by an external capacitor (CPWM) between the pin TPWM and ground, per the following:

Equation 7

$$F_{PWM} = 0.1/C_{PWM}$$

Where C is in μF and F is in kHz. A typical switching rate is 100kHz, implying C_{PWM} = 0.001μF. MOD pulse width is modulated between 0 and 90% of the switching period.

To prevent oscillation in the voltage and current control loops, frequency compensation networks (C or R-C) are typically required on the V_{COMP} and I_{COMP} pins (respectively).

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	-20	+70	°C	Commercial
T_{STG}	Storage temperature	-55	+125	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10 sec. max.

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds ($T_A = T_{OPR}$; V_{CC} = 5V ±10%)

Symbol	Parameter	Rating	Unit	Tolerance	Notes
V_{REF}	Internal reference voltage	2.05	V	1%	T_A = 25°C
	Temperature coefficient	-0.5	mV/°C	10%	
V_{LTF}	TS maximum threshold	0.6 * V_{CC}	V	±0.03V	Low-temperature fault
V_{HTF}	TS hysteresis threshold	0.44 * V_{CC}	V	±0.03V	High-temperature fault
V_{TCO}	TS minimum threshold	0.4 * V_{CC}	V	±0.03V	Temperature cutoff
V_{HCO}	High cutoff voltage	2.3V	V	1%	
V_{MIN}	Under-voltage threshold at BAT	0.2 * V_{CC}	V	±0.03V	
V_{LCO}	Low cutoff voltage	0.8	V	±0.03V	
V_{SNS}	Current sense at SNS	0.250	V	10%	I_{MAX}
		0.050	V	10%	I_{COND}

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{TEMP}	Temperature sense voltage	0	-	V_{CC}	V	V_{TS} - V_{SNS}
V_{CELL}	Per cell battery voltage input	0	-	V_{CC}	V	V_{BAT} - V_{SNS}
I_{CC}	Supply current	-	2	4	mA	Outputs unloaded
I_{IZ}	DSEL tri-state open detection	-2	-	2	µA	Note 2
	I_{TERM} tri-state open detection	-2		2	µA	
V_{IH}	Logic input high	V_{CC}-0.3	-	-	V	DSEL, I_{TERM}
V_{IL}	Logic input low	-	-	V_{SS}+0.3	V	DSEL, I_{TERM}
V_{OH}	LED_{1-3}, $\overline{ICTL}$, output high	V_{CC}-0.8	-	-	V	$I_{OH} \leq 10mA$
	MOD output high	V_{CC}-0.8	-	-	V	$I_{OH} \leq 10mA$
V_{OL}	LED_{1-3}, $\overline{ICTL}$, output low	-	-	V_{SS}+0.8V	V	$I_{OL} \leq 10mA$
	MOD output low	-	-	V_{SS}+0.8V	V	$I_{OL} \leq 10mA$
	LCOM output low	-	-	V_{SS}+0.5	V	$I_{OL} \leq 30mA$
I_{OH}	LED_{1-3}, $\overline{ICTL}$, source	-10	-	-	mA	$V_{OH} = V_{CC}$-0.5V
	MOD source	-5.0	-	-	mA	$V_{OH} = V_{CC}$-0.5V
I_{OL}	LED_{1-3}, $\overline{ICTL}$, sink	10	-	-	mA	$V_{OL} = V_{SS}$+0.5V
	MOD sink	5	-	-	mA	$V_{OL} = V_{SS}$+0.8V
	LCOM sink	30	-	-	mA	$V_{OL} = V_{SS}$+0.5V
I_{IL}	DSEL logic input low source	-	-	+30	µA	V = V_{SS} to V_{SS}+ 0.3V, Note 2
	I_{TERM} logic input low source	-	-	+70	µA	V = V_{SS} to V_{SS}+ 0.3V
I_{IH}	DSEL logic input high source	-30	-	-	µA	V = V_{CC} - 0.3V to V_{CC}
	I_{TERM} logic input high source	-70	-	-	µA	V = V_{CC} - 0.3V to V_{CC}

Notes: 1. All voltages relative to V_{SS} except where noted.

2. Conditions during initialization after V_{CC} applied.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
R_{BATZ}	BAT pin input impedance	50	-	-	MΩ	
R_{SNSZ}	SNS pin input impedance	50	-	-	MΩ	
R_{TSZ}	TS pin input impedance	50	-	-	MΩ	
R_{PROG1}	Soft-programmed pull-up or pull-down resistor value (for programming)	-	-	10	kΩ	DSEL
R_{PROG2}	Pull-up or pull-down resistor value	-	-	3	kΩ	I_{TERM}
R_{MTO}	Charge timer resistor	20	-	480	kΩ	

Timing ($T_A = T_{OPR}$; V_{CC} = 5V ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{MTO}	Charge time-out range	1	-	24	hours	See Figure 7
t_{QT}	Pre-charge qual test time-out period	-	t_{MTO}	-	-	
t_{HO}	Termination hold-off period	1.14	-	1.52	sec.	
t_{IMIN}	Min. current detect filter period	80		160	msec.	
F_{PWM}	PWM regulator frequency range	-	100		kHz	C_{PWM} = 0.001µF (equation 7)

Capacitance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
C_{MTO}	Charge timer capacitor	-	-	0.1	µF
C_{PWM}	PWM R-C capacitance	-	0.001	-	µF

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	5, 7, 8, 10	Value Change	Changed V_{SNS} and I_{MAX}
2	5, 10	Value Change	Changed V_{REF}
3	10	Coefficient Addition	Temperature coefficient added
4	5	New state diagram	Diagram inserted
4	1, 2, 8, 12	NC pin replaced with $\overline{ICTL}$	
4	3, 5, 13	Termination hold-off period added I_{MIN} detect filtering added	
5	11	V_{HCO} Rating changed to 2.3V V_{HCO} Tolerance changed to 1%	Changed values for V_{HCO}
6	13	t_{QT} in Timing Specifications	t_{QT} changed from (0.16 * t_{MTO}) to t_{MTO}
7	5	I_{TERM} in Table 2	Z changes to Float
7	8	Figure 6	RB1 and RB2 changed to RT1 and RT2
8	10	T_{OPR}	Deleted industrial temperature range.

Notes: Change 3 = April 1996 C changes from Dec. 1995 B.
Change 4 = Sept. 1996 D changes from April 1996 C.
Change 5 = Nov. 1996 E changes from Sept. 1996 D.
Change 6 = Oct. 1997 F changes from Nov. 1996 E.
Change 7 = Oct. 1997 G changes from Oct. 1997 F.
Change 8 = June 1999 H changes from Oct. 1997 G.

Ordering Information

bq2054

Package Option:
PN = 16-pin plastic DIP
SN = 16-pin narrow SOIC

Device:
bq2054 Li-Ion Fast-Charge IC

UNITRODE

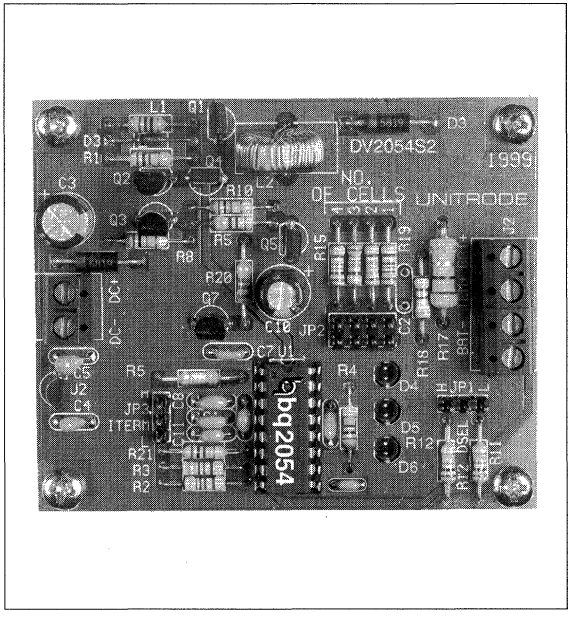
Product Brief **DV2054S2**

Li-Ion Charger Development System

Control of On-Board PNP Switch-Mode Regulator

Features

- bq2054 fast-charge control evaluation and development, based on switching buck converter with low-side battery-current sensing
- On-board configuration for fast charge of 1, 2, 3, or 4 Li-Ion cells
- Charge termination by selectable minimum current, or maximum time-out
- Constant current (up to 1.25A) and constant voltage (up to 16.8V) provided by on-board switch-mode regulator
- Jumper-configurable LED display
- Direct connections for battery and thermistor
- Maximum charge time of 5 hours



General Description

The DV2054S2 Development System provides a development environment for the bq2054 Lithium Ion Fast-Charge IC. The DV2054S2 incorporates a bq2054 and a buck-type switch-mode regulator to provide fast charge control for 1 through 4 Li-Ion cells.

Fast charge is preceded by a pre-charge qualification period.

Fast charge termination occurs on:

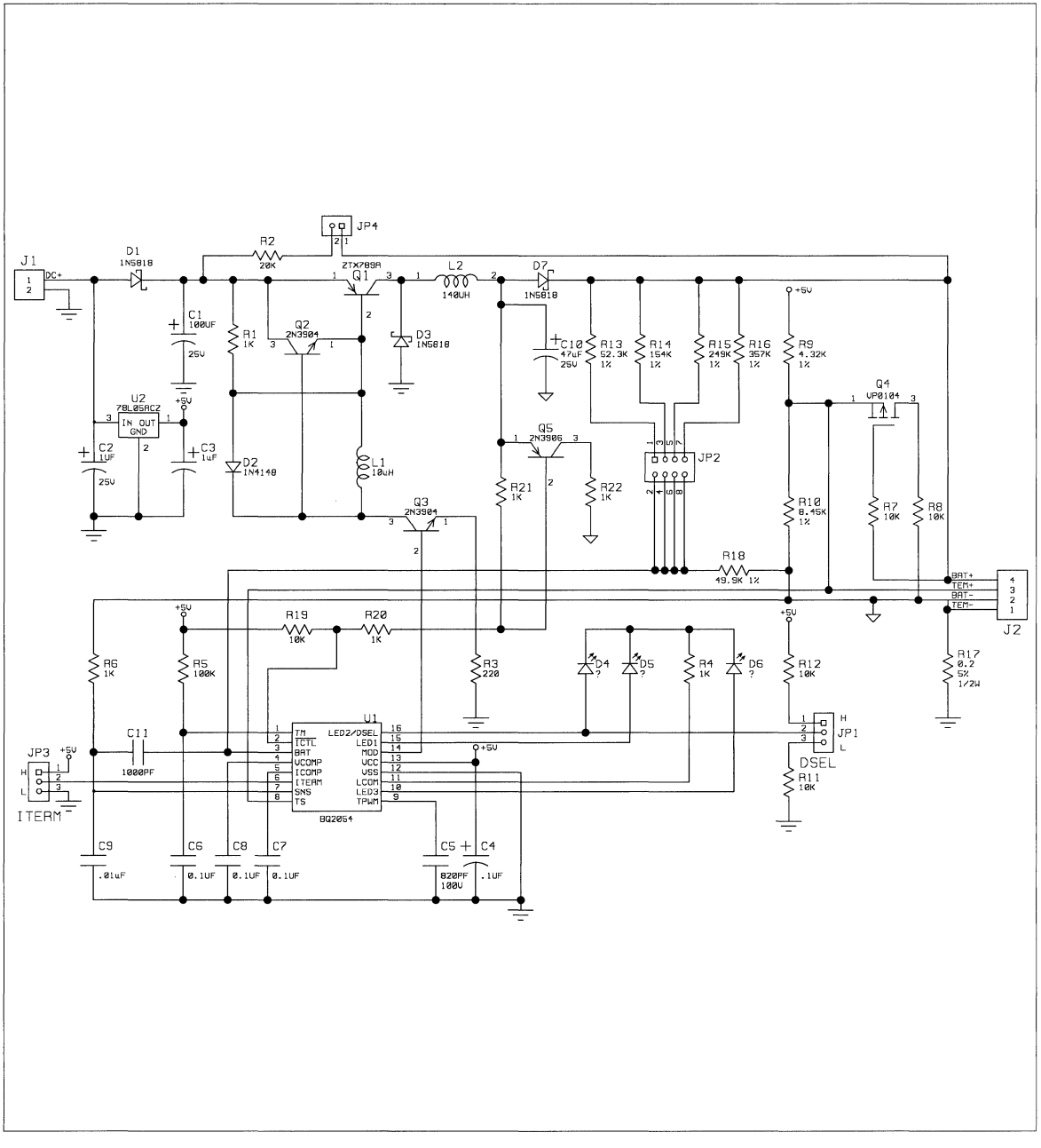
- Minimum current – I_{MAX} divided by 10, 20, or 30
- Maximum time-out

The bq2054 can be reset and a new charge cycle started by applicaton of power to the board or battery replacement.

The user provides a DC power supply and batteries and configures the board for the number of cells, the minimum current threshold, and the LED display mode. The board has direct connections for the battery and the provided thermistor.

Before using the DV2054S2 board, please review the bq2054 data sheet. A full data sheet for this product is available on the Unitrode web site, or you may contact the factory for one.

DV2054S2 Board Schematic



Rev. B Board

Low-Dropout Li-Ion Charge-Control ICs with AutoComp™ Charge-Rate Compensation

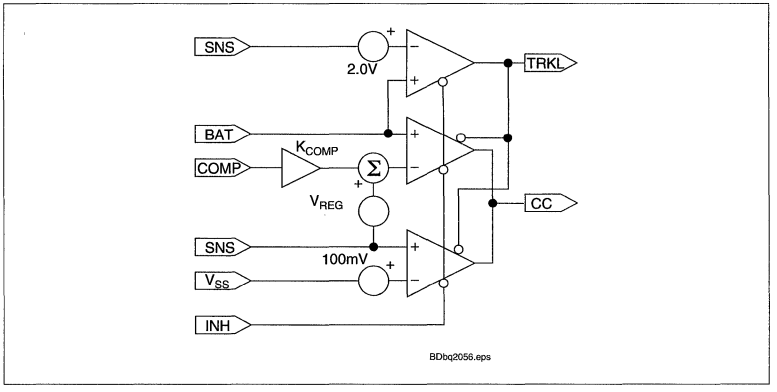
Features

- Significant reduction in charge time with AutoComp charge-rate compensation
- Ideal for low-dropout linear regulator design
- 1-cell, 2-cell, and programmable multicell versions
- Low-cost charger implementation with minimum number of external components
- Programmable current limit to accommodate any battery size
- Interface to external trickle charger for reviving deeply discharged batteries
- High-accuracy charge control
- Sleep mode for low power consumption
- Direct battery voltage sense without resistive dividers (bq2056 and bq2056T)
- Small 8-pin SOIC package

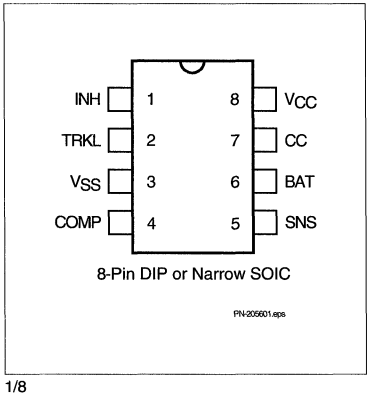
General Description

The bq2056 series ICs are low-cost precision linear charge-control devices for Li-Ion batteries. With a minimum number of external components, the bq2056 is a complete low-dropout linear charger. The dropout voltage is typically less than 0.5V when the bq2056 is used with an external PNP transistor or P-channel FET. Features include proprietary automatic charge-rate compensation (AutoComp) and a trickle-charger interface output for reviving deeply discharged cells. The bq2056 supports a single-cell 4.1V pack and the 2056T supports a two-cell 8.2V pack. The bq2056V may be externally programmed for supporting other voltages. All versions feature a sleep mode for low-power applications.

Functional Block Diagram



Pin Connections



Pin Names

INH	Charge-inhibit input	SNS	Current sense input
TRKL	Trickle-charge interface output	BAT	Battery voltage input
		CC	Charge control output
V_{SS}	Ground		
COMP	Charge-rate compensation input	V_{CC}	Supply input

Pin Descriptions:

INH **Charge-inhibit input**

When input to this pin is high, the bq2056 suspends the charge in progress and places the device in sleep mode. When input is low, the bq2056 resumes operation.

TRKL **Trickle-charge interface output**

This output is driven low if the battery voltage is less than an internal threshold level and INH is low. This open-drain output can enable an external trickle charger to revive a deeply discharged battery.

V_{SS} **Ground**

COMP **Charge-rate compensation input**

This input is used to set the charge-rate compensation level. The voltage regulation output may be programmed to vary as a function of the charge current delivered to the battery. This feature, called AutoComp, provides compensation for internal cell impedance and voltage drops in protection circuitry and therefore may be used to safely reduce charging time. Connecting this pin to V_{SS} disables the AutoComp feature.

SNS **Current sense input**

Battery current is sensed via the voltage developed on this pin by an external sense-resistor, connected in series with the negative terminal of the battery pack.

BAT **Battery voltage input**

This is the battery voltage sense input. It is tied directly to the positive side of the battery pack on bq2056 and bq2056T versions. A simple resistive divider is required to generate this input for bq2056V.

CC **Charge-control output**

CC is an open-collector output that is used to control the charging current to the battery.

V_{CC} **V_{CC} supply input**

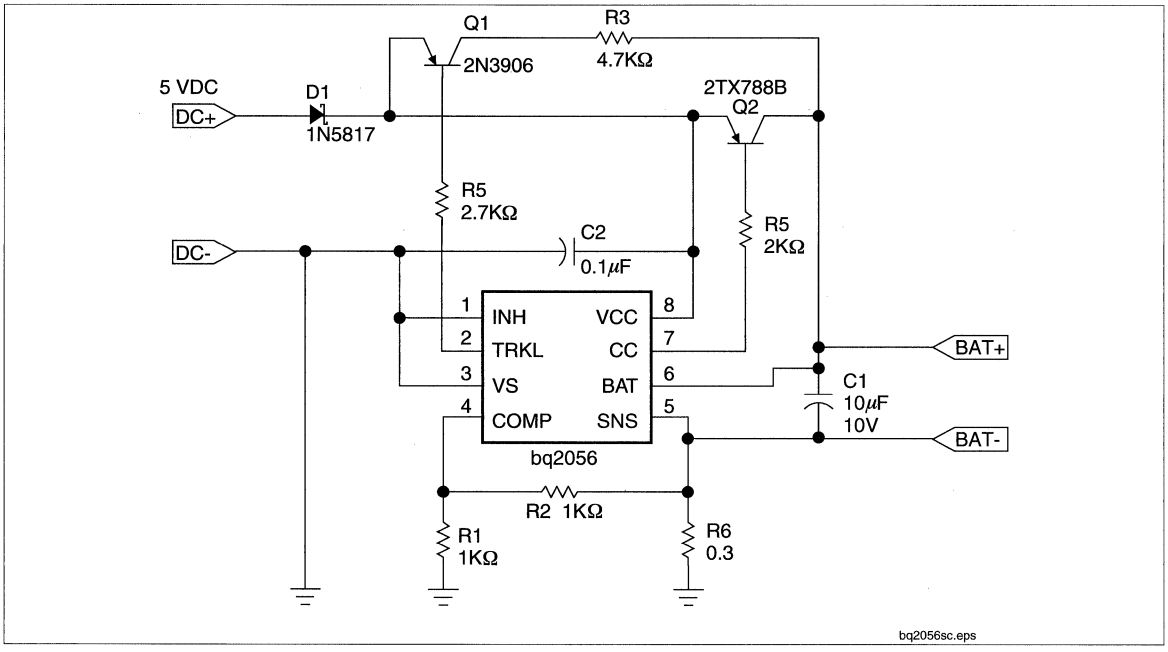


Figure 1. Low-Dropout Single-Cell Li-Ion Charger

Functional Description

The bq2056 supports a precision current- and voltage-limited charging system for Li-Ion batteries. The no-load voltage regulation references (V_{REG}) for the bq2056 and bq2056T are maintained at 4.1V and 8.2V, respectively. The bq2056V provides variable regulation to accommodate a wide range of charge voltages and may be used to meet tighter tolerance requirements through external trimming. The functional block diagram for the bq2056 is on the first page of this data sheet, and Figure 1 illustrates a typical application.

Charge Algorithm

The bq2056 completes the charge cycle in two phases. A constant current phase replenishes approximately 70% of battery capacity, while an accurate voltage regulation phase completes the charge.

Figure 2 shows a typical charge algorithm for bq2056, including charge qualification, current regulation, and voltage regulation phases.

Charge Qualification

During charge qualification the bq2056 detects a low battery and reports this status on pin TRKL. Detection is accomplished by comparing pin BAT voltage to the internal threshold V_{MIN}. While pin BAT voltage is less than V_{MIN} and pin INH is low, the open-drain output TRKL is driven low and the voltage/current regulator is disabled (CC=high-Z). In the bq2056V, low-voltage detection occurs when the voltage on pin BAT is less than or equal to V_{MIND}. As shown in Figure 1, TRKL enables an external trickle-charge circuit to bring the battery voltage up to V_{MIN} or V_{MIND}.

Current Regulation

The bq2056 provides current regulation while the pack voltage is below the voltage limit. Charge-current feedback, applied through pin SNS, maintains regulation around a threshold of V_{SNS}. The following formula calculates the value of the sense-resistor connected in series with the negative terminal of the battery pack (Figure 3):

$$R_{SNS} = 0.1 / I_{MAX}$$

where I_{MAX} is the maximum charging current. I_{MAX} should not exceed 1A.

An external PNP or power P-FET may be used as the series pass element with control provided through output pin CC.

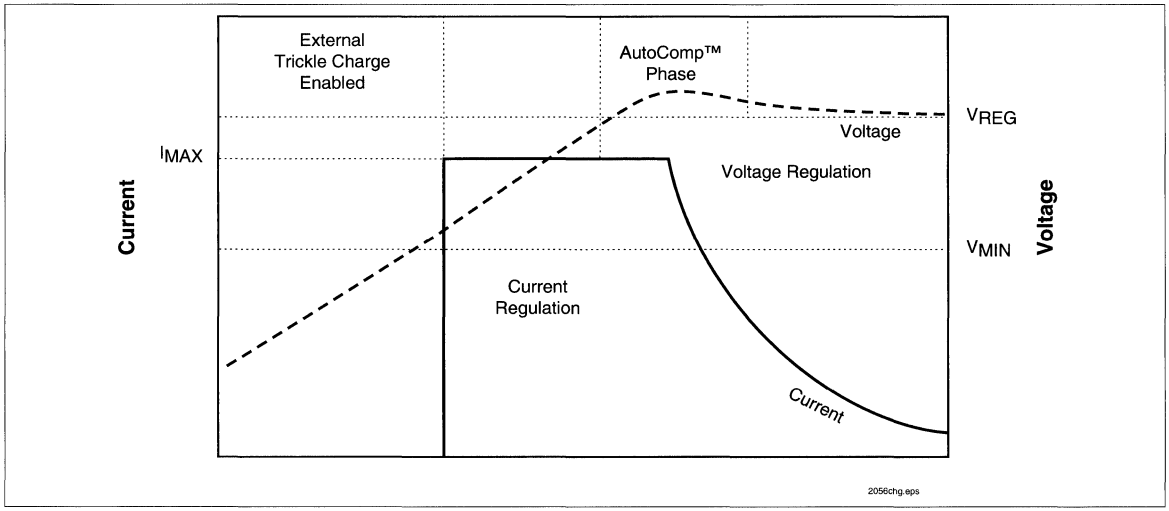


Figure 2. bq2056 Charge Algorithm

Voltage Regulation

Voltage regulation feedback is through pin BAT. This pin is connected directly to the pack in the bq2056 and bq2056T. This voltage is compared with the voltage regulation reference, V_{REG}. In the bq2056V, a resistive divider may be used to generate this input (Figure 4). In this case, the voltage presented on pin BAT is compared with the internal reference voltage V_{REF}. The resistor values R_{B1} and R_{B2} (Figure 4) are calculated based on the following equation:

$$\frac{R_{B1}}{R_{B2}} = \frac{N * V_{CELL}}{V_{REF}} - 1$$

where

N = Number of cells in series

V_{CELL} = Manufacturer-specified charging voltage

Automatic Charge-Rate Compensation (AutoComp) Feature

To reduce charging time, the bq2056 series uses the proprietary AutoComp technique to compensate safely for internal impedance of battery and any voltage drops in the protection circuitry. This maximizes battery's capacity while reducing charging time. Compensation is through input pin COMP (Figure 5). A portion of the current-sense voltage, presented through this pin, is scaled by a factor of K_{COMP} and summed with the regulation reference, V_{REG}. This process increases the output voltage to compensate for the battery's internal impedance and undesired voltage drops in the circuit.

For bq2056 and bq2056T, the voltage across the battery pack, V_{PAK}, is

$$V_{PAK} = V_{REG} + (K_{COMP} * \text{voltage on pin COMP})$$

For bq2056V, the compensation voltage is added to the product of the internal voltage reference, V_{REF}, and the gain, KDIV, of the external resistive divider between the battery pack and BAT input, (Figure 4).

$$V_{PAK} = (V_{REF} * K_{DIV}) + (K_{COMP} * \text{voltage on pin COMP})$$

Sleep Mode

The charge function may be disabled through pin INH. When INH is driven high, internal current consumption is reduced, and pins CC and TRKL assumes a high-impedance output state.

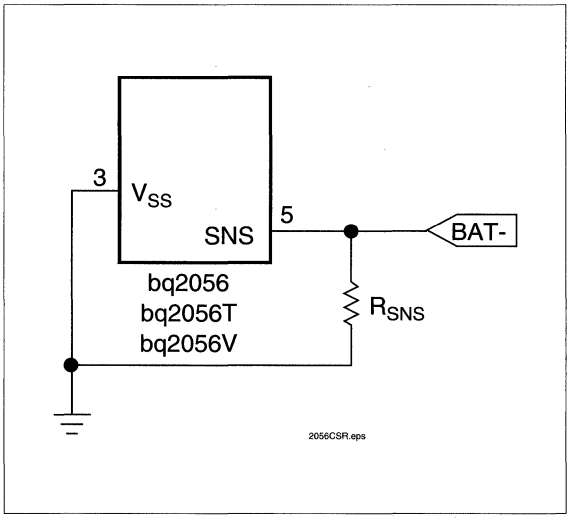


Figure 3. Current-Sensing Resistor

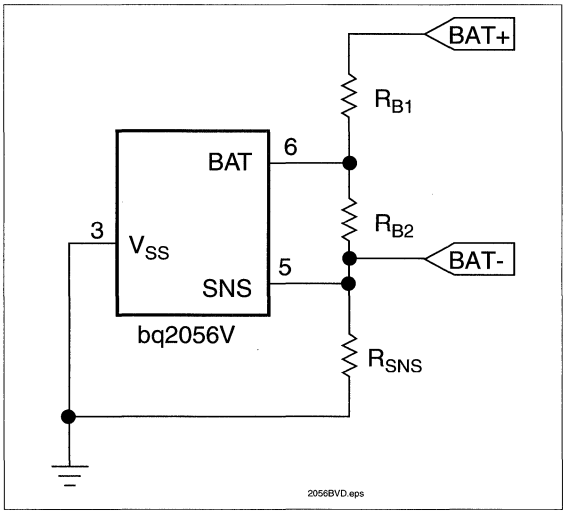


Figure 4. Battery Voltage Divider for bq2056V

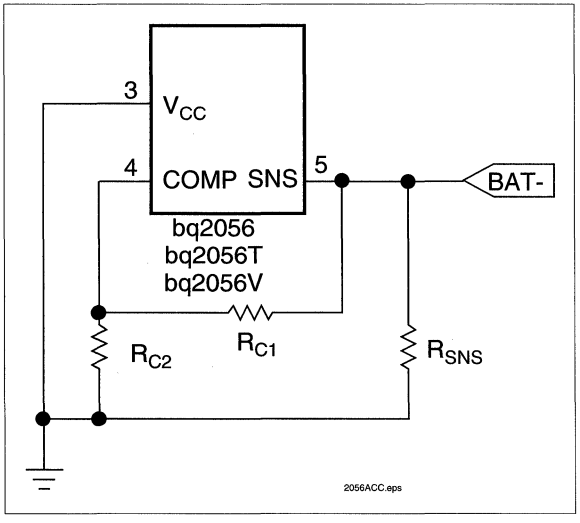


Figure 5. AutoComp Circuit

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+18	V	
V_T	DC voltage applied on any pin (excluding V_{CC}) relative to V_{SS}	-0.3	V_{CC}+0.3	V	
T_{OPR}	Operating ambient temperature	-20	70	°C	
T_{STG}	Storage temperature	-40	125	°C	
T_{SOLDER}	Soldering temperature	-	260	°C	10s max.
P_D	Power dissipation		300	mW	

DC Thresholds (T_A=T_{OPR} and V_{CC} = 5–17V unless otherwise specified)

Symbol	Parameter	Rating	Unit	Tolerance	Notes
V_{REG} (bq2056)	Voltage regulation reference	4.10	V	±1%	
V_{REG} (bq2056T)	Voltage regulation reference	8.20	V	±1%	
V_{REF} (bq2056V)	Voltage regulation reference	3.35	V	±1%	
V_{SNS}	Current regulation reference	100	mV	±15%	
V_{MIN} (bq2056)	Trickle-charge voltage reference	2.0	V	±15%	
V_{MIN} (bq2056T)	Trickle-charge voltage reference	4.0	V	±15%	
V_{MIND} (bq2056V)	Trickle-charge voltage reference	1.64	V	±15%	
K_{COMP} (bq2056)	AutoComp constant	2.0	-	±10%	
K_{COMP} (bq2056T)	AutoComp constant	4.0	-	±10%	
K_{COMP} (bq2056V)	AutoComp constant	1.7	-	±10%	

6/8

Recommended DC Operating Conditions (T_A=25°C)

Symbol	Parameter	Min	Typical	Max	Units	Notes
V_{CC}	Supply voltage relative to V_{SS}	5.0	-	17.0	V	
I_{CC}	Supply current	-	1	2	mA	INH = LOW
I_{CCS}	Sleep current	-	10	30	µA	INH = HIGH
V_{IL}	Input low	-	-	0.5	V	Pin INH
V_{IH}	Input high	2.0	-	-	V	Pin INH
V_{OL}	Output low	-	-	0.4	V	Pin TRKL, I_{OL} = 1mA
I_{OH}	Leakage current	-	-	1	µA	Pin TRKL
I_{SNK}	Sink current	-	-	40	mA	Pin CC

Impedance

Symbol	Parameter	Min	Typical	Max	Units	Notes
R_{BAT}	BAT pin input impedance	-	1	-	MΩ	
R_{SNS}	SNS pin input impedance	-	100	-	kΩ	
R_{COMP}	COMP pin input impedance	-	100	-	kΩ	

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	6	Changed tolerance for V_{REG} and V_{REF} in DC Thresholds table	Was: ±0.7% with ±0.5% variation over power supply and temperature range Is: ±1% over power supply and temperature range
1	6	Changed value and tolerance for K_{COMP} in DC Thresholds table	Was: 2.0, ±15% Is: bq2056: 2.0, ±10% bq2056T: 4.0, ±10% bq2056V: 1.7, ±10%

Note: Change 1 = Oct. 1998 B changes from March 1998.

Ordering Information

bq2056

Package Option:
PN = 8-pin plastic DIP
SN = 8-pin narrow SOIC

Device:
bq2056 Li-Ion Fast-Charge IC for One Cell
bq2056T Li-Ion Fast-Charge IC for Two Cells
bq2056V Programmable Li-Ion Fast-Charge IC

UNITRODE

bq2902

Rechargeable Alkaline Charge/Discharge Controller IC

Features

- Safely charges two rechargeable alkaline batteries such as Renewal® from Rayovac®
- Terminates pulsed charge with maximum voltage limit
- Contains LED charge status output
- Features a pin-selectable low-battery cut-off
- Pre-charge qualification indicates fault condition
- Available in 8-pin 300-mil DIP or 150-mil SOIC

General Description

The bq2902 is a low-cost charger for rechargeable alkaline batteries such as Renewal® batteries from Rayovac®. The bq2902 combines sensitive, full-charge detection for two rechargeable alkaline cells, with a low-battery cut-off for overdischarge protection.

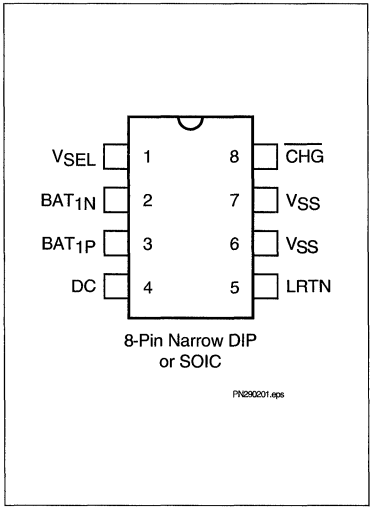
Designed for system integration into a two-cell system, the bq2902 can improve the service life of the rechargeable alkaline cells by properly managing the charge and discharge. The bq2902 requires a voltage limited current source to generate the proper charge pulses for the Renewal® cell. Each cell is individually monitored to ensure full charge without a damaging overcharge.

Charge completion is indicated when the average charge rate falls below approximately 3% of the fast charge rate. A status output is provided to indicate charge in progress, charge complete, or fault indication.

The bq2902 avoids over-depleting the battery by using the internal end-of-discharge control circuit. The bq2902 also eliminates the external power switching transistors needed to separately charge individual Renewal cells.

For safety, charging is inhibited if the per-cell voltage is greater than 3.0V during charge (closed-circuit voltage), or if the cell voltage is less than 0.4V (open-circuit voltage).

Pin Connections



8-Pin Narrow DIP
or SOIC

Pin Names

DC	Charging supply input
$\overline{CHG}$	Battery status output
BAT_{1P}	Battery 1 positive input
BAT_{1N}	Battery 1 negative input
V_{SS}	Battery 2 negative input IC ground
LRTN	System load return
V_{SEL}	End-of-discharge voltage select input

Pin Descriptions

DC **DC supply input**

This input is used to charge the rechargeable alkaline cells and power the bq2902 during charge. To charge the batteries, this input should be connected to a current-source limited to 300 mA. If the DC input current is greater than 300mA, the power dissipation limits of the package may be exceeded. The DC input should also be capable of supplying a minimum of 3.3V and should not exceed 5.5V.

$\overline{CHG}$ **Charge status**

This open-drain output is used to signify the battery charging status and is valid only when DC is applied.

V_{SEL} **End-of-discharge select input**

This three-level input selects the desired end-of-discharge cut-off voltage for the bq2902. V_{SEL} = BAT_{1P} selects an EDV of 1.10V. V_{SEL} floating selects EDV = 1.0V. V_{SEL} = V_{SS} selects EDV = 0.9.V

BAT_{1P} **Battery 1 positive input**

This input connects to the positive terminal of the battery designated BAT_1 (see Figure 3). This pin also provides power to the bq2902 when DC is not present.

BAT_{1N} **Battery 1 negative input**

This input connects to the negative terminal of the battery designated BAT_1 (see Figure 3).

V_{SS} **Battery 2 negative input/IC ground**

This input connects to the negative terminal of the battery designated BAT_2 (see Figure 3).

LRTN **Load return**

This open-drain pull-down output is typically used as a low-side switch. High-side load switching is also possible with the addition of an external P-FET.

Functional Description

Figure 1 is a block diagram outlining the major components of the bq2902.

Figure 2 illustrates the charge control and display status during a bq2902 cycle. Table 1 outlines the vari-

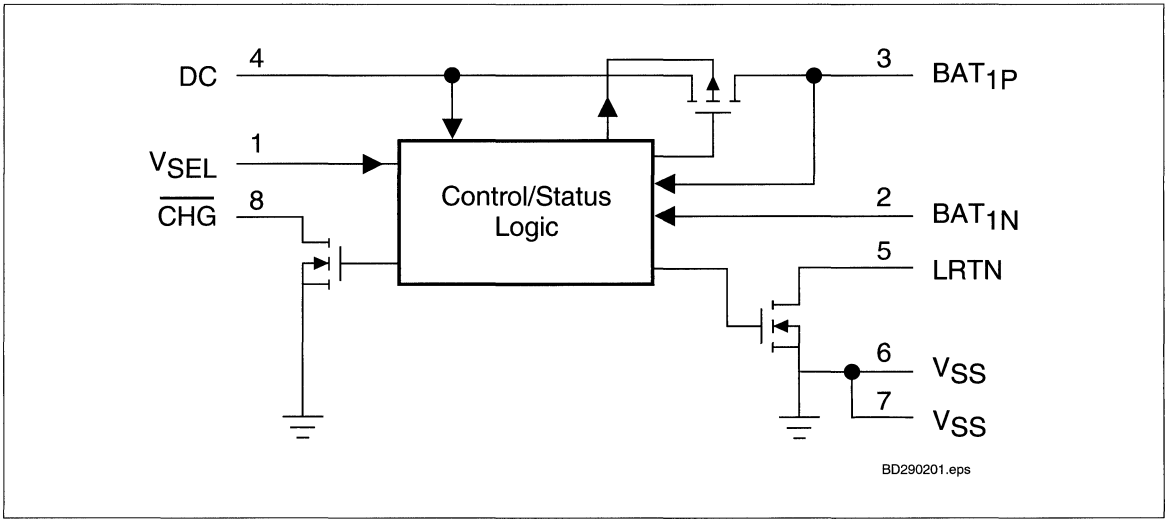


Figure 1. Functional Block Diagram

ous operational states and their associated conditions which are described in detail in the following section. Figure 3 is an application example.

Charge Initiation

The bq2902 always initiates and performs a charge cycle whenever a valid DC input is applied. A charge cycle consists of pulse charging the battery and then checking for a termination condition. The charging section explains charging in greater detail.

Charge Pre-Qualification

After DC is applied, the bq2902 checks the open-circuit voltage (V_{OCV}) of each cell for an undervoltage condition (V_{MIN} = 0.4V) and begins a charge cycle when the V_{OCV} of all cells is above V_{MIN}. If V_{OCV} of any cell is below V_{MIN}, the bq2902 enters a charge-pending mode and indicates a fault condition (see Table 1). The bq2902 remains in a charge-pending mode until V_{OCV} of each cell is above V_{MIN}.

Charge Termination

Once a charge cycle begins, the bq2902 terminates charge when the average charge rate falls below 3% of the maximum charge rate. The bq2902 also terminates charge when the closed-circuit voltage (V_{CCV}) of any cell exceeds 3.0V (V_{FLT}) during charge and indicates a fault condition on the $\overline{CHG}$ output (see Table 1).

Charge Re-Initiation

If DC remains valid, the bq2902 suspends all charge activity after full-charge termination. A charge cycle is re-initiated when all cell potentials fall below 1.4V. The rechargeable alkaline cells, unlike other rechargeable chemistries, do not require a maintenance charge to keep the cells in a fully charged state. The self-discharge rate for the Renewal cells is typically 4% per year at room temperature.

Charge Status Indication

Table 1 and Figure 2 outline the various charge action states and the associated BAT_{1P}, and $\overline{CHG}$ output states. The charge status output is designed to work with an LED indicator. In all cases, if DC is not present at the DC pin, or if the DC supply is less than the voltage at the BAT_{1P} pin, the CHG output is held in a high-impedance condition.

Charging

The bq2902 controls charging by periodically connecting the DC current-source to the battery stack, not to the individual battery cells. The charge current is pulsed from the internal clock at approximately a 80Hz rate on the BAT_{1P} pin.

The bq2902 pulse charges the battery for approximately 10ms of every 12.5ms, when conditions warrant. The bq2902 measures the open-circuit voltage (V_{OCV}) of each battery cell during the idle period. If a single-cell potential of any battery is above the maximum open-circuit voltage (V_{MAX} = 1.63V ±3%), the following pulses are

Table 1. bq2902 Operational Summary

Charge Action State	Conditions	BAT_{1P} Input	$\overline{CHG}$ Output
DC absent	$V_{DC} < V_{BAT1P}$	Low battery detection per V_{SEL}	Z
Charge initiation	DC applied	-	-
Charge pending/ fault	$V_{OCV} < 0.4V$[1] or $V_{CCV} > 3.0V$[2]	-	⅔ sec = Low ⅔ sec = Z
Charge pulse	$V_{OCV} \leq$ 1.63V before pulse	Charge pulsed @ 80Hz per Figure 2	⅙ sec = Low ⅙ sec = Z
Pulse skip	V_{OCV} > 1.63V before pulse	Pulse skipped per Figure 2	⅙ sec = Low ⅙ sec = Z
Charge complete	Average charge rate falls below 3% of the fast charge rate	Charge complete	Low

Notes: 1. V_{OCV} = Open-circuit voltage of each cell between positive and negative leads.

2. V_{CCV} = Closed-circuit voltage.

skipped until all cell potentials fall below the V_{MAX} limit. Charging is terminated when the average charge rate falls below approximately 3% of the maximum charge rate. Once charging is terminated, the internal charging FET remains off, and the $\overline{CHG}$ output becomes active per Table 1 and Figure 2. With DC applied, the internal discharge FET will always remain on.

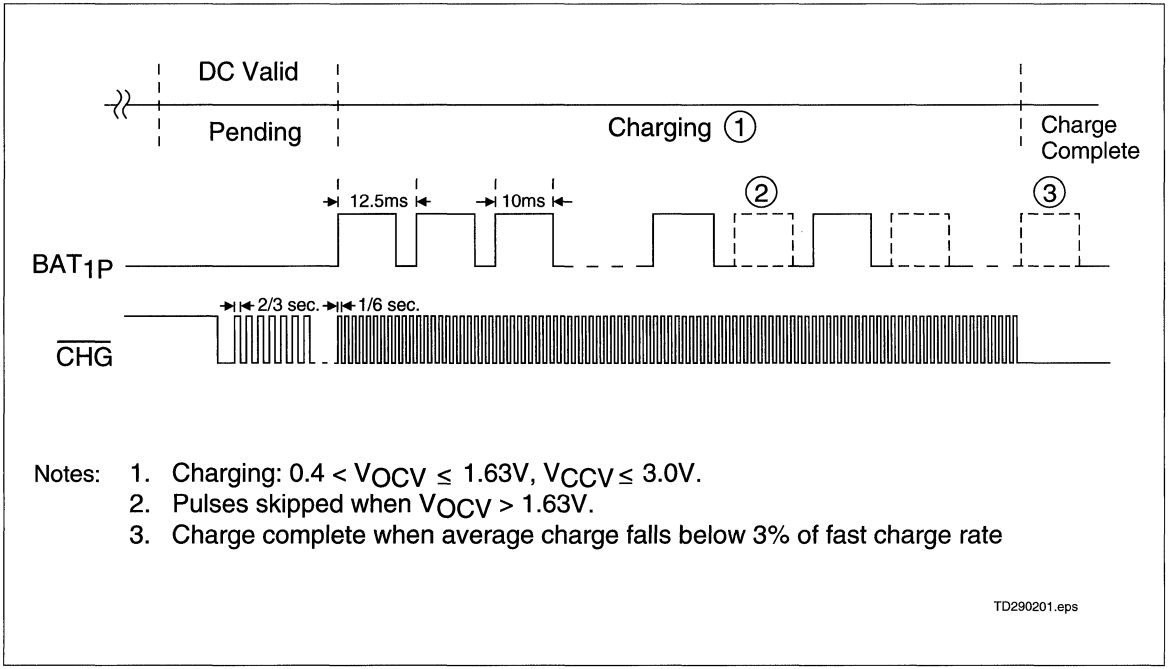
End-of-Discharge Control

When DC is not present or less than the voltage present on the BAT_{1P} pin, the bq2902 power is supplied by the voltage present at the BAT_{1P} pin. In this state, the batteries discharge down to the level determined by the V_{SEL} pin. The bq2902 monitors the cell voltage of the rechargeable alkaline cells.

If the voltage across any cell is below the voltage specified by the V_{SEL} input, the bq2902 disconnects the battery stack from the load by turning the internal discharge FET off. The discharge FET remains off until either the batteries are replaced or DC is reapplied, initiating a new charge cycle. After disconnecting the battery stack from the load, the standby current in the bq2902 is reduced to less than 1µA. The end-of-discharge voltage (V_{EDV}) is selectable by connecting the V_{SEL} pin as outlined in Table 2. Typically, higher discharge loads (>200mA) should use a lower discharge voltage cut-off to maximize battery capacity.

Table 2. bq2902 EDV Selections

End-of-Discharge Voltage	Pin Connection
1.10V	$V_{SEL} = BAT_{1P}$
1.00V	$V_{SEL} = Z$
0.90V	$V_{SEL} = V_{SS}$



Notes:
1. Charging: $0.4 < V_{OCV} \leq 1.63V$, $V_{CCV} \leq 3.0V$.
2. Pulses skipped when $V_{OCV} > 1.63V$.
3. Charge complete when average charge falls below 3% of fast charge rate

TD290201.eps

Figure 2. bq2902 Application Diagram

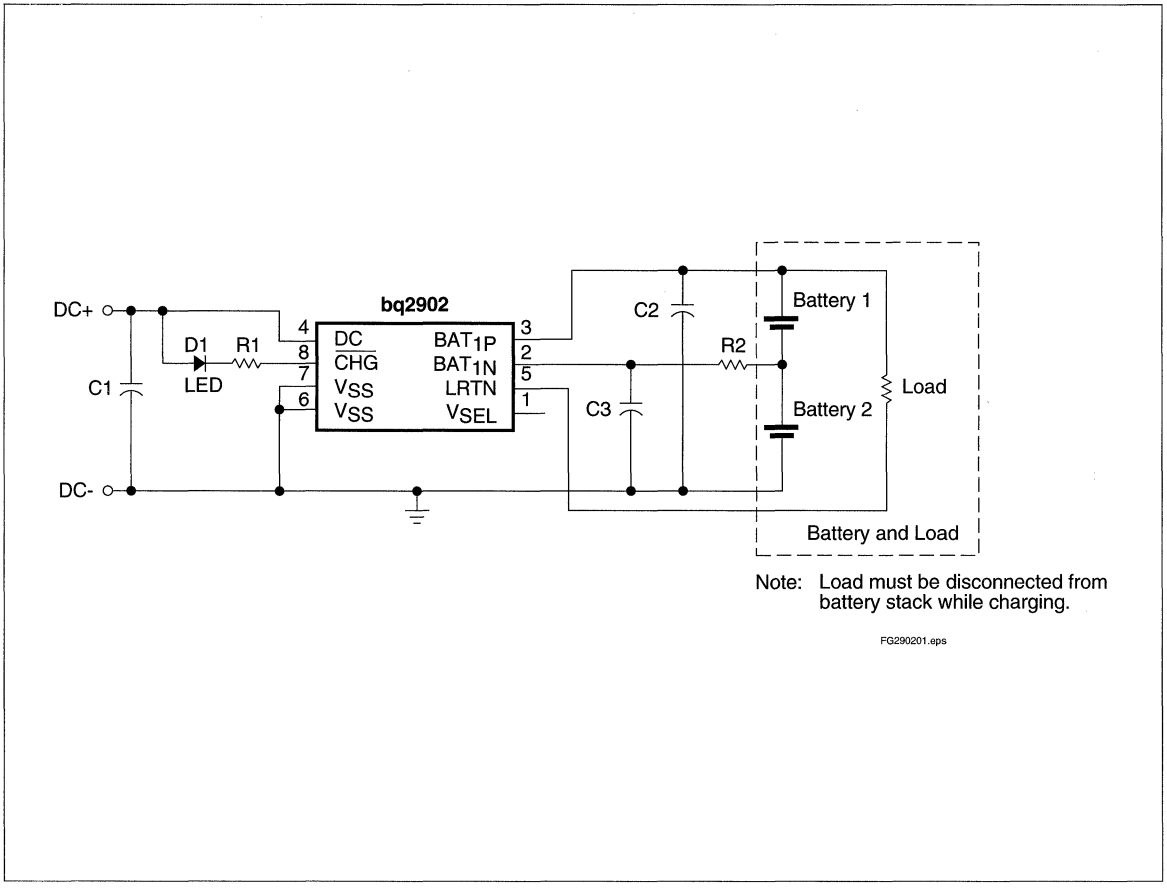


Figure 3. bq2902 Application Example, 1.0V EDV

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
DC_{IN}	V_{DC} relative to GND	-0.3	7.0	V	
V_T	DC threshold voltage applied on any pin, excluding the DC pin, relative to GND	-0.3	7.0	V	
T_{OPR}	Operating ambient temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial
T_{STG}	Storage temperature	-40	+85	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10 sec max.
I_{DC}	DC charging current	-	400	mA	
I_{LOAD}	Discharge current	-	500	mA	
I_{OL}	Output current	-	-	mA	$\overline{CHG}$

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds (T_A = 25°C; V_{DC} = 5.5V)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{MAX}	Maximum open-circuit voltage	1.63	±3%	V	$V_{OCV} > V_{MAX}$ inhibits/terminates charge pulses
V_{EDV}	End-of-discharge voltage	0.90	±5%	V	$V_{SEL} = BAT_{2N}$
		1.00	±5%	V	V_{SEL} = Z
		1.10	±5%	V	$V_{SEL} = BAT_{1P}$
V_{FLT}	Maximum open-circuit voltage	3.00	±5%	V	$V_{CCV} > V_{FLT}$ terminates charge, indicates fault
V_{MIN}	Minimum battery voltage	0.40	±5%	V	$V_{OCV} < V_{MIN}$ inhibits charge
V_{CE}	Charge enable	1.40	±5%	V	$V_{OCV} < V_{CE}$ on both cells re-initiates charge

Note: Each DC threshold parameter above has a temperature coefficient associated with it. To determine the coefficient for each parameter, use the following formula:

$$\text{Tempco} = \frac{\text{ParameterRating}}{1.63} * \text{-0.5mV/°C}$$

The tolerance for these temperature coefficients is 10%.

6/8

Timing (TA = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_P	Pulse period	-	12.5	-	ms	See Figure 2
t_{PW}	Pulse width	-	10	-	ms	See Figure 2

Note: Typical is at T_A = 25°C.

DC Electrical Characteristics (TA = TOPR)

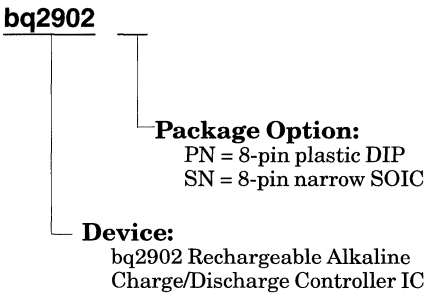
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{IH}	Logic input high	V_{BAT1P} - 0.1	-	V_{BAT1P}	V	V_{SEL}
V_{IL}	Logic input low	V_{SS}	-	V_{SS} + 0.1	V	V_{SEL}
V_{OL}	Logic output low	-	-	0.8	V	I_{OL} = 10mA
I_{OL}	Output current	10	-	-	mA	@V_{OL} = V_{SS} + 0.8V
I_{CC}	Supply current	-	-	250	µA	Outputs unloaded, V_{DC} = 5.5V
I_{SB1}	Standby current	-	-	25	µA	V_{DC} = 0V, V_{OCV} > V_{EDV}
I_{SB2}	End-of-discharge standby current	-	-	1	µA	VDC = 0V
I_L	Input leakage	-	-	±1	µA	V_{SEL}
I_{OZ}	Output leakage in high-Z state	-5	-	-	µA	$\overline{CHG}$
R_{DSON}	On resistance	-	0.5	-	Ω	Discharge FET; V_{BAT1P} = 1.8V
I_{IL}	Logic input low	-	-	70	µA	V_{SEL}
I_{IH}	Logic input high	-70	-	-	µA	V_{SEL}
I_{IZ}	Logic input float	-2	-	2	µA	V_{SEL}
I_{DC}	DC charging current	-	-	300	mA	
V_{DC}	DC charging voltage	3.3	-	5.5	V	DC
I_{LOAD}	Discharge current	-	-	400	mA	
V_{OP}	Operating voltage	1.8	-	5.5	V	BAT_{1P}

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	2	Figure 1. Functional Block Diagram	Updated block diagram

Notes: Change 1 = May 1999 C changes from Jan. 1997 B.

Ordering Information



8/8

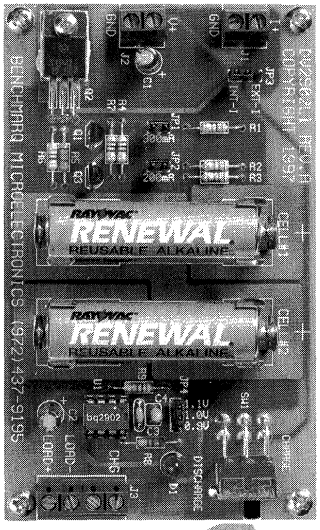
UNITRODE

Product Brief **DV2902**

Rechargeable Alkaline Development System

Features

- bq2902 evaluation and development system for two rechargeable alkaline cells.
- Battery holder for AA or AAA cells
- Charge status LED
- Direct connection for external voltage source or external current source
- Onboard current source for charging
- Terminates pulsed charge with maximum voltage limit
- Selectable end-of-discharge voltage
- Selectable charging rates: 100mA, 200mA, or 300mA



General Description

The DV2902 Development System provides a development environment for the bq2902 Charge/Discharge Controller IC used for managing two rechargeable alkaline cells. The user provides the charging source, the load, and two AA or AAA rechargeable alkaline cells.

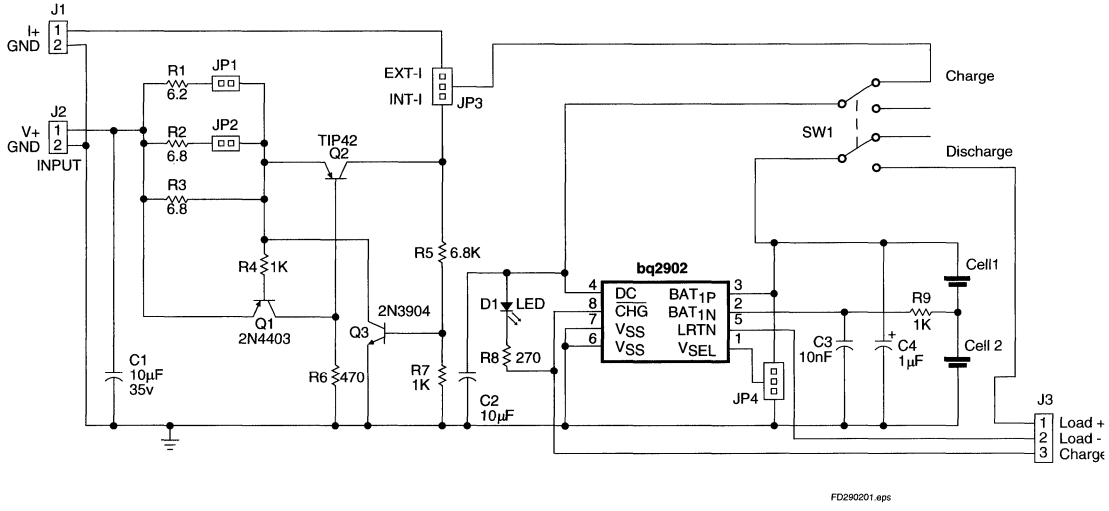
The user provides either a voltage source such as an AC/DC wall adapter and then use the on-board current source, or can provide an external voltage limited current source of their own design.

Fast charge is terminated by a maximum voltage limit. The status LED will remain on when charging has been terminated while the charging source is still supplied.

The DV2902 also provides for a selectable end-of-discharge voltage (EDV). This is configured using a jumper. When EDV is met, the bq2902 disconnects the battery stack from the load.

For a better understanding of the operation of the DV2902, please review the bq2902 data sheet. A full data sheet of this product is available on the Unitrode web site, or you may contact the factory for one.

DV2902 Board Schematic



UNITRODE

bq2903

Rechargeable Alkaline Charge/Discharge Controller IC

Features

- Safe charge of three or four rechargeable alkaline batteries such as Renewal® from Rayovac®
- Pulsed charge terminated with maximum voltage limit
- LED outputs indicate charge status
- Selectable end-of-discharge voltage prevents overdischarge and improves cycle life
- Optional external FET drive allows high current loads
- Pre-charge qualification indicates fault conditions
- Automatic charge control simplifies charger design
- Available in 14-pin 300-mil DIP or 150-mil SOIC

General Description

The bq2903 is a cost-effective charge controller for rechargeable alkaline batteries such as Renewal batteries from Rayovac. The bq2903 combines sensitive, full-charge detection for three to four rechargeable alkaline cells, with a low-battery cut-off for over-discharge protection.

Designed for integration into a three- or four-cell system, the bq2903 can improve the service life of the rechargeable alkaline cells by properly managing the charge and discharge. The bq2903 requires a voltage-limited current source to generate the proper charge pulses for the Renewal cell. Each cell is individually monitored to ensure full charge without a damaging overcharge.

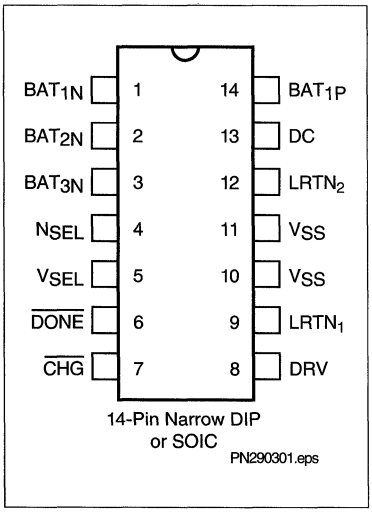
Charge completion is indicated when the average charge rate falls below approximately 6% of the fast charge rate. Status outputs are provided to indicate charge in progress, charge complete, or fault condition.

The bq2903 avoids over-depleting the battery by using the internal end-of-discharge control circuitry. The bq2903 also eliminates the external power switching transistors needed to separately charge individual Renewal cells.

To reduce external component count, the discharge and charge control FETs are internal to the bq2903; however, if the discharge load is greater than 400mA, a DRV pin is provided to drive an external N-FET, reducing the effective discharge path resistance for the system.

For safety, charging is inhibited if the voltage of any cell is greater than 3.0V during charge or if the voltage of any cell is less than 0.4V when not charging (open-circuit voltage).

Pin Connections



Pin Names

DC	Charging supply input	BAT_{1N}	Battery 1 negative input
$\overline{CHG}$	Battery status output 1	BAT_{2N}	Battery 2 negative input
$\overline{DONE}$	Battery status output 2	BAT_{3N}	Battery 3 negative input
N_{SEL}	Number of cells input	V_{SS}	Battery 4 negative input/ IC ground
V_{SEL}	End of discharge voltage select input	$LRTN_{1, 2}$	System load returns
BAT_{1P}	Battery 1 positive input	DRV	External FET drive output

Pin Descriptions

DC **DC supply input**

This input is used to recharge the rechargeable alkaline cells and power the bq2903 during charge. This input must be connected to a voltage-limited current source.

$\overline{CHG}$ **Charge status**

This open-drain output is used to signify the battery charging status and is valid only when DC is applied. See Figure 4 and Table 1.

$\overline{DONE}$ **Charge done**

This open-drain output is used to signify charge completion and is valid only when DC is applied.

N_{SEL} **Number of cells input**

This input selects whether the bq2903 charges 3 or 4 cells. N_{SEL} = BAT_{1P} selects 4 cells, and N_{SEL} = V_{SS} selects 3 cells.

V_{SEL} **End-of-discharge select input**

This three-level input selects the desired end-of-discharge cut-off voltage for the bq2903. V_{SEL} = BAT_{1P} selects an EDV of 1.10V. V_{SEL} floating selects EDV = 1.0V. V_{SEL} =V_{SS} selects EDV = 0.9V.

BAT_{1P} **Battery 1 positive input**

This input connects to the positive terminal of the battery designated BAT_1 (see Figure 3). This pin also provides power to the bq2903 when DC is not present.

BAT_{1N} **Battery 1 negative input**

This input connects to the negative terminal of the battery designated BAT_1 (see Figure 3).

BAT_{2N} **Battery 2 negative input**

This input connects to the negative terminal of the battery designated BAT_2 (see Figure 3).

BAT_{3N} **Battery 3 negative input**

This input connects to the negative terminal of the battery designated BAT_3 (see Figure 3).

V_{SS} **Battery 4 negative input/IC ground**

This input connects to the negative terminal of the battery designated BAT_4 (see Figure 3).

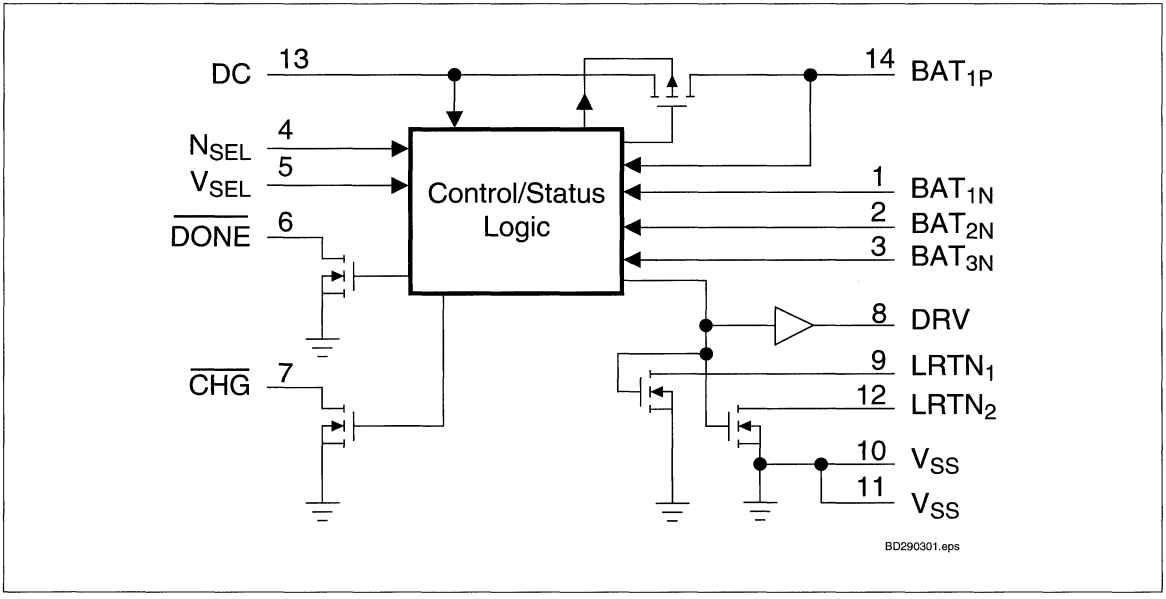


Figure 1. Functional Block Diagram

LRTN1, 2 Load returns

These open-drain pull-down outputs are typically used as low-side load switches. High-side load switching is also possible with the addition of an external P-FET

DRV External FET drive output

This push-pull output drives an optional external N-FET (see Figure 4). See page 5 for a full description.

Functional Description

Figure 1 is a block diagram outlining the major components of the bq2903. Figure 2 illustrates the charge control and display status during a bq2903 cycle. Table 1 outlines the various operational states and their associated conditions which are described in detail in the following section.

DC Input

This input is used to charge the rechargeable alkaline cells and power the bq2903 during a charge. To charge the batteries, this input should be connected to a current source limited to 300mA. If the DC input current is greater than 300mA, the power dissipation limits of the package will be exceeded. The DC input should also be capable of supplying a minimum of 2.0V*N, where N is the number of cells to be charged. The DC input should not exceed 10V.

Charge Pre-Qualification

After DC is applied, the bq2903 checks the open-circuit voltage (V_{OCV}) of each cell for an undervoltage condition (V_{OCV}<0.4V). If the V_{OCV} of any cell is below V_{MIN}, the bq2903 enters a charge-pending mode and indicates a fault (see Table 1).

If all cells are above V_{MIN} and the minimum operating voltage VOP(min)=2.7V at the DC pin is met, the bq2903 will initiate a charge cycle. A charge cycle consists of pulse charging the battery and then checking for a termination condition.

Charge Termination

Once a charge cycle begins, the bq2903 terminates charge when the average charge rate falls below 6% of the maximum charge rate. The bq2903 also terminates charge when the closed-circuit voltage (V_{CCV}) of any cell exceeds 3.0V (V_{FLT}) during charge and indicates a fault condition on the $\overline{CHG}$ output (see Table 1).

Charge Re-Initiation

If DC remains valid, the bq2903 will suspend all charge activity after full-charge termination. A charge cycle is reinitiated when all cell potentials fall below 1.4V. The rechargeable alkaline cells, unlike other rechargeable chemistries, do not require a maintenance charge to keep the cells in a fully charged state. The self-discharge rate for the Renewal cells is typically 4% per year at room temperature.

Charge Status Indication

Table 1 and Figure 2 outline the various charge action states and the associated BAT_{1P}, $\overline{CHG}$, and $\overline{DONE}$ output states. The charge status outputs are designed to work with individual or tri-color LED indicators. In all cases, if the voltage at the DC pin is less than the voltage at the BAT_{1P} pin, $\overline{CHG}$ and $\overline{DONE}$ outputs are held in a high-impedance condition.

Table 1. bq2903 Operational Summary

Charge Action State	Conditions	BAT_{1P} Input	$\overline{CHG}$ Output	$\overline{DONE}$ Output
DC absent	$V_{DC} < V_{BAT1P}$	-	Z	Z
Charge initiation	DC applied	-	-	-
Charge pending/ fault	$V_{OCV} < 0.4V$[1] or $V_{CCV} > 3.0V$[2]	-	⅙ sec = Low ⅙ sec = Z	Z
Charge pulse	$V_{OCV} \leq$ 1.63V before pulse	Charge pulsed @ 100Hz per Figure 1	Low	Z
Pulse skip	V_{OCV} > 1.63V before pulse	Pulse skipped per Figure 1	Low	Z
Charge complete	Average charge rate falls below 6% of the fast charge rate	Charge complete	Z	Low

Notes:
1. V_{OCV} = Open-circuit voltage of each cell between positive and negative leads.
2. V_{CCV} = Closed-circuit voltage.

Charging

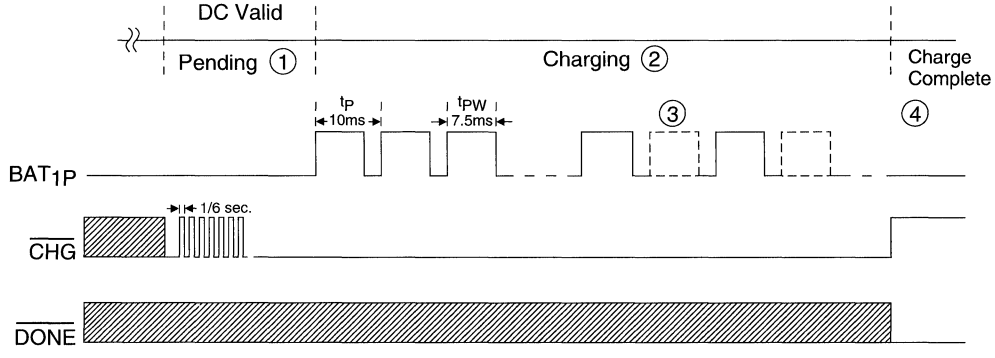
The bq2903 controls charging by periodically connecting the DC current source to the battery stack, not to the individual battery cells. The charge current is pulsed from the internal clock at approximately a 100 Hz rate on the BAT_{1P} pin.

The bq2903 pulse charges the battery for approximately 7.5ms of every 10ms, when conditions warrant. The bq2903 measures the open circuit voltage (V_{OCV}) of each battery cell during the idle period. If a single-cell potential of any battery is above the maximum open-circuit voltage (V_{MAX} = 1.63V ±3%), the following pulses are skipped until all cell potentials fall below the V_{MAX} limit. Charging is terminated when the average charge rate falls below approximately 6% of the maximum charge rate. Once charging is terminated, the internal charging FET remains off, and the $\overline{DONE}$ output becomes active per Table 1 and Figure 2. With DC applied, the internal discharge FET will always remain on, and the DRV output will remain high.

End-of-Discharge Control

When DC is less than the voltage on BAT_{1P}, the bq2903 is powered by the battery at BAT_{1P}. In this state, the batteries discharge down to the level determined by the V_{SEL} pin. The end-of-discharge voltage (V_{EDV}) is selectable by connecting the V_{SEL} pin as outlined in Table 2. If the voltage across any cell is below the voltage specified by the V_{SEL} input, the bq2903 disconnects the battery stack from the load by turning the internal discharge FET off. The DRV output is also driven low, disabling the external FET. After disconnecting power (the battery stack) to the load, the standby current in the bq2903 is reduced to less than 1µA. Typically, higher discharge loads (>200mA) should use a lower discharge voltage cut-off to maximize battery capacity.

After disconnecting the battery stack from the load, the internal discharge FET remains off, and the DRV output remains low until the batteries are replaced or DC is reapplied, initiating a new charge cycle.



Notes:
1. Charging Pending: 0.4 < V_{OCV} < 0.4V per cell, V_{CCV} > 3.0V per cell.
2. Charging: 0.4 < V_{OCV} ≤ 1.63V, V_{CCV} ≤ 3.0V.
3. Pulses skipped when V_{OCV} > 1.63V.
4. Charge complete when average charge rate falls below approximately 6% of the fast charge rate.

Figure 2. bq2903 Example of Charge Action Events

4/10

Table 2. bq2903 EDV Selections

End-of-Discharge Voltage	Pin Connection
1.10V	$V_{SEL} = BAT_{1P}$
1.00V	$V_{SEL} = Z$
0.90V	$V_{SEL} = V_{SS}$

Number-of-Cell Selection

N_{SEL} is used to select whether the bq2903 will charge 3 or 4 cells. Figure 3 shows the proper connection for a 3- or 4-cell system. For 4 cell operation, $N_{SEL} = BAT_{1P}$. For 3 cell operation, $N_{SEL} = V_{SS}$ and the BAT_{2N} pin should be connected to the BAT_{3N} pin.

DRV Pin

The bq2903 controls battery discharge with two internal FETs between LRTN1, LRTN2, and V_{SS}. The current through each switch should be limited to 200mA. LRTN1 can be tied to LRTN2 for discharge current of up to 400mA. To reduce the effective discharge switch resistance, or for high current loads, the DRV pin can control an external N-FET, as shown in Figure 4. DRV is "high" when a valid charging voltage is applied to the DC pin and remains "high" during discharge. DRV goes "low" during discharge to turn off the external FET when an end-of-discharge condition is met. This pin should not be connected if the external FET option is not used.

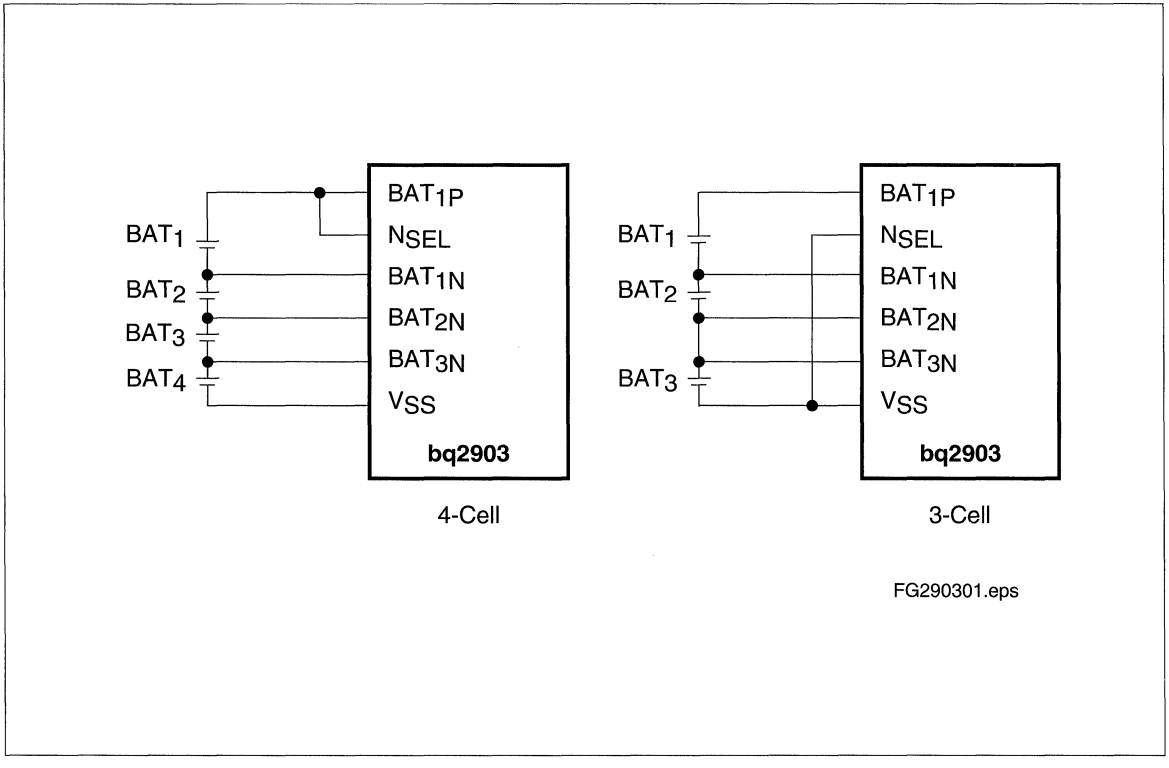


Figure 3. N_{SEL} Connection Diagram

5/10

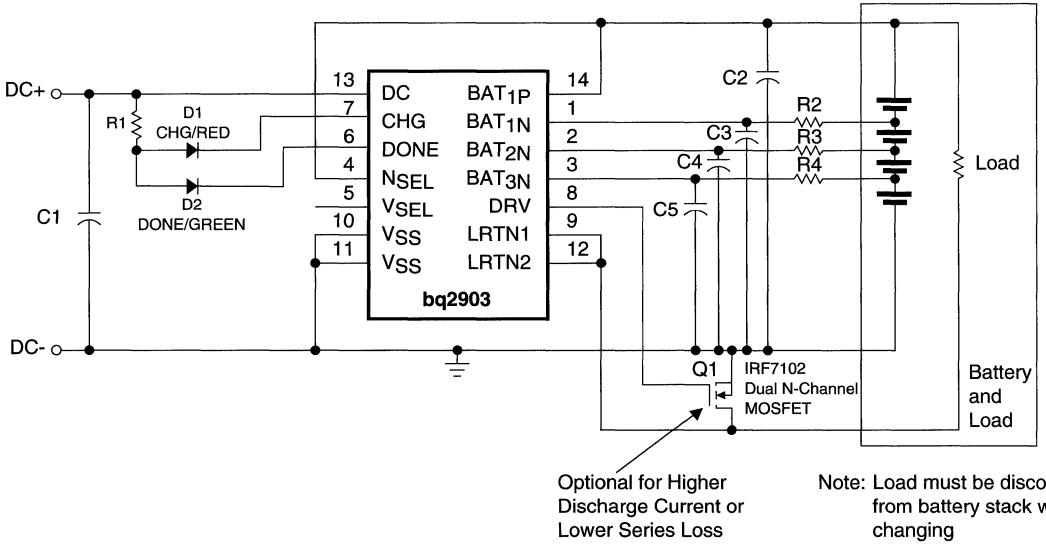


Figure 4. bq2903 Application Example, 4–Cell and 1.0V EDV

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
DC_{IN}	V_{DC}	-0.3	11.0	V	
V_T	DC threshold voltage applied on any pin, excluding DC pin	-0.3	11.0	V	
T_{OPR}	Operating ambient temperature	0	+70	°C	Commercial
T_{STG}	Storage temperature	-40	+85	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10 sec max.
I_{DC}	DC charging current	-	400	mA	
I_{LOAD}	Discharge current	-	500	mA	No external FET
I_{OL}	Output current	-	20	mA	$\overline{CHG}$, $\overline{DONE}$

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds (T_A = 25°C; V_{DC} =10V)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{MAX}	Maximum open-circuit voltage	1.63	±3%	V	$V_{OCV} > V_{MAX}$ inhibits or terminates charge pulses
V_{EDV}	End-of-discharge voltage	0.90	±5%	V	$V_{SEL} = V_{SS}$
		1.00	±5%	V	V_{SEL} = Z
		1.10	±5%	V	$V_{SEL} = BAT_{1P}$
V_{FLT}	Maximum closed-circuit voltage	3.00	±5%	V	$V_{CCV} > V_{FLT}$ terminates charge, indicates fault
V_{MIN}	Minimum battery voltage	0.40	±5%	V	$V_{OCV} < V_{MIN}$ inhibits charge
V_{CE}	Charge enable	1.40	±5%	V	$V_{OCV} < V_{CE}$ on all cells re-initiates charge

Note: Each parameter above has a temperature coefficient associated with it. To determine the coefficient for each parameter, use the following formula:

$$\text{Tempco} = \frac{\text{ParameterRating}}{1.63} * \text{-0.5mV/°C}$$

The tolerance for these temperature coefficients is 10%.

Timing (T_A = 25°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_P	Pulse period	-	10	-	ms	See Figure 2
t_{PW}	Pulse width	-	7.5	-	ms	See Figure 2

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{IH}	Logic input high	V_{BAT1P} - 0.1	-	V_{BAT1P}	V	V_{SEL}, N_{SEL}
V_{IL}	Logic input low	V_{SS}	-	V_{SS} + 0.1	V	V_{SEL}, N_{SEL}
V_{OL}	Logic output low	-	-	1.0	V	$\overline{DONE}$, $\overline{CHG}$, I_{OL} = 5mA
		-	-	0.4	V	I_{OL} = 1.0mA, DRV
V_{OH}	Gate drive output	(Greater of V_{BAT1P} or V_{DC}) - 1.0	-	-	V	DRV, I_{OH} = -1.0mA
I_{OL}	Output current	5	-	-	mA	$V_{OL} = V_{SS}$ + 1.0V, $\overline{CHG}$, $\overline{DONE}$
		1	-	-	mA	DRV = V_{SS} + 1.0V
I_{DC}	Supply current	-	35	250	µA	Outputs unloaded, V_{DC} = 10.0V
I_{SB1}	Standby current	-	25	40	µA	V_{DC} = 0, $V_{OCV} > V_{EDV}$, BAT_{1P-3N}
I_{SB2}	End-of-discharge standby current	-	-	1	µA	V_{DRV} = 0V, V_{DC} = 0
I_L	Input leakage	-	-	±1	µA	NSEL
I_{OZ}	Output leakage in high-Z state	-	-	±5	µA	$\overline{CHG}$, $\overline{DONE}$
R_{DSON}	Discharge on resistance	-	0.5	-	Ω	Discharge FETs; V_{BAT1P} = 2.7V, LRTN1 (pin 9) must be tied to LRTN2 (pin 12)
I_{LOAD}	Discharge current without external N-FET	-	-	400	mA	No external FET; LRTN1 (pin 9) must be tied to LRTN2 (pin 12).
I_{IL}	Logic input low	-	-	70	µA	V= GND to GND + 0.5V, V_{SEL}
I_{IH}	Logic input high	-70	-	-	µA	V = V_{DC} -0.5 to V_{DC}, V_{SEL}
I_{IZ}	Logic input float	-2	-	2	µA	V_{SEL}
I_{DC}	DC charging current	-	-	300	mA	
V_{OP}	Operating voltage	2.7	-	10	V	

Note: All voltages relative to V_{SS}.

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	1	Pin connections	LRTN1 (pin 9) was LRTN, LRTN2 (pin 12) was LRTN
1	2	Functional block diagram	Updated block diagram
1	3	Pin description	Added descriptions for LRTN1 and LRTN2
1	5	DRV pin	Clarified LRTN1 and LRTN2 description
1	6	Application example	Corrected schematic
1	9	R_{DSON} and I_{LOAD} specification	Added notes on LRTN1 and LRTN2
2	7	T_{OPR}	Deleted industrial temperature range

Notes: Change 1 = May 1999 B changes from July 1996.
Change 2 = June 1999 C changes from May 1999 B

Ordering Information

bq2903

Package Option:
PN = 14-pin narrow plastic DIP
SN = 14-pin narrow SOIC

Device:
bq2903 Rechargeable Alkaline Charge/Discharge Controller IC

10/10

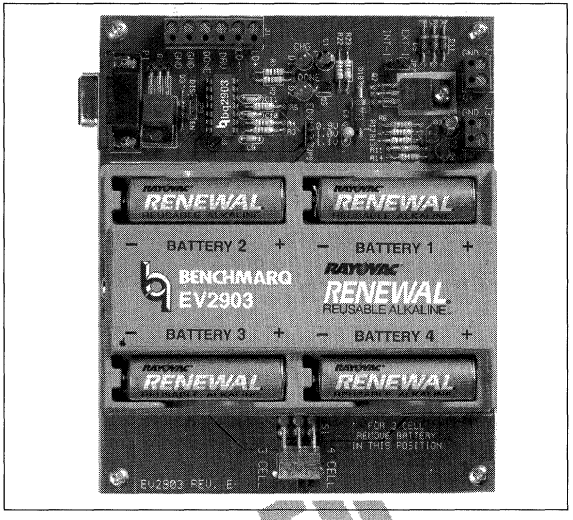
UNITRODE

Product Brief EV2903

bq2903 Evaluation System

Features

- bq2903 fast charge control evaluation and development system for rechargeable alkaline batteries such as Renewal® from Rayovac®
- Optional on-board 300mA current-limited charge supply
- Fast charge of three or four alkaline cells
- Pulsed charge terminated by minimum current and backed up by a maximum voltage safety termination
- Selectable end-of-discharge voltage
- Charge status indicator LEDs
- Datalog capability for charge and discharge currents through the serial port of a PC



General Description

The EV2903 Evaluation System provides a development and evaluation environment for the bq2903 Rechargeable Alkaline Charge/Discharge Controller IC. The EV2903 incorporates a bq2903, a bq2014 Gas Gauge IC, an onboard discharge N-FET, and all other hardware needed to charge three or four rechargeable alkaline batteries, such as Renewal from Rayovac.

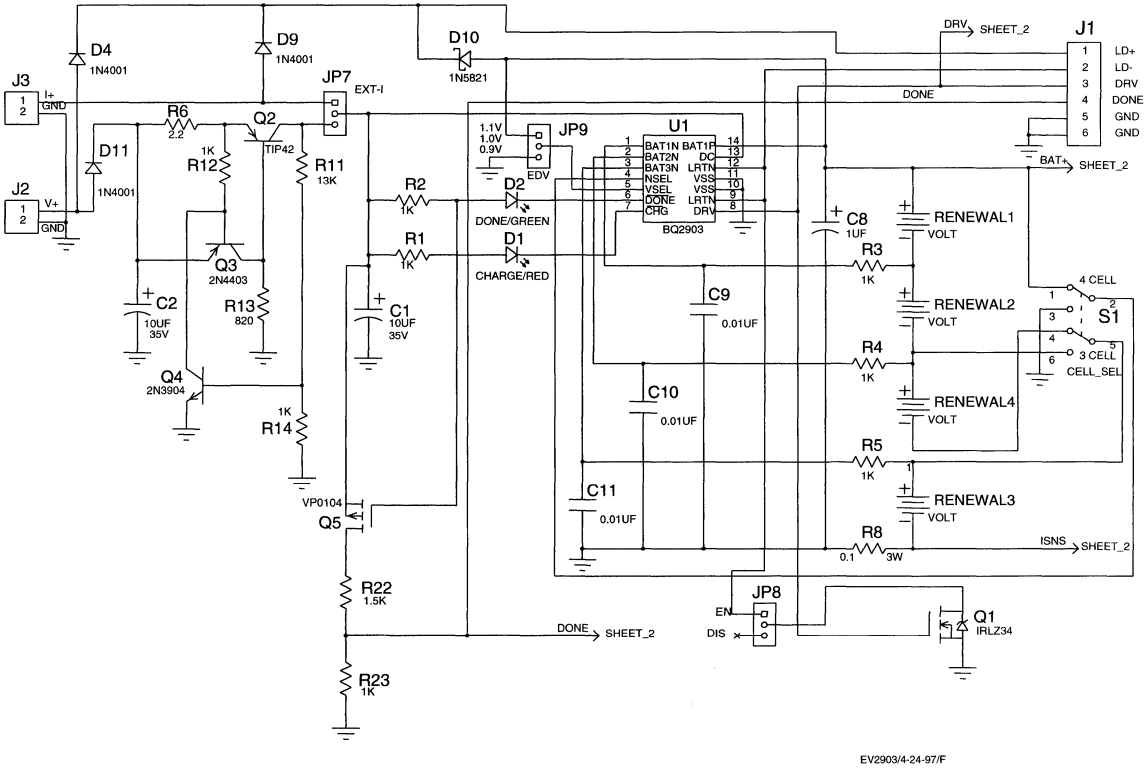
Fast charge is terminated when the average charge rate falls below approximately 3% of the fast charge rate. For safety, charging is inhibited if the voltage of any cell is greater than 3.0V during charge or if the voltage of any cell is less than 0.4V when not charging (open-circuit voltage).

The user provides batteries and DC power supply. The user configures the EV2903 for the number of cells (three or four), end-of-discharge voltage, and on-board or off-board current regulation.

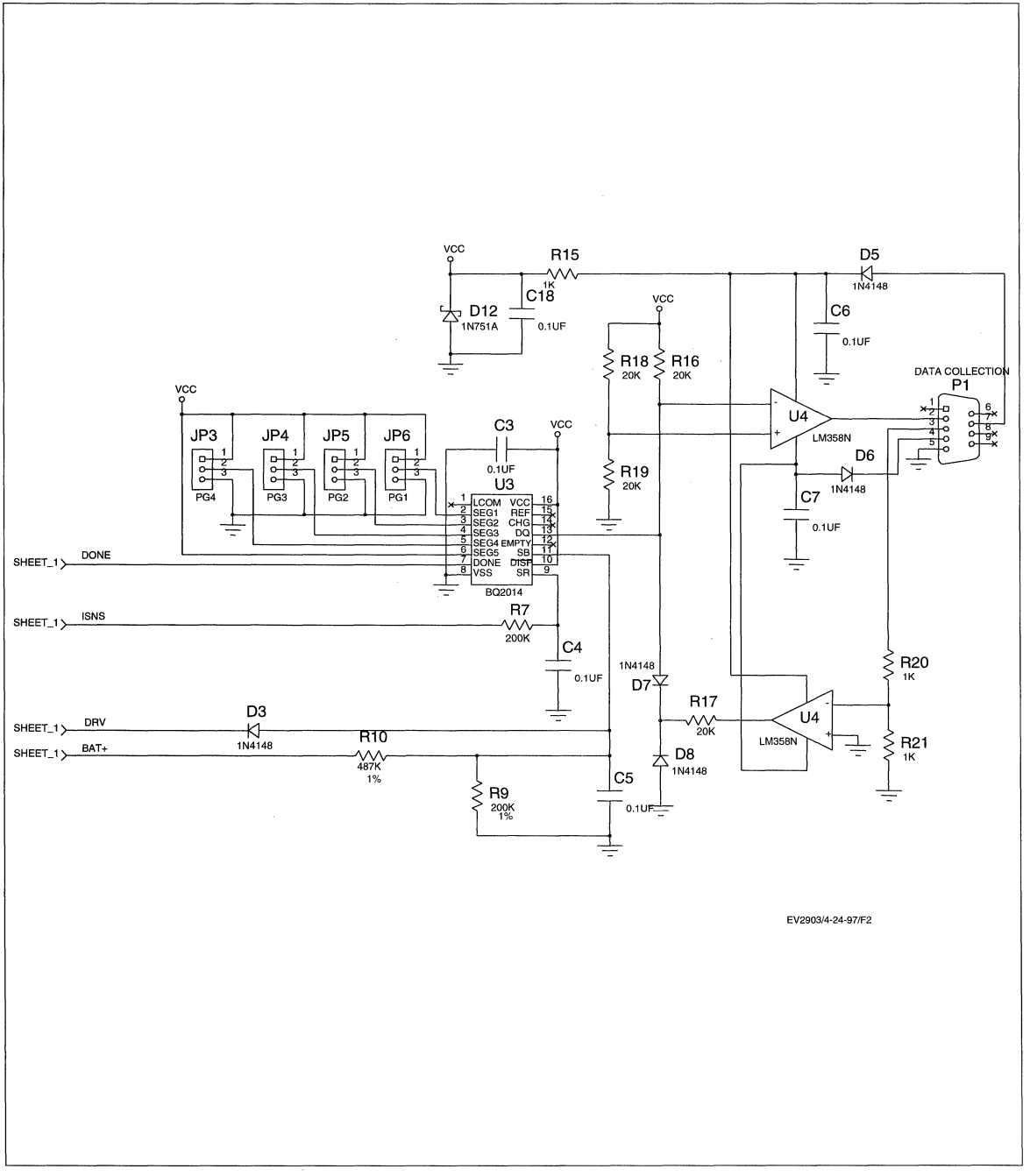
A full data sheet of this product is available on the Unitrode web site, or you may contact the factory for one.

10/97

EV2903 Schematic



EV2903 Schematic (Continued)



Lithium Ion Charge Management IC with Integrated Switching Controller

Features

- ➤ Safe charge of Li-Ion battery packs
- ➤ Pulse-width modulation control for current and voltage regulation
- ➤ Programmable high-side/low-side current-sense
- ➤ Fast charge terminated by selectable minimum current; safety backup termination at maximum time
- ➤ Pre-charge qualification detects shorted or damaged cells and conditions battery
- ➤ Charging continuously qualified by temperature and voltage limits
- ➤ Direct LED control outputs to display charge status and fault conditions

General Description

The bq2954 Li-Ion Charge-Management IC uses a flexible pulse-width modulation regulator to control voltage and current during charging. The regulator frequency is set by an external capacitor for design flexibility. The switch-mode design minimizes power dissipation.

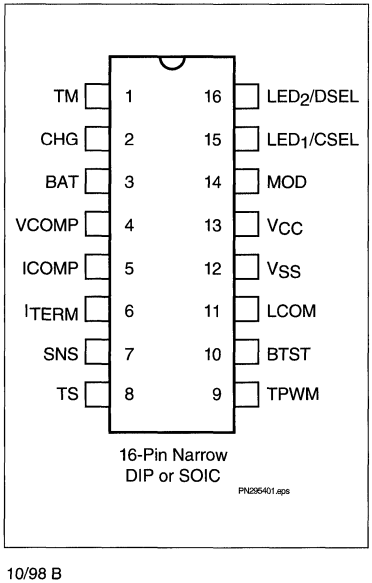
For safety, the bq2954 inhibits fast charging until the battery voltage and temperature are within configured limits. If the battery voltage is less than the low-voltage threshold, the bq2954 provides low-current conditioning of the battery.

For charge qualifiction, the bq2954 uses an external thermistor to measure battery temperature. Charging begins when power is applied or the battery is inserted

The bq2954 charges a battery in two phases. First a constant-current phase replenishes approximately 70% of battery capacity. Then a voltage-regulation phase completes the battery charge.

The bq2954 provides status indications of all charger states and faults for accurate determination of the battery and charge-system conditions.

Pin Connections



Pin Names

TM	Time-out programming input
CHG	Charge active output
BAT	Battery voltage input
VCOMP	Voltage loop comp input
ICOMP	Current loop comp input
ITERM	Minimum current termination select input
SNS	Sense resistor input
TS	Temperature sense input
TPWM	Regulator timebase input
BTST	Battery test output
LCOM	Common LED output
VSS	System ground
VCC	5.0V±10% power
MOD	Modulation control output
LED1/ CSEL	Charge status output 1/ Charge sense select input
LED2/ DSEL	Charge status output 2/ Display select input

Pin Descriptions

TM **Time-out programming input**

Sets the maximum charge time. The resistor and capacitor values are determined using Equation 5. Figure 10 shows the resistor/capacitor connection.

CHG **Charge active output**

An open-drain output is driven low when the battery is removed, during a temperature pend, when a fault condition is present, or when charge is done. CHG can be used to disable a high-value load capacitor to detect quickly any battery removal.

BAT **Battery voltage input**

Sense input. This potential is generally developed using a high-impedance resistor divider network connected between the positive and the negative terminals of the battery. See Figures 6 and 7 and Equation 1.

VCOMP **Voltage loop compensation input**

Connects to an external R-C network to stabilize the regulated voltage.

ICOMP **Current loop compensation input**

Connects to an external R-C network to stabilize the regulated current.

I_{TERM} **Charge full and minimum current termination select**

Three-state input is used to set I_{FULL} and I_{MIN} for fast charge termination. See Table 4.

SNS **Charging current sense input**

Battery current is sensed via the voltage developed on this pin by an external sense-resistor.

TS **Temperature sense input**

Used to monitor battery temperature. An external resistor-divider network sets the lower and upper temperature thresholds. (See Figures 8 and 9 and Equations 3 and 4.)

TPWM **Regulation timebase input**

Uses an external timing capacitor to ground to set the pulse-width modulation (PWM) frequency. See Equation 7.

BTST **Battery test output**

Driven high in the absence of a battery in order to provide a potential at the battery terminal when no battery is present.

LCOM **Common LED output**

Common output for LED_{1-2}. This output is in a high-impedance state during initialization to read programming input on DSEL and CSEL.

V_{SS} **Ground**

V_{CC} **V_{CC} supply**

5.0V, ±10%

MOD **Current-switching control output**

Pulse-width modulated push/pull output used to control the charging current to the battery. MOD switches high to enable current flow and low to inhibit current flow. (The maximum duty cycle is 80%.)

LED_1–LED_2 **Charger display status 1–2 outputs**

Drivers for the direct drive of the LED display. These outputs are tri-stated during initialization so that DSEL and CSEL can be read.

DSEL **Display select input (shared pin with LED_2)**

Three-level input that controls the LED_{1-2} charge display modes.

CSEL **Charge sense-select input (shared pin with LED_1)**

Input that controls whether current is sensed on low side of battery or high side of battery. A current mirror is required for high-side sense.

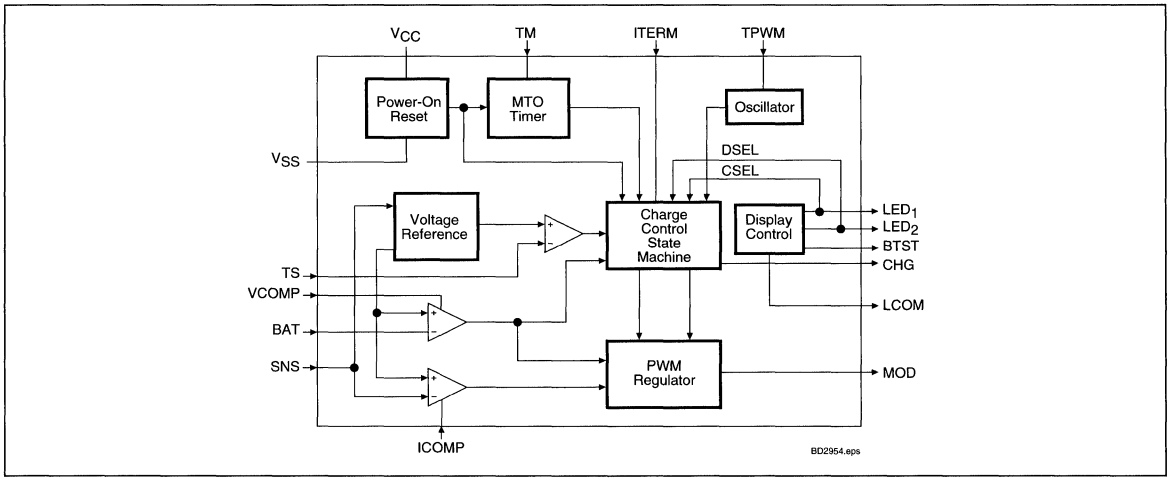


Figure 1. Functional Block Diagram

Functional Description

The bq2954 functional operation is described in terms of the following (Figure 1):

- Charge algorithm
- Charge qualification
- Charge status display
- Configuring the display and termination
- Voltage and current monitoring
- Battery insertion and removal
- Temperature monitoring
- Maximum time--out
- Charge regulation
- Recharge after fast charge

Charge Algorithm

The bq2954 uses a two-phase fast-charge algorithm. In phase 1, the bq2954 regulates constant current until the voltage on the BAT pin, V_{BAT}, rises to the internal threshold, V_{REG}. The bq2954 then transitions to phase 2 and regulates constant voltage ($V_{BAT} = V_{REG}$) until the charging current falls below the programmed I_{MIN} threshold. Fast charge then terminates, and the bq2954 enters the Charge Complete state. (See Figure 2.)

Charge Qualification

The bq2954 starts a charge cycle when power is applied while a battery is present or when a battery is inserted. Figure 2 shows the state diagram for the bq2954. The bq2954 first checks that the battery temperature is within the allowed, user-configurable range. If the temperature is out of range, the bq2954 remains in the QUALIFICATION state (S01) and waits until the battery temperature and voltage are within the allowed range.

If during any state of charge, a temperature excursion occurs HOT, the bq2954 proceeds to the DONE state (S04) and indicates this state on the LED outputs and provides no current. If this occurs, the bq2954 remains in the DONE state unless the following two conditions are met:

- Temperature falls within valid charge range
- V_{BAT} falls below the internal threshold, V_{RCHG}

If these two conditions are met, a new charge cycle begins. During any state of charge, if a temperature excursion occurs COLD, the bq2954 terminates charge and returns to the QUALIFICATION state (S01). Charge restarts if V_{BAT} and temperature are in valid range.

When the temperature and voltage are valid, the bq2954 enters the CONDITIONING state (S02) and regulates current to I_{COND} (=I_{MAX}/10). After an initial holdoff period t_{HO} (which prevents the IC from reacting to transient voltage spikes that may occur when charge current is first applied), the IC begins monitoring V_{BAT}. If V_{BAT} does not rise to at least V_{MIN} before the expiration of

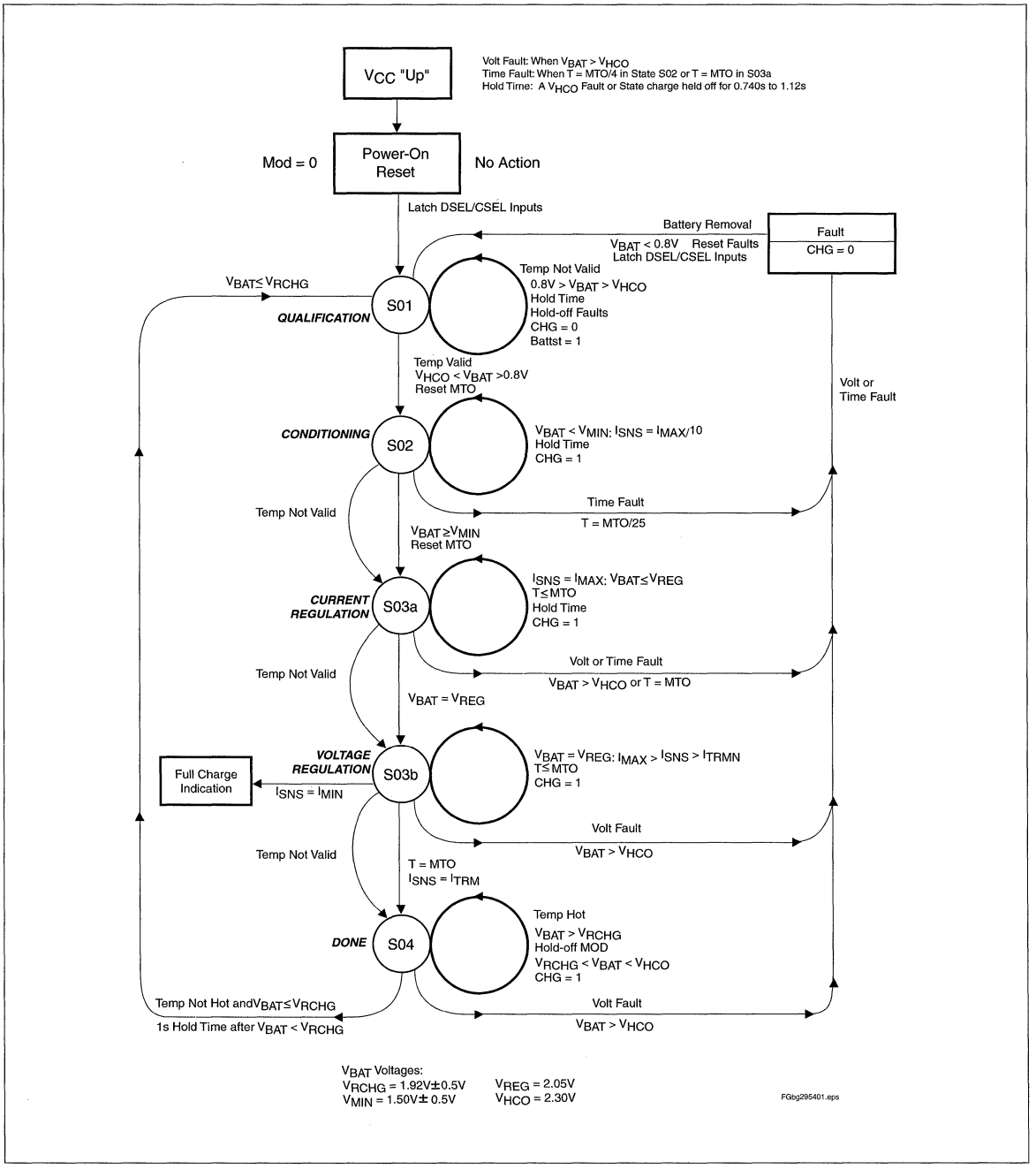
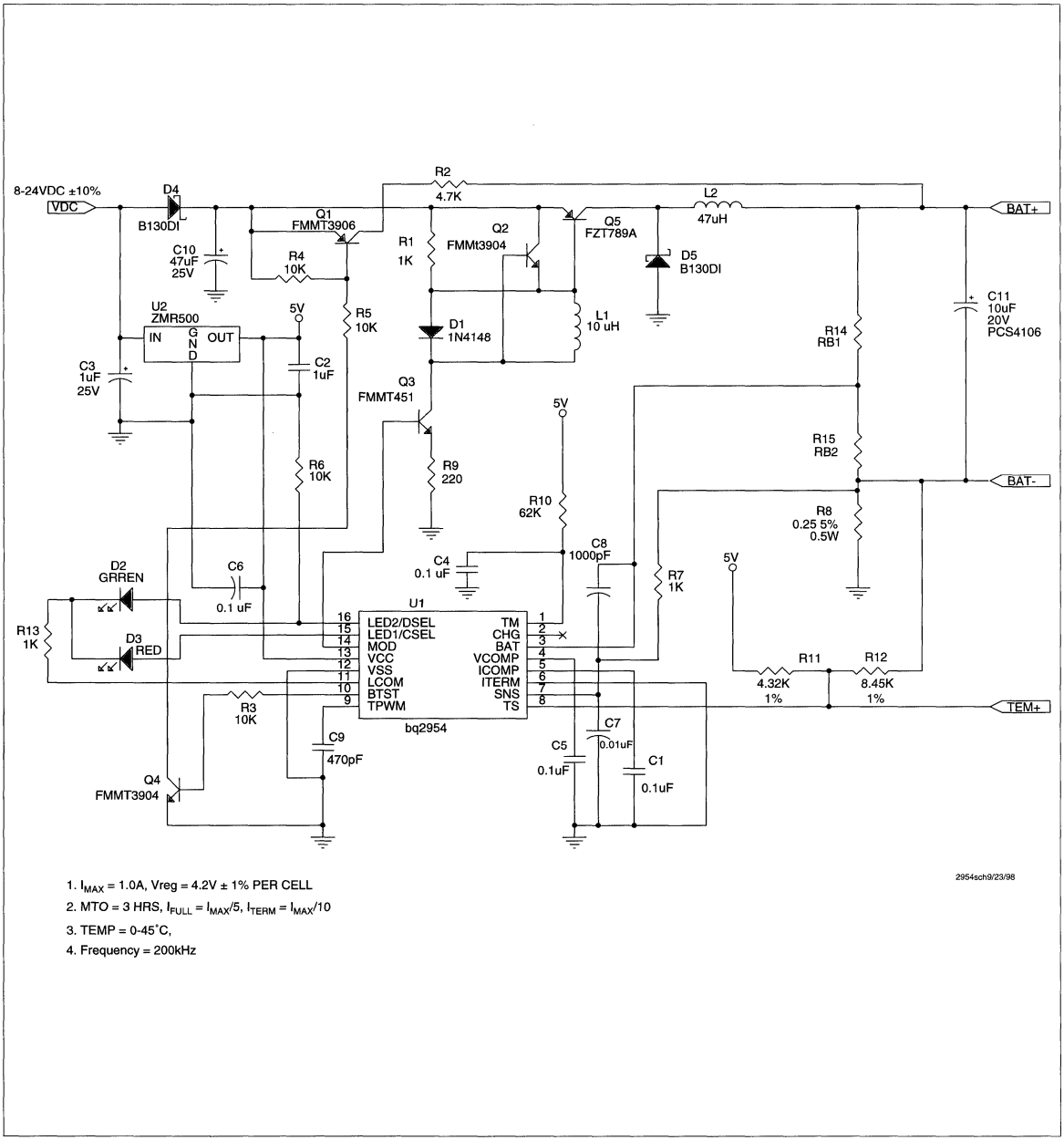


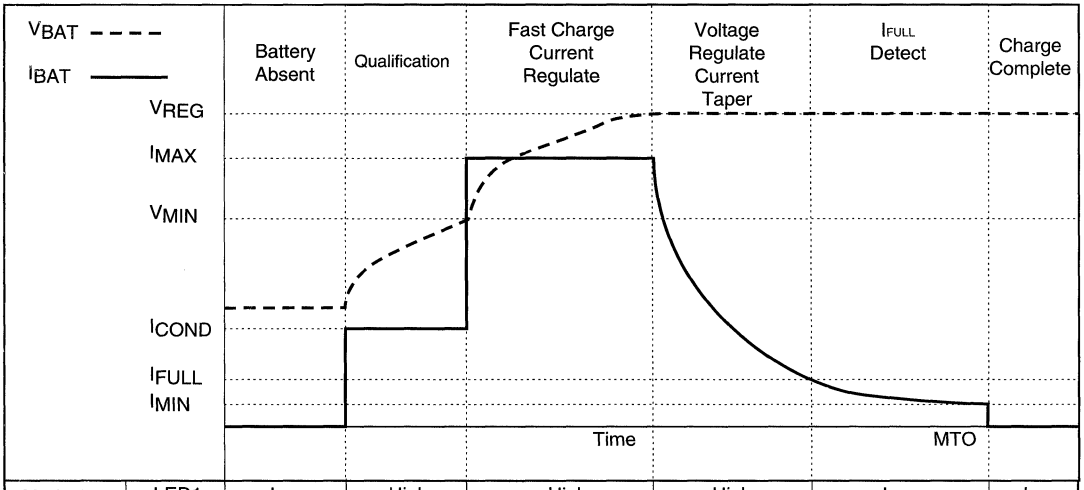
Figure 2. bq2954 Charge Algorithm



1. I_{MAX} = 1.0A, Vreg = 4.2V ± 1% PER CELL
2. MTO = 3 HRS, $I_{FULL} = I_{MAX}/5$, $I_{TERM} = I_{MAX}/10$
3. TEMP = 0-45°C,
4. Frequency = 200kHz

Figure 3. High-Efficiency Li-Ion Charger for 1–4 Cells

Table 1. Normal Fast Charge Cycle



Mode 1 (DSEL = 0)	LED1	Low	High	High	High	Low	Low
	LED2	Low	Low	Low	Low	High	High
Mode 2 (DSEL = 1)	LED1	Low	High	High	High	Low	Low
	LED2	Low	Low	Low	Low	High	High
Mode 3 (DSEL = F)	LED1	Low	High	High	High	Low	Low
	LED2	Low	Low	Low	High	High	High
Mode 1 and 2	CHG	Low	High	High	High	High	Low
	BTST	High	Low	Low	Low	Low	Low
Mode 3	CHG	Low	High	High	High	High	Low
	BTST	High	High	Low	Low	Low	Low

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time-out limit t_{QT} (i.e., the battery has failed short), the bq2954 enters the Fault state. Then t_{QT} is set to 25% of t_{MTO}. If V_{MIN} is achieved before expiration of the time limit, the bq2954 begins fast charging.

Once in the Fault state, the bq2954 waits until V_{CC} is cycled or a new battery insertion is detected. It then starts a new charge cycle and begins the qualification process again.

Charge Status Display

Charge status is indicated by the LED driver outputs LED_1–LED_2. Three display modes (Tables 1– 3) are available in the bq2954 and are selected by configuring pin DSEL. Table 1 illustrates a normal fast charge cycle, Table 2 a recharge-after-fast-charge cycle, and Table 3 an abnormal condition.

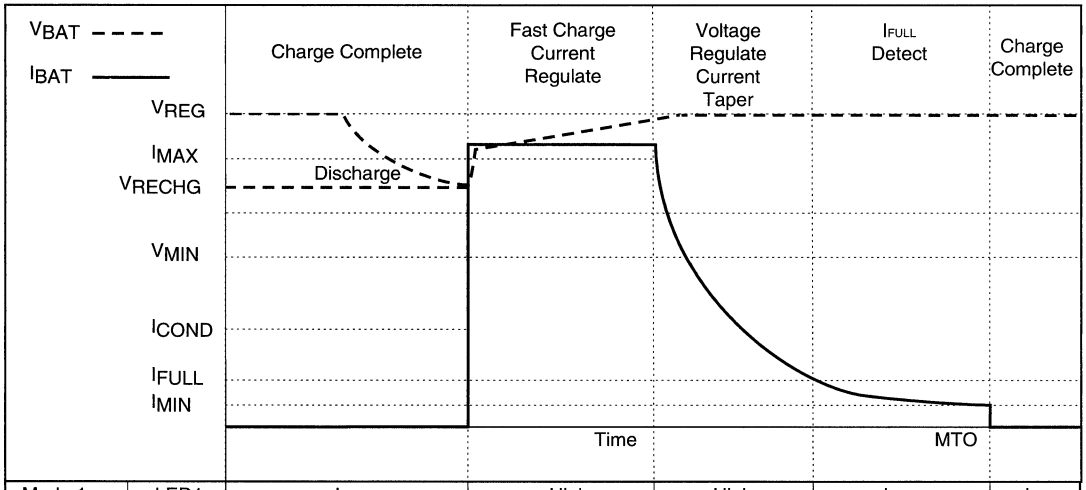
Configuring the Display Mode, I_{FULL}/I_{MIN}, and I_{SENSE}

$DSEL/LED_2$ and $CSEL/LED_1$ are bi-directional pins with two functions: as LED driver pins (output) and as programming pins (input). The selection of pull-up, pull-down, or no-resistor programs the display mode on DSEL as shown in Tables 1 through 3. A pull-down or no-resistor programs the current-sense mode on CSEL.

The bq2954 latches the programming data sensed on the DSEL and CSEL input when V_{CC} rises to a valid level. The LEDs go blank for approximately 400ms (typical) while new programming data are latched.

When fast charge reaches a condition where the charging current drops below I_{FULL}, the LED1 and LED2 outputs indicate a full-battery condition. Fast charge terminates when the charging current drops below the

Table 2. Recharge After Fast Charge Cycle



Mode 1 (DSEL = 0)	LED1	Low	High	High	Low	Low
	LED2	High	Low	Low	High	High
Mode 2 (DSEL = 1)	LED1	Low	High	High	Low	Low
	LED2	High	Low	Low	High	High
Mode 3 (DSEL = F)	LED1	Low	High	High	Low	Low
	LED2	High	Low	High	High	High
Mode 1 and 2	CHG	Low	High	High	High	Low
	BTST	Low	Low	Low	Low	Low
Mode 3	CHG	Low	High	High	High	Low
	BTST	Low	Low	Low	Low	Low

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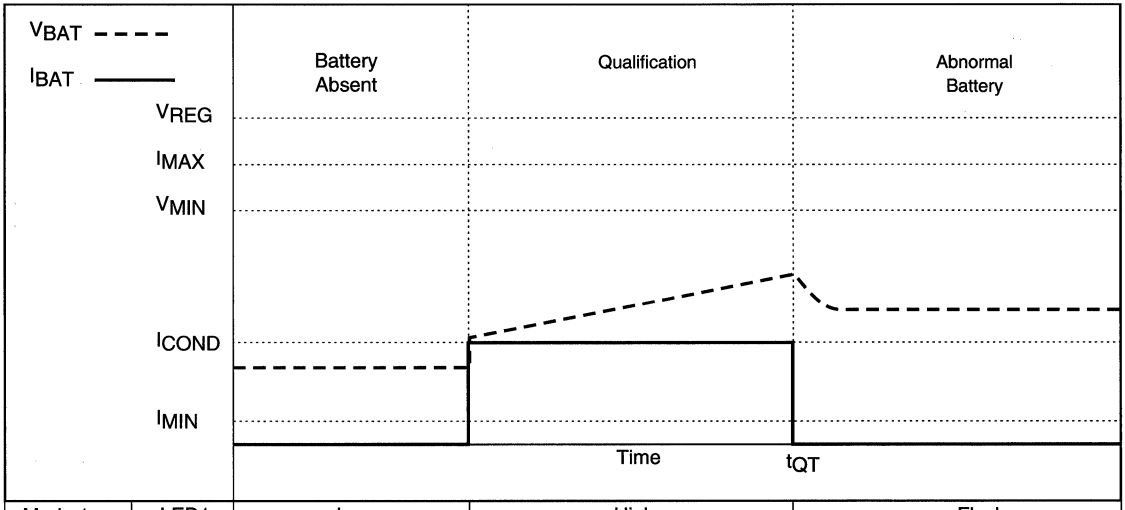
7/16

Table 3. Abnormal Condition



Mode 1 (DSEL = 0)	LED1	Low	High	Flash
	LED2	Low	Low	Low
Mode 2 (DSEL = 1)	LED1	Low	High	Low
	LED2	Low	Low	Low
Mode 3 (DSEL = F)	LED1	Low	High	Low
	LED2	Low	Low	Low
CHG		Low	High	Low
BTST		High	Low	Low

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Table 4. I_{FULL} and I_{MIN} Thresholds

I_{TERM}	I_{FULL}	I_{MIN}
0	$I_{MAX}/5$	$I_{MAX}/10$
1	$I_{MAX}/10$	$I_{MAX}/15$
Z	$I_{MAX}/15$	$I_{MAX}/20$

minimum current threshold, I_{MIN}. The I_{FULL} and I_{MIN} thresholds are programmed using the I_{TERM} input pin (See Table 4.)

Figures 4 and 5 show the bq2954 configured for display mode 2 and $I_{FULL} = I_{MAX}/5$ while $I_{MIN} = I_{MAX}/10$.

Voltage and Current Monitoring

In low-side current sensing, the bq2954 monitors the battery pack voltage as a differential voltage between BAT and pins. In high-side current sensing, the bq2954 monitors the battery pack voltage as a differential voltage between BAT and V_{SS} pins. This voltage is derived by scaling the battery voltage with a voltage divider. (See Figures 6 and 7.) The resistance of the voltage divider must be high enough to minimize battery drain but low enough to minimize noise susceptibility. RB1 + RB2 is typically between 150kΩ and 1MΩ. The voltage-divider resistors are calculated from the following:

$$\frac{RB1}{RB2} = \frac{N * V_{CELL}}{V_{REG}} - 1 \quad (1)$$

where

V_{CELL} = Manufacturer-specified charging cell voltage
N = Number of cells in series
V_{REG} = 2.05V

The current sense resistor, R_{SNS} (see Figures 6 and 7), determines the fast-charge current. The value of R_{SNS} is given by the following:

$$R_{SNS} = \frac{0.25V}{I_{MAX}} \quad (2)$$

where I_{MAX} is the current during the constant-current phase of the charge cycle. (See Table 1.)

Battery Insertion and Removal

V_{BAT} is interpreted by the bq2954 to detect the presence or absence of a battery. The bq2954 determines that a battery is present when V_{BAT} is between the High-Voltage Cutoff ($V_{HCO} = V_{REG} + 0.25V$) and the Low-Voltage Cutoff ($V_{LCO} = 0.8V$). When V_{BAT} is outside this range, the bq2954 determines that no battery is present and transitions to the battery test state, testing for valid battery voltage. The bq2954 detects battery removal when V_{BAT} falls below V_{LCO}. The BTST pin is driven high during battery test and can activate an external battery contact pull-up. This pull-up may be used to activate an over-discharged Li-Ion battery pack. The V_{HCO} limit implicitly serves as an over-voltage charge fault. The CHG output can be used to disconnect capacitors from the regulation circuitry in order to quickly detect a battery-removed condition.

Battery insertion is detected within 500ms. Transition to the fast-charge phase, however, will not occur for time t_{HO} (approximately one second), even if voltage qualification V_{MIN} is reached. This delay prevents a voltage spike at the BAT input from causing premature entry into the fast-charge phase. It also creates a delay in detection of battery removal if the battery is removed during this hold-off period.

Temperature Monitoring

Temperature is measured as a *differential* voltage between TS and BAT-. This voltage is typically generated by a NTC (negative temperature coefficient) thermistor and thermistor linearization network. The bq2954 compares this voltage to its internal threshold voltages to determine if charging is allowed. These thresholds are the following:

- High-Temperature Cutoff Voltage: $V_{TCO} = 0.4 * V_{CC}$ This voltage corresponds to the maximum temperature (TCO) at which charging is allowed.
- High-Temperature Fault Voltage: $V_{HTF} = 0.44 * V_{CC}$ This voltage corresponds to the temperature (HTF) at which charging resumes after exceeding TCO.
- Low-Temperature Fault Voltage: $V_{LTF} = 0.6 * V_{CC}$ This voltage corresponds to the minimum temperature (LTF) at which charging is allowed.

Charging is inhibited if the temperature is outside the LTF—TCO window. Once the temperature exceeds TCO, it must drop below HTF before charging resumes.

RT1 and RT2 for the thermistor linearization network are determined as follows:

$$0.6 * V_{CC} = \frac{V}{1 + \frac{RT1 * (RT2 + R_{LTF})}{(RT2 * R_{LTF})}} \quad (3)$$

$$0.44 = \frac{1}{1 + \frac{RT1 * (RT2 + R_{HTF})}{(RT2 * R_{HTF})}} \quad (4)$$

where

R_{LTF} = thermistor resistance at LTF

R_{HTF} = thermistor resistance at HTF

$V = V_{CC}$ - 0.250 in low-side current sensing

$V = V_{CC}$ in high-side current sensing

TCO is determined by the values of RT1 and RT2. 1% resistors are recommended.

9/16

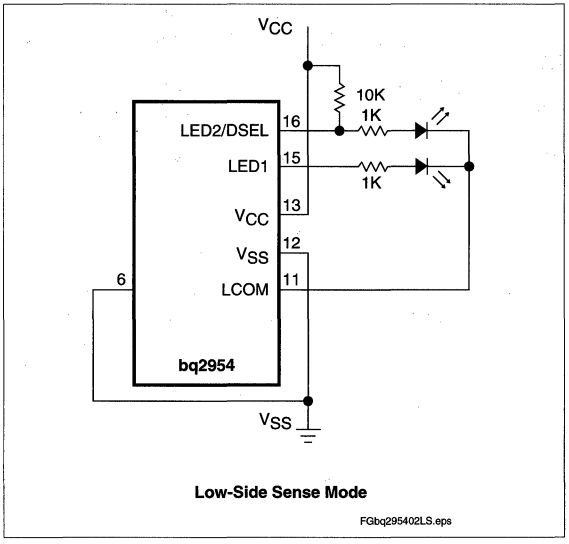


Figure 4. Configured Display Mode (Low-Side Sense)

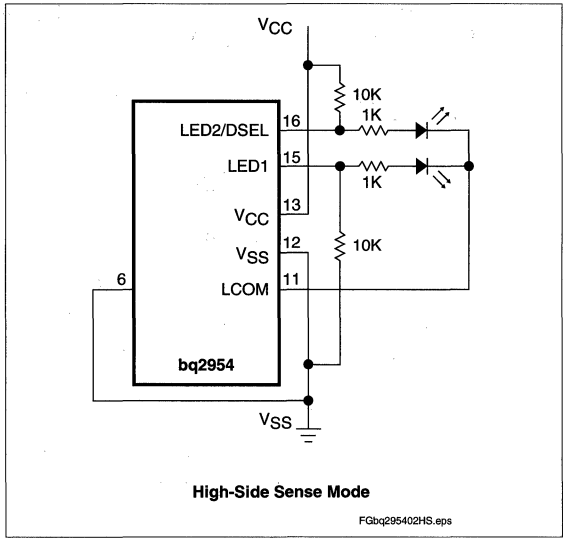


Figure 5. Configured Display Mode (High-Side Sense)

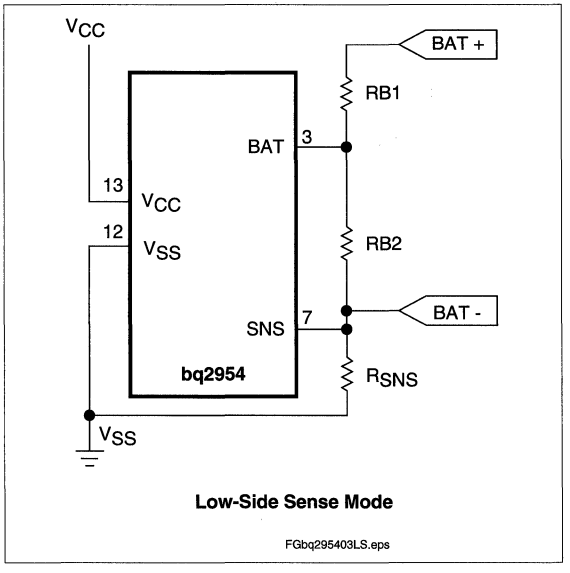


Figure 6. Configuring the Battery Divider (Low-Side Sense)

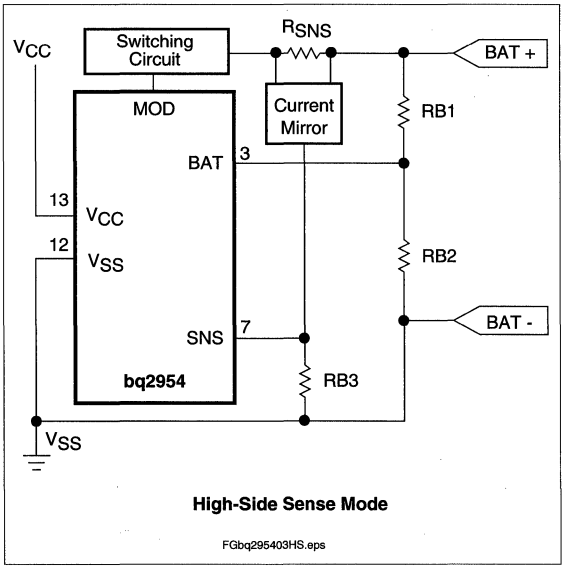


Figure 7. Configuring the Battery Divider (High-Side Sense)

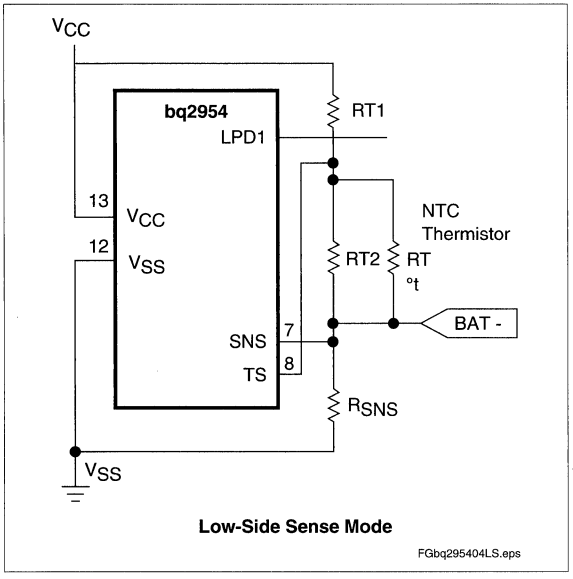


Figure 8. Low-Side Temperature Sensing

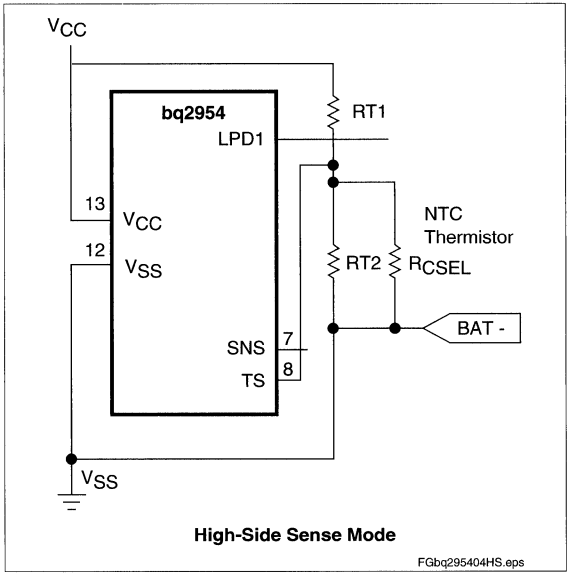


Figure 9. High-Side Temperature Sensing

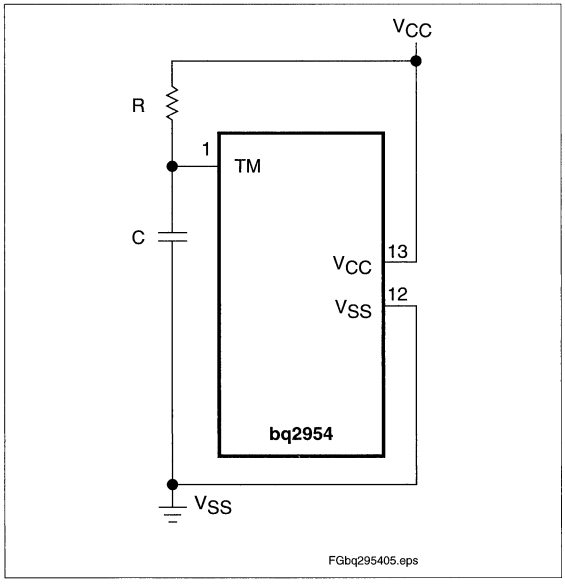


Figure 10. R-C Network/Setting MTO

Disabling Temperature Sensing

Temperature sensing can be disabled by placing a 10kΩ resistor between TS and BAT- and a 10kΩ resistor between TS and V_{CC}. See Figures 8 and 9.

Maximum Time-Out

Maximum Time-Out period (t_{MTO}) is programmed from 1 to 24 hours by an R-C network on the TM pin (see Figure 10) per the following equation:

$$t_{MTO} = 500 * R * C \quad (5)$$

where R is in ohms, C is in Farads, and t_{MTO} is in hours. The recommended value for C is 0.1µF.

The MTO timer is reset at the beginning of fast charge. If the MTO timer expires during the voltage regulation phase, fast charging terminates and the bq2954 enters the Charge Complete state. If the conditioning phase continues for time equal to t_{QT} (MTO/4) and the battery potential does not reach V_{MIN}, the bq2954 enters the fault state and terminates charge. See Table 3. If the MTO timer expires during the current-regulation phase (V_{BAT} never reaches V_{REG}), fast charging is terminated, and the bq2954 enters the fault state.

Charge Regulation

The bq2954 controls charging through pulse-width modulation of the MOD output pin, supporting both constant-current and constant-voltage regulation. Charge current is monitored at the SNS pin, and charge voltage is monitored at the BAT pin. These voltages are compared to an internal reference, and the MOD output is modulated to maintain the desired value. The maximum duty cycle is 80% .

Voltage at the SNS pin is determined by the value of resistor R_{SNS}, so nominal regulated current is set by the following equation:

$$I_{MAX} = V_{SNS} / R_{SNS} \quad (6)$$

The switching frequency of the MOD output is determined by an external capacitor (CPWM) between the pin TPWM and V_{SS} pins, per the following:

$$f_{PWM} = \frac{1 * 10^{-4}}{C_{PWM}} \quad (7)$$

Where C is in Farads and the frequency is in Hz. A typical switching rate is 100kHz, implying C_{PWM} = 0.001µF. MOD pulse width is modulated between 0 and 80% of the switching period.

To prevent oscillation in the voltage and current control loops, frequency compensation networks (C and R-C respectively) are typically required on the V_{COMP} and I_{COMP} pins .

Recharge After Fast Charge

Once charge completion occurs, a fast charge is initiated when the battery voltage falls below V_{RECHG} threshold. A delay of approximately one second passes before recharge begins so that adequate time is allowed to detect battery removal. (See Table 1.)

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	-20	+70	°C	Commercial
		-40	+85	°C	Industrial "N"
T_{STG}	Storage temperature	-55	+125	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10s max.

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds ($T_A = T_{OPR}$; V_{CC} = 5V ±10%)

Symbol	Parameter	Rating	Unit	Tolerance	Notes
V_{REG}	Internal reference voltage	2.05	V	1%	TA = 25°C
	Temperature coefficient	-0.5	mV/°C	10%	
V_{LTF}	TS maximum threshold	0.6 * V_{CC}	V	±0.03V	Low-temperature fault
V_{HTF}	TS hysteresis threshold	0.44 * V_{CC}	V	±0.03V	High-temperature fault
V_{TCO}	TS minimum threshold	0.4 * V_{CC}	V	±0.03V	Temperature cutoff
V_{HCO}	High cutoff voltage	V_{REG} + 0.25V	V	±0.03V	
V_{MIN}	Under-voltage threshold at BAT	1.5	V	±0.05V	
V_{RECHG}	Recharge voltage threshold at BAT	1.92	V	±0.05V	
V_{LCO}	Low cutoff voltage	0.8	V	±0.03V	
V_{SNS}	Current sense at SNS	0.250	V	10%	I_{MAX}
		0.025	V	10%	I_{COND}

13/16

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{TEMP}	TS voltage potential	0	-	V_{CC}	V	V_{TS} - V_{SNS}
V_{BAT}	BAT voltage potential	0	-	V_{CC}	V	
I_{CC}	Supply current	-	2	4	mA	Outputs unloaded
I_{IZ}	DSEL tri-state open detection	-2	-	2	µA	Note
	I_{TERM} tri-state open detection	-2		2	µA	
V_{IH}	Logic input high	V_{CC} - 0.3	-	-	V	DSEL, I_{TERM}
V_{IL}	Logic input low	-	-	V_{SS} + 0.3	V	DSEL, CSEL, I_{TERM}
V_{OH}	LED_1, LED_2, BTST, output high	V_{CC} - 0.8	-	-	V	$I_{OH} \leq 10mA$
	MOD output high	V_{CC} - 0.8	-	-	V	$I_{OH} \leq 10mA$
V_{OL}	LED_1, LED_2, BTST, output low	-	-	V_{SS} +0.8	V	$I_{OL} \leq 10mA$
	MOD output low	-	-	V_{SS} + 0.8	V	$I_{OL} \leq 10mA$
	CHG output low	-	-	V_{SS} + 0.8	V	$I_{OL} \leq 5mA$, Note 3
	LCOM output low	-	-	V_{SS} + 0.5	V	$I_{OL} \leq 30mA$
I_{OH}	LED_1, LED_2, BTST, source	-10	-	-	mA	$V_{OH} = V_{CC}$ - 0.5V
	MOD source	-5.0	-	-	mA	$V_{OH} = V_{CC}$ - 0.5V
I_{OL}	LED_1, LED_2, BTST, sink	10	-	-	mA	$V_{OL} = V_{SS}$ + 0.5V
	MOD sink	5	-	-	mA	$V_{OL} = V_{SS}$ + 0.8V
	CHG sink	5	-	-	mA	$V_{OL} = V_{SS}$ + 0.8V, Note 3
	LCOM sink	30	-	-	mA	$V_{OL} = V_{SS}$ + 0.5V
I_{IL}	DSEL logic input low source	-	-	+30	µA	V = V_{SS} to V_{SS} + 0.3V, Note 2
	I_{TERM} logic input low source	-	-	+70	µA	V = V_{SS} to V_{SS} + 0.3V
I_{IH}	DSEL logic input high source	-30	-	-	µA	V = V_{CC} - 0.3V to V_{CC}
	I_{TERM} logic input high source	-70	-	-	µA	V = V_{CC} - 0.3V to V_{CC}

Notes:
1. All voltages relative to V_{SS}.
2. Conditions during initialization after V_{CC} applied.
3. SNS = 0V.

Impedance ($T_A = T_{OPR}$; V_{CC} = 5V ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
R_{BATZ}	BAT pin input impedance	50	-	-	MΩ	
R_{SNSZ}	SNS pin input impedance	50	-	-	MΩ	
R_{TSZ}	TS pin input impedance	50	-	-	MΩ	
R_{PROG1}	Soft-programmed pull-up or pull-down resistor value (for programming)	-	-	10	kΩ	DSEL, CSEL
R_{PROG2}	Pull-up or pull-down resistor value	-	-	3	kΩ	I_{TERM}
R_{MTO}	Charge timer resistor	20	-	480	kΩ	

Timing ($T_A = T_{OPR}$; V_{CC} = 5V ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{MTO}	Charge time-out range	1	-	24	hours	See Figure 10
t_{QT}	Pre-charge qual test time-out period	-	0.25 * t_{MTO}	-	-	
t_{HO}	Pre-charge qual test hold-off period	300	600	900	ms	
f_{PWM}	PWM regulator frequency range	-	100	200	kHz	See Equation 7
d_{PWM}	Duty cycle	0	-	80	%	

Capacitance

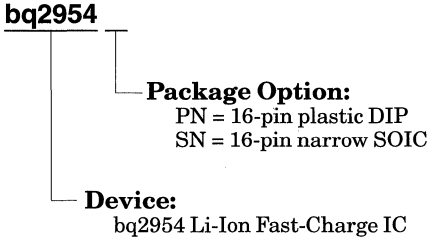
Symbol	Parameter	Minimum	Typical	Maximum	Unit
C_{MTO}	Charge timer capacitor	-	-	0.1	µF
C_{PWM}	PWM capacitor	-	0.001	-	µF

Data Sheet Revision History

ChangeNo.	Page No.	Description of Change
1	All	"Final" changes from "Preliminary" version

Note: Change 1 = Oct. 1998 B changes from Nov. 1997 "Preliminary."

Ordering Information

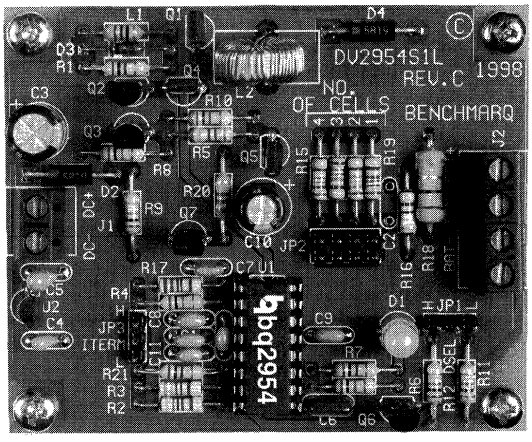


Li-Ion Charger Development System

Control of On-Board PNP Switch-Mode Regulator with Low-Side Current Sensing

Features

- bq2954 fast-charge control evaluation and development, based on switching buck converter with low-side battery-current sensing
- On-board configuration for fast charge of 1, 2, 3, or 4 Li-Ion cells
- Charge termination by maximum voltage, selectable minimum current, or maximum time-out
- Constant current (up to 1.25A) and constant voltage (up to 16.8V) provided by on-board switch-mode regulator
- Jumper-configurable bicolor-LED display
- Direct connections for battery and thermistor
- Maximum charge time of 5 hours



General Description

The DV2954S1L Development System provides a development environment for the bq2954 Lithium Ion Fast-Charge IC. The DV2954S1L incorporates a bq2954 and a buck-type switch-mode regulator to provide fast charge control for 1 through 4 Li-Ion cells.

Fast charge is preceded by a pre-charge qualification period.

Fast charge termination occurs on:

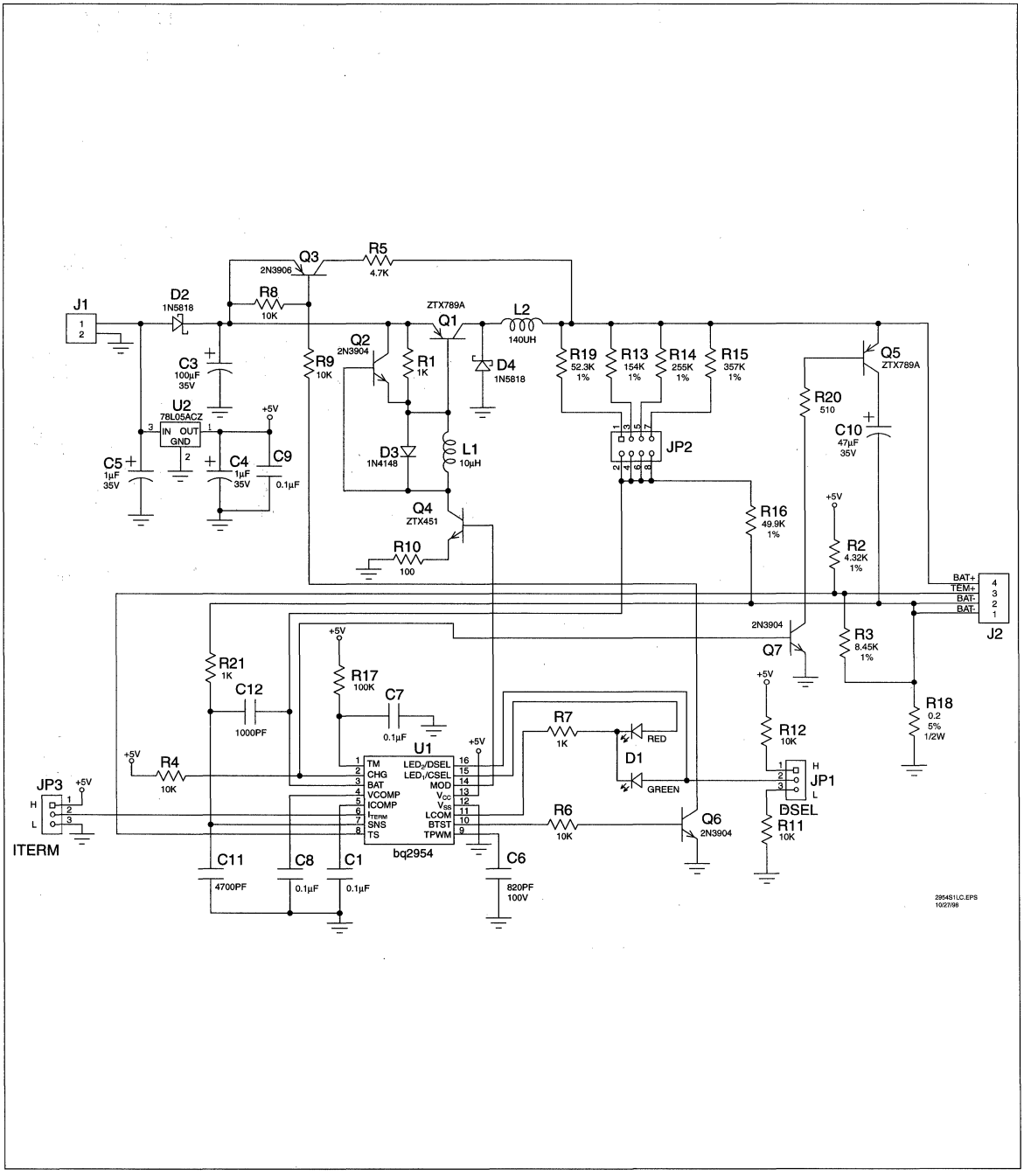
- Minimum current – I_{MAX} divided by 10, 15, or 20
- Maximum time-out

The bq2954 can be reset and a new charge cycle started by applicaton of power to the board or battery replacement. The board automatically initiates a recharge when the battery voltage drops to 3.85V per cell.

The user provides a DC power supply and batteries and configures the board for the number of cells, the minimum current threshold, and the LED display mode. The board has direct connections for the battery and the provided thermistor.

Before using the DV2954S1L board, please review the bq2954 data sheet. A full data sheet for this product is available on the Unitrode web site, or you may contact the factory for one

DV2954S1L Board Schematic



Rev. C Board

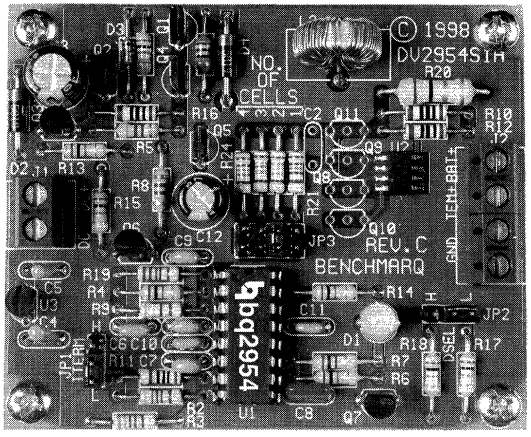
Product Brief **DV2954S1H**

Li-Ion Charger Development System

Control of On-Board PNP Switch-Mode Regulator with High-Side Current Sensing

Features

- bq2954 fast-charge control evaluation and development, based on switching buck converter with high-side battery-current sensing
- On-board configuration for fast charge of 1, 2, 3, or 4 Li-Ion cells
- Charge termination by maximum voltage, selectable minimum current, or maximum time-out
- Constant current (up to 1.25A) and constant voltage (up to 16.8V) provided by on-board switch-mode regulator
- Jumper-configurable bicolor-LED display
- Direct connections for battery and thermistor
- Maximum charge time of 5 hours



General Description

The DV2954S1H Development System provides a development environment for the bq2954 Lithium Ion Fast-Charge IC. The DV2954S1H incorporates a bq2954 and a buck-type switch-mode regulator to provide fast-charge control for 1–4 Li-Ion cells.

Fast charge is preceded by a pre-charge qualification period.

Fast charge termination occurs on:

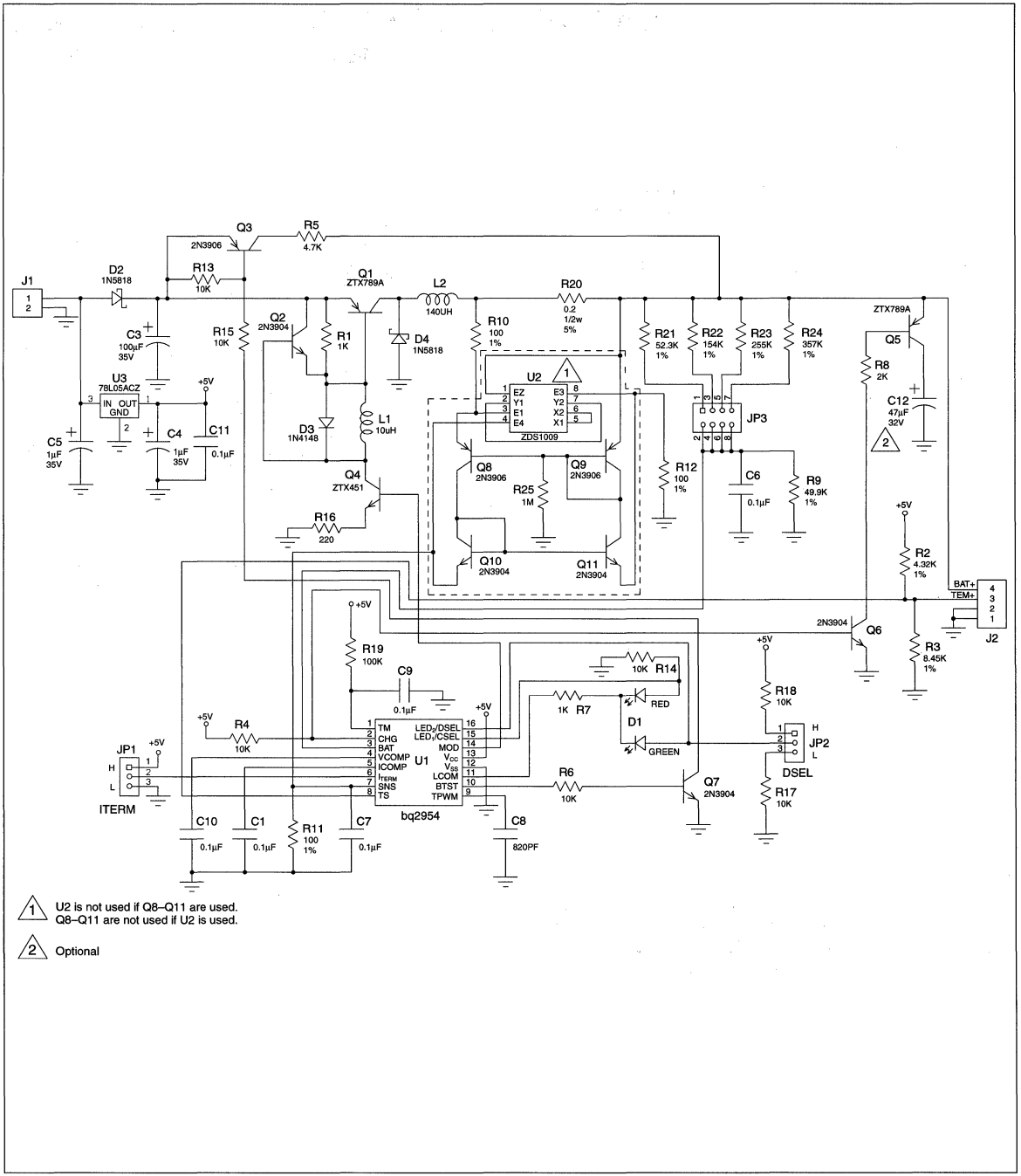
- Minimum current – I_{MAX} divided by 10, 15, or 20
- Maximum time-out

The bq2954 can be reset and a new charge cycle started by applicaton of power to the board or replacement of the battery. The board automatically initiates a recharge when the battery voltage drops to 3.85V per cell.

The user provides a DC power supply and batteries and configures the board for the number of cells, the minimum current threshold, and the LED display mode. The board has direct connections for the battery and the provided thermistor.

Before using the DV2954S1H board, please review the bq2954 data sheet. A full data sheet for this product is available on the Unitrode web site, or you may contact the factory for one

DV2954S1H Board Schematic



1 U2 is not used if Q8–Q11 are used.
Q8–Q11 are not used if U2 is used.

2 Optional

Rev. C Board

UNITRODE

application INFO available

UC2906
UC3906

Sealed Lead-Acid Battery Charger

FEATURES

- Optimum Control for Maximum Battery Capacity and Life
- Internal State Logic Provides Three Charge States
- Precision Reference Tracks Battery Requirements Over Temperature
- Controls Both Voltage and Current at Charger Output
- System Interface Functions
- Typical Standby Supply Current of only 1.6mA

DESCRIPTION

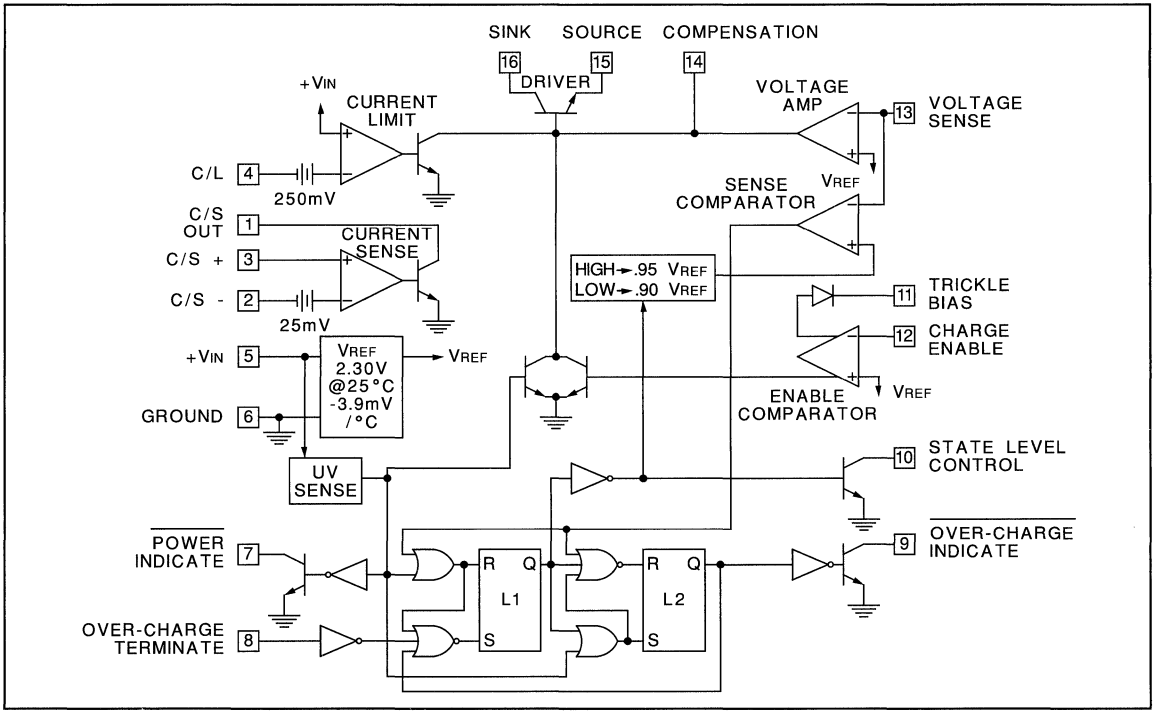
The UC2906 series of battery charger controllers contains all of the necessary circuitry to optimally control the charge and hold cycle for sealed lead-acid batteries. These integrated circuits monitor and control both the output voltage and current of the charger through three separate charge states; a high current bulk-charge state, a controlled over-charge, and a precision float-charge, or standby, state.

Optimum charging conditions are maintained over an extended temperature range with an internal reference that tracks the nominal temperature characteristics of the lead-acid cell. A typical standby supply current requirement of only 1.6mA allows these ICs to predictably monitor ambient temperatures.

Separate voltage loop and current limit amplifiers regulate the output voltage and current levels in the charger by controlling the onboard driver. The driver will supply up to 25mA of base drive to an external pass device. Voltage and current sense comparators are used to sense the battery condition and respond with logic inputs to the charge state logic. A charge enable comparator with a trickle bias output can be used to implement a low current turn-on mode of the charger, preventing high current charging during abnormal conditions such as a shorted battery cell.

Other features include a supply under-voltage sense circuit with a logic output to indicate when input power is present. In addition the over-charge state of the charger can be externally monitored and terminated using the over-charge indicate output and over-charge terminate input.

BLOCK DIAGRAM



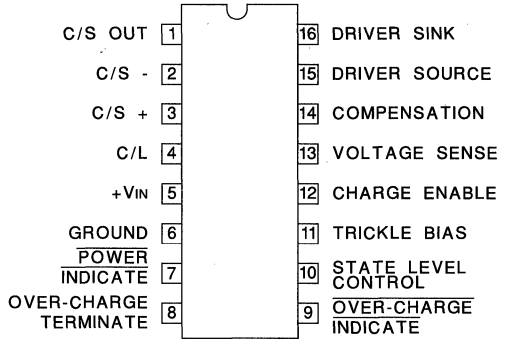
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (+V_{IN}) 40V
Open Collector Output Voltages 40V
Amplifier and Comparator Input Voltages . . . . . –0.3V to +40V
Over-Charge Terminate Input Voltage . . . . . –0.3V to +40V
Current Sense Amplifier Output Current. 80mA
Other Open Collector Output Currents 20mA
Trickle Bias Voltage Differential with respect to V_{IN} . . . . . –32V
Trickle Bias Output Current . . . . . –40mA
Driver Current 80mA
Power Dissipation at T_A = 25°C (Note 2) 1000mW
Power Dissipation at T_C = 25°C (Note 2) 2000mW
Operating Junction Temperature . . . . . –55°C to +150°C
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

Note 1: *Voltages are referenced to ground (Pin 6). Currents are positive into, negative out of, the specified terminals.*

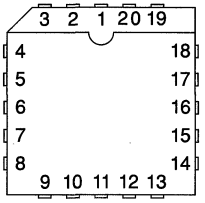
Note 2: *Consult Packaging section of Databook for thermal limitations and considerations of packages.*

DIL-16, SOIC-16 (TOP VIEW)
J or N Package, DW Package



CONNECTION DIAGRAMS

PLCC-20, LCC-20 (TOP VIEW)
Q, L Packages



PIN FUNCTION	PIN
N/C	1
C/S OUT	2
C/S-	3
C/S+	4
C/L	5
N/C	6
+V_{IN}	7
GROUND	8
POWER INDICATE	9
OVER CHARGE TERMINATE	10
N/C	11
OVER CHARGE INDICATE	12
STATE LEVEL CONTROL	13
TRICKLE BIAS	14
CHARGE ENABLE	15
N/C	16
VOLTAGE SENSE	17
COMPENSATION	18
DRIVER SOURCE	19
DRIVER SINK	20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –40°C to +70°C for the UC2906 and 0°C to +70°C for the UC3906, +V_{IN} = 10V, T_A = T_J.

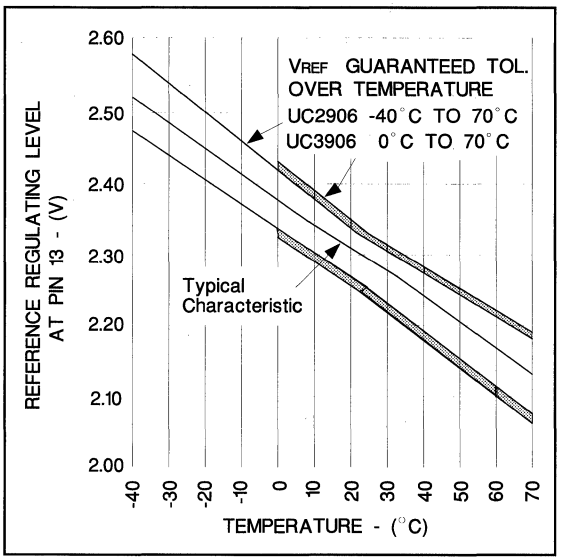
PARAMETER	TEST CONDITIONS	UC2906			UC3906			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Supply								
Supply Current	+V_{IN} = 10V		1.6	2.5		1.6	2.5	mA
	+V_{IN} = 40V		1.8	2.7		1.8	2.7	mA
Supply Under-Voltage Threshold	+V_{IN} = Low to High	4.2	4.5	4.8	4.2	4.5	4.8	V
Supply Under-Voltage Hysteresis			0.20	0.30		0.20	0.30	V
Internal Reference (V_{REF})								
Voltage Level (Note 3)	Measured as Regulating Level at Pin 13 w/ Driver Current = 1mA, T_J = 25°C	2.275	2.3	2.325	2.270	2.3	2.330	V
Line Regulation	+V_{IN} = 5 to 40V		3	8		3	8	mV
Temperature Coefficient			–3.9			–3.9		mV/°C

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –40°C to +70°C for the UC2906 and 0°C to +70°C for the UC3906, $+V_{IN}$ = 10V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC2906			UC3906			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Voltage Amplifier								
Input Bias Current	Total Input Bias at Regulating Level	–0.5	–0.2		–0.5	–0.2		µA
Maximum Output Current	Source	–45	–30	–15	–45	–30	–15	µA
	Sink	30	60	90	30	60	90	µA
Open Loop Gain	Driver current = 1mA	50	65		50	65		dB
Output Voltage Swing	Volts above GND or below $+V_{IN}$		0.2			0.2		V
Driver								
Minimum Supply to Source Differential	Pin 16 = $+V_{IN}$, I_O = 10mA		2.0	2.2		2.0	2.2	V
Maximum Output Current	Pin 16 to Pin 15 = 2V	25	40		25	40		mA
Saturation Voltage			0.2	0.45		0.2	0.45	V
Current Limit Amplifier								
Input Bias Current			0.2	1.0		0.2	1.0	µA
Threshold Voltage	Offset below $+V_{IN}$	225	250	275	225	250	275	mV
Threshold Supply Sensitivity	$+V_{IN}$ = 5 to 40V		0.03	0.25		0.03	0.25	%/V
Voltage Sense Comparator								
Threshold Voltage	As a function of V_{REF}, L_1 = RESET	0.945	0.95	0.955	0.945	0.95	0.955	V/V
	As a function of V_{REF}, L_1 = SET	0.895	0.90	0.905	0.895	0.90	0.905	V/V
Input Bias Current	Total Input Bias at Thresholds	–0.5	–0.2		–0.5	–0.2		µA
Current Sense Comparator								
Input Bias Current			0.1	0.5		0.1	0.5	µA
Input Offset Current			0.01	0.2		0.01	0.2	µA
Input Offset Voltage	Referenced to Pin 2, I_{OUT} = 1mA	20	25	30	20	25	30	mV
Offset Supply Sensitivity	$+V_{IN}$ = 5 to 40V		0.05	0.35		0.05	0.35	%/V
Offset Common Mode Sensitivity	CMV = 2V to $+V_{IN}$		0.05	0.35		0.05	0.35	%/V
Maximum Output Current	V_{OUT} = 2V	25	40		25	40		mA
Output Saturation Voltage	I_{OUT} = 10mA		0.2	0.45		0.2	0.45	V
Enable Comparator								
Threshold Voltage	As a function of V_{REF}	0.99	1.0	1.01	0.99	1.0	1.01	V/V
Input Bias Current		–0.5	–0.2		–0.5	–0.2		µA
Trickle Bias Maximum Output Current	$V_{OUT} = +V_{IN} - 3V$	25	40		25	40		mA
Trickle Bias Maximum Output Voltage	Volts below $+V_{IN}$, I_{OUT} = 10mA		2.0	2.6		2.0	2.6	V
Trickle Bias Reverse Hold-Off Voltage	$+V_{IN}$ = 0V, I_{OUT} = –10µA	6.3	7.0		6.3	7.0		V
Over-Charge Terminate Input								
Threshold Voltage		0.7	1.0	1.3	0.7	1.0	1.3	V
Internal Pull-Up Current	At Threshold		10			10		µA
Open Collector Outputs (Pins 7, 9, and 10)								
Maximum Output Current	V_{OUT} = 2V	2.5	5		2.5	5		mA
Saturation Voltage	I_{OUT} = 1.6mA		0.25	0.45		0.25	0.45	V
	I_{OUT} = 50µA		0.03	0.05		0.03	0.05	V
Leakage Current	V_{OUT} = 40V		1	3		1	3	µA

Note 3. The reference voltage will change as a function of power dissipation on the die according to the temperature coefficient of the reference and the thermal resistance, junction-to-ambient.

OPERATION AND APPLICATION INFORMATION



Internal reference temperature characteristic and tolerance.

Dual Level Float Charger Operations

The UC2906 is shown configured as a dual level float charger in Figure 1. All high currents are handled by the external PNP pass transistor with the driver supplying base drive to this device. This scheme uses the TRICKLE BIAS output and the charge enable comparator to give the charger a low current turn on mode. The output current of the charger is limited to a low-level until the battery reaches a specified voltage, preventing a high current charging if a battery cell is shorted. Figure 2 shows the state diagram of the charger. Upon turn on the UV sense circuitry puts the charger in state 1, the high rate bulk-charge state. In this state, once the enable threshold has been exceeded, the charger will supply a peak current that is determined by the 250mV offset in the C/L amplifier and the sensing resistor R_S.

To guarantee full re-charge of the battery, the charger's voltage loop has an elevated regulating level, V_{OC}, during state 1 and state 2. When the battery voltage reaches 95% of V_{OC}, the charger enters the over-charge state, state 2. The charger stays in this state until the OVER-CHARGE TERMINATE pin goes high. In Figure 1, the charger uses the current sense amplifier to generate this signal by sensing when the charge current has tapered to a specified level, I_{OCT}. Alternatively the over-charge could have been controlled by an external source, such as a timer, by using the OVER-CHARGE INDICATE signal at Pin 9. If a load is applied to the battery and begins to discharge it, the charger will contribute its full output to the load. If the battery drops 10% below the float level, the charger will reset itself to state 1. When the load is removed a full charge cycle will follow. A graphical representation of a charge, and discharge, cycle of the dual lever float charger is shown in Figure 3.

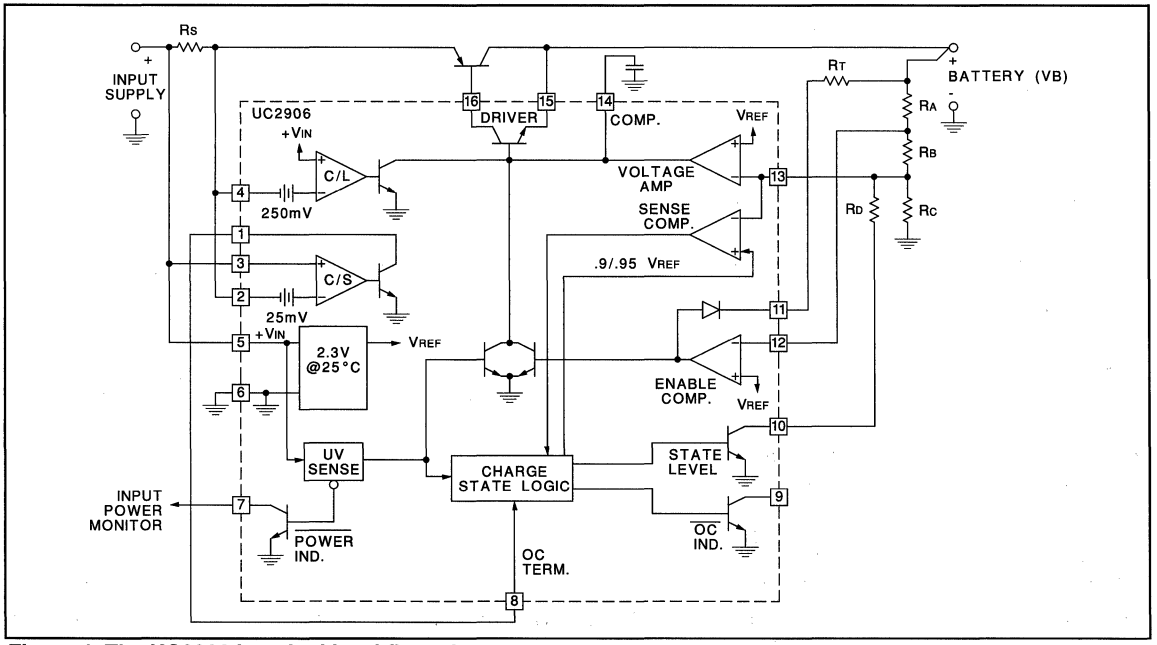


Figure 1. The UC2906 in a dual level float charger.

OPERATION AND APPLICATION INFORMATION (cont.)

Design Procedure

1) *Pick divider current, I_D. Recommended value is 50μA to 100μA.*

2) $R_C = 2.3V / I_D$

3) $R_A + R_B = R_{SUM} = (V_F - 2.3V) / I_D$

4) $R_D = 2.3V \bullet R_{SUM} / (V_{OC} - V_F)$

5) $R_A = (R_{SUM} + R_X)(1 - 2.3V / V_T)$
WHERE: $R_X = R_C \bullet R_D / (R_C + R_D)$

6) $R_B = R_{SUM} - R_A$

7) $R_S = 0.25V / I_{MAX}$

8) $R_T = (V_{IN} - V_T - 2.5V) / I_T$

9) $I_{OCT} = \frac{I_{MAX}}{10}$

Note: $V_{12} = 0.95 V_{OC}$,
$V_{31} = 0.90 V_F$,

For further design and application information see UICC Application Note U-104

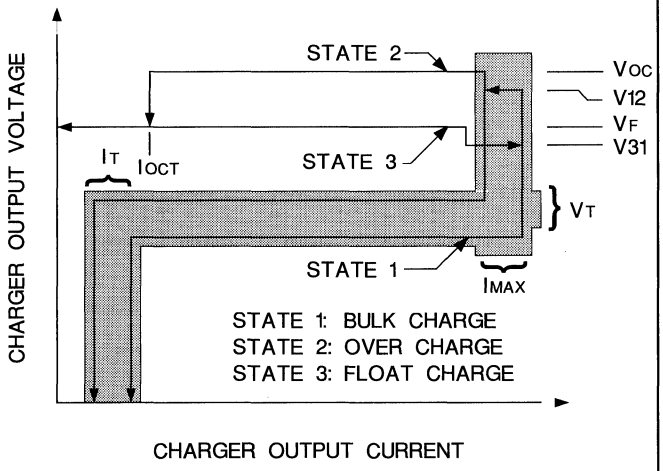
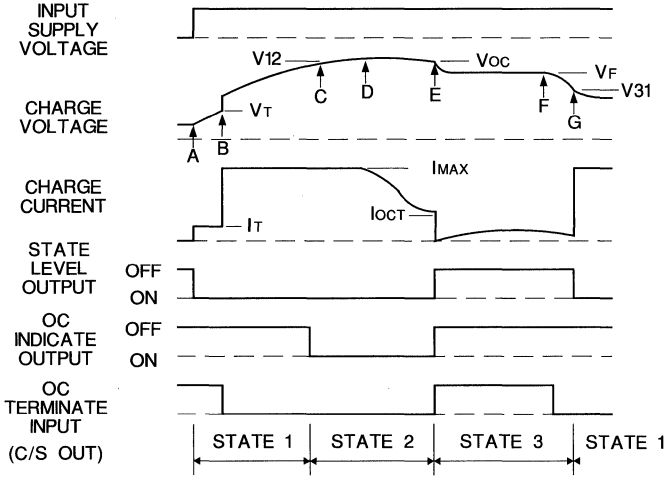


Figure 2. State diagram and design equations for the dual level float charger.



Explanation: Dual Level Float Charger

A. *Input power turns on, battery charges at trickle current rate.*
B. *Battery voltage reaches V_T enabling the driver and turning off the trickle bias output, battery charges at I_{MAX} rate.*
C. *Transition voltage V_{12} is reached and the charger indicates that it is now in the over-charge state, state 2.*
D. *Battery voltage approaches the over-charge level V_{OC} and the charge current begins to taper.*
E. *Charge current tapers to I_{OCT}. The current sense amplifier output, in this case tied to the OC TERMINATE input, goes high. The charger changes to the float state and holds the battery voltage at V_F.*
F. *Here a load (>I_{MAX}) begins to discharge the battery.*
G. *The load discharges the battery such that the battery voltage falls below V_{31}. The charger is now in state 1, again.*

Figure 3. Typical charge cycle: UC2906 dual level float charger.

OPERATION AND APPLICATION INFORMATION (cont.)

Compensated Reference Matches Battery Requirements

When the charger is in the float state, the battery will be maintained at a precise float voltage, V_F. The accuracy of this float state will maximize the standby life of the battery while the bulk-charge and over-charge states guarantee rapid and full re-charge. All of the voltage thresholds on the UC2906 are derived from the internal reference. This reference has a temperature coefficient that tracks the temperature characteristic of the optimum-charge and hold levels for sealed lead-acid cells. This further guarantees that proper charging occurs, even at temperature extremes.

Dual Step Current Charger Operation

Figures 4, 5 and 6 illustrate the UC2906's use in a different charging scheme. The dual step current charger is useful when a large string of series cells must be charged. The holding-charge state maintains a slightly elevated voltage across the batteries with the holding current, 1H. This will tend to guarantee equal charge distribution between the cells. The bulk-charge state is similar to that of the float charger with the exception that when V_{12} is reached, no over-charge state occurs since Pin 8 is tied high at all times. The current sense amplifier is used to regulate the holding current. In some applications a series resistor, or external buffering transistor, may be required at the current sense output to prevent excessive power dissipation on the UC2906.

A PNP Pass Device Reduces Minimum Input to Output Differential

The configuration of the driver on the UC2906 allows a good bit of flexibility when interfacing to an external pass transistor. The two chargers shown in Figures 1 and 4 both use PNP pass devices, although an NPN device driven from the source output of the UC2906 driver can also be used. In situations where the charger must operate with low input to output differentials the PNP pass device should be configured as shown in Figure 4. The PNP can be operated in a saturated mode with only the series diode and sense resistor adding to the minimum differential. The series diode, D1, in many applications, can be eliminated. This diode prevents any discharging of the battery, except through the sensing divider, when the charger is attached to the battery with no input supply voltage. If discharging under this condition must be kept to an absolute minimum, the sense divider can be referenced to the $\overline{\text{POWER INDICATE}}$ pin, Pin 7, instead of ground. In this manner the open collector off state of Pin 7 will prevent the divider resistors from discharging the battery when the input supply is removed.

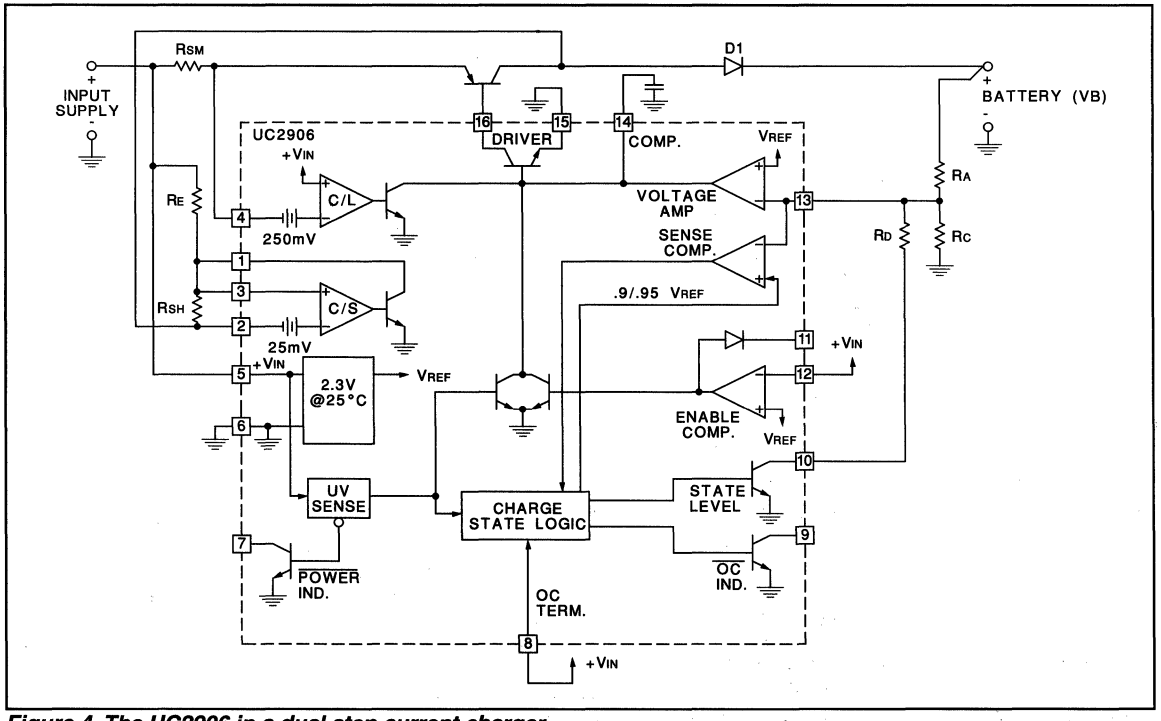


Figure 4. The UC2906 in a dual step current charger.

OPERATION AND APPLICATION INFORMATION (cont.)

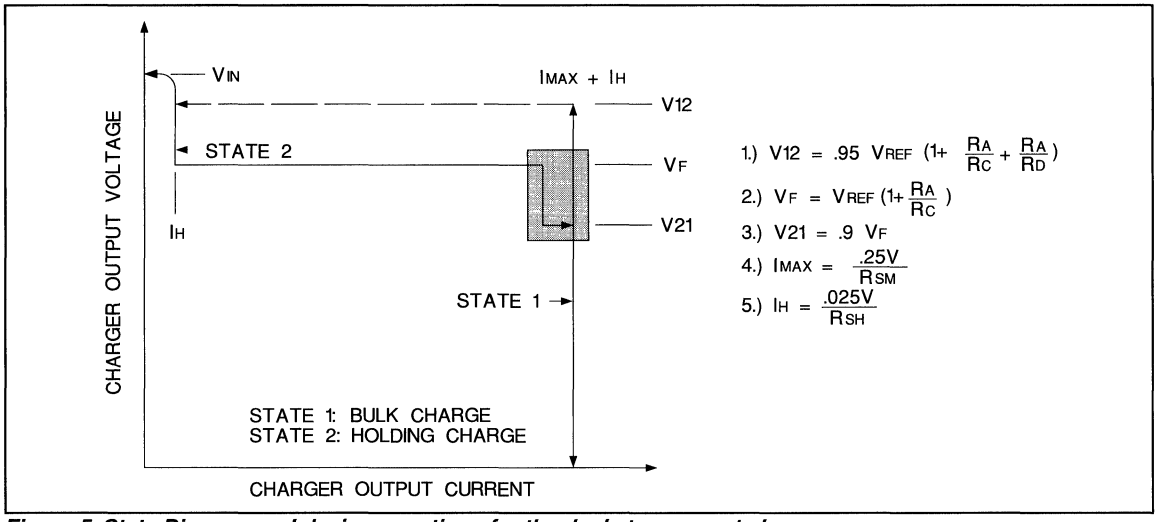
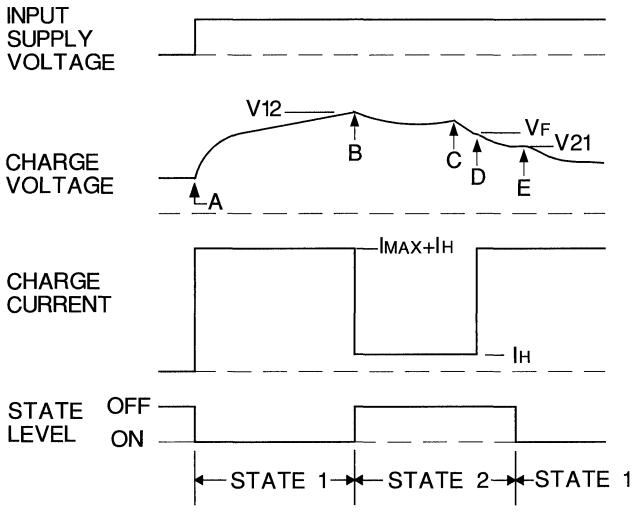


Figure 5. State Diagram and design equations for the dual step current charger.



Explanation: Dual Step Current Charger

A. *Input power turns on, battery charges at a rate of $I_H + I_{MAX}$.*
B. *Battery voltage reaches V_{12} and the voltage loop switches to the lower level V_F. The battery is now fed with the holding current I_H.*
C. *An external load starts to discharge the battery.*
D: *When V_F is reached the charger will supply the full current $I_{MAX} + I_H$.*
E. *The discharge continues and the battery voltage reaches V_{21} causing the charger to switch back to state 1.*

Figure 6. Typical charge cycle: UC2906 dual step current charger

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Switchmode Lead-Acid Battery Charger

application INFO available

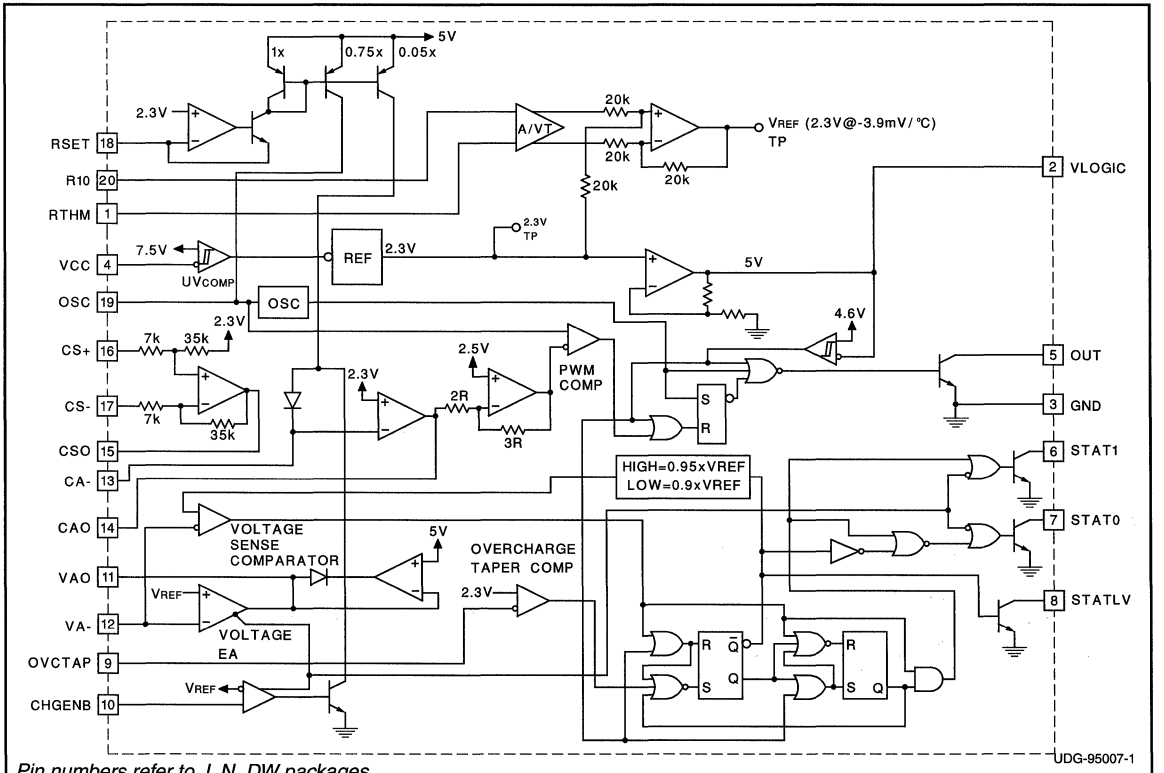
FEATURES

- Accurate and Efficient Control of Battery Charging
- Average Current Mode Control from Trickle to Overcharge
- Resistor Programmable Charge Currents
- Thermistor Interface Tracks Battery Requirements Over Temperature
- Output Status Bits Report on Four Internal Charge States
- Undervoltage Lockout Monitors VCC and VREF

DESCRIPTION

The UC3909 family of Switchmode Lead-Acid Battery Chargers accurately controls lead acid battery charging with a highly efficient average current mode control loop. This chip combines charge state logic with average current PWM control circuitry. Charge state logic commands current or voltage control depending on the charge state. The chip includes undervoltage lockout circuitry to insure sufficient supply voltage is present before output switching starts. Additional circuit blocks include a differential current sense amplifier, a 1.5% voltage reference, a –3.9mV/°C thermistor linearization circuit, voltage and current error amplifiers, a PWM oscillator, a PWM comparator, a PWM latch, charge state decode bits, and a 100mA open collector output driver.

BLOCK DIAGRAM



Pin numbers refer to J, N, DW packages.

ABSOLUTE MAXIMUM RATINGS

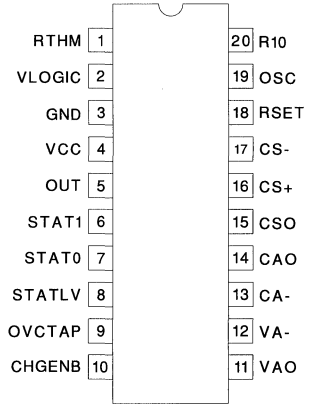
Supply Voltage (VCC), OUT, STAT0, STAT1 . . . . . 40V
Output Current Sink 0.1A
CS+, CS- . . . . . -0.4 to VCC (Note 1)
Remaining Pin Voltages . . . . . -0.3V to 9V
Storage Temperature . . . . . -65°C to +150°C
Junction Temperature . . . . . -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

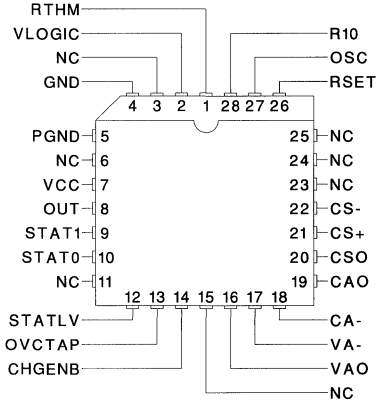
Note 1: *Voltages more negative than -0.4V can be tolerated if current is limited to 50mA.*

CONNECTION DIAGRAMS

DIL-20, (Top View)
J or N, DW Packages



LCC-28, PLCC-28 (Top View)
L, Q Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –40°C to +85°C for UC2909; °0C to +70°C for UC3909; C_T = 330pF, R_{SET} = 11.5k, R10 = 10k, R_{THM} = 10k, V_{CC} = 15V, Output no load, R_{STAT0} = R_{STAT1} = 10k, CHGENB = OVCTAP = VLOGIC, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Sense AMP (CSA) Section	V_{ID} = CS+ – CS–				
DC Gain	CS– = 0, CS+ = -50mV; CS+ = –250mV	4.90	5	5.10	V/V
	CS+ = 0, CS– = 50mV; CS–- = 250mV	4.90	5	5.10	V/V
V_{OFFSET} (V_{CSO} – V_{CAO})	CS+ = CS– = 2.3V, CAO = CA–			15	mV
CMRR	V_{CM} = –0.25 to VCC – 2, 8.8 < VCC < 14	50			dB
	V_{CM} = –0.25 to VCC, 14 < VCC < 35	50			dB
V_{OL}	V_{ID} = –550mV, –0.25V < VCM < VCC–2, I_O = 500µA		0.3	0.6	V
V_{OH}	V_{ID} = +700mV, –0.25V < VCM < VCC–2, I_O = –250µA	5.2	5.7	6.2	V
Output Source Current	V_{ID} = +700mV, CSO = 4V		–1	–0.5	mA
Output Sink Current	V_{ID} = –550mV, CSO = 1V	3	4.5		mA
3dB Bandwidth	V_{ID} = 90mV, V_{CM} = 0V	200			kHz

ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –40°C to +85°C for UC2909; °0C to +70°C for UC3909; C_T = 330pF, R_{SET} = 11.5k, R10 = 10k, R_{THM} = 10k, V_{CC} = 15V, Output no load, R_{STAT0} = R_{STAT1} = 10k, CHGENB = OVCTAP = VLOGIC, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Error Amplifier (CEA) Section					
I_B	8.8V < VCC < 35V, V_{CHGENB} = V_{LOGIC}		0.1	0.8	µA
V_{IO} (Note 2)	8.8V < VCC < 35V, CAO = CA–			10	mV
A_{VO}	1V < VAO < 4V	60	90		dB
GBW	T_J = 25°C, F = 100kHz	1	1.5		MHz
V_{OL}	I_O = 250µA		0.4	0.6	V
V_{OH}	I_O = –5mA	4.5	5		V
Output Source Current	CAO = 4V		–25	–12	mA
Output Sink Current	CAO = 1V	2	3		mA
$I_{CA–}$, $I_{TRCK\_CONTROL}$	V_{CHGENB} = GND	8.5	10	11.5	µA
Voltage Amplifier (CEA) Section					
I_B	Total Bias Current; Regulating Level		0.1	1	µA
V_{IO} (Note 2)	8.8V < VCC < 35V, VCM = 2.3V, VAO = VA–		1.2		mV
A_{VO}	1V < CAO < 4V	60	90		dB
GBW	T_J = 25°C, F = 100kHz	0.25	0.5		MHz
V_{OL}	I_O = 500µA		0.4	0.6	V
V_{OH}	I_O = –500µA	4.75	5	5.25	V
Output Source Current	CAO = 4V	–2	–1		mA
Output Sink Current	CAO = 1V	2	2.5		mA
VAO Leakage: High Impedance State	V_{CHGENB} = GND, STAT0 = 0 & STAT1 = 0, VAO = 2.3V	–1		1	µA
Pulse Width Modulator Section					
Maximum Duty Cycle	CAO = 0.6V	90	95	100	%
Modulator Gain	CAO = 2.5V, 3.2V	63	71	80	%/V
OSC Peak			3		V
OSC Valley			1		V
Oscillator Section					
Frequency	8.8V < VCC < 35V	198	220	242	kHz
Thermistor Derived Reference Section	V_{ID} = V_{RTHM} – V_{R10}				
Initial Accuracy, VAO (RTHM = 10k)	V_{ID} = 0, R10 = RTHM =10k (Note 3)	2.2655	2.3	2.3345	V
	V_{ID} = 0, R10 = RTHM =10k, –40°C ≤T_A < 0°C (Note 3)	2.254	2.3	2.346	V
Line Regulation	V_{CC} = 8.8V to 35V		3	10	mV
VAO	RTHM = 138k, R10 = 10k	2.458	2.495	2.532	V
	RTHM = 138k, R10 = 10k, -40°C ≤ T_A < 0°C	2.445	2.495	2.545	V
	RTHM = 33.63k, R10 = 10k	2.362	2.398	2.434	V
	RTHM = 33.63k, R10 = 10k, -40°C ≤ T_A < 0°C	2.350	2.398	2.446	V
	RTHM = 1.014k, R10 = 10k	2.035	2.066	2.097	V
	RTHM = 1.014k, R10 = 10k, -40°C ≤ T_A < 0°C	2.025	2.066	2.107	V
Charge Enable Comparator Section (CEC)					
Threshold Voltage	As a function of VA–	0.99	1	1.01	V/V
Input Bias Current	CHGENB = 2.3V	–0.5	–0.1		µA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –40°C to +85°C for UC2909; °0C to +70°C for UC3909; C_T = 330pF, R_{SET} = 11.5k, R10 = 10k, R_{THM} = 10k, V_{CC} = 15V, Output no load, R_{STAT0} = R_{STAT1} = 10k, CHGENB = OVCTAP = VLOGIC, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Sense Comparator Section (VSC)					
Threshold Voltage	STAT0 = 0, STAT1 = 0, Function of V_{REF}	0.945	0.95	0.955	V/V
	STAT0 = 1, STAT1 = 0, Function of V_{REF}	0.895	0.9	0.905	V/V
Over Charge Taper Current Comparator Section (OCTIC)					
Threshold Voltage	Function of 2.3V REF, CA- = CAO	0.99	1	1.01	V/V
Input Bias Current	OVCTAP = 2.3V	–0.5	–0.1		µA
Logic 5V Reference Section (VLOGIC)					
VLOGIC	VCC = 15V	4.875	5.0	5.125	V
Line Regulation	8.8V < V_{CC} < 35V		3	15	mV
Load Regulation	0 < I_O < 10mA		3	15	mV
Reference Comparator Turn-on Threshold			4.3	4.8	V
Short Circuit Current	V_{REF} = 0V	30	50	80	mA
Output Stage Section					
I_{SINK} Continuous			50		mA
I_{PEAK}			100		mA
V_{OL}	I_O=50mA		1	1.3	V
Leakage Current	V_{OUT}=35V			25	µA
STAT0 & STAT1 Open Collector Outputs Section					
Maximum Sink Current	V_{OUT} = 8.8V	6	10		mA
Saturation Voltage	I_{OUT} = 5mA		0.1	0.45	V
Leakage Current	V_{OUT} = 35V			25	µA
STATLV Open Collector Outputs Section					
Maximum Sink Current	V_{OUT} = 5V	2.5	5		mA
Saturation Voltage	I_{OUT} = 2mA		0.1	0.45	V
Leakage current	V_{OUT} = 5V			3	µA
UVLO Section					
Turn-on Threshold		6.8	7.8	8.8	V
Hysteresis		100	300	500	mV
I_{CC} Section					
I_{CC} (run)	(See Fig. 1)		13	19	mA
I_{CC} (off)	VCC = 6.5V		2		mA

Note 2: *VIO is measured prior to packaging with internal probe pad.*
Note 3: *Thermistor initial accuracy is measured and trimmed with respect to VAO; VAO = VA–.*

PIN DESCRIPTIONS

CA–: The inverting input to the current error amplifier.

CAO: The output of the current error amplifier which is internally clamped to approximately 4V. It is internally connected to the inverting input of the PWM comparator.

CS–, CS+: The inverting and non-inverting inputs to the current sense amplifier. This amplifier has a fixed gain of five and a common-mode voltage range of from –250mV to +VCC.

CSO: The output of the current sense amplifier which is internally clamped to approximately 5.7V.

CHGENB: The input to a comparator that detects when battery voltage is low and places the charger in a trickle charge state. The charge enable comparator makes the output of the voltage error amplifier a high impedance while forcing a fixed 10µA into CA– to set the trickle charge current.

PIN DESCRIPTIONS (cont.)

GND: The reference point for the internal reference, all thresholds, and the return for the remainder of the device. The output sink transistor is wired directly to this pin.

OVCTAP: The overcharge current taper pin detects when the output current has tapered to the float threshold in the overcharge state.

OSC: The oscillator ramp pin which has a capacitor (C_T) to ground. The ramp oscillates between approximately 1.0V to 3.0V and the frequency is approximated by:

$$frequency = \frac{1}{1.2 \bullet C_T \bullet R_{SET}}$$

OUT: The output of the PWM driver which consists of an open collector output transistor with 100mA sink capability.

R10: Input used to establish a differential voltage corresponding to the temperature of the thermistor. Connect a 10k resistor to ground from this point.

RSET: A resistor to ground programs the oscillator charge current and the trickle control current for the oscillator ramp.

The oscillator charge current is approximately $\frac{1.75}{R_{SET}}$.

The trickle control current ($I_{TRCK\_CONTROL}$) is approximately $\frac{0.115}{R_{SET}}$.

RTHM: A 10k thermistor is connected to ground and is thermally connected to the battery. The resistance will vary exponentially over temperature and its change is used to vary the internal 2.3V reference by –3.9mV/°C. The recommended thermistor for this function is part number L1005-5744-103-D1, Keystone Carbon Company, St. Marys, PA.

STAT0: This open collector pin is the first decode bit used to decode the charge states.

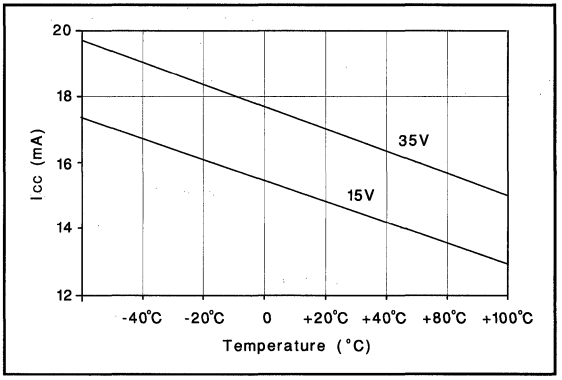


Figure 1. I_{CC} vs. temperature.

STAT1: This open collector pin is the second decode bit used to decode the charge states.

STATLV: This bit is high when the charger is in the float state.

VA–: The inverting input to the voltage error amplifier.

VAO: The output of the voltage error amplifier. The upper output clamp voltage of this amplifier is 5V.

VCC: The input voltage to the chip. The chip is operational between 7.5V and 40V and should be bypassed with a 1µF capacitor. A typical I_{CC} vs. temperature is shown in Figure 1.

VLOGIC: The precision reference voltage. It should be bypassed with a 0.1µF capacitor.

Charge State Decode Chart

STAT0 and STAT1 are open collector outputs. The output is approximately 0.2V for a logic 0.

	STAT1	STAT0
Trickle Charge	0	0
Bulk Charge	0	1
Over Charge	1	0
Float Charge	1	1

APPLICATION INFORMATION

A Block Diagram of the UC3909 is shown on the first page, while a Typical Application Circuit is shown in Figure 2. The circuit in Figure 2 requires a DC input voltage between 12V and 40V.

The UC3909 uses a voltage control loop with average current limiting to precisely control the charge rate of a lead-acid battery. The small increase in complexity of average current limiting is offset by the relative simplicity of the control loop design.

CONTROL LOOP

Current Sense Amplifier

This amplifier measures the voltage across the sense resistor RS with a fixed gain of five and an offset voltage of 2.3V. This voltage is proportional to the battery current. The most positive voltage end of RS is connected to CS- ensuring the correct polarity going into the PWM comparator.

CSO = 2.3V when there is zero battery current.

RS is chosen by dividing 350mV by the maximum allowable load current. A smaller value for RS can be chosen to reduce power dissipation.

Maximum Charge Current, Ibulk, is set by knowing the maximum voltage error amplifier output, V_{OH} = 5V, the maximum allowable drop across RS, and setting the resistors RG1 and RG2 such that;

$$\frac{RG1}{RG2} = \frac{5 \bullet V_{RS}}{VLOGIC - CA-} = \frac{5 \bullet V_{RS}}{5V - 2.3V} = \frac{5 \bullet V_{RS}}{2.7V} = 1.852 \bullet I_{BULK} \bullet RS \quad (1)$$

The maximum allowable drop across RS is specified to limit the maximum swing at CSO to approximately 2.0V to keep the CSO amplifier output from saturating.

No charge/load current: V_{CSO} = 2.3V,

Max charge/load current: $V_{max(CSO)}$ = 2.3V–2.0V = 0.3V

Voltage Error Amplifier:

The voltage error amplifier (VEA) senses the battery

voltage and compares it to the 2.3V – 3.9mV/°C thermistor generated reference. Its output becomes the current command signal and is summed with the current sense amplifier output. A 5.0V voltage error amplifier upper clamp limits maximum load current. During the trickle charge state, the voltage amplifier output is opened (high impedance output) by the charge enable comparator. A trickle bias current is summed into the CA– input which sets the maximum trickle charge current.

The VEA, V_{OH} = 5V clamp saturates the voltage loop and consequently limits the charge current as stated in Equation 1.

During the trickle bias state the maximum allowable charge current (ITC) is similarly determined:

$$ITC = \frac{I_{TRICK\_CONTROL} \bullet RG1}{RS \bullet 5} \quad (2)$$

$I_{TRCK\_CONTROL}$ is the fixed control current into CA–. $I_{TRCK\_CONTROL}$ is 10µA when R_{SET} = 11.5k. See RSET pin description for equation.

Current Error Amplifier

The current error amplifier (CA) compares the output of the current sense amplifier to the output of the voltage error amplifier. The output of the CA forces a PWM duty cycle which results in the correct average battery current. With integral compensation, the CA will have a very high DC current gain, resulting in effectively no average DC current error. For stability purposes, the high frequency gain of the CA must be designed such that the magnitude of the down slope of the CA output signal is less than or equal to the magnitude of the up slope of the PWM ramp.

CHARGE ALGORITHM

Refer to Figure 3 in UC3906 Data Sheet in the data book.

A) Trickle Charge State
STAT0 = STAT1 = STATLV = logic 0

When CHGNB is less than VREF (2.3V – 3.9mV/°C), STATLV is forced low. This decreases the sense voltage divider ratio, forcing the battery to overcharge (VOC).

$$VOC = (VREF) \bullet \frac{(RS1 + RS2 + RS3 \,||\, RS4)}{(RS3 \,||\, RS4)} \quad (3)$$

During the trickle charge state, the output of the voltage error amplifier is high impedance. The trickle control current is directed into the CA– pin setting the maximum trickle charge current. The trickle charge current is defined in Equation 2.

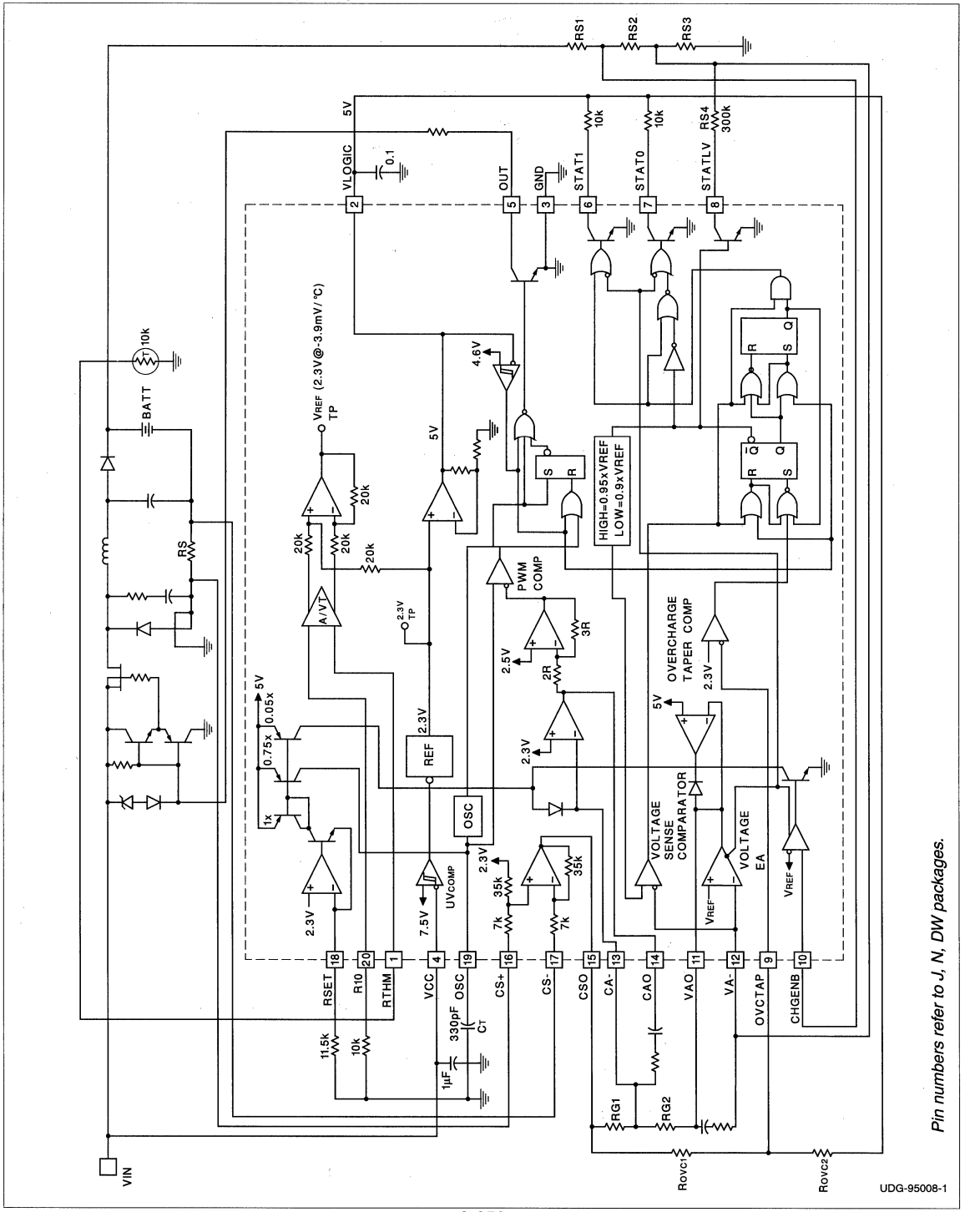
B) Bulk Charge State
STAT1 = STATLV = logic 0, STAT0 = logic 1

As the battery charges, the UC3909 will transition from trickle to bulk charge when CHGENB becomes greater than 2.3V. The transition equation is

$$VT = VREF \bullet \frac{(RS1 + RS2 + RS3 || RS4)}{(RS2 + RS3 || RS4)} \quad (4)$$

STATLV is still driven low.

APPLICATION INFORMATION (cont.)



Pin numbers refer to J, N, DW packages.

Figure 2. Typical application circuit

APPLICATION INFORMATION (cont.)

During the bulk charge state, the voltage error amplifier is now operational and is commanding maximum charge current (I_{BULK}) set by Equation 1. The voltage loop attempts to force the battery to VOC.

C) Overcharge State

STAT0 = STATLV = logic 0, STAT1 = logic 1

The battery voltage surpasses 95% of VOC indicating the UC3909 is in its overcharge state.

During the overcharge charge state, the voltage loop becomes stable and the charge current begins to taper off. As the charge current tapers off, the voltage at CSO increases toward its null point of 2.3V. The center connection of the two resistors between CSO and VLOGIC sets the overcurrent taper threshold (OVCTAP). Knowing the desired overcharge terminate current (I_{OCT}), the resistors R_{OVC1} and R_{OVC2} can be calculated by choosing a value of R_{OVC2} and using the following equation:

$$R_{OVC1} = (18518) \bullet I_{OCT} \bullet RS \bullet R_{OVC2} \quad (5)$$

D) Float State

STAT0 = STAT1 = STATLV = logic 1

The battery charge current tapers below its OVCTAP threshold, and forces STATLV high increasing the voltage sense divider ratio. The voltage loop now forces the battery charger to regulate at its float state voltage (V_F).

$$V_F = (V_{REF}) \frac{(RS1 + RS2 + RS3)}{RS3} \quad (6)$$

If the load drains the battery to less than 90% of V_F, the charger goes back to the bulk charge state, STATE 1.

OFF LINE APPLICATIONS

For off line charge applications, either Figure 3 or Figure 4 can be used as a baseline. Figure 3 has the advantage of high frequency operation resulting in a small isolation transformer. Figure 4 is a simpler design, but at the expense of larger magnetics.

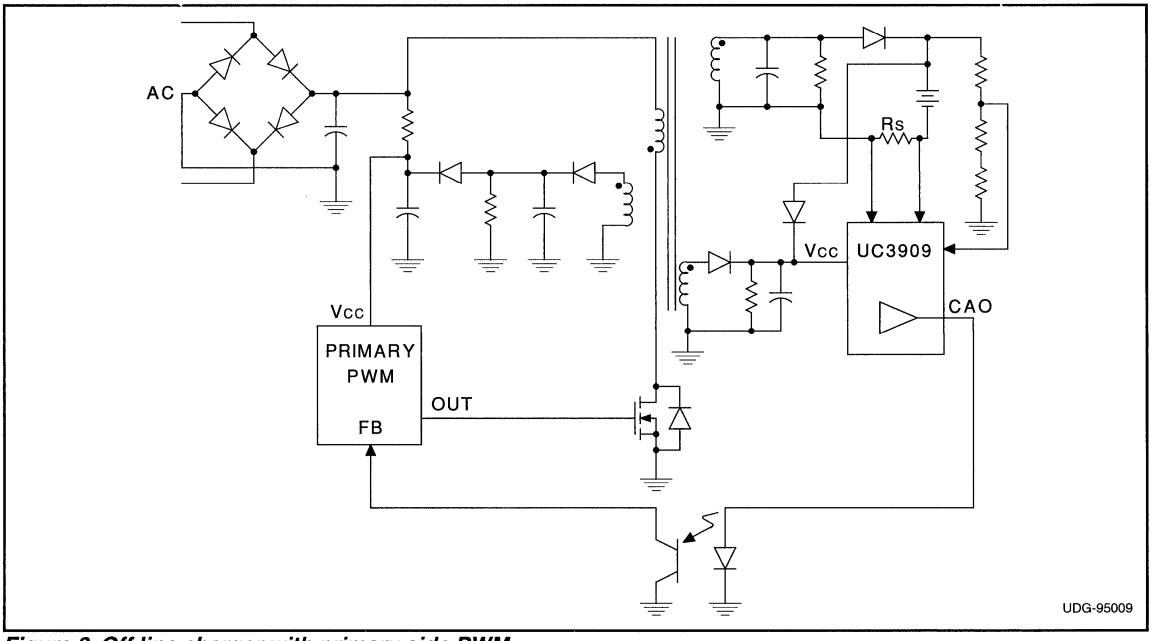


Figure 3. Off line charger with primary side PWM

APPLICATION INFORMATION (cont.)

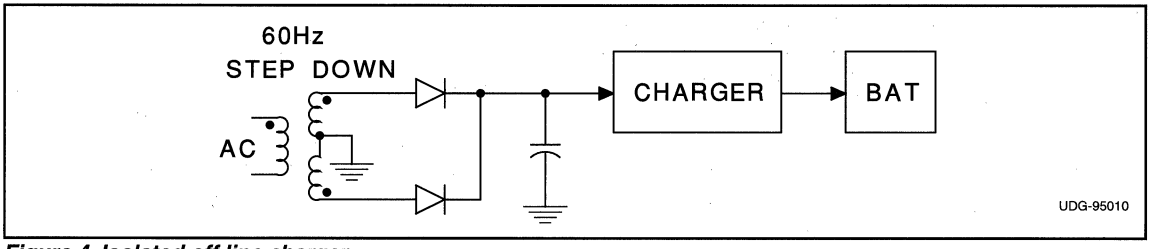


Figure 4. Isolated off line charger

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

Switch Mode Lithium-Ion Battery Charger Controller

PRELIMINARY

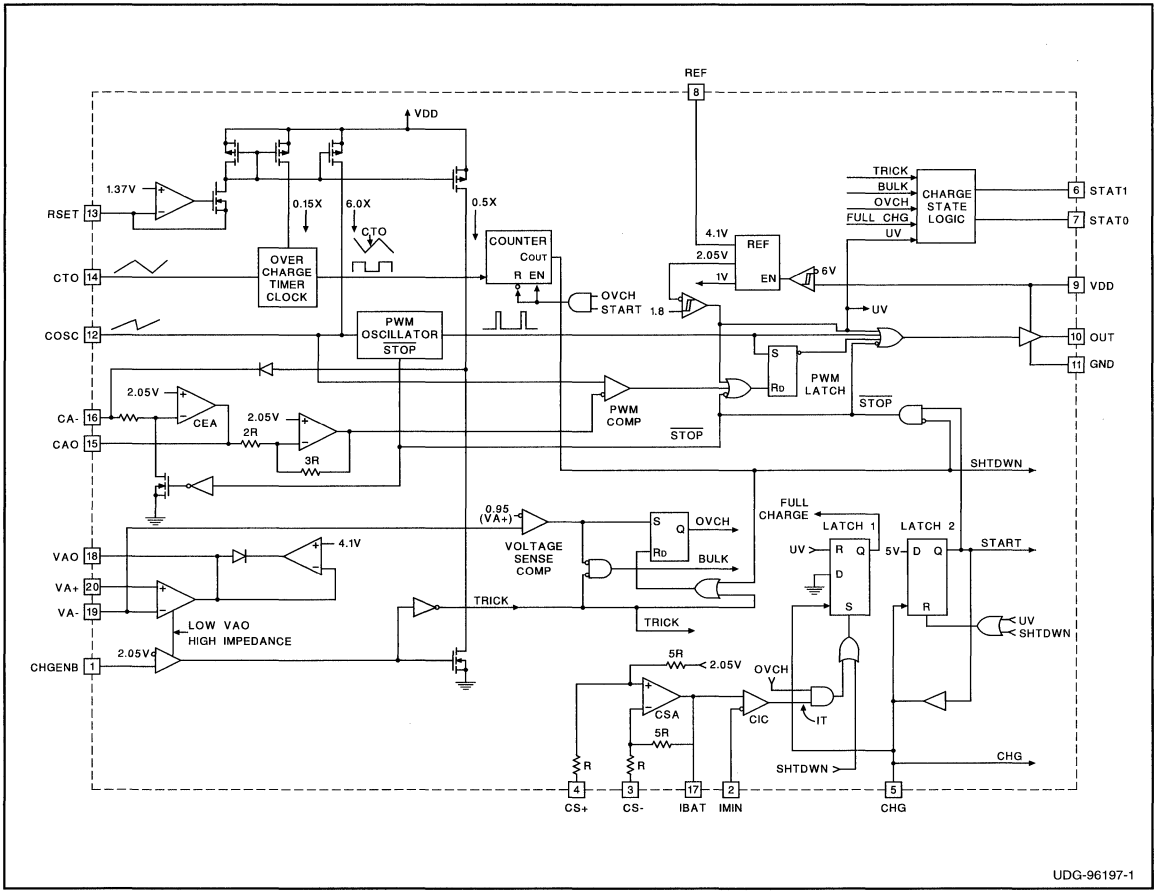
FEATURES

- Precision 4.1V Reference (1%)
- High Efficiency Battery Charger Solution
- Average Current Mode Control from Trickle to Over Charge
- Resistor Programmable Charge Currents
- Internal State Logic Provides Four Charge States
- Programmable Over Charge Time
- Fully Differential Switch Mode Current Sensing
- CHG Pin Initiates Charging

DESCRIPTION

The UCC3956 family of Switch Mode Lithium-Ion Battery Charger Controllers accurately control lithium-ion battery charging with a highly efficient average current control loop. This chip is designed to work as a stand alone charger controller for a single cell or multiple cell battery pack. This chip combines charge state logic and average current PWM control circuitry with a 14 bit counter to program the over charge time. The charge state logic indicates current or voltage control depending on the charge state. The chip includes undervoltage lockout circuitry to insure sufficient supply voltage is present before output switching starts. Additional circuit blocks include a differential current sense amplifier, a 1% voltage reference, voltage and current error amplifiers, PWM latch, charge state decode bits, and a 500mA output driver.

BLOCK DIAGRAM



UDG-96197-1

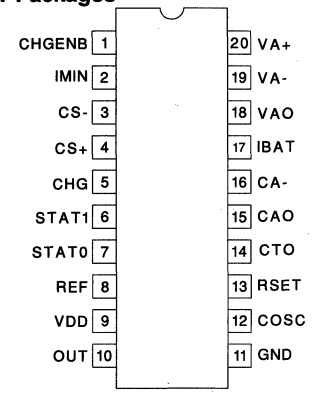
ABSOLUTE MAXIMUM RATINGS

Supply Voltage VDD, OUT 20V
Output Current Sink
  Continuous 120mA
  Peak 600mA
Output Current Source
  Continuous 120mA
  Peak 600mA
CS+, CS–
  Voltage . . . . . –0.5 to VDD
  Current with CS+, CS– less than –0.5. . . . . 50mA
Remaining Pin Voltages . . . . . –0.3V to 6V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature. . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIP-20, SOIC-20 (Top View)
J or N, DW Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = –40°C to +85 for UCC2956 and 0°C to +70°C for UCC3956, COSC = 500pF, RSET = 70k, CTO = 169nF, VDD = 12V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Sense Amplifier (CSA)					
DC Gain	CS– = 0, CS+ = –50mV and CS+ = –250mV	4.9	5	5.1	V/V
	CS+ = 0, CS– = 50mV and CS– = 250mV	4.9	5	5.1	V/V
CAO	CS+ = CS– = 0V	1.99	2.05	2.11	mV
CMRR	V_{CM} = 1.1V to 18V, VDD = 18V	50	65		dB
V_{OL}	CS+ = –0.2V, CS– = 0.5V, IO = 1mA		0.3		V
V_{OH}	CS+ = 0.5V, CS– = –0.2V, IO = –500µA	3.7	4.1	4.4	V
Output Source Current	IBAT = 3V, VID = 700mV	–500			µA
Output Sink Current	IBAT = 1V, VID = –700mV	500			µA
3dB Bandwidth	V_{CM} = 0V, CS+ - CS– = 100mV (Note 2)	0.1	3		MHz
Current Error Amplifier (CEA)					
IB	8V < V_{DD}< 18V, CHGENB = REF		0.1	0.5	µA
CA– Voltage	8V < V_{DD} < 18V, CAO = CA–	1.99	2.05	2.11	V
AVO		60	90		dB
GBW	T_J = 25°C, F = 100kHz	1	3		MHz
V_{OL}	IO = 250µA, CA– = 3V		0.5		V
V_{OH}	IO = –1mA, CA– = 2V	3.7	4.1	4.4	V
$I_{CA–}$, Itrck_control	V_{CHGENB} = GND	8	10	12	µA
Voltage Error Amplifier (VEA)					
IB	Total Bias Current; Regulating Level		0.5	3	µA
VIO	8V < V_{DD} < 18V, –0.2 < VCM < 5V			10	mV
AVO		60	90		dB
GBW	T_J = 25°C, F = 100kHz	0.75	3		MHz
V_{OL}	IO = 500µA, VA– = 3.8V		0.2	1	V
V_{OH}	IO = –500µA, VA– = 4.4V	3.8	4.1	4.3	V
VAO Leakage	V_{CHGENB} = GND, STAT0 = 0 and STAT1 = 0, VAO = 2.05V	–1		1	µA
Pulse Width Modulator					
Maximum Duty Cycle	CAO = 0.5V	85	92	100	%
Modulator Gain	CAO = 1.7V, 2.1V	57	64	71	%/V

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = –40°C to +85 for UCC2956 and 0°C to +70°C for UCC3956, COSC = 500pF, RSET = 70k, CTO = 169nF, VDD = 12V, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM Oscillator (OSC)					
Frequency	7V < V_{DD} < 18V	90	100	110	kHz
Over Charge Timer (OCT)					
Frequency	7V < V_{DD} < 18V (Note 1)	4.65	5	5.35	Hz
Reference					
Initial Accuracy	T_J = 25°C	4.06	4.1	4.14	V
Accuracy	0 < T_J < 70°C, V_{DD} = 8V to 18V	4.05	4.1	4.15	V
Load Regulation	0 < I_O < 2mA		3	15	mV
Accuracy	–40°C < T_J < 85°C, V_{DD} = 8V to 18V	4.03	4.1	4.17	V
Short Circuit I	REF = 0V	8	20	30	mA
Charge Enable Comparator (CEC)					
Threshold Voltage		1.9	2.05	2.15	V
Input Bias Current		–0.5	–0.2		µA
Voltage Sense Comparator (VSC)					
Threshold Voltage	Volts below VA+	50	125	200	mV
Charge Current Comparator (CIC)					
Threshold Voltage	CS+ = CS– = 0, Function of IBAT = 2.05V	2	2.05	2.1	V/V
Input Bias Current	Total Bias Current; Regulating Level	–0.5	–0.2		µA
Output Stage					
V_{OL}	I_O = 10mA		0.1	0.3	V
V_{OH}, Volts Below VDD	I_O = –10mA		0.1	0.5	V
Rise Time	C_{OUT} = 1nF		30	70	ns
Fall Time	C_{OUT} = 1nF		30	70	ns
STAT0 and STAT1 Open Drain Outputs					
Maximum Sink Current	V_{OUT} = 12V	15	30		mA
V_{OL}	I_{OUT} = 1mA		0.1	0.2	V
Charge Control (CHG)					
Threshold Voltage		1.5	1.8	2.1	V
Charge Pin Pull Down Resistance			3.0	5.0	kΩ
UVLO Section					
Turn-on Threshold		6.0	6.5	6.75	V
Hysteresis		100	150	400	mV
IDD					
IDD (Run)			5	8	mA
IDD (UVLO)	V_{DD} = 5V		0.25	0.75	mA

PIN DESCRIPTIONS

CA–: The inverting input to the current error amplifier.

CAO: The output of the current error amplifier and inverting input of the PWM comparator. This pin is driven high during shutdown.

CS–, CS+: The inverting and non-inverting inputs to the current sense amplifier. This amplifier has a fixed gain of 5.

CHG: A rising edge triggered input pin that indicates charging. Once the internal 14 bit timer has timed out the chip enters its shutdown charge state. At this point CHG is pulled low by an internal buffer. Another low to high transition is required to reset the timer and restart charging.

CHGENB: The input to a comparator that detects when the battery voltage is low and places the charger in trickle charge. The charge enable comparator forces the output of the voltage error amplifier to a high impedance state while forcing a fixed 10µA current into the CA– to set the trickle charge.

COSC: The oscillator ramp pin which has a capacitor (COSC) to ground. The ramp oscillates between 0.8V to 3.2V and the frequency is determined by:

PIN DESCRIPTIONS (cont.)

$$\text{Frequency} = \frac{3.475}{(\text{COSC} + 20\text{pF}) \bullet \text{RSET}}$$

A rising edge on CHG initiates the oscillator.

CTO: The slow oscillator ramp pin which is used to generate a clock signal for the 14 bit timer to program the over charge time. A capacitor to ground is charged and discharged with equal currents at a frequency programmed between 0.75Hz to 5Hz. The ramp oscillates between 1.0V to 3.0V and the frequency is determined by:

$$\text{Frequency} = \frac{0.06}{\text{CTO} \bullet \text{RSET}}$$

The oscillator operates only while in overcharge.

GND: The reference point for the internal reference, all thresholds, and the return for the remainder of the device.

IBAT: The output of the current sense amplifier.

IMIN: The minimum charge current programming pin is provided to program an optional charge termination in addition to the programmable timer.

OUT: The output of the PWM driver.

REF: The 4.1V precision reference which should be bypassed with a 0.1µF capacitor.

RSET: This pin programs the charge current for the oscillator ramp. The oscillator charge current is determined by:

$$\frac{1.37\text{V}}{\text{RSET}}.$$

The trickle control current (Itrck_control) is determined by:

$$\frac{0.68\text{V}}{\text{RSET}}.$$

STAT0, STAT1: CMOS open drain binary output decode pins indicating the four different charge states. The maximum high voltage sense comparator.

VA–: The inverting input to the voltage error amplifier that is used as a battery sense input. It is also the input to the voltage sense comparator. The bulk charge state is completed and over charge state is initiated when VA– reaches 95% of VA+.

VA+: The non-inverting input to the voltage error amplifier that is used as the battery charge reference voltage.

VAO: The output of the voltage error amplifier. The upper output clamp of this amplifier is 4.1V.

VDD: The input voltage of the chip. This chip is operational between 6V and 18V and should be bypassed with a 0.1µF capacitor.

CHARGE STATE DECODE CHART

	STAT1	STAT0	
Trickle Charge	0	0	CHGENB < 2.05V
Bulk Charge	0	1	VA– < 95% VA+ and CHGENB > 2.05V
Over Charge	1	0	VA– > 95% VA+ and VIBAT< VIMIN
Over Charge (Top Off)	1	1	VIBAT > VIMIN

APPLICATION INFORMATION

The UCC3956 contains all the necessary control functions for implementing an efficient switch mode Lithium-Ion battery charger. Lithium-Ion batteries are rapidly becoming the battery of choice for rechargeable portable and lap top products. When compared to NiCd, NiMH, and Lead Acid batteries, Lithium-Ion offer less weight and volume for the same energy. Lithium-Ion batteries do not suffer from the memory effect found in NiCd batteries. This effect, caused by not completely discharging and charging a battery, will reduce battery capacity over several charge cycles. Because Lithium-Ion batteries have a high average cell voltage of around 3.6V, they can often replace 2 to 3 Nickel based cells.

The advantages that Lithium-Ion batteries offer come at the cost of a wide operating voltage. Near zero capacity, the cell will typically have a voltage of 2.5V. A fully charged cell will typically have a voltage of 4.1V. Unlike many so called "smart" or "universal" chargers, the UCC3956 is optimized for Lithium-Ion characteristics. In order to restore capacity quickly, the chip features both constant current and constant voltage modes of operation. A programmable over charge time, provided by the UCC3956 timer, allows the charger to predictably restore 100% capacity to the battery.

Charger Operation

When CHG is transitioned from a low to high logic level, the chip will cycle through several charge states. If the battery voltage is severely depleted, the charger will begin in a low current trickle charge state. When the bat-

APPLICATION INFORMATION (cont.)

tery voltage is above a user set threshold, the charger will initiate a constant current bulk charge state. Once the battery reaches 95% of it's final voltage, the charger will enter an over charge state. During the over charge state, the converter will transition from a constant current to a constant voltage mode of operation. Figure 2 shows typical current, voltage, and capacity levels of a Lithium-Ion battery during a complete charge cycle.

A Block Diagram of the UCC3956 is shown on the first page of the data sheet, while Figure 1 shows a typical application circuit for a Buck derived switch mode charger. The UCC3956 can be used for charging a single cell or multiple cells in series. If more than two cells are stacked in series, however, a level shifting gate drive will be needed to operate the buck switch. The application circuit charges a 1200mAh 2 cell stack at a 1C rate.

Setting the Oscillator Frequency

The frequency of operation for the converter is set by picking values for RSET and COSC.

$$fOSC = \frac{3.475}{(COSC + 20pF) \bullet RSET}$$

The UCC3956 is capable of operating at frequencies higher than 200kHz. However, the actual operating frequency of the buck converter will ultimately be determined by the usual tradeoffs of size, cost and efficiency. The application circuit frequency is set at 100kHz with COSC = 180pF and RSET = 162k.

Trickle Charge State

When the battery's voltage is below a predetermined threshold, the battery is either deeply discharged or has shorted cells. The trickle charge state offers a low charging current to bring the battery up above zero capacity. In the case of shorted cells, the trickle charge state prevents the charger from delivering high currents during this fault condition. Stacking several cells makes the detection of a shorted cell more difficult.

For Lithium-Ion batteries, the trickle charge threshold is typically set to a value around 2.5V per cell (this corresponds to near zero capacity). When the cell voltage is below the threshold, only a trickle current will be applied to the battery. The threshold is established by programming CHGENB to 2.05V when the battery (or stack) voltage is at the threshold. Referring to the application circuit

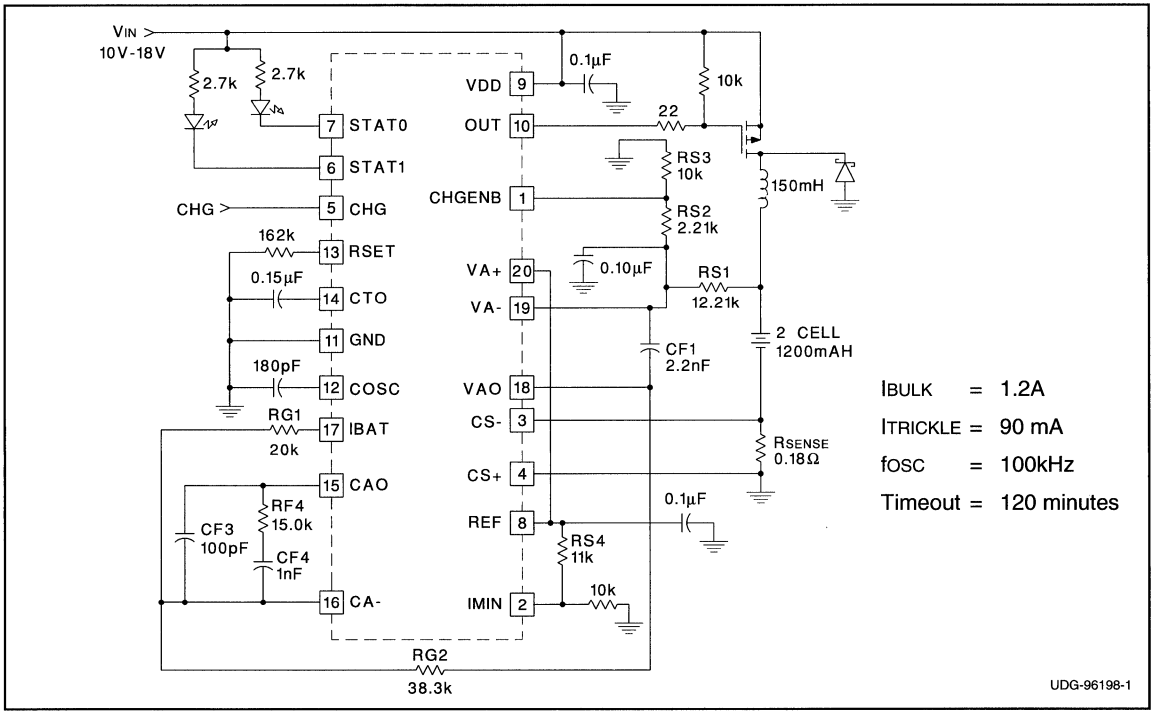


Figure 1. Typical Application Circuit

APPLICATION INFORMATION (cont.)

of Figure 1, the trickle charge voltage threshold is determined by:

$$VTRICKLE\_THRESHOLD = \frac{RS1 + RS2 + RS3}{RS3} \bullet 2.05$$

With a trickle threshold of 5V (for 2 cells) and setting RS3 to 10k, RS1+ RS2 should be approximately 14.4k.

The applications circuit trickle charge current is set to about 7.5% of the bulk charge current. The current value is set by picking the appropriate value for RG1. Referring to the Block Diagram and Figure 1, during trickle charge a fixed current

$$\frac{0.68}{RSET}$$

flows out of the current amplifier's inverting input and into RG1. The voltage amplifier output is disabled during trickle charge and acts as a high impedance node. The resulting voltage at the output of the current sense amplifier sets the trickle charge current.

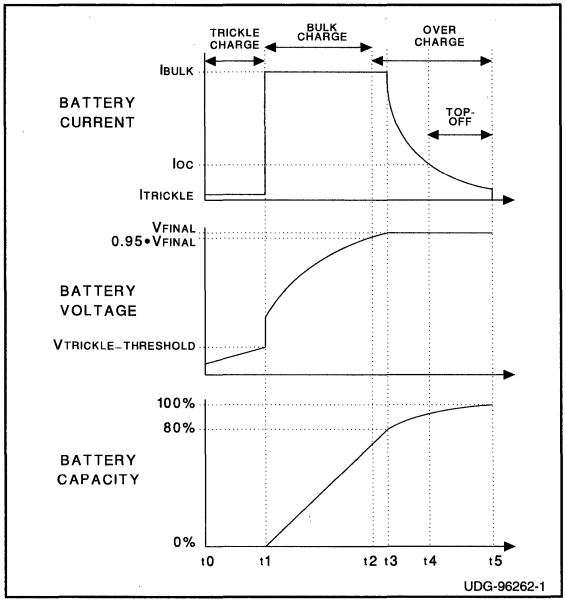


Figure 2. Typical Charge Cycle Levels

$$ITRICKLE = \frac{RG1}{7.5 \bullet RSET \bullet RSENSE}$$

In the application circuit the sense resistor is 0.18Ω and RSET is 162k, for a trickle current of about 90mA a 20k resistor is selected for RG1.

The converter is typically designed to run in discontinuous conduction mode during trickle charge. This allows a reasonably small value of inductance to be used. The average current mode of the UCC3956 provides improved discontinuous duty cycle control, when compared to peak current mode implementations.

In Figure 2, the trickle charge state corresponds to the time interval between t0 (when CHG is transitioned from low to high) and t1. During the trickle charge state STAT0 and STAT1 are logic level lows. At time t1 the trickle threshold is met, and the charger transitions to the bulk charge state. In many instances, the battery voltage will initially be above the trickle threshold. In this case, the trickle charge state will not be needed.

Bulk Charge State

As the name implies, the bulk charge state is responsible for restoring a majority of the charge back into the battery. The bulk charge current is determined by the C rate and the capacity of the battery. In the application circuit, 2 stacked 1200mAH batteries are charged at a 1C rate. This will require 1.2A of current during bulk charge. In this case, a fully discharged battery will take about 60 minutes to reach approximately 80% capacity. Battery packs with a high ESR will typically have a shorter bulk period, due to the voltage drop generated by the bulk current and the ESR of the battery.

Both the voltage and current sense amplifiers are enabled during bulk charge. The voltage amplifier is saturated in this state as the battery voltage is slowly rising, but is not yet high enough to drive the voltage amplifier into regulation. The output of voltage amplifier is clamped at a nominal voltage of 4.1V. The current sense amplifier is configured such that its output voltage increases with decreasing RSENSE current. RSENSE should be sized such that the output voltage of the current sense amplifier VIBAT is within specification during bulk charge.

$$VIBAT(BULK) = 2.05 - 5 \bullet IBULK \bullet RSENSE$$

With 1.2A of bulk current and setting the current sense amplifier output at 1V, a sense resistor of 0.18Ω is required. As always, power dissipation and converter efficiency must be considered when choosing RSENSE.

Referring to the Feedback Diagram of Figure 3, the output of the voltage and current sense amplifiers are summed together at the inverting input of the current amplifier. Assuming that the current amplifier is within regulation, the required value of RG2 can be calculated. The application circuit uses a value of 38.3k for RG2, setting the bulk current to 1.2A.

$$RG2 = \frac{2.05 \bullet RG1}{5 \bullet IBULK \bullet RSENSE}$$

Referring to Figure 2, the bulk charge state corresponds

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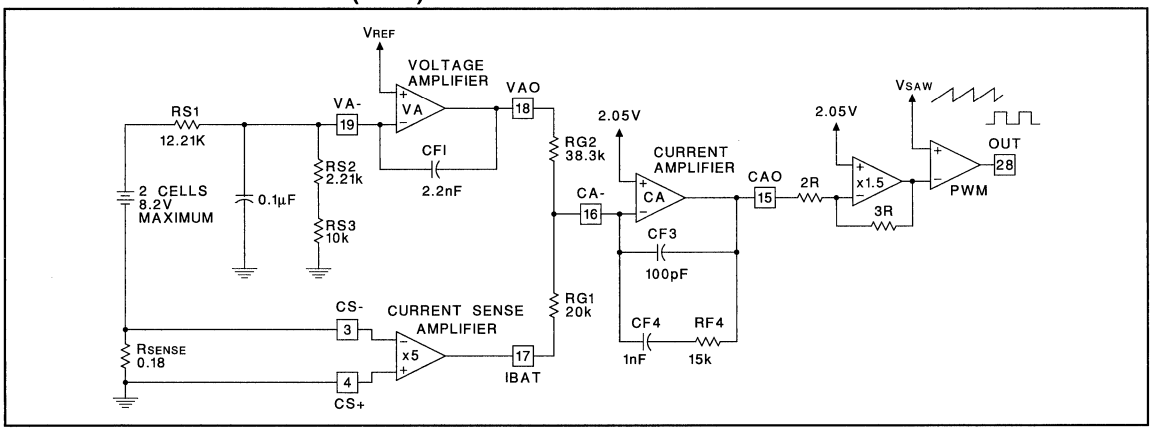

Figure 3. Simplified Feedback Diagram

UDG-96263-1

to the interval between t1 and t2. The step in voltage at time t1 is caused by bulk current flowing into the battery ESR and sense resistor. In the bulk charge state STAT0 is a logic level high and STAT1 is a logic level low.

Over Charge State

The over charge state of the converter starts when the battery reaches 95% of its final voltage (time t2 of Figure 2). The over charge state is initiated when the voltage at the inverting input of the voltage amplifier is 95% of the non-inverting input voltage. Using 95% rather than 100% of the final battery voltage assures that the over charge timer will always be set, before the battery current tapers off. At the beginning of over charge STAT0 indicates a logic level low and STAT1 indicates a logic level high.

In the application circuit of Figure 1, the voltage at which over charge is initiated is set by resistors RS1, RS2 and RS3. These resistors are also used to set the trickle charge threshold. A 0.1µF decoupling capacitor is added to this node as a filter. The battery (or stack) voltage that will initiate the over charge state is:

$$VOC\_THRESHOLD = 0.95 \bullet \frac{RS1 + RS2 + RS3}{RS2 + RS3} \bullet 4.1$$

For a single cell stack, RS1 should be 0Ω. This results in a final battery voltage of 4.1V. It is important not to charge a Lithium-Ion battery above 4.2V. When charging a battery stack, RS1 should be selected to properly set the final stack voltage. In the application circuit, RS1 is selected to be 12.21k and RS2 is selected to be 2.21k. This sets the over charge level at 8.2V, while setting the trickle charge threshold to about 5V.

The battery voltage at the beginning of the over charge state may not correspond to the voltage amplifier coming out of saturation. Therefore, bulk current may continue in the battery during the initial portion of the over charge state (see Figure 2). When the voltage amplifier comes into regulation, the amplifier's output voltage will begin to decrease. The current sense amplifier's output voltage will need to increase, in order for the current amplifier's inverting input to remain at 2.05V. This will translate into a decreasing battery current. The battery current will continue to decrease as the battery approaches 100% capacity.

Although the bulk charge state restores a majority of the capacity to the battery, the over charge state will typically take a majority of the charge cycle time. The bulk charge state will usually take 1/3 of the total charge time, while the over charge state will take the remaining 2/3. Different methods are used to terminate the charge of Lithium-Ion batteries. Many chargers use a current threshold to terminate charge. While this method is simple to implement, the current tail near the end of charge is often quite flat (see Figure 2). To make matters worse, the current level versus battery capacity may differ from cell to cell. This makes it difficult to accurately terminate at 100% capacity. In order to avoid the possibility of over charging the battery, the design may require termination at a higher current level (before 100% capacity is reached). A more predictable method of charge termination is to use a fixed over charge time.

The UCC3956 provides both a current level detection as well as a timer. In a typical design, the current level detection is used to give an indication of near full charge. In Figure 2 this occurs at time t4. This indication is useful since the time to charge from t4 to t5 may be quite long. Since Lithium-Ion batteries have no memory effect, there is little reason to have the user wait for the battery to be

APPLICATION INFORMATION (cont.)

100% charged. If the battery is not taken from the charger at time t4, the charger will continue charging. The timer will expire and the charge cycle will terminate at time t5.

A typical value of current used to indicate near full charge is 1/10 of the bulk current value. This current level is established by setting the appropriate voltage on IMIN. IMIN is tied to an internal comparator along with the output of the current sense amplifier. When the current sense amplifier voltage becomes greater than the voltage on IMIN, the internal state machine indicates near full charge by setting STAT0 and STAT1 to logic level highs. In the application circuit of Figure 1, resistors RS4 and RS5 determine the voltage at IMIN. With RS4 at 11k and RS5 at 10k, near full charge is indicated at 120mA.

$$VIMIN = 4.1 \bullet \frac{RS5}{RS4 + RS5}$$

$$INEAR\_FULL = \frac{2.05 - VIMIN}{5 \bullet RSENSE}$$

The UCC3956 timer has a 14 bit counter that allows long over-charge times with reasonable component values. As stated above, the charger will continue charging the battery until the timer expires (unless the battery is pulled from the charger). Referring to Figure 2, the timer starts at time t2 and expires at time t5. The frequency of the timer can be determined as follows:

$$fTIMER = \frac{0.06}{RSET \bullet CTO}$$

With a 14 bit counter the time-out period in minutes becomes:

$$TIMEOUT = 4550 \bullet CTO \bullet RSET$$

In the application circuit, a value of 0.15µF is used for CTO to give 120 minutes of overcharge (more than twice the bulk charge time). When the timer expires, CHG is pulled low by an internal buffer and the charge cycle terminates. If tied to a bi-directional port, CHG can be read by a microprocessor.

Inductor Sizing

For good efficiency, the inductor should be sized to give continuous current in the bulk charge state. For a buck converter, duty cycle in continuous mode is given by:

$$D = \frac{VBATTERY + VSCHOTTKY}{VINPUT + VSCHOTTKY}$$

Allowing a 25% ripple in the bulk current will give a reasonable value of inductance. The inductor value can be calculated as follows:

$$L = \frac{4 \bullet (VINPUT - VBAT) \bullet D}{IBULK \bullet fOSC}$$

A 150µH inductor is used in the application circuit.

Current Control Loop

The UCC3956 features an outer voltage loop and an inner average current loop. The virtues of average current mode control are well documented in Reference [1]. A simplified block diagram of the feedback elements is provided in Figure 3. The network for the current amplifier could be as simple as a single capacitor, providing a dominant pole response, which may be adequate for a battery charger application. The current amplifier network of Figure 3 provides improved transient performance. The component values for CF3, CF4, and RF4 will be selected to give a constant gain from approximately fOSC/10 to fOSC. At frequencies below fOSC/10, the network gain will increase at 20dB/decade, giving a high DC gain. The network will attenuate at 20dB/decade above the switching frequency, giving noise immunity.

A feedback design that optimizes transient response will have the amplified inductor current down-slope approach the PWM saw-tooth slope [1]. This occurs by designing the total loop gain to cross unity at 1/3 to 1/6 of the switching frequency. The applications circuit is designed to cross unity gain at 1/10 of the switching frequency (10kHz), with a 12V nominal input. The power stage small signal gain can be approximated by:

$$GPOWER\_STAGE = \frac{VIN \bullet RSENSE}{SL + RSENSE + ESR}$$

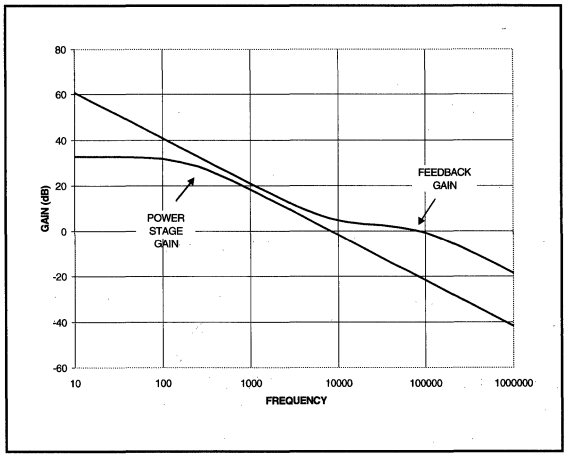

Figure 4a. Current Loop Power Stage and Feedback Gain

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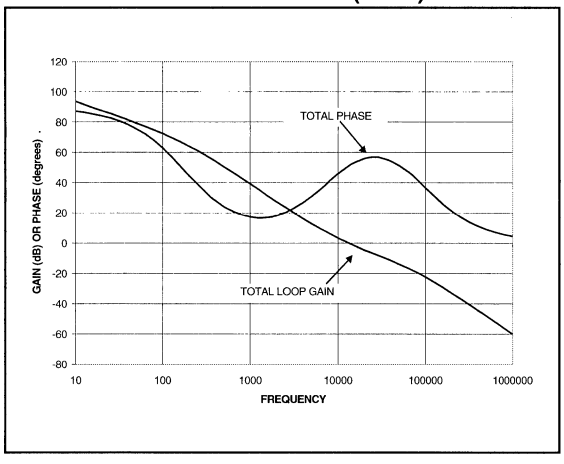

Figure 4b. Current Loop Total Gain and Phase

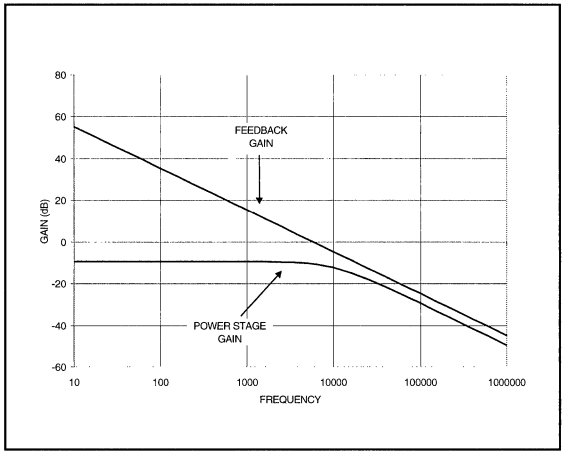

Figure 5a. Voltage Loop Power Stage Gain

Referring to Figure 3, the current sense amplifier provides a gain of 5, an inverting stage adds a gain of 1.5, and the modulator has a gain of 0.64; adding a fixed gain of 4.8 to the power stage. The current amplifier's gain between fOSC/10 and fOSC is equal to RF4 divided by the parallel combination of RG1 and RG2 times the resistive divider RG2/(RG1+RG2), simplifying to:

$$GCA = \frac{RF4}{RG1}$$

RF4 is selected to be 15k, resulting in a 10kHz crossover frequency. Once RF4 is determined, CF3 and CF4 can be selected to give corner frequencies at fOSC/10 and fOSC respectively.

$$CF3 = \frac{1}{2 \bullet \pi \bullet fOSC \bullet RF4}$$

$$CF4 = \frac{10}{2 \bullet \pi \bullet fOSC \bullet RF4}$$

In the applications circuit, a value of 100pF is used for CF3 and 1.0nF is used for CF4. Figure 4a shows the power stage gain and feedback network gain for the current loop. Figure 4b shows the total open loop gain and phase.

Adding the Voltage Control Loop

The voltage loop comes into regulation during the overcharge period of operation. The output of the voltage amplifier begins to decrease, demanding less current to the battery. With the current loop closed, the power stage gain of the voltage loop is equal to 1/(5*RSENSE) out to the crossover frequency (10kHz). In order to avoid interactions with the current loop, the voltage loop will cross unity at 2kHz. The voltage loop is attenuated by the divider RG1/(RG1+RG2). A single pole network is added to the voltage amplifier, giving a high gain at DC. Referring to Figure 3, the voltage amplifier gain is equal to the impedance of CF1 divided by RS1. A 2.2nF capacitor will give a total crossover frequency near 2kHz. Figure 5a shows the gain of the power and feedback stages for the voltage loop. Figure 5b shows the total gain and phase of the voltage loop.

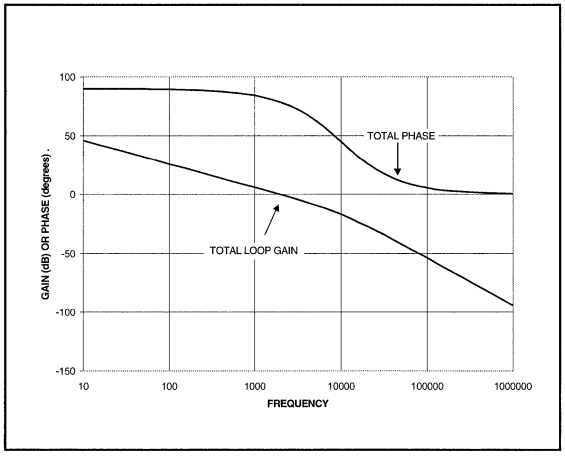

Figure 5b. Voltage Loop Total Gain and Phase

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U-504 Using the bq2000/T to Control Fast Charge

Introduction

The bq2000/T are programmable, monolithic ICs for fast-charge management of nickel cadmium (NiCd), nickel metal-hydride (NiMH), and lithium-ion (Li-Ion) batteries in single- or multi-chemistry applications. This application note discusses simple ways to select all necessary components to implement various switch-mode topologies. It also discusses how to configure the bq2000/T inputs to accommodate different application concerns. Please review the bq2000 and bq2000T data sheets before using this application note.

Basic Charge-Control Operation

Charge Initiation

The bq2000/T initiates a charge on either (1) power-up or (2) excursion at the BAT input from above a V_{RCH} threshold to below it. The V_{RCH} threshold is below the threshold of voltage regulation, V_{MCV}, and therefore does not initiate charge of a "full" Li-Ion battery. This feature is especially useful if cell polarization is taken into account because the battery voltage decays to a lower value following fast charge.

Configuring the BAT Input

The BAT input to the bq2000/T is the input to an A/D converter with a resolution of about 3mV. A/D measurement is performed only when the timing oscillator and current regulator have been switched off. The BAT input has the following four voltage thresholds:

1. V_{LBAT} (approximately 1.0V) is the minimum qualified input voltage to initiate full current to the battery at the start of fast charge. Below this level, the bq2000/T follows its pulse-trickle algorithm. This arrangement enables it to "wakeup" a pack protector in a Li-Ion pack or trickle up a deeply discharged nickel-based chemistry pack.

2. V_{RCH} (1.9V) is the battery replacement threshold. As described above, an excursion through this threshold triggers battery replacement and reinitiates of fast charge.

3. V_{MCV} (2.0V) is the threshold of voltage regulation. Above this level, the MOD output is forced low, regardless of the condition of the SNS input, resulting in a pulsed current regulation similar in operation to a bang-bang type voltage regulator. When the BAT input voltage exceeds 2.0V more than 85% of the time, charge is terminated.

4. V_{SLP} is the sleep-mode threshold and approximately 1.0V below Vcc. If the BAT input is driven to this threshold, power to the IC is turned off and the MOD output is driven low. This threshold is internally provided for implementations in which the IC must remain connected to the battery when charge power is removed. Under this sleep mode, the IC draws 1µA or less.

The operation of these four thresholds determines the following design guidelines for configuring the BAT input

To charge a fixed number of nickel-based cells, the BAT input is configured for the voltage of a single cell. Thus for an N-cell pack the resistor ratio of the divider is (N-1):1. See Figure 1. This configuration assures a 3mV PVD sensitivity for fast charge, which is an excellent termination criterion for NiMH cells and good for most NiCd cells. Of course the total divider network represents a load on the battery when power is not present and is sized accordingly. Also, the BAT input must not be driven with more than 20µA in the absence of power. (This is the permissible limit for the substrate diode that clamps this input to Vcc.)

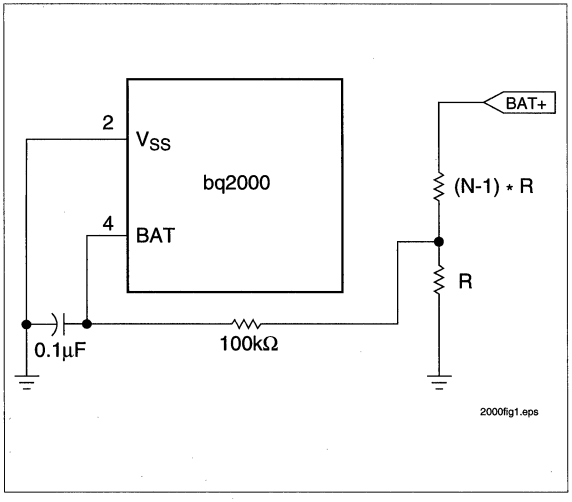


Figure 1. Battery Voltage Divider for Nickle Chemistry—Single Pack

Charging multi-cell packs of nickel-based chemistry and some high-capacity NiCd packs often requires compressing the batteries' signal voltage into the range of the A/D converter to accommodate the cell range or to require a steeper negative slope on the battery as a criterion of ter-

mination. This compression is accomplished by a single additional resistor in the divider chain from the battery, R_1. See Figure 2. This extra resistor adds offset to the battery-divider voltage, allowing a larger voltage excursion on the battery for a smaller excursion at the BAT input. The fixed in-circuit voltage to which this additional resistor is tied is Vcc.

The design procedure for the varying pack size is as follows:

1. Determine the difference between the end-of-charge voltage for the maximum number of cells and the start-of-charge voltage for the minimum number of cells. This signal, which must be compressed into the A/D voltage window of 1–2V, is $V_{EXCURSION}$. For a 1V window, the gain of the divider network is simply $1/V_{EXCURSION}$.

2. Determine the offset, V_{OFF}, from one of the endpoint equations by substituting the gain calculated in step 1. The minimum condition is expressed by the equation

$$(V_{BAT} - V_{OFF}) * \left(\frac{1}{V_{EXCURSION}}\right) + V_{OFF} = 1$$

   Substituting the minimum battery voltage for V_{BAT} and Solving for V_{OFF} gives the voltage that would appear at the BAT input in the absence of the battery.

3. Choose a suitable resistor divider from Vcc to GND to establish this offset voltage.

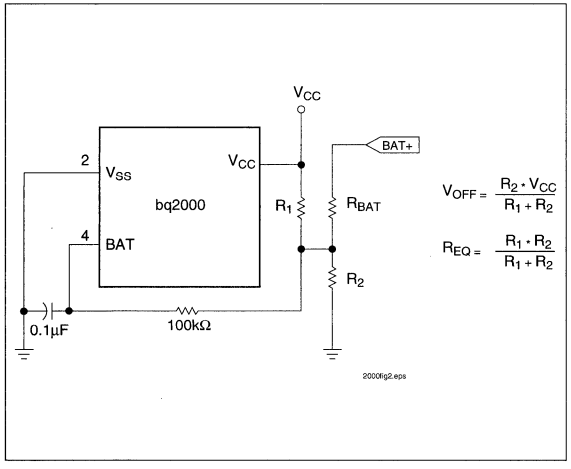


Figure 2. Battery Voltage Divider for Nickle Chemistry—Multi-Pack or High-Capacity NiCd

4. Implement the gain function by determining the equivalent resistance of the parallel combination of the offset setting resistors, R_{EQ}, and setting

$$R_{BAT} = (V_{EXCURSION} - 1) * R_{EQ}$$

where R_{BAT} is the resistor connected between BAT+ and the offset point. See Figure 2.

For high-capacity packs, the goal is to increase the per-cell negative voltage excursion, which will serve as a criterion of fast-charge termination. **Note:** Throughout this application note, the expression PVD is often equated with -ΔV. Although some think of these as different termination criteria, they are actually two ways of saying the same thing. For a voltage to qualify as a "peak", a subsequent measurement must be less than this "peak" measurement by a discernable amount. Since no circuit can anticipate a subsequent reading, the peak voltage detection occurs upon measuring a subsequent voltage that is discernibly less than the maximum voltage measured to that point in time. In the case of the bq2000/T this sensitivity is -3.8mV, leading to the parallel drawn between PVD and -ΔV, as the later is usually just a less sensitive PVD. The desensitization is accomplished by compressing the total battery voltage excursion during charge into a fraction of the A/D voltage window at the BAT input to the bq2000/T. This design procedure is as follows:

1. Determine the multiplier of the peak voltage sensitivity desired for the battery. A typical desired -ΔV value for high-capacity cells is –15mV The multiplier is then (–15mV/–3.8mV) or about 4. The gain is then determined to be 1/(4 * N), where N is the number of cells.

2. The offset is determined from the goal of having the maximum battery voltage correspond to the maximum input voltage. In this example, the resulting offset is (6 * N)/(4 * N-1), where N is the number of cells. This offset is established at BAT by choosing a resistive divider from V_{CC} to GND. These resistors correspond to resistors R_1 and R_2 as shown in Figure 2.

3. A third resistor, R_{BAT}, is chosen to establish the proper gain with respect to the parallel combination of resistors R_1 and R_2 represented by R_{EQ}. In the example used in step 1, the gain was 1/4N. This is achieved by setting $R_{BAT} = R_{EQ} * (4N-1)$.

Finally, Li-Ion batteries can be charged at a constant current only until their characteristic regulation voltage is reached. The bq2000/T accommodates this restriction by regulating the voltage at the BAT input to 2V. The battery resistive divider should ensure that the BAT input reaches its regulation voltage when the battery reaches its characteristic regulation voltage. See Figure 3.

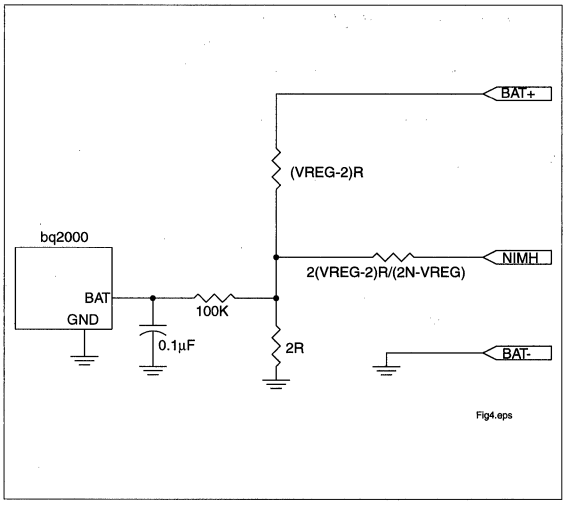


Figure 3. Voltage Regulation Battery Divider for Multi-chemistry Applications

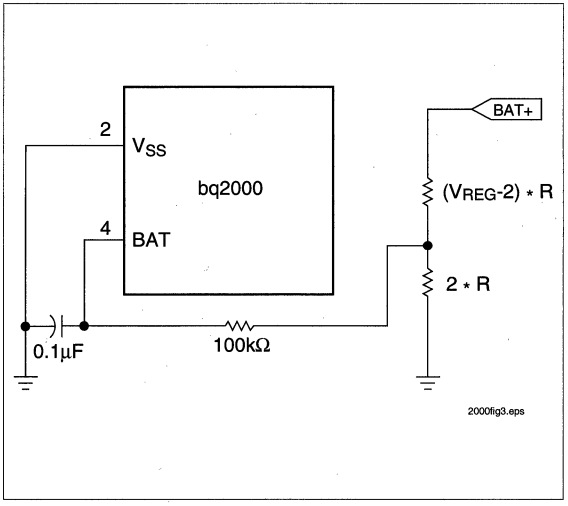


Figure 4. Voltage Regulation Battery Divider

The safest way to design for multi-chemistry packs is to add a mechanical connection to the nickel-based chemistry packs, constituting an additional battery negative connection. The default Li-Ion resistive divider is attenuated by a resistor in the charger, which connects to this point when a nickel battery is installed, but which floats when a lithium battery is installed. This fail-safe mechanism is normally required by cell ratios of 1 lithium to 3 nickel. See Figure 3.

NiMH batteries rarely exceed 1.6V per cell at charge rates consistent with lithium cells. Therefore, the single divider network as shown in Figure 4 is acceptable for cell ratios of 2 lithium to 5 NiMH, as long as the maximum charge voltage of the nickel-based pack is below that of the Li-Ion pack. This design is not recommended for NiCd batteries, however, as they will often achieve voltages in excess of 1.8V/cell, especially toward the end of cycle life. If the nickel-based chemistry cells do reach the regulation voltage during charge, they usually terminate only for maximum time or temperature with the bq2000. The bq2000T is the safest choice for the 2:5 ratio, because it relies on $\Delta T/\Delta t$ as the primary means to terminate nickel-based chemistries. Ratios of 2 lithium to 4 nickel normally fit comfortably within the charge window for their useful lives, for either voltage-based or temperature-based termination.

Configuring the SNS Input

If the SNS input is within ±50mV of the bq2000/T ground (V_{SS}), the MOD output is fully enabled. If the SNS input is greater than 50mV (V_{SNSHI}) or less than -50mV (V_{SNSLO}) compared to the ground of the bq2000/T, then the MOD output is driven low. Since battery and temperature voltages are always measured with respect to ground, the user can take advantage of this feature to implement both high-side and low-side current sense regulators. If no control of MOD is desired, the SNS pin can be grounded and the MOD output used only to switch an external current source on or off. The control feature makes it possible to configure the SNS input to provide either linear or switching regulation of charge current. Furthermore, frequency is most dependent on filter components and hysteresis-setting capacitance and only slightly dependent on power component values. This characteristic makes it possible to "slave" the circuit to an external oscillator of fixed frequency.

Low-Side Sensing

For low-side sensing applications, the sense resistor is placed in the path between the battery's negative terminal and power supply ground. See Figure 5. The battery's negative terminal becomes the signal ground for the bq2000/T. Signals and power applied to the bq2000/T are capacitively decoupled and referenced to this point. The resistor selected should have a value equal to 50mV divided by the desired charge current. Thus, at a current of 1A, the sense resistor is 50mΩ. Some applications may

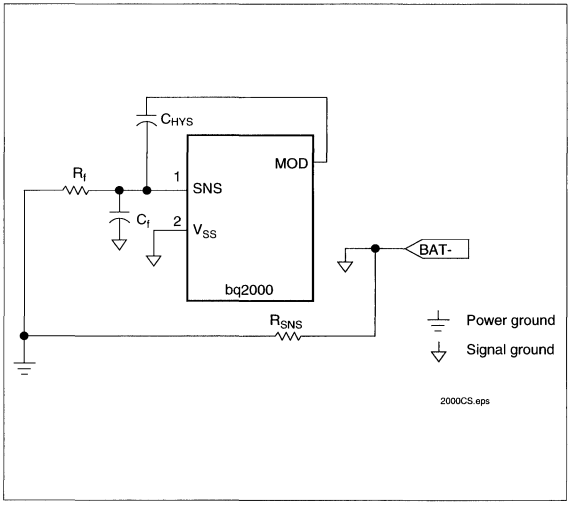


Figure 5. Current-Sensing Circuit

find the resulting sense resistor too small to be practical. These are easily accommodated by making the sense voltage presented to the bq2000/T a suitable fraction of the sense current. In the 1A example, the sense resistor can be made to be 0.1Ω provided the voltage across the sense resistor is divided between two equal resistors at its presentation to the SNS input. The application however, must also be able to tolerate the higher voltage on the sense resistor.

As suggested from the above, the voltage on the sense resistor is presented to the SNS input through a resistance that forms part of a filter. The rest of the filter is a capacitor that decouples the SNS input from the Vss of the bq2000/T. When the user is content with a sense voltage of 50mV, the SNS input is connected to the power supply ground at the grounded terminal of the sense resistor through a resistor sized for the desired operating frequency. See Figure 5. An exact expression for the sizes of the capacitive and resistive components involves the simultaneous solution of two very complex equations. A few simplifying assumptions, however, can allow most users to bound their operating frequencies to within about 5%.

The six values that determine operating frequency are input voltage V_{IN}, inductance L, sense resistor R_{SNS}, filter resistance R_F, filter capacitance C_F, and hysteresis capacitor C_{HYS}. Input voltage is given. The sense resistor converts the current waveform in the inductor to a voltage waveform for presentation to the SNS input. Low detection voltage, while requiring low-valued resistors to sense current, makes possible the sharing of resistors between a charger and gas gauge IC. The hysteresis capacitor and SNS input filter components have the most influence on operating frequency. The hysteresis capacitor is connected from the MOD output to SNS input directly; however, the voltage hysteresis is attenuated by the ratio between the two capacitors. Since the MOD output swings 5V, the SNS input moves by the ratio $5V * C_{HYS}/(C_{HYS} + C_F)$. This injected hysteresis is of 5–25mV for best results. Below is a simplified design procedure:

1. Select the desired maximum operating frequency F. This is the frequency of operation when the output voltage is exactly half the input voltage. At duty cycles of 75% or 25%, the frequency is 75% of this value.

2. Choose C_{HYS} = 4.7pF to minimize the capacitive load on the MOD output.

3. Choose

$$R_F * C_F = \frac{1}{(4 * F)}.$$

This reduces exponential functions to constants in the equations relating all the values. Choose C_F for the desired hysteresis level, and then calculate R_F from the above relation.

4. Calculate the inductor value L from the relationship below:

$$L = \frac{V_{IN} * R_{SNS} * R_F * C^2_F * V_{CC}}{C_{HYS} * (57.87V)}$$

The constant in the denominator results from the dimensionless exponential functions. Consider the example below:

Battery is 5-NiMH cells.

V_{IN} = 12V I = 1A $\therefore R_{SNS}$ = 0.05Ω
F_{MAX} = 100KHz C_{HYS} = 4.7pF

Choose C_F = 2200pF for a hysteresis of 10.7mV (approximately 20% of the 50mV signal). R_F = 1.1K from 3 above.

Then L = 58µH. The actual current ripple at this frequency is 25%, 5% of this is due to the phase delay through the filter. Since it is desirable to keep the ripple current large to keep the inductor small, the assumption made in 3 above is a good rule of thumb. For a smaller ripple current, increase the size of the capacitive filter staying at or below 4700pF. For a larger ripple, diminish the size of C_F staying at or above 1000pF. The inductor changes in value accordingly.

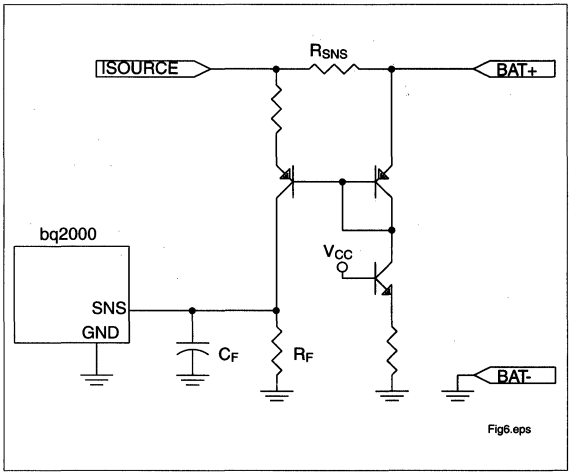


Figure 6. Voltage-to-Current Converter Design for High-Side Sensing

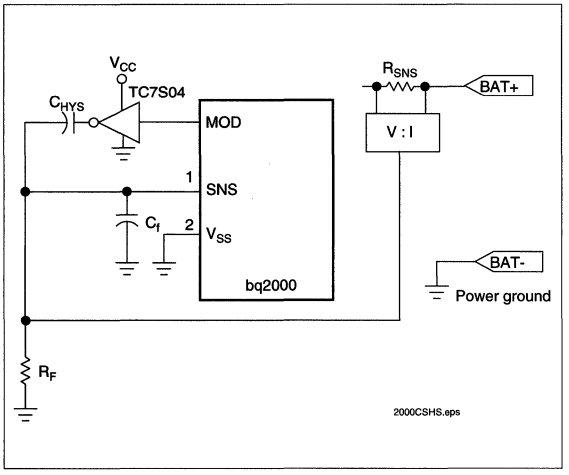


Figure 7. Current-Sensing Circuit—High Side

High-Side Sensing

High-side sense requires that the sense resistor be placed in the circuit between the switching inductor and the battery positive terminal. From there, the signal must be translated down to the SNS input to the bq2000/T. While this translation may seem difficult at first, the AC signal integrity needs to be good only about the regulation point. This limitation makes a three transistor voltage mirror possible. See Figure 6. One transistor of NPN polarity provides constant-current bias to a diode-connected PNP transistor with the sense resistor in its emitter. A second PNP transistor with a suitably large emitter resistor is connected in parallel with the diode connected PNP and sense resistor, but with its collector open. This collector drives the filter resistor R_F to the regulation voltage above ground. In this case, the V_{SS} of the bq2000/T is itself connected to power ground, and all signals and power are decoupled to power ground. The filter capacitor C_F is connected in parallel with R_F in this case. The last remaining difficulty is providing the hysteresis signal from MOD as in this case the signal output from MOD must be inverted to properly drive the SNS input. Most buck-mode switching regulators have such an inversion in the circuit that can be conveniently capacitively coupled to the SNS input. Failing that, it is possible to add a single inverter to the circuit such as a TC7S04F. See Figure 7. Such a single-gate circuit is necessary in synchronized battery-charger designs.

Synchronizing the bq2000/T to a Fixed Oscillator

Synchronizing the bq2000/T is actually quite simple. First, design the filter components and choose the inductor for a maximum operating frequency below the desired frequency for synchronizing the bq2000/T. The big difference between configuring for synchronization or for high-side or low-side sensing is that the hysteresis capacitor in synchronization is not connected directly to the MOD output, but rather to the output of either a single AND gate in the case of low-side sensing or to the output of a NAND gate in the case of high-side sensing. One of the inputs to the gate is MOD and the other is the desired synchronizing frequency. Possible single-gate devices are the TC7S00FU and the TC7S08FU. See Figure 8.

Configuring the TS Input

The TS input to the bq2000/T is characterized by three operational thresholds that determine qualification and termination conditions. The thresholds on the TS input are all ratiometric to the power supply. This design allows resistor biasing to V_{CC} and V_{SS} of a single negative temperature coefficient (NTC) thermistor with consistent temperature thresholds at any operating voltage as shown in Figure 11. We recommend a filter capacitor at this input of no more than 0.01µF, combined with a 100kΩ resistor, to prevent noise terminations at elevated operating temperatures.

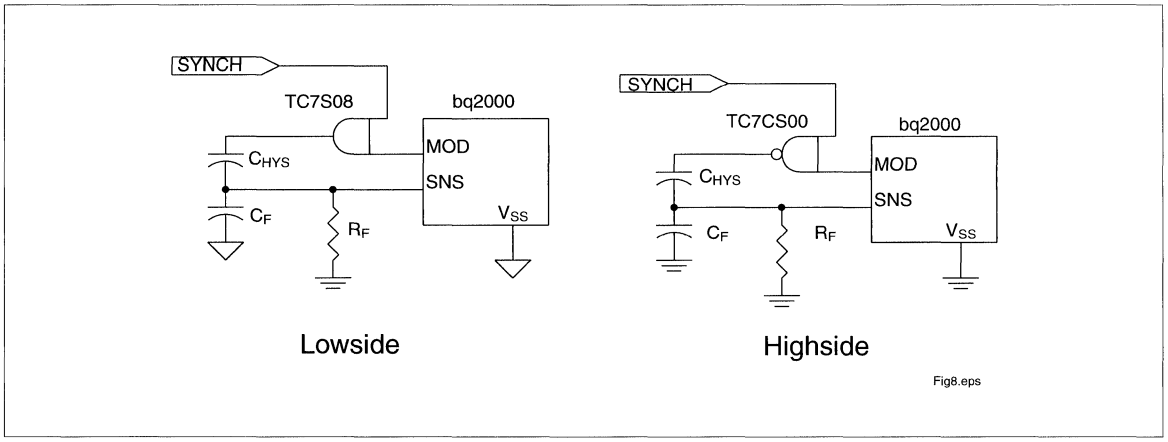


Figure 8. Synchronization Circuit for Low- and High-Side Designs

The following are descriptions of the three thresholds:

1. V_{LTF} set at 0.5 * V_{CC} is the cold temperature/pause threshold. At voltages above this threshold, the bq2000/T pulse-trickles and flashes the LED pin to indicate that the bq2000/T is in the pause or inhibit mode. This process suspends fast charge in progress by freezing the contents of elapsed-time counters, defeating all termination algorithms and resetting all data-gathering. When restored to a normal operating range, the bq2000/T resumes a suspended fast charge or top-off in progress but rebuilds discarded historical data before the fast-charge termination algorithms can take effect.

2. V_{HTF} set at 0.25 * V_{CC} is the maximum starting temperature threshold. If fast charge starts at input voltages below this threshold on the TS input, the bq2000/T flashes the LED pin as it does in the pause mode to indicate that charge is pending. This threshold has no effect after fast charge has started.

3. V_{TCO} set at 0.225 * V_{CC} is the cutoff temperature for fast charge and top-off. At voltages below this threshold on the TS input, a fast charge or top-off in progress terminates and does not resume. This is considered a "done" condition. Note that this condition is superceded at the start of fast charge by the starting temperature threshold described above. A very hot battery placed in the charger causes the bq2000/T to flash the LED pin to indicate charge pending, even if the cutoff temperature is exceeded. The bq2000/T does not pulse-trickle charge an overheated battery until it cools below the cutoff temperature threshold. Then the battery is pulse-trickled until it cools below the starting temperature threshold, following which it starts fast charging.

A simple configuration procedure is as follows:

If no temperature limits or inhibit (pause) function are desired, bias the TS input to a voltage level between 1.25 and 2.0 volts. This biasing can be done with a simple divider network between V_{CC} and V_{SS}. See Figure 9.

If temperature limits are not required, but an inhibit function is, use the same bias network, but terminate the second resistor to the inhibit signal rather than to V_{SS}. A logic high inhibits, while a low enables. See Figure 10.

Finally, if a full-featured design is desired, choose two resistor values to bias a NTC thermistor taking note of its cold temperature value, R_C, and its high temperature value R_H. The resistor from V_{CC} to the thermistor, R_1, and from the thermistor to V_{SS}, R_2, can be calculated from the formulas given below:

$$R_1 = \frac{22 * R_H * R_C}{9 * (R_C - R_H)} \qquad R_2 = \frac{22 * R_H * R_C}{(9 * R_C) - (31 * R_H)}$$

If the denominator of R_2 becomes zero, or nearly so, R_2 can be left out, effectively making it infinite; however, this equation places a limit on the effective range of temperature for any given thermistor. In most cases, this does not present a problem as it corresponds to about a 30°C range. The thermistor value at which charge is inhibited because of overtemperature can now be represented by this term:

$$R_{THERM} = \frac{1.25 * R_1 * R_2}{3.75 * R_2 - 1.25 * R_1}$$

6/11

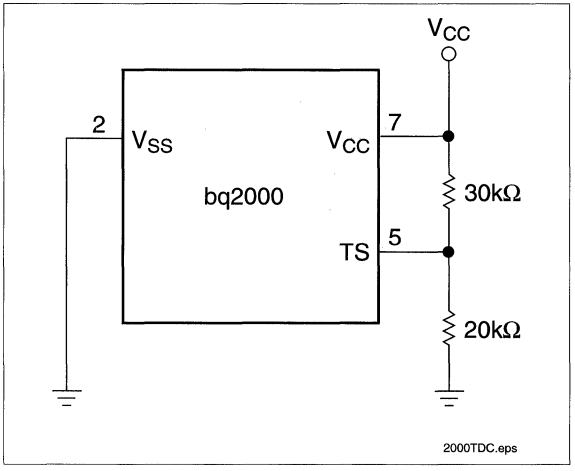


Figure 9. Temperature Defeating Configuration

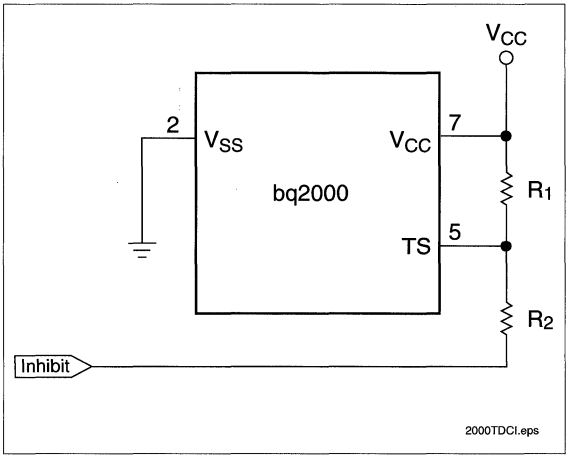


Figure 10. Temperature Defeating Configuration with Inhibit

Constraining the High-Temperature Start of Charge

Some applications emphasize not starting charge above a certain temperature more than exactly where charging terminates for an overtemperature condition. If this is the case, the following two equations can be substituted for those above, with the understanding that R_H now represents the high-temperature prequalification resistance of the NTC thermistor, and the term to the extreme right represents the thermistor value at cutoff:

$$\frac{1.125 * R_1 * R_2}{3.875 * R_2 - 1.125 * R_1}$$

Where:

$$R_1 = \frac{2 * R_H * R_C}{R_C - R_H}$$

$$R_2 = \frac{2 * R_H * R_C}{R_C - 3 * R_H}$$

Configuring the TS Input to the bq2000T for ΔT/Δt Termination

A Thevenin-equivalent circuit can be used to represent the bias on the thermistor connected to the TS input. As such, a circuit has only two characteristics capable of modification, and only two constraints can be imposed on the voltage excursion resulting from the thermistor's variation with temperature. Thus, in the case of the bq2000T, the most critical specification is the charge range, usually the high-temperature cutoff, while the second constraint is the rate of change of temperature with time, which is the criterion of charge termination. Generally, the temperature at which the ΔT/Δt condition should apply is approximately 5°C above the expected ambient. This condition is ratiometric to the supply voltage but corresponds to a rate of 31mV/min with a 5V V_{CC} voltage (V_{CC}/161). The following system of equations calculates two resistor values (R1, connected between V_{CC} and the thermistor and R2, connected in parallel with the thermistor), which bias the thermistor connected inside the battery pack to the negative terminal of the battery:

$$\frac{R_{T30} * R_2 * 5}{(R_{T3} * R_2) + R_1 * (R_{T30} + R_2)} -$$

$$\frac{R_{T31} * R_2 * 5}{(R_{T31} * R_2) + R_1 * (R_{T31} + R_2)} = 0.031$$

$$\frac{R_{THI} * R_2 * 5}{(R_{THI} * R_2) + R_1 * (R_{THI} + R_2)} = 1.125$$

where R_{T30} and R_{T31} represent the thermistor value at 30°C and 31°C respectively, and R_{THI} represents the high temperature cutoff resistance. Selecting a low beta thermistor such as the Semitec 103ET-2 together with a 40°C cutoff affords a range of 0 to 40°C with a 1°C per minute sensitivity at 30°C. The same sensitivity can be attained with a range of 0 to 50°C by selecting a high beta thermistor such as the Semitec 103GT-1. Note that,

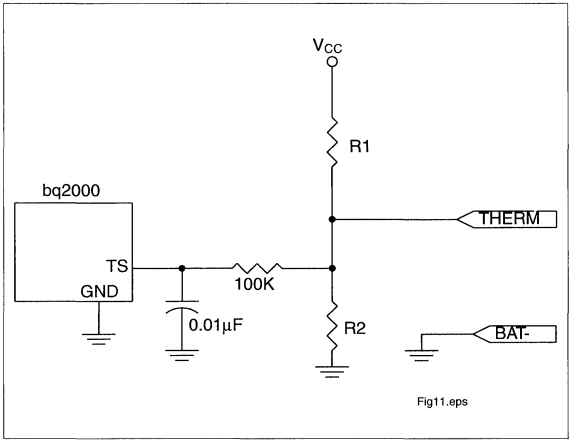


Figure 11. Configuring the TS Input

in solving these equations, $R_1 \geq R_2$ implies that there will be *no* cold temperature fault.

For ease of design, a table of values for R_1 and R_2 is presented below for various popular thermistors and temperature ranges.

Thermistor	Range (°C)	R_1	R_2
Semitec 103AT-2	-1.6–40	17.8K	45.3K
	0.7–45	14.7K	33.2K
	4–50	12.4K	23.7K
	8–55	10.5K	23.2K
Semitec 103ET-2	0–40	19.1K	69.8K
	1.8–45	15.8K	45.3K
	4.6–50	13.3K	34.8K
	8.2–55	11.5K	29.4K
Semitec 103GT-1	-10.8–40	13.7K	17.4K
	-6–45	11.3K	14.7K
	-0.2–50	9.31K	12.7K
	6.9–55	7.87K	11.5K
Philips 2322-640-63103 or Fenwal197-103LA6-A01	-7.9–40	14.7K	21K
	-4–45	12.1K	17.4K
	1.3–50	10K	15K
	7.2–55	8.45K	13.3K
Keystone RL0703-5744-103-S1	-9.6–40	14K	18.7K
	-5.2–45	11.5K	15.8K
	0.6–50	9.53K	13.7K
	7.1–55	8.06K	12.4K

Selecting the Timing Components

The RC pin of the bq2000/T provides for an infinitely variable time-out range, so the user is not bound to binary multiples and submultiples of a 1C charge rate. The time-out set by these pins expressed in minutes is determined by the formula R * C * 35988, where R is in ohms and C is in Farads. The value of R also determines the rate of maintenance trickle following charge for nickel-based chemistries. A C value of 0.13µF or greater selects a top-off algorithm to follow fast charge for pulse-trickle duty cycles of 8.33% or less. top-off is characterized by an interval equal to the time-out during which the battery is pulse-charged at a $1/16^{th}$ duty cycle.

The main consideration in selecting the timing components is the rate at which charge is being restored to the battery expressed as a fraction (or multiple) of its rated capacity. As most battery manufacturers deliver batteries that exceed their rated capacities, the recommended time-out period is that which allows 33% more charge than the rated capacity to be returned to the battery during the timed charge interval. Thus, for a battery charged at a 1C rate, the timeout interval is 80 minutes. This interval allows for up to a 20% overcapacity that may occur in new batteries, a small allowance for charge efficiency, and a small overcharge to insure cell balance. Batteries charged at rates below C/4 may need to add significant additional time to accommodate charge inefficiency. Note that the 14-hour time-out normally recommended for NiCd batteries charged at C/10 is because of the poor charge efficiency at this rate of charge. Li-Ion or Lead Acid batteries require voltage regulation as part of the charge algorithm and normally take longer to charge, and the bq2000/T has incorporated a time-out doubler that is activated if the battery achieves voltage regulation.

Here then is a design procedure :

1. Express the charge rate as a fraction or multiple of the capacity.
2. Divide 80 minutes by this fraction or multiple to determine the desired time-out expressed in minutes.
3. Divide this result by 35,988 to determine the R·C product.
4. If top-off is desired, choose C ≥ 0.13µF. If not, choose C ≤ 0.07µF.
5. Calculate R from time-out = R * C * 35,988. An additional condition on top-off is that R < 300K. (Even with the time-out capacitor and a resistor of less than 300k, a time-out of 23 hours can be realized.)

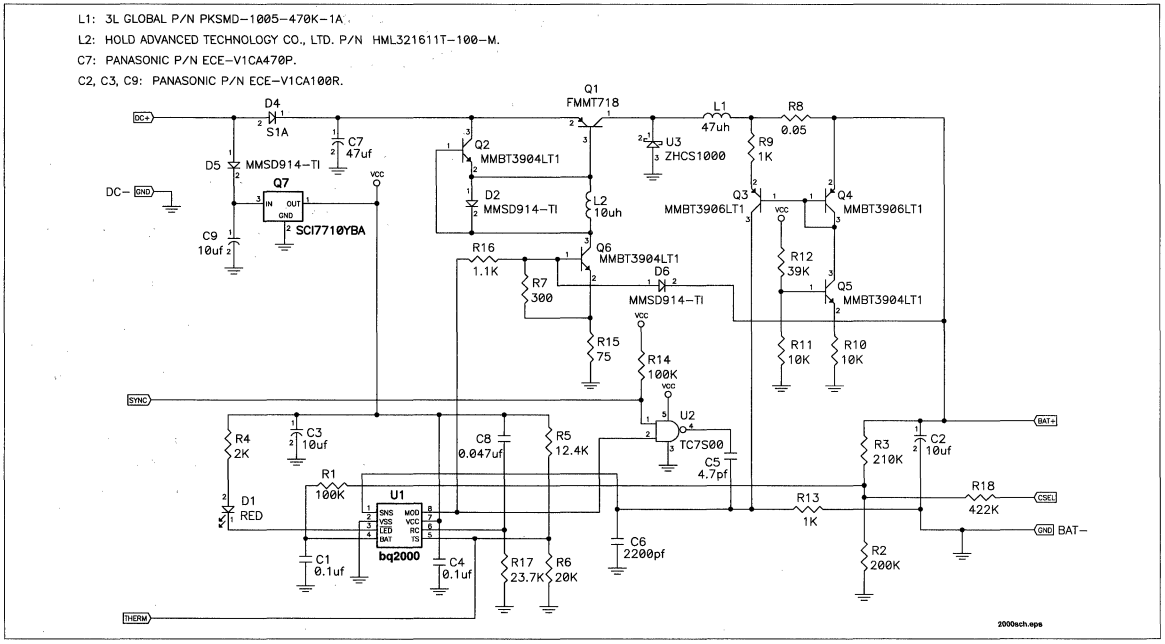


Figure 12. Dual-Chemistry Buck Regulator with High-Side Current Sensing

6. Verify that the trickle-pulse rate selected from the graph multiplied by the charge rate determined in step 1, is less than or equal to 1/32 for NiCd or 1/64 for NiMH, and that R < 500000.
7. Failing any condition imposed in steps 5 and 6, return to step 4 and choose a larger value for C within the limits specified.

Example: NiCd Battery

1. C/2
2. 160 minutes
3. $R * C = 4.4459 \cdot 10^{-3}$
4. Choose C = 0.001µF (1000pF)
5. R = 4.446MΩ
6. R > 500KΩ **(Selected capacitor is too small.)**
7. Choose C = 0.01µF
8. R = 444KΩ
9. Pulse-trickle = 1/10.7(>1/32) **(Pulse-trickle exceeds recommended value for NiCd.)**
10. Choose C = 0.047µF
11. R = 94.6KΩ
12. Pulse-trickle = C/50 **(All parameters within specified limits.)** For standard values, choose R = 95.3KΩ and C = 0.047µF.

Charge Termination Considerations

Fast charge terminates when any of the following conditions is fulfilled:

1. The average voltage at the BAT input to the bq2000/T declines by PVD threshold from its highest previous value (bq2000/T).
2. The signal at the TS input declines at a rate of V_{TERM} (bq2000T).
3. Regulation voltage is attained at the BAT input and the current tapers to I_{MIN} threshold.
4. The maximum temperature threshold at the TS input is exceeded.
5. The timer expires.

Measurement accuracy made in 3 above may depend on the degree to which the battery voltage is filtered. A larger value of capacitance connected across the battery leads to a more accurate termination measurement.

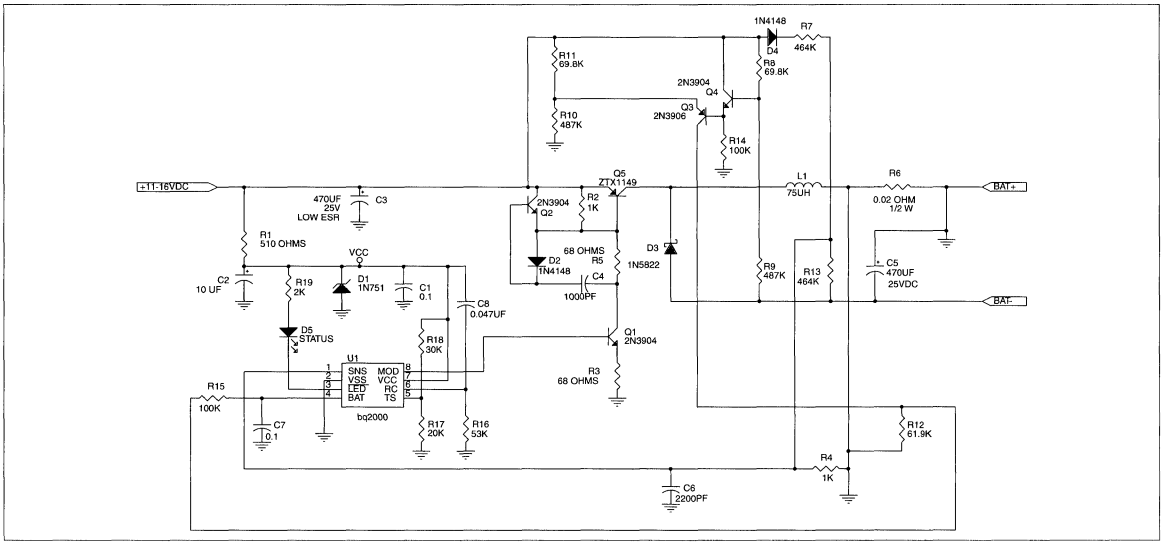


Figure 13. Simple Buck-Boost Design

Configuring the LED Output

The LED output is an open-drain MOSFET capable of sinking up to 10mA of DC current. Unlike the CMOS inputs to the bq2000/T, the LED output is protected from overvoltage by a punch-through ESD structure. Thus the LED output can tolerate voltages within the recommended operating range, independent of the bias on the V_{CC} pin.

Layout Considerations

The bq2000/T makes its voltage and temperature measurements with the switching regulator and timing oscillator turned off. This prevents layout considerations from affecting termination decisions. Layout is very important, however, for predicting the performance of the switching regulation function. One rule applies for high or low-side regulation:

Minimize the size of all input pin nodes. Locate all bypass, feedback, and filtering components adjacent to their connected input pins, or power pins in the case of bypass. Ground connections associated with any power or input pin to the bq2000/T must be kept separate from all other grounds and brought directly to the correct side of the sense resistor. The resistor associated with the SNS input filter must connect separately and alone to the opposite side of the sense resistor.

Application Example: Simple Dual-Chemistry Buck Regulator

To safely accommodate two distinct battery chemistries in the same charger, voltage regulation must supercede completeness of charge. This requirement implies that, for simplicity of charger design, the user must sacrifice similarity of discharge voltage, but for similarity of pack voltage under discharge, the user must default under conditions of contact failure to voltage regulation for safety reasons. A fixed cell-ratio usually applies for applications requiring similar discharge voltage—for example, 3 NiCd/NiMH to 1 Li-Ion. The safest design approach for these packs is to include an additional negative battery contact on the nickel chemistry packs that will adjust the battery divider in the charger to accommodate the higher charge voltage requirement. See Figure 12.

If packs of dissimilar voltage can be allowed, the user may select a pack of higher output voltage for the voltage regulated chemistry while the nickel chemistry pack has a higher amp-hour rating. These pack cell ratios should be 2 Li-Ion to 5 or fewer nickel cells or 2 lead acid to 3 or fewer nickel cells. Care must be taken here to limit the charge current to the nickel cells so they do not achieve voltage regulation. If they do, they will not terminate for $-\Delta V$. The safest approach to cell counts that risk this situation is to use the bq2000T.

Buck-Boost Design

This section illustrates a commonly encountered application, one in which a user wishes to design an automotive charger for a number of cells whose voltage at end of charge would exceed the supply. A nickel cell count of 8 would fit the requirement of a buck-boost implementation if charged from a cigarette lighter. This circuit maintains a constant current to the battery by compensating the current regulation in the inductor for the difference between the input and output voltages from the supply. The voltage inversion allows the inductor to remain a single winding. See Figure 13.

Charging Lead-Acid Batteries

The bq2000/T charges lead-acid batteries where a pulsed-charge algorithm is acceptable. The charger is designed so that (1) the bulk voltage (nominally 2.45 V/cell) on the battery causes the regulation voltage to appear on the BAT input and (2) the float voltage (nominally 2.275V/cell) causes the battery replaced voltage of 1.9V to appear on the BAT input. The SNS input can be configured normally for current limit. For temperature compensation, an NTC thermistor is part of the resistive divider. The design procedure is to solve the following four equations simultaneously for values R_1, R_2, R_3, and R_4:

$$\left(\frac{V(LO)_{BULK} - 2}{R_1 + \frac{R_{T(LOW)} * R_4}{R_{T(LOW)} + R_4}} + \frac{3}{R_2} \right) * (R_3) = 2$$

$$\left(\frac{V(25)_{BULK} - 2}{R_1 + \frac{R_{T(25)} * R_4}{R_{T(25)} + R_4}} + \frac{3}{R_2} \right) * (R_3) = 2$$

$$\left(\frac{V(25)_{FLOAT} - 2}{R_1 + \frac{R_{T(25)} * R_4}{R_{T(25)} + R_4}} + \frac{3.1}{R_2} \right) * (R_3) = 1.9$$

$$\left(\frac{V(HI)_{BULK} - 2}{R_1 + \frac{R_{T(HI)} * R_4}{R_{T(HI)} + R_4}} + \frac{3}{R_2} \right) * (R_3) = 2$$

where bulk and float voltages and thermistor values are HI for the high-temperature limit, LO for the low-temperature limit, and 25 for the value at 25°C. R_1 is connected from the battery positive terminal to the higher voltage side of the thermistor. R_2 is connected between the lower-voltage side of the thermistor and Vcc. R_3 is connected between the lower-voltage side of the thermistor and ground of the IC. R_4 is in parallel with the thermistor. The voltage at the juncture of the thermistor, R_4, R_3, and R_2 is applied to the BAT input through a filter. The 3V and 3.1V values on the left side of the above equations assume 5V for V_{CC}. In applications where an alternative voltage for V_{CC} is used, these values would be (V_{CC} – 2) and (V_{CC} – 1.9) respectively. A thermistor value of 100KΩ or greater at 25°C is recommended.

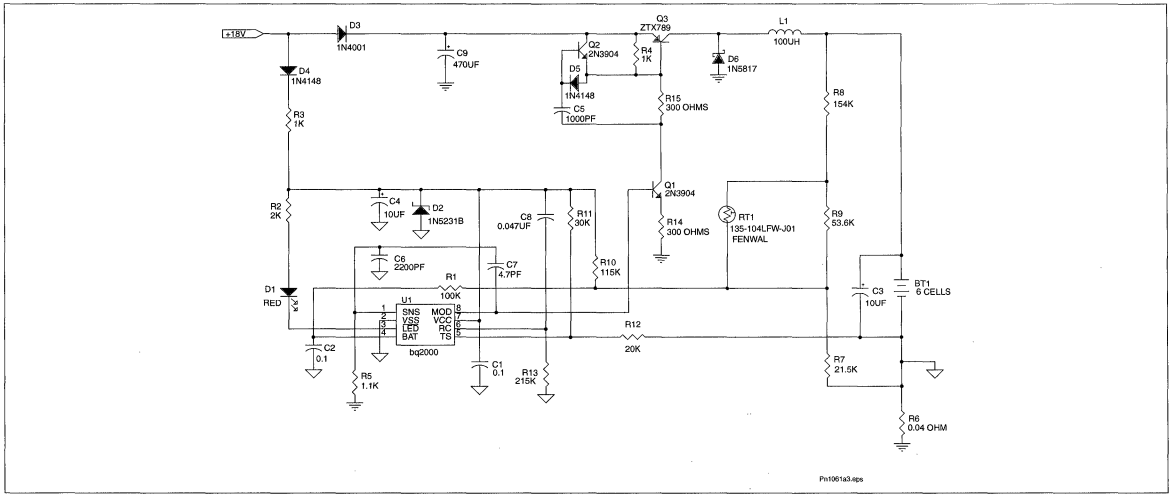


Figure 14. Design Example for Lead-Acid Batteries

UNITRODE

U-505 Using the bq2003 to Control Fast Charge

Introduction

This application note describes the use and functions of the bq2003 gating a current source to fast charge NiCd or NiMH batteries. Examples describe the ease with which the bq2003 is incorporated into applications.

The bq2003 may also serve as the modulator for a switch-mode constant-current regulator to provide an efficient charge current source. This is discussed in the Application Note, "Step-Down Switching Current Regulation Using the bq2003 Fast Charge IC."

Examples for additional applications are being developed. Please contact Unitrode if your application is not supported by one of these examples.

The bq2003 is targeted for applications requiring state-of-the-art fast-charging performance at minimal cost. It provides sophisticated full-charge detection techniques such as $\Delta T/\Delta t$ (delta temperature/delta time) and $-\Delta V$ (negative delta voltage) that enable the user to take advantage of advanced battery technologies such as nickel metal-hydride (NiMH) and high-capacity fast-charge nickel cadmium (NiCd). Systems using the bq2003 can be easily upgraded from NiCd batteries to NiMH batteries without system redesign.

Background

A significant advantage of the bq2003 over other fast-charge solutions is the use of $\Delta T/\Delta t$ and/or $-\Delta V$ as the primary decisions for fast-charge termination. $\Delta T/\Delta t$ detection is one of the most sensitive and reliable methods for fast-charge termination when charging NiMH and NiCd batteries. Near maximum charge acceptance, the temperature rise begins to accelerate at the same time that voltage rise accelerates. The $\Delta T/\Delta t$ decision typically precedes the peak voltage, allowing for minimal overcharge stress.

The $\Delta T/\Delta t$ method also tolerates varying rates of charge, which may be desirable when charging during system operation.

Compared to the ΔT method, which uses two sensors to monitor battery temperature and ambient temperature, the $\Delta T/\Delta t$ method uses a single thermistor to monitor the rate of temperature increase. This approach is more tolerant in cases when the initial battery temperature is significantly different from the ambient temperature.

bq2003 temperature monitoring may be permanently disabled without affecting other bq2003 charge-termination functions.

The bq2003 monitors the voltage across the battery to detect $-\Delta V$, which is a very reliable charge terminator for NiCd batteries. $-\Delta V$ detection in the bq2003 may be temporarily disabled during periods when the charge current fluctuates greatly or during the beginning of a fast charge to eliminate false peaks. $-\Delta V$ may be permanently disabled without affecting other bq2003 charge-termination functions.

To ensure safety for the battery and system, fast charging also terminates based on a hot-temperature cutoff threshold (TCO), a safety time period, and a maximum cell voltage threshold (MCV). To avoid possible premature fast-charge termination when charging batteries after long periods of storage, the bq2003 disables MCV and $-\Delta V$ detection during a short "hold-off" period at the start of fast charge. This hold-off period is configured as described in the bq2003 data sheet.

The bq2003 may be configured to have one, two, or three charge stages. As a one-stage charger, the bq2003 controls charge with no trickle. In a two-stage configuration, the fast-charge stage controlled by the bq2003 is preceded and followed by a continuous trickle charge at a rate controlled by a current-limiting resistor outside of the bq2003. In a three-stage configuration, the fast charge is followed by a "top-off" charge stage at $\frac{1}{8}$ the fast charge rate. This allows the battery to be quickly and safely brought to a full charge state. Following top-off, an external resistor controls trickle charge to the battery at a minimal charge-sustaining rate, typically $\frac{1}{40}$ or $\frac{1}{50}$.

Basic Charge-Control Operation

Two detailed applications follow this section. One provides direct control of a linear regulator, and the other provides control of any external current source.

Gating Current

Figure 1 shows an example of external source gating. With SNS tied to chip ground, the bq2003 enables charge current to the battery by taking MOD high at the start of charging and maintaining this state until charging is terminated. In this example, R7, Q2, R15, and Q1 form the switching circuit. When MOD goes high, Q2 switches on—turning on Q1. When MOD goes low, the base current in Q1 collapses, breaking the charging path.

The current-handling capability of this circuit is limited by the product of the current gains of the transistors and by the 5mA drive capability of the MOD pin.

This limitation may be removed by replacing the PNP at Q1 with a pFET. See Table 1 for suggested transistors.

Table 1. Suggested Transistors (Q1)

Q1	Type	Package	Maximum Current	Maximum Voltage
IRFR9010	pFET	DPAK	5.3	-50
IRFR9022	pFET	DPAK	9.0	-50
IRFR9020	pFET	DPAK	9.9	-50
IRFD9014	pFET	HEXDIP	1.1	-60
IRFD9024	pFET	HEXDIP	1.6	-60
IRF9Z10	pFET	TO-220	4.7	-50
IRF9Z22	pFET	TO-220	8.9	-50
IRF9Z20	pFET	TO-220	9.7	-50
IRF9Z32	pFET	TO-220	15	-50
BD136	PNP	TO-225	1.5	-60
MJE171	PNP	TO-225	3.0	-60
TIP42A	PNP	TO-220	6.0	-60

Note: For very high currents, two paralleled pFETs or an nFET with a high-side driver circuit may be suitable.

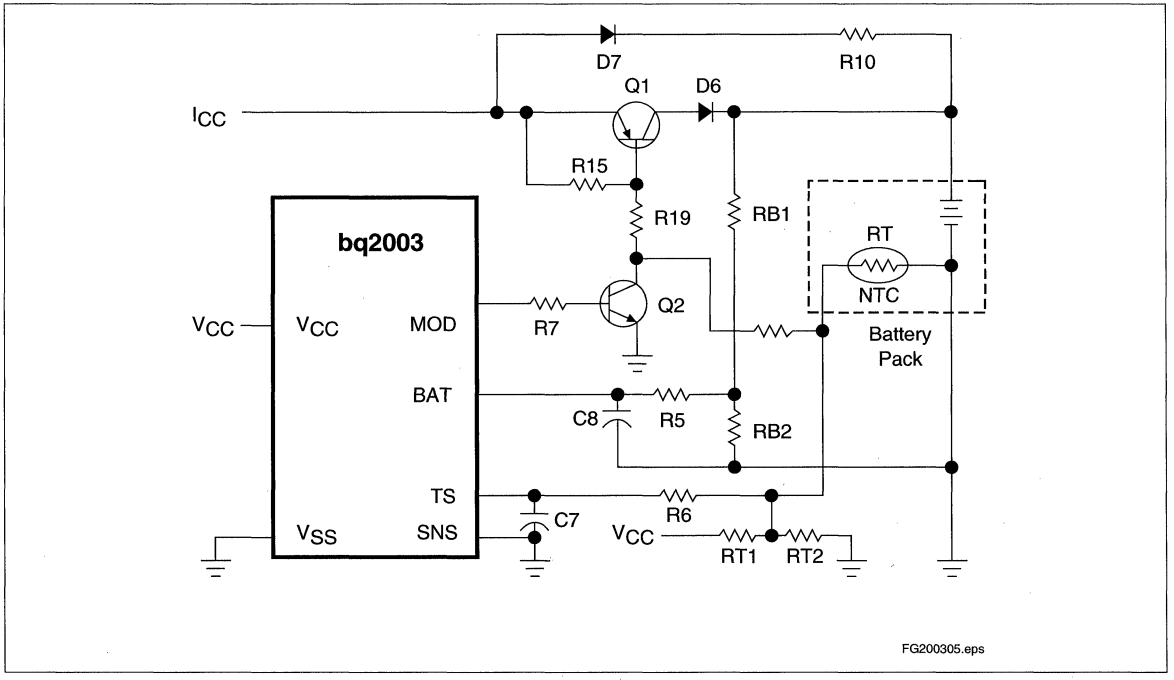


Figure 1. Gated External Source (Bipolar Switch Option)

Charge Status

The charge status of the bq2003 is indicated by two outputs. Each output may directly drive an LED. One LED uses distinctive flashing patterns to indicate the current charger status as:

Charge Action State	Charge Status Output	
	Low	High
Battery absent/abort	-	Continuous
Pending charge (waiting for proper temperature and/or voltage)	1/8 sec	1 3/8 sec
Discharging (optional)	1 3/8 sec	1/8 sec
Fast charging	Continuous	-
Charging complete	1/8 sec	1/8 sec
Top-off (optional)	1/8 sec	1/8 sec

A second LED indicates that the battery temperature detected by the bq2003 and associated thermistor is out of range for fast charging.

Charge Initiation

Charge may be initiated by power to the IC, battery replacement, or application of a digital signal. Configuration options are shown in Figure 2.

Charge initiation by application of power to the IC works as follows: When V_{CC} is applied, the bq2003 is held in reset for approximately one and one-half seconds. At the end of the reset period, the CCMD pin (pin 1) is sampled and, if CCMD and DCMD are low, a charge cycle initiates as soon as conditions allow.

Charge initiation on battery replacement relies on the BAT pin voltage being greater than MCV in the absence of a battery, and falling below MCV when the battery is connected. For example, in Figure 1 a resistor R10 is inserted between the positive battery terminal and I_{DC}. This resistor, in conjunction with RB1 and RB2, is sized to pull the BAT pin (pin 7) above the value programmed on MCV (pin 11, maximum cell voltage threshold) when the battery is removed.

When the battery is replaced in this case, the voltage on BAT should fall below MCV, at which time a charge cycle initiates as soon as conditions allow (if CCMD) and DCMD are low).

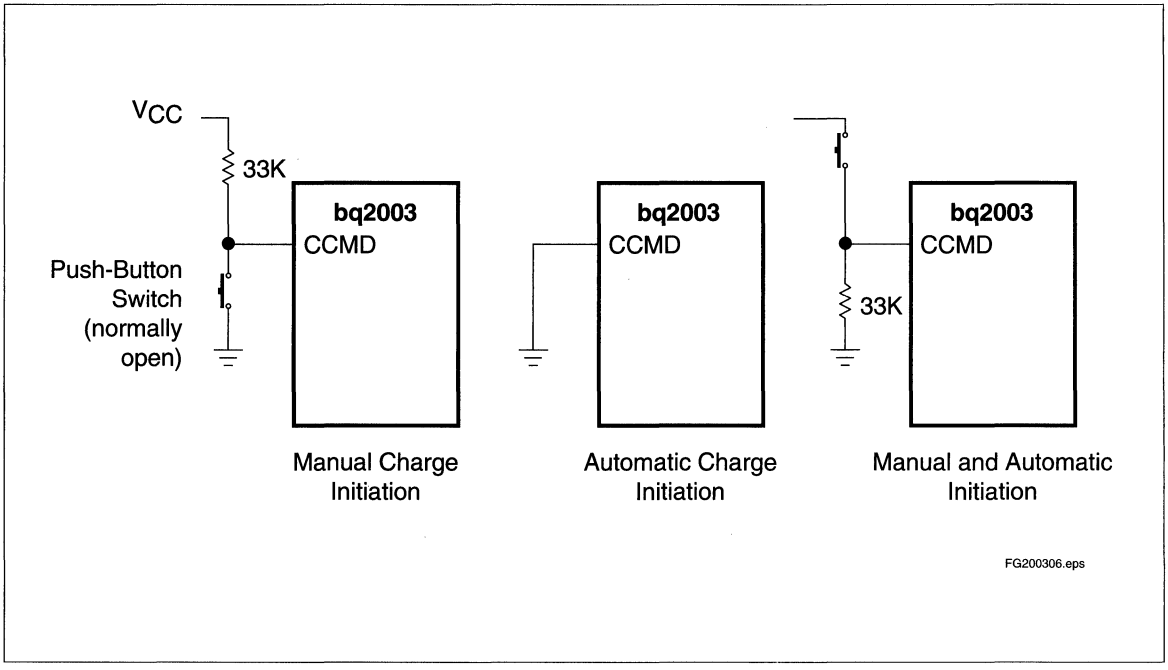


Figure 2. Charge Initiation Network

3/18

Charge initiation by digital signal occurs on the rising edge of CCMD with DCMD low. Digital charge initiation, which is simply a request to charge the battery, results in charging as soon as conditions allow.

The charge command may be issued at any time, but charging may be disqualified because the battery voltage or temperature is outside programmed limits. Fast charging remains pending until all charge qualifications become valid. When conditions allow, fast charging begins. A CCMD-initiated charge with battery absent remains pending until battery replacement.

Discharge-Before-Charge

It may be desirable in the application to allow the user to occasionally discharge the battery to a known voltage level prior to charge. The reason for this may either be to remedy a voltage-depression effect found in some NiCd batteries or to determine the battery's charge capacity.

Figure 3 illustrates the implementation of this function. Discharge-before-charge is initiated on a positive strobe signal on DCMD. **This function takes precedence over a charge action and commences immediately when conditions warrant, forcing DIS to a high state until the voltage sensed on BAT falls below $V_{CC}/5$.** Charging begins as soon as conditions allow.

Care should be taken not to overheat the battery during this process; excessive temperature is not a condition that terminates discharge.

A strobe on CCMD terminates the discharge phase and initiates fast charging.

Unlike a CCMD-initiated charge, the discharge-before-charge function is ignored or terminated when $V_{BAT} - V_{SNS} > V_{MCV}$ (battery removed).

If the discharge-before-charge function is not desired, DCMD should be tied to V_{SS}.

Configuring the BAT Input

The bq2003 uses the battery voltage sense input on the BAT pin to control discharge-before-charge, qualify charge initiation, terminate charge at an absolute limit, and facilitate negative delta voltage (-ΔV) detection.

V_{BAT} may be derived from a simple passive network across the battery. As shown in Figure 1, resistors RB1 and RB2 are chosen to divide the battery voltage down to the optimal detection range, which is between V_{MCV} and $V_{MCV} - 1V$.

For NiCd and NiMH batteries, the battery terminal voltage is divided down to a per-cell potential. If, for example, the battery contains four NiCd cells, RB1 may be chosen as 562KΩ and RB2 as 187KΩ.

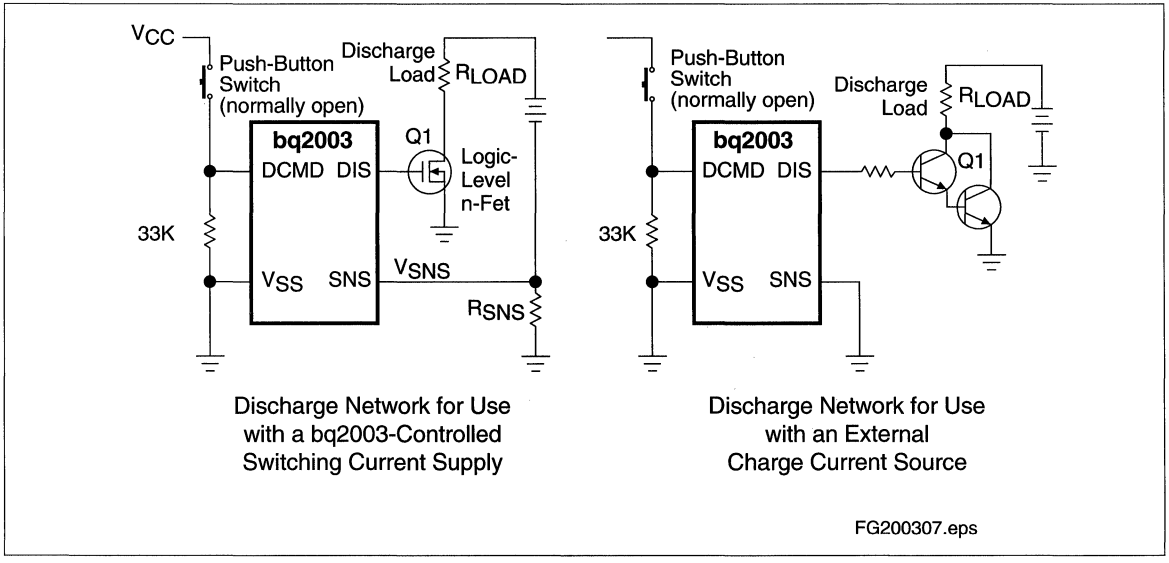


Figure 3. Battery Conditioning Network

Although virtually any value may be chosen for RB1 and RB2 due to the high input impedance of the BAT pin, the values selected must not be so low as to appreciably drain the battery nor so large as to degrade the circuit's noise performance. Constraining the source resistance as seen from BAT between 20KΩ and 1MΩ is acceptable over the bq2003 operating range. Total impedance between the battery terminal and V_{SS} should typically be about 300K Ω to 1MΩ . See Table 2.

Notes: (1) Because V_{SNS} may be positive in bq2003 switching regulation applications, the actual internal comparison uses V_{BAT} – V_{SNS}, or V_{CELL}. This internal value V_{CELL} maintains a representative single-cell voltage independent of any current through R_{SNS}.

(2) The R-C time delay in the presentation of V_{BAT} must be shorter than 200ms (t_{MCV}). A longer delay may result in a failure to determine "battery replaced."

Table 2. Suggested RB1 and RB2 Values for NiCd and NiMH Cells

Number of Cells (V_{BAT} Divisor)	RB1	RB2
4	562 KΩ	187 KΩ
5	649 KΩ	162 KΩ
6	590 KΩ	118 KΩ
8	931 KΩ	133 KΩ
10	953 KΩ	105 KΩ
12	374 KΩ	34 KΩ
14	649 KΩ	49.9 KΩ
16	750 KΩ	49.9 KΩ

Configuring the MCV Input

Battery over-voltage protection is accomplished by comparing V_{CELL} to the voltage on the MCV input pin. If V_{CELL} becomes greater than V_{MCV}, both charging and top-off terminate.

A typical MCV value is 1.8V for NiCd and NiMH batteries. The MCV voltage is derived from either of the networks shown in Figure 4. The combined network has the advantage of fewer resistors in generating both the MCV and TCO thresholds, but loses the independence of threshold adjustment.

To detect the presence of a battery, the DC supply voltage must be larger than MCV * N + V_{LOSST}, where V_{LOSST} is defined as the trickle charging path voltage loss and N is the V_{BAT} divisor.

Temperature Sensing and the TCO Pin

The bq2003 uses the temperature sense input on the TS pin to qualify charge initiation and termination. A negative temperature coefficient (NTC) thermistor referenced to SNS and placed in close proximity to the battery may be used as a temperature-to-voltage transducer as shown in Figure 1. This example shows a simple linearization network constituted by RT1 and RT2 in conjunction with the thermistor, RT. If this temperature sensor is to be used for charge control, it should be directly in contact with the cells.

Temperature-decision thresholds are defined as LTF (low-temperature fault), HTF (hot-temperature fault), and TCO (temperature cutoff). Charge action initiation is inhibited if the temperature is outside the LTF-to-HTF range. In this case, the temperature fault indicator on TEMP is driven low, and charging does not initiate until the battery temperature is within range.

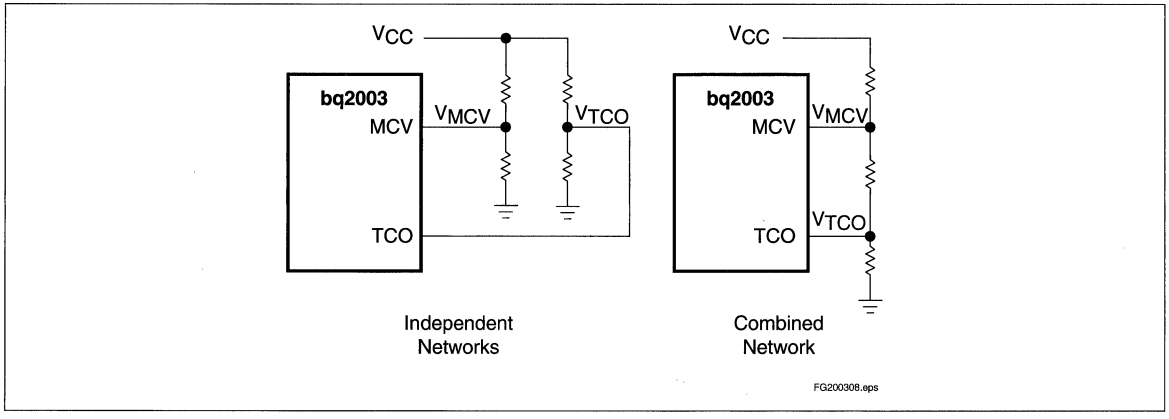


Figure 4. Threshold Networks

Once initiated, charging terminates if the temperature is either less than LTF or greater than TCO. The bq2003 interprets the reference points V_{LTF}, V_{HTF}, and V_{TCO} as V_{SS}-referenced voltages, with V_{LTF} fixed at $\frac{2}{5}$ V_{CC} and V_{TCO} equal to the voltage presented on the TCO pin. See Figure 5. Note that since the voltage on pin TS decreases as temperature increases, V_{TCO} should always be less than $\frac{2}{5}$ V_{CC}. V_{HTF} is set internally $\frac{7}{8}$ of the way from V_{LTF} to V_{TCO}. The resistive dividers shown in Figure 4 may be used to generate the desired V_{TCO}.

Note: HTF is not meaningful for bq2003 switching current regulation chargers. See the Application Note, "Step-Down Switching Current Regulation Using the bq2003 Fast Charge IC."

$\Delta T/\Delta t$ detection adds an additional constraint on the selection of temperature sense components. Detection occurs when the voltage TS – SNS declines at a rate between 0.0024 V_{CC} and 0.0040 V_{CC} per 68 seconds, with a nominal 5V V_{CC} producing a nominal detection rate of 14mV/min (16mV/68sec). For example, assuming a 1°C/min desired average $\Delta T/\Delta t$ detection rate ($T_{\Delta T}$), and minimum and maximum charge temperatures of 0° and 40°C, respectively, V_{TCO} equals:

$$V_{TCO} = (2 * V_{CC}/5) - (0.0028 * V_{CC} * (T_{TCO} - T_{LTF}))$$

$$= 2 - (0.014 * (40 - 0))$$

$$= 1.44V$$

Table 3 shows the temperature control values that apply for Application Examples 1 and 2, assuming the Fenwal part number 197-103LA6-A01 thermistor. Appendix A explains the derivation of such component values.

New $\Delta T/\Delta t$ samples are processed every 34 seconds. To minimize the risk of premature termination, the design should be configured assuming a minimum charge cutoff rate of 0.0024 * V_{CC}, or 10.6mV per minute (at 25°C; V_{CC} = 5V). This is the lowest signal that may be recognized as meeting the decision threshold. Repeating samples cause a decision quickly as the voltage ramps between this minimum threshold and the nominal 14mV per minute. The system is self-compensating in that the thermistor provides increasingly overstated negative voltage change with increasing temperature, making the measurement more sensitive at higher temperatures. The last three columns of Table 3 are an example of this relationship.

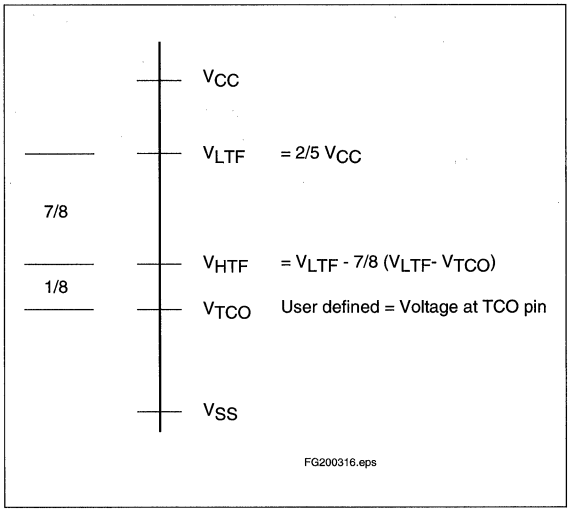


Figure 5. Temperature Reference Points

Table 3. Example Values, Temperature Sense Network

LTF (°C)	HTF (°C)	TCO (°C)	V_{TCO} (V)	RT1 (KΩ)	RT2 (KΩ)	$T_{\Delta T}$ (°C/min)	Minimum-to-Nominal $\Delta T/\Delta t$ Rate (°C/min) @ 25°C	@ 35°C	@ 45°C
10	47	50	1.50	3.65	2.80	1.04	0.94–1.26	0.75–1.00	0.64–0.85

Notes:
1. V_{SR} = 0V.
2. Temperature control and qualification may be disabled by tying pin TCO to V_{SS} and fixing the voltage on pin TS to 0.1 * V_{CC}.

V_{CC} Supply

The V_{CC} supply provides both power and voltage reference to the bq2003. This reference directly affects BAT voltage and internal time-base voltage measurements.

A 5% or tighter tolerance on V_{CC} is recommended to minimize the error regarding MCV. For example, if MCV nominal is set to be 1.8V per cell, a 5% error on V_{CC} results in MCV = 1.71V to 1.89V. This range is acceptable from the perspective that an MCV charge termination represents a faulty battery. The minimum MCV must be safely above a "healthy" charging voltage. The maximum MCV must satisfy the requirement to recognize battery removed/replaced (see the section, "Configuring the MCV Input").

The time-base is trimmed during manufacturing to within 5 percent of the typical value with V_{CC} = 5V. The oscillator varies directly with V_{CC}. If, for example, a 5% regulator supplies V_{CC}, the time-base could be in error by as much as 10%.

Trickle Resistor

The trickle resistor, R10, is sized to limit the constant trickle current, I_T.

$$R10 = (V_{DC} - V_{BAT}) / I_T$$

The resistance of R10 is calculated using I_T = charge current desired after full (typically a $\frac{1}{20}$ to $\frac{1}{50}$ rate, possibly less) and the voltage for a fully charged battery (number of cells * 1.4V).

The wattage rating of R10 must accommodate periods of higher I_T when V_{BAT} is at a lower voltage (no fast-charge pending charge qualification).

A very low trickle current contributes to longer battery life, and is particularly critical for NiMH cells.

Top-Off Charge

The top-off charge option allows for the self-discharge replacement trickle current to be very low, but still provides for filling up the last fraction of capacity after the fast-charge phase has terminated. Top-off occurs at a $\frac{1}{8}$ pulsed rate to prevent excess heat generation, and terminates after a period equal to the safety time-out. It also terminates if TCO or MCV is detected.

Top-off is not recommended in applications where a battery charge is re-initiated with extremely high frequency (many times per day); for example, when the unit is returned to the charge cradle after each short period of use.

Negative Delta Voltage Fast-Charge Detection

-ΔV full-charge detection may operate in parallel with the ΔT/Δt detection. If temperature control is disabled by design, then -ΔV should be enabled (DVEN to V_{CC}). If -ΔV is enabled, a constant-current charging source is required. Otherwise a drop in current may cause a false -ΔV determination. DVEN may change state at any time.

Mode Selection Pins TM1 and TM2

These two pins are used to select the safety time-out (5 selections, 23 to 360 minutes) and optional top-off charge (4 selections, 23 to 180 minutes, equal to the safety time selection).

The safety time-out should be selected to be longer than any reasonably expected charge time. The nominal charge time (Ahr capacity/charge rate) must be factored up to allow for both charge inefficiency and the fact that many batteries hold more than the rated charge. A safety time-out 1.3–1.5 times the nominal time is normally adequate (i.e., 90 minutes for a 1C charge). The safety time-out may be far in excess of the nominal charge time if the temperature monitor is enabled.

Note: If the charge rate varies (such as fast charging during system operation using ΔT/Δt termination), then the safety time-out selection should allow for the slowest charges that may occur. The 180- or 360-minute selection may be appropriate.

System-Controlled Charge Inhibition

Some in-system chargers may require the ability to block fast charge activity when the system is on.

Two small 1N4148-type diodes—with cathodes connected outside the R-C filter—control the bq2003 BAT and TS inputs to provide this capability. A high signal (INHIBIT) applied to anodes of these diodes blocks charge activity. See Figure 8.

With a high signal applied to BAT and TS, charge is inhibited and both LEDs are off. INHIBIT must be high for longer than t_{MCV} max (300ms) if a subsequent low state is to initiate charge.

INHIBIT could be the system V_{CC}, blocking fast charge at all times the system is ON. This may be needed if -ΔV termination is to be used and the charge supply cannot simultaneously support fast charge and peak system loads.

INHIBIT might also be CPU-controlled, allowing the charger to be inhibited as required by specific situations.

Power Supply Selection

The DC supply voltage, V_{DC}, must satisfy two requirements:

1. To support the bq2003 V_{CC} supply, V_{DC} must be adequate to provide for 5V regulation after the losses in the regulator and across D1 ($V_{DC} \geq 7.7V$ using the 78L05).
2. To support the charge operation, V_{DC} > (number of cells * MCV_{MAX}) + V_{LOSS} in the charging path. (MCV_{MAX} is the maximum cell voltage threshold with the maximum bq2003 V_{CC}.)

Polarity Reversal Protection

If the DC input has any risk of being accidentally connected with power (+) and ground (–) reversed, then the system input should include either a protection diode to protect against circuit damage or a diode bridge to provide both protection and operation. This also increases minimum input voltage for charger operation by approximately 1V to 2V.

Layout Guidelines

PCB layout to minimize the impact of system noise on the bq2003 is important when the bq2003 is used as a switching modulator, with a separate nearby switching regulator, or close to any other significant noise source.

1. Avoid mixing signal and power grounds by using a single-point ground technique incorporating both a small signal ground path and a power ground path.
2. The charging path components and associated traces should be kept relatively isolated from the bq2003 and its supporting components.
3. 0.1µF and 10µF decoupling capacitors should be placed close together and very close to the V_{CC} pin.
4. 0.1µF capacitors and resistors forming R-C filters connected to pins BAT, TS, TCO, and MCV should be as close as possible to their associated pins.
5. Because the bq2003 uses V_{CC} for its reference, additional loading on V_{CC} is not recommended.
6. Diode D1 (1N4148) is recommended for rectification and filtering.
7. If the DCMD input is electronically controlled, care should be taken to prevent noise-induced false transitions.
8. For bq2003-modulated switching applications:
   - A 2KΩ resistor is required between the MOD pin and the transistor.
   - A 1000pF capacitor/1KΩ resistor R-C filter should be as close as possible to the SNS pin.
   - The 0.1µF capacitors for BAT and TS should be routed directly to SNS and not to ground.

Figures 6 and 7 show an example layout of the non-power path circuits in the "kernel board" available from Benchmarq. Figure 8 is a schematic of the board. Table 4 contains the parts list for the board. A comparable layout is recommended.

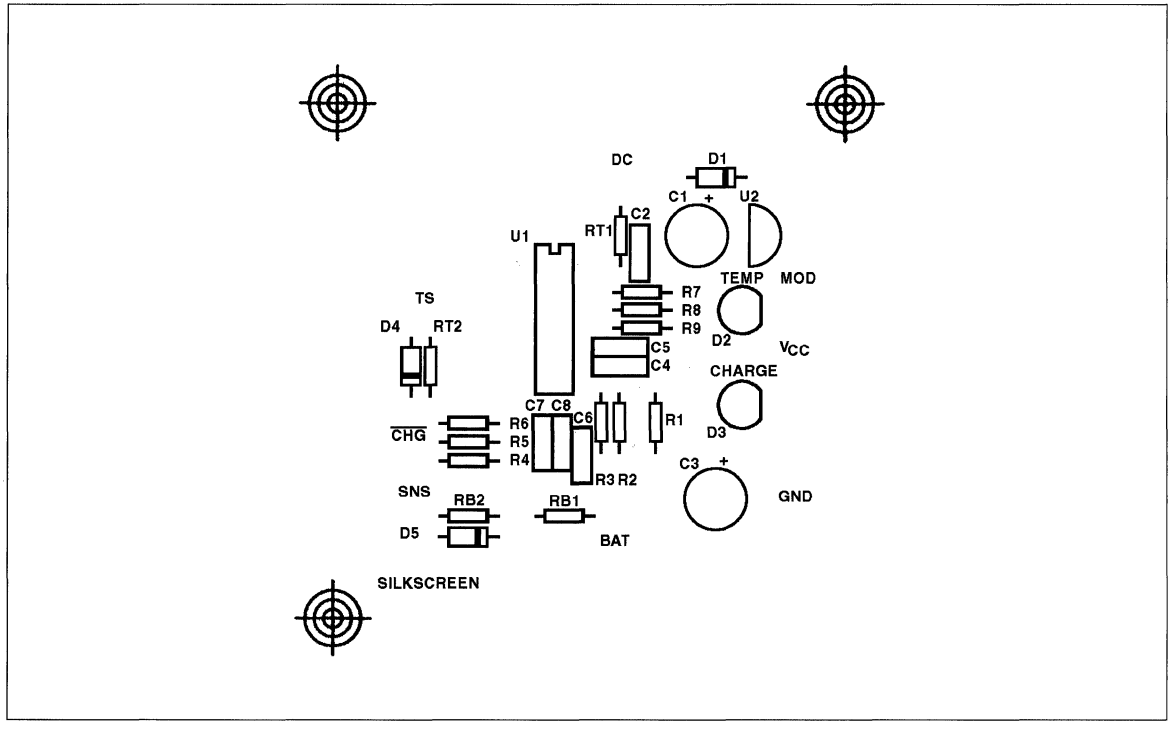
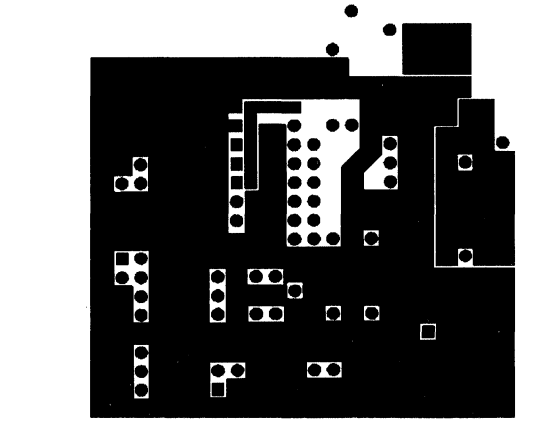
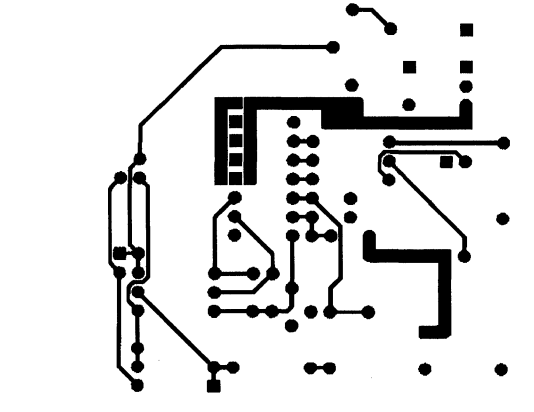


Figure 6. bq2003 Kernel Board Layout, Component Placement

9/18



Layer 1 Component Side



Layer 2 Solder Side

Figure 7. bq2003 Kernel Board Layout

Table 4. bq2003 Kernel Board Parts List

Component Name	Component Description
C1	10µF 50V electrolytic
C2, C4, C5, C7, C8	0.1µF ceramic
C3	10µF 7V electrolytic
C6	1000pF ceramic
D1, D4, D5	1N4148
D2, D3	HLMP 4700 red LED
R1	User-defined 1% ¼W or ⅛W carbon film
R2	User-defined 1% ¼W or ⅛W carbon film
R3	User-defined 1% ¼W or ⅛W carbon film
R4, R7, R8, R9	1KΩ 5% ¼W or ⅛W carbon film
R5, R6	100KΩ 5% ¼W or ⅛W carbon film
RB1	User-defined 1% ¼W or ⅛W carbon film
RB2	User-defined 1% ¼W or ⅛W carbon film
RT1	User-defined 1% ¼W or ⅛W carbon film
RT2	User-defined 1% ¼W or ⅛W carbon film
U1	bq2003
U2	LM78L05ACZ

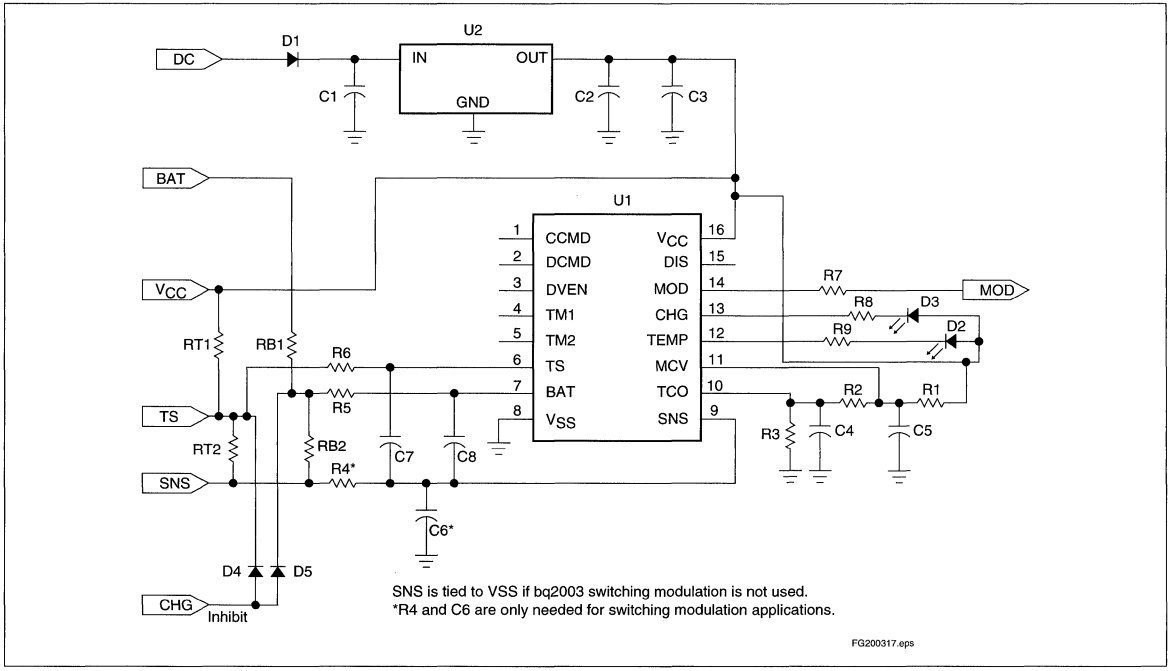


Figure 8. bq2003 Kernel Board Schematic

11/18

Application Example 1: Linear Regulator

In the example in Figure 9, the bq2003 is used to implement a linear regulator/charge controller that can charge 4 to 12 NiCd or NiMH cells with current regulated up to 1.5A. R_{16} determines the charge rate per the formula:

$$I = 1.25V / R_{16}$$

Charge is initiated on battery replaced or V_{CC} valid. -ΔV detection is enabled (DVEN high), and discharge control is disabled (DCMD low). MCV = 1.8V; LTF = 10°C; HTF = 47°C; TCO = 50°C; $T_{\Delta T}$ (average ΔT/Δt) = 1.04°C/ minute. Timer-mode selection (see data sheet) and trickle resistor R10 selection (see page 7) are determined by the designer.

Components to complete this schematic may be selected from the preceding table:

- Table 2: BAT network RB1 and RB2 values

Table 5 contains the parts list for the board.

Notes: (1) Temperature control and qualification may be disabled by tying pin TCO to V_{SS} and fixing the voltage on pin TS to 0.1 * V_{CC}.

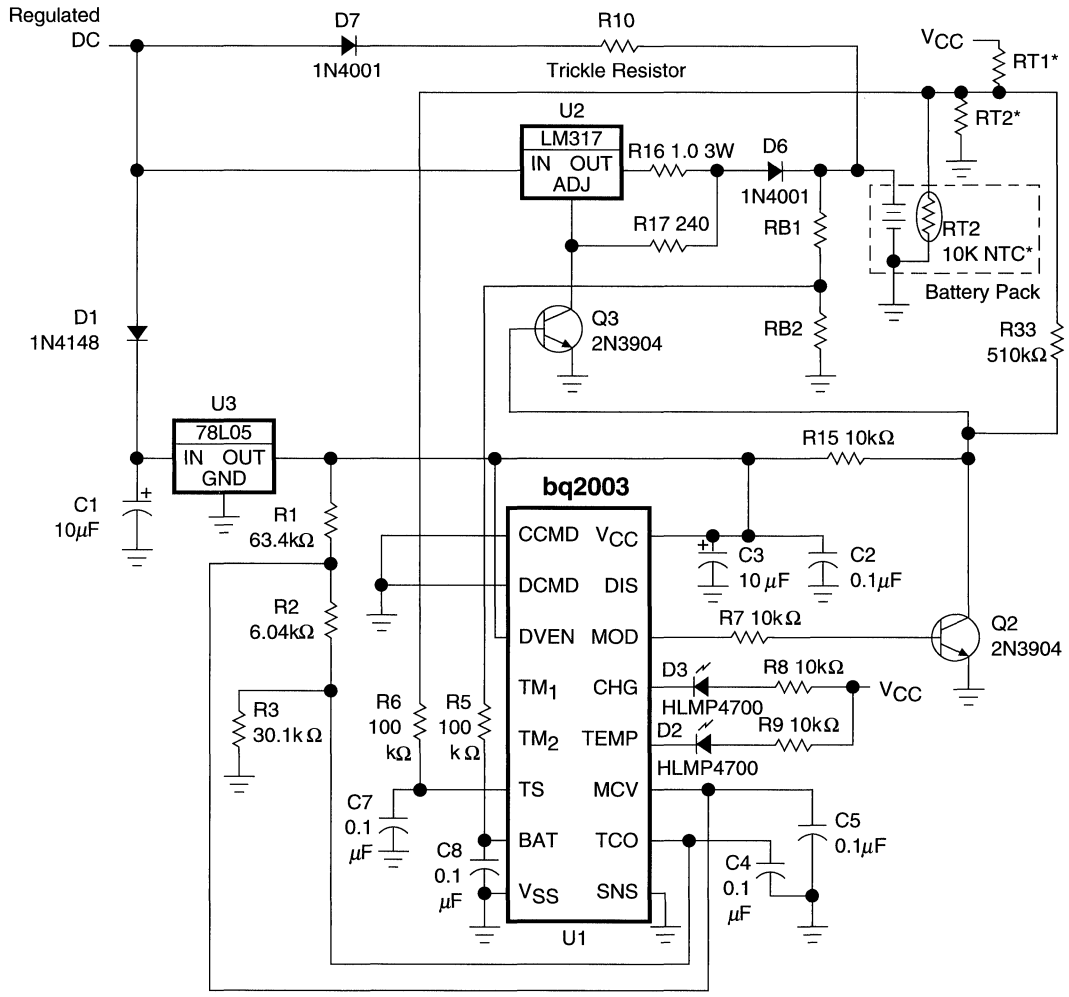
(2) The voltage drop (V_{LOSS}) across LM317, D6, and R16 is 4.25V minimum. The charging supply voltage must be greater than the following:

Number of cells * max. cell voltage + V_{LOSS}

The maximum allowable power loss across the LM317 depends on the heat sinking.

Table 5. Linear Regulator/Charge Controller Board Parts List

Component Name	Component Description
C1	10µF 50V electrolytic
C2, C4, C5, C7, C8	0.1µF ceramic
C3	10µF 7V electrolytic
D1	1N4148 or equivalent
D2, D3	HLMP 4700 red LED
D6	1N5400
D7	1N4001
Q2, Q3	2N3904
R1	63.4KΩ 1% ¼W or ⅛W carbon film
R2	6.04KΩ 1% ¼W or ⅛W carbon film
R3	30.1KΩ 1% ¼W or ⅛W carbon film
R5, R6	100KΩ 5% ¼W or ⅛W carbon film
R7, R15	10KΩ 5% ¼W or ⅛W carbon film
R8, R9	1.0KΩ 5% ¼W or ⅛W carbon film
R10	User-defined 5% carbon film
R16	1Ω 1% 3W carbon film
R17	240Ω 5% ¼W or ⅛W carbon film
R33	510KΩ 5% ¼W or ⅛W carbon film
RB1	User-defined 1% ¼W or ⅛W carbon film
RB2	User-defined 1% ¼W or ⅛W carbon film
RT	Negative temperature coefficient (NTC) thermistor (see Figure 9)
RT1	1% ¼W or ⅛W carbon film (see Figure 9)
RT2	1% ¼W or ⅛W carbon film (see Figure 9)
U1	bq2003
U2	LM317T
U3	LM78L05ACZ



TM1, TM2: To V_{CC}, V_{SS}, or float as required. DIS: No connect.
The R-C filters on MCV and TCO are recommended in noisy environments.

*NTC, RT1, and RT2: Thermistor	RT1	RT2
Keystone RL0703-5744-103-S1	3.57K	2.67K
Philips 2322-640-63103	3.65K	2.80K
Fenwal Type 16, 197-103LA6-A01	3.65K	2.80K

FG200309.eps

Figure 9. Linear Regulator/Charge Controller

13/18

Application Example 2: Gated External Current Source

In the example in Figure 10, the bq2003 is used to gate an external current-limited or regulated charge source that can charge NiCd or NiMH cells.

Charge is initiated on battery replaced or V_{CC} valid. -ΔV detection is enabled (DVEN high), and discharge control is disabled (DCMD low). MCV = 1.8V; LTF = 10°C; HTF = 47°C; TCO = 50°C; $T_{\Delta T}$ (average $\Delta T/\Delta t$) = 1.04°C/ minute. Timer-mode selection (see data sheet) and trickle resistor R10 selection (see page 7) are determined by the designer.

Components to complete this schematic may be selected from these preceding tables:

- Table 1: Power switch Q1
- Table 2: BAT network RB1 and RB2 values

Table 5 contains the parts list for the board.

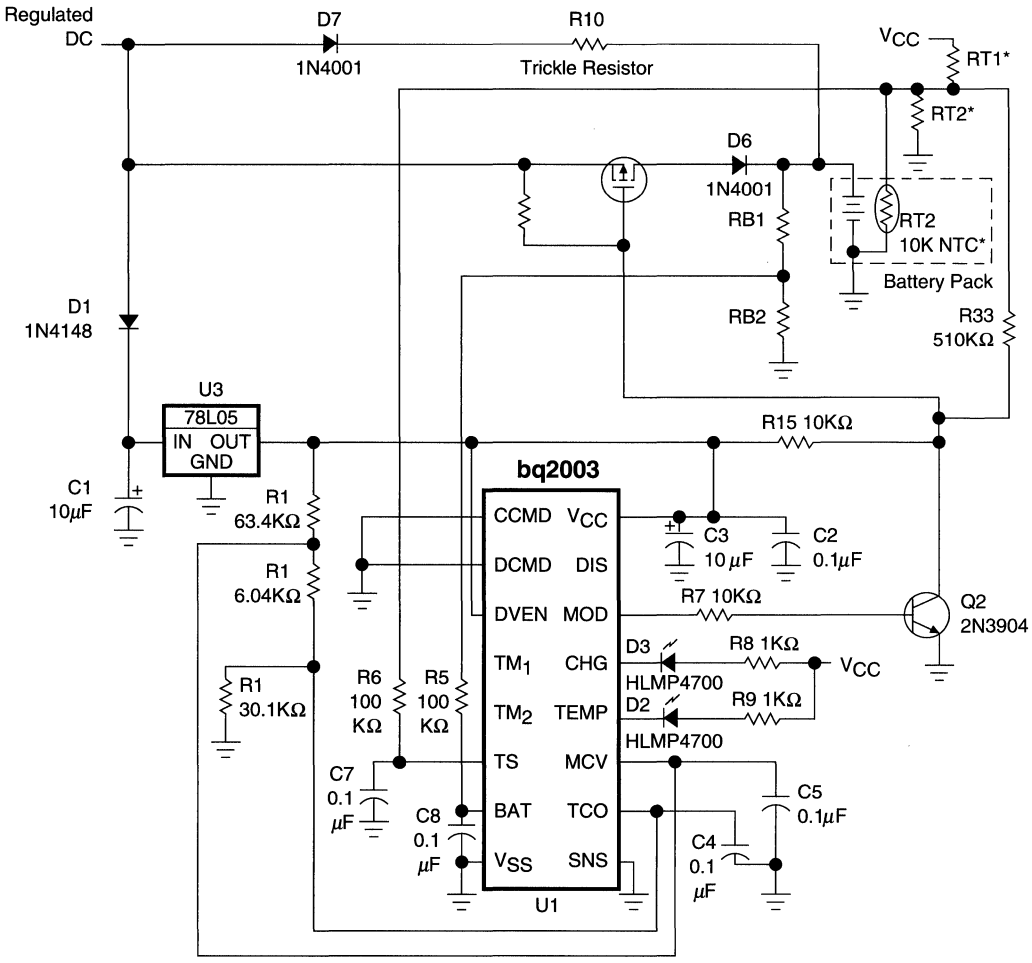
Notes: (1) Temperature control and qualification may be disabled by tying pin TCO to V_{SS} and fixing the voltage on pin TS to 0.1 * V_{CC}.

(2) The charging supply voltage must be greater than the following:

Number of cells * max. cell voltage + V_{LOSS}

Table 6. Gated External Current Source Board Parts List

Component Name	Component Description
C1	10µF 50V electrolytic
C2, C4, C5, C7, C8	0.1µF ceramic
C3	10µF 7V electrolytic
D1	1N4148 or equivalent
D2, D3	HLMP 4700 red LED
D6	1N5400
D7	1N4001
Q1	User-defined pFET
Q2	2N3904
R1	63.4kΩ 1% ¼W or ⅛W carbon film
R2	6.04kΩ 1% ¼W or ⅛W carbon film
R3	30.1kΩ 1% ¼W or ⅛W carbon film
R5, R6	100kΩ 5% ¼W or ⅛W carbon film
R7	10kΩ 5% ¼W or ⅛W carbon film
R8, R9, R15	1kΩ 5% ¼W or ⅛W carbon film
R10	User-defined 5% carbon film
RB1	User-defined 1% ¼W or ⅛W carbon film
RB2	User-defined 1% ¼W or ⅛W carbon film
RT	Negative temperature coefficient (NTC) thermistor (see Figure 10)
RT1	1% ¼W or ⅛W carbon film (see Figure 10)
RT2	1% ¼W or ⅛W carbon film (see Figure 10)
U1	bq2003
U3	LM78L05ACZ



TM1, TM2: To V_{CC}, V_{SS}, or float as required. DIS: No connect.
The R-C filters on MCV and TCO are recommended in noisy environments.

*NTC, RT1, and RT2: Thermistor	RT1	RT2
Keystone RL0703-5744-103-S1	3.57K	2.67K
Philips 2322-640-63103	3.65K	2.80K
Fenwal Type 16, 197-103LA6-A01	3.65K	2.80K

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Figure 10. Gating External Current Source

15/18

Appendix A
Determining Temperature-Control Component Values

The bq2003 uses a negative temperature coefficient (NTC) thermistor to determine temperature. The ΔT/Δt sensitivity can be adjusted using different resistor values (RT1 and RT2 in Figure 1 and Application Examples 1 and 2) and a different high-temperature cutoff voltage. Table A-1 lists various thermistor manufacturers, with the appropriate part numbers.

Follow these steps to determine temperature-control component values (see Figure 5 on page 6):

1a. The low-temperature fault (LTF) limit for charging must be established. LTF for charging is determined by the battery specification and the charge rate used. A typical value for the low-temperature limit is 10°C.

b. V_{LTF} is set within the bq2003 at $0.4 * V_{CC}$.

2a. The high-temperature cutoff (TCO) for charging must be established. TCO for charging is determined by the battery specification, the charge rate, and the heat dissipation of the system. Typical values range from 40°C to 50°C, although values outside this range may be applicable.

b. The average ΔT/Δt sensitivity from LTF to TCO ($T_{\Delta T}$, expressed as °C/minute) for termination must be established. As mentioned in this application note, the bq2003 provides a typical ΔT/Δt charge termination of 14 mV per minute. The $T_{\Delta T}$ value is determined by the battery specification, the charge rate, and the heat dissipation of the system. Typical nominal values for $T_{\Delta T}$ range from 0.75°C/min to 1.5°C/min.

Relative to the average value $T_{\Delta T}$, the minimum-to-maximum range of ΔT/Δt at a specific temperature depends on two parameters:

- The measurement resolution of the bq2003, which contributes a ±25% error.
- The non-linearity of the thermistor between LTF and TCO. As the temperature nears LTF, the expected ΔT/Δt is less than $T_{\Delta T}$ (less sensitive), and as the temperature nears TCO, the expected ΔT/Δt is more than $T_{\Delta T}$ (more sensitive).

The ΔT/Δt range should be considered in determining the nominal $T_{\Delta T}$. Nominal $T_{\Delta T}$ should be selected so that its minimum value represents an acceptable (non-premature) termination threshold. Thus a first bq2003 sample does not cause a premature termination. Multiple sampling ensures that the termination occurs well before the $T_{\Delta T}$ max.

c. The high-temperature cutoff voltage, V_{TCO}, must be established. This V_{TCO} limit is determined by the $T_{\Delta T}$ and may be calculated by:

$$V_{TCO} = 2 * {}^{V_{CC}}/_{5} - 0.0028 * V_{CC} * (TCO - LTF)/T_{\Delta T}$$

V_{TCO} is provided at the TCO pin by a resistor-divider network as shown in Figures 9 and 10: $V_{TCO} = V_{CC} * R3 / (R1 + R2 + R3)$. In this arrangement, R1 and R2 are selected such that $MCV = V_{CC} * (R2 + R3) / (R1 + R2 + R3)$.

4. Select the thermistor to be used. If it is not from Table A-1, the thermistor sensitivity at 25°C should be at least -4% and the ΔR steps between 30oC and 50oC should be comparable to or greater than those in Table A-1 to obtain the appropriate accuracy. Lower values affect the linearity of the ΔT/Δt.

5. Determine the thermistor resistance at LTF and TCO (R_{LTF} and R_{TCO}, respectively). This may be done using the thermistor temperature versus resistance conversion table provided with the thermistor specification. These tables are usually in 5°C increments.

6. The values for RT1 and RT2 may be calculated by:

$$T1 = R_{LTF} * (1 - (2 / V_{CC})) / (2 / V_{CC})$$

$$T2 = R_{TCO} * (1 - (V_{TCO} / (V_{CC} - V_{SNS}))) / (V_{TCO} / (V_{CC} - V_{SNS}))$$

$$RT2 = ((T2 * R_{LTF}) - (T1 * R_{TCO})) / (T1 - T2)$$

$$RT1 = (RT2 * T1) / (R_{LTF} + RT2)$$

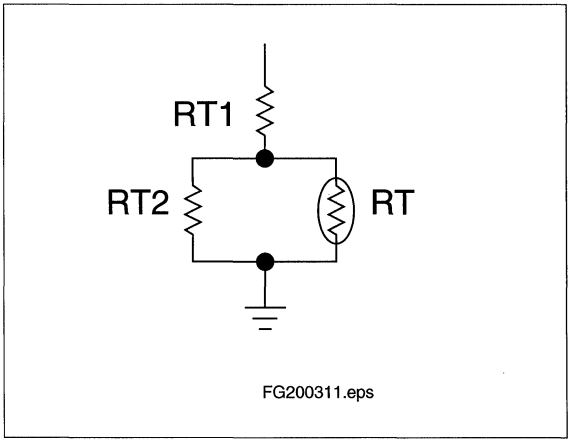


Figure A-1. Resistor Network

Table A-1. 10K NTC Thermistor Types and Resistance Values

Temperature (°C)	Nominal Resistance (Ω) at Temperature			
	Keystone Carbon Co. RL0703-5744-103-S1 (Tel: 814/781-1591)	Philips Components 2322-640-63103 (Tel: 407/743-2112)	Fenwal Electronics Type 16; 197-103LAG-A01 (Tel: 508/478-6000)	Thermometrics C100Y103J (Tel: 908/287-2870)
-30	188172	173900	177000	-
-25	138043	128500	-	-
-20	102263	95890	970700	-
-15	76461	72230	-	-
-10	57672	54890	55330	-
-5	43864	42070	-	-
0	33630	32510	32650	29588
5	25988	25310	-	23515
10	20243	19860	19900	18813
15	15889	15690	-	15148
20	12562	12490	12490	12271
25	10000	10000	10000	10000
30	8013	8060	8057	8195
35	6461	6536	-	6752
40	5241	5331	5327	5593
45	4276	4373	-	4656
50	3507	3606	3603	3894
55	2894	2989	-	3273
60	2400	2490	2488	2762
65	2001	2085	-	2342
70	1677	1753	1752	1993.7
75	1412	1481	-	1704.0
80	1194	1256	1258	1462.0
85	1014	1070	-	1259.1
90	865.2	915.5	917.7	1088.3
95	741.0	786.1	-	943.9
100	636.9	677.5	680.0	821.4

Application Note Revision History

Change No.	Page No.	Description	Nature of Change
1	13, 15	Changed thermistor values on Figures 9 and 10	Correction
1	12-15	Added component R33 to Figure 9 and Table 5 and R33 and D17 to Figure 10 and Table 6	Correction for cold temperature charge initiation
1	15	Corrected R1 value	Was 6.34K; is 63.4K
2	13	Corrected R1, R2, and R3 labels	Were all R1

Note: Change 1 = Dec. 1992 B changes from Oct. 1992 A.

Change 2 = May 1999 C changes from Dec. 1992 B.

UNITRODE

U-506 Step-Down Switching Current Regulation Using the bq2003 Fast-Charge IC

3

Introduction

This application note describes the use of the bq2003 Fast-Charge IC as the modulator in a buck-type switch-mode regulator to fast charge NiCd and NiMH batteries. Please refer to the application note entitled "Using the bq2003 to Control Fast Charge" for a discussion of bq2003 charge control operation and for descriptions of non-switch-mode applications that gate current-limited sources to control battery charging.

Examples for additional applications are being developed. Please contact Unitrode if your application is not supported by one of these examples.

The bq2003 is targeted for applications requiring state-of-the-art fast-charging performance at minimal cost. It provides sophisticated full-charge detection techniques such as $\Delta T/\Delta t$ (delta temperature/delta time) and $-\Delta V$ (negative delta voltage) that enable the user to take advantage of advanced battery technologies such as nickel metal-hydride (NiMH) and high-capacity fast-charge nickel cadmium (NiCd). Systems using the bq2003 can be easily upgraded from NiCd batteries to NiMH batteries without system redesign.

Background

The bq2003 may serve as a controller to provide a switch-mode current source configuration for battery charging. Switch-mode current source regulation is much more efficient than linear current-limited regulators.

The electrical and thermal requirements of the application determine the configuration used with the bq2003. If the charge supply is either current- or power-limited at a level compatible with fast charging the battery, switch-mode operation may not be needed. The use of a gated current configuration as described in "Using the bq2003 to Control Fast Charge" is most likely more economical.

If the charge current in a switch-mode application is less than 3A, a p-channel MOSFET buck-type power stage is generally recommended. This is desirable because of the minimal number of support components required for the bq2003. If the switch-mode charge current is above 3A, using an n-channel FET may be more economical. Several small signal support components must be added for gate drive of the n-channel MOSFET.

Thermal packaging requirements are often the practical limits in electronic design. Basic thermal management or component thermal stress/reliability issues can affect an otherwise successful product. The use of switching power-conversion techniques results in dramatically less heat being generated in the product.

A comparison of power loss demonstrates the advantage of switch-mode control versus linear control. Either may be used to charge a four-C-cell NiCd battery pack from a 12V DC source at a rate of 2A. Loss in the switch-mode circuit may be held below 2W, whereas loss in the linear circuit can be above 12W.

Operational Aspects

In Figures 1 and 2, the bq2003 MOD pin controls the switching transistor Q1. In the switch-mode operation, the SNS pin is driven by the high side of the sense resistor R26. The current waveform of the inductor is represented by a voltage waveform across R26. MOD transitions from high to low after SNS ramps up to 0.250V and from low to high after SNS ramps down to 0.220V. This action sustains a self-referenced oscillation about these two thresholds.

Both V_{TS} and V_{BAT} are referenced to V_{SNS} by an internal A-to-D converter. For this reason, both the TS and BAT pins must be well-coupled to SNS using the associated capacitors (C7 and C8) and resistors (R5 and R6). If the waveforms at TS and BAT are viewed with an oscilloscope, the AC content found at SNS is seen at TS and BAT. This is normal.

A resistor (R7) is placed in series with the Q3 gate to drive a small signal-switching FET, Q3. Internal bq2003 noise is lowered with this resistor in place.

V_{LTF}, V_{HTF}, and V_{TCO} are voltage-reference points monitored on the TS pin to qualify charge initiation and termination on temperature. Operation of the bq2003 in a non-switch-mode application is described fully in the application note entitled "Using the bq2003 to Control Fast Charge."

When the bq2003 is used as a switch-mode controller, the application of these reference points is somewhat different:

- Prior to charge initiation, $V_{SNS} = V_{SS}$.
- While charging, V_{SNS} (average) = 0.235V.

Because the bq2003 internal A-to-D converter measures differentially between V_{TS} and V_{SNS}, component selection for temperature qualification of charge initiation must be done assuming V_{SNS} = 0V, and component selection for temperature qualification of charge termination must be done assuming V_{SNS} = 0.235V.

V_{TS} is the voltage at the node of RT1, RT2, and the thermistor. The voltage is derived from reference V_{CC} (5V) by RT1 connected to V_{CC} and RT2 in parallel with the thermistor connected to SNS. Prior to charging, the voltage being divided is V_{CC}. When switching regulation is active, the bottom side of RT2 and the thermistor is biased positively by 0.235V, reducing the reference voltage to 4.65V.

Because V_{TCO} and V_{LTF} are both referenced to V_{CC}, V_{TS} for a particular temperature represents a colder temperature when the switch-mode is inactive than when the switch-mode is active. This effect could negate the HTF charge initiation qualification threshold. V_{HTF} is $\frac{1}{8} * V_{LTF} + \frac{7}{8} * V_{TCO}$. V_{TCO} is a threshold selected for use when the switch-mode is active. V_{LTF} is internally fixed at 0.4* V_{CC}. The values of RT1, RT2, and the thermistor that define the LTF temperature (charging off) also define the TCO temperature (switch mode on). The resulting HTF temperature with charging off approaches or may even be above the TCO temperature (switch mode on), limiting the uselfulness of HTF to qualify the start of charge.

The bq2003 bQuick™ design disk is available to optimize these component values and thresholds for specific application objectives.

P-Channel MOSFET Buck-Topology Switch-Mode Charger

In this example, the bq2003 is used to implement a switching regulator/charge controller that can charge 4 to 12 NiCd or NiMH cells with current regulated up to 3A.

Figure 1 is a standard configuration for a pFET switch-mode charger. MOD drives a small signal DMOS FET, Q3. When MOD is high, Q3 is on, turning on Q1 via the path through D8 and D9.

L1 inductor current ramps up linearly while MOD is high. L1 current is in series with the battery and R26. The resulting voltage across R26, V_{SNS}, is delivered via R4 to C6 at the SNS pin. The L1 inductor current ramps up linearly until V_{SNS} reaches 0.250V, at which time MOD goes low and Q1 turns off. A flux reversal occurs in L1, causing D10 to conduct. Charge is now being transferred from L1 into the battery. The L1 current ramps down linearly until V_{SNS} reaches 0.220V. At this point the cycle repeats with MOD going high.

For input voltages that are higher than the rated Q1 safe operating gate voltage, Zener diode D9 can be placed in series with the drain lead of Q3. The Zener voltage should be sized to allow full Q1 enhancement while Q3 is conducting. See Table 1.

Capacitor C9 is used to provide a low-impedance for the Q1 source lead. Without C9 in place, Q1 can be connected to an overly inductive voltage supply. D6 is a blocking diode that keeps the battery from discharging via U2 during removal of the DC power source input.

Table 1. Lookup Table for D9 Selection

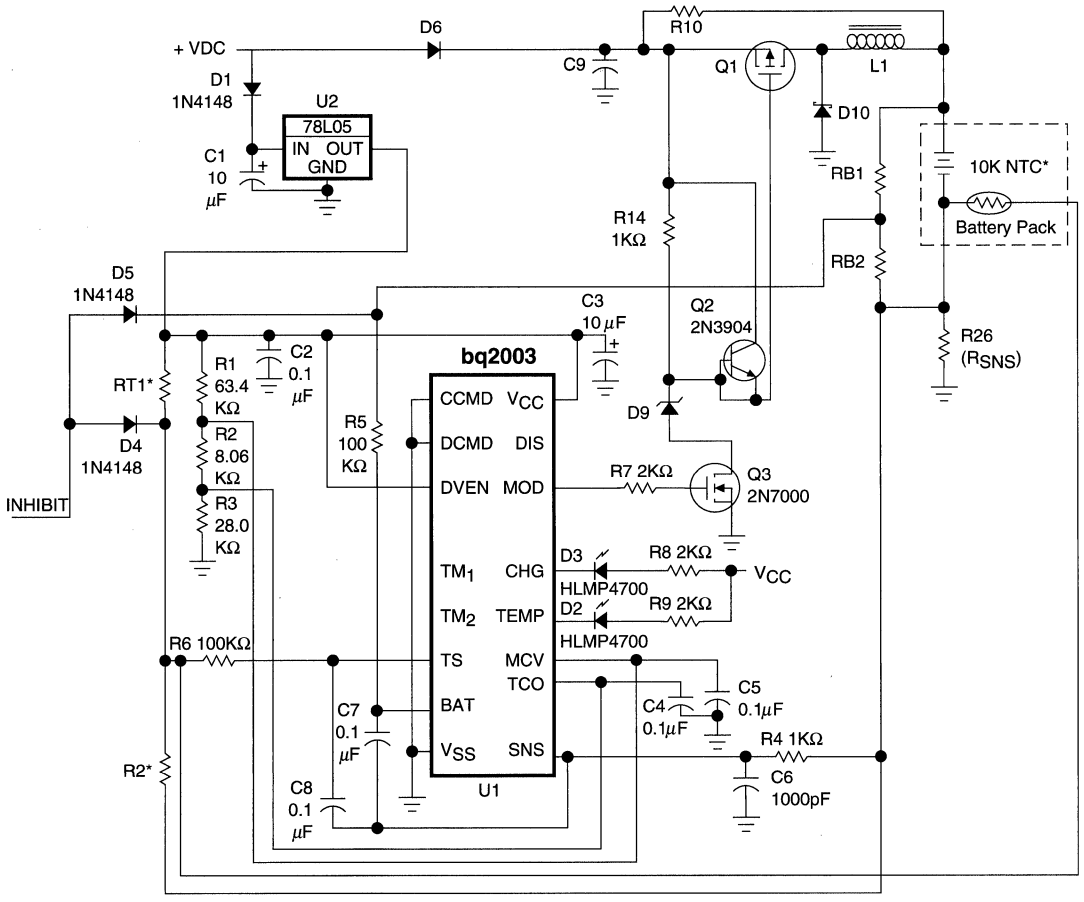
+VDC Input (Volts)	Motorola Part No.	Nominal Zener Voltage
Below 15	Shorted	0
15–18	1N749	4.3
18–21	1N755	7.5
21–24	1N758	10
24–27	1N964A	13
27–30	1N966A	16
30–32	1N967A	18
32–35	1N968A	20

Charge is initiated on battery replaced or V_{CC} valid. -ΔV detection is enabled (DVEN high), and discharge control is disabled (DCMD low). MCV = 1.8V; LTF = 10°C; TCO = 50°C; $\Delta T/\Delta t$ at 30°C = 0.82°C/min. (i.e., typical = 1.10°C/min.). Timer-mode selection (see data sheet) and trickle resistor R10 selection (see page 2-85 of the application note entitled "Using the bq2003 to Control Fast Charge") are determined by the designer. R26 is selected such that $I_{CHG} * R26 = 0.235V$.

The values of RB1 and RB2 to complete this schematic may be selected from Table 2 in the application note entitled "Using the bq2003 to Control Fast Charge."

Note: Temperature control and qualification may be disabled by tying the TCO pin to V_{SS} and fixing the voltage on the TS pin to 0.1 * V_{CC}.

Table 2 lists suggested components for different-rate chargers. Table 3 lists other components shown in Figure 1.



DIS: No connect.

*NTC, RT1, and RT2:

Thermistor	RT1	RT2
Keystone RL0703-5744-103-S1	3.83K	2.94K
Philips 2322-640-63103	4.02K	3.09K
Fenwal Type 16, 197-103LA6-A01	4.02K	3.09K

FG200312.eps

Figure 1. P-Channel MOSFET Switching-Mode Charger

3/16

Table 2. Suggested Components—P-Channel MOSFET Charger

Suggested Max. Charging Current	Q1	D6	D10	C9	L1
1A	IRF9Z14	1N4001	1N5818	ECA-1VFQ390 39µF/35V/460mΩESR	30 turns, #26 AWG, wound on Magnetics, Inc., P/N 77040 core; nominal inductance 59µH; GFS Mfg., Inc., P/N 92-2156-1
2A	IRF9Z24	1N5821	1N5821	ECA-1VFQ560 56µF/35V/300mΩESR	37 turns, #22 AWG, wound on Magnetics, Inc., P/N 77120 core; nominal inductance 98µH; GFS Mfg., Inc., P/N 92-2157-1
3A	IRF9Z34	1N5821	1N5821	ECA-1VFQ121 120µF/35V/170mΩESR	
Source	International Rectifier	Motorola	Motorola	Panasonic	GFS Mfg., Inc. Dover, NH (603) 742-4375

Table 3. Other Components—P-Channel MOSFET Charger

Component Name	Component Description
C1	10µF 35V electrolytic
C2, C4, C5, C7, C8	0.1µF ceramic
C3	10µF 10V electrolytic
C6	1000pF ceramic
D1, D4, D5, D8	1N4148
D2, D3	HLMP 4700 red LED
Q2	2N3904
Q3	2N7000
R1, R2, R3	User-defined 1% ¼W or ⅛W
R4	1KΩ 5% ¼W
R5, R6	100KΩ 5% ¼W or ⅛W
R7, R8, R9	2KΩ 5% ¼W or ⅛W
R10, R26	User-defined
RB1	User-defined 1% ¼W or ⅛W
RB2	User-defined 1% ¼W or ⅛W
RT1	User-defined 1% ¼W or ⅛W
RT2	User-defined 1% ¼W or ⅛W
U1	bq2003
U2	LM78L05ACZ

N-Channel MOSFET Buck-Topology Switch-Mode Charger

The advantage of an n-FET buck topology is the price-versus-performance benefit of the n-FET family. The disadvantage is the number of additional components required to support it.

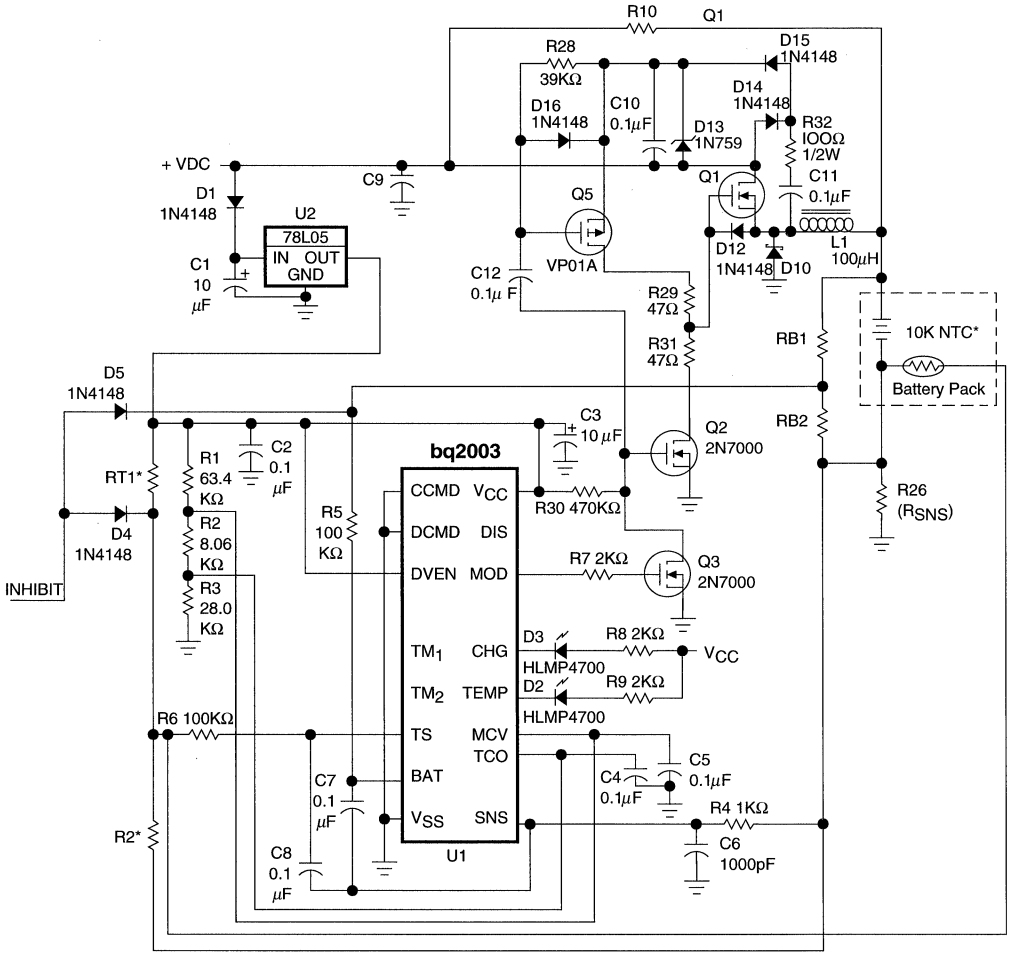
The schematic in Figure 2 is a standard configuration for an nFET switch-mode charger that can charge 4 to 12 NiCd or NiMH cells with current regulated up to 9A. The Q1 gate must be driven positive with respect to the drain in this application to provide full enhancement of the device. When catch diode D10 is conducting, C11 is charged. When Q1 is conducting, C11 is charging C10. This charge pump allows adequate voltage to drive Q1 into full enhancement via Q5. As Q2 conducts, the Q1 gate charge is depleted, causing Q1 to turn off.

Charge is initiated on battery replaced or V_{CC} valid. -ΔV detection is disabled (DVEN low), and discharge control is disabled (DCMD low). MCV = 1.8V; LTF = 10°C; TCO = 50°C; $\Delta T/\Delta t$ at 30°C = 0.82°C/min. (i.e., typical = 1.10°C/min.). Timer-mode selection (see data sheet) and trickle resistor R10 selection (see page 2-85 of the application note entitled "Using the bq2003 to Control Fast Charge") are determined by the designer. R26 is selected such that $I_{CHG} * R26 = 0.235V$.

The values of RB1 and RB2 to complete this schematic may be selected from Table 2 in the application note entitled "Using the bq2003 to Control Fast Charge."

Note: Temperature control and qualification may be disabled by tying the TCO pin to V_{SS} and fixing the voltage on TS pin to $0.1 * V_{CC}$.

Table 4 lists suggested components for different-rate chargers. Table 5 lists other components shown in Figure 2.



DIS: No connect.

Thermistor values:

Thermistor	RT1	RT2
Keystone RL0703-5744-103-S1	3.83K	2.94K
Philips 2322-640-63103	4.02K	3.09K
Fenwal Type 16, 197-103LA6-A01	4.02K	3.09K

FG200313.eps

Figure 2. N-Channel MOSFET Switching-Mode Charger

6/16

Table 4. Suggested Components—N-Channel MOSFET Charger

Suggested Max. Charging Current	Q1	D6	D10	C9	L1
3A	IRFZ34	1N5821	1N5821	ECA-1VFQ121 120µF/35V/170mΩESR	37 turns, #22 AWG, wound on Magnetics, Inc., P/N 77120 core; nominal inductance 98µH; GFS Mfg., Inc., P/N 92-2157-1
6A	IRFZ44	MBR735	MBR735	ECA-1VFQ391 390µF/35V/55mΩESR	33 turns, #18 AWG, wound on Magnetics, Inc., P/N 77310 core; nominal inductance 98µH; GFS Mfg., Inc., P/N 92-2158-1
9A	IRFZ48	MBR1035	MBR1035	ECA-1VFQ681 680µF/35V/34mΩESR	25 turns, #16 AWG, wound on Magnetics, Inc., P/N 77930 core; nominal inductance 98µH; GFS Mfg., Inc., P/N 92-2159-1
Source	International Rectifier	Motorola	Motorola	Panasonic	GFS Mfg., Inc. Dover, NH (603) 742-4375

Table 5. Other Components—N-Channel MOSFET Charger

Component Name	Component Description
C1	10µF 35V electrolytic
C2, C4, C5, C7, C8, C10, C11, C12	0.1µF ceramic
C3	10µF 10V electrolytic
C6	1000pF ceramic
D1, D12, D14, D15, D16	1N4148
D2, D3	HLMP 4700 red LED
D13	1N759 12V 500mW Zener
Q2, Q3	2N7000
Q5	VP01A
R1, R2, R3	User-defined 1% ¼W or ⅛W
R4	1KΩ 5% ¼W or ⅛W
R5, R6	100KΩ 5% ¼W or ⅛W
R7, R8, R9	2KΩ 5% ¼W or ⅛W
R10, R26	User-defined
R28	2.7KΩ 5% ¼W or ⅛W
R29, R31	47KΩ 5% ¼W or ⅛W
R30	470KΩ 5% ¼W or ⅛W
R32	100KΩ 5% ½W or ⅛W
RB1	User-defined 1% ¼W or ⅛W
RB2	User-defined 1% ¼W or ⅛W
RT1	User-defined 1% ¼W or ⅛W
RT2	User-defined 1% ¼W or ⅛W
U1	bq2003
U2	LM78L05ACZ

Operating Switching Frequency

During Q1 on-time, the L1 current ramps up linearly. During Q1 off-time (D10 conduction), the L1 current ramps down linearly. The rate of rise and fall (slew rate) of L1 current is determined by the inductance value of L1 and the DC voltage placed across L1. The slew rate is usually different between Q1 conduction time and D10 conduction time. This is because the DC voltage across L1 is usually different during these two timing intervals.

The sum of these two timing intervals equals the switching period. The switching period reciprocal equals the switching frequency.

Use the following equation to estimate the switching frequency.
F =

$$\frac{1}{\frac{L\left(\frac{0.030V}{R_{SNS}}\right)}{V_{DC}-(V_{BAT}+V_{SNS}+D6_{VF}+Q1_{DROP})}+\frac{L\left(\frac{0.030V}{R_{SNS}}\right)}{V_{BAT}+V_{SNS}+D10_{VF}}}$$

where:

F = Frequency in Hertz

L = L1 inductance in Henrys

$D6_{VF}$ = D6 average forward voltage drop

$D10_{VF}$ = D10 average forward voltage drop

R_{SNS} = R26 value in ohms

$Q1_{DROP}$ = Charge current times Q1 on-state-resistance
= $(^{0.235V}/_{R_{SNS}})\, Q1_{RDSON}$

V_{DC} = Input DC voltage

V_{BAT} = Battery pack instantaneous voltage

Charge Current Regulation With Varying System Loads

Systems with an integrated charger and a constant-power external supply may not be capable of fast charging the batteries while simultaneously supporting system operation. In such cases the system operation takes priority, and the peak system energy demand must be supported.

In this situation, the charger designer has two options regarding charge during system operation:

1. The battery charging current may be held constant at a low level that is supportable during peak system operation loads. During periods of low system power demand, available power is not used. The charge time during system operation is typically quite long.
2. The battery charging current may be allowed to vary inversely with the system load. As the system power demand decreases, the charge rate increases and vice versa. For portable systems with varying load requirements (such as those using "power management"), this allows any surplus power during low system activity to be used for battery charging. The charge time during system operation depends on the average system power requirement, not the peak requirement.

Option 1 may be implemented when using the bq2003 as the charge current regulator by using the system V_{CC} as an "INHIBIT" signal to pull pins BAT and TS high when the system is on. (See Figures 1 and 2 and the System-Controlled Charge Inhibition discussion in "Using the bq2003 to Control Fast Charge.") When the system is on, fast charge is inhibited. The only charge path is the trickle resistor.

Option 2A may be implemented using the bq2003 as the charge current regulator with the system load return at the high end of the sense resistor R26 (Figure 3). $\Delta T/\Delta t$ charge termination is enabled and $-\Delta V$ termination is disabled.

With a battery pack cell voltage ≥ 1V per cell, the system load always receives its required current. The system load current flows through R26 along with the battery charge current. The battery receives any difference between the programmed charge current and the system load current. If the system load current exceeds the programmed charge current, then no charge current will be delivered to the battery. The system load current biases the SNS voltage via R26, which limits the buck regulator's current delivered to the battery. The total available

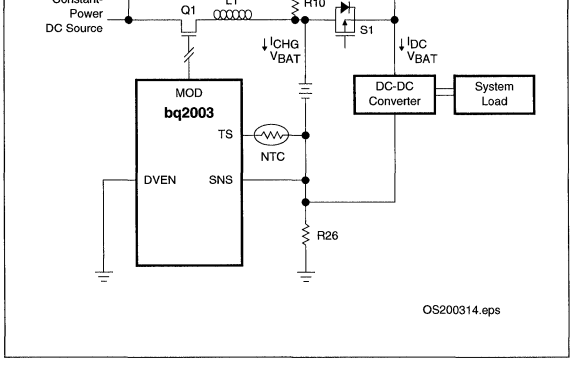


Figure 3. Option 2A

power may be allocated between the battery charge and system operation such that power used = (I_{CHG} + I_{DC}) * V_{BAT}.

Using this method, the sense resistor R26 and its associated energy penalty are not in the battery discharge path. The charge current is regulated in a variable fashion such that R26 * (I_{CHG} + I_{DC}) = 0.235V.

Charge current regulation may occur until I_{DC} * R26 ≥ 0.250V. Above this point, the MOD output is held low (off). When actively switching, the MOD frequency remains very nearly constant.

If the battery voltage is extremely low, the bq2003 does not begin charging until the battery trickle charges to 1V per cell. This protects the system voltage from being pulled down to an inoperable range by a very low battery.

-ΔV is disabled to prevent false terminations due to the varying charge current and the battery's internal impedance. Slight but significant voltage perturbations at V_{BAT} can cause a false -ΔV charge termination during variations in battery charge current in this configuration. ΔT/Δt, however, is *not* affected by variations in charge current because the battery's physical mass has a relatively slow time constant that naturally integrates all variations.

Switch S1 is turned on for battery operation and off during charge. Switch S1 is driven by appropriate logic defined by the needs of the application. The presence or absence of an input DC power source could control this logic. A Schottky diode is a simpler alternative to S1, but the voltage drop may not be desirable.

Option 2B is another variable charge rate approach (Figure 4). This option may be preferred if the available power is considerably more than the maximum I_{CHG} * V_{BAT} (ignoring voltage loss). In the first approach, the system load return is to the high end of the sense resistor R26, limiting the power used to approximately (I_{CHG} + I_{DC}) * V_{BAT}, with I_{CHG} = 0 when I_{DC} ≥ maximum I_{CHG}.

For this second approach to use all the available power, the system load return is at the low end of the sense resistor. This accomplishes the fastest possible charge during system operation, but carries a penalty during battery operation because of the energy and voltage loss from discharge through the sense resistor (or the cost and impedance of a switch to bypass the sense resistor).

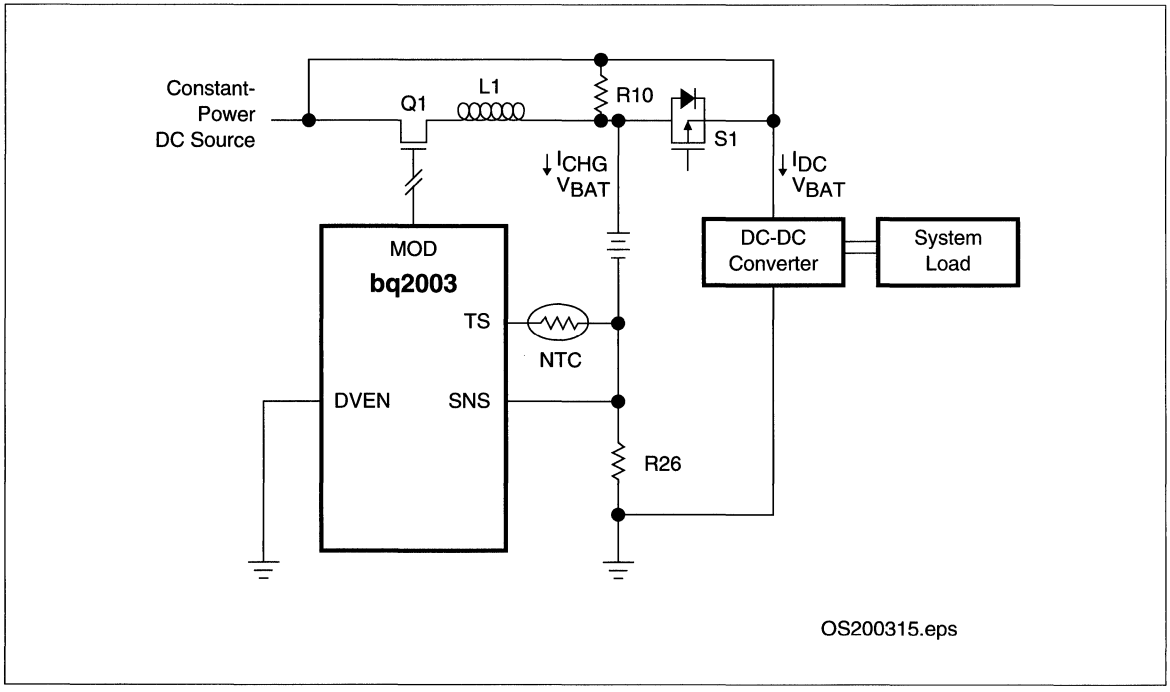


Figure 4. Option 2B

9/16

Layout and EMI Considerations

The best approach to PC board layout follows the strict rule of a single-point ground return. Sharing high current ground with small signal ground causes undesirable noise on the small signal nodes. Referencing Figures 1 and 2, C2 and C3 should be placed as close as possible to the V_{CC} pin. C6 should be placed at the SNS pin. C7 and C8 should be associated between the TS/SNS and the BAT/SNS pins, respectively, with short leads. Isolation resistors R5 and R6 should be placed close to the BAT and TS pins.

Layout of power components C9, D10, L1, Q1, and R26 should reduce lead-length paths between these components to an absolute minimum.

If a dual-layer PC board is used, route signal lines on the solder side. This leaves the component side to be used as a ground plate. This technique reduces noise on adjacent nodes within the circuit and helps reduce EMI by giving the high-energy fields a ground plane to work against.

P-FET and N-FET Layout Examples

Figures 5–7 illustrate the layout of the p-channel MOSFET switch-mode charger board, and Figures 8–10 illustrate the layout of the n-channel MOSFET switch-mode charger board.

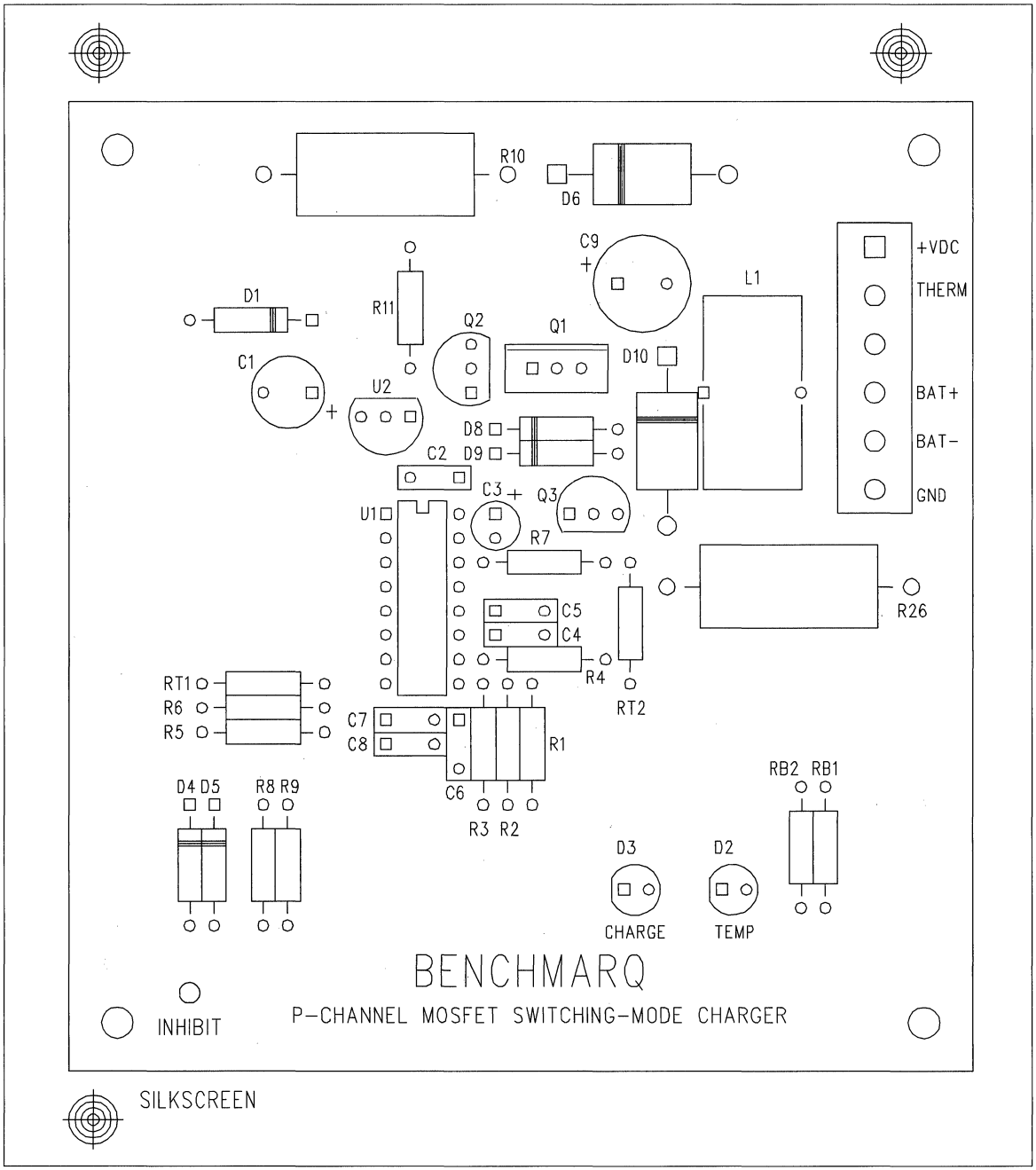


Figure 5. P-Channel MOSFET Switching Charger—Silkscreen

11/16

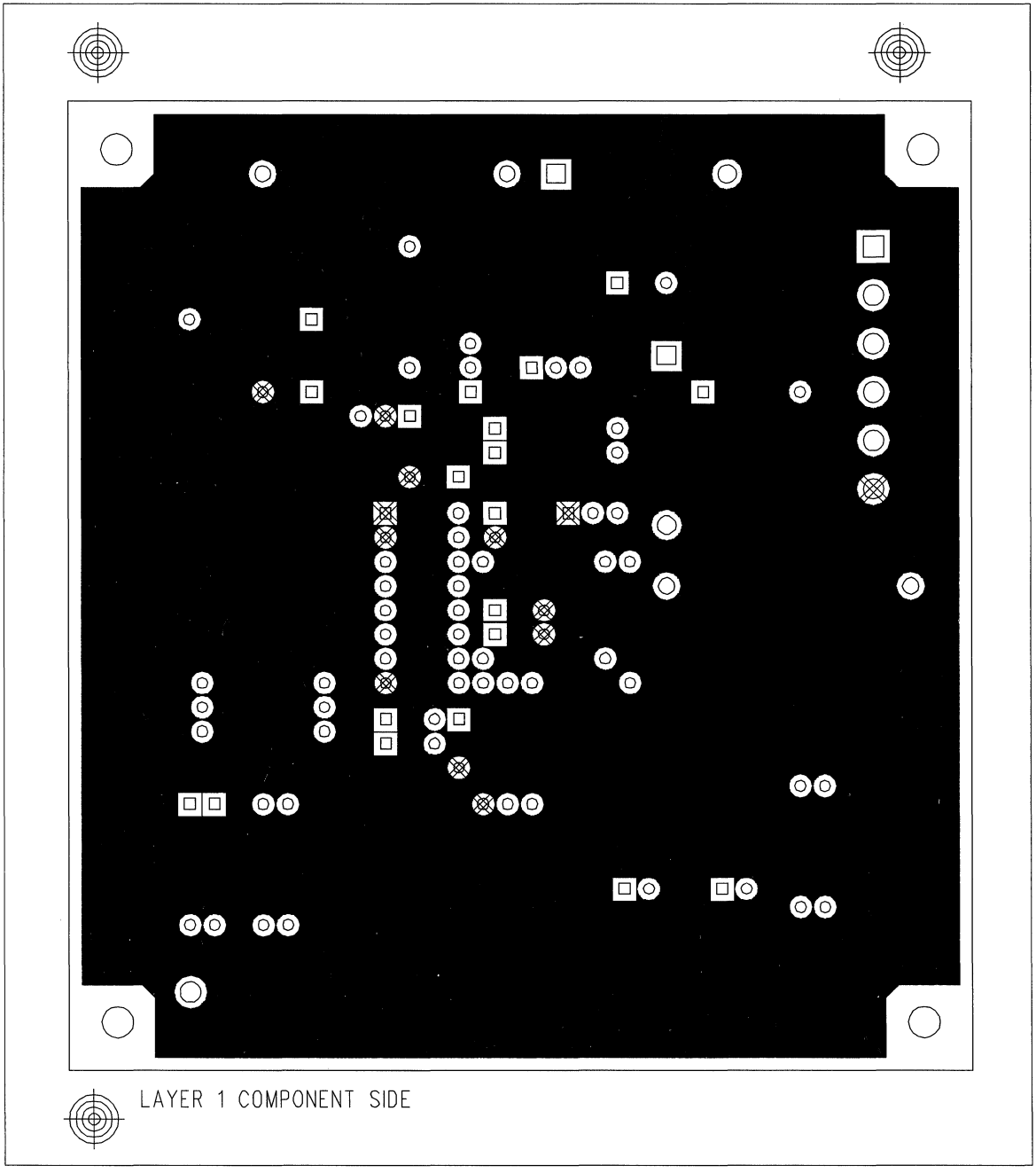


Figure 6. P-Channel MOSFET Switching Charger—Component Side

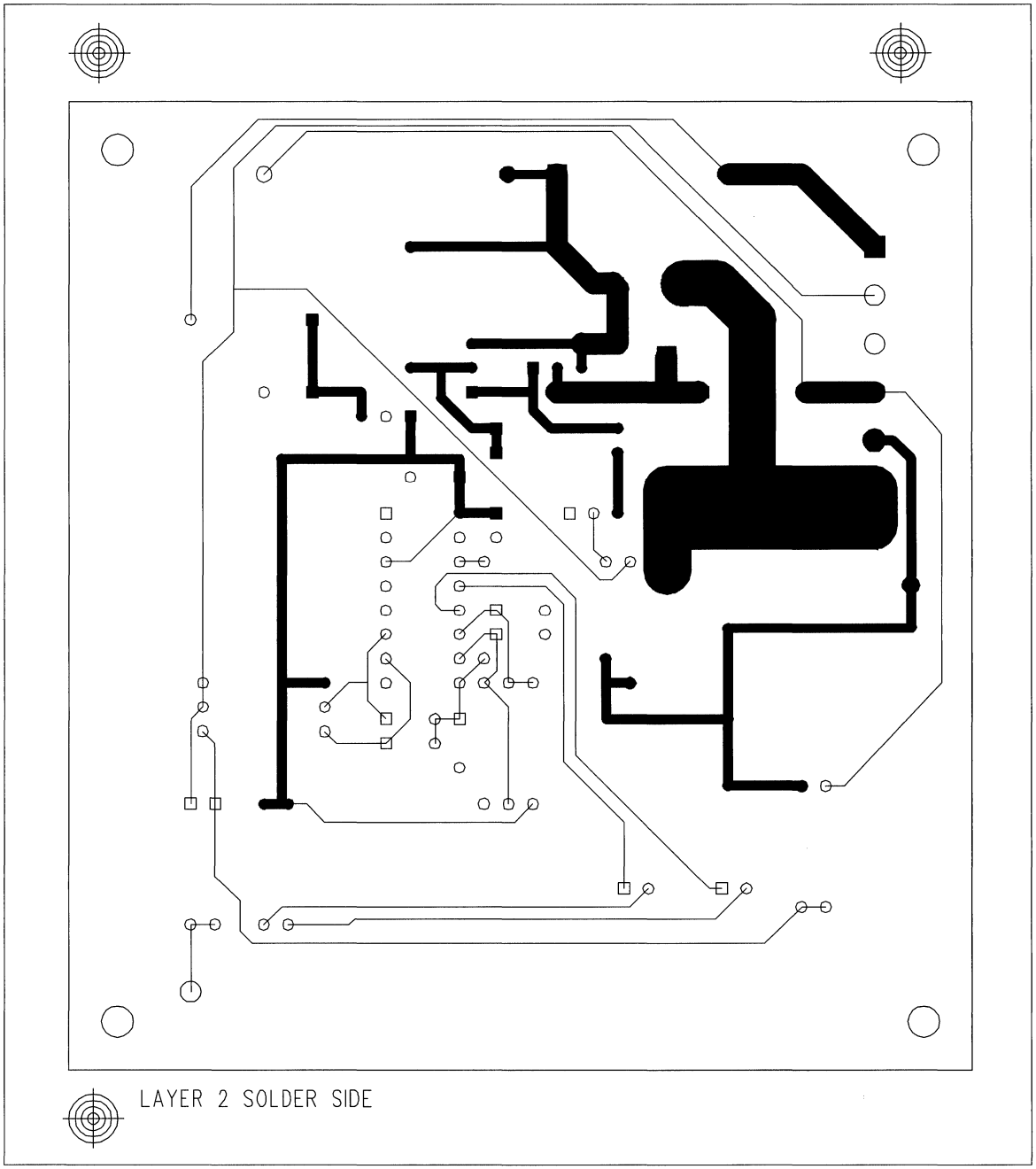


Figure 7. P-Channel MOSFET Switching Charger—Solder Side

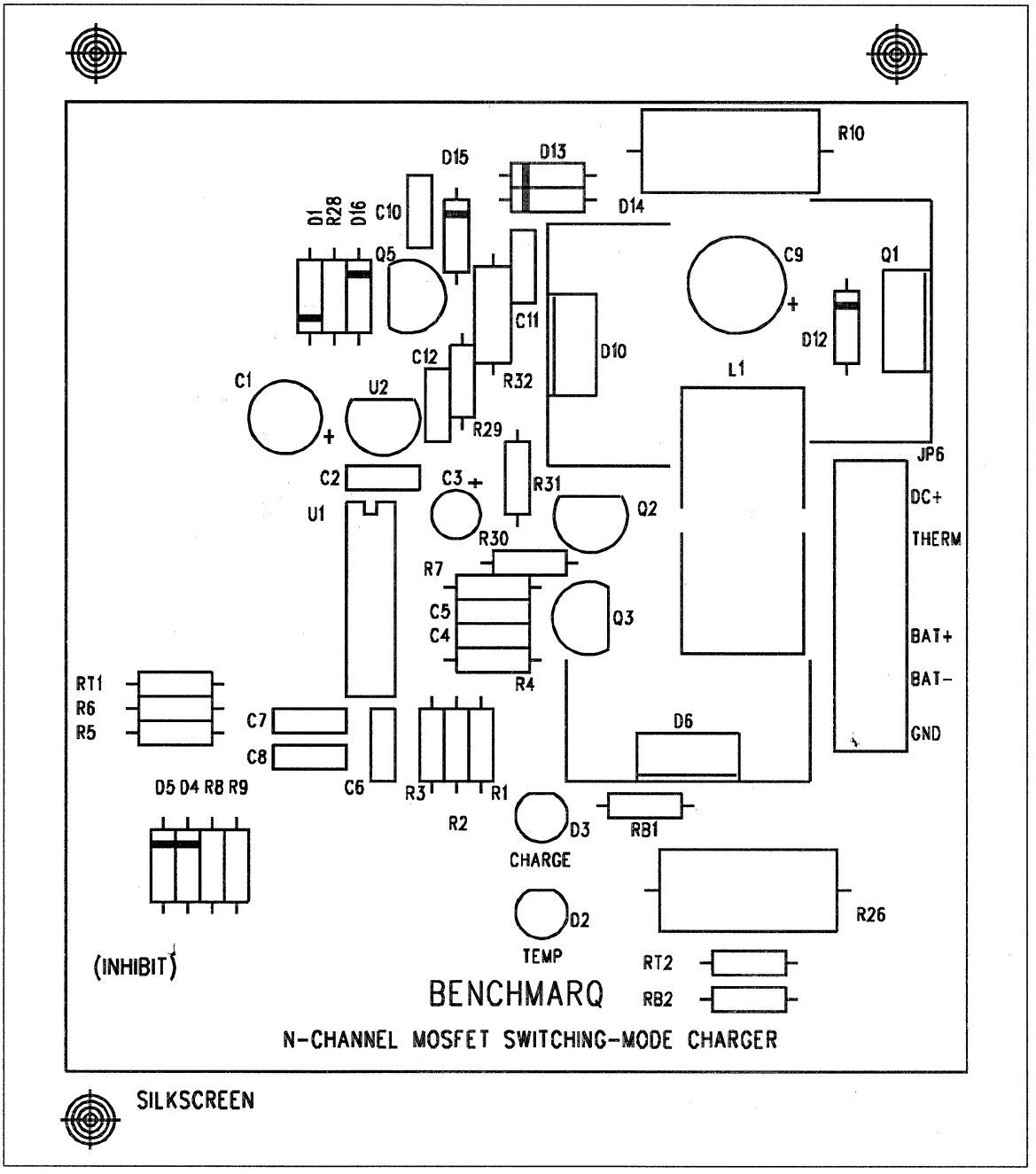


Figure 8. N-Channel MOSFET Switching Charger—Silkscreen

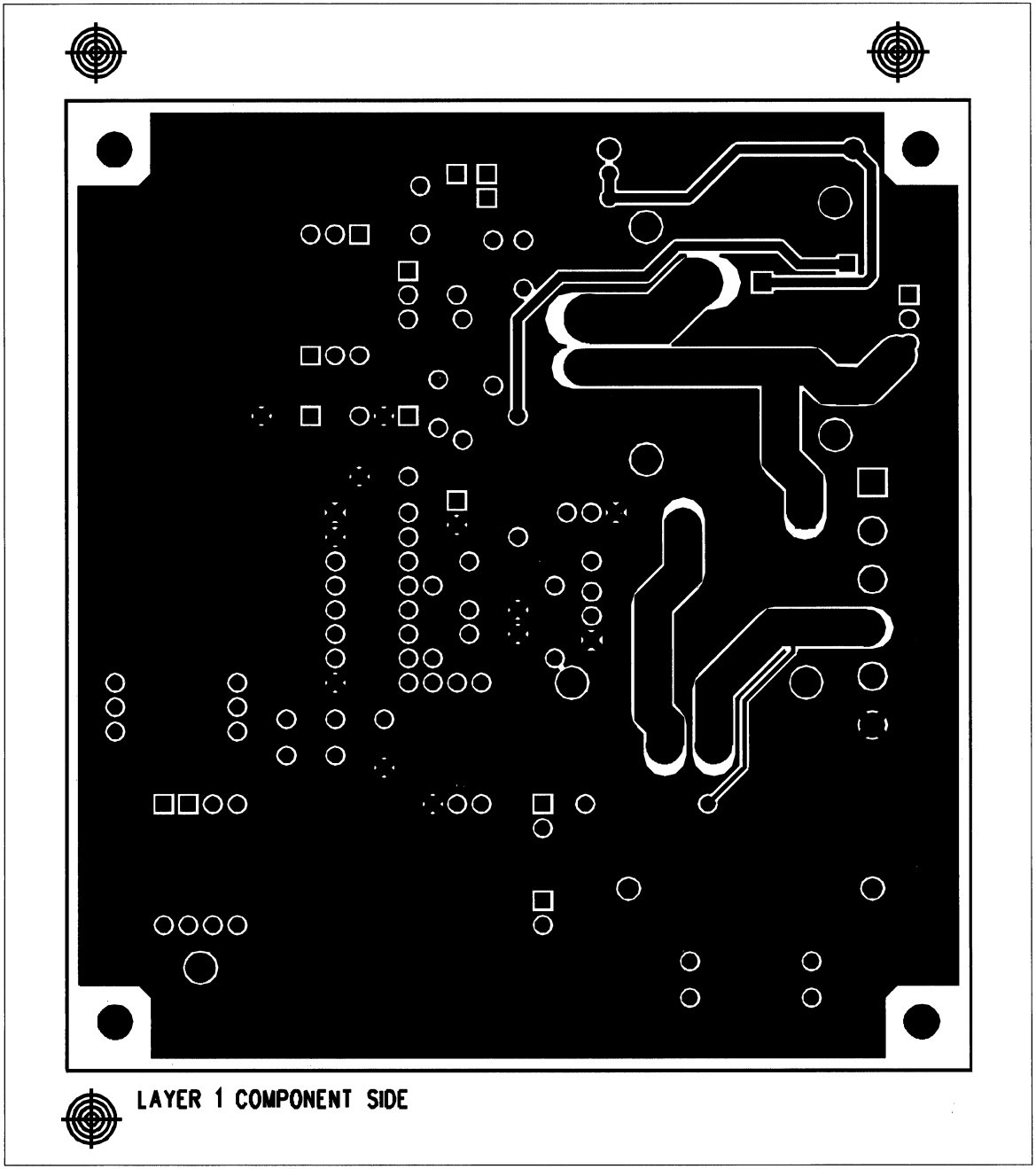


Figure 9. N-Channel MOSFET Switching Charger—Component Side

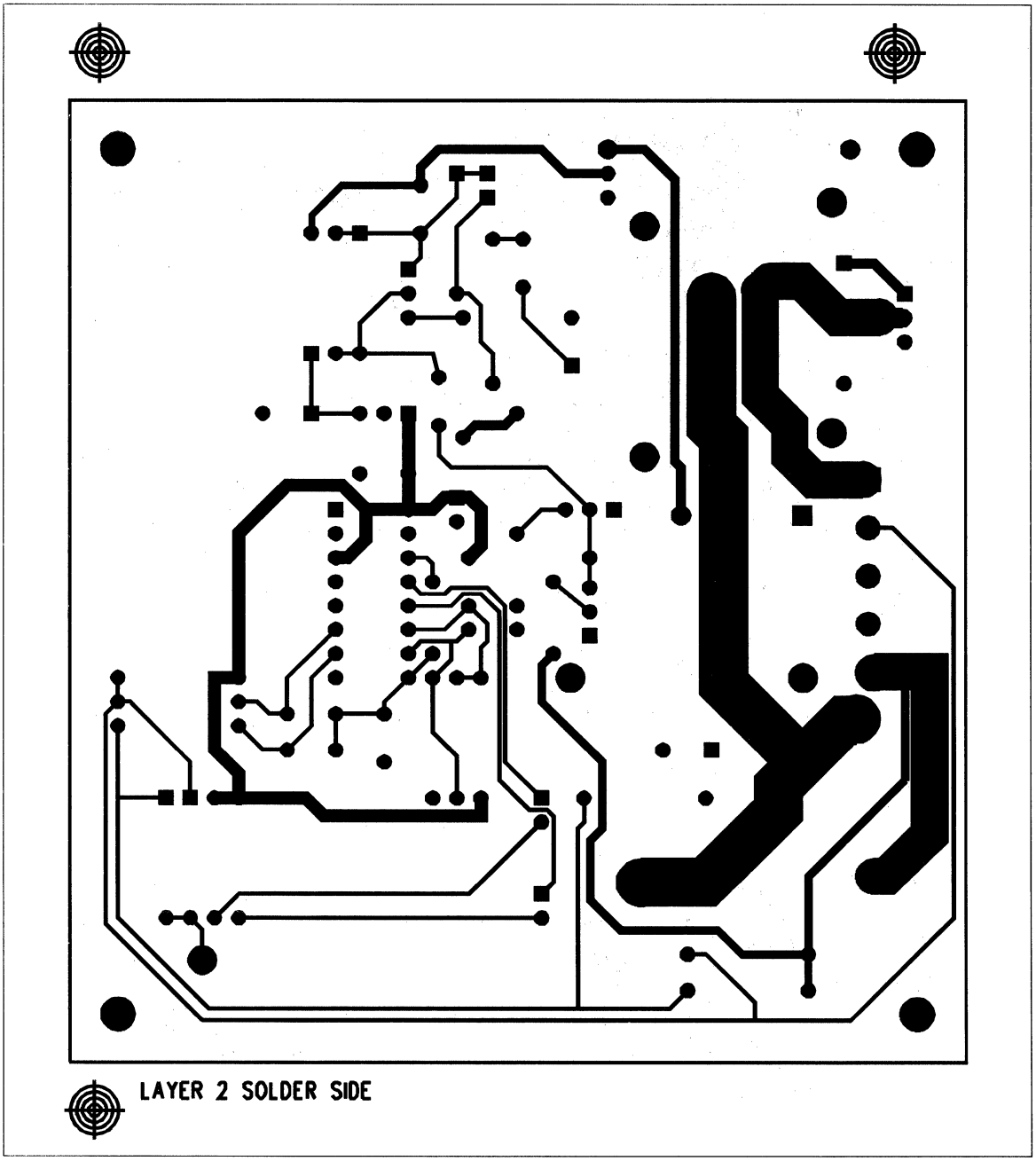


Figure 10. N-Channel MOSFET Switching Charger—Solder Side

16/16

UNITRODE

DN-502 High-Side Current Sensing With Unitrode's Benchmarq Fast-Charge Control ICs

Introduction

A low-side, current-sensing resistor in a fast-charge control circuit generates a small voltage drop between the low side of the battery pack and ground. This drop is not a problem in most cases; however, some applications, particularly mobile communications circuits, are intolerant of any potential difference between the low side of the battery pack and ground. Using a few additional components in the circuit, high-side current sensing solves this problem and allows the charging source, application circuit, and battery pack to share a common ground.

Circuit Implementation

In a high-side sensing application, the sense resistor (R_1, usually 10–100mΩ) is between the inductor and the positive battery-pack terminal. (See Figure 1.) The negative pack terminal is connected to ground. The voltage across R_1 is translated to a ground-referenced signal for presentation at the current-sense pin of the fast-charge control IC by two PNP small signal transistors (Q1, Q2) that form a "voltage mirror." The mirror reflects the voltage across R_1 onto the much larger 1kΩ resistor R_2 in the emitter of PNP transistor Q2. The collector current of Q2 (the "sense-resistor signal current") will recreate the sense-resistor voltage each time it is passed through a 1kΩ resistor (R_3 and R_4) referenced to ground.

The mirror's transistor pair is biased by a current sink formed by an NPN transistor (Q3) with its base at V_{CC} and its emitter connected to ground through an 18kΩ resistor (R_5). This arrangement assures that (1) the battery will not be loaded by the bias network when power is not applied, and (2) the best voltage compliance will occur at the regulated value of charging current.

The inputs to both the pack-voltage monitoring pin (BAT) and temperature sensing pin (TS) of the fast-charge control IC must be translated up in voltage by the sense resistor voltage in order to simulate the fast-charge control chip's accustomed low-side sensing environment.

For the TS input, the sense-resistor signal current is intercepted by the emitter of another PNP transistor (Q5), the base of which is biased to the thermistor connection point. The 1kΩ resistor (R_3) in the emitter path of Q5 creates a voltage equal to the sense-resistor voltage plus the base-emitter drop of Q5. Buffering this point with a complementary NPN transistor (Q4) subtracts this base-emitter drop and leaves the proper signal level to be applied to the TS input. Q4 requires a load: the 10kΩ resistor (R_6) to ground in its emitter path.

Having flowed through Q5 and its emitter resistor, the sense resistor signal current now flows through the 1kΩ resistor (R_4) in Q5's collector to ground, re-creating the voltage across the sense resistor (R_1) for the SNS input.

BAT input-voltage is translated by connecting the battery pack voltage-divider pair between the high side of the sense-resistor and the SNS input. This configuration allows the BAT input to ride on top of the sense resistor voltage at SNS. The total bias current of the battery divider network must not significantly disturb current regulation; a bias current of 10μA or less will contribute less than 4.3% error in this example circuit.

The principles of operation of this circuit can be applied to all of Unitrode's Benchmarq Fast-Charge Control ICs.

High-Side Current Sensing

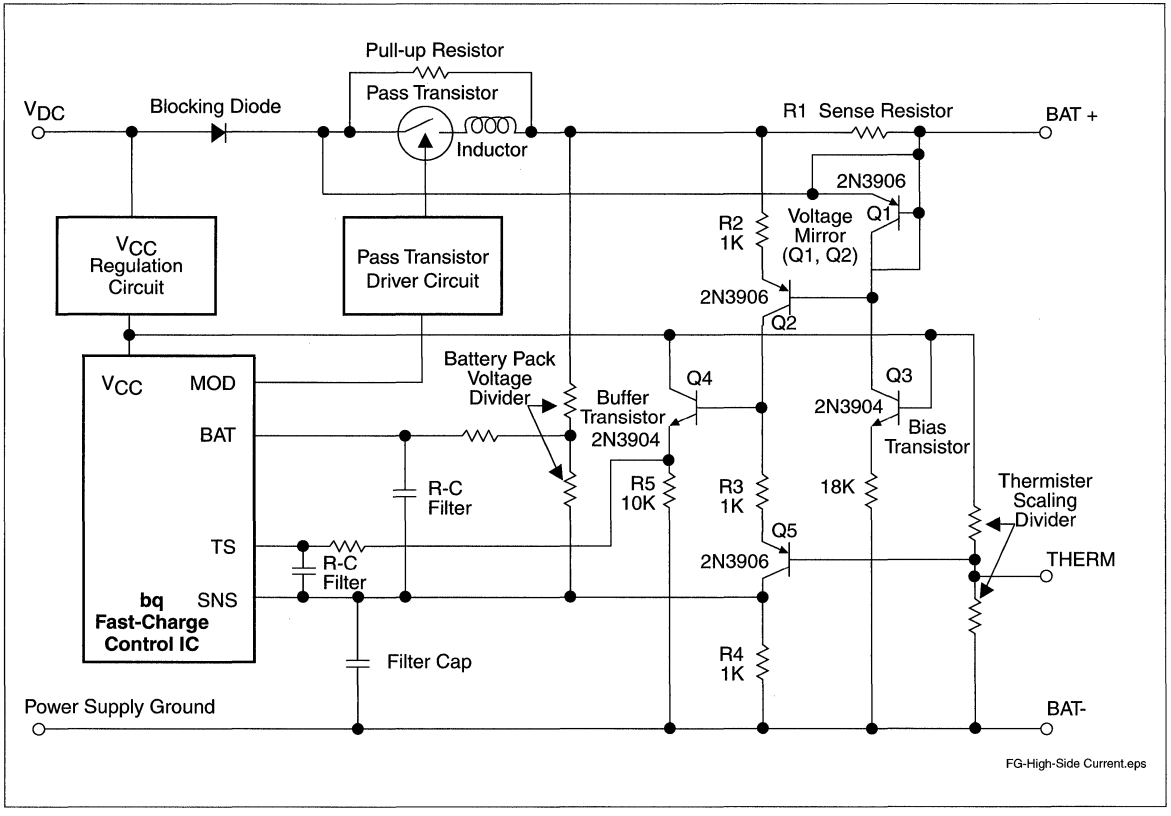


Figure 1. High-Side Sensed Diagram

UNITRODE

U-507 Using the bq2005 to Control Fast Charge

Introduction

This application note describes the use and functions of the bq2005 controlling a current source to fast charge NiCd or NiMH batteries. The bq2005 may also serve as the modulator for a switching-mode constant-current regulator to provide an efficient charge current source. Examples illustrate the ease with which the bq2005 is incorporated into applications.

The bq2005 is targeted for applications requiring state-of-the-art dual-battery fast-charging at minimal cost. It provides sophisticated full-charge detection techniques such as $\Delta T/\Delta t$ (delta temperature/delta time) and $-\Delta V$ (negative delta voltage) that enable the user to take advantage of advanced battery technologies such as nickel metal-hydride (NiMH) and high-capacity fast-charge nickel cadmium (NiCd). Systems using the bq2005 can be easily upgraded from NiCd batteries to NiMH batteries without system redesign.

Background

A significant advantage of the bq2005 over other fast-charge solutions is the use of $\Delta T/\Delta t$ and/or $-\Delta V$ as the primary decisions for fast-charge termination. $\Delta T/\Delta t$ detection is one of the most sensitive and reliable methods for fast-charge termination when charging NiMH and NiCd batteries. Near full charge, the temperature rise begins to accelerate. The $\Delta T/\Delta t$ decision typically precedes the peak voltage, allowing for minimal overcharge stress. The $\Delta T/\Delta t$ method also tolerates varying rates of charge, which may be desirable when charging during system operation.

Compared to the ΔT method, which uses two sensors to monitor battery temperature and ambient temperature, the $\Delta T/\Delta t$ method uses a single thermistor to monitor the rate of temperature increase. This approach is more sound in cases when the initial battery temperature may be significantly different from the ambient temperature. This $\Delta T/\Delta t$ termination decision can easily be disabled.

An input from a battery voltage divider enables the bq2005 to detect $-\Delta V$, which is a very reliable charge terminator for NiCd batteries and most NiMH batteries, depending on the application. $-\Delta V$ detection in the bq2005 may be temporarily disabled during periods when the charge current fluctuates greatly or during the beginning of a fast charge to eliminate false peaks. $-\Delta V$ termination is logic-level selectable without affecting other termination choices.

To help ensure safety for the battery and system, fast charging may also be terminated at a high-temperature cutoff threshold (TCO), a safety time period, or a maximum cell voltage threshold (MCV). To avoid possible premature fast-charge termination when charging batteries after long periods of storage, the bq2005 disables $-\Delta V$ detection during a short "hold-off" period at the start of fast charge. This hold-off period is configured as described in the bq2005 data sheet.

The bq2005 may be configured to have two or three charge stages. In a two-stage configuration, the fast-charge stage controlled by the bq2005 is preceded and followed by a pulse-trickle charge at a rate controlled by the programming pins of the bq2005. In a three-stage configuration, the fast charge is followed by a top-off charge stage at $\frac{1}{8}$ the fast charge rate. This allows the battery to be quickly and safely brought to a full charge state. Following top-off, a trickle charge at a pulsed rate equivalent to $\frac{1}{64}$ is supplied to the battery to compensate for self-discharge

Basic Charge-Control Operation

Three detailed applications follow this section. One provides direct control of a linear regulator, and the other two provide switch-mode current rgulation.

Gating Current

Figure 1 shows an example of external source gating. With SNS tied to V_{SS}, the bq2005 enables charge current to the battery by asserting MOD at the start of charge and maintaining this state until charge is terminated. In this example, R1, Q2, R4, R5, R6, and Q1 form the switching circuit. MOD drives Q2 into conduction— saturating Q1.

The current-handling capability of this circuit depends on the components selected to perform the switching and current-regulation functions. Table 1 shows some suggested component combinations for corresponding currents.

The voltage-boost circuit shown in Figure 1 is necessary to keep the voltage on either BAT_A or BAT_B above MCV while the other battery is charging (assumes only one battery is inserted). This implementation is limited to 15V DC. Please contact Unitrode's Applications Group for assistance with other input voltage configurations, or for alternative methods.

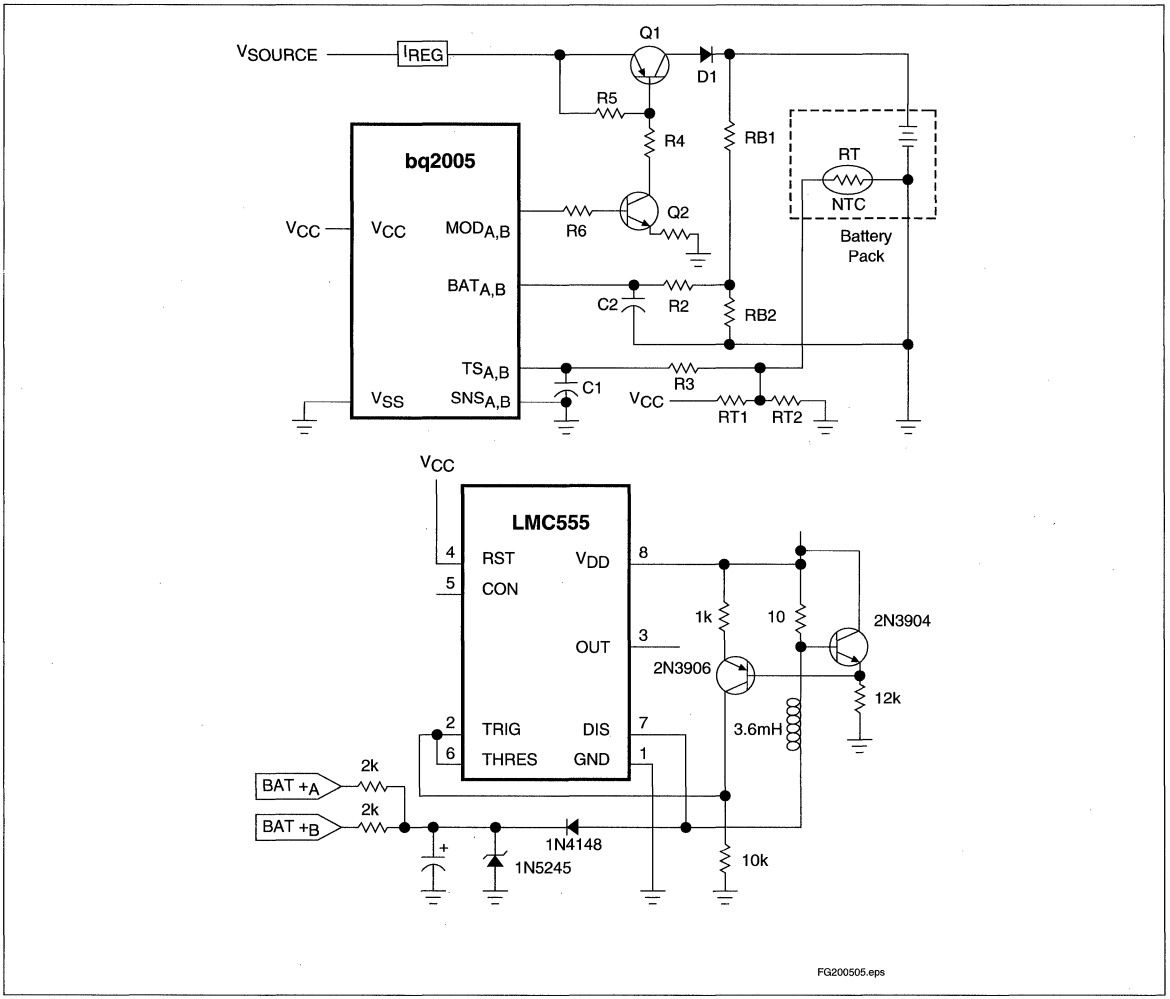


Figure 1. Gated External Source (Bipolar Switch Option)

Table 1. Suggested Component Combinations

I_{IN}	Q1	Q2	R1	R4	R5	R6
0.5A	MPS750	2N3904	150Ω ¼W	–	1KΩ	–
1A	MPS750	2N3904	68Ω ½W	100Ω ½W	1KΩ	–
2A	TIP42	2N3904	43Ω ½W	51Ω ½W	200Ω	–
3A	TIP42	2N3904	27Ω 1W	27Ω 1W	200Ω	–
5A	IRFR9010	2N3904	100Ω ¼W	–	1KΩ	33KΩ
8A	IRF9Z22	2N3904	100Ω ¼W	–	1KΩ	33KΩ

Charge Initiation

Charge may be initiated by applying power to the IC or by battery insertion. Charge initiation by application of power to the IC works as follows: When V_{CC} is applied, the bq2005 is held in reset for approximately one and one-half seconds. At the end of the reset period, a charge cycle initiates as soon as conditions allow. If both batteries are present, fast-charging battery B takes precedence over charging battery A. If battery A is inserted while fast charge is pending on battery B, the bq2005 trickle charges both batteries, and then fast charges battery B after conditions allow. If battery B is inserted while fast charge is pending on battery A, the bq2005 trickle charges both batteries, and then fast charges battery B when conditions allow.

Charge initiation on battery replacement relies on the $BAT_{A,B}$ pin voltage being greater than MCV in the absence of a battery, and falling below MCV when the battery is connected. To ensure this condition, pull-up resistors from $BAT_{A,\ B+}$ (positive pack terminals) to the charging voltage source (V_{DC} in step-down regulators, the boosted charging voltage in step-up regulators) are sized to elevate the empty battery location voltage on the $BAT_{A,B}$ pins such that MCV is exceeded.

When the battery is replaced, the voltage on $BAT_{A,B}$ should fall below MCV, at which time a charge cycle initiates as soon as conditions allow.

Table 2, Charge Action Truth Table, describes the bq2005 charge actions under a variety of battery and charge states.

Discharge-Before-Charge

It may occasionally be desirable to discharge the battery to a known voltage level prior to charge. The reason for this may either be to remedy a voltage-depression effect found in some NiCd batteries or to determine the battery's charge capacity.

Figure 2 illustrates the implementation of this function for battery A. If $\overline{DCMD_A}$ is directly connected to V_{SS}, automatic discharge-before-charge is enabled with battery replaced or application of power to the bq2005. A negative strobe signal on $\overline{DCMD_A}$ also initiates discharge-before-charge. **This function takes precedence over a charge action and commences immediately when conditions warrant, forcing DIS_A to a high state until the voltage sensed on BAT_A falls below V_{EDV} (0.475 * V_{CC}).** Charging begins as soon as conditions allow.

Care should be taken not to overheat the battery during this process; excessive temperature is not a condition that terminates discharge.

Note: Because V_{SNS} may be above V_{SS} in bq2005 switching regulation applications, the internal battery voltage monitoring uses $V_{BAT} - V_{SNS}$, or V_{CELL}. This battery voltage monitoring V_{CELL} maintains a representative comparison voltage independent of any current through R_{SNS}.

Table 2. Charge Action Truth Table

V_{CC}	BAT_A	BAT_B	Charge Action
0→5V	V	V	Fast charge B, pend A
0→5V	V	N	Fast charge A
0→5V	N	V	Fast charge B
5V	↑	F	Fast charge B, pend A
5V	↑	L	Trickle A and B, fast charge B and pend A when conditions allow
5V	L	↑	Trickle A and B, fast charge B and pend A when conditions allow
5V	F	↑	Fast charge A, pend B
5V	D	L	Trickle A, trickle B
5V	L	D	Trickle A, trickle B
5V	D	V	Fast charge B, pend top-off A
5V	V	D	Fast charge A, pend top-off B
5V	D	D	Top off B, trickle A, then top off A, trickle B
5V	D	↑	Abort top-off A
5V	↑	D	Abort top-off B
5V	T	L	Trickle A, trickle B
5V	L	T	Trickle A, trickle B
5V	T	V	Fast charge B, pend trickle A
5V	V	T	Fast charge A, pend trickle B
5V	T	T	Trickle A, trickle B

V = Battery inserted and valid charge conditions: $0.475 * V_{CC} \le V_{CELL} \le 0.95 * V_{CC}$ $0.4 * V_{CC} \ge V_{TS} \ge V_{HTF}$

L = Battery inserted and outside temperature limit or below V_{EDV}.

N = Battery removed: $V_{CELL} > 0.95 * V_{CC}$

F = Fast charge

D = Top-off

T = Trickle

↑ = Battery insertion: V_{DIV} transitioning from ≥ $0.95 * V_{CC}$ to $V_{CELL} \le 0.95 * V_{CC}$

3/18

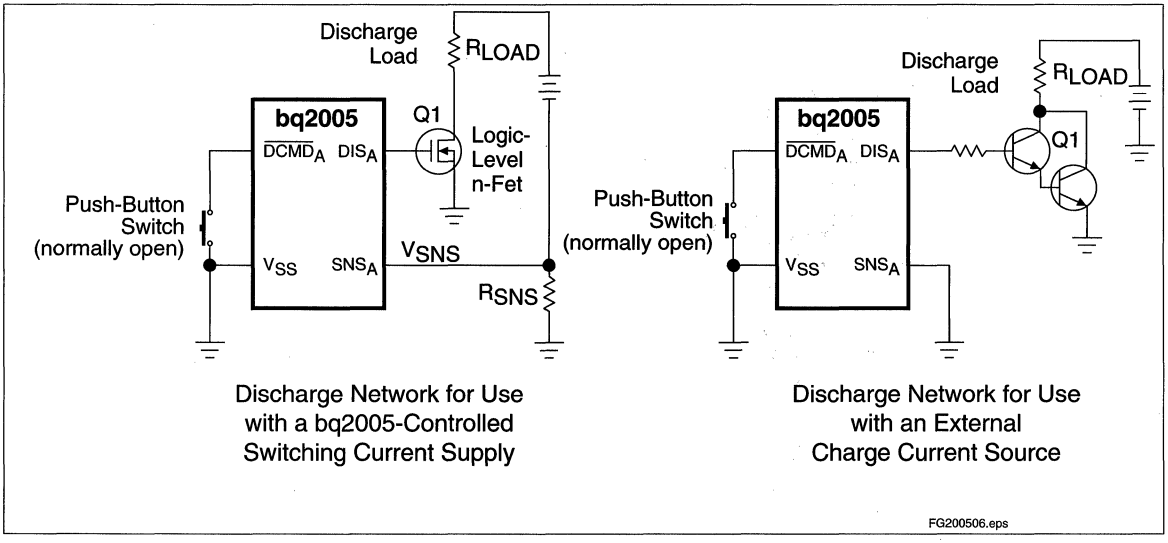


Figure 2. Battery Conditioning Network

The discharge-before-charge function is ignored or terminated when $V_{BAT} - V_{SNS} > V_{MCV}$ (battery removed). If the discharge-before-charge function is not desired, $\overline{DCMD}_A$ should be tied to V_{CC} or left floating. $\overline{DCMD}_A$ is internally pulled up to V_{CC}.

Configuring the $BAT_{A,B}$ Inputs

The bq2005 uses the battery voltage sense input on the $BAT_{A,B}$ pins to control discharge-before-charge, qualify charge initiation, terminate charge at an absolute limit, and facilitate negative delta voltage (-ΔV) detection.

V_{BAT} may be derived from a simple passive network across the battery. As shown in Figure 1, resistors RB1 and RB2 are chosen to divide the battery voltage down to the optimal detection range, which is between V_{MCV} and V_{EDV} ($0.475 * V_{CC} \leq V_{DIV} \leq 0.95 * V_{CC}$).

For NiCd and NiMH batteries, the battery terminal voltage is divided down to this potential per the following equation:

$$\frac{RB1}{RB2} = \frac{N}{2.375} - 1$$

where N = number of cells, RB1 is the resistor connected to the positive battery terminal, and RB2 is the resistor connected to the negative $SNS_{A,B}$ pins.

Although virtually any value may be chosen for RB1 and RB2 due to the high input impedance of the $BAT_{A,B}$ pin, the values selected must not be so low as to appreciably drain the battery nor so large as to degrade the circuit's noise performance. Constraining the source resistance as seen from $BAT_{A,B}$ between 20KΩ and 1MΩ is accept-voltage protection is accomplished by comparing V_{CELL}

Table 3. Suggested RB1 and RB2 Values for NiCd and NiMH Cells

Number of Cells (V_{BAT} Divisor)	RB1	RB2
3	137 KΩ	523 KΩ
4	357 KΩ	523 KΩ
5	309 KΩ	280 KΩ
6	301 KΩ	196 KΩ
7	316 KΩ	162 KΩ
8	649 KΩ	274 KΩ
9	383 KΩ	137 KΩ
10	442 KΩ	137 KΩ
12	412 KΩ	102 KΩ
14	499KΩ	102 KΩ
16	649 KΩ	113 KΩ

to the internal MCV reference. If V_{CELL} becomes greater than V_{MCV}, then charging, top-off, and trickle charge terminate, and $\overline{CH}_{A,B}$ and $\overline{FCC}_{A,B}$ outputs are high impedance.

A typical MCV value equates to 2.0V per cell. To detect the presence of a battery, the DC supply voltage must be greater than 2.0 * N, where N is the number of battery cells. Battery packs with fewer than three cells require an external amplifier to use the bq2005 (see Figure 3).

Temperature Sensing and the TCO Pin

The bq2005 uses the temperature sense input on the $TS_{A,B}$ pins to qualify charge initiation and termination. A negative temperature coefficient (RNTC) thermistor referenced to SNS and placed in close proximity to the battery may be used as a temperature-to-voltage transducer as shown in Figure 4. This example shows a simple linearization network constituted by RT1 and RT2 in conjunction with the thermistor, RT. If this temperature sensor is to be used for charge control, it should be in direct contact with the cells.

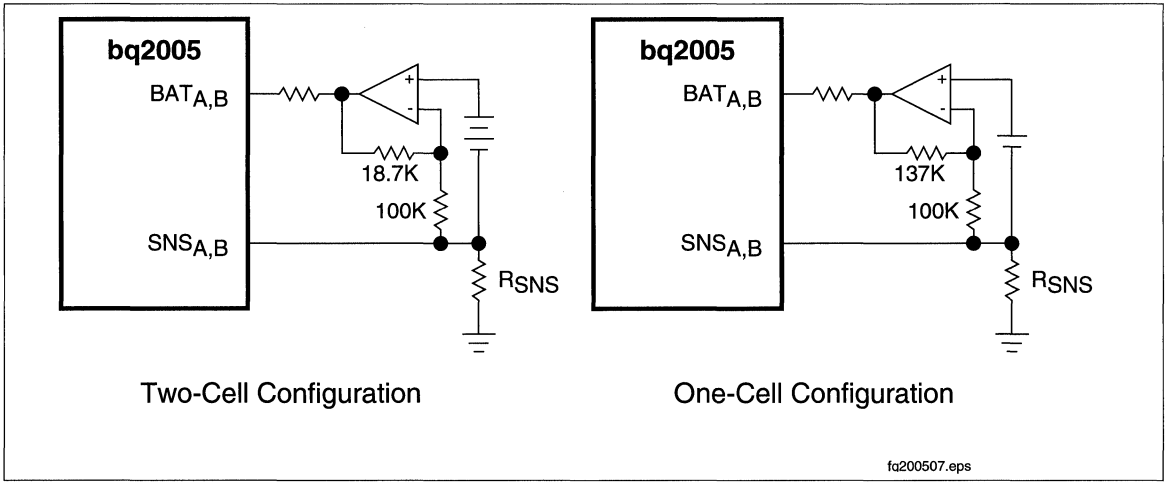


Figure 3. Battery Cell Voltage Amplifier for Fewer Than Three Cells

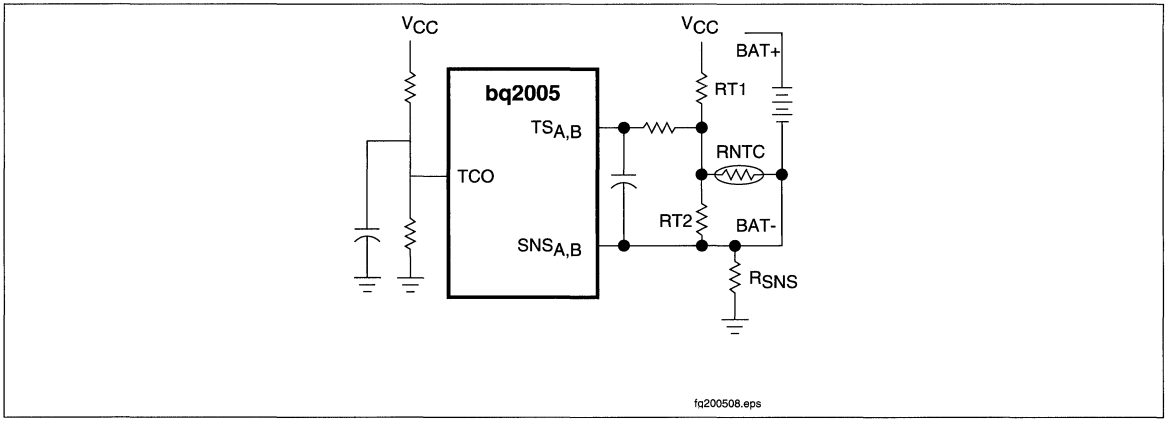


Figure 4. Temperature Sense Inputs

Temperature-decision thresholds are defined as LTF (low-temperature fault), HTF (hot-temperature fault), and TCO (temperature cutoff). Charge action initiation is inhibited if the temperature is not within the LTF-to-HTF range. In this case, $\overline{CH}_{A,B}$ is alternating high and low at a 4Hz rate, and charging does not initiate until the battery temperatures enter this range.

Once initiated, charging terminates if the temperature is either less than LTF or greater than TCO. The bq2005 interprets the reference points V_{LTF}, V_{HTF}, and V_{TCO} as V_{SS}-referenced voltages, with V_{LTF} fixed at $\frac{2}{5}$ V_{CC} and V_{TCO} equal to the voltage presented on the TCO pin. See Figure 5. Note that since the voltage on pin $TS_{A,B}$ decreases as temperature increases, V_{TCO} should always be less than $\frac{2}{5}$ V_{CC}. V_{HTF} is set internally $\frac{3}{4}$ of the way from V_{LTF} to V_{TCO}. The resistive dividers shown in Figure 4 may be used to generate the desired V_{TCO}.

$\Delta T/\Delta t$ detection adds an additional constraint on the selection of temperature sense components. Detection occurs when the voltage $TS_{A,B} - SNS_{A,B}$ declines at a rate between 0.0024 V_{CC} and 0.0040 V_{CC} per 68 seconds, with a nominal 5V V_{CC} producing a nominal detection rate of 14mV/min (16mV/68sec). For example, assuming a 1°C/min desired average $\Delta T/\Delta t$ detection rate ($T_{\Delta T}$), and minimum and maximum charge temperatures of 0° and 40°C, respectively, V_{TCO} equals:

$$V_{TCO} = (2 * V_{CC}/5) - (0.0028 * V_{CC} * (T_{TCO} - T_{LTF}))$$

$$= 2 - (0.014 * (40 - 0))$$

$$= 1.44V$$

Table 4 shows the temperature control values that apply for the application example assuming the Philips thermistor. Appendix A explains the derivation of such component values.

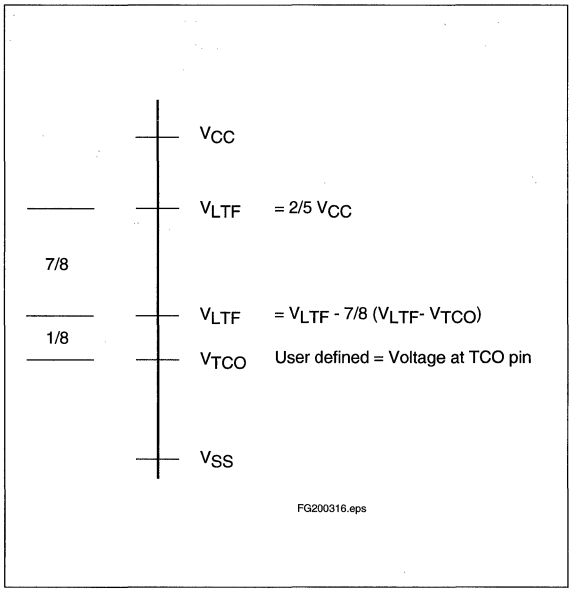


Figure 5. Temperature Reference Points

New $\Delta T/\Delta t$ samples are processed every 34 seconds. To minimize the risk of premature termination, the design should be configured assuming a minimum charge cutoff rate of 0.0024 * V_{CC}, or 10.6mV per minute (at 25°C; V_{CC} = 5V). This is the lowest signal that may be recognized as meeting the decision threshold. Repeating samples cause a decision quickly as the voltage ramps between this minimum threshold and the nominal 14mV per minute. The system is self-compensating in that the thermistor provides increasingly overstated negative voltage change with increasing temperature, making the measurement more sensitive at higher temperatures. The last three columns of Table 4 are an example of this relationship.

Table 4. Example Values, Temperature Sense Network

LTF (°C)	HTF (°C)	TCO (°C)	V_{TCO} (V)	RT1 (KΩ)	RT2 (KΩ)	$T_{\Delta T}$ (°C/min)	Minimum-to-Nominal $\Delta T/\Delta t$ Rate (°C/min)		
							@ 25°C	@ 35°C	@ 45°C
10	44.4	50	1.303	5110	4120	1.00	0.75–1.00	0.63–0.83	0.56–0.74

Notes:
1. V_{SR} = 0V.
2. Temperature control and qualification may be disabled by tying pin TCO to V_{SS} and fixing the voltage on pin $TS_{A,B}$ to 0.2 * V_{CC}.

V_{CC} Supply

The V_{CC} supply provides both power and voltage reference to the bq2005. This reference directly affects the internal time-base voltage measurements.

The time-base is trimmed during manufacturing to within 5 percent of the typical value with V_{CC} = 5V. The oscillator varies directly with V_{CC}. If, for example, a 5% regulator supplies V_{CC}, the time-base could be in error by as much as 10%.

For applications requiring even more cost-cutting measures, using a Zener diode-resistor combination as the bq2005 power supply sacrifices very little accuracy and performance. To minimize +5V loading, LEDs are cascode-driven as shown in Figure 6.

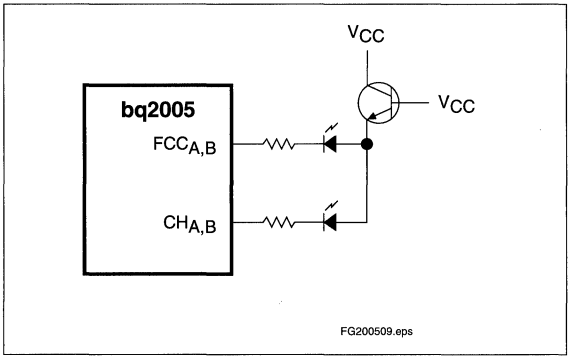


Figure 6. Cascode-Driven LEDs

The DC supply voltage, V_{DC}, must satisfy two requirements:

1. To support the bq2005 V_{CC} supply, V_{DC} must be adequate to provide for 5V regulation after the losses in the regulator and across D1 ($V_{DC} \geq 7.7V$ using the 78L05).
2. To support the proper charge operation and the rated current, V_{DC} must be greater than the number of cells * 2V + V_{LOSS} in the charging path.

Battery Removal Detection

An external 2K resistor in Figure 1 (lower left) is sized to pull $BAT_{A,B}$ above MCV with the removal of the battery. The resistance of R7 should be selected to pull the battery sense pin above MCV and yet keep input current on $BAT_{A,B}$ less than 20µA.

Top-Off Charge

The top-off charge option allows for filling up the last fraction of capacity after the fast-charge phase has terminated. Top-off is needed for NiMH batteries, which accept charge poorly at charge states above 85%. Top-off occurs at a 1/8 pulsed rate to prevent excess heat generation, and terminates after a period equal to the safety time-out. Top-off terminates if TCO or MCV is exceeded or if charge or discharge is initiated on the other battery. Top-off has a lower priority than charge; it pends until both batteries have been charged and then charges the batteries in sequence—first battery B and then battery A.

Top-off is not recommended in applications where a battery charge is re-initiated with extremely high frequency (many times per day); for example, when the unit is returned to the charge cradle after each short period of use. Top-off is also not necessary for NiCd batteries.

-Δ Voltage Fast-Charge Detection

-ΔV full-charge detection may operate in parallel with ΔT/Δt detection. If temperature control is disabled by design, then -ΔV should be enabled (DVEN tied to V_{CC}). If -ΔV is enabled, a constant-current charging source is required. Otherwise a drop in current may cause a false -ΔV determination. DVEN may change state at any time.

Mode Selection Pins TM_1 and TM_2

These two pins are used to select the safety time-out (five selections, 23 to 360 minutes) and optional top-off charge (four selections, 23 to 180 minutes, equal to the safety time selection).

The safety time-out should be selected to be longer than any reasonably expected charge time. The nominal charge time (Ah capacity/charge rate) should be increased to allow for both charge inefficiency and the fact that many batteries hold more than the rated charge. A safety time-out 1.3–1.5 times the nominal time is normally adequate (i.e., 90 minutes for a 1C charge). The safety time-out may be far in excess of the nominal charge time if temperature termination is enabled.

Note: If the charge rate varies (such as fast charging during system operation using ΔT/Δt termination), then the safety time-out selection should allow for the slowest charges that may occur. The 180- or 360-minute selection may be appropriate.

In addition to selecting the safety timer period and top-off enabled/disabled, TM_1 and TM_2 select the appropriate pulse trickle period. 1/32 is recommended for NiCd cells, while 1/64 is recommended for NiMH batteries. Top-off and pulsed trickle can be disabled by tying TM_1 and TM_2 low, selecting a six-hour charge time-out. TM_1 and TM_2 may be changed at any time during a charge cycle to select different conditions; however, changing them during charge may result in an indeterminate time-out period. TM_1 and TM_2 are held constant throughout the entire charge cycle.

System-Controlled Charge Inhibition

System control of battery charging is best accomplished by driving the temperature and voltage sense pins high, terminating or inhibiting charge. Driving $\overline{INH}$ voltage to V_{SS} results in a transition at the $BAT_{A/B}$ sense pin, terminating any fast charge, top-off, or trickle in process. When $\overline{INH}$ transitions to V_{CC}, charging is reinitiated if a battery is present and within temperature and voltage limits. See Figure 7.

Polarity Reversal Protection

If the DC input has any risk of being accidentally connected with power (+) and ground (–) reversed, then the system input should include either a protection diode to protect against circuit damage or a diode bridge to provide both protection and operation. This also increases minimum input voltage for charger operation by 1V to 2V. For maximum efficiency, a polyswitch may be used in combination with a suitably sized Schottky diode reversed across the electronics.

Layout Guidelines

PCB layout to minimize the impact of system noise on the bq2005 is important when the bq2005 is used as a switching modulator, with a separate nearby switching regulator, or close to any other significant noise source.

1. Avoid mixing signal and power grounds by using a single-point ground technique incorporating both a small signal ground path and a power ground path.
2. The charging path components and associated traces should be kept isolated from the bq2005 and its supporting components.
3. 0.1µF and 10µF decoupling capacitors should be placed close together and very close to the V_{CC} pin.

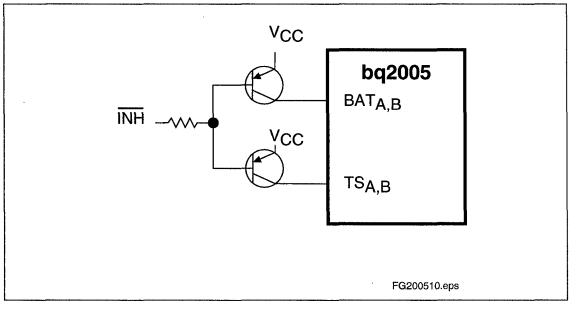


Figure 7. Inhibit Battery Charging Circuit

4. 0.1µF capacitors and resistors forming R-C filters connected to pins $BAT_{A,B}$, $TS_{A,B}$, and TCO should be as close as possible to their associated pins.
5. Because the bq2005 uses V_{CC} for its reference, additional loading on V_{CC} is not recommended.
6. Diode D1 (1N4148) is recommended for rectification and filtering.
7. If the $\overline{DCMD_A}$ input is electronically controlled, care should be taken to prevent noise-induced false transitions.
8. For bq2005-modulated switching applications:
   - A 1000pF capacitor/1KΩ resistor R-C filter should be as close as possible to the $SNS_{A,B}$ pins.
   - The 0.1µF capacitors for $BAT_{A,B}$ and $TS_{A,B}$ should be routed directly to $SNS_{A,B}$ and not to ground.

Application Example 1: Linear Regulator

In the frequency-modulated example of Figure 8, the bq2005 is used to implement a linear regulator/charge controller that can charge 4, 5, 6, 8, or 10 NiCd or NiMH cells (selected by JP4 and JP5) by controlling the base drive to a series pass PNP transistor. The current must be limited to stay within the power dissipation of the transistor in free air or connected to an appropriately sized heat sink. Table 5 contains the parts list for the board.

Charge is initiated on battery replacement or power-up. Jumper JP1 controls -ΔV detection: selecting V_{CC} enables -ΔV and GND disables it. Switch SW1 controls discharge of battery A. HTF = 48°C, TCO = 48°C, and LTF = 10°C for the component values listed in Table 6 for RTB1, RBT2, R5, and R6 with a Philips thermistor (Part No. 2322-640-63103) with ΔT/Δt termination set for 1°C/minute at 30°C.

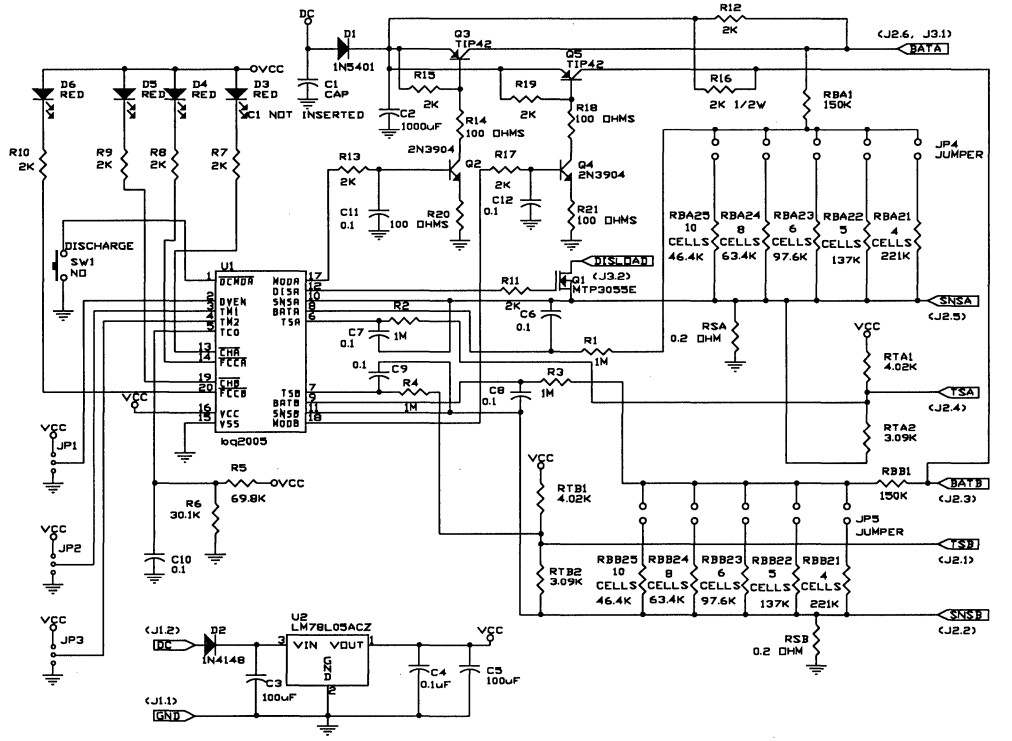
Safety time-out is selected by programming TM1 and TM2 with jumpers JP2 and JP3, respectively. To customize the design for a specific application, ensure that the power components are rated for the stresses they must handle. Charge current is a function of $RS_{A,B}$ and an internal bq2005 threshold:

$$I_{CHARGE} \approx \frac{0.225V}{RS_{A,B}}$$

The source power supply must provide sufficient voltage differential to the battery to account for losses in polarity protection diodes or resistive drops.

The selection of component values for R13, R17, C11, and C12 in this example affects the switching frequency of MOD and the delay to full current sense at the sense

pins of the bq2005. Although the effects on fast charge and top-off are minimal because the delay is small compared to the total time, the effect on pulse-trickle charge is significant. Transistors Q2 and Q4 may not turn on in some cases, which may be advantageous if no trickle charge is desired.



Thermistor values :

Thermistor	RT1	RT2
Keystone RL0703-5744-103-S1	3.83K	2.94K
Philips 2322-640-63103	4.02K	3.09K
Fenwal Type 16, 197-103LA6-A01	4.02K	3.09K
Ozhumi 150-108-00(4)	4.64K	3.74K
Semetic 103AT-2	4.87K	4.02K

BD-202

Figure 8. Linear Regulator/Charge Controller

Table 5. Linear Regulator/Charge Controller Board Parts List

Component Name	Quantity	Component Description
C1, C2	1	1000µF 25V aluminum (C1 is optional—not stuffed)
C3	1	100µF 25V aluminum
C5	1	100µF 6.3V aluminum
C4, C6, C7, C8, C9, C10, C11, C12	8	0.1µF ceramic
D1	1	1N5400
D2	1	1N4148
D3, D4, D5, D6	4	HMLP-D150 HP LED
J1, J3	2	2-position terminal block
J2	1	6-position terminal block
JP1, JP2, JP3	3	3-pin single-row header
JP4, JP5	2	12-pin dual-row header
JP6	1	2-pin single-row header
Q1	1	MTP3055EL FET
Q2, Q4	2	2N3904
Q3, Q5	2	TIP42
R1, R2, R3, R4	4	1MΩ 5% ¼W
R5	1	69.8KΩ 1% ¼W
R6	1	30.1KΩ 1% ¼W
R7, R8, R9, R10, R11, R12, R13, R15, R16, R17, R19	11	2KΩ 5% ¼W
R14, R18, R20, R21	2	100Ω 5% ¼W
RBA1, RBB1	2	150KΩ 1% ¼W
RBA21, RBB21	2	221KΩ 1% ¼W
RBA22, RBB22	2	137KΩ 1% ¼W
RBA23, RBB23	2	97.6KΩ 1% ¼W
RBA24, RBB24	2	63.4KΩ 1% ¼W
RBA25, RBB25	2	46.4KΩ 1% ¼W
RSA, RSB	2	0.2Ω 1% 3W wirewound Dale LVR3
RTA1, RTB1	2	4.53KΩ 1% ¼W
RTA2, RTB2	2	3.57KΩ 1% ¼W
S1	1	SPST momentary switch, Panasonic P8008S
U1	1	bq2005
U2	1	LM78L05ACZ
Heatsink	1	Thermalloy 6298B
Mounting kit	2	TO-220
Socket	1	20-pin solder tail ICO-203-58-T
PCB	1	DV2005L1
Screws	4	6-32 thread x ¼inch
Legs	4	Stand-off ½inch 6-32 thread

Application Example 2: Single Magnetics Low-Cost Dual-Switching Charger

Figure 9 illustrates a low-cost dual-sequential switching charger using a small, low Q inductor to speed up the bipolar transistor commutation. Table 6 contains the parts list for the board. Bipolar transistors Q2 and Q5 are used to multiplex the energy stored in L1 by the charger's charge cycles.

Transistor Q3 is used to switch energy into L1 from the power source. Low-Q inductor L2 helps to turn Q3 off to limit its power dissipation. This circuit has the advantage of using bipolar transistors with saturation voltages far below the IR drops of comparably sized p-channel MOSFETs. This also results in significant cost savings. Designers must use care in selecting Q3 for suitability as a switching transistor. The Zetex Super-E line is ideal for applications up to 3A.

Layout guidelines are described on page 8. Possible layout concerns include:

- Diode D2 is installed to catch inductor energy in the event of battery removal during charge.
- Battery voltage differentials are applied to the base-emitter junctions of transistors Q5 and Q2 in the reverse direction. (Although the bq2005 will not charge a shorted battery, the design should ensure that Q5 and Q2 are protected if the battery could be shorted during charge.)

Q3 must be a high-speed switching transistor with suitably high V_{CE} rating for the application. The ZTX789A has a breakdown rating of 25V and a continuous current rating of 3A. This transistor's high gain enables it to saturate to a very low V_{CE} (< 0.25V) at 2A. The "on-time" power dissipation makes up most of the component power loss, but the switching loss must be added to give a complete picture of the transistor's required power dissipation.

A good switching transistor is gauged by its transition frequency (F_T) rating. A transistor with an F_T rating of >50MHz is a superior switching transistor for a switch-mode application, whereas a transistor with an F_T of 10MHz may be usable. In this example, the ZTX789A has an F_T of 100MHz. Manufacturers sometimes cite turnoff time as a sum of storage and fall time; some cite these values independently. The turnoff time is important for frequency selection, but the fall time is critical to determine power dissipation.

The influence of fall time on power dissipation can be estimated using the following formula:

$$P_{SW} = F \times T_F \times V_{IN} \times \frac{I_P}{6}$$

where:

P_{SW} = Power loss when switching

F = Switching frequency

T_F = Fall time

V_{IN} = Maximum input voltage

I_P = Peak switching current

Component power dissipation is the sum of P_{SW} and P_{ON}, which is estimated from the following formula:

$$P_{ON} = \frac{V_{BAT}}{V_{IN}} \times V_{CESAT} \times I_{AV}$$

where:

P_{ON} = Power dissipation when the transistor is on

V_{BAT} = Battery voltage

V_{IN} = Input voltage

V_{CESAT} = Maximum transistor saturation voltage

I_{AV} = Average battery charge current

The Zetex E-line package can dissipate the heat resulting from this design in free air.

Other switching transistors that may be useful in applications up to 3A are the MJE210 and the D45H series transistors. Q2 and Q5 are selected for high HFE and low V_{CESAT}.

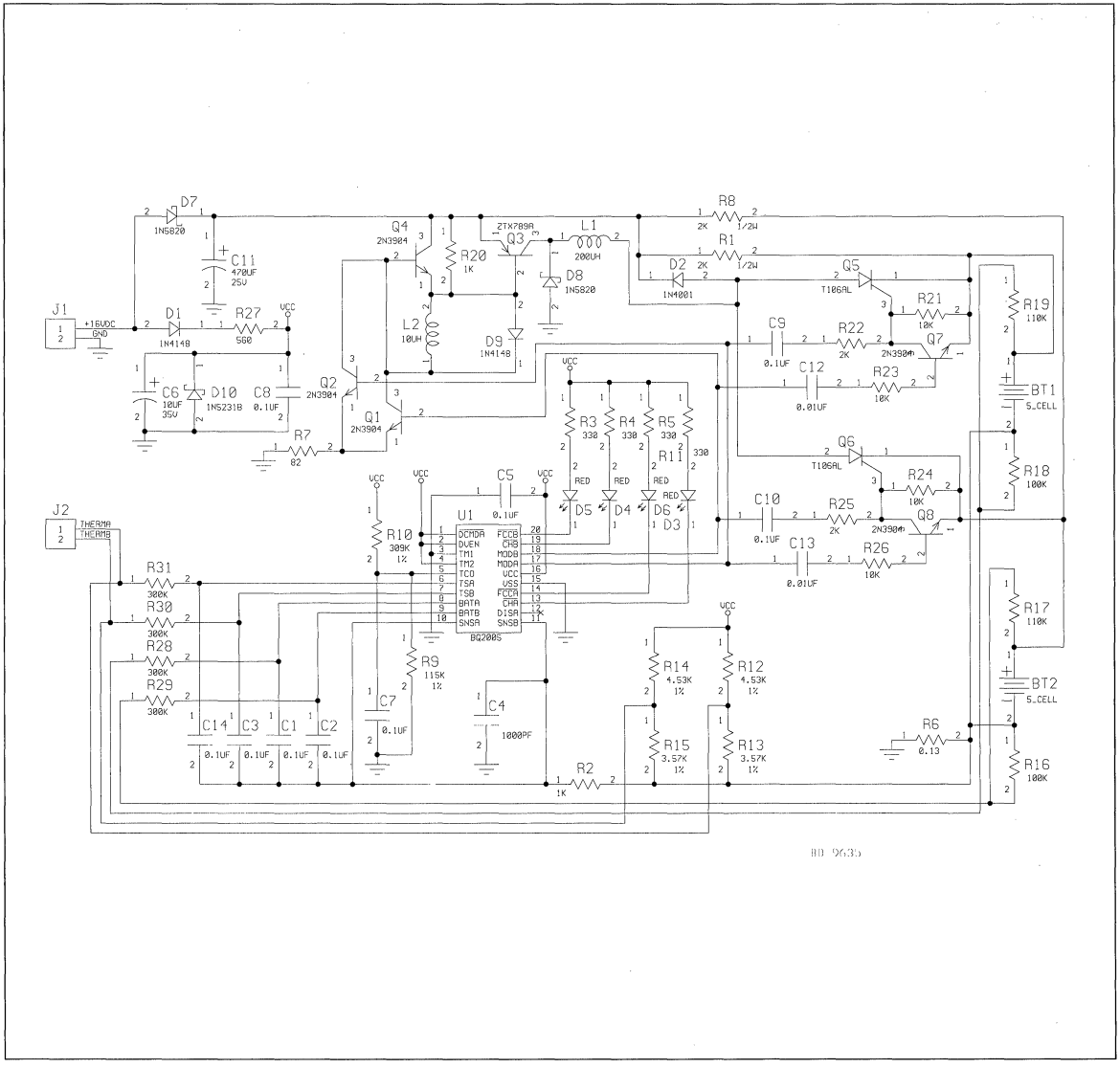


Figure 9. Single-Magnetics Low-Cost Dual-Switching Charger

Table 6. Single-Magnetics Low-Cost Dual-Switching Parts List

Component Name	Quantity	Component Description
C1, C6	2	1000pF 50V ceramic
C2, C3, C4, C5, C7, C10, C11, C12, C13	9	0.1µF 50V ceramic
C14, C15	2	0.01µF 50V ceramic
C8	1	10µF 35V aluminum
C9	1	470µF 35V aluminum
D1, D9	2	1N4148
D2	1	1N4001
D3, D4, D5, D6	4	HMLP-D150 red HP LED
D7, D8	2	1N5820 Schottky
D10	1	1N5231B Zener
L1	1	200µH toroid inductor
L2	1	10µH J.W. Miller 78F100J
Q1, Q2, Q4, Q7, Q8	5	2N3904
Q3	1	ZTX789A, Zetex high gain, med. power
Q5, Q6	2	T106A1, Teccor 4A SCR
R1, R10, R28, R31	4	2KΩ 5% ¼W carbon film
R2, R3, R26	3	1KΩ 5% ¼W carbon film
R4, R5, R6, R13	4	330Ω 5% ¼W carbon film
R7, R8	2	0.13Ω 5% 1W metal oxide
R9	1	82Ω 5% ¼W carbon film
R11	1	115KΩ 1% ¼W metal film
R12	1	309Ω 1% ¼W metal film
R14, R16	2	4.53KΩ 1% ¼W metal film
R15, R17	2	3.57KΩ 1% ¼W metal film
R18, R20	2	100KΩ 5% ¼W carbon film
R19, R21	2	110KΩ 5% ¼W carbon film
R22, R23, R24, R25	4	1MKΩ 5% ¼W carbon film
R27, R29, R30, R32	4	10KΩ 5% ¼W carbon film
R33	1	560Ω 5% ¼W carbon film
U1	1	bq2005

Application Example 3: P-Channel MOSFET Buck-Topology Switch-Mode Charger

In this example, the bq2005 is used to implement a switching regulator/charge controller that can charge 4 to 10 NiCd or NiMH cells with current regulated up to 3A.

Figure 10 is a standard configuration for a p-FET switch-mode charger. MOD drives a small signal DMOS FET, Q2/Q5. When MOD is high, Q2/Q5 is on, turning on Q4/Q7 via the path through D8/D12 and D11/D7.

L1/L2 inductor current ramps up linearly while MOD is high. L1/L2 current is in series with the battery and RSA or RSB. The inductor current ramps up linearly until V_{SNS} reaches 0.250V, at which time MOD goes low and Q4/Q7 turns off. A flux reversal occurs in L1/L2, causing D9/D13 to conduct. Charge is now being transferred from L1/L2 into the battery. The L1/L2 current ramps down linearly until V_{SNS} reaches 0.20V. At this point the cycle repeats with MOD going high.

For input voltages that are higher than the rated Q4/Q7 safe operating gate voltage, Zener diode D7/D11 can be placed in series with the drain lead of Q2/Q5. The Zener voltage should be sized to allow full Q4/Q7 enhancement while Q2/Q5 is conducting. See Table 7.

Capacitor C2 is used to provide a low-impedance for the Q2/Q5 source lead. Without C2 in place, Q2/Q5 can be connected to an overly inductive voltage supply. D1 is a blocking diode that keeps the battery from discharging via U2 during removal of the DC power source input.

Charge is initiated on battery replaced or V_{CC} valid. -ΔV detection can be enabled (DVEN high), and discharge control is through $\overline{DCMD}$ (SW1 low). MCV = 1.8V; LTF = 10°C; TCO = 50°C; $\Delta T/\Delta t$ at 30°C = 0.82°C/min. (i.e., typical = 1.10°C/min.). Timer-mode selection (see data sheet) and resistor R15/R17 are determined by the designer. RSA/RSB is selected such that $I_{CHG} * RSA/RSB = 0.225V$.

The values of RB1 and RB2 to complete this schematic may be selected from Table 3.

Note: Temperature control and qualification may be disabled by tying the TCO pin to V_{SS} and fixing the voltage on the $TS_{A,B}$ pins to $0.1 * V_{CC}$.

Table 8 lists suggested components for different-rate chargers. Table 9 lists other components shown in Figure 10.

Table 7. Lookup Table for D7/D11 Selection

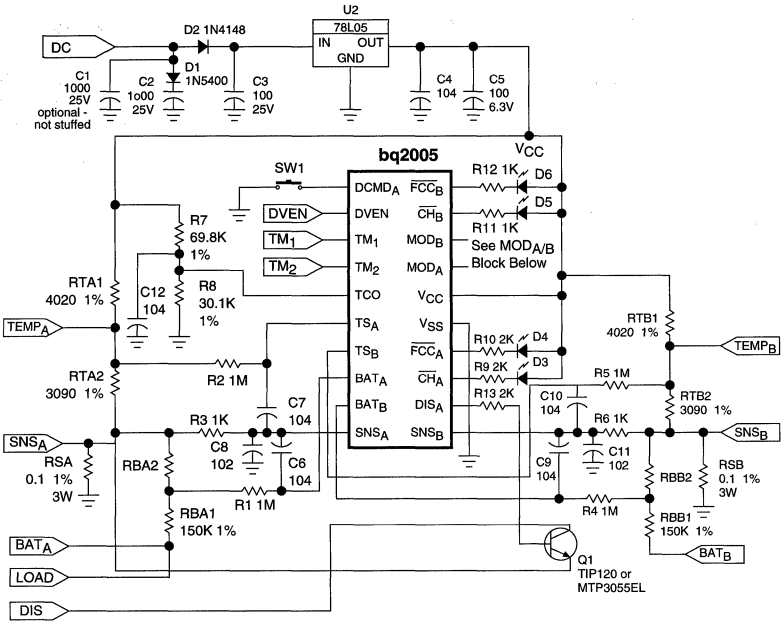
+VDC Input (Volts)	Motorola Part No.	Nominal Zener Voltage
Below 15	Shorted	0
15–18	1N749	4.3
18–21	1N755	7.5
21–24	1N758	10
24–27	1N964A	13
27–30	1N966A	16
30–32	1N967A	18
32–35	1N968A	20

Table 8. Suggested Components—P-Channel MOSFET Charger

Suggested Max. Charging Current	Q4/Q7	D9/ D13	D10/ D14	L1/L2
1A	IRF9Z14	1N4001	1N5818	30 turns, #26 AWG, wound on Magnetics, Inc., P/N 77040 core; nominal inductance 59µH; GFS Mfg., Inc., P/N 92-2156-1
2A	IRF9Z24	1N5821	1N5821	37 turns, #22 AWG, wound on Magnetics, Inc., P/N 77120 core; nominal inductance 98µH; GFS Mfg., Inc., P/N 92-2157-1
3A	IRF9Z34	1N5821	1N5821	
Source	International Rectifier	Motorola	Motorola	GFS Mfg., Inc. Dover, NH (603) 742-4375

Table 9. Other Components—P-Channel MOSFET Charger

Component Name	Component Description
C1, C2	1000µF 5V electrolytic
C3	100µF 25V electrolytic
C4, C6, C7, C9, C10, C12	0.1µF ceramic
C5	100µF 6.3V electrolytic
C8, C11	1000pF ceramic
D1	1N5400
D2, D8, D12	1N4148
D3, D4, D5, D6	HLMP 4700 red LED
D7/D11	Optional Zener; see Table 9
D9/D13	1N5821
D10/D14	1N4001
Q1	TIP120 or MTP3055EL
Q2, Q5	2N7000
Q3, Q6	2N3904
Q4/Q7	MTP23P06
R1, R2, R4, R5	1MΩ 5% ¼W or ⅛W
R3, R6	1KΩ 5% ¼W
R7, R8	User-defined 1% ¼W or ⅛W
R9, R10, R11, R12, R13	2KΩ 5% ¼W or ⅛W
R14/R16	6.8KΩ 5% ¼W or ⅛W
RSA, RSB	0.1Ω 1% 3W
RBA1, RBB1	150KΩ 1% ¼W or ⅛W
RBA2, RBB2	User-defined 1% ¼W or ⅛W
RTA1, RTB1	User-defined 1% ¼W or ⅛W
RTA2, RTB2, R15, R17	User-defined 1% ¼W or ⅛W
L1/L2	See Table 10
U1	bq2005
U2	LM78L05ACZ



Thermistor Values:

Thermistor	RT1	RT2
Keystone RL0703-5744-103-S1	3.83K	2.94K
Philips 2322-640-63103	4.02K	3.09K
Fenwal Type 16, 197-103LA6-A01	4.02K	3.09K
Ozhumi 150-108-00(4)	4.64K	3.74K
Semetic 103AT-2	4.87K	4.02K

Notes: All 104 capacitors are 0.1µF ceramic.
All 102 capacitors are 0.001µF ceramic.

FG200511.eps

Notes: All 104 capacitors are 0.1µF ceramic.
All 102 capacitors are 0.001µF ceramic.

Figure 10. P-Channel MOSFET Switching-Mode Charger

Appendix A
Determining Temperature-Control Component Values

The bq2005 uses a negative temperature coefficient (NTC) thermistor to determine temperature. The ΔT/Δt sensitivity can be adjusted using different resistor values (RT1 and RT2 in Figure 1 and the application example) and a different high-temperature cutoff voltage. Table A-1 lists various thermistor manufacturers, with the appropriate part numbers.

Follow these steps to determine temperature-control component values (see Figure 6):

1a. The low-temperature fault (LTF) limit for charging must be established. LTF for charging is determined by the battery specification and the charge rate used. A typical value for the low-temperature limit is 10°C.

b. V_{LTF} is set within the bq2005 at $0.4 * V_{CC}$.

2a. The high-temperature cutoff (TCO) for charging must be established. TCO for charging is determined by the battery specification, the charge rate, and the heat dissipation of the system. Typical values range from 40°C to 50°C, although values outside this range may be applicable.

b. The average ΔT/Δt sensitivity from LTF to TCO ($T_{\Delta T}$, expressed as °C/minute) for termination must be established. As mentioned in this application note, the bq2005 provides a typical ΔT/Δt charge termination of 14 mV per minute. The $T_{\Delta T}$ value is determined by the battery specification, the charge rate, and the heat dissipation of the system. Typical nominal values for $T_{\Delta T}$ range from 0.75°C/min to 1.5°C/min.

Relative to the average value $T_{\Delta T}$, the minimum-to-maximum range of ΔT/Δt at a specific temperature depends on two parameters:

- The measurement resolution of the bq2005, which contributes a ±25% error.
- The non-linearity of the thermistor between LTF and TCO. As the temperature nears LTF, the expected ΔT/Δt is less than $T_{\Delta T}$ (less sensitive), and as the temperature nears TCO, the expected ΔT/Δt is more than $T_{\Delta T}$ (more sensitive).

The ΔT/Δt range should be considered in determining the nominal $T_{\Delta T}$. Nominal $T_{\Delta T}$ should be selected so that its minimum value represents an acceptable (non-premature) termination threshold. Thus a first bq2005 sample does not cause a premature termination. Multiple sampling ensures that the termination occurs well before the $T_{\Delta T}$ max.

c. The high-temperature cutoff voltage, V_{TCO}, must be established. This V_{TCO} limit is determined by the $T_{\Delta T}$ and may be calculated by:

$$V_{TCO} = (2 * V_{CC}/5) - [(0.0028 * V_{CC} * (TCO - LTF)) / T_{\Delta T}]$$

V_{TCO} is provided at the TCO pin by a resistor-divider network as shown in Figures 8 and 9: $V_{TCO} = V_{CC} * R1 / (R1 + R2)$.

4. Select the thermistor to be used. If it is not from Table A-1, the thermistor sensitivity at 25°C should be at least -4% and the ΔR steps between 30°C and 50°C should be comparable to or greater than those in Table A-1 to obtain the appropriate accuracy. Lower values affect the linearity of the ΔT/Δt.

5. Determine the thermistor resistance at LTF and TCO (R_{LTF} and R_{TCO}, respectively). This may be done using the thermistor temperature versus resistance conversion table provided with the thermistor specification. These tables are usually in 5°C increments.

6. The values for RT1 and RT2 may be calculated by:

$$T1 = R_{LTF} * (1 - (2 / V_{CC})) / (2 / V_{CC})$$

$$T2 = R_{TCO} * (1 - (V_{TCO} / (V_{CC} - V_{SNS}))) / (V_{TCO} / (V_{CC} - V_{SNS}))$$

$$RT2 = ((T2 * R_{LTF}) - (T1 * R_{TCO})) / (T1 - T2)$$

$$RT1 = (RT2 * T1) / (R_{LTF} + RT2)$$

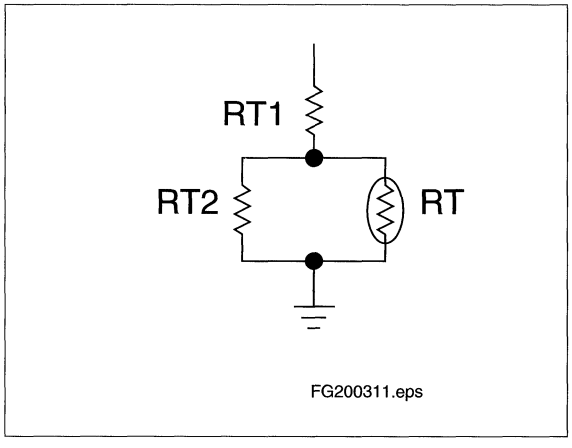


Figure A-1. Resistor Network

Table A-1. 10K NTC Thermistor Types and Resistance Values

Temperature (°C)	Nominal Resistance (Ω) at Temperature			
	Keystone Carbon Co. RL0703-5744-103-S1 (Tel: 814/781-1591)	Philips Components 2322-640-63103 (Tel: 407/743-2112)	Fenwal Electronics Type 16; 197-103LA6-A01 (Tel: 508/478-6000)	Thermometrics C100Y103J (Tel: 908/287-2870)
-30	188172	173900	177000	-
-25	138043	128500	-	-
-20	102263	95890	97070	-
-15	76461	72230	-	-
-10	57672	54890	55330	-
-5	43864	42070	-	-
0	33630	32510	32650	29588
5	25988	25310	-	23515
10	20243	19860	19900	18813
15	15889	15690	-	15148
20	12562	12490	12490	12271
25	10000	10000	10000	10000
30	8013	8060	8057	8195
35	6461	6536	-	6752
40	5241	5331	5327	5593
45	4276	4373	-	4656
50	3507	3606	3603	3894
55	2894	2989	-	3273
60	2400	2490	2488	2762
65	2001	2085	-	2342
70	1677	1753	1752	1993.7
75	1412	1481	-	1704.0
80	1194	1256	1258	1462.0
85	1014	1070	-	1259.1
90	865.2	915.5	917.7	1088.3
95	741.0	786.1	-	943.9
100	636.9	677.5	680.0	821.4

U-508 Using the bq2007

Display Mode Options

Introduction

The bq2007 Fast Charge IC provides flexibility with a wide variety of charge status monitor display mode formats. The bq2007 internal charge status monitor can be configured to support up to a seven-segment bargraph or a single BCD digit display. The bargraph display indicates up to seven monotonic steps, whereas the BCD digit indicates ten steps of 10% increments. The bq2007 output drivers can direct-drive either LCD or LED interface levels.

Display Driver Modes

The bq2007 is designed to interface directly with LCD or LED type displays. The display driver mode is selected with the soft-programmed input MSEL and is independent of the state-of-charge monitor format or indications. The LED signal levels are driven when the MSEL soft-programmed input is pulled to V_{CC} at initialization. The output pin COM is the common-anode connection for LED SEG_{A-G}. See Figure 1.

The LCD interface mode is enabled when the MSEL soft-programmed input is pulled to V_{SS} at initialization. An internal oscillator generates all timing signals required for the LCD interface. Output pin COM is the common connection for static direct-driving of the LCD display backplane and is driven with an AC signal at the frame period. When enabled, each of the SEG_{A-G} pins are driven with the correct-phase AC signal to activate the LCD segment. See Figure 1.

Charge Status Indication

Table 1 summarizes the bq2007 charge status display indications. The charge status indicators include the DIS output, which can be used to indicate the discharge state, the audio ALARM output, which indicates charge completion and fault conditions, and the dedicated status outputs, LED_1 and LED_2.

Outputs LED_{1-2} have three display modes that are selected at initialization by the input pins $DSEL_1$ and $DSEL_2$. The $DSEL_1$ and $DSEL_2$ input pins, when pulled down to V_{SS}, are intended for implementation of a simple two-LED system, where LED_1 indicates the precharge status (i.e., charge pending and discharge) and LED_2 indicates the charge status (i.e., charging and completion). $DSEL_1$ pulled up to V_{CC} and $DSEL_2$ pulled down to V_{SS} mode allows the implementation of a single tri-color LED such that discharge, charging, and completion each have a unique color. $DSEL_1$ pulled down to V_{SS} and $DSEL_2$ pulled up to V_{CC} mode allows for fault status information. See Figure 2.

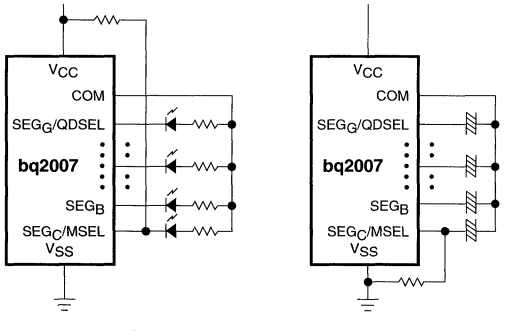


Figure 1. Display Driver Configurations

Using the bq2007 Display Mode Options

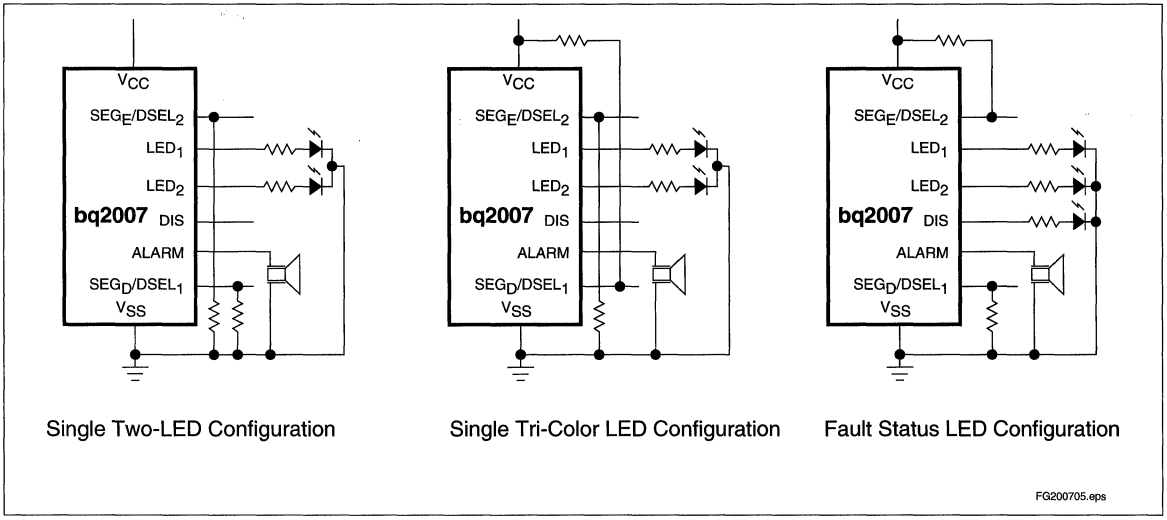


Figure 2. Charge Status Display Configurations

Table 1. bq2007 Charge Status Display Summary

Mode	Charge Action State	LED_1	LED_2	DIS	ALARM
$DSEL_1$ = L $DSEL_2$ = L (Mode 1)	Battery absent	0	0	0	0
	Charge pending (temp. limit, low voltage)	0	Flashing	0	0
	Discharge in progress	0	1	1	0
	Charging	Flashing	0	0	0
	Charge complete	1	0	0	High tone
	Fault (low-voltage time-out)	0	0	0	High tone
$DSEL_1$ = H $DSEL_2$ = L (Mode 2)	Battery absent	0	0	0	0
	Discharge in progress, pending	1	1	1	0
	Charging	1	0	0	0
	Charge complete	0	1	0	High tone
	Fault (low-voltage time-out)	0	0	0	High tone
$DSEL_1$ = L $DSEL_2$ = H (Mode 3)	Battery absent	0	0	0	0
	Charge pending (temp. limit, low voltage)	0	Flashing	0	0
	Discharge in progress	0	Flashing	1	0
	Charging	Flashing	0	0	0
	Charge complete	1	0	0	High tone
	Fault (low-voltage time-out)	0	1	0	High tone

Note: 1 = on; 0 = off; L = pulled down to V_{SS}; H = pulled up to V_{CC}.

Audio Output Alarm

The bq2007 audio alarm output generates an audio tone to indicate a charge completion or fault condition. The audio alarm output is a symmetrical duty-cycle AC signal that is compatible with standard piezoelectric alarm elements. A valid battery insertion is indicated by a single 3.5kHz beep of ½-second typical duration. The charge completion and fault conditions are indicated by a 9.5- to 15-second high-tone sequence of ½-second typical duration at a 2-second typical repetition rate.

Charge Status Monitoring

The bq2007 charge status monitor may display the battery voltage or charge safety timer as a percentage of the full-charged condition. These options are selected with the MULT soft-programmed input pin.

When MULT is pulled down to V_{SS}, the battery charge status is displayed as a percentage of the battery voltage, and the single-cell battery voltage at the BAT pin is compared with internal charge voltage reference thresholds. When V_{BAT} is greater than the internal thresholds of V_{20}, V_{40}, V_{60}, or V_{80}, the respective 20%, 40%, 60%, or 80% display outputs are activated. The battery voltage directly indicates 20% charge increments, while the 10% charge increments use a timer that is a function of the charge safety timer.

When MULT is pulled down to V_{SS} and when V_{BAT} exceeds V_{20} during charging, the 20% charge indication is activated and the timer begins counting for a period equal to $1/64$ to $1/32$ of the charge safety time-out period. When the timer count is completed, the 30% charge indication is activated. Should V_{BAT} exceed V_{40} prior to the timer count completion, the charge status monitor activates the 30% and 40% indications. This technique is used for all the odd percentage charge indications to assure a monotonic charge status display.

When MULT is pulled up to V_{CC}, the bq2007 charge status monitor directly displays $1/32$ of the charge safety timer as a percentage of the full-charge time. This method is recommended over the voltage-based method when charging packs with different cell configuration (i.e. 5-cell or 6-cell pack) where the battery terminal voltages will vary greatly between packs. This method offers an accurate charge status indication when the battery is fully discharged. When using the timer-based method, discharge-before-charge is recommended.

During discharge with MULT pulled down to V_{SS}, the charge status monitor indicates the percentage of the battery voltage by comparing V_{BAT} to the internal discharge voltage reference thresholds. In BCD format, the discharge thresholds V80, V60, V40, and V20 correspond to a battery charge state indication of 90%, 70%, 50%, and 30%, respectively. In bargraph format, the same discharge thresholds correspond to a battery charge state indication of 90%, 60%, 40%, and 30%, respectively. Differences in the battery charge state indications are due to the finer granularity of the BCD versus the bargraph format.

During discharge and when MULT is pulled up to V_{CC}, the state-of-charge monitor BCD format displays the discharge condition, letter "d," whereas the bargraph format has no indication.

The charge status display is blanked during the charge pending state and when the battery pack is removed.

Charge Status Display Modes

The bq2007 charge status monitor can be displayed in two modes summarized in Table 2. The display modes are a seven-segment monotonic bargraph or a seven-segment BCD single-digit format. When QDSEL is pulled down to V_{SS}, pins SEG_{A-G} drive the decoded seven segments of a single BCD digit display, and when QDSEL is pulled up to V_{CC}, pins SEG_{A-G} drive the seven segments of a bargraph display.

In the bargraph display mode, outputs SEG_{A-G} allow options for a three-segment to seven-segment bargraph display. The three-segment charge status display uses outputs SEG_B, SEG_D, and SEG_F for 30%, 60%, and 90% charge indications, respectively. The four-segment charge status display uses outputs SEG_A, SEG_C, SEG_D, and SEG_E for 20%, 40%, 60%, and 80% indications, respectively. The seven-segment charge status monitor uses all segments. See Figure 3.

The BCD display mode drives pins SEG_{A-G} with the decoded seven-segment single-digit information. The display indicates in 10% increments from a BCD zero count at charge initiation to a BCD nine count indicating 90% charge capacity. Charge completion is indicated by the letter "F," a fault condition by the letter "E," and the discharge condition by the letter "d." See Figure 4.

Table 2. bq2007 Charge Status Display Summary

Mode	Display Indication	SEG_A	SEG_B	SEG_C	SEG_D	SEG_E	SEG_F	SEG_G
QDSEL = H	20% charge	1	0	0	0	0	0	0
	30% charge	1	1	0	0	0	0	0
	40% charge	1	1	1	0	0	0	0
	60% charge	1	1	1	1	0	0	0
	80% charge	1	1	1	1	1	0	0
	90% charge	1	1	1	1	1	1	0
	Charge complete	1	1	1	1	1	1	1
QDSEL = L	0% charge—digit 0	1	1	1	1	1	1	0
	10% charge—digit 1	0	1	1	0	0	0	0
	20% charge—digit 2	1	1	0	1	1	0	1
	30% charge—digit 3	1	1	1	1	0	0	1
	40% charge—digit 4	0	1	1	0	0	1	1
	50% charge—digit 5	1	0	1	1	0	1	1
	60% charge—digit 6	1	0	1	1	1	1	1
	70% charge—digit 7	1	1	1	0	0	1	0
	80% charge—digit 8	1	1	1	1	1	1	1
	90% charge—digit 9	1	1	1	1	0	1	1
	Charge complete—letter F	1	0	0	0	1	1	1
	Fault condition—letter E	1	0	0	1	1	1	1
	Discharge—letter d	0	1	1	1	1	0	1

Note: 1 = on; 0 = off; L = pulled down to V_{SS}; H = pulled up to V_{CC}.

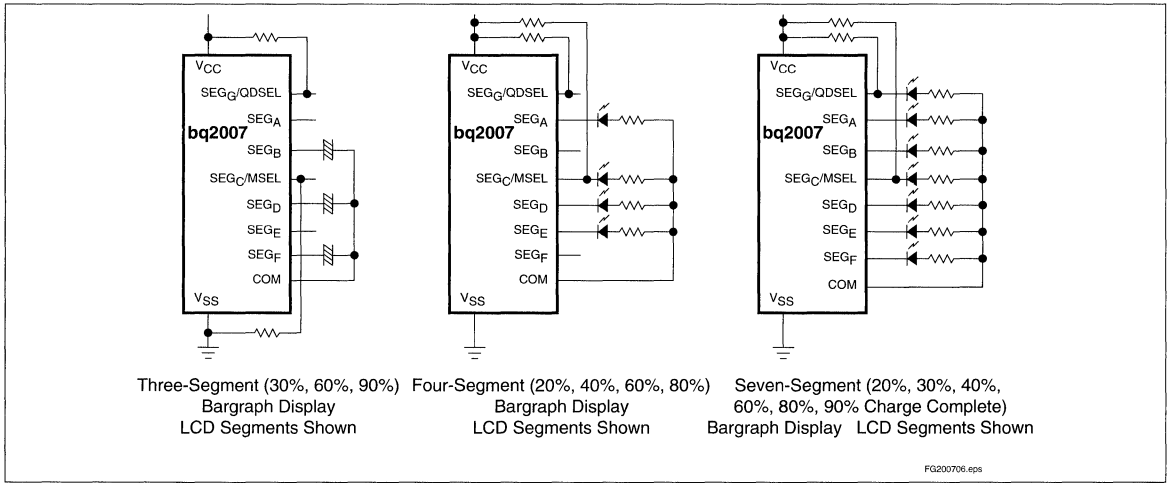


Figure 3. Charge Status Bargraph Display Configurations

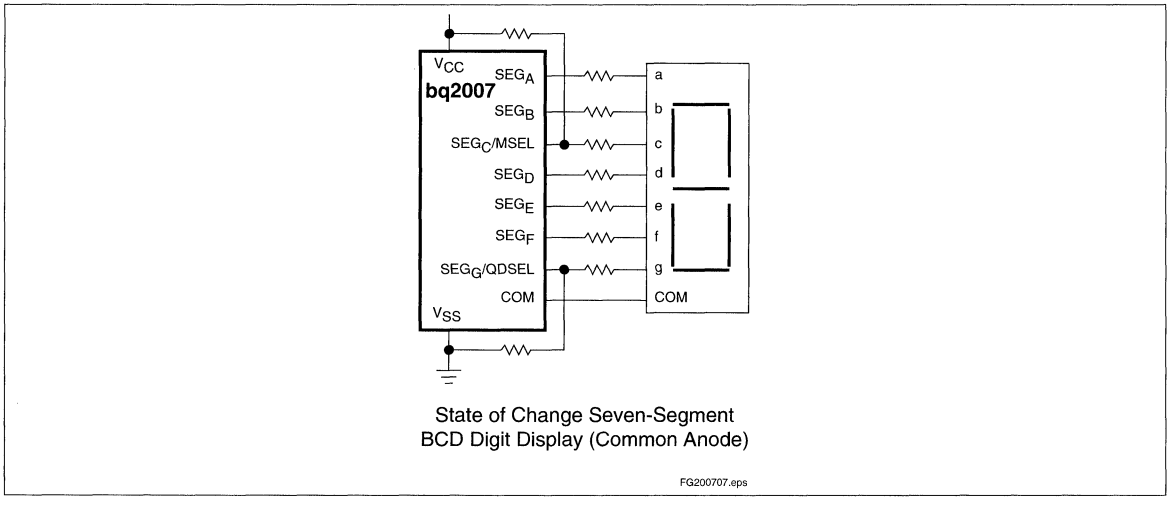


Figure 4. Charge Status BCD Digit Display Mode

UNITRODE

U-509 Using the bq2007 Enhanced Features for Fast Charge

Introduction

This application note describes the correct setup of the bq2007 features and gives design examples for a NiCd or NiMH switch-mode and gated current source fast-charger applications.

The bq2007 is targeted for applications requiring fast-charging and charge status monitoring at minimal cost. It provides sophisticated full-charge detection techniques such as PVD (peak voltage detection) and -ΔV (negative delta voltage) that enable the user to take advantage of advanced battery technologies such as nickel metal-hydride (NiMH) and high-capacity fast-charge nickel cadmium (NiCd).

The bq2007 offers flexibility by providing a wide variety of charge status monitoring and charge state display formats. The internal charge status monitor can be configured to support up to a seven-segment bargraph or a single-digit display. The bargraph display indicates seven monotonic steps, whereas the single digit counts in ten steps of 10% increments. The output can direct-drive either LCD or LED interface levels.

The bq2007 indicates charge state status with an audio alarm output option and two dedicated output pins with programmable display options. The $DSEL_{1-2}$ inputs can select one of the three display modes for the LED_{1-2} outputs.

Background

A significant advantage of the bq2007 over other fast-charge solutions is the flexibility to select PVD or -ΔV as the primary decisions for fast-charge termination. PVD is the recommended termination method for NiMH batteries, while -ΔV is recommended for NiCd batteries. -ΔV or PVD detection in the bq2007 may be temporarily disabled during periods when the charge current fluctuates. -ΔV or PVD may be permanently disabled without affecting other bq2007 charge-termination functions.

The bq2007 provides battery protection by trickle-charge conditioning of a battery that is below the low-voltage threshold (V_{EDV}). The battery voltage (V_{CELL}) is compared to the low-voltage threshold (V_{EDV}) and charge will be inhibited if $V_{CELL} < V_{EDV}$. The condition trickle current and fault time-out are a percentage of the fast charge rate and maximum time-out (MTO).

To ensure safety for the battery and system, fast charging also terminates based on a high-temperature cutoff threshold (TCO), a safety time-out, and a maximum cell voltage threshold (MCV). To avoid possible premature fast-charge termination when charging batteries after long periods of storage, the bq2007 disables PVD, and -ΔV detection during a short "hold-off" period at the start of fast charge. During the hold-off period when fast charge is selected, the bq2007 charges at the topoff rate to prevent excessive overcharging of a fully charged battery. This hold-off period is configured as described in the bq2007 data sheet.

The bq2007 may be configured to have two or three charge stages. In a two-stage configuration, the fast-charge stage controlled by the bq2007 is preceded and followed by a pulse trickle charge at a rate controlled by bq2007 input pins FAST, TM, and VSEL. In a three-stage configuration, the fast charge is followed by a "top-off" charge stage where the battery is charged at $\frac{1}{8}$ of the fast charge rate. This allows the battery to be quickly and safely brought to a full charge state. Following top-off, pulse trickle is used to compensate for self-discharge while the battery is idle. The trickle rate is $\frac{1}{64}$ for PVD and $\frac{1}{32}$ when -ΔV is enabled.

Charger Circuit Examples

Two detailed applications follow this section. One provides direct control of a switch-mode regulator, and the other provides control of an external current source.

The switching-mode constant-current regulator is used on the DV2007S1 development system. The board layout and schematic is described in the layout guidelines section.

Gating Current

Figure 1 shows an example of external gated current source. With SNS connected to V_{SS}, the bq2007 enables charge current to the battery by taking MOD high at the start of charging and maintaining this state until charging is terminated. In this example, R7, R19, R15, and Q1 and Q2 form the switching circuit. When MOD goes high, Q2 switches on—turning on Q1. When MOD goes low, the base current in Q1 is turned off and the charging path is switched off.

The current-handling capability of this circuit is limited by the product of the current gains of the transistors and by the 5mA drive capability of the MOD pin.

This limitation may be removed by replacing the PNP at Q1 with a pFET. See Table 1 for suggested transistors.

Table 1. Suggested Transistors (Q1)

Q1	Type	Package	Maximum Current	Maximum Voltage
IRFR9010	pFET	DPAK	5.3	-50
IRFR9022	pFET	DPAK	9.0	-50
IRFR9020	pFET	DPAK	9.9	-50
IRFD9014	pFET	HEXDIP	1.1	-60
IRFD9024	pFET	HEXDIP	1.6	-60
IRF9Z10	pFET	TO-220	4.7	-50
IRF9Z22	pFET	TO-220	8.9	-50
IRF9Z20	pFET	TO-220	9.7	-50
IRF9Z32	pFET	TO-220	15	-50
BD136	PNP	TO-225	1.5	-60
MJE171	PNP	TO-225	3.0	-60
TIP42A	PNP	TO-220	6.0	-60

Note: For very high currents, two parallel pFETs or an nFET with a high-side driver circuit may be suitable.

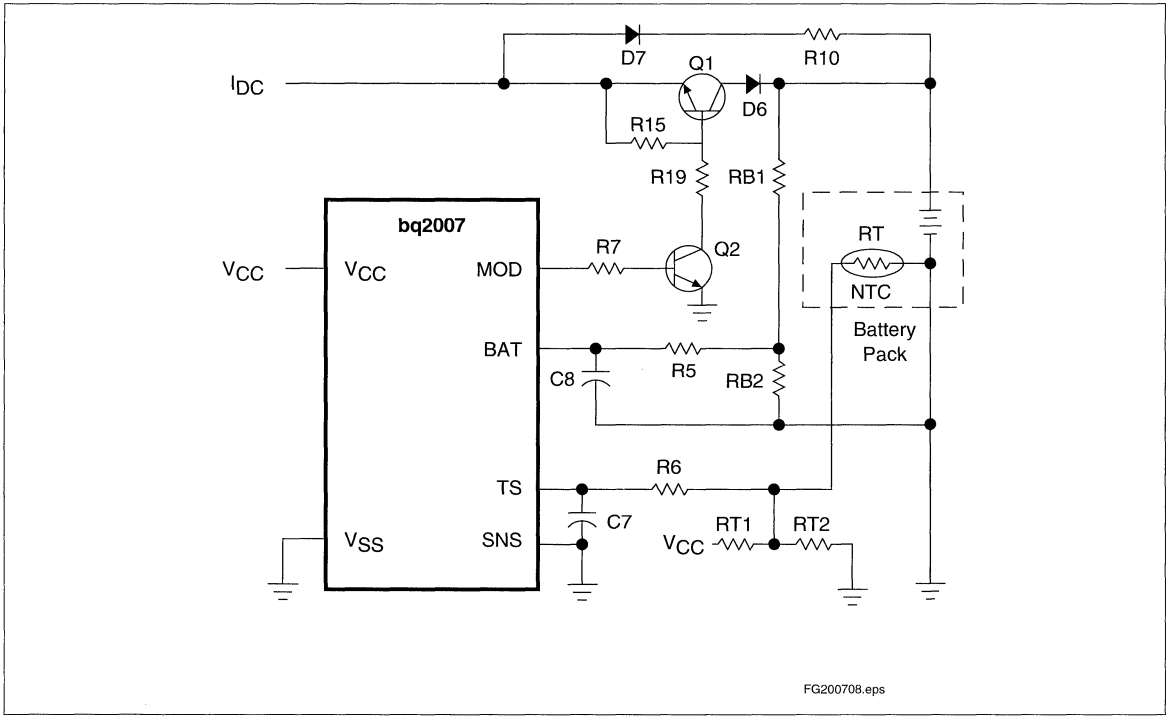


Figure 1. Gated External Source (Bipolar Switch Option)

2/14

Charge Action Control

The bq2007 charge action is controlled by input pins $\overline{DCMD}$, VSEL, FAST, and TM. When charge action is initiated, the bq2007 enters the charge-pending state, checks for acceptable battery voltage and temperature, and performs any required discharge-before-charge operations. $\overline{DCMD}$ controls the discharge-before-charge function, and VSEL, FAST, and TM select the charger configuration. See Tables 4 and 5 of the bq2007 data sheet.

Charge Status Indication

Table 2 summarizes the bq2007 charge status display. The charge status indicators include the DIS output, which can be used to indicate the discharge state, the audio ALARM output, which indicates charge completion and fault conditions, and the dedicated status outputs, LED_1 and LED_2.

Outputs LED_{1-2} have three display modes that are selected at initialization by the input pins $DSEL_1$ and $DSEL_2$. The $DSEL_1$ and $DSEL_2$ input pins, when pulled down to V_{SS}, are intended for implementation of a simple two-LED system, where LED_2 indicates the precharge status (i.e., charge pending and discharge) and LED_1 indicates the charge status (i.e., charging and completion). $DSEL_1$ pulled up to V_{CC} and $DSEL_2$ pulled down to V_{SS} mode is for implementation of a single tri-color LED such that discharge, charging, and completion each have a unique color. $DSEL_1$ pulled down to V_{SS} and $DSEL_2$ pulled up to V_{CC} mode allows for fault status information.

Audio Alarm Selection

The alarm output waveform is a 3.5KHz square wave signal that allows a direct connection to drive standard piezoelectric alarm elements. Piezoelectric alarm elements are designed for a maximum sound output at a specific frequency and drive voltage. The alarm element must be selected for a maximum sound output at a frequency of 3.5kHz with a 5V peak-to-peak drive signal. The PCB mount element can be connected directly to the bq2007 alarm output with a 20K isolation resistor. The design of a molded resonant cavity should follow the manufacturers recommended procedures to assure maximum sound output. Manufactures also provide several boost circuits that can be used to increase the drive voltage for increased sound output levels.

Table 2. bq2007 Charge Status Display Summary

Mode	Charge Action State	LED_1	LED_2	DIS	ALARM
$DSEL_1$ = L $DSEL_2$ = L (Mode 1)	Battery absent	0	0	0	0
	Charge pending (temp. limit, low voltage)	0	Flashing	0	0
	Discharge in progress	0	1	1	0
	Charging	Flashing	0	0	0
	Charge complete	1	0	0	High tone
	Fault (low-voltage time-out)	0	0	0	High tone
$DSEL_1$ = H $DSEL_2$ = L (Mode 2)	Battery absent	0	0	0	0
	Discharge in progress, pending	1	1	1	0
	Charging	1	0	0	0
	Charge complete	0	1	0	High tone
	Fault (low-voltage time-out)	0	0	0	High tone
$DSEL_1$ = L $DSEL_2$ = H (Mode 3)	Battery absent	0	0	0	0
	Charge pending (temp. limit, low voltage)	0	Flashing	0	0
	Discharge in progress	0	Flashing	1	0
	Charging	Flashing	0	0	0
	Charge complete	1	0	0	High tone
	Fault (low-voltage time-out)	0	1	0	High tone

Note: 1 = on; 0 = off; L = pulled down to V_{SS}; H = pulled up to V_{CC}.

Selecting the BAT Divider for Charge Monitoring

The voltage based state of charge monitoring is enabled when charging packs with a fixed number of cells by pulling the multi-cell pack select input MULTI to V_{SS}. When MULT = 0, internal voltage thresholds are compared with the BAT pin input voltage for both charge and discharge capacity status indications. When discharge-before-charge is initiated, the state-of-charge monitor indicates the discharge condition as monotonic decreasing steps from the charged condition. The voltage charge status monitoring circuit is shown in Fig. 2. The circuit changes its voltage threshold reference divider for charge or discharge monitoring when the discharge signal is zero or one, respectively. The voltage thresholds are a fixed ratio of the V_{CC} supply voltage and are specified in the bq2007 data sheet in the section entitled "DC Thresholds." The voltage thresholds were selected based on typical NiCad and NiMH battery characteristics for a typical charge rate of 1C and a typical discharge rate of 1 Amp.

To optimize the charge status monitoring for a range of fixed-cell packs (i.e. MULTI = 1), the BAT divider should be calculated such that the highest fixed cell pack will be centered at the EDV threshold. For example, to charge packs that range from 4 to 6 fixed cells, select the BAT divider MULTI = 0. The BAT divider should be determined by BAT divider equation 2 for values shown in Table 4. To further optimize, you can fit the battery characteristics to the end points of the EDV and MCV thresholds. This will center the battery voltage charge characteristics in the center of the bq2007 charge monitoring thresholds. This is possible since the full charge detection methods (PVD, -DV) are not dependent on absolute voltage value. When adjusting the battery divider, the maximum cutoff voltage (V_{MCV}) must not be exceeded.

Charge Status Monitoring

The bq2007 charge status monitor may display the battery voltage or charge safety timer as a percentage of the full-charged condition. These options are selected with the MULT input pin.

When MULT is pulled down to V_{SS}, the battery charge status is displayed as a percentage of the battery voltage, and the single-cell battery voltage at the BAT pin is compared with internal charge voltage reference thresholds. When V_{BAT} is greater than the internal thresholds of V_{20}, V_{40}, V_{60}, or V_{80}, the respective 20%, 40%, 60%, or 80% display outputs are activated. The battery voltage directly indicates 20% charge increments, while the 10% charge

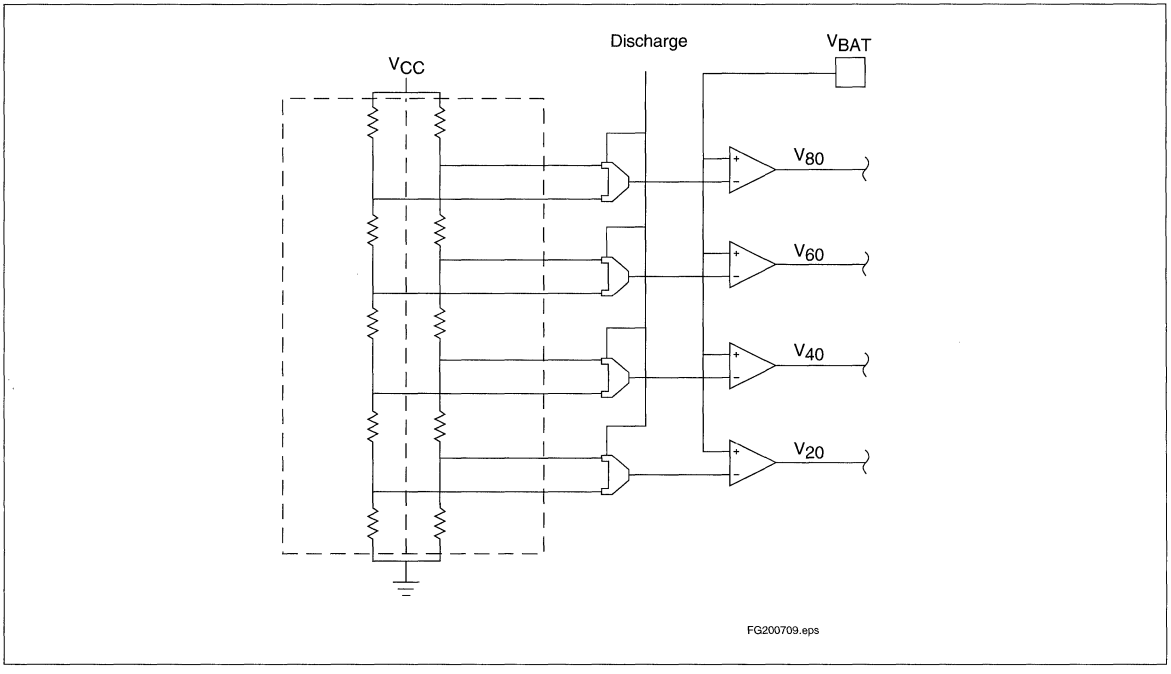


Figure 2. Voltage Charge Status Monitoring Circuit

increments use a timer that is a function of the charge safety timer.

When MULT is pulled down to V_{SS} and when V_{BAT} exceeds V_{20} during charging, the 20% charge indication is activated and the timer begins counting for a period equal to $\frac{1}{64}$ to $\frac{1}{32}$ of the charge safety time-out period. When the timer count is completed, the 30% charge indication is activated. Should V_{BAT} exceed V_{40} prior to the timer count completion, the charge status monitor activates the 30% and 40% indications. This technique is used for all the odd percentage charge indications to assure a monotonic charge status display.

When MULT is pulled up to V_{CC}, the bq2007 charge status monitor directly displays $\frac{1}{32}$ of the charge safety timer as a percentage of full charge. This method is recommended over the voltage-based method when charging multi-cell packs where the battery terminal voltages can vary greatly between packs. This method offers an accurate charge status indication when the battery is fully discharged.

During discharge with MULT pulled down to V_{SS}, the charge status monitor indicates the percentage of the battery voltage by comparing V_{BAT} to the internal discharge voltage reference thresholds. In BCD format, the discharge thresholds V80, V60, V40, and V20 correspond to a battery charge state indication of 90%, 70%, 50%, and 30%, respectively. In bargraph format, the same discharge thresholds correspond to a battery charge state indication of 90%, 60%, 40%, and 30%, respectively. Differences in the battery charge state indications are due to the finer granularity of the BCD versus the bargraph format.

During discharge and when MULT is pulled up to V_{CC}, the state-of-charge monitor segment format displays the discharge condition, letter "d," whereas the bargraph format has no indication.

The charge status display is blanked during the charge pending state and when the battery pack is removed.

Charge Status Display Modes

The bq2007 charge status monitor can be displayed in two modes summarized in Table 3. The display modes are a seven-segment monotonic bargraph or a seven-segment single-digit format. When QDSEL is pulled down to V_{SS}, pins SEG_{A-G} drive the decoded seven segments of a single segment digit display, and when QDSEL is pulled up to V_{CC}, pins SEG_{A-G} drive the seven segments of a bargraph display.

In the bargraph display mode, outputs SEG_{A-G} allow options for a three-segment to seven-segment bargraph display. The three-segment charge status display uses outputs SEG_B, SEG_D, and SEG_F for 30%, 60%, and 90% charge indications, respectively. The four-segment charge status display uses outputs SEG_A, SEG_C, SEG_D, and SEG_E for 20%, 40%, 60%, and 80% indications, respectively. The seven-segment charge status monitor uses all segments.

The segment display mode drives pins SEG_{A-G} with the decoded seven-segment single-digit information. The display indicates in 10% increments from a segment zero count at charge initiation to a segment nine count indicating 90% charge capacity. Charge completion is indicated by the letter "F," a fault condition by the letter "E," and the discharge condition by the letter "d." See Table 3.

Display Driver Modes

The bq2007 is designed to interface with LCD or LED type displays. The LED signal levels are driven when the MSEL input is pulled to V_{CC} at initialization. The output pin COM is the common anode connection for LED SEG_{A-G}.

The LCD interface mode is enabled when the MSEL input pin is pulled to V_{SS} at initialization. An internal oscillator generates all the timing signals required for the LCD interface. The output pin COM is the common connection for static direct-driving of the LCD display backplate and is driven with an AC signal at the frame period. When enabled, each of the SEG_{A-G} pins is driven with the correct-phase AC signal to activate the LCD segment. In segment mode, output pins SEG_{A-G} interface to LED or LCD segments.

Discharge Before Charge

It may be desirable in the application to allow the user to occasionally discharge the battery to a known voltage level prior to charge. The reason for this may either be to remedy a voltage-depression effect found in some NiCd batteries or to determine the battery's charge capacity.

Figure 3 illustrates the implementation of this function. Discharge-before-charge is initiated on a positive strobe signal on DCMD.

Note: This function takes precedence over a charge action and commences immediately when conditions warrant, forcing DIS to a high state until the voltage sensed on BAT falls below $V_{CC}/5$. Charging begins as soon as conditions allow.

Care should be taken not to overheat the battery during this process; excessive temperature is not a condition that terminates discharge.

Configuring the BAT Input

The bq2007 uses the battery voltage sense input on the BAT pin to control discharge-before-charge, qualify charge initiation, terminate charge at an absolute limit, facilitate peak voltage detect (PVD) and negative delta voltage (-ΔV) detection, and detect a battery replacement.

V_{BAT} may be derived from a simple resistive network across the battery. As shown in Figure 1, resistors RB1 and RB2 are chosen to divide the battery voltage down to the optimal detection range. When MULT is pulled up to V_{CC}, battery voltage is sensed at the BAT pin by a resistive voltage divider that divides the terminal voltage between 0.262 * V_{CC} (V_{EDV}) and 0.8 * V_{CC} (V_{MCV}). The bq2007 charges multi-cell battery packs from a minimum of N cells, to a maximum of 1.5 * N cells. The battery voltage divider is set to the minimum cell battery pack (N) by the BAT pin voltage divider ratio equation:

$$\frac{R1}{R2} = \left(\frac{N}{1.33}\right) - 1 \qquad \text{Equation 1}$$

When MULT is pulled down to V_{SS}, tighter charge voltage limits and voltage-based charge status display are selected. This is recommended for charging packs with a fixed number of cells where the battery voltage divider range is between 0.4 * V_{CC} (V_{EDV}) and 0.8 * V_{CC} (V_{MCV}). The bq2007 charges fixed-cell battery packs of N cells. The battery voltage divider is set by the divider ratio equation:

$$\frac{R1}{R2} = \left(\frac{N}{2}\right) - 1 \qquad \text{Equation 2}$$

Although virtually any value may be chosen for RB1 and RB2 due to the high input impedance of the BAT pin, the values selected must not be so low as to appreciably drain the battery nor so large as to degrade the circuit's noise performance. Constraining the source resistance as seen from BAT between 20KΩ and 1MΩ is acceptable over the bq2007 operating range. Total impedance between the battery terminal and VSS should typically be about 300KΩ to 1MΩ . See Table 4.

Note: Because V_{SNS} may be positive in bq2007 switching regulation applications, the actual internal comparison

Table 3. bq2007 Charge Status Display Summary

Mode	Display Indication	SEG_A	SEG_B	SEG_C	SEG_D	SEG_E	SEG_F	SEG_G
QDSEL = H	20% charge	1	0	0	0	0	0	0
	30% charge	1	1	0	0	0	0	0
	40% charge	1	1	1	0	0	0	0
	60% charge	1	1	1	1	0	0	0
	80% charge	1	1	1	1	1	0	0
	90% charge	1	1	1	1	1	1	0
	Charge complete	1	1	1	1	1	1	1
QDSEL = L	0% charge—digit 0	1	1	1	1	1	1	0
	10% charge—digit 1	0	1	1	0	0	0	0
	20% charge—digit 2	1	1	0	1	1	0	1
	30% charge—digit 3	1	1	1	1	0	0	1
	40% charge—digit 4	0	1	1	0	0	1	1
	50% charge—digit 5	1	0	1	1	0	1	1
	60% charge—digit 6	1	0	1	1	1	1	1
	70% charge—digit 7	1	1	1	0	0	1	0
	80% charge—digit 8	1	1	1	1	1	1	1
	90% charge—digit 9	1	1	1	1	0	1	1
	Charge complete—letter F	1	0	0	0	1	1	1
	Fault condition—letter E	1	0	0	1	1	1	1
	Discharge—letter d	0	1	1	1	1	0	1

Note: 1 = on; 0 = off; L = pulled down to V_{SS}; H = pulled up to V_{CC}.

6/14

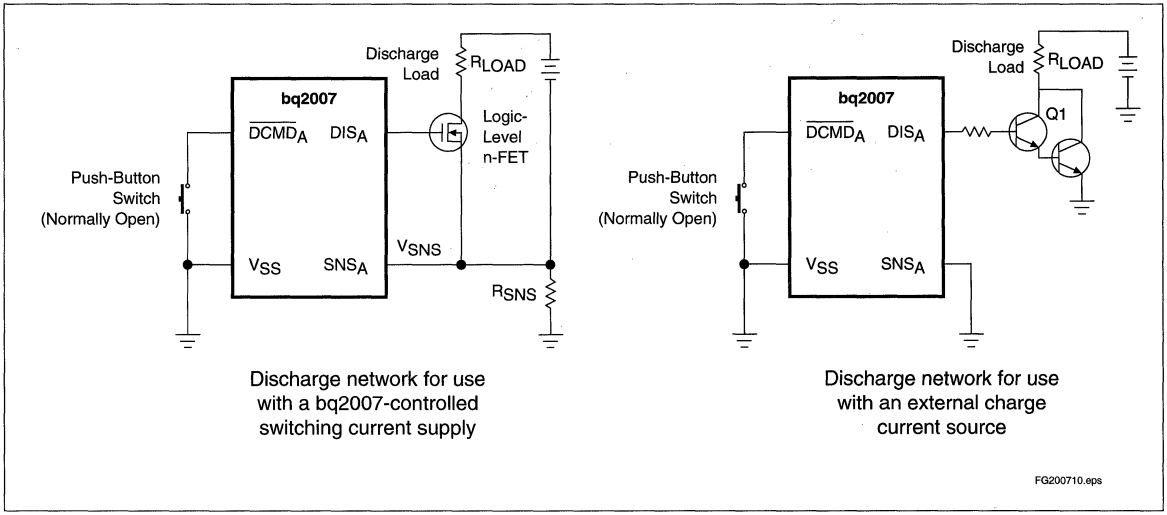


Figure 3. Battery Conditioning Network

Table 4. Suggested RB1 and RB2 Values for NiCd and NiMH Cells

Number of Cells (V_{BAT} Divisor)	RB1(KΩ)	RB2(KΩ)
4	150	165
5	150	110
6	150	80.6
8	150	53.6
10	150	40.2

Note: MULTI = 0; RB1/RB2 = (N/2) - 1.

uses $V_{BAT} - V_{SNS}$, or V_{CELL}. This internal value V_{CELL} maintains a representative voltage independent of any current through R_{SNS}.

Temperature Sensing and the TCO Pin

The bq2007 uses the temperature sense input on the TS pin to qualify charge initiation and termination. A negative temperature coefficient (NTC) thermistor referenced to SNS and placed in close proximity to the battery may be used as a temperature-to-voltage transducer as shown in Figure 1. This example shows a simple linearization network constituted by RT1 and RT2 in conjunction with the thermistor, RT.

Temperature-decision thresholds are defined as LTF (low-temperature fault) and TCO (temperature cutoff). Charge action initiation is inhibited if the temperature is not within the LTF-to-TCO range. In this case, the charge pending state is active on the charge status display (see Table 2), and charging does not initiate until the battery temperature returns to this range.

Once initiated, charging terminates if the temperature is either less than LTF or greater than TCO. The bq2007 interprets the reference points V_{LTF} and V_{TCO} as V_{SS}-referenced voltages, with V_{LTF} fixed at ½ V_{CC} and V_{TCO} equal to the voltage presented on the TCO pin. See Figure 4. Note that since the voltage on pin TS decreases as temperature increases, V_{TCO} should always be less than ½ V_{CC}. The resistive dividers may be used to generate the desired V_{TCO}.

Vcc Supply

The V_{CC} supply provides both power and voltage reference to the bq2007. This reference directly affects BAT voltage and internal time-base voltage measurements.

The time-base is trimmed during manufacturing to within 5 percent of the typical value with V_{CC} = 5V. The oscillator varies directly with V_{CC}. If, for example, a 5% regulator supplies V_{CC}, the time-base could be in error by as much as 10%.

Charge State Actions

Once the required discharge is completed and temperature and voltage prequalifications are met, the charge state is initiated. The charge state is configured by the VSEL, FAST, and TM input pins. The FAST input selects between Fast and Standard charge rates. The Standard

Table 5. bq2007 Charge Action Control Summary

FAST Input State	TM Input State	Time-out Period (min)	MOD Duty Cycle	Hold-off period (sec)	Trickle Rep Rate -ΔV $^{C}/_{32}$	Trickle Rep Rate PVD $^{C}/_{64}$
V_{SS}	Float	640 ($^{C}/_{8}$)	25%	2400	219Hz	109Hz
V_{SS}	V_{SS}	320 ($^{C}/_{4}$)	25%	1200	109Hz	55Hz
V_{SS}	V_{CC}	160 ($^{C}/_{2}$)	25%	600	55Hz	27Hz
V_{CC}	Float	160 ($^{C}/_{2}$)	100%	600	219Hz	109Hz
V_{CC}	V_{SS}	80 (C)	100%	300	109Hz	55Hz
V_{CC}	V_{CC}	40 (2C)	100%	150	55Hz	27Hz

charge rate is $^{1}/_{4}$ of the Fast charge rate, which is accomplished by disabling the regulator for a period of 286µs of every 1144µs (25% duty cycle). In addition to throttling back the charge current, time-out and hold-off safety time are increased accordingly.

The VSEL input selects the voltage termination method. The termination mode sets the top-off state and trickle charge current rates. The TM input selects the Fast charge rate, the Standard rate, and the corresponding charge times. Once charging begins at the Fast or Standard rate, it continues until terminated by any of the following conditions:

- Negative delta voltage (-ΔV)
- Peak voltage detect (PVD)
- Maximum temperature cutoff (TCO)
- Maximum time-out (MTO)
- Maximum cutoff voltage (MCV)

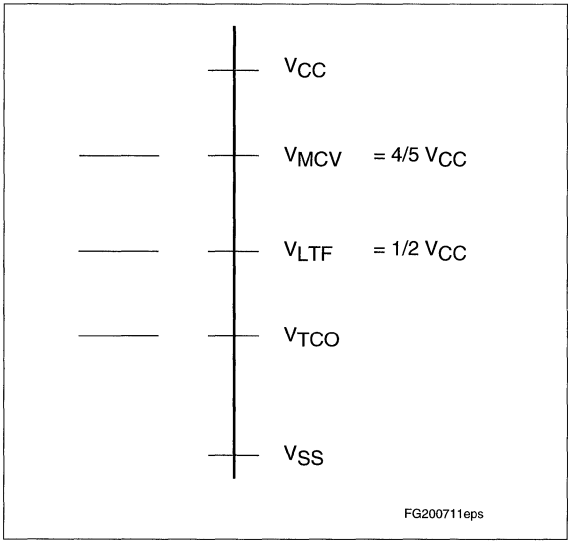


Figure 4. Temperature Reference Points

Voltage Termination Hold-off

To prevent early termination due to an initial false peak battery voltage, the -ΔV and PVD terminations are disabled during a short "hold-off" period at the start of charge. During the hold-off period when fast charge is selected (FAST = 1), the bq2007 will top off charge to prevent excessive overcharging of a fully charged battery. Once past the initial charge hold-off time, the termination is enabled. TCO and MCV terminations are not affected by the hold-off time.

-ΔV or PVD Termination

Table 6 summarizes the two modes for full-charge voltage termination detection. When VSEL = V_{SS}, negative delta voltage detection occurs when the voltage seen on the BAT pin falls 12mV (typical) below the maximum sampled value. VSEL = V_{CC} selects peak voltage detect termination and the top-off charge state. When charging a battery pack with a fixed number of cells, the -ΔV and PVD termination thresholds are -6mV and 0 to -3mV per cell, respectively. The valid battery voltage range on V_{BAT} for -ΔV or PVD termination is from 0.262 * V_{CC} to 0.8 * V_{CC}.

Top-Off Charge

The top-off charge option allows for the self-discharge replacement trickle current to be very low, but still provides for filling up the last fraction of capacity after the fast-charge phase has terminated. Top-off occurs at 1/8 of the fast charge rate to prevent excess heat generation, and terminates after a period equal to the safety time-out. It also terminates if TCO or MCV is detected.

Top-off is not recommended in applications where a battery charge is re-initiated with extremely high frequency (many times per day); for example, when the unit is returned to the charge cradle after each short period of use.

Pulse trickle is used to compensate for self-discharge while the battery is idle and to condition a depleted low-voltage battery to a valid voltage prior to high-current charging. The battery is pulse trickle charged when Fast, Standard, or top-off charge is not active. This results in a trickle rate of $C/64$ for PVD and $C/32$ when -ΔV is enabled.

Table 6. VSEL Configuration

VSEL	Detection Method	Top-Off	Pulse Trickle Rate
V_{SS}	-ΔV	Disabled	$C/32$
V_{CC}	PVD	Enabled	$C/64$

Charge Inhibit

Fast charge, top-off, and pulse trickle may be inhibited by using the $\overline{INH}$ input pin. When low, the bq2007 suspends all charge activity, drives all outputs to high impedance, and assumes a low-power operational state. When $\overline{INH}$ returns high, a fast-charge cycle is qualified and begins as soon as conditions allow.

Power Supply Selection

The DC supply voltage, V_{DC}, must satisfy two requirements:

1. To support the bq2007 V_{CC} supply, V_{DC} must be adequate to provide for 5V regulation after the losses in the regulator and across D1 ($V_{DC} \geq 7.7V$ using the 78L05).
2. To support the charge operation, V_{DC} > (number of cells * MCV_{MAX}) + V_{LOSS} in the charging path. (MCV_{MAX} is the maximum cell voltage threshold with the maximum bq2007 V_{CC}.)

Polarity Reversal Protection

If the DC input has any risk of being accidentally connected with power (+) and ground (–) reversed, then the system input should include either a protection diode to protect against circuit damage or a diode bridge to provide both protection and operation. This also increases minimum input voltage for charger operation by approximately 1V to 2V.

Layout Guidelines

PCB layout to minimize the impact of system noise on the bq2007 is important when the bq2007 is used as a switching modulator, with a separate nearby switching regulator, or close to any other significant noise source.

1. Avoid mixing signal and power grounds by using a single-point ground technique incorporating both a small signal ground path and a power ground path.
2. The charging path components and associated traces should be kept relatively isolated from the bq2007 and its supporting components.
3. 0.1µF and 10µF decoupling capacitors should be placed close together and very close to the V_{CC} pin.
4. 0.1µF capacitors and resistors forming R-C filters connected to pins BAT, TS, TCO, and MCV should be as close as possible to their associated pins.
5. Because the bq2007 uses V_{CC} for its reference, additional loading on V_{CC} is not recommended.
6. Diode D1 (1N4148) is recommended for rectification and filtering.
7. If the DCMD input is electronically controlled, care should be taken to prevent noise-induced false transitions.
8. For bq2007-modulated switching applications:
   - A 2KΩ resistor is required between the MOD pin and the transistor.
   - A 1000pF capacitor/1KΩ resistor R-C filter should be as close as possible to the SNS pin.
   - The 0.1µF capacitors for BAT and TS should be routed directly to SNS and not to ground.

Figures 6, 7, and 8 show an example layout of the DV2007S1 Development Board. Figure 9 is a schematic of the board. Table 7 contains the parts list for the board. A comparable layout is recommended.

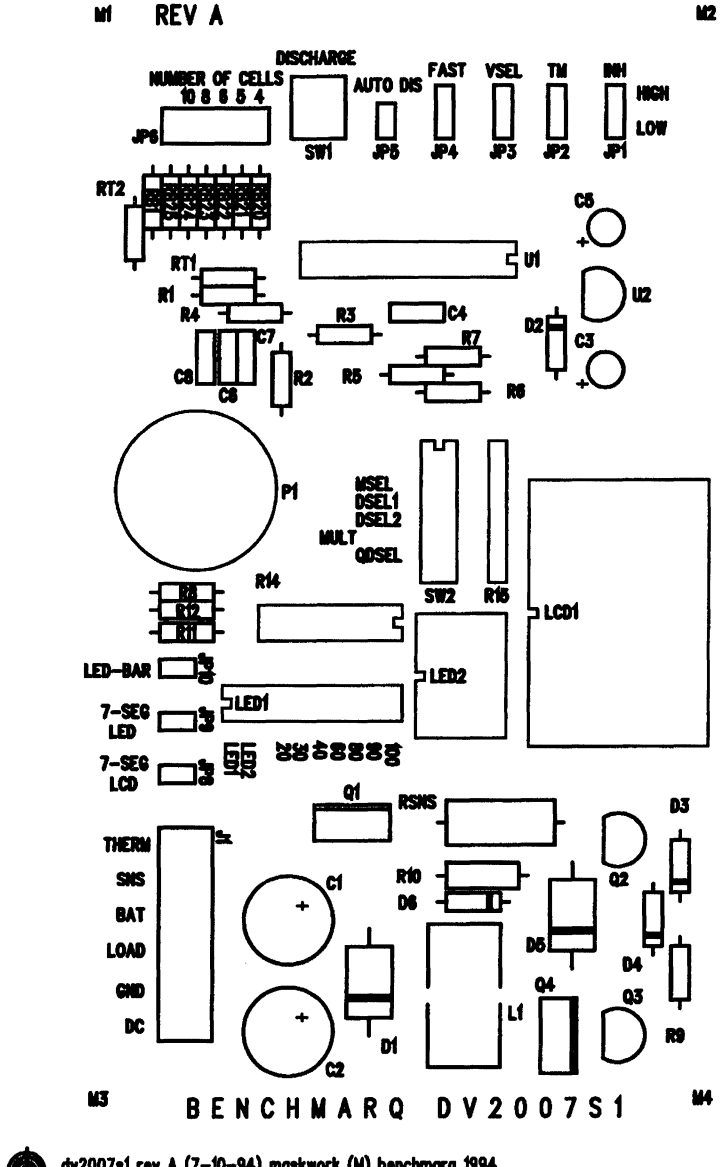


Figure 6. DV2007S1 Development Board Layout Component Placement

10/14

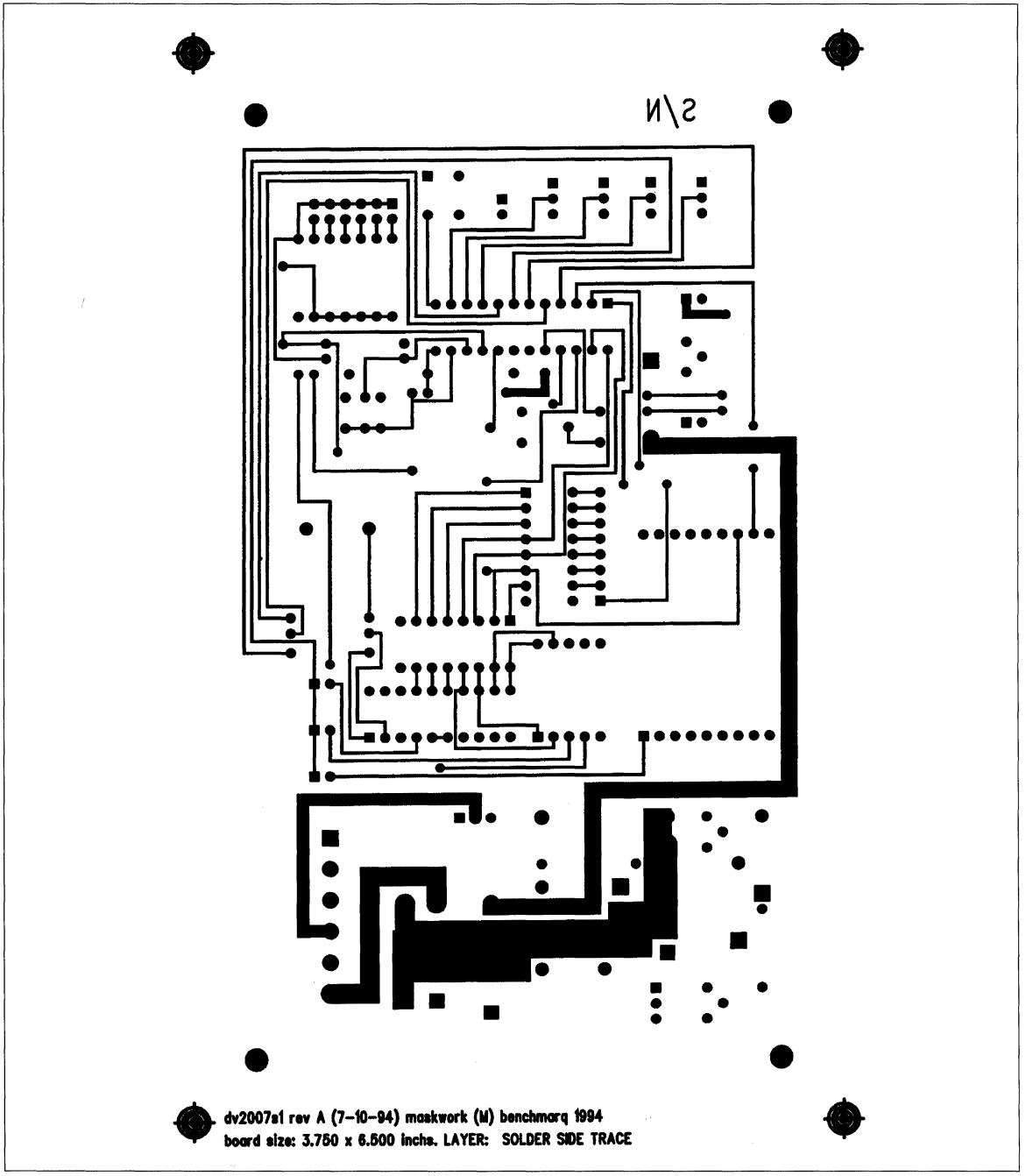


Figure 7. DV2007S1 Development Board Layout

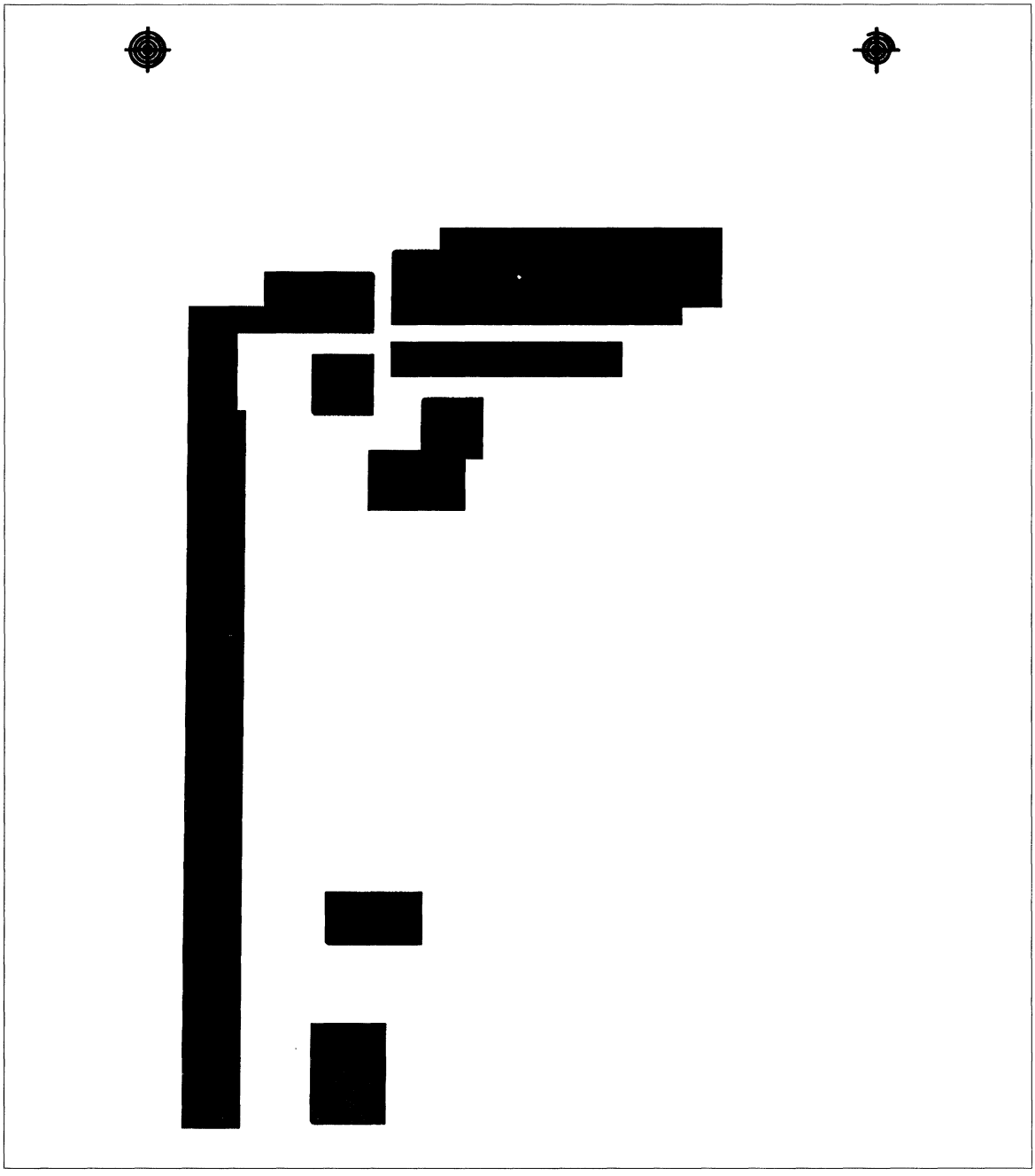


Figure 8. DV2007S1 Development Board Layout

12/14

Table 7. DV2007S1 Development Board Parts List

Component Name	Component Description
C2, C1– Optional	1000µF
C5, C3	100µF
C4, C6, C7	0.1µF
C8	1nF
D1	1N5400
D4, D2	1N4148
D3	1N751A
D5	1N5821
D6	1N4001
JP1, JP2, JP3, JP4	HEADER 3
JP5, JP8, JP9, JP10	HEADER 2
J1	CON6
LCD1	7-SEG LED
LED1	LED BAR
LED2	7-SEG LCD
L1	100µH
P1	BUZZER
Q1	MTP3055EL
Q2	2N7000
Q3	2N3904
Q4	MTP23P06E
R14	Resistor 8pack
RB1	150K
RB2X	User Selected
RSNS	0.2
RT1	20K
RT2	Open
R1	300K
R6, R7	100K
R2, R5, R10	2K
R3	82K
R4	20K
R8	20K
R9	6.8K
R12, R11	510
SR	SIP8
SW1	SW pushbutton
SW2	SW DIP-8
U1	bq2007
U2	78L05

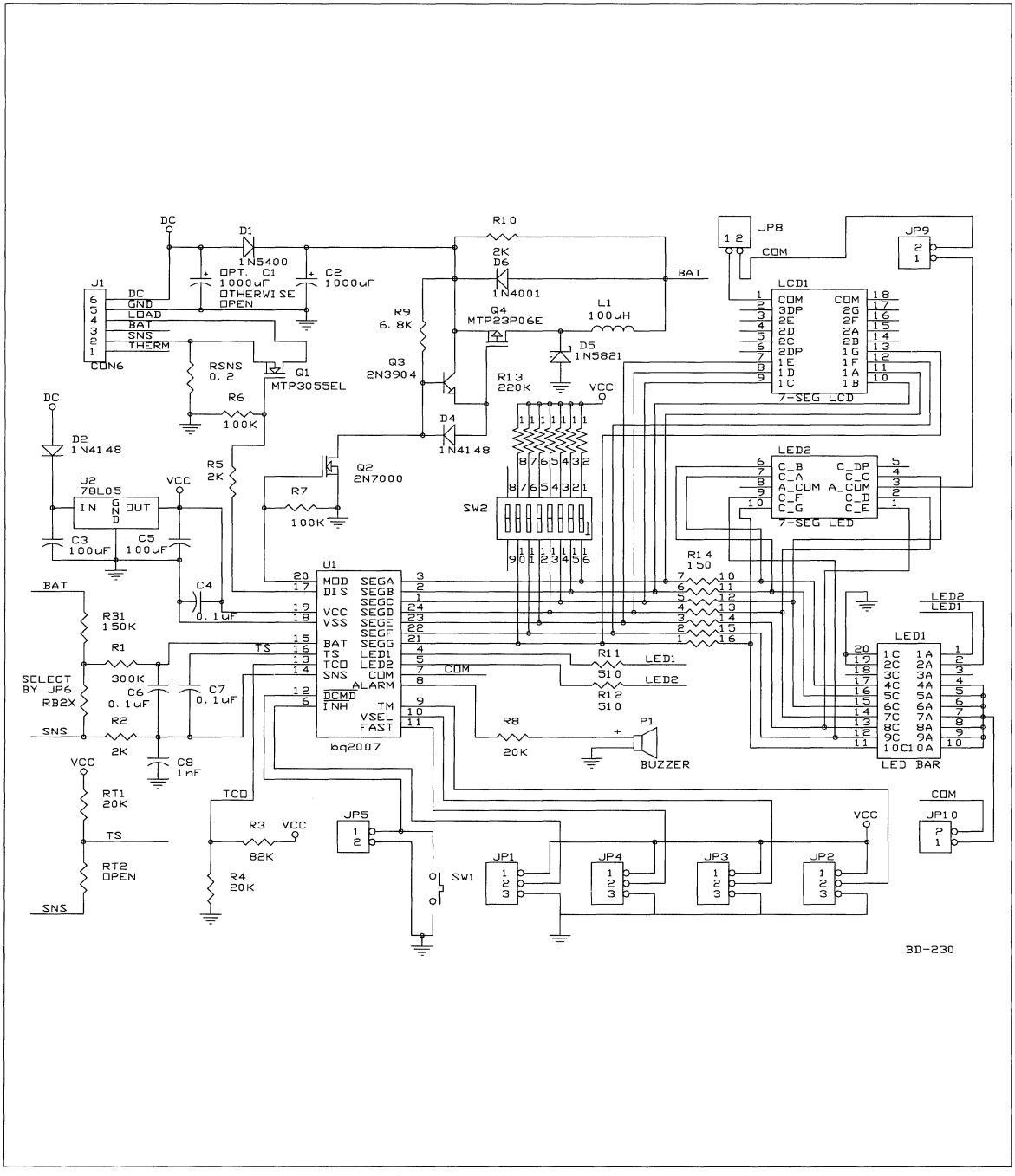


Figure 9. DV2007S1 Development Board Schematic

U-510 Using the bq2031 to Charge Lead-Acid Batteries

Description of Operation

The bq2031 has two primary functions: lead-acid battery charge control and switch-mode power conversion control. Figure 1 is a block diagram of the bq2031. The charge control circuitry is capable of a variety of full-charge detection techniques and supports three different charging algorithms. The Pulse-Width Modulator (PWM) provides control for high-efficiency current and voltage regulation.

Starting a Charge Cycle and Battery Qualification

When V_{CC} becomes valid (rises past its minimum value), the first activates battery temperature monitoring. Temperature is indicated by the voltage between the pins TS and SNS (V_{TEMP}). If the bq2031 finds the temperature out of range (or the thermistor is absent), it enters the Charge Pending State. In this state, all timers are suspended, charging current is kept off by MOD being held low, and the state is annunciated by LED_3 alternating high and low at approximately $\frac{1}{6}$th second intervals.

Temperature checks remain active throughout the charge cycle. They are masked only when the bq2031 is in the Fault state (see below). When the temperature returns to the allowed charging range, timers are restarted (not reset) and the bq2031 returns to the state it was in when the temperature fault occurred.

When the thermistor is present and the temperature is within the allowed range, the bq2031 then checks for the presence of a battery. If the voltage between the BAT and SNS pins (V_{CELL}) is between the Low-Voltage Cut-Off threshold (V_{LCO}) and the High-Voltage Cut-Off (V_{HCO}), the bq2031 perceives a battery to be present and begins pre-charge battery qualification after a 500ms (typical) delay. If any new temperature or voltage faults occur during this time, the bq2031 immediately transitions to the appropriate state.

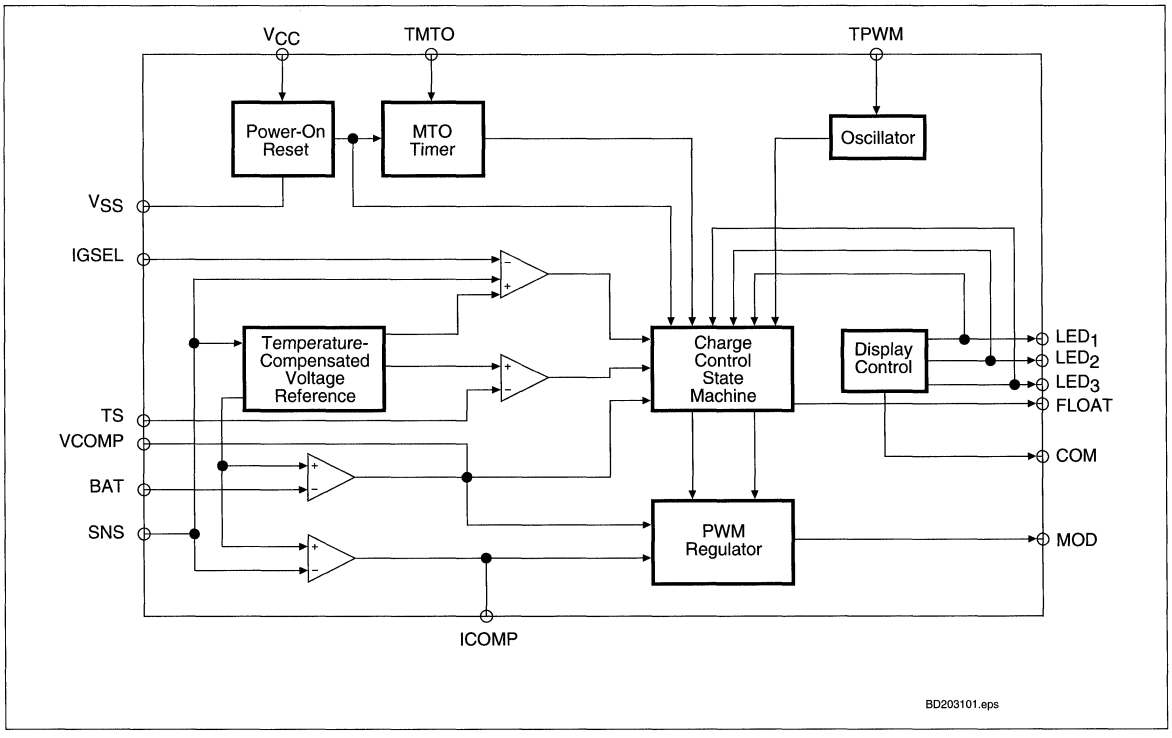


Figure 1. Block Diagram of the bq2031

If V_{CELL} is less than V_{LCO} or above V_{HCO}, the bq2031 believes no battery is present and enters the Fault state; MOD is held low and LED_3 is turned on. This light gives the customer an indication that the charger is on, even though no battery is present. The bq2031 leaves the Fault state only if it sees V_{BAT} rise past V_{LCO} or fall past V_{HCO}, indicating a new battery insertion. If temperature is within bounds, there will again be a 500ms delay before battery qualification tests start.

Battery Qualification Tests

In test 1, the bq2031 attempts to regulate a voltage = V_{FLT} + 0.25V across the battery pack. The bq2031 monitors the time required for ISNS, the charging current, to rise to $I_{COND} = I_{MAX}/5$. If the current fails to rise to this level before the time-out period t_{QT1} expires (e.g., the battery has failed open), the bq2031 enters the Fault state, indicated by the LED_3 pin going high. Charging current is removed from the battery by driving the MOD pin low, and the bq2031 remains in this state until it detects the conditions to start a new charge cycle; the battery is replaced or V_{CC} is cycled off and then back on.

If test 1 passes, the bq2031 starts test 2 by attempting to regulate a charging current of I_{COND} into the battery pack. It monitors the time required for the pack voltage to rise above V_{MIN} (the voltage may already be over this limit). If the voltage fails to rise to this level before the time out period t_{QT2} expires (e.g., the battery has failed short), the bq2031 again enters the Fault state as described above. If test 2 passes, the bq2031 then begins fast (bulk) charging.

Fast Charging

The user configures the bq2031 for one of three fast charge and maintenance algorithms.

Two-Step Voltage (Figure 3)

This algorithm consists of three phases:

- Fast-Charge phase 1: The charging current is limited at I_{MAX} until the cell voltage rises to V_{BLK}.
- Fast-Charge phase 2: The charging voltage is regulated at V_{BLK} until the charging current drops below I_{MIN}.
- Maintenance phase: The charging voltage is regulated at V_{FLT}.

Two-Step Current (Figure 4)

This algorithm consists of two phases:

- Fast-Charge phase: The charging current is regulated at I_{MAX} until the cell voltage rises to V_{BLK} **or** the "Second Difference" of cell voltage drops below -8mV while V_{BAT} is over 2.0V. Second Difference is the accumulated differences between successive samples of V_{BAT}. The Second Difference technique looks for a negative change in battery voltage as the battery begins overcharging (see Figure 6).
- Maintenance phase: Fixed-width pulses of charging current = I_{COND} are modulated in frequency to achieve an average value of I_{MIN}. See Appendix A for implementation details.

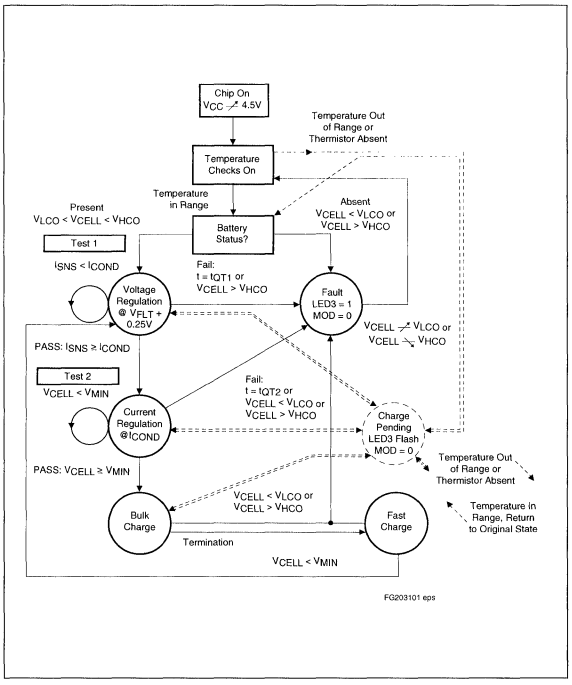


Figure 2. Cycle Start/Battery Qualification State Diagram

Pulsed Current (Figure 5)

This algorithm consists of two phases:

- Fast-Charge phase: The charging current is regulated at I_{MAX} until the cell voltage rises to V_{BLK}.
- Maintenance phase: Charging current is removed until the battery voltage falls to V_{FLT}; charging current is then restored and regulated at I_{MAX} until the battery voltage once again rises to V_{BLK}. This cycle is repeated indefinitely.

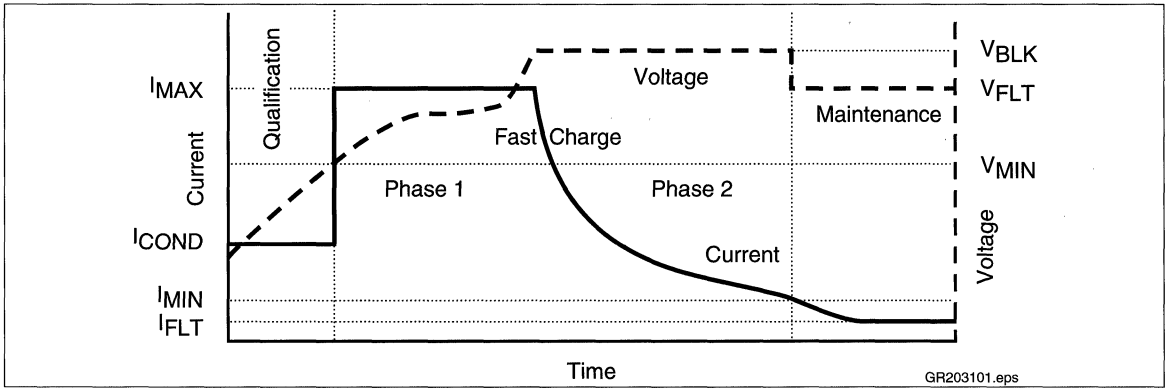


Figure 3. Two-Step Voltage Algorithm

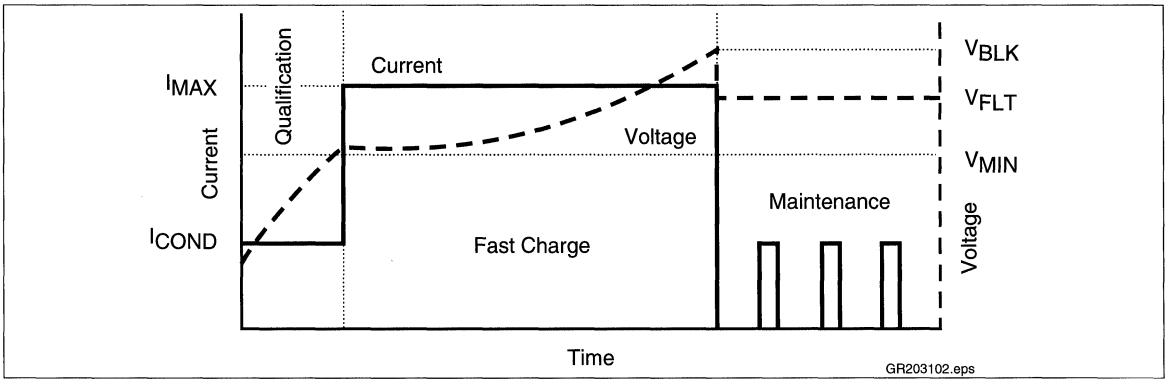


Figure 4. Two-Step Current Algorithm

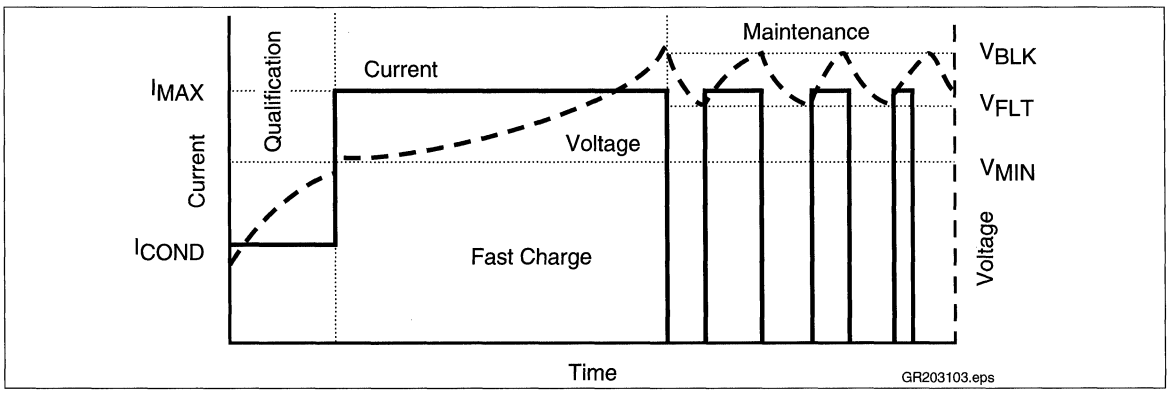


Figure 5. Pulsed Current Algorithm

Safety Time-Out

A safety timer limits the time the charger can spend in any phase of the charging cycle except maintenance. This Maximum Time-Out (MTO) timer is reset at the end of successful pre-charge qualification when the bq2031 begins fast charging1. If MTO times out before a fast charge termination criterion is met, the charging current is turned off (MOD driven low) and the bq2031 enters the Fault state exactly as if it had failed a pre-charge qualification test.

There is one exception. In the Two-Step Voltage algorithm, MTO is reset when the bq2031 transitions from the current-limited phase 1 to the voltage-regulated phase 2 of fast charging. If MTO expires while the bq2031 is still in phase 1, it does not enter the Fault state but instead transitions to maintenance phase.

During maintenance, the MTO timer is reset at the beginning of each new pulse in the Two-Step Current and Pulsed Current algorithms. It expires (and puts the bq2031 in the Fault state) only when the bq2031 beccomes "jammed" with a pulse stuck "on." The MTO timer is not active during the maintenance phase of the Two-Step Voltage algorithm.

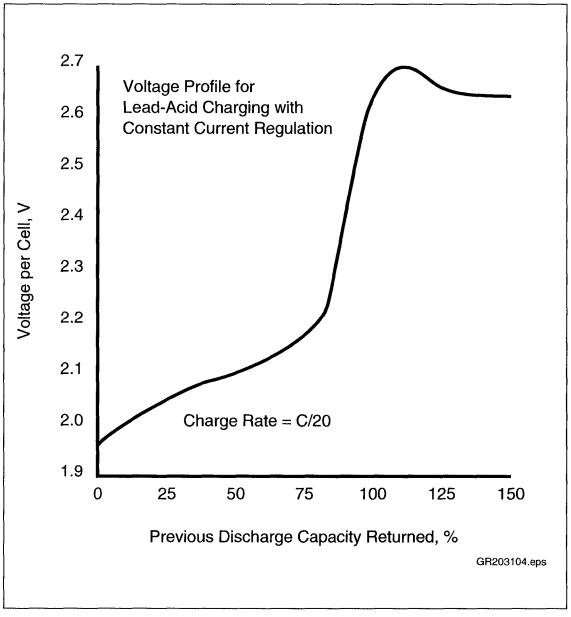


Figure 6. Voltage Roll-Off in Constant-Current Charging Profile

Hold-off Periods

Old age and/or abuse can create conditions in lead-acid batteries that may generate a large transient voltage spike when current-regulated charging is first applied. This spike could cause early termination in the fast charge algorithms by mimicking their voltage-based termination criteria. To prevent this, the bq2031 uses a "hold-off" period at the beginning of the fast charge phase. During this time, all voltage criteria are ignored except cutoff voltages. (Straying outside the range between V_{HCO} and V_{LCO} still causes the bq2031 to believe the battery has been removed, and the bq2031 enters the Fault state and shuts off charging current.) A hold-off period is also enforced during test 2 of pre-charge qualification for the same reason.

Configuration Instructions

Selecting Charge Algorithm and Display Mode

$QSEL/LED_3$, $DSEL/LED_2$, and $TSEL/LED_1$ are bi-directional pins with two functions: they are LED driver pins as outputs and programming pins for the bq2031 as inputs. The selection of pull-up, pull-down, or no pull resistor for these pins programs the charging algorithm on QSEL and TSEL per Table 1 and the display mode on DSEL per Table 2. The bq2031 forces the output driver on these bi-directional pins to their high-impedance state (as well as their common return output pin, COM) and latches the programming data sensed on the inputs when any one of the following three events occurs:

1. V_{CC} rises to a valid level.
2. The bq2031 leaves the Fault state.
3. The bq2031 detects battery insertion.

The LEDs go blank for approximately 0.75s. (typical) while new programming data is latched.

Figure 7 shows the bq2031 configured for the Two-Step Current algorithm and display mode 2.

Table 1. Programming Charge Algorithms

Charge Algorithms	QSEL	TSEL	Programmable Thresholds
Two-Step Voltage	L	H/L*	I_{MAX}, V_{BLK}, V_{FLT}
Two-Step Current	H	L	I_{MAX}, V_{BLK}, I_{MIN}
Pulsed Current	H	H	I_{MAX}, V_{BLK}, V_{FLT}

Note: * Set either high or low; do not float pin.

1 The MTO timer also resets at the beginning of the pre-charge qualification period. However, t_{QT1} or t_{QT2} (the qualification test time limits) expire and put the bq2031 in the Fault state before the MTO limit can be reached. The MTO timer is suspended while the bq2031 is in the Fault state, and is reset by the conditions that allow the bq2031 to exit that state.

Table 2. bq2031 Display Output Summary

Mode	Charge State	LED_1	LED_2	LED_3
DSEL = 0 (Mode 1)	Battery absent	Low	Low	High
	Pre-charge qualification	Flash*	Low	Low
	Fast charging	High	Low	Low
	Maintenance charging	Low	High	Low
	Charge pending (temperature out of range)	X	X	Flash*
	Fault	X	X	High
DSEL = 1 (Mode 2)	Battery absent	Low	Low	High
	Pre-charge qualification	High	High	Low
	Fast charge	Low	High	Low
	Maintenance charging	High	Low	Low
	Charge pending (temperature out of range)	X	X	Flash*
	Fault	X	X	High
DSEL = Float (Mode 3)	Pre-charge qualification	Flash*	Flash*	Low
	Battery absent	Low	Low	High
	Fast charge: current regulation	Low	High	Low
	Fast charge: voltage regulation	High	High	Low
	Maintenance charging	High	Low	Low
	Charge pending (temperature out of range)	X	X	Flash*
	Fault	X	X	High

Notes: 1 = V_{CC}, 0 = V_{SS}, X = LED state when fault occurred.
* Flash = 1/6 sec. low, 1/6 sec. high

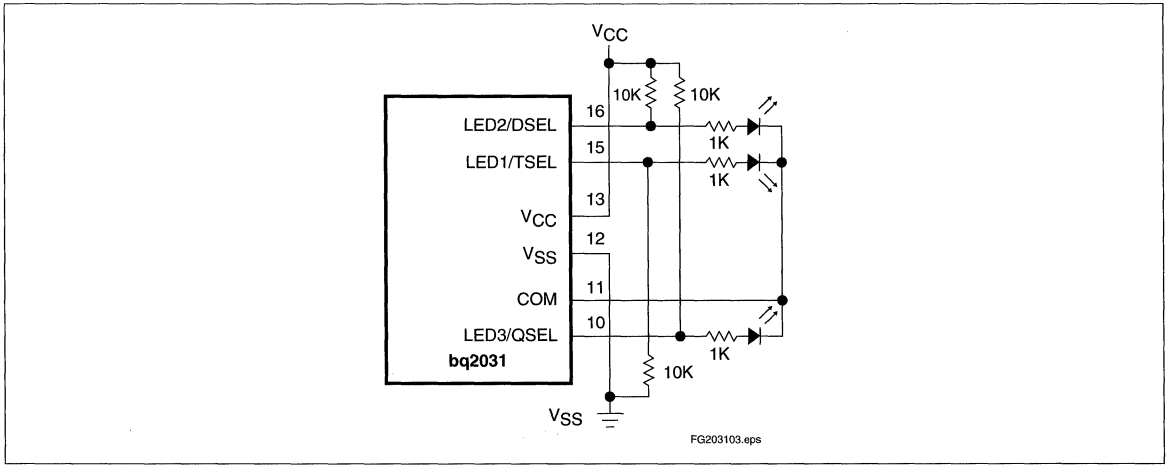


Figure 7. Configuring 10K Two-Step Current Algorithm and Display Mode Selection

Setting Voltage and Current Thresholds

Fixed Thresholds

The bq2031 uses the following fixed thresholds:

- **V_{HCO}**—High-Cutoff Voltage: V_{BAT} rising above this level is interpreted as battery removal, cutting off charging current. $V_{HCO} = 0.6 * V_{CC}$.
- **V_{LCO}**—Low-Cutoff Voltage: V_{BAT} dropping below this level is interpreted as battery removal, cutting off charging current. $V_{LCO} = 0.8V$.
- **V_{MIN}**—Minimum Voltage: Used in pre-charge qualification test 2. $V_{MIN} = 0.34 * V_{CC}$.
- **I_{COND}**—Conditioning Current: Used in the maintenance phase of the Two-Step Current algorithm and pre-charge qualification tests 1 and 2. $I_{COND} = I_{MAX}/5$. I_{MAX} is set by Equation 3.

Configurable Thresholds

The bq2031 uses the following configurable thresholds:

- **V_{BLK}**—Upper voltage limit during fast charge, typically specified by the battery manufacturers to be 2.45V–2.5V per cell @ 25°C.
- **V_{FLT}**—Minimum charge voltage required to compensate for the battery's self-discharge rate and maintain full charge on the battery. A value is usually recommended by the battery manufacturer.
- **I_{MAX}**—Fast charge current specified as a function of "C," the capacity of the battery in Ampere-hours (e.g., a charge rate of 1C for a 5Ah battery is 5A). Typical values range from $\frac{1}{10}$ to C, although some battery vendors may approve higher charge rates.

V_{FLT}, V_{BLK}, and I_{MAX} are configured by the user when selecting resistor values for the battery voltage divider network (see Figure 8). V_{FLT} is set by RB1 and RB2 by:

Equation 1

$$\frac{RB1}{RB2} = \frac{(N * V_{FLT})}{2.2V} - 1$$

VBLK is determined by:

Equation 2

$$\frac{RB1}{RB2} + \frac{RB1}{RB3} = \left(\frac{N * V_{BLK}}{2.2}\right) - 1$$

I_{MAX} is determined by:

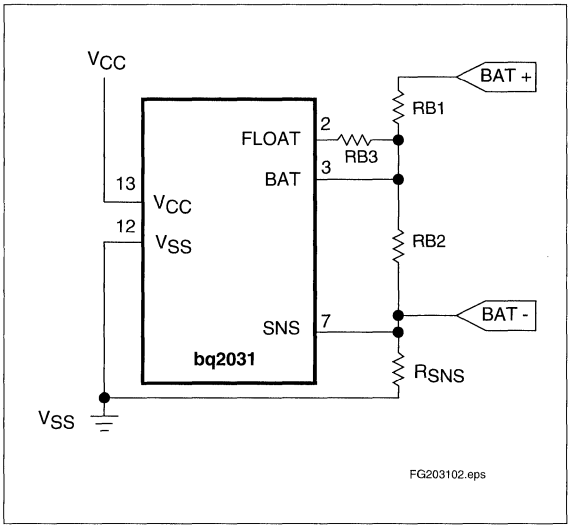


Figure 8. configuring the Battery Divider and Current Sense Circuit

Equation 3

$$I_{MAX} = \frac{0.250V}{R_{SNS}}$$

where:

- N = Number of series cells in the battery pack
- V_{FLT} = Value recommended by manufacturer
- V_{BLK} = Value recommended by manufacturer at 25°C. If you have selected the Two-Step Current algorithm and want Second Difference detection to be your primary fast charge termination criterion, use V_{BLK} = 2.75V.
- I_{MAX} = Desired maximum charge current

The bq2031 internal band-gap reference voltage at 25°C is 2.2V. This reference shifts with temperature at -3.9mV/°C to compensate for the negative temperature coefficient of lead-acid chemistry.

The total resistance presented by the divider between BAT+ and BAT- (RB1 + RB2) should be between 150kΩ and 1MΩ . The minimum value ensures that the divider network does not drain the battery excessively when the power source is disconnected. Exceeding the maximum value increases the noise susceptibility of the BAT pin.

An empirical procedure for setting the values in the resistor network is as follows:

1. Set RB2 to 49.9 kΩ (for 3 to 18 series cells).

6/14

2. Determine RB1 from equation 1 given V_{FLT}.
3. Determine RB3 from equation 2 given V_{BLK}.
4. Determine R_{SNS} from equation 3 given I_{MAX}.

Table 3 shows the results of these calculations at several example cell counts for V_{FLT} = 2.25V and V_{BLK} = 2.45V. 1% resistors are recommended.

Table 3. Example Resistor Values by Number of Cells

Number of Cells	RB1 (kΩ)	RB2 (kΩ)	RB3 (kΩ)
3	102.0	49.9	383.0
6	261.0	49.9	475.0
12	562.0	49.9	511.0
18	866.0	49.9	536.0

I_{MIN}—In the Two-Step Voltage algorithm, I_{MIN} is the level to which charging current must drop to terminate fast charge. In the Two-Step Current algorithm, it is the average value of pulsed current in the maintenance phase. I_{MIN} is a fraction of I_{MAX} programmed by the state of the pin IGSEL and the charging algorithm selected, per Table 4.

Table 4. Programming I_{MIN}

Two-Step Voltage		Two-Step Current	
IGSEL	I_{MIN}	IGSEL	I_{MIN}
L	I_{MAX}/10	L	I_{MAX}/10
H	I_{MAX}/20	H	I_{MAX}/20
Z	I_{MAX}/30	Z	I_{MAX}/40

Setting Temperature Thresholds

The bq2031 senses temperature by monitoring the voltage between the TS and SNS pins. The bq2031 assumes a Negative Temperature Coefficient (NTC) thermistor, so the voltage on the TS pin is inversely proportional to the temperature (see Figure 9). The temperature thresholds used by the bq2031 and their corresponding TS pin voltage are:

TCO—Temperature Cut-Off: Higher limit of the temperature range in which charging is allowed. $V_{TCO} = 0.4 * V_{CC}$.

HTF—High-Temperature Fault: Threshold to which temperature must drop after Temperature Cut-Off is exceeded before charging can begin again. $V_{HTF} = 0.44 * V_{CC}$

LTF—Low-Temperature Fault: Lower limit of the temperature range in which charging is allowed. $V_{LTF} = 0.6 * V_{CC}$.

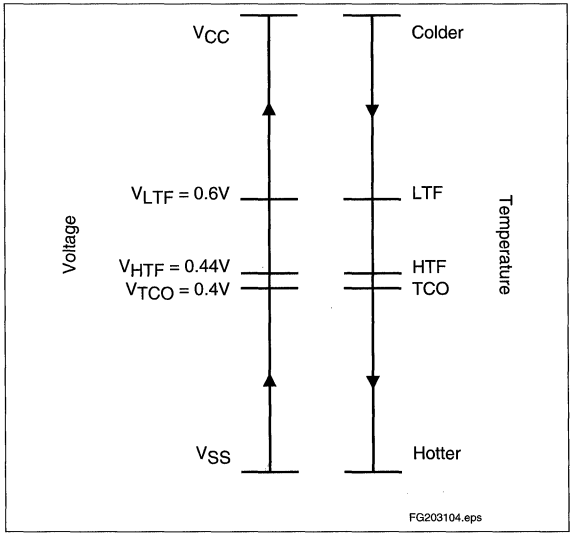


Figure 9. Voltage Equivalent of Current Thresholds

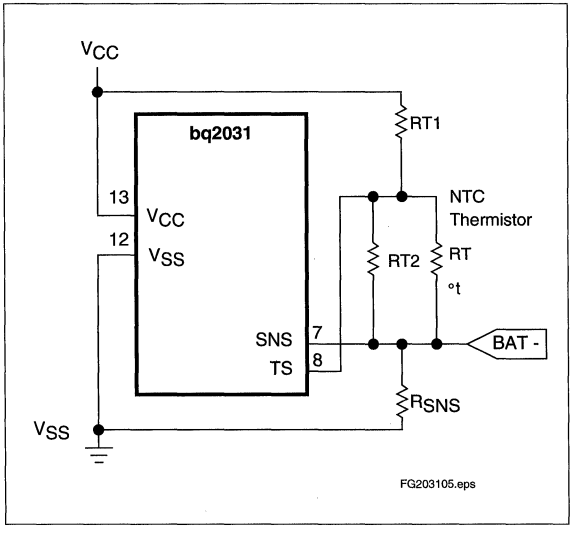


Figure 10. Configuring Temperature Sensing

A resistor-divider network must be implemented that presents the defined voltage levels to the TS pin at the desired temperatures (see Figure 10).

The equations for determining RT1 and RT2 are:

Equation 4

$$0.6 * V_{CC} = \frac{(V_{CC} - 0.250)}{1 + \frac{RT1 * (RT2 + R_{LTF})}{(RT2 * R_{LTF})}}$$

Equation 5

$$0.44 = \frac{1}{1 + \frac{RT1 * (RT2 + R_{HTF})}{(RT2 * R_{HTF})}}$$

where:

- R_{LTF} = Thermistor resistance at LTF
- R_{HTF} = Thermistor resistance at HTF

TCO is determined by the values of RT1 and RT2. 1% resistors are recommended. As an example, the resistor values for several temperature windows computed for a Philips 2333-640-63103 thermistor are shown in Table 5.

Table 5. RT1 and RT2 Values for Temperature Thresholds

LTF (°C)	HTF (°C)	TCO (°C)	RT1 (kΩ)	RT2 (kΩ)
0	45	47	3.57	7.50
5	45	47	3.65	8.66
–5	50	52	2.74	5.36

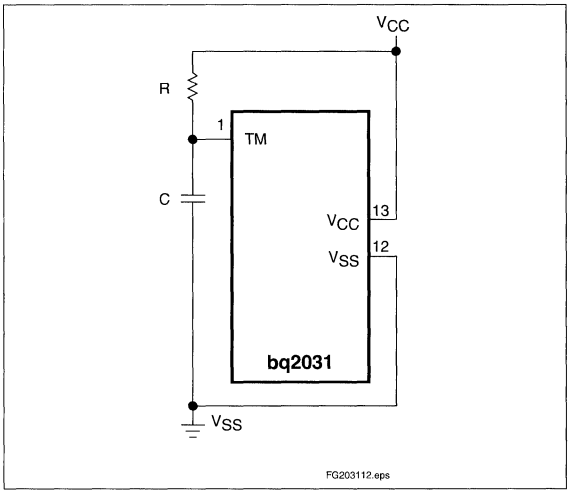


Figure 11. RC Network for Setting MTO

Disabling Temperature Sensing

Temperature sensing may be disabled by removing the thermistor and RT1, and using a value of 100kΩ for RT1 and RT2.

Setting Timers

The user sets the Maximum Time-Out (MTO) value. All other timing periods used in the bq2031 are fixed as fractions of MTO (see Table 6). MTO is set by an R-C network on the TMTO pin as shown in Figure 11.

Table 6. Timing Parameters

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{MTO}	Maximum Time Out range	1	-	24	hours
t_{QT1}	Qualification time-out test 1	-	$0.02t_{MTO}$	-	-
t_{QT2}	Qualification time-out test 2	-	$0.16t_{MTO}$	-	-
t_{DV}	$-\Delta^2V$ termination sample frequency	-	$0.008t_{MTO}$	-	-
t_{HO1}	Qualification test 2 hold-off period	-	$0.002t_{MTO}$	-	-
t_{HO2}	Bulk-charge hold-off period	-	$0.015t_{MTO}$	-	-

8/14

The equation for MTO is:

Equation 6

$$\text{MTO (in hours)} = 0.5 * R * C$$

where R is in kΩ and C is in μF. The value for C must not exceed 0.1μF.

Example: An MTO of 5 hours is set by R = 100kΩ and C = 0.1μF

Switch-Mode Power Conversion

The bq2031 incorporates the necessary PWM control circuitry to support switch-mode voltage and current regulation.

Figure 12 shows a functional block diagram of a switch-mode buck topology converter using the bq2031. The battery voltage is divided down to a per-cell equivalent value at the BAT pin. During voltage regulation, the voltage on the BAT pin (V_{BAT}) is regulated to the internal band-gap reference of 2.2V at 25°C (with a temperature drift of -3.9 mV/°C). The charge current through the inductor L is sensed across the resistor R_{SNS}. During current regulation, the bq2031 regulates the voltage on the SNS pin (V_{SNS}) to a temperature-compensated reference of 0.250V.

The passive components C_I on the I_{COMP} pin, R_V and C_V on the V_{COMP} pin, and C_F across the high side of the battery voltage divider form the phase compensation network for the current and voltage control loops, respectively. The diodes (Db1 and Db2) serve to prevent battery drain when VDC is absent, while the pull-up resistor (R_P) is used to detect battery removal. The resistor R_S, typically a few tens of mΩ, is optional and depends on the battery impedance and the resistance of the battery leads to and from the charger board.

Pulse-Width Modulator

The bq2031 incorporates two PWM circuits, one for each control loop (voltage and current, see Figure 13). Each PWM circuit runs off a common saw-tooth waveform (V_S) whose time-base is controlled by a timing capacitor (CPWM) on the TPWM pin.

The relationship between CPWM and the switching frequency (F_S) is given by :

Equation 7

$$F_S = \frac{0.1}{C_{PWM}} \text{ kHz}$$

where CPWM is in μF.

Each PWM loop starts with a comparator whose positive terminal is driven by V_S. The negative terminal is driven by the output of an Operational Transconductance Amplifier (OTA) which, with the compensation network connected via V_{COMP} or I_{COMP}, generates the control signal V_C. The OTA characteristics are: R_O = 250kΩ; G_M = 0.42m-mho; gain bandwidth = 80MHz. The output of each comparator, along with the ramp waveform (V_S), is used to generate a pulse-width modulated waveform at a constant frequency on the MOD output. Figure 14 shows the relationship of MOD with V_C and V_S.

The MOD output swings rail-to-rail and can source and sink 10mA. It is used to control the drive circuitry of the switching transistor.

The pulse-width modulated square-wave signal on the MOD pin is synchronized to the internal sawtooth ramp signal. The ramp-down time (T_D) is fixed at approximately 20% of the ramp time-period (T_P). This limits the maximum duty-cycle achievable to approximately 80%. See Figure 14.

Example: At a switching frequency of F_S = 100kHz, T_D = 2μs.

Inductor Selection

The inductor selection criteria for a DC-DC buck converter vary depending on the charging algorithm used. For the Two-Step Current and Pulsed Current charge algorithms, the inductor equation is:

Equation 8

$$L = \frac{(N * V_{BLK} * 0.5)}{F * \Delta I}$$

where:

- N = Number of cells
- V_{BLK} = Bulk voltage per cell, in volts
- F_S = Switching frequency, in Hertz
- ΔI = Ripple current at I_{MAX}, in amperes

The ripple current is usually set between 20–25% of I_{MAX}.

Example: A 6-cell SLA battery is to be charged at I_{MAX} = 2.75A in a buck topology running at 100kHz. The V_{BLK} threshold is set at 2.45V per cell and the charger is configured for Pulsed Current mode. Assuming a ripple = 25% of I_{MAX}, the inductor value required is:

Equation 9

$$L = \frac{(6 * 2.45 * 0.5)}{(100000 * 0.6875)} = 107\mu H$$

The inductor formula for the Two-Step Voltage charge algorithm is dictated by the inductor current, which must remain continuous down to I_{MIN} during Fast Charge phase 2 (voltage regulation phase).

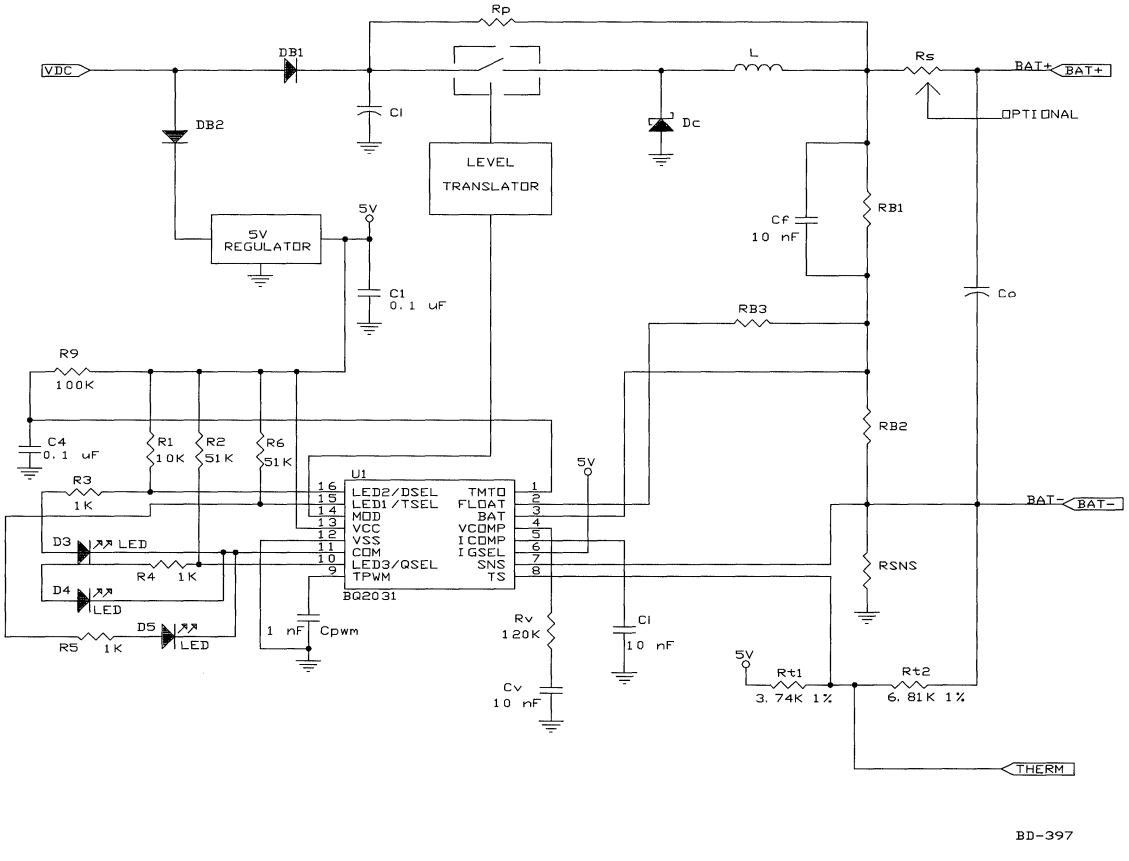


Figure 12. Functional Diagram of a Switch-Mode Buck Regulator Lead-Acid Charger Using the bq2031

10/14

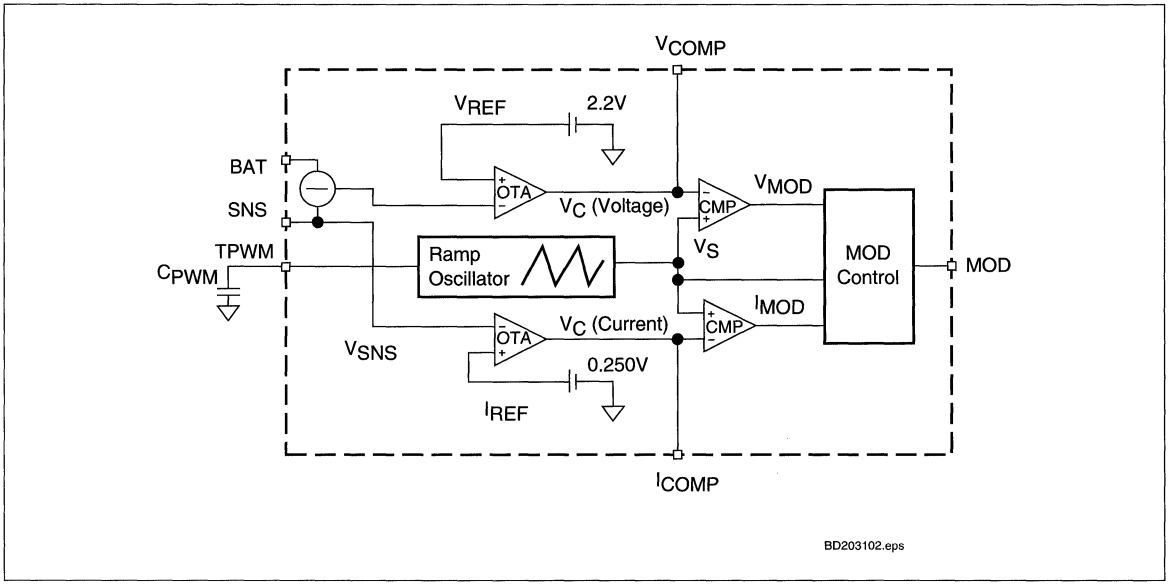


Figure 13. Block Diagram of the bq2031 PWM Control Circuitry

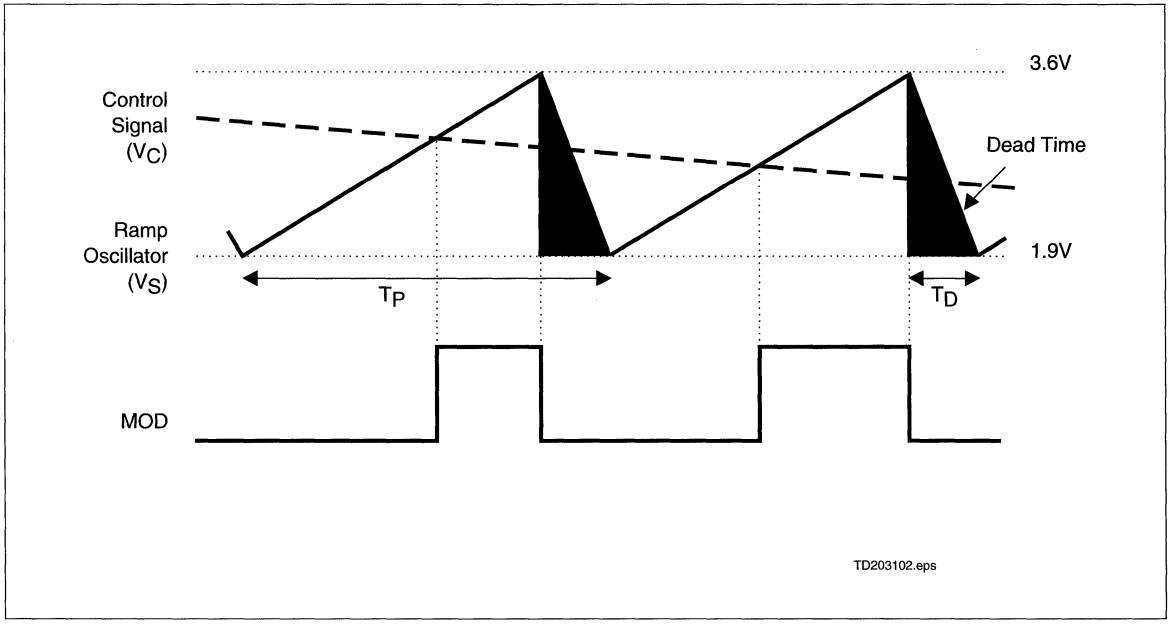


Figure 14. Relationship of MOD Output to Sawtooth Waveform V_S and Control Signal V_C

Equation 10

$$L = \frac{N * V_{BLK} * 0.5}{F_S * 2 * I_{MIN}}$$

Example: A 6-cell SLA battery is to be charged at I_{MAX} = 2.75A in a buck topology running at 100kHz. The V_{BLK} threshold is set at 2.45V per cell and the charger is configured for Two-Step Voltage mode, with I_{MIN} = $I_{MAX}/20$. The inductor value required is:

Equation 11

$$L = \frac{6 * 2.45 * 0.5}{(100000 * 2 * 0.1375)} = 267\mu H$$

Phase Compensation

For buck-mode switching applications, the suggested component values shown in Figure 12 are good starting points. More details on the calculations used in this program are available in the application note entitled "Switch-Mode Power Converson Using the bq2031." For assistance with other power supply topologies, contact one of our field application engineers.

Miscellaneous Issues

V_{CC} Supply

The V_{CC} supply provides bq2031 power and serves as the reference voltage for all temperature sense thresholds (V_{LTF}, V_{HTF}, and V_{TCO}) and the battery voltage thresholds V_{HCO} and V_{MIN}. The timer thresholds (MTO and its derivatives) are trimmed within 5% of the typical value with V_{CC} = 5V.

The V_{BLK} and V_{FLT} thresholds are set from an external divider network powered by the battery. These thresholds are referenced to an internal band-gap reference, and the accuracy of voltage regulation will not be adversely affected by variation in V_{CC}. The current regulation threshold (I_{MAX}) is referenced to a temperature compensated reference and is also unaffected by V_{CC}.

DC Power Supply

The DC power supply voltage (V_{DC}) for a switch-mode application must satisfy the following criterion:

Equation 12

$$V_{DC} = (N * V_{BLK} * 1.2) + 2$$

where:

- N = Number of cells
- V_{BLK} = Bulk voltage threshold per cell

Logical Control of Charging

Charge Inhibit

An inhibit input may be implemented by connecting the cathode of a small-signal diode to the TS pin. A CMOS logic-level "1" applied to the anode of the diode then functions as an inhibit input, by driving the temperature sense voltage out of its allowed range and simulating an under-temperature condition. The bq2031 enters the Charge Pending state, shutting off charging current (driving MOD low) and suspending all timers. When the Inhibit signal is allowed to float, the bq2031 returns to its previous state (as long as the temperature is still within the allowed range). The bq2031 restarts (but does not reset) its timers, and the suspended charge cycle resumes at the point where it stopped.

Reset

A logical Reset signal for the bq2031 can be created in a manner similar to the Charge Inhibit input described above. Instead of being connected to the T_S pin, however, the diode is connected to the BAT input. In this configuration, a logic "1" on the diode drives V_{BAT} above V_{HCO}, simulating battery removal. The bq2031 enters the Fault state and waits to see a battery insertion; V_{BAT} rising past V_{LCO} or falling past V_{HCO}. Removing the logic "1" from the diode creates this transition (as long as a battery is still present), and the bq2031 starts a new charge cycle.

Caution: To avoid damage to the bq2031, always keep the voltage applied to the anode of the diode below V_{CC} for either the Charge Inhibit or Reset implementations.

Layout Guidelines

Printed circuit board layout must adhere to the following guidelines to minimize noise injection on the high-impedance pins (BAT, V_{COMP}, I_{COMP}, and SNS).

1. Use a single-point grounding technique such that the isolated small-signal ground path and the high-current power ground path return to the power supply ground.
2. The charging path components and traces must be isolated from the voltage and current feedback small signal paths.
3. 0.1µF and 10µF decoupling capacitors must be placed close to the V_{CC} pin. This also helps to prevent voltage dips while the bq2031 is driving the LEDs.
4. A 100pF capacitor, if used for coupling the BAT and SNS pins, must be placed close to those pins.
5. The compensation network on I_{COMP} and V_{COMP} must be placed close to their respective pins.

6. Minimize loop area in paths with high pulsating currents.

Battery Removal Detection

The bq2031 interprets V_{BAT} rising past V_{HCO} or falling past V_{LCO} as battery removal, and the bq2031 enters the Fault state until a new battery insertion is seen. The battery removal transitions are precluded during periods of voltage regulation unless circuitry (e.g., a pull-up to V_{DC}) is provided to pull V_{BAT} out of the "battery present" range.

Voltage regulation occurs during phase 2 of the Two-Step Voltage fast charge algorithm and in battery qualification test 1 which precedes all three algorithms. The time-out period of this test (= 0.02 * MTO) is at least 1.2 minutes and may be as long as 28.8 minutes. Unless waiting through this period before detecting battery removal is acceptable, the pull-up is required in the purely current regulated algorithms as well. A diode should also be installed in the path of the pull-up to prevent the power supply from draining the battery when the supply is turned off. Refer to resistor R12 and diode D3 in the example design in Figure 15.

This pull-up creates a background trickle charge current to the battery that can be minimized by minimizing the voltage overhead; that is, the voltage difference between the V_{DC} supply and the battery stack.

Load-Only Operation

The bq2031 supports the case in which the charger must supply the load in the absence of a battery, provided the load can pass the two pre-charge qualifications tests (draw current of at least I_{COND} when regulated at V_{FLT} + 0.25V and maintain voltage of at least V_{MIN} when regulated at I_{COND}). Further, the load must not create conditions that cause fast charge termination or it must be able to tolerate the conditions of maintenance regulation for the charge algorithm selected. This is regulation at V_{FLT} in the case of the Two-Step Voltage algorithm or constant or hysteretic pulsed current supply in the case of the Two-Step Current and Pulsed Current algorithms, respectively. This can be a problem for intermittent loads unless circuitry is provided to maintain these conditions during the low-load or no-load periods.

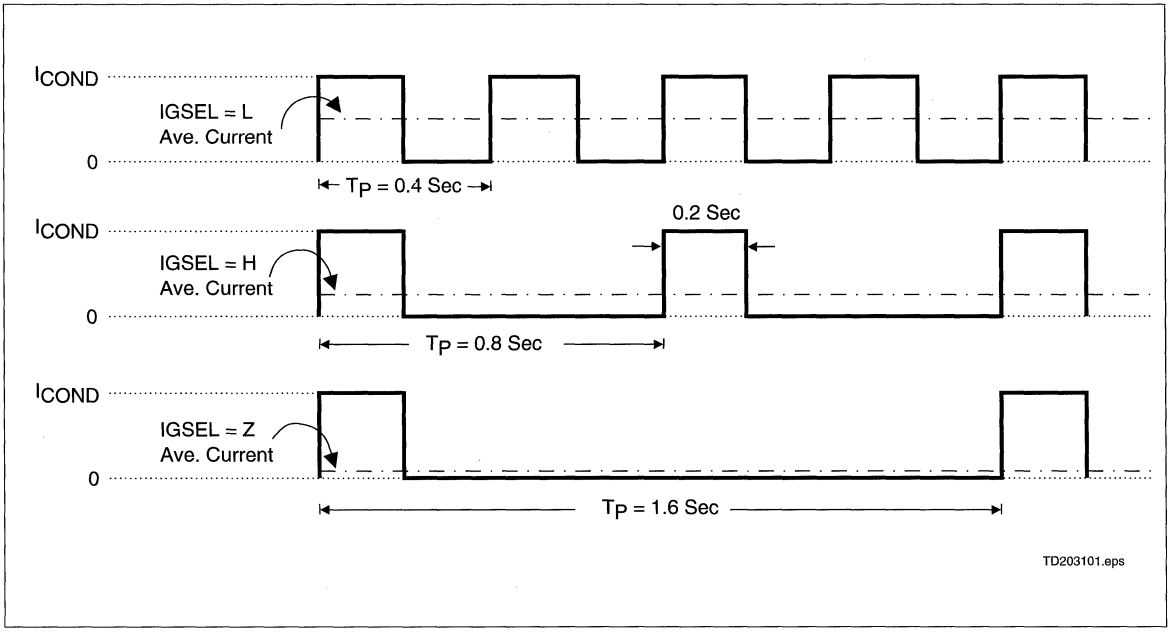


Figure 15. Implementation of Fixed-Pulse Maintenance Charge

Back-up Supply Regulation

To protect the system from damage during periods of fast charge voltage regulation, the bq2031 regulates to I_{MAX} if the current tries to rise above that level, and has an absolute current limit of 1.25 * I_{MAX}. Similarly, during periods of fast charge current regulation, the bq2031 enforces a V_{BLK} upper limit on voltage, and regulates to V_{BLK} if the voltage tries to rise above this level. During the maintenance phase, the bq2031 regulates to V_{FLT} and I_{COND} during periods of current or voltage regulation, respectively.

Applications Example: Single-Ended Buck Charger

For an application example, please see the DV2031S1 data sheet and schematic.

Appendix A: Implementation Details of Pulsed Maintenance Charging

Two-Step Current Algorithm

Maintenance charging in the Two-Step Current Algorithm is implemented by varying the period (TP) of a fixed current (I_{COND} = I_{MAX}/5) and duration (0.2 second) pulse to achieve the configured average maintenance current value. See Figure 16.

Maintenance current can be calculated by:

Equation 14

$$\text{Maintenance current} = \frac{((0.2) * I_{COND})}{T_P} = \frac{((0.04) * I_{MAX})}{T_P}$$

where TP is the period of the waveform in seconds.

Table 7 gives the values of TP programmed by IGSEL.

Table 7. Fixed-Pulse Period by IGSEL

IGSEL	T_P (s)
L	0.4
H	0.8
Z	1.6

Revision History

Charge No.	Page No.	Description	Nature of Change
1	4, 5	Renamed	Figure 7 was: Pulsed Current; Is: Two-Step Current
1	6, 8	Changed values in Equations 3 and 4	Was: 0.275V; is now 0.250V
1	9	Under Switch-Mode Power Conversion	Changed value, was: 0.275V; is now 0.250V
1	11	Figure 13 changed	Block diagram has been reconfigured. VC was 0.275V; us biw 0.250V
1	13	Applications Example changed	Changed to: For an application example, please see the DV2031S1 datasheet and schmatic
1	14	Figure 15. Example Schematic of a Single-Ended Buck Topology Charger	Deleted
1	15	Table 7. Parts List for Single-Ended Buck Charger	Deleted
2	8	Equation 4	Was: -0.275 Is: -0.250
2	9	Temperature-compensated reference	Was: 0.275V Is: 0.250V
2	12	Equation 12	Was: V_{DC} = (N * V_{BLK}) + 3V Is: V_{DC} = (N * V_{BLK} * 1.2) + 2
3	12	Clarify description for phase compensation	

Notes: Change 1 = April 1997 B changes from Dec. 1995.
Change 2 = Oct. 1997 C changes from April 1997 B.

14/14

UNITRODE

U-511 Switch-Mode Power Conversion Using the bq2031

Introduction

The bq2031 incorporates the necessary PWM control circuitry to support switch-mode voltage and current regulation, as required by its charge control function block. This application note describes how to configure the bq2031 in buck mode switching power supply topology. A methodology for phase compensation of the voltage and current feedback loops is recommended. A brief description of the PWM control circuitry and phase compensation criteria appears below, followed by a discussion dealing with topology-specific issues.

The Pulse-Width Modulator

The bq2031 incorporates two voltage mode direct duty cycle Pulse-Width Modulators, one for each control loop (voltage and current). A block diagram is shown in Figure 1. Each PWM runs off a common saw-tooth waveform whose time-base is controlled by a capacitor, C_{PWM} on the TPWM pin.

The relationship of C_{PWM} to the switching frequency, FS is given by:

Equation 1

$$F_S = \frac{0.1}{C_{PWM}} \text{ kHz}$$

where:

- C_{PWM} is in µF.

The PWM for either loop consists of a comparator whose positive terminal is driven by the output of the sawtooth ramp signal, V_S, while the negative terminal is driven by the output of an Operational Transconductance Amplifier (OTA). The output is the control signal, V_C. The output of each PWM is logically ORed to generate a constant frequency pulse width modulated rectangular waveform at the MOD output. The relationship of the MOD output with respect to the OTA control signal, V_C, and the sawtooth ramp signal, V_S, is shown in Figure 2.

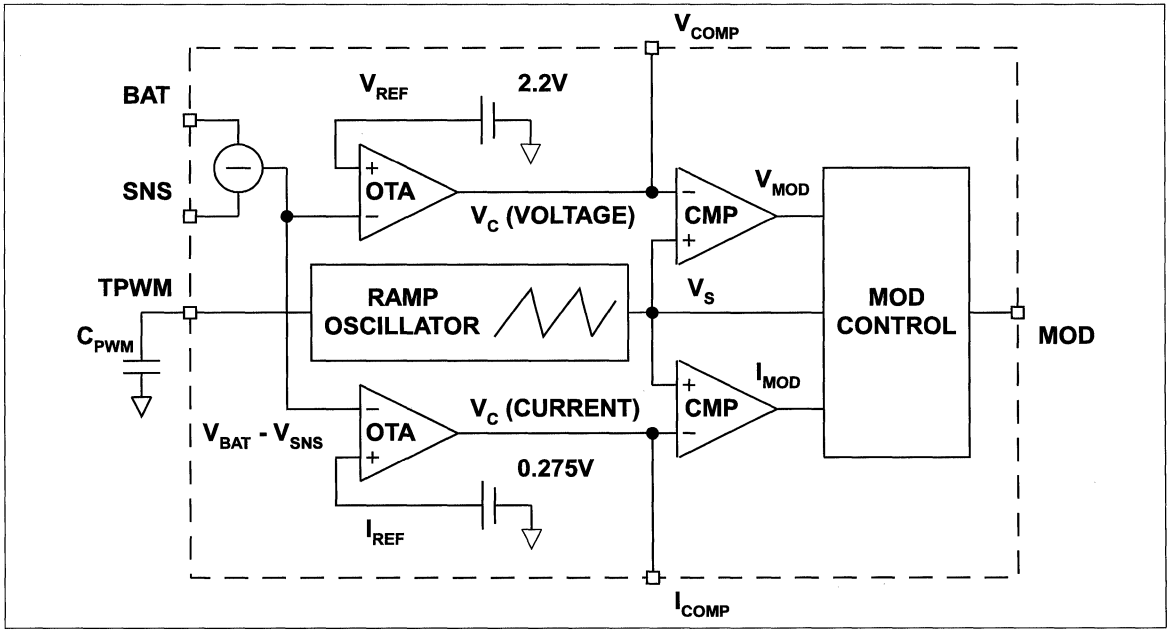


Figure 1. Block Diagram of the bq2031 PWM Control Circuitry

The MOD output swings rail-to-rail and can source and sink 10mA. It is used to control a switching transistor in a switch-mode application.

The pulse width modulated square wave signal on the MOD pin is synchronized to the internal sawtooth ramp signal. The ramp-down time (T_D) is fixed at approximately 20% of the total period (T_P). This condition limits the maximum duty-cycle to approximately 80%. For example, with a switching frequency F_S = 100kHz, T_D = 2µs.

Phase Compensation

As in any feedback control system, phase compensation is necessary to achieve both loop stability and dynamic line and load response. As shown in the PWM block diagram (Figure 1) the bq2031 provides two high-impedance nodes, I_{COMP} and V_{COMP}, for current and voltage loop phase compensation. In a battery charger application the dynamic load response is not as much a concern as loop stability, especially during voltage regulation.

Voltage and Current Control Loops

Two independent PWM function blocks implement direct duty cycle control for current and voltage regulation. During current regulation the feedback signal is the voltage across the current sense resistor, R_{SNS}, as shown in the current feedback loop model of Figure 3.

The current regulation total open-loop transfer function, IL(s), may be expressed as:

Equation 2

$$I_L(s) = A(s) * P_\omega(s) * P_T(s)$$

where:

- A(s) is OTA error amplifier and compensation network transfer function, V_C/V_O
- $P\omega(s)$ is the PWM transfer function, D/V_C
- $P_T(s)$ is the power train transfer function, $V_{O/D}$
- D is the duty cycle of the PWM waveform

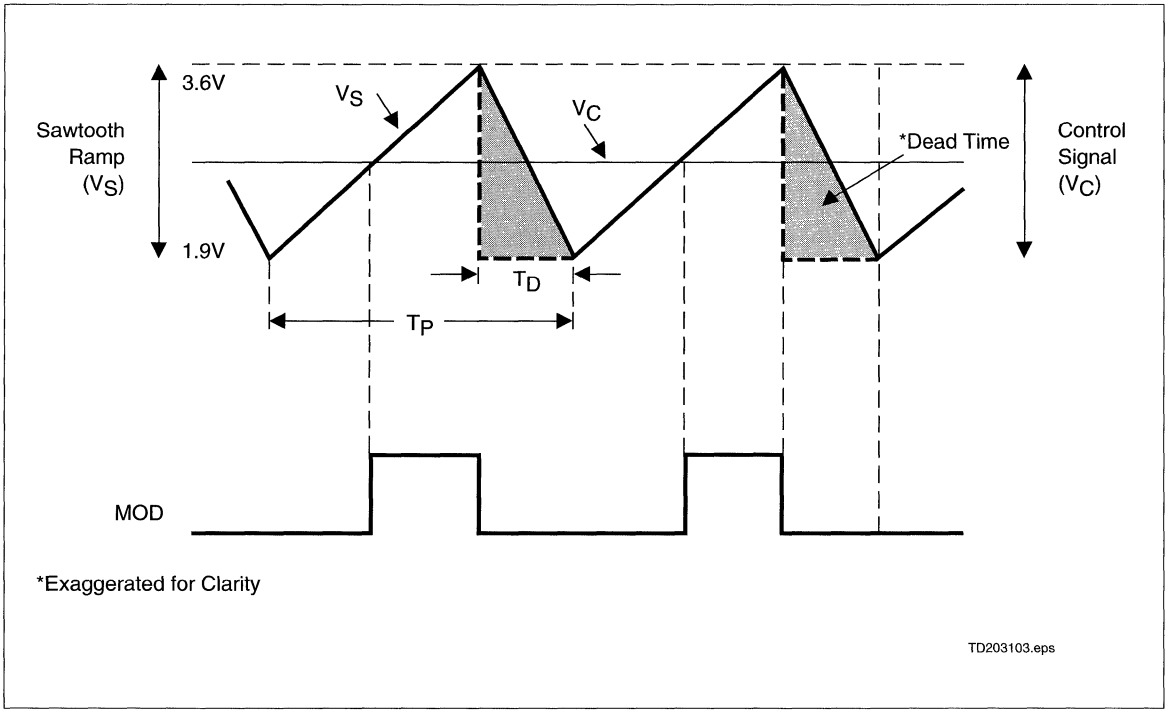


Figure 2. Relationship of MOD Output to Sawtooth Waveform V_S and Control Signal V_C

During voltage regulation, the feedback signal is the voltage sensed at the midpoint of the battery voltage divider (between RB1 and RB2). The voltage feedback control loop is modeled as shown in Figure 4.

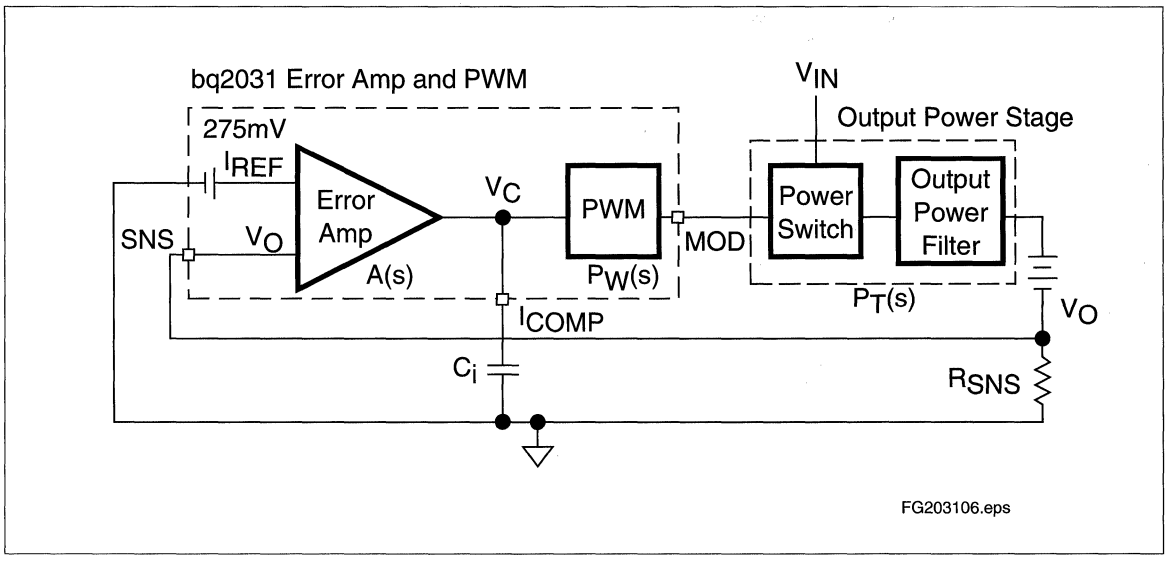


Figure 3. Model of Current Control Loop

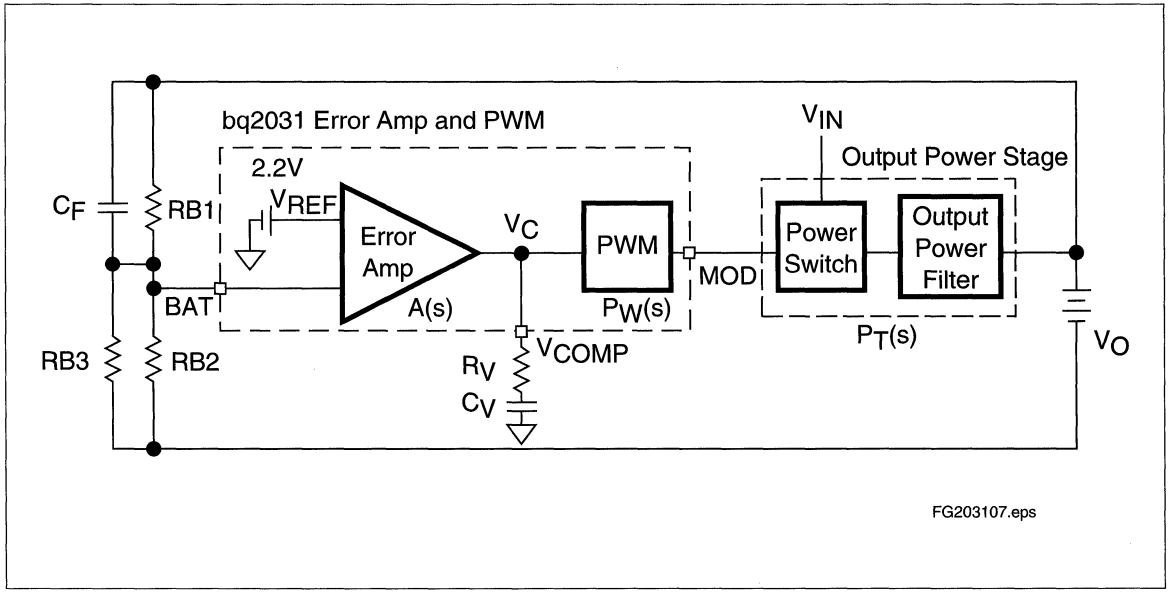


Figure 4. Model of Voltage Control Loop

For voltage regulation, the total open-loop transfer function, VL(s), may be expressed as:

Equation 3

$$V_L(s) = A(s) * P_\varpi(s) * P_T(s)$$

where:

- $P_T(s)$ is the transfer function of the output power stage, $V_{O/D}$.

The switching frequency and circuit topology of the system dictate the gain-frequency characteristics of the output power stage. The PWM characteristics are fixed within the bq2031. This situation leaves the OTA and its associated compensation network as the only function block whose characteristics can be changed to achieve the desired loop stability and response.

The Error Amplifier

The bq2031 error amplifiers are the OTA (Operational Transconductance Amplifier) type. The parameters of interest (see Figure 6) are:

- Transconductance gain, gm = 0.42 milli-mhos
- Output resistance of error amplifier, R = 250kΩ
- Gain Bandwidth product = 80MHz

This situation fixes the maximum voltage gain at 105 (gm*R) or 40.4dB, which is good out to the 3dB corner frequency of 2MHz. Note that the 40dB gain is the maximum achievable, regardless of the impedance across the output to ground.

Criteria for Loop Stability

The gain and phase characteristics of the OTA and associated circuitry must be adjusted to meet the following three criteria for loop stability:

1. Total open-loop gain (IL(s) and VL(s) above) must be forced to 0dB at a crossover frequency (FC) equal to at least 1/6 the switching frequency (FS).
2. The phase of the total open-loop gain at FC must be at least 45 degress less than 180 degrees.

The above criteria for loop stability can be easily achieved if the total loop-gain transfer function exhibits dominant pole characteristics as shown in Figure 5.

Stabilizing the Current Loop

From Equation 2, the total open-loop transfer function is expressed as:

$$I_L(s) = A(s) * P_\varpi(s) * P_T(s)$$

Pω(s) (the transfer function for the PWM) is given as:

$$P_\varpi(s) = \frac{D_{MAX}}{V_S}$$

where:

- D_{MAX} is the maximum duty cycle of the PWM waveform
- V_S is the peak-to-peak amplitude of the sawtooth waveform

For the bq2031, V_S is fixed at 1.7V, and the maximum duty cycle is 80%. This condition reduces the PWM transfer function to:

Equation 4

$$P_\varpi(s) = 0.47$$

$P_T(s)$ (the transfer function for the output power stage) is given as:

Equation 5

$$P_T(s) = \frac{V_{IN} * (1 + s * R_i * C_B) * R_{SNS}}{R_i + R_{SNS} + s[L + R_O R_L * C_B + R_{SNS} + R_i * C_B] + s^2 L * R_L * C_B}$$

where:

- s is the complex variable jω
- V_{IN} is DC input voltage
- CB is the equivalent internal battery capacitance (see Figure 11)
- L is inductor value
- R_L is inductor resistance
- R_i is the equivalent internal battery resistance (see Figure 11)
- R_{SNS} is sense resistor value
- R_O is the equivalent battery load resistance (see Figure 11)

Stabilizing the current loop requires the compensation of the loop error amplifier to be such that the transfer function A(s) has dominant pole characteristics. This can be achieved by adding a capacitor, C_i, between ground and the output of the OTA error amplier as shown in Figure 6.

The transfer function A(s) is given as :

$$A(s) = \frac{V_C}{V_O} = \frac{(g_m * R)}{(1 + (s * R * C_i))}$$

4/16

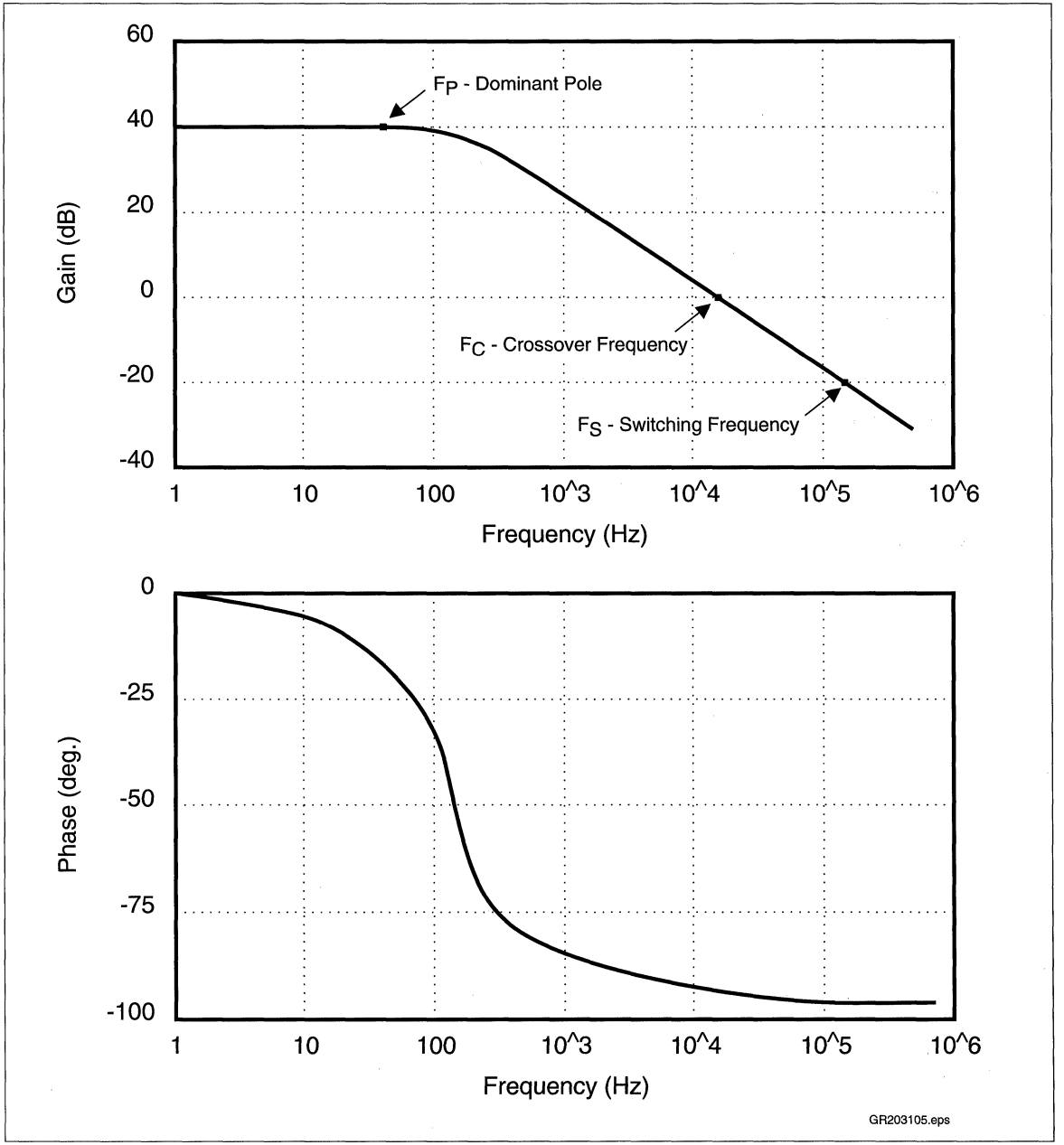


Figure 5. Target Gain and Phase Characteristics of a Stable Closed-Loop System

Substituting values for gm and R, we get:

Equation 6

$$A(s) = \frac{105}{(1 + (s * 250000 * C_i))}$$

where:

- C_i is the output capacitance of the error amplifier (see Figure 6)

Substituting Equations 4 and 5 in Equation 2 gives the compensated total current loop gain transfer function:

Equation 7

$$I_L(s) = \frac{0.47 * V_{IN} * 105}{(1 + (s * 250000 * C_i))}$$

As shown in the bode plot for IL(s) (Figure 7), C_i can be varied to achieve the necessary phase and gain margin for different V_{IN} values.

Stabilizing the Voltage Loop

Recalling Equation 3, the voltage regulation open-loop transfer function can be expressed as:

$$V_L(s) = A(s) * P_\varpi(s) * P_T(s)$$

The output power stage transfer function $P_T(s)$ depends on the inductor and battery impedances.

The components required to compensate the error amplifier for achieving voltage loop stability appear in Figure 8.

The resultant transfer function of the compensated error amplifier may be expressed as:

Equation 8

$$A(s) = \frac{D * 105 * (1 + s * RB1 * C_F) * (1 + (s * R_V * C_V))}{(1 + s * D * RB_1 * C_F) * (1 + s * (2.5 * 10^5 + R_V) * C_V)}$$

where:

- D = Battery voltage divider ratio during voltage regulation:

$$D = \frac{RB2 \parallel RB3}{((RB2 \parallel RB3) + RB1)}$$

  - **Note:** See the application note entitled "Using the bq2031 to Charge Lead-Acid Batteries" for instructions on calculating RB1, RB2, and RB3.
- RB1 = the resistor value between the high side of the battery stack and the BAT pin in the battery voltage divider network
- C_F = the capacitance in parallel with RB1
- R_V = series resistance between V_{COMP} and ground
- C_V = series capacitance between V_{COMP} and ground

(See Figure 8 and **Voltage Loop Error Amplifier Compensation** below for calculating the values of C_F, R_V, and C_V.)

The above transfer function contributes two poles and two zeros.

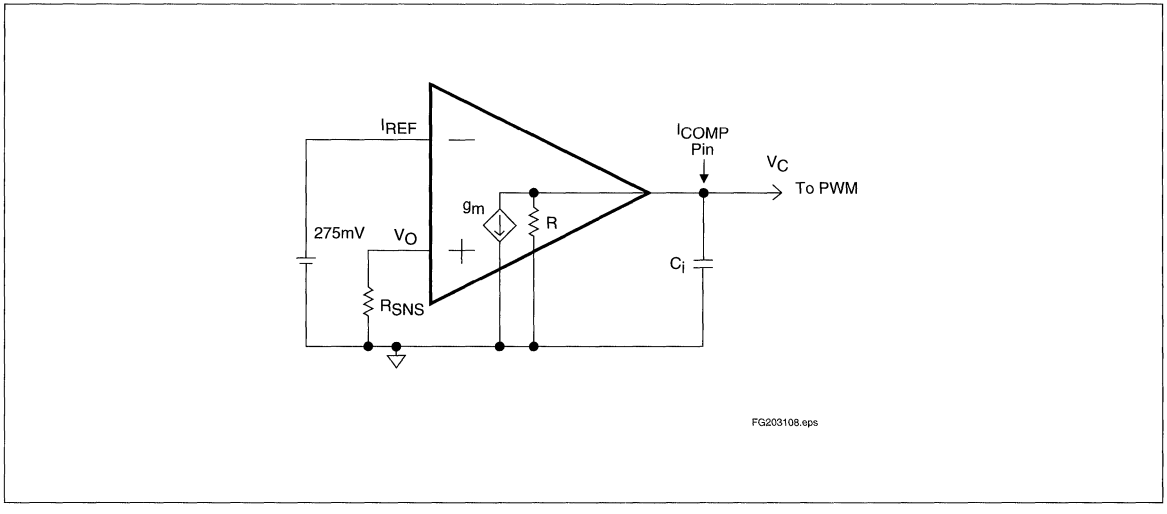


Figure 6. Compensation Network for the Current Loop

6/16

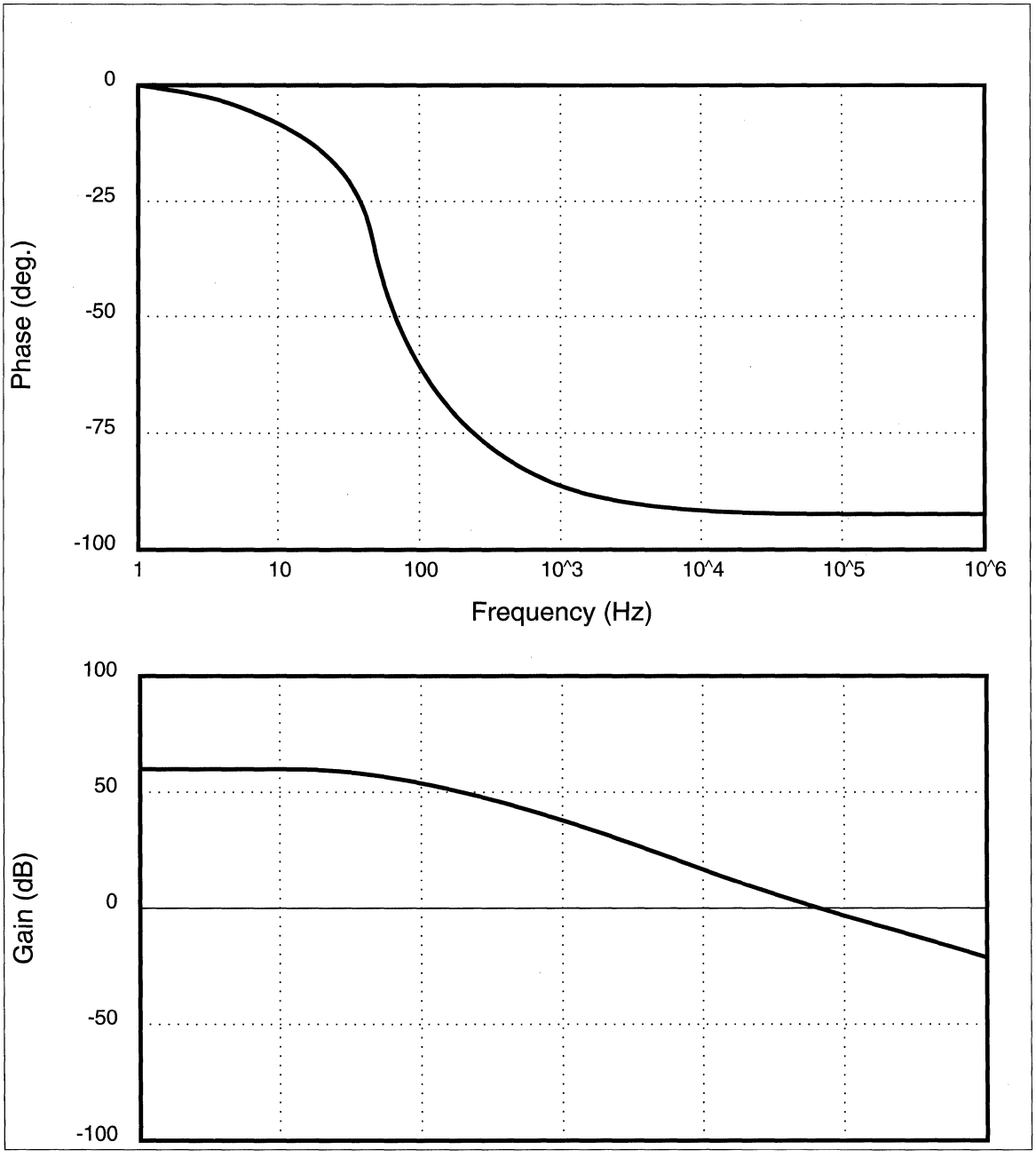


Figure 7. Bode Plot of the Current Loop-Gain Transfer Function for V_{IN} = 24V

Poles (Equation 9)

$$fp1 = \frac{1}{(2\pi * (2.5 * 10^5 + R_V) * C_V)}$$

$$fp2 = \frac{1}{(2\pi * D * RB1 * C_F)}$$

Zeros (Equation 10)

$$fz1 = \frac{1}{(2\pi * RB1 * C_F)}$$

$$fz2 = \frac{1}{(2\pi * R_V * C_V)}$$

The effect of this feedback and compensation network on the transfer function of A(s) is shown in Figure 9.

Voltage Loop Compensation for Buck Topology

Figure 10 shows a functional diagram of a switch-mode buck topology converter using the bq2031. The battery voltage is divided down to a per-cell equivalent value at the BAT pin. During voltage regulation, the voltage on the BAT pin (V_{BAT}) is regulated to the internal band-gap reference of 2.2V (with a temperature drift of -3.9mV/°C). The charge current through the inductor L is sensed across the resistor R_{SNS}. During current regulation, the bq2031 regulates the voltage on the SNS pin (V_{SNS}) to a temperature-compensated reference of 0.275V. This in turn regulates the current to I_{MAX}, provided that a properly designed resistor network is in use.

The passive component C on the I_{COMP} pin and R_V and C_V on the V_{COMP} pin form the phase compensation network for the current and voltage control loops, respectively. The diode (D_{b1}) prevents battery drain when V_{DC} is absent, while the pull-up resistor (R) detects battery removal. The resistor R13, typically a few tens of mΩ, is optional and depends on the battery impedance and the resistance of the battery leads to and from the charger board.

The Output Power Stage

The output power stage in a buck topology charger comprises the inductor L and the parallel combination of the output capacitor, Co, and impedance of the battery (see Figure 12). The output capacitor is electrolytic and in the range from 47µF to 100µF. It nullifies the inductive effect of long leads from the charger terminals to the battery.

Inductor Selection

The inductor selection criteria for a DC-DC buck converter vary depending on the charging algorithm used. For the Two-Step Current and Pulsed Current charge algorithms, the inductor equation is:

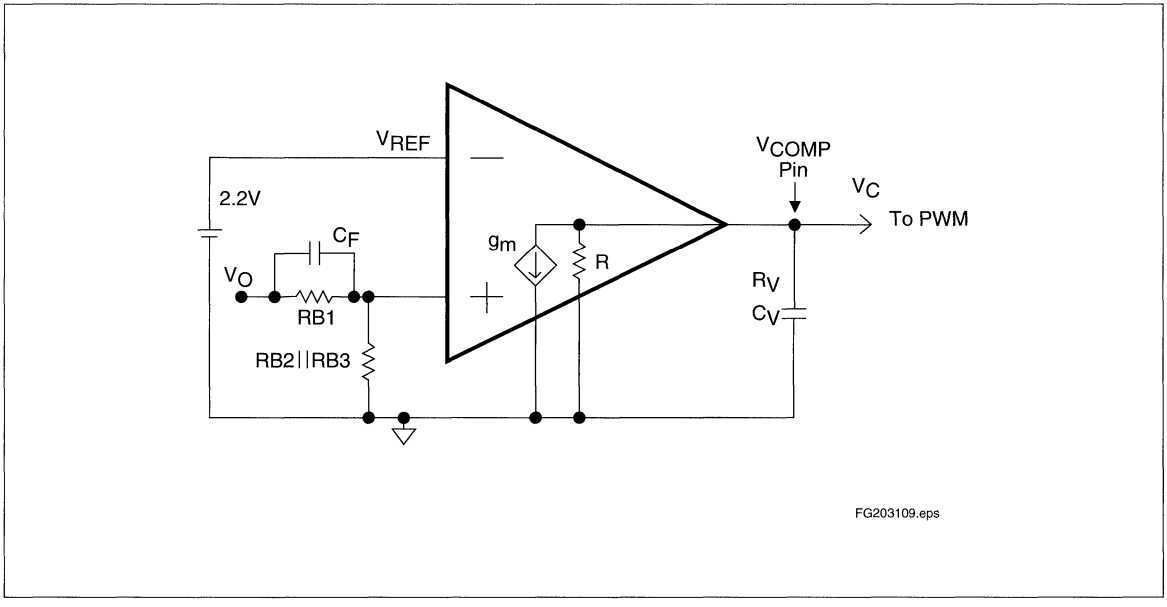


Figure 8. Compensation Network for the Voltage Loop

8/16

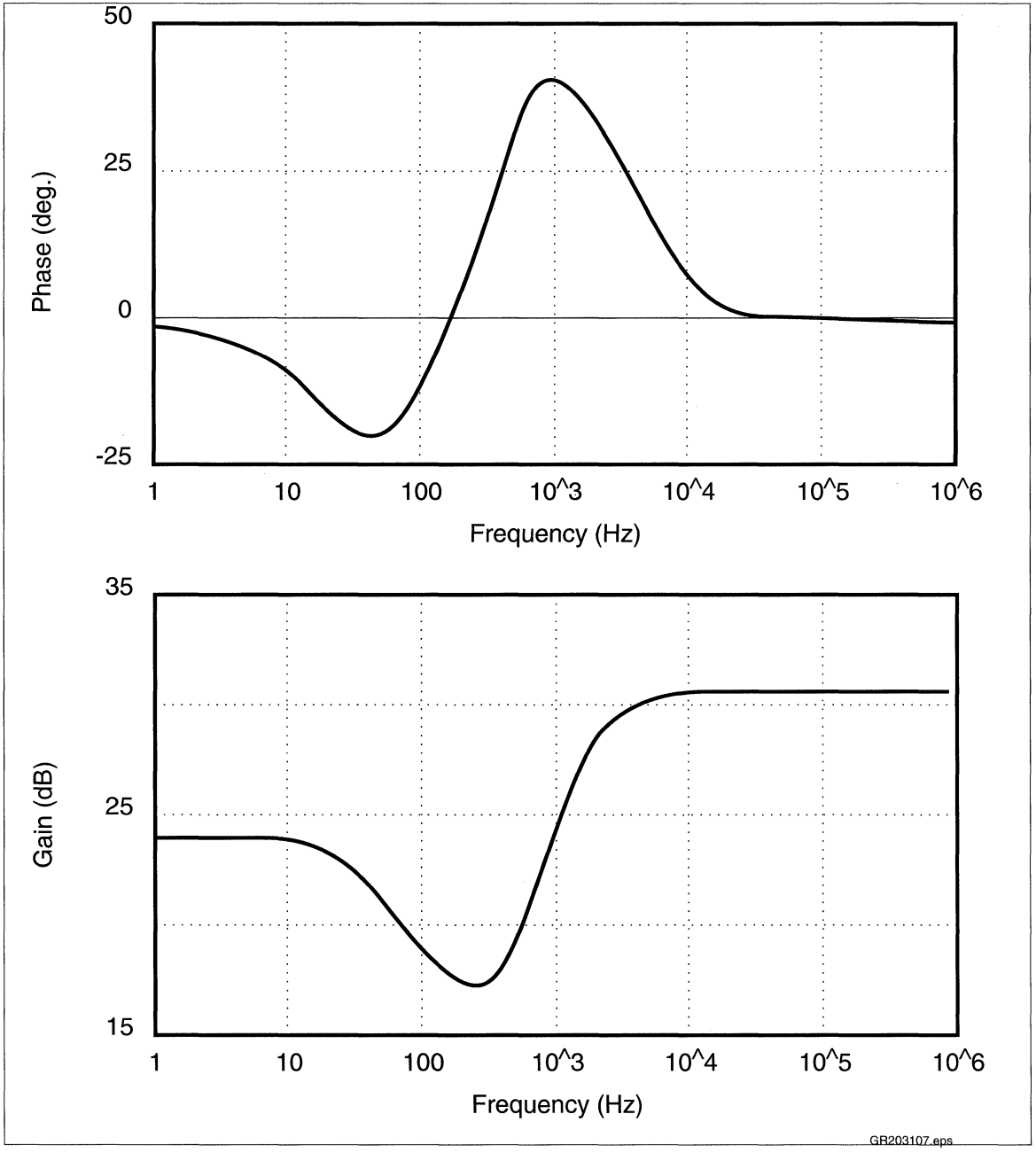


Figure 9. Effect of Compensation Network on Amplifier Transfer Function, A(s)

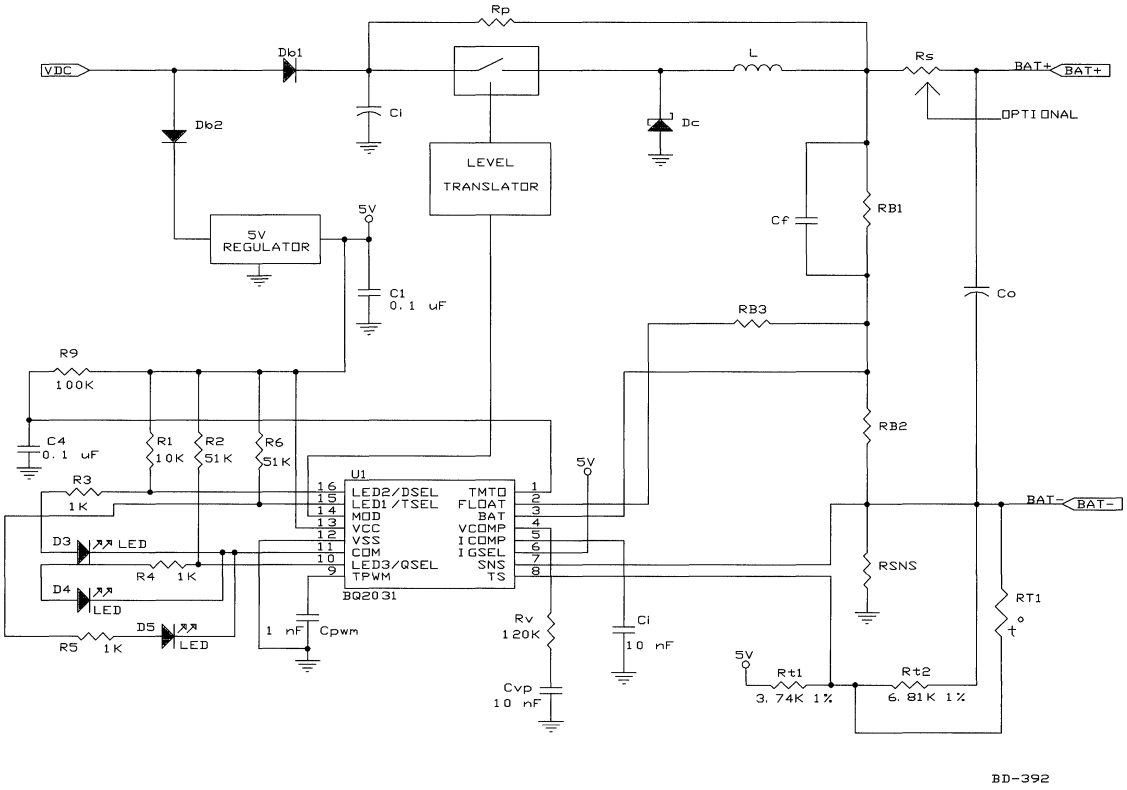


Figure 10. Functional Diagram of a Switch-Mode Buck Regulator Lead-Acid Charger Using the bq2031

10/16

Equation 11

$$L = \frac{(N * V_{BLK} * 0.5)}{F * \Delta I}$$

where:

- N = number of cells
- V_{BLK} = bulk voltage per cell, in volts
- F_S = switching frequency, in Hertz
- ΔI = ripple current at I_{MAX}, in amperes

The ripple current is usually set between 20–25% of I_{MAX}.

Example: A 6-cell SLA battery is to be charged at I_{MAX} = 2.75A in a buck topology running at 100kHz. The V_{BLK} threshold is set at 2.45V per cell and the charger is configured for Pulsed Current mode. Assuming a ripple = 25% of I_{MAX}, the inductor value required is:

$$L = \frac{(6 * 2.45 * 0.5)}{(10^5 * 0.6875)} = 107\mu H$$

The inductor current, which must remain continuous down to I_{MIN} during Fast-Charge phase 2 (voltage regulation phase), dictates the inductor formula for the Two-Step Voltage charge algorithm.

Equation 12

$$L = \frac{N * V_{BLK} * 0.5}{F_S * 2 * I_{MIN}}$$

Example: A 6-cell SLA battery is to be charged at I_{MAX} = 2.75A in a buck topology running at 100kHz. The V_{BLK} threshold is set at 2.45V per cell and the charger is configured for Two-Step Voltage mode, with I_{MIN} = $I_{MAX/20}$. The inductor value required is:

$$L = \frac{6 * 2.45 * 0.5}{(10^5 * 2 * 0.1375)} = 267\mu H$$

Model of a Lead Acid Battery

The battery impedance can be represented as a capacitor (C_B) in series with its internal impedance (R) as shown in Figure 12. The capacitance can be empirically derived from the amp-hour rating of the battery. The rule of thumb is:

$$C_B = 100 * C$$

where C = the capacity of the battery in ampere-hours.

The internal resistance Ri of a lead-acid battery is dictated by:

- Number of cells, N
- Amp-hour capacity, C
- State of charge

Figure 12 shows the variation of the internal impedance of a Yuasa NP6-12 (12V, 6 amp-hrs) battery as a function of its state of charge.

An average value of the impedance swing is recommended for use in loop stability equations. For example, with the battery above, R = 0.05Ω is recommended.

The resistor RO models the loading effects of the battery when a voltage equivalent to V_{BLK} (typically 2.45V/cell) is applied across the battery. The range of values RO takes on depends on the bulk charge current, the bulk voltage, and the I_{MIN} to I_{MAX} ratio. For example: A 12V

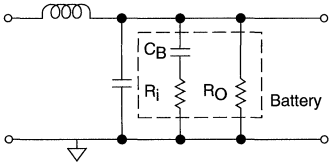


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Figure 11. Model of Output LC Filter for Buck Topology

battery being charged at I_{MAX} = 3A exhibits the following range with a I_{MIN}/I_{MAX} ratio of 1:20.

$$R_L(\min) = 6 * \frac{2.45}{3} = 4.9\Omega$$

$$R_L(\max) = 6 * \frac{2.45}{0.15} = 98\Omega$$

Use the minimum value for worst-case scenario of loop stability.

The Power Stage Transfer Function

The transfer function of the output power stage, $P_T(s)$ can be expressed as:

Equation 13

$$P_T(s) = \frac{V_{IN} * (1 + (s * R * C_B))}{(1 + (s / \omega_0)^2 + (s * (R_i C_B + {}^{L}/_{R_O})))}$$

where:

$$\omega_0 = 1 / \sqrt{L * C_B}$$

The poles and zeros of $P_T(s)$ are:

Equation 14

$$fzo = \frac{1}{(2\pi * R_i * C_B)}$$

$$fpo = 1 / (2\pi * \sqrt{L * C_B})$$

A second pole is not used in these calculations:

$$\frac{1}{2\pi * (R_i C_B + {}^{L}/_{R_O})}$$

Typical Switch-Mode Buck Charger Specifications

The application specifications for a switch-mode buck topology charger are usually given as :

- DC input voltage, V_{IN} = 20 to 30V
- Switching frequency, F_S = 100kHz, T = 10µs
- Charge algorithm = Two-Step Voltage mode:
  - V_{BLK} = 2.45V/cell , V_{FLT} = 2.2V/cell
  - I_{MAX} = 3A, I_{MIN} = I_{MAX}/30 = 300mA
- Battery specs: 12V, 10A-hr, Internal impedance: 0.02 to 0.07Ω

PWM and Output Power Stage Transfer Functions

Starting again from the basic voltage regulation loop-gain transfer function (Equation 3) is given as :

$$V_L(s) = A(s) * P_\omega(s) * P_T(s)$$

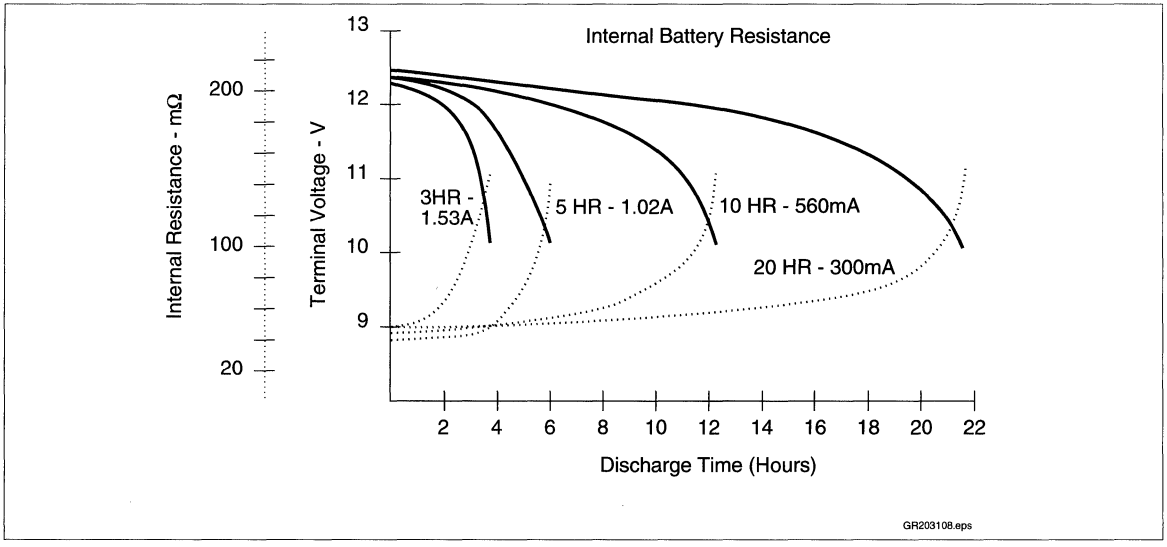


Figure 12. Internal Resistance of Yuasa NP6-12 Battery vs. State of Charge

12/16

This equation can be written as:

$$V_L(s) = A(s) * G(s)$$

where G(s) is the combined transfer function of $P_O(s)$ and $P_T(s)$

Combining Equations 4 and 13:

Equation 15

$$G(s) = \frac{0.47 * V_{IN} * (1 + (s * R * C_B))}{(1 + (s / \omega_0)^2 + (s * (R_i C_B + L/R_O)))}$$

Based on the typical values in the section above, the worst-case values for loop parameters are:

- $V_{IN} = 30$ V
- Ri = 0.05Ω
- $C_B = 100 * 10 = 1000\mu F$
- $R_O = 4.9\Omega$

From Equation 12:

$$L = \frac{(6 * 2.45 * 0.5)}{(10^5 * 2 * 0.1)} = 367.5\mu H$$

The resulting bode plots for G(s) are shown below.

Since the plots exhibit similar characteristics to that of the output power filter, Equation 14 can be used to determine the poles and zeros:

- fpo = 263Hz
- fzo = 3183Hz

Voltage Loop Error Amplifier Compensation

For this control loop, appropriate values must be found for R_V and C_V, the compensation components for the V_{COMP} pin. From Table 3 of "Using the bq2031 to Charge Lead-Acid Batteries," the values for the divider network components are:

- RB1=261K
- RB2=49.9K
- RB3= 475K

Therefore

$$D = \frac{(RB2 * RB3)}{(RB2 * RB3 + (RB1 * (RB2 + RB3)))} = 0.15$$

From the first criterion for loop stability, set the crossover frequency F_C (0 dB loop-gain) to 1/20th the switching frequency:

$$F_C = F_{S/20} = 5kHz$$

Set the two zeros of A(s), fz1 and fz2, at 1/2 to cancel the second-order poles of G(s) at fpo:

$$fz1 = fz2 = fpo/2 = 263/2 = 131.5 \text{ Hz}$$

From Equation 10's first zero, fz1:

$$C_F = \frac{1}{(2\pi * RB1 * fz1)} = \frac{1}{(2\pi * 2.61 * 10^5 * 131)} = 4.63nF$$

From Equation 9's second pole, fp2:

$$fp2 = 865 \text{ Hz}$$

To achieve 0 dB loop-gain at F_C, the compensated amplifier gain at fp2 must be forced to the absolute gain of G(s) at the crossover frequency, which can be determined from the Bode plot in Figure 13 to be -31dB = 35.48.

The value for R_V can be determined from the gain magnitude equation for A(s) at fp2

$$A(f_{p2}) = \frac{105 * D * R_V}{2.5 * 10^5 * R_V}$$

Using the value of 35.48 for A(fp2) in the above equation gives:

$$R_V = \frac{35.48 * 2.5 * 10^5}{35.48 - 15.75} = 450k\Omega$$

Plugging this value for R_V into equation 10 for fz2 yields:

$$C_V = \frac{1}{2\pi * 450 * 10^3 * 131} = 2.7nF$$

Substituting these values for R_V and C_V in equation 10 for fp2 gives:

$$fp2 = \frac{1}{2\pi * (450k\Omega + (2.5 * 10^5)) * 2.7nF} = 84.2Hz$$

Figures 14 and 15 show the resultant Bode and loop gain plots for A(s), respectively.

Current Loop Error Amplifier Compensation

For this control loop, the value must be found for C_i, the compensation component for the I_{COMP} pin. The compensation network component C_i must be chosen such that the current loop gain transfer function has a dominant pole at 1/20th of the switching frequency, F(s).

$$\frac{1}{2\pi * (2.5 * 10^5) * C_i} = 131.5$$

$$C_i = \frac{1}{2\pi * (2.5 * 10^5) * 131.5} = 4.84nF$$

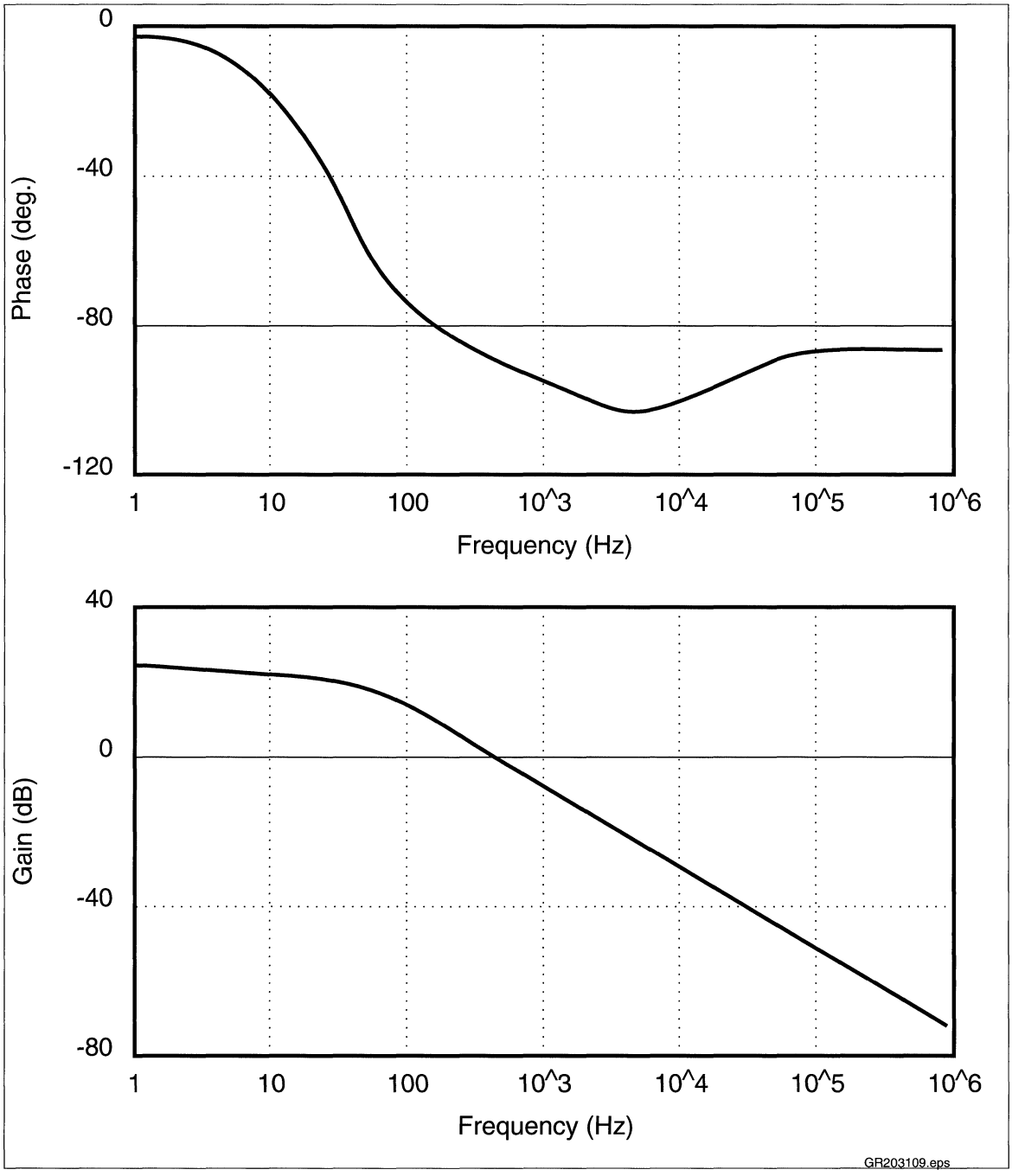


Figure 13. Bode Plot for G(s)

14/16

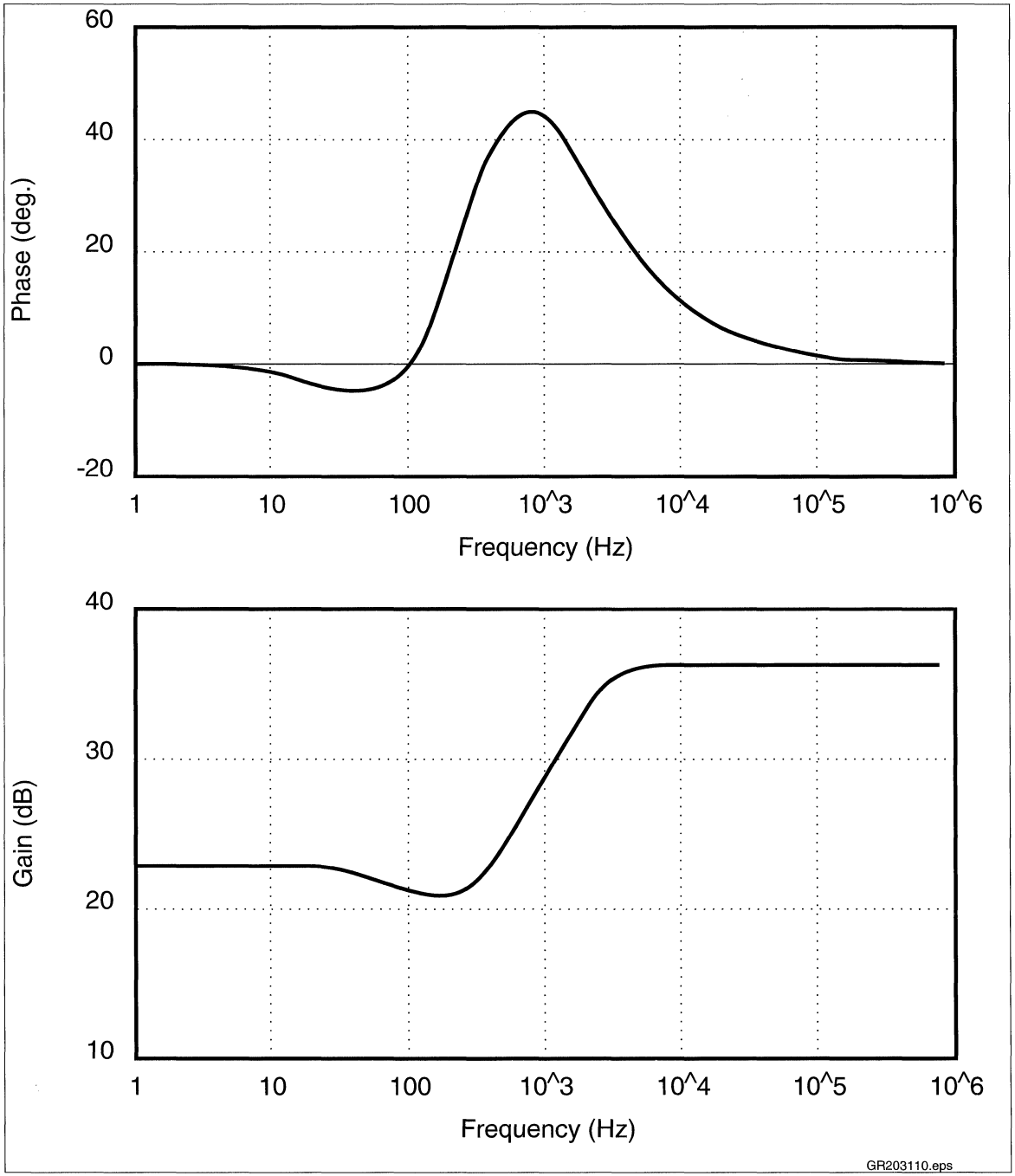


Figure 14. Bode Plot for Error Amplifier, A(s)

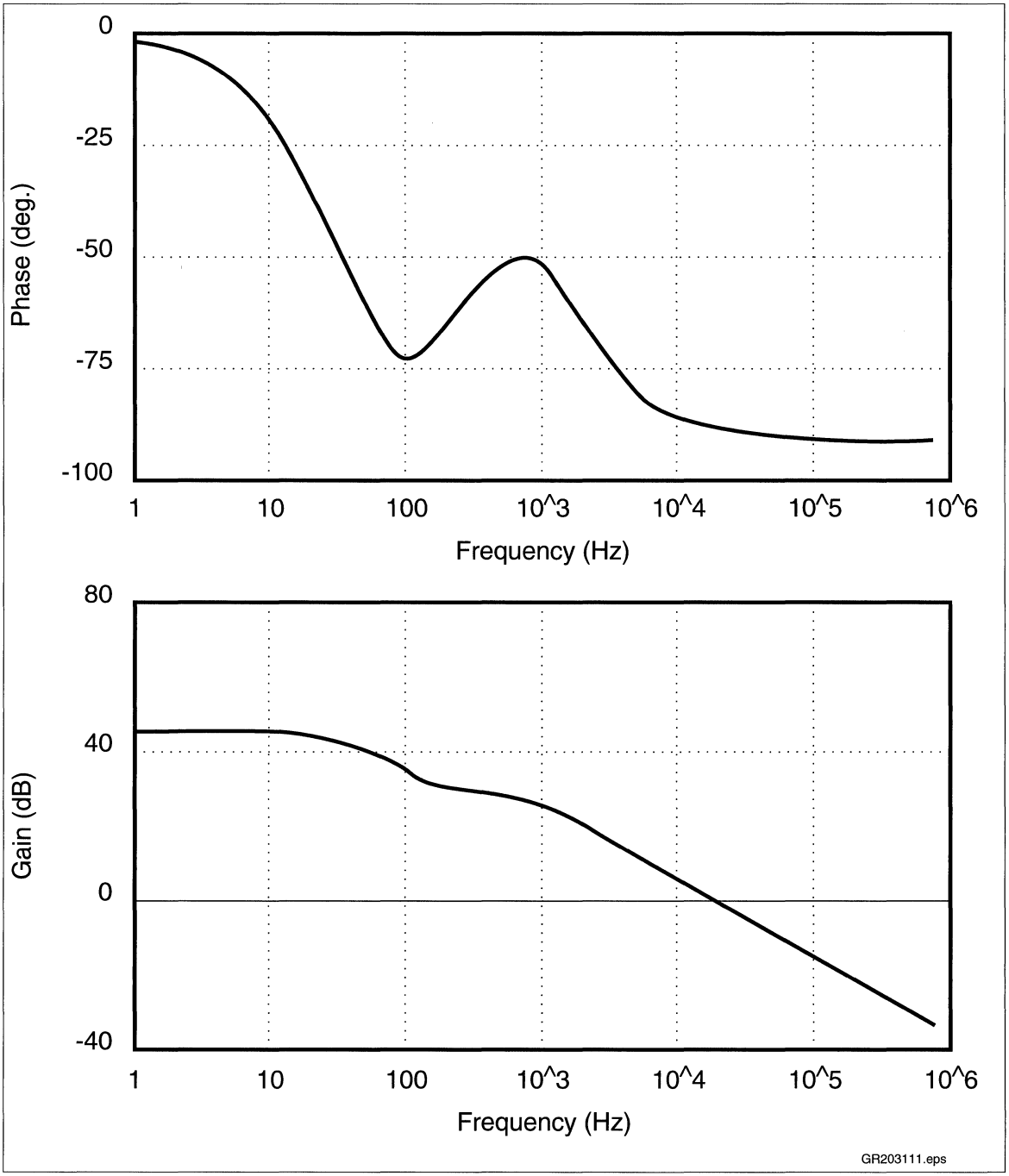


Figure 15. Loop Gain Bode/Example Buck Charger Design

16/16

UNITRODE

U-512 Using the bq2902/3

Rechargeable Alkaline ICs

Introduction

Choosing the right battery chemistry for a particular application depends on many factors. In some cases, the appropriate choice is rechargeable alkalines, which have advantages over other secondary battery chemistries, such as NiCd or NiMH:

- Much lower self-discharge rate
- Increased capacity
- Increased energy density
- Low cell cost and good availability

For low to moderate power levels (AA or AAA cells at 20–400mA loads), these advantages are exploited in applications which include portable audio, handheld instruments, palmtop computers, calculators, personal communication devices, electronic games, personal care products, and others.

The internal resistance of alkalines, however, is higher than that of the spirally wound NiCd or NiMH systems. As a result, alkaline cells provide lower effective capacity at higher discharge currents.

The bq2902 and bq2903 ICs manage rechargeable alkalines such as the Renewal® cells from Rayovac®. These ICs monitor the charge and discharge cycles of rechargeable alkalines to extend their cycle life. The bq2902 manages two cells, and the bq2903 manages either three or four cells.

These parts feature the following:

- LED driver output(s) to indicate charge status
- Selectable end-of-discharge voltage (EDV) to prevent overdischarge and to improve cycle life
- Optional external FET drive, allowing higher current loads (bq2903 only)
- Pulsed current taper

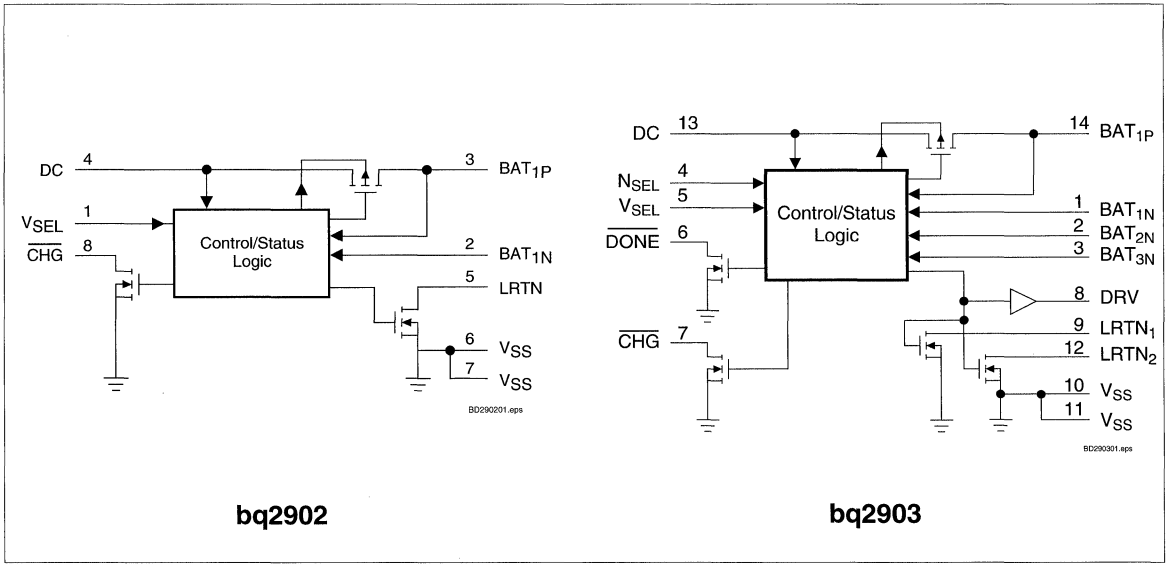


Figure 1. Functional Block Diagrams

Contents

This application note discusses these key points about the bq2902/3:

- Functional Description
- Charge Control
- Discharge Control
- Practical Considerations

For complete device specification, please refer to the bq2902 or bq2903 data sheet.

Functional Description

The bq2902 and bq2903 function similarly. There are certain differences between the two ICs, however, as indicated in Table 1.

Table 1. bq2902/3 Differences

Feature	bq2902	bq2903
Number of monitored cells	2	3 or 4
V_{OP} (Max)	5.5V	10V
Status outputs	1	2
External FET drive (DRV pin)	No	Yes

The DRV pin on the bq2903 controls an external N-FET for use when discharge currents are in excess of 400mA. (See the functional descriptions in the bq2902 and bq2903 data sheets.) Figure 1 shows the bq2903 functional block diagram; note that the DRV pin is present in that diagram. The bq2902 does not provide a DRV pin for external discharge FET control.

Charging

The bq2902/3 charges cells in series; therefore, it is not recommended for use in stand-alone chargers where anywhere from one to four cells are charged.

A load should not be connected to the battery during charge because the bq2902/3 requires an accurate measurement of the no-load battery voltage (i.e., open-circuit voltage) to terminate charge properly. See the "Powering the Load While Charging" section of this application note. The open-circuit voltage (V_{OCV}) of each cell is monitored during the idle period, as seen in Figure 2.

During the OCV test, if any cell is above 1.63V, then the following charge pulse is skipped. The bq2903 terminates charge when a cell remains above 1.63V long enough for 16 consecutive pulses to be skipped. The effective charging current equals approximately 6% of the fast charge rate. The bq2902 terminates charge when 32 consecutive pulses are skipped. This effective charging current equals approximately 3% of the fast charge rate. These algorithms effectively taper the charging current until termination occurs. Charge termination can be indicated using an LED .

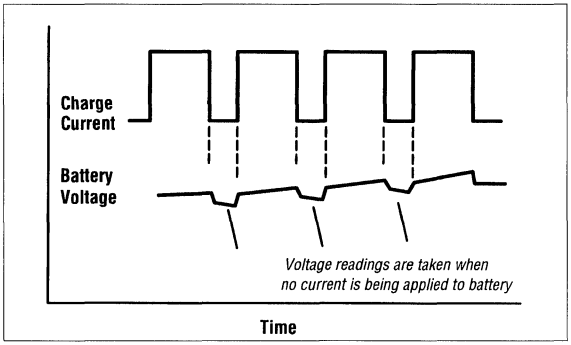


Figure 2. Cell Voltage/Current During Charging

Charging Source

The charging supply must limit the current through the DC pin to less than 300mA to prevent excessive power dissipation in the internal charge switch. The charging supply must provide at least 2.0V*N (where N is number of cells) to charge the battery properly. The bq2902/3 controls charging by periodically connecting the current source to the battery stack through the BAT_{IP} pin. The compliance voltage of the current source should also be limited to prevent the DC pin from exceeding its rated operating voltage (V_{OP} max.) when the charge switch is "off."

The charging current can be extended to above 300mA, as discussed in the "Constant-Current Charging: >300mA" section of this application note. At higher charging currents, the cell voltage takes longer to recover, thus skipping more charging pulses and terminating charge earlier. A few percentage points in capacity can be gained by limiting the charging source to below 300mA, but the trade-off is a longer charge time. By testing charge times in your application, you can determine these trade-offs.

Charge Control

Low-Current Charging: ≈ 100mA

A low charge rate of 100mA or less may be acceptable in some applications such as electric toothbrushes, cordless phones, and flashlights. Quasi-constant-current charging can be cost-effective for these applications. (See Figure 3.)

The charge current is limited by an inexpensive resistor, R5, or by the secondary winding resistance of an AC-DC wall-mount adapter. The charge current into the DC pin now varies with the battery's state of charge and input voltage. As the battery charges and the voltage rise, the peak current into the DC pin decreases with the decreasing voltage drop across R5. Low efficiency limits the suitability of this design to low-rate charging.

Design example:

Given: V_{IN} =12V, I_{CHG}(min) ≈ 100mA

Find: R5 for the charger in Figure 3

Solution:

$$R5 = (12V - 3 \text{ cells} * 2V/\text{cell})/100mA = 60\Omega.$$

Choose a standard resistance value: R5 = 56Ω

Verify that the charge current is under 300mA if the per cell voltage is 0.4V:

$$I = (12V - 3 \text{ cells} * 0.4V/\text{cell})/56\Omega = 193 \text{ mA}$$

The maximum power dissipation in R5 is

$$Pd(R5) = 0.75 * 56\Omega * (193mA)2 = 1.56W.$$

The maximum power dissipation of D4 is

$$Pd(D4) = (12V - 10V)/56\Omega * 10V = 375mW$$

The charge current varies between 107mA and 193mA, depending on the battery's state of charge.

In most instances, the cell voltage does not go below the minimum EDV cutoff voltage of 0.9V. In these cases, the value of R5 can be increased and its power rating decreased accordingly.

R2, R3, and C1-C3 are for ESD and latch-up protection. Q1 and D3 allow the load to operate from the charging supply or from the battery. The operation of this circuit is discussed in greater depth in "Powering the Load While Charging."

Constant Current Charging: ≤ 300mA

The circuit in Figure 4 can charge up to a 300mA rate. The front end (Q1, Q2, Q3, R2, R3, R4, R8, and R_{SNS}) is a constant-current source with output voltage limiting. The charge current and output voltage limits are set as follows:

Charge current: $I_{CHG} \approx 0.65V/R_{SNS}$

V_{OUT} limit: $R3/R4 \approx (V_O/0.65V-1)$

The output voltage limit is set at 9.1V, providing enough voltage to charge 4 cells. I_{CHG} is set at 295mA.

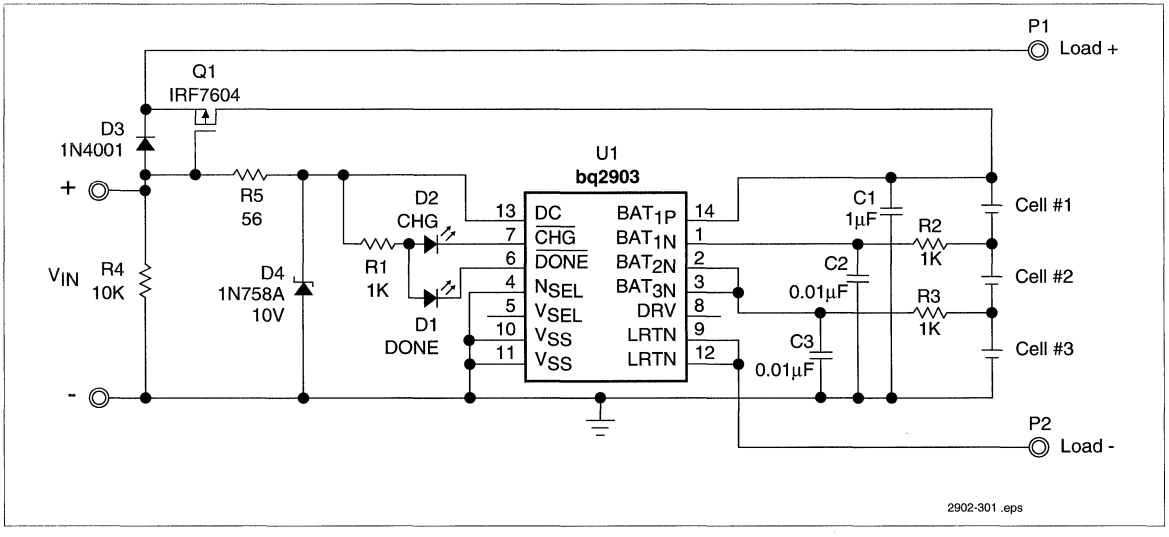


Figure 3. Low-Cost Quasi-Constant-Current Charger

The maximum power dissipated by Q1 is

$$Pd(Q1) = (16V - 0.4V/cell * 4 cells) * 300mA * 75\%$$

or

$$Pd(Q1) = 3.24W$$

This calculation assumes an unregulated power supply with an output voltage of 10V–16V. The power dissipated by Q1 reduces to 1.89W if the power supply is regulated to 10V.

D4 ensures that the bq2902/3 can change from the charge to discharge mode if the charging supply is turned off. This mode change is triggered by the DC pin falling 155mV below the voltage at BAT_{1P}. If the capacitance at the current source input is too large and D4 is absent (i.e., replaced with a short), the bq2902/3 gets stuck in the charge mode. A large capacitance can appear at the current source input if the charger is connected to an adapter that is unplugged from the outlet. A typical adapter has a large filter capacitor across its output (e.g., 1000µF). To understand how the bq2902/3 can get stuck in the charge mode, consider the sequence of events that occur after the charging supply is turned off. Remember, the bq2902/3 is initially in the charge mode, so its internal charge switch is pulsing at a 75% duty cycle.

The sequence of events is as follows:

1. Turn off the charging supply.
2. The voltage at the DC pin falls until it is equal to the voltage at BAT_{1P}.
3. The charge switch is closed. The voltage at the DC pin is forced to the voltage at BAT_{1P}.
4. The charge switch is open. The voltage at the DC pin falls below the voltage at BAT_{1P}. The rate of decay is determined by the capacitance at the current source input
5. If the capacitance is large, the voltage at the DC pin does not fall 155mV below the voltage at BAT_{1P} while the switch is opened. The bq2902/3 remains in the charge mode and the charge switch closes again.
6. The charge switch is closed. The capacitor is connected across the battery through Q1 (Q1 turns on because of its non-zero reverse β). The capacitor is charged to the voltage at BAT_{1P}.
7. The cycle repeats at step 4.

In summary, D4 behaves as a one-way valve. It allows the input capacitor to discharge, but prevents it from being charged by the battery. The capacitor voltage eventually decays and the bq2902/3 exits the charge mode. D4 can be omitted if the capacitor across the current source is small enough to allow the charger to function properly.

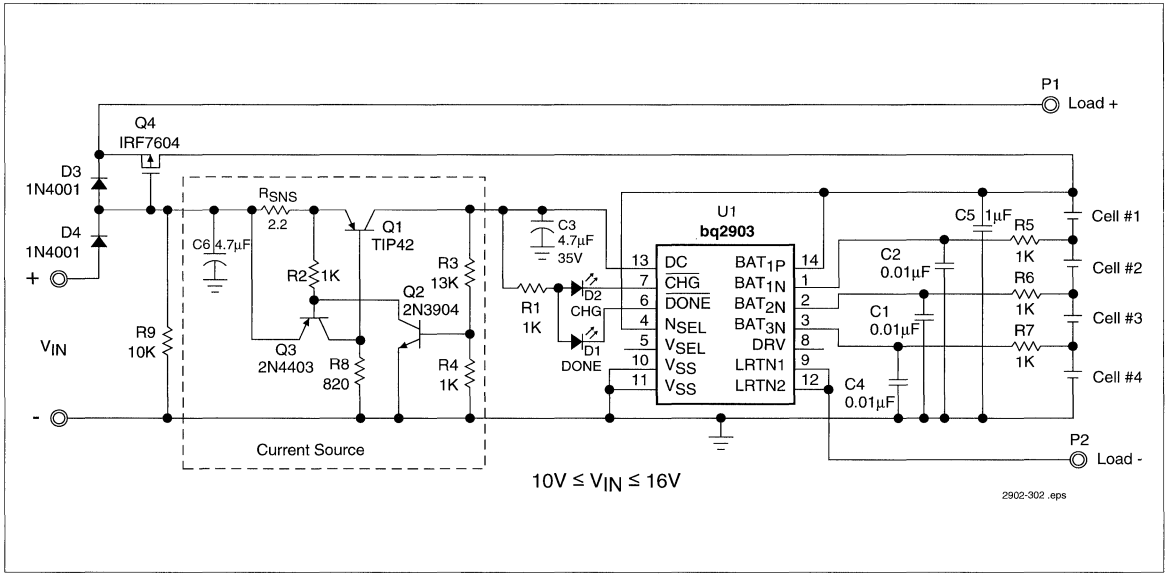


Figure 4. 300mA Linear Charger

Constant-Current Charging: >300mA

There are times when charging at greater than 300mA is desirable—for example, when charging either C or D size cells. The bq2902/3 can carry a maximum charge current of 300mA; however, the bq2902/3 can be used to control rather than carry the charge current. This charge method is used in Figures 5 and 6.

As a point of reference, the table below outlines the maximum recommended pulse charge current for Renewal cells.

Table 2. Maximum Pulse Current for Renewal Cells

Cell	Peak Current (mA)
AAA	300
AA	700
C	1500
D	1500

The circuit in Figure 5 can fast charge C or D cells. The current source (Q1, Q2, Q4, Q6, R_{SNS}, R3, R6, R8, and R9) turns on when the bq2903 gates current into the battery. Less than 1% of the charge current flows through the bq2903. The bulk of the charge current flows directly from the current source to the battery.

D5 prevents the DC pin from exceeding its maximum rated voltage. D4 prevents the battery from being discharged by the current source. Q3 is in parallel with the internal discharge FET to reduce the effective resistance of the discharge path.

A self-oscillating switch-mode current source can be used instead of a linear current source to reduce power dissipation, as shown in Figure 6. Power conversion efficiency is typically 75% for the former and 40% for the latter. In Figure 6, the loop area formed by C5, R_{SNS}, Q2, D4, and D6 should be small to minimize RF emissions.

The peak charge current for the linear or switch-mode current source is set by R_{SNS}:

$$I_{CHG} \approx 0.65/R_{SNS}$$

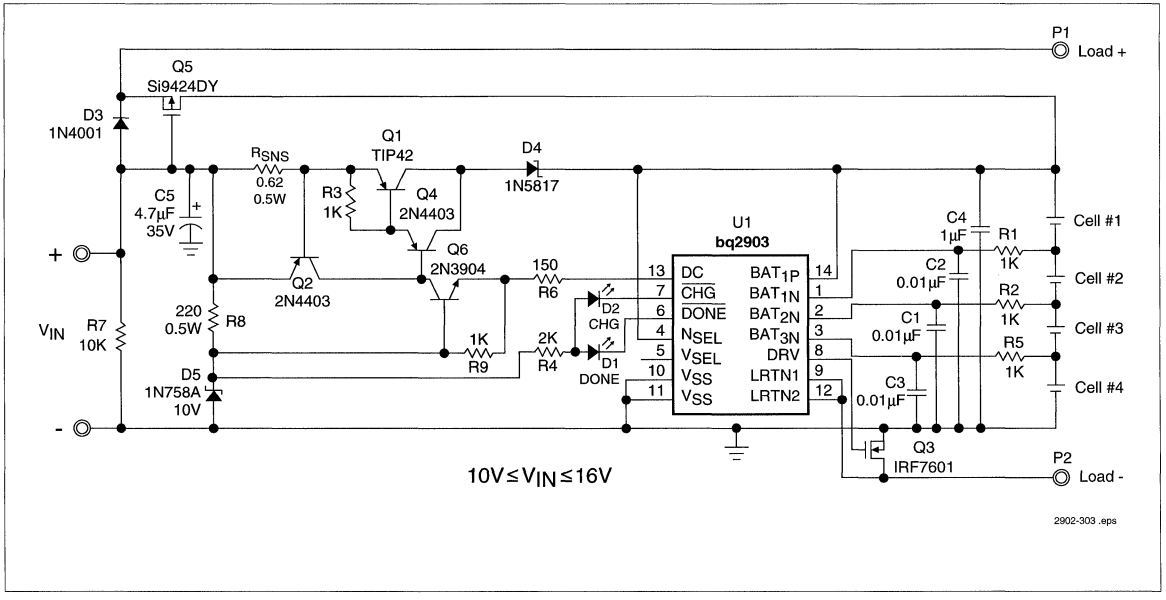


Figure 5. One-Amp Linear Charger

Discharge Control

EDV Selection

The most important causes of capacity fade are over-discharge and the number of discharge cycles. The depth of discharge (DOD) is determined by the rate of discharge and the end-of-discharge voltage (EDV).

The DOD to a given EDV is affected by the internal resistance of rechargeable alkalines. (See Figure 8.) Internal resistance increases with storage time and use. At low discharge rates, the voltage drop across this resistance is low, allowing for a greater DOD than at higher rates. This DOD causes a higher degree of capacity fade at low discharge currents. High discharge rates create a higher voltage drop across the battery's internal resistance, thus allowing a lower EDV with less effect on cycle life.

The bq2902/3 uses a low-side switch connected between LRTN and V_{SS}, as seen in Figure 1, to disconnect the load from the battery when a cell falls below the user selected EDV. EDV can be configured to be 1.1V, 1.0V, or 0.9V, as shown in Table 3.

Table 3. Configuring for Selectable End-of-Discharge Voltage (V_{EDV})

V_{SEL}	V_{EDV}
BAT_{1P}	1.1V
Floating	1.0V
V_{SS}	0.9V

The EDV cutoff function is active only if the bq2902/3 is in the discharge mode (V_{DC}< V_{BAT1P}). If the bq2902/3 is in the charge mode (V_{DC} >V_{BAT1P}), the EDV cutoff function is disabled, and the discharge switch stays "on."

Again, the discharge current, the battery's internal resistance, and the end-of-discharge voltage together determine the depth of discharge. Table 4 suggests some EDV values for various cell sizes and rates of discharge to help maximize cumulative discharge capacity.

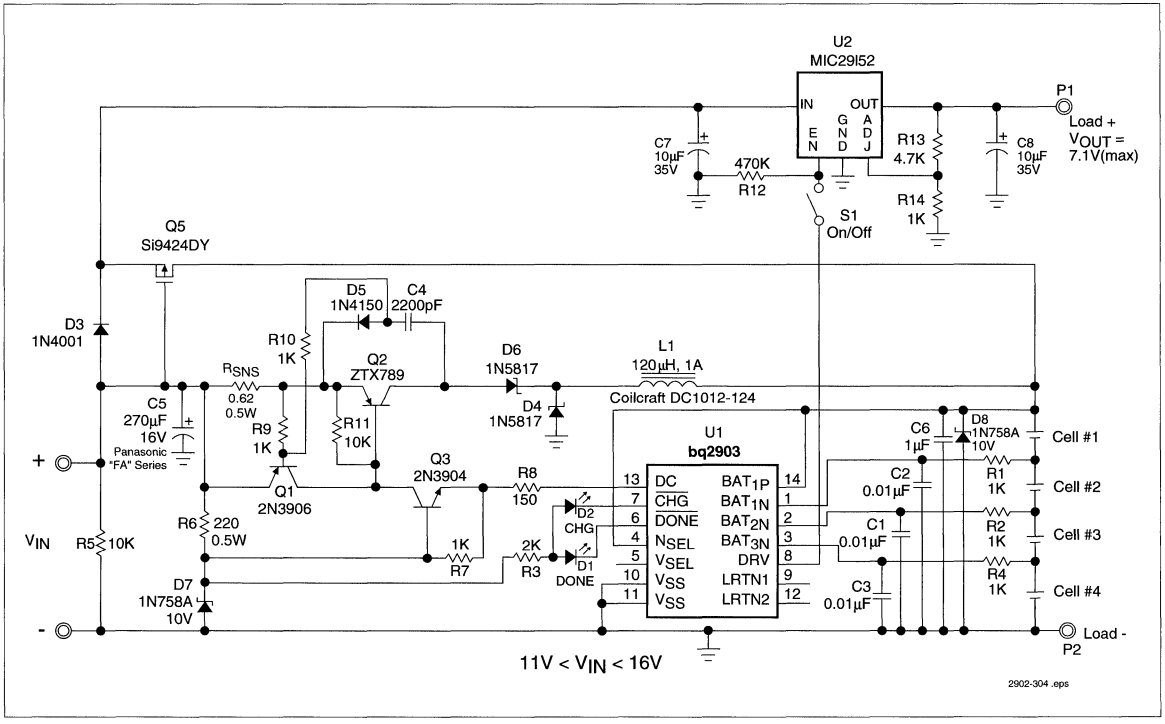


Figure 6. One-Amp Switch-Mode Charger Using an LDO for a Voltage Clamp and High-Side Load Switch

Table 4. Suggested EDV for Various Discharge Rates

V_{EDV}	AAA	AA	C	D
1.1V	20mA	50mA	100mA	100mA
1.0V	50mA	100mA	200mA	200mA
0.9V	>100mA	>200mA	>300mA	>300mA

These voltages may differ depending on the use of the cells in the actual application.

Low-Side Switch

Either the bq2902 or bq2903 can sink 400mA of load current with its internal FET. Current handling can be augmented by paralleling the internal FET with an external FET (Q3) as shown in Figure 5. Only the bq2903, however, has the DRV pin available to drive the gate of the external FET.

High-Side Switch

A high-side load switch can be used if the load and battery must share the same return. The switch is implemented with a P-channel MOSFET (Q5) as illustrated in Figure 7. The current through the LRTN pull-up resistor should be comparable to the battery's leakage current to minimize battery drain during in-system storage.

The leakage current is determined from the self discharge rate of a rechargeable alkaline which is typically 0.01% per day. For example, the leakage current of a 1.4Ahr capacity AA-cell is

$$I = 0.01\% * (1.4Ahr/24hr) = 5.8\mu A$$

Discharge Switch Selection

The external discharge FET must have enough threshold voltage to stay "on" throughout discharge. The number of cells and the EDV setting determine the maximum threshold voltage. For example, an application using 3 cells and an EDV of 0.9V (±5%) requires a FET with a threshold of less than 2.57V.

Table 5 lists FETs that work equally well in 3- or 4-cell applications.

In addition to the threshold voltage constraint, the external discharge FET's on-resistance, or R_{DS} (on), should be low relative to the battery pack's internal resistance. Typical cell resistances at room temperature are 0.3Ω for a AAA-cell, 0.2Ω for a AA-cell, 0.15Ω for a C-cell, and 0.1Ω for a D-cell. Stacking cells in series increases the pack resistance while paralleling cells decreases the pack resistance.

Figure 8 shows a graph of a typical cell's resistance for AA- and D-cell size versus temperature.

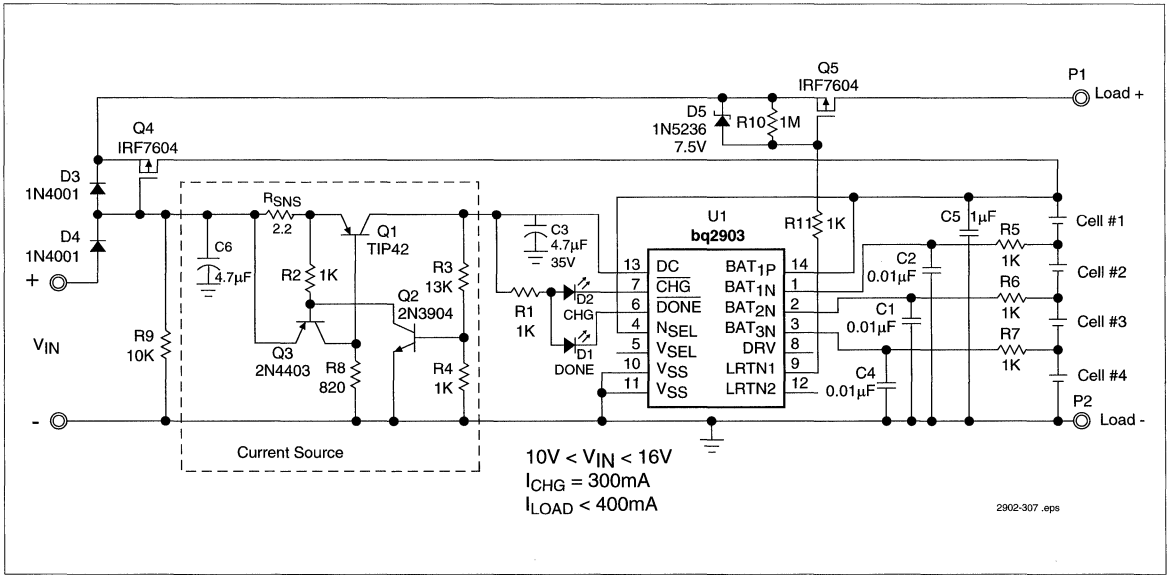


Figure 7. Discharge Control With High-Side Load Switch

7/12

Table 5. Switches for 3- and 4-cell Applications

External FET	Maximum $R_{DS(on)}$	Package	Manufacturer
Low-Side Switch (N-FETs)			
TN0200T	0.5Ω	SOT-23	Siliconix
IRLML2402	0.35Ω	SOT23	IR
Si6946DQ	0.11Ω	TSSOP-8	Siliconix
IRF7601	0.05Ω	Micro-8	IR
Si6426DQ	0.040	TSSOP-8	Siliconix
IRF7401	0.03Ω	SO-8	IR
Si9426DY	0.016Ω	SO-8	Siliconix
High-Side Switch (P-FETs)			
IRLML6302	0.9Ω	Micro-3	IR
TP0101T	0.85Ω	SOT-23	Siliconix
Si6943DQ	0.18Ω	TSSOP-8	Siliconix
Si6433DQ	0.09Ω	TSSOP-8	Siliconix
Si9434DY	0.060	SO-8	Siliconix
IRF7404	0.06Ω	SO-8	IR
Si9424DY	0.033Ω	SO-8	Siliconix
IRF7604	0.013	Micro-8	IR

Powering the Load While Charging

The bq2902/3 requires that the load be disconnected from the battery while the cells are charging to

- Prevent the battery from discharging to 0V if the load current exceeds the effective charge current (the discharge switch stays "on" when the bq2902/3 is in the charge mode)
- Allow the bq2902/3 to accurately measure a cell's open circuit voltage for proper charge termination
- Ensure the battery is at full capacity when the "charge complete" LED is "on"
- Maximize battery life by reducing the number of charge/discharge cycles (the battery cycles between charge and discharge if the battery is lightly loaded)
- Prevent the battery's ripple voltage from interfering with operation of the load

What if the load must operate while the battery is charging? Such operation may be desirable or even necessary for certain applications such as tape recorders, radios, electronic organs, portable computers, and cordless phones. In this case, the charger's power supply

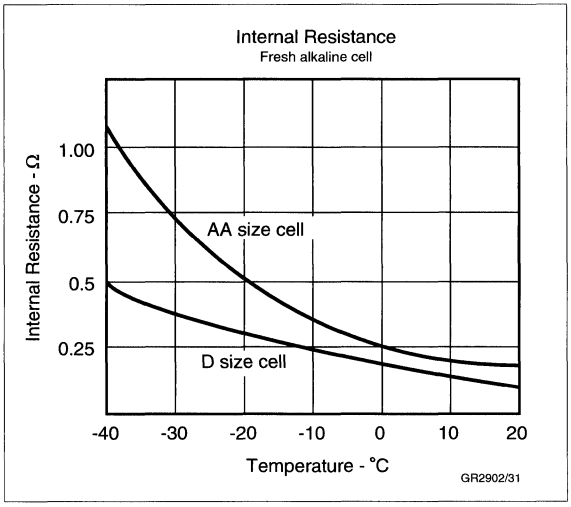


Figure 8. Typical Cells Resistance vs. Temperature

powers the load when the battery is charging; the battery powers the load when the battery is not charging.

A crude way to enable the load to be powered by either the battery or the charger is to wire-OR the power supply and battery to the load with rectifiers. This solution may be simple, but it is inefficient because the rectifiers' voltage drop reduces the available operating time.

To improve efficiency, the rectifier between the battery and the load is replaced with a P-channel MOSFET, Q4, as shown in Figure 4. When the charger's power supply is on, D3 conducts, turning off Q4. The load disconnects from the battery and connects to the charger's power supply. When the power supply output is off, the battery initially powers the load through the body diode of Q4. The voltage drop across the body diode is rather high (Vf ≈ 1V). As C6 discharges, the gate of Q4 is pulled to ground turning on Q4. Q4 shorts out the body diode, reducing the voltage drop between the battery and the load.

In some cases, the power supply's output voltage can be significantly higher than the battery voltage. In Figure 4, the power supply voltage can be as high as 16V and the battery voltage can be as low as 4V. Many loads cannot tolerate this voltage swing. These loads may require either a voltage regulator or a voltage clamp to limit the excursion. A low drop-out regulator (LDO), U2 in Figure 6, limits the load voltage to 7.1V. The LDO operates in the linear region when the power supply is on and can dissipate significant power at moderate load currents. Efficiency is of little consequence when operating from external power because run-time is not affected, as it is when operating from a battery.

8/12

When the power supply is off, the LDO saturates, becoming a switch, since the battery voltage is less than the regulation voltage. The voltage drop across the MIC29152 LDO is 350mV (typ) at a 1.5A load. The low loss connection between the battery and load maximizes operating time. The bq2903 turns the LDO off when EDV is reached. Here the discharge FET is not used.

Adapting the circuit in Figure 6 to 2 cells (i.e., with the bq2902) is difficult because present LDOs and MOSFETs do not work well with the lower voltage from 2 cells. This situation should change as manufacturers respond to the proliferation of 2-cell applications.

Practical Considerations

Cell Matching

Replace all cells as a set. Battery performance is optimal when cells are matched for capacity and state of charge. Cells with different charge and discharge histories suffer from different degrees of capacity fade.

Battery Interchangeability

In some cases, the use of both rechargeable and primary alkalines in an application may be desirable. If so, it is especially important not to allow the primary alkalines to be charged, because charging could cause the primary battery to leak or explode.

Rayovac has developed a special charger contact for AA and AAA Renewal cells that can be used to detect if a Renewal cell is placed into a holder. (See Figure 9.)

Renewal cells have a unique exposed anode shoulder with which the contact can make a connection. For primary alkalines, the insulating outer layer covers up the shoulder, not allowing a connection to be made to the contact. This recharge contact allows primary alkalines to be used in place of rechargeable alkalines. A schematic showing how to implement a circuit using this contact is shown in Figure 10.

If a primary alkaline cell is placed into the holder, it cannot be recharged because the current source is disabled; the current source is enabled only if the special recharge contact is in electrical contact with the battery's anode. Thus the bq2902/3 is prevented from charging, but it still disconnects the load from the battery when EDV is reached.

The contacts in Figure 9 may be obtained from

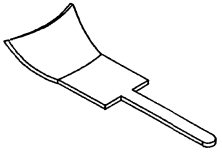
Memory Protection Devices
320 Broadhollow Road
Farmingdale, NY 11735
(516) 293-5891

For C and D size cells, the Renewal cells have a smaller diameter nubbin, allowing the nubbin to pass through a hole only large enough for Renewal cells. For more information on special contact systems for Renewal cells, please contact Rayovac.

Power-up Initialization

Power-on reset begins when BAT1P rises above 1.4V. During reset, the bq2902/3 turns on its discharge FET, checks the cells for EDV, and turns off the discharge FET if EDV is detected. The bq2902/3 must reset after the last cell is installed to initialize properly. ESD protection diodes at BAT_{1N}–BAT_{3N} allow the bq2902/3 to power up with a missing cell, however, causing reset to occur prematurely. The discharge FET initializes off

Contact	Part Number
Negative	SN-T5-1
Recharge	ABG-147
Positive	SN-T5-2



Recharge contact

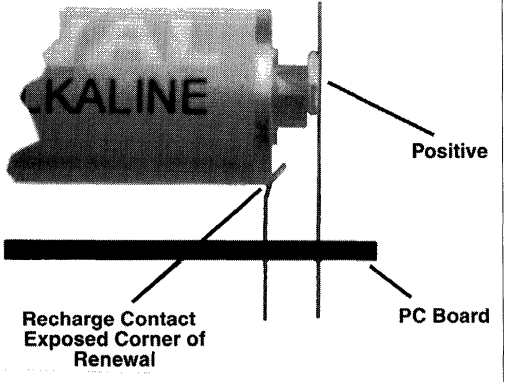


Figure 9. Charging Contacts for AA and AAA Cells

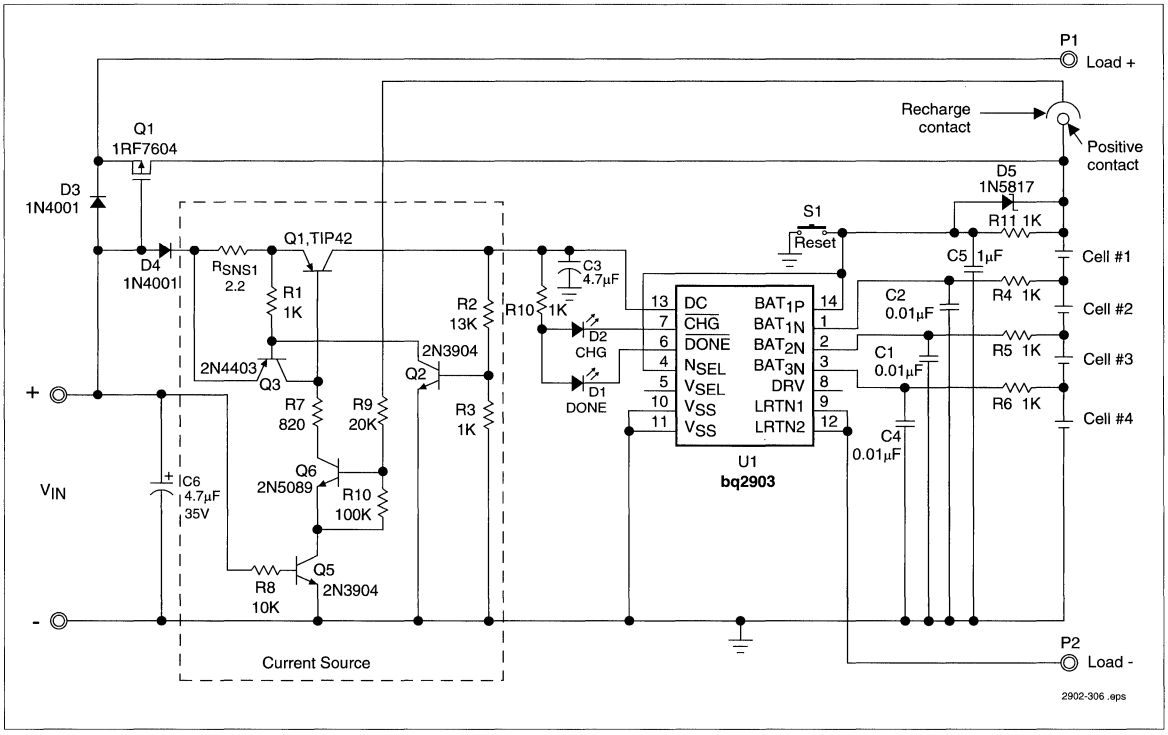


Figure 10. Using Rayovac Contacts to Permit Only Renewal Cells to Charge

(i.e., EDV is detected) by the time the missing cell is inserted. The discharge FET is reset by charging the battery, but if a wall outlet is not available or if primary alkalines are used (i.e., charging is disabled), the FET must be reset in another way.

Manual Reset

S1 in Figure 10 allows manual initialization of the discharge FET. By grounding BAT_{1P} (removing power to the bq2903) and then reapplying power (letting up on switch S1), the bq2903 initializes with the discharge FET on. S1 must be depressed long enough to discharge the capacitors at BAT_{1N}–NAT_{3N}. These capacitors discharge through the bq2902/3's internal ESD protection diodes. D5 allows S1 to be depressed without shorting the battery while maintaining a low-impedance charging path to the battery. The bq2902/3 measures the battery's open-circuit voltage through R11; D5 is off during this interval.

Automatic Reset

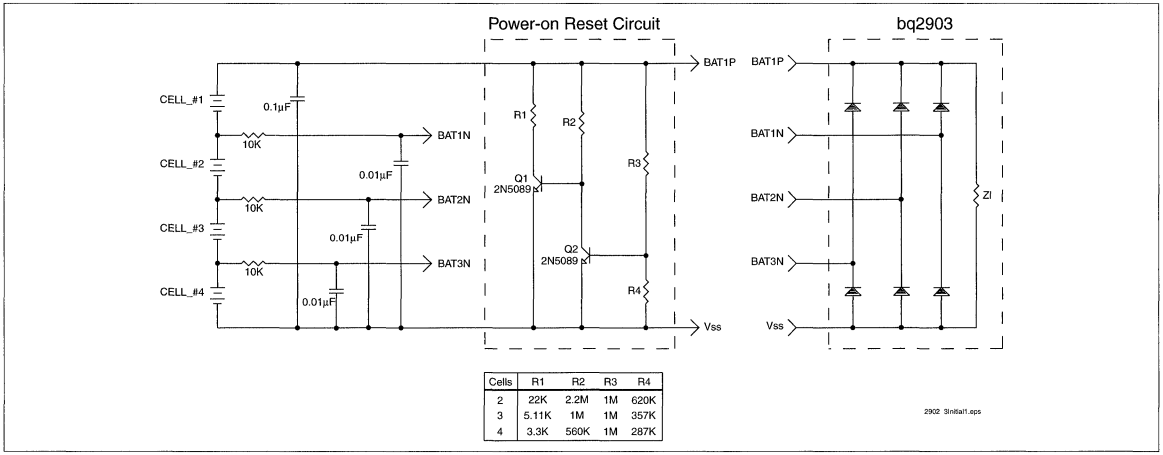
Q1 in Figure 11 holds the voltage at BAT_{1P} below the 1.4V reset threshold until the last cell is inserted. The last cell forces the voltage at BAT_{1P} above 1.4V to initiate the reset cycle. Note that the input current-limiting resistors at BAT_{1N}–BAT_{3N} are 10kΩ.

ESD and Latch-up

The battery contacts are subject to ESD during battery installation. These contacts are connected to the BAT_{1P}, BAT_{1N}, BAT_{2N},and BAT_{3N} pins of the bq2902/3. Bypass capacitors from these pins to V_{SS} are recommended for ESD protection. Latch-up can occur if these contacts are subjected to excessive ESD. Series resistors at these inputs limit the current so that latch-up cannot be sustained.

Reverse Battery Insertion

Excessive current through BAT_{1P} and V_{SS} damages the bq2902/3 if cells are inserted backwards. Figure 12 shows several ways to protect the bq2902/3 from cell reversal. The MOSFET in Figures 12a and 12b turns on only when the cells are correctly inserted.



Cells	R1	R2	R3	R4
2	22K	2.2M	1M	620K
3	5.11K	1M	1M	357K
4	3.3K	560K	1M	287K

Figure 11. Automatic Power-Up Iniatilization

Battery Storage

Cells may be stored in the system (i.e., making connection to the bq2902/3) only if all cells are present. A missing cell can turn on parasitic structures in the IC that can discharge the battery. The discharge rate is limited by external resistors in series with BAT_{1N-3N}.

EMI

Twist + and – leads of the cell stack to reduce EMI.

References

[1] Upal Sengupta, "Real World Aspects of Smart Battery Management," Proceedings of the Third Annual Portable by Design Conference 1996, pp. 299–305.

[2] Rayovac 1996–1997 OEM Designer's Guide and Technical Data.

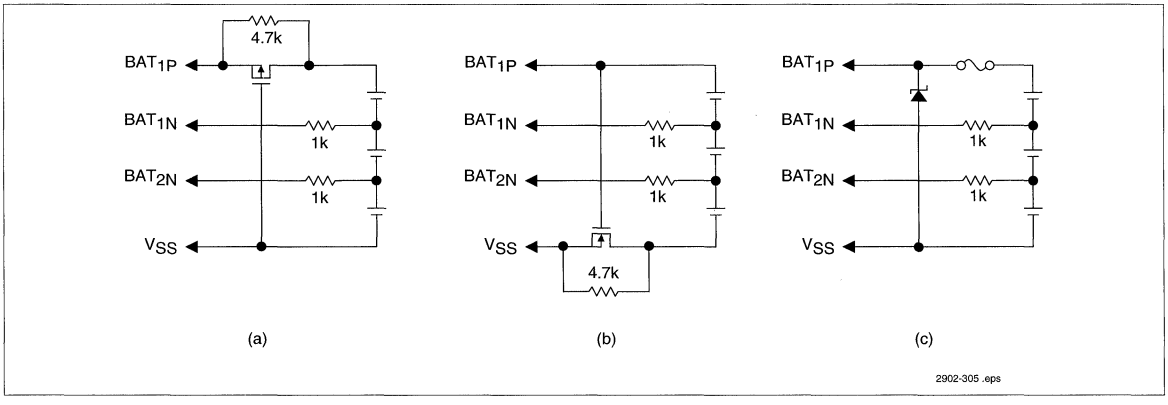


Figure 12. Protecting the bq2902/3 Against Reverse Battery Insertion

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	2	Table 1	Clarified table
1	3, 4, 5, 6, 7, 10	Schematic	Updated schematic.

Notes: Change 1 = May 1999 B changes from Oct. 1997.

UNITRODE
APPLICATION NOTE

IMPROVED CHARGING METHODS FOR LEAD-ACID BATTERIES USING THE UC3906

ABSTRACT

This paper describes the operation and application of the UC3906 Sealed Lead-Acid Battery Charger. This IC provides reductions in the cost and design effort of implementing optimal charge and hold cycles for lead-acid batteries. Described are the design and operation of several charging circuits using this IC. The charger designs use current and voltage sensing combined with sequenced current and voltage control to maximize battery capacity and life for various applications. The presented material provides insight into expected improvements in battery performance with respect to these specific charging methods. Also presented are uses of the many auxiliary functions included on this part. The unique combination of features on this control IC has made it practical to create charge and hold cycles that truly get the most out of a battery.

AN IC FOR CHARGING LEAD-ACID BATTERIES

Battery technology has come a long way in recent years. Driven by the reduction of size and power requirements of processing functions, batteries now are used to provide portability and failsafe protection to a new generation of electronic systems. Although a number of battery technologies have evolved, the lead-acid cell remains the workhorse of the industry due to its combination of prolonged standby and cycle life with a high energy storage capacity. The makers of uninterruptible power supplies, portable equipment, and any system that requires failsafe protection are taking advantage of the improvements in this technology to provide secondary power sources to their products, for example, the sealed cell, using a trapped or gelled electrolyte, has eliminated the positional sensitivity and greatly reduced the dehydration problem.

The charging methods used to replenish or maintain the charge on a lead-acid battery have a significant effect on the performance of the cells. Building an optimum charger, one that gets the most out of a battery, is not a trivial task. Making sure that a battery undergoes the proper charge and hold cycle requires precision sensing and control of both voltage and current, logic to sequence the charger through its cycle, and temperature corrections — added to the charger's control and sensing circuits — to allow proper charging at any temperature. In the past this has required a significant number of components, and a substantial design effort as well. The UC3906 Sealed Lead-

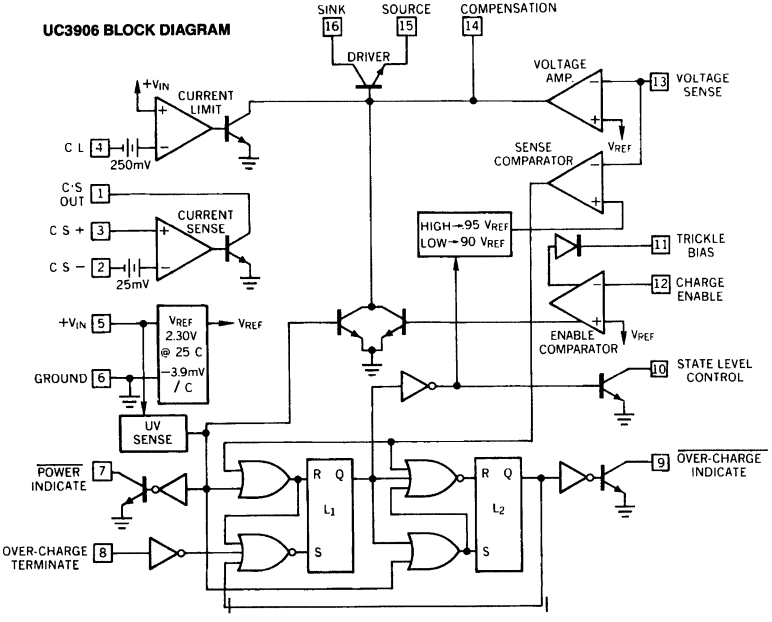


FIGURE 1. The UC3906 Sealed Lead-Acid Battery Charger combines precision voltage and current sensing with voltage and current control to realize optimum battery charge cycles. Internal charge state logic sequences the device through charging cycles. Voltage control and sensing is referenced to an internal voltage that specially tracks the temperature characteristics of lead-acid cells.

Acid Battery Charger has all the control and sensing functions necessary to optimize cell capacity and life in a wide range of battery applications.

The block diagram for the UC3906 is shown in figure 1. Separate voltage loop and current limit amplifiers regulate the output voltage and current levels in the charger by controlling the onboard driver The driver will supply 25mA of base drive to an external pass element. Voltage and current sense comparators are used to sense the battery condition and respond with logic inputs to the charge state logic. The charge enable comparator on this IC can be used to remotely disable the charger The comparator's 25mA trickle bias output is active high when the driver is disabled. These features can be combined to implement a low current turn-on mode in a charger, preventing high current charging during abnormal conditions such as a shorted or reversed battery.

A very important feature of the UC3906 is its precision reference. The reference voltage is specially temperature compensated to track the temperature characteristics of lead-acid cells. The IC operates with very low supply current, only 1.7mA, minimizing on-chip dissipation and permitting the accurate sensing of the operating environmental temperature. In addition, the IC includes a supply under-voltage sensing circuit, used to initialize charging cycles at power on. This circuit also drives a logic output to indicate when input power is present. The UC3906 is specified for operation over the commercial temperature range of 0°C to 70°C. For operation over extended temperatures, -40°C to 70°C the UC2906 is available.

WHAT IS IMPORTANT IN A CHARGER?

Capacity and life are critical battery parameters that are strongly affected by charging methods. Capacity, C, refers to the number of ampere-hours that a charged battery is rated to supply at a given discharge rate. A battery's rated capacity is generally used as the unit for expressing charge and discharge current rates, i.e., a 2.5 amp-hour battery charging at 500mA is said to be charging at a C/5 rate. Battery life performance is measured in one of two ways; cycle life or stand-by life. Cycle life refers to the number of charge and discharge cycles that a battery can go through before its capacity is reduced to some threshold level. Standby life, or float life, is simply a measure of how long the battery can be maintained in a fully charged state and be able to provide proper service when called upon. The measure which actually indicates useful life expectancy in a given application will depend on the particulars of the application. In general, both aspects of battery life will be important.

During the charge cycle of a typical lead-acid cell, lead sulfate, $PbSO_4$, is converted to lead on the battery's negative plate and lead dioxide on the battery's positive plate. Once the majority of the lead sulfate has been converted, over-charge reactions begin. The typical result of over-charge is the generation of hydrogen and oxygen gas. In unsealed batteries this results in the immediate loss of water. In sealed cells, at moderate charge rates, the majority of the hydrogen and oxygen recombine before dehydration occurs. In either type of cell, prolonged charging rates significantly above C/500, will result in dehydration, accelerated grid corrosion, and reduced service life.

The onset of the over-charge reaction will depend on the rate of charge. At charge rates of >C/5, less than 80% of the cell's previously discharged capacity will be returned as the over-charge reaction begins. For over-charge to coincide with 100% return of capacity, charge rates must typically be reduced to less than C/100. Also, to accept higher rates the battery voltage must be allowed to increase as over-charge is approached. Figure 2 illustrates this phenomenon, showing cell voltage vs. percent return of previously discharged capacity for a variety of charge rates. The over-charge reaction begins at the point where the cell voltage rises sharply, and becomes excessive when the curves level out and start down again.

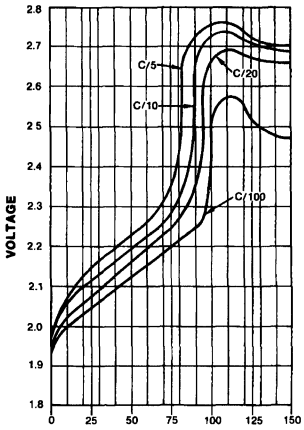


FIGURE 2. Depending on the charge rate, over-charge reactions begin, (indicated by the sharp rise in battery voltage), well below 100% return of capacity. (Reprinted with the permission of Gates Energy Products. Inc.)

Once a battery is fully charged, the best way to maintain the charge is to apply a constant voltage to the battery. This burdens the charging circuit with supplying the correct float charge level; large enough to compensate for self-discharge, and not too large to result in battery degradation from excessive overcharging. With the proper float charge, sealed lead-acid batteries are expected to give standby service for 6 to 10 years. Errors of just five percent in a float charger's characteristics can halve this expected life.

To compound the above concerns, the voltage characteristics of a lead-acid cell have a pronounced negative temperature dependence, approximately -4.0mV/°C per 2V cell. In other words, a charger that works perfectly at 25°C may not maintain or provide a full charge at 0°C and conversely may drastically over-charge a battery at +50°C. To function properly at temperature extremes a charger must have some form of compensation to track the battery temperature coefficient.

To provide reasonable re-charge times with a full 100% return of capacity, a charge cycle must adapt to the state of charge and the temperature of the battery. In sealed, or recombinate, cells, following a high current charge to return the bulk of the expended capacity, a controlled over-charge should take place. For unsealed cells the over-charge reaction must be minimized. After the over-charge, or at the onset of over-charge, the charger should convert to a precise float condition.

A DUAL LEVEL FLOAT CHARGER

A state diagram for a sealed lead-acid battery charger that would meet the above requirements is shown in figure 3.

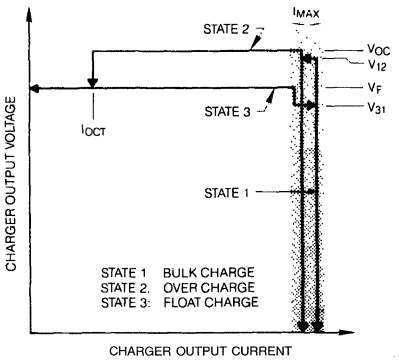


FIGURE 3. The dual level float charger has three charge states. A constant current bulk charge returns 70-90% of capacity to the battery with the remaining capacity returned during an elevated (constant) voltage over-charge. The float charge state maintains a precision voltage across the battery to optimize stand-by life.

This charger, called a dual level float charger, has three states, a high current bulk charge state, an over-charge state, and a float state. A charge cycle begins with the charger in the bulk charge state. In this state the charger acts like a current source providing a constant charge rate at I_{MAX}. The charger monitors the battery voltage and as it reaches a transition threshold, V_{12}, the charger begins its over-charge cycle. During the over-charge, the charger regulates the battery at an elevated voltage, V_{OC}, until the charge rate drops to a specified transition current, I_{OCT}. When the current tapers to I_{OCT}, with the battery at the elevated level, the capacity of the cell should be at nearly 100%. At this point the charger turns into a voltage regulator with a precisely defined output voltage, V_F. The output voltage of the charger in this third state sets the float level for the battery.

With the UC3906, this charge and hold cycle can be implemented with a minimum of external parts and design effort. A complete charger is shown in figure 4. Also shown are the design equations to be used to calculate the element values for a specific application. All of the programming of the voltage and current levels of the charger are determined by the appropriate selection the external resistors R_S, R_A, R_B, R_C.

Operation of this charger is best understood by tracing a charge cycle. The bulk charge state, the beginning, is initiated by either of two conditions. One is the cycling on of the input supply to the charger; the other is a low voltage condition on the battery that occurs while the charger is in the float state. The under-voltage sensing circuit on the UC3906 measures the input supply to the IC. When the input supply drops below about 4.5V the sensing circuit forces the two state logic latches (see figure 1) into the bulk charge condition (L1 reset and L2 set). This circuit also disables the driver output during the under-voltage condition. To enter the bulk charge state while power is on, the charger must first be in the float state (both latches set). The input to the charge state logic coming from the voltage sense comparator reports on the battery voltage. If the battery voltage goes low this input will reset L1 and the bulk charge state will be initiated.

With L1 reset, the state level output is always active low. While this pin is low the divider resistor, R_B is shunted by resistor R_C, raising the regulating level of the voltage loop. If we assume that the battery is in need of charge, the voltage amplifier will be in its stops trying to turn on the driver to force the battery voltage up. In this condition the voltage amplifier output will be over-ridden by the current limit amplifier. The current limit amplifier will control the driver, regulating the output current to a constant level. During this

time the voltage at the internal, non-inverting, input to the voltage sense comparator is equal to 0.95 times the internal reference voltage. As the battery is charged its voltage will rise; when the scaled battery voltage at PIN 13, the inverting input to the sense comparator, reaches 0.95Vref the sense comparator output will go low. This will reset the second latch and the over-charge state will be entered. At this time the over-charge indicator output will go low. Other than this there is no externally observable change in the charger Internally, the starting of the over-charge state arms the set input of the first latch – assuming no reset signal is present -– so that when the over-charge terminate input goes high, the charger can enter the float state.

In the over-charge state, the charger will continue to supply the maximum current. As the battery voltage reaches the elevated regulating level, V_{OC}, the voltage amplifier will take command of the driver, regulating the output voltage at a constant level. The voltage at PIN 13 will now be equal to the internal reference voltage. The battery is completing its charge cycle and the charge acceptance will start to taper off.

As configured in figure 4, the current sense comparator continuously monitors the charge rate by sensing the voltage across R_S. The output of the comparator is connected to the over-charge terminate input. Whenever the charge current is less than I_{OCT}, ($25mV/R_S$), the open collector output of the comparator will be off. When this transition current is reached, as the charge rate tapers in the over-charge state, the off condition of the comparator output will allow an internal 10μA pull-up current at PIN 8 to pull that point high. A capacitor can be added from ground to this point to provide a delay to the over-charge-terminate function, preventing the charger from prematurely entering the float state if the charging current temporarily drops due to system noise or whatever. When the voltage at PIN 8 reaches its 1V threshold, latch L1 will be set, setting L2 as well, and the charger will be in the float state. At this point the state level output will be off, effectively eliminating R_C from the divider and lowering the regulating level of the voltage loop to V_F.

In the float state the charger will maintain V_F across the battery, supplying currents of zero to I_{MAX} as required. In addition, the setting of L1 switches the voltage sense comparator's reference level from 0.95 to 0.90 times the internal reference. If the battery is now discharged to a voltage level 10% below the float level, the sense comparator output will reset L1 and the charge cycle will begin anew.

The float voltage V_F, as well as V_{OC} and the transition voltages, are proportional to the internal reference on the UC3906. This reference has a temperature coefficient of

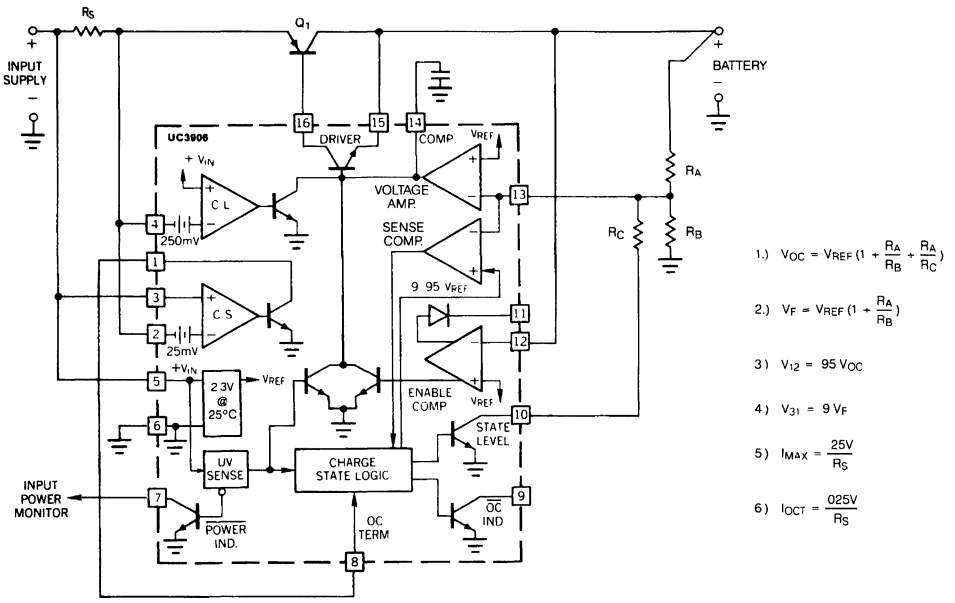


FIGURE 4. Using a few external parts and following simple design equations the UC3906 can be configured as a dual level float charger.

-3.9mV/°C. This temperature dependence matches the recommended compensation of most battery manufacturers. The importance of the control of the charger's voltage levels is reflected in the tight specification of the tolerance of the UC3906's reference and its change with temperature, as shown in figure 5.

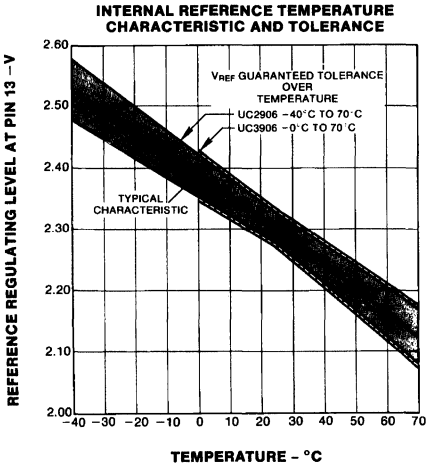


FIGURE 5. The specially temperature compensated reference on the UC3906 is tightly specified over 0 to 70°C (-40 to 70°C for the UC2906). to allow proper charge and hold characteristics at all temperatures.

I_{MAX}, I_{OCT}, V_{OC}, and V_F can all be set independently. I_{MAX}, the bulk charge rate can usually be set as high as the available power source will allow, or the pass device can handle. Battery manufacturers recommend charge rates in the C/20 to C/3 range, although some claim rates up to and beyond 2C are OK if protection against excessive overcharging is included. I_{OCT}, the over-charge terminate threshold, should be chosen to correspond, as close as possible, to 100% recharge. The proper value will depend on the over-charge voltage (V_{OC}) used and on the cell's charge current tapering characteristics at V_{OC}.

I_{MAX} and I_{OCT} are determined by the offset voltages built into the current limit amplifier and current sense comparator respectively, and-the resistor(s) used to sense current. The offsets have a fixed ratio of 250mV/25mV. If ratios other than ten are necessary separate current sensing resistors or a current sense network, must be used. The penalty one pays in doing this is increased input-to-output differential requirements on the charger during high current charging. Examples of this are shown in figure 6.

An alternative method for controlling the over-charge state is to use the over-charge indicate output, PIN 9, to initiate an external timer. At the onset of the over-charge cycle the over-charge indicate pin will go low. A timer triggered by this signal could then activate the over-charge terminate input, PIN 8, after a timed over-charge has taken place. This method is particularly attractive in systems with a centralized system controller where the controller can provide the timing function and automatically be aware of the state of charge of the battery.

The float, V_F, and over-charge, V_{OC}, voltages are set by the internal reference and the external resistor network, R_A, R_B, and R_C as shown in figure 4. For the dual level float charger the ranges at 25°C for V_F and V_{OC} are typically 2.3V-2.40V and 2.4V-2.7V, respectively. The float charge level will normally be specified very precisely by the battery manufacturer, little variation exists among most battery suppliers. The over-charge level, V_{OC}, is not as critical and will vary as a function of the charge rate used. The absolute value of the divider resistors can be made large, a divider current of 50μA will sacrifice less than 0.5% in accuracy due to input bias current offsets.

AUXILIARY CAPABILITIES OF THE CHARGER IC

Besides simply charging batteries, the UC3906 can be used to add many related auxiliary functions to the charger that would otherwise have to be added discretely. The enable comparator and its trickle bias output can be used in a number of different ways. The modification of the state diagram in figure 2 to establish a low current turn-on mode

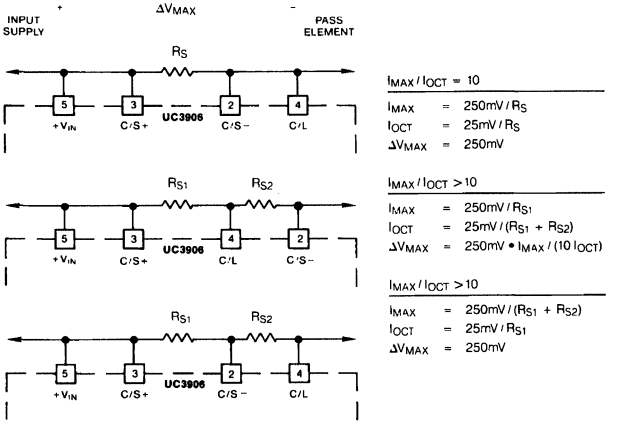


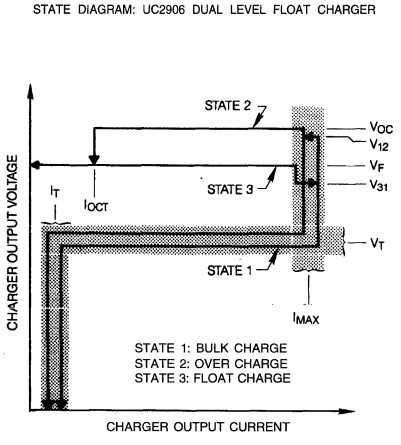
FIGURE 6. Although the ratio of input offset voltages on the current limit and current sense stages is fixed at 10. other ratios for I_{MAX}/I_{OCT} are easily obtained. Note that a penalty for ratios greater than 10 is increased voltage drop across the sensing network at I_{MAX}.

of the charger (see figure 7) is easily done. By reducing the output current of the charger when the battery voltage is below a programmable threshold, the charging system protects against: One, high current charging of a string with a shorted cell that could result in excessive outgassing from the remaining cells in the string. Two, dumping charge into a battery that has been hooked up backwards. Three, excessive power dissipation in the charger's pass element. As shown in figure 7, the enable comparator input taps off the battery sensing divider, When the battery voltage is below the resulting threshold, V_T, the driver on the UC3906 is disabled and the trickle bias output goes high. A resistor, R_T, connected to the battery from this output can then be used to set a trickle current, ($\leq$ 25mA) to the battery to help the charger discriminate between severely discharged cells and damaged, or improperly connected, cells.

In applications where the charger is integral to the system, i.e. always connected to the battery, and the load currents on the battery are very small, it may be necessary to absolutely minimize the load on the battery presented by the charger when input power is removed. There are two simple precautions that, when taken, will remove essentially all reverse current into the charging circuit. In figure 8 the diode in series with the pass element will prevent any reverse current through this path. The sense divider should still be referenced directly to the battery to maintain accurate control of voltage. To eliminate this discharge path, the divider in the figure is referenced to the open collector power indicate output, PIN 7, instead of ground. Connected in this manner the divider string will be in series with essentially an open when input power is removed. When power is present, the open collector device will be on, holding the divider string end at nearly ground. The saturation voltage of the open collector output is specified to be less than 50mV with a load current of 50μA.

Figure 9 illustrates the use of the enable comparator and its output to build over-discharge protection into a charger. Over-discharging a lead-acid cell, like over-charging, can severely shorten the service life of the cell. The circuit monitors the discharging of the battery and disconnects all load from the battery when its voltage reaches a specified cutoff point. The load will remain disconnected from the battery until input power is returned and the battery recharged.

This scheme uses a relay between the battery and its load that is controlled by Q1 and the presence of voltage across the load. When primary power is available Q1 is on via D5. The battery is charging, or charged, and the trickle bias output at PIN 11 is off. When input power is removed, C2 provides enough hold-up time at the load to let Q1 turn off, and the relay to close as current flows through R1. The battery is now providing power to the load and, through D1, power to the charger. The charger current draw will typically be less than 2mA. As the battery discharges, the UC3906 will continue to monitor its voltage. When the vol-



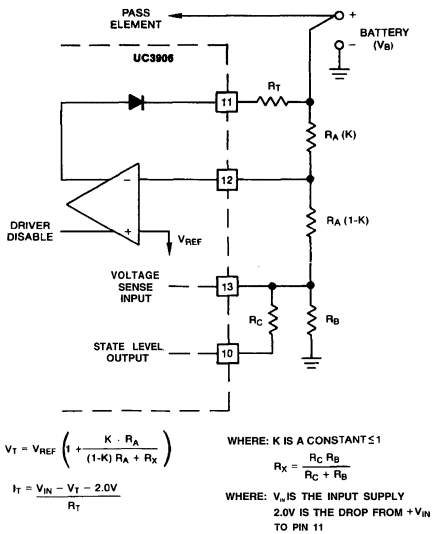


FIGURE 7. The charge enable comparator, with its trickle bias output, can be used to build protection into the charger. The current foldback at low battery voltages prevents high current charging of batteries with shorted cells, or improperly connected batteries, and also protects the pass element from excessive power dissipation.

tage reaches the cut-off level, set by the divider network, R5-R8, the trickle bias output, PIN 11, will go high. Q1 will turn back on and the relay current will collapse opening its contacts. As the load voltage drops, capacitor Cl supplies power to the UC3906 to keep Q1 on. Once the input to the charger has collapsed the power indicate pin, as shown in figure 8, will open the divider string. The battery will remain open-circuited until input power is returned. At that time the battery will begin to recharge.

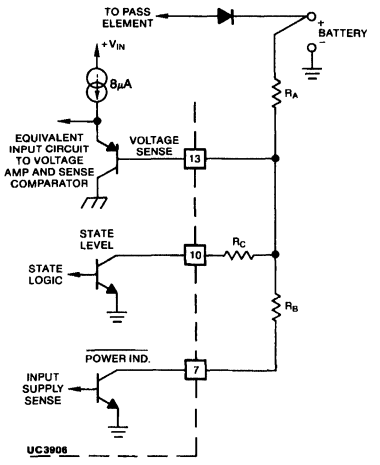


FIGURE 8. By using a diode in series with the pass element, and referencing the divider string to the power indicate pin. pin 7, reverse current into the charger, (when the charger is tied to the battery with no input power), can be eliminated.

CHARGING LARGE SERIES STRINGS OF LEAD-ACID CELLS

When large series strings of batteries are to be charged, a dual step current charger has certain advantages over the float charger of figures 3 and 4. A state diagram and circuit implementation of this type of charger is shown in figure 10. The voltage across a large series string is not as predictable as a common 3 or 6 cell string. In standby service varying self discharge rates can significantly alter the state of charge of individual cells in the string if a constant float voltage is used. The elevated voltage, low current holding state of the dual step current charger maintains full and equal charge on the cells. The holding, or trickle current, IH, will typically be on the order of 0.005C to 0.0005C.

To give adequate and accurate recharge this charger has a bulk charge state with temperature compensated transition thresholds, V_{12}, and V_{21}. Instead of entering an elevated voltage over-charge, upon reaching V_{12} the charger switches to a constant current holding state. The holding current will maintain the battery voltage at a slightly elevated level but not high enough to cause significant overcharging. If the battery current increases, the charger will attempt to hold the battery at the V_F level as shown in the state diagram. This may happen if the battery temperature increases significantly, increasing the self-discharge rate beyond the holding current. Also, immediately following the transition from the bulk to float states, the battery will only be 80% to 90% charged and the battery voltage will drop to the V_F level for some period of time until full charging is achieved.

In this charger the current sense comparator is used to regulate the holding current. The level of holding current is determined by the sensing resistor, R_{SH}. The other series

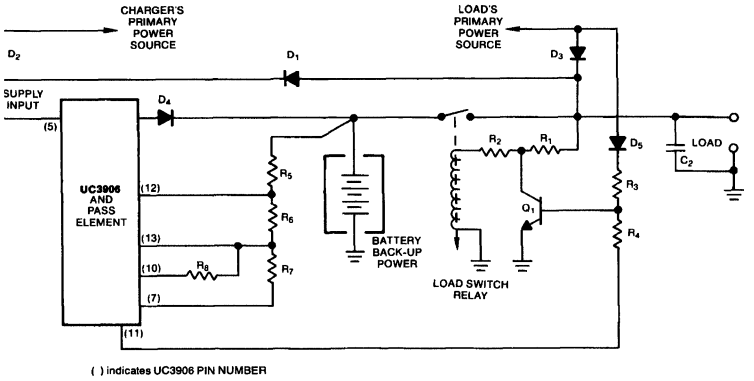


FIGURE 9. Using the enable comparator to monitor the battery voltage a precise discharge cut-off voltage can be set. When the battery reaches the cut-off threshold the trickle bial output switches off the load switch relay and the battery is left open circuited until input power is returned.

resistor, R_E, is necessary for the current sense comparator to regulate the holding current. Its value is selected by dividing the value of I_H into the minimum input to output differential that is expected between the battery and the input supply. If the supply variation is very large, or the holding current large, (> 25mA), then an external buffering element may be required at the output of the current sense comparator.

The operating supply voltage into the UC3906 should be kept less than 45V. However, the IC can be adapted to charge a battery string of greater than 45V. To charge a large series string of cells with the dual step current charger the ground pin on the UC3906 can be referenced to a tap point on the battery string as shown in figure 11. Since the charger is regulating current into the batteries, the cells will all receive equal charge. The only offset results from the bias current of the UC3906 and the divider string current adding to the current charging the battery cells below the tap point. R_B can be added to subtract the bulk of this current improving the ability of the charger to control the low level currents. The voltage trip points using this technique will be based on the sum of the cell voltages on the high side of the tap.

PICKING A PASS ELEMENT AND COMPENSATING THE CHARGER

There are four factors to consider when choosing a pass device. These are:

1. The pass device must have sufficient current and power handling capability to accommodate the desired maximum charging rate at the maximum input to output differential.
2. The device must have a high enough current gain at the maximum charge rate to keep the drive current required to less than 25mA.
3. The type of device used, (PNP, NPN, or FET), and its configuration, may be dictated by the minimum input to output differential at which the charger must operate.
4. The open loop gain of both the voltage and the current control loops are dependent on the pass element and its configuration.

Figure 12 contains a number of possible driver configurations with some rough break points on applicable current ranges as well as the resulting minimum input to output differentials. Also included in this figure are equations for the dissipation that results on the UC3906 die, equations for a resistor, R_D, that can be added to minimize this dissipation, and expressions for the open loop gains of both the voltage and current loops.

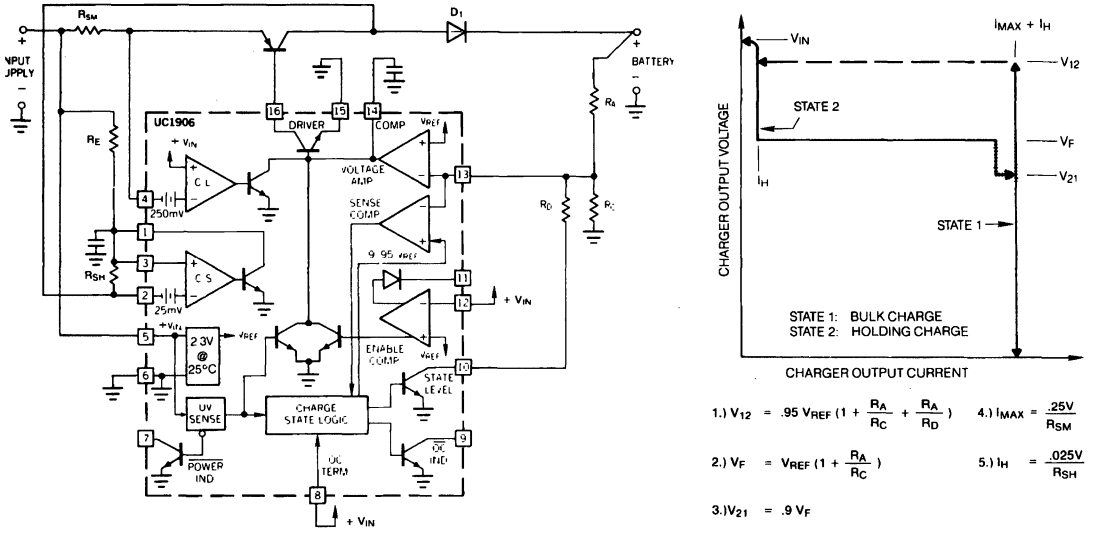


FIGURE 10. A dual step current charger has some advantages when large series strings must be charged. This type of charger maintains constant current during normal charging that results in equal charge distribution among battery cells.

As reflected in the gain expressions in figure 12, the open loop voltage gains of both the voltage and current control loops are dependent on the impedance, Z_C at the compensation pin. Both loops can be stabilized by adjusting the value of this impedance. Using the expressions given, one can go through a detailed analysis of the loops to predict respective gain and phase margins. In doing so one must not forget to account for all the poles in the open loop expressions. In the common emitter driver examples, 1 and 3, the equivalent load impedance at the output of the charger directly affects loop characteristics. In addition, a pole, or poles, will be added to the loop response due to the roll-off of the pass device's current gain, Beta. This effect will occur at approximately the rated unity gain frequency of the device divided by its low frequency current gain. The transconductance terms for the voltage and current limit amplifiers, (1/1.3K and 1/300 respectively), will start to roll off at about 500KHZ. As a rule of thumb, it is wise to kill the loop gain well below the point that any of these, not-so-predictable poles, enter the picture.

If you prefer not to go through a BODE analysis of the loops to pick a compensation value, and you recognize the fact that battery chargers do not require anything close to optimum dynamic response, then loop stability can be assured by simply oversizing the value of the capacitor used at the compensation pin. In some cases it may be necessary to add a resistor in series with the compensation capacitor to put a zero in the response. Typical values for the compensation capacitor will range from 1000pF to 0.22μF depending on the pass device and its configuration. With composite common emitter configurations, such as example 3 in figure 12, compensation values closer to the 0.22μF value will be required to roll off the large open loop gain that results from the Beta squared term in the gain expression. Series resistance should be less than 1K, and may range as low as 100 ohms and still be effective.

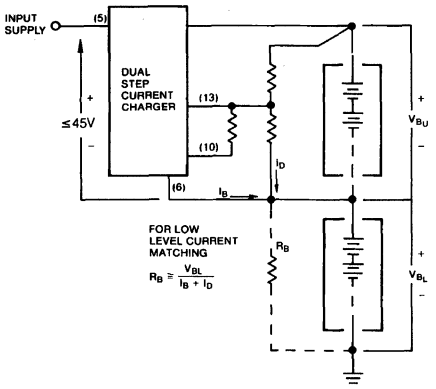
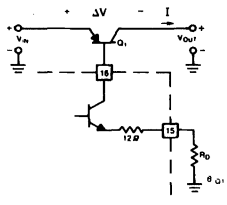
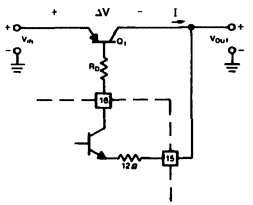
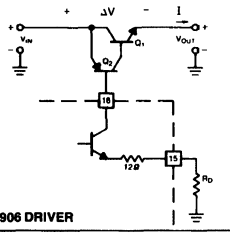
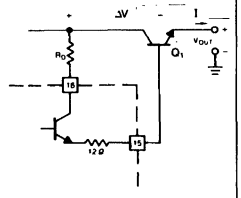


FIGURE 11. A dual step current charger can be configured to operate with input supplies of greater than 45V by using a tap on the battery to reference the UC3906. The charger uses the voltage across the upper portion of the battery to sense charging transition points. To minimize charging current offsets, R_B can be added to cancel the UC3906 bras and divider currents.

The power dissipated by the UC3906 requires attention since the thermal resistance, (100°C/Watt) of the DIP package can result in significant differences in temperature between the UC3906 die and the surrounding air, (battery), temperature. Different driver/pass element configurations result in varying amounts of dissipation at the UC3906. The dissipation can be reduced by adding external dropping resistors in series with the UC3906 driver,

TOPOLOGY	COMMON EMITTER PNP	COMPOSITE FOLLOWER	COMPOSITE COMMON EMITTER	NPN EMITTER FOLLOWER
				
	UC3906 DRIVER	UC3906 DRIVER	UC3906 DRIVER	UC3906 DRIVER
CURRENT RANGE	25mA < I < 1000mA	25mA < I < 1000mA	600mA < I < 15A	25mA < I < 1000mA
MINIMUM ΔV	$\Delta V > 0.5V$	$\Delta V > 2.0V$	$\Delta V > 1.2V$	$\Delta V > 2.7V$
UC3906 DRIVER DISSIPATION	$P_D \approx \frac{V_{IN} - 0.7V}{\beta_{Q1}} \bullet I - \frac{I^2 R_D}{\beta^2_{Q1}}$	$P_D \approx \frac{V_{IN} - 0.7V - V_{OUT}}{\beta_{Q1}} \bullet I - \frac{I^2 R_D}{\beta^2_{Q1}}$	$P_D \approx \frac{V_{IN} - 0.7V}{\beta_{Q1}\beta_{Q2}} \bullet I - \frac{I^2 R_D}{\beta^2_{Q1}\beta^2_{Q2}}$	$P_D \approx \frac{V_{IN} - 0.7V - V_{OUT}}{\beta_{Q1}} \bullet I - \frac{I^2 R_D}{\beta^2_{Q1}}$
EXPRESSION FOR R_D	$R_D \approx \frac{V_{IN\,MIN} - 2.0V}{I_{MAX}} \bullet \beta_{Q1\,MIN}$	$R_D \approx \frac{V_{IN\,MIN} - V_{OUT\,MAX} - 1.2V}{I_{MAX}} \bullet \beta_{Q1\,MIN}$	$R_D \approx \frac{V_{IN\,MIN} - 0.7V}{I_{MAX}} \bullet \beta_{Q1\,MIN}\beta_{Q2\,MIN}$	$R_D \approx \frac{V_{IN\,MIN} - V_{OUT\,MAX} - 1.2V}{I_{MAX}} \bullet \beta_{Q1\,MIN}$
OPEN LOOP* GAIN OF THE VOLTAGE CONTROL LOOP	$A_{OV} \approx \frac{Z_C}{1.3K} \bullet \frac{1}{R_D + 12} \bullet \beta_{Q1} \bullet Z_O \bullet \frac{V_{REF}}{V_{OUT}}$	$A_{OV} \approx \frac{Z_C}{1.3K} \bullet \frac{V_{REF}}{V_{OUT}}$	$A_{OV} \approx \frac{Z_C}{1.3K} \bullet \frac{1}{R_D + 12} \bullet \beta_{Q1} \bullet \beta_{Q2} \bullet Z_O \bullet \frac{V_{REF}}{V_{OUT}}$	$A_{OV} \approx \frac{Z_C}{1.3K} \bullet \frac{V_{REF}}{V_{OUT}}$
OPEN LOOP* GAIN OF THE CURRENT LIMIT LOOP	$A_{OC} \approx \frac{Z_C}{300} \bullet \frac{1}{R_D + 12} \bullet \beta_{Q1} \bullet R_S$	$A_{OC} \approx \frac{Z_C}{300} \bullet \frac{1}{12/\beta_{Q1} + Z_O} \bullet R_S$	$A_{OC} \approx \frac{Z_C}{300} \bullet \frac{1}{R_D + 12} \bullet \beta_{Q1} \bullet \beta_{Q2} \bullet R_S$	$A_{OC} \approx \frac{Z_C}{300} \bullet \frac{1}{12/\beta_{Q1} + Z_O} \bullet R_S$

*Z_C = IMPEDANCE AT COMPENSATION PIN, PIN 14. = IMPEDANCE AT CHARGER OUTPUT

FIGURE 12. There are a large number of possible driver/pass element configurations, a few are summarized here. The trade-offs are between current gain, input to output differential. and in some cases, power dissipation on the UC3906. When dissipation is a problem it can be reduced by adding a resistor in series with the UC3906 driver.

(see figure 12). These resistors will then share the power with the die. The charger parameters most affected by increased driver dissipation are the transition thresholds, (V_{12} and V_{21}), since the charger is, by design, supplying its maximum current at these points. The current levels will not be affected since the input offset voltages on the current amplifier and sense comparator have very little temperature dependence. Also, the stand-by float level on the charger will still track ambient temperature accurately since, normally, very little current is required of the charger during this condition.

To estimate the effects of dissipation on the charger's voltage levels, calculate the power dissipated by the IC at any given point, multiply this value by the thermal resistance of the package, and then multiply this product by -3.9mV/°C and the proper external divider ratio. In most cases, the effect can be ignored, while in others the charger design must be tweaked to account for die dissipation by adjusting charger parameters at critical points of the charge cycle.

SOME RESULTS WITH THE DUAL LEVEL FLOAT CHARGER

In figure 13 the schematic is shown for a dual level, float charger designed for use with a 6V, 2.5amp-hour, sealed lead-acid battery. The specifications, at 25°C, for this charger are listed below.

Input supply voltage . . . . . 9.0V to 13V
Operating temperature range . . . . . 0°C to 70°C
Start-up trickle current (I_T) . . . . . 10mA (V_{IN} = 10V)
Start-up voltage (V_T) 5.1V
Bulk charge rate (I_{MAX}) 500mA (C/5)
Bulk to OC transition voltage (V_{12}) . . 7.125V
OC voltage (V_{OC}) 7.5V
OC terminate current (I_{OCT}) 50mA (C/50)
Float voltage (V_F) 7.0V
Float to Bulk transition voltage (V_{31}) 6.3V
Temperature coefficient on voltage levels . . . . . -12mV/°C
Reverse current at charger output with the input supply at 0.0V . . . . $\leq 5\mu A$

In order to achieve the low input to output differential, (1.5V) the charger was designed with a PNP pass device that can operate in its saturation region under low input supply conditions. The series diode, required to meet the reverse current specification, accounts for 1.0V of the 1.5V minimum differential. Keeping the reverse current under 5μA also requires the divider string to be disconnected when input power is removed. This is accomplished, as discussed earlier, by using the input power indicate pin to reference the divider string.

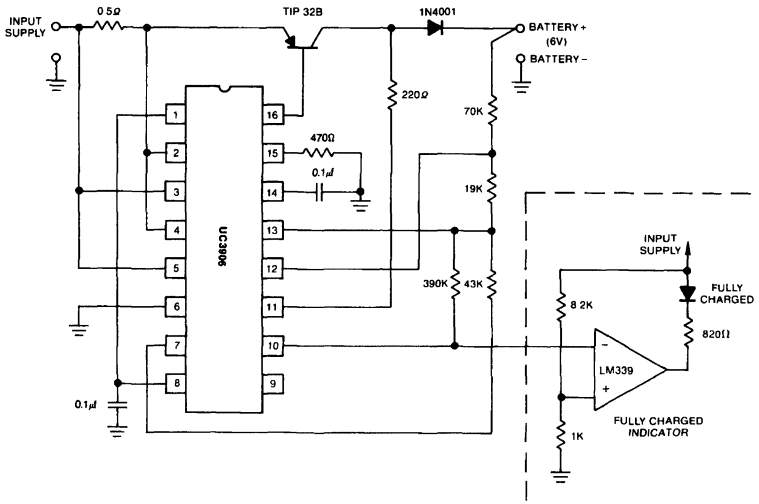


FIGURE 13. This dual level float charger was designed for a 6V (three 2V cells) 2.5AH battery. A separate "fully charged" indicator was added for visual indication of charge completion.

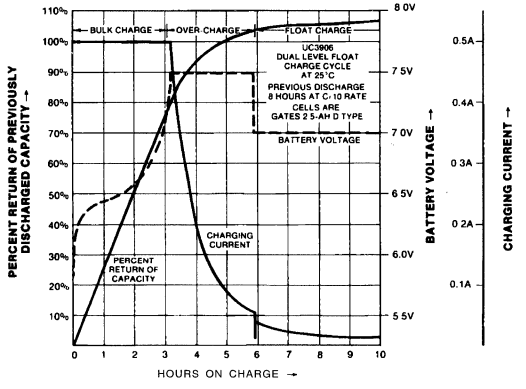


FIGURE 14. The nearly ideal characteristics of the dual level float charger are illustrated in these curves. The over-charge state is entered at about 80% return of capacity and float charging begins at just over 100% return.

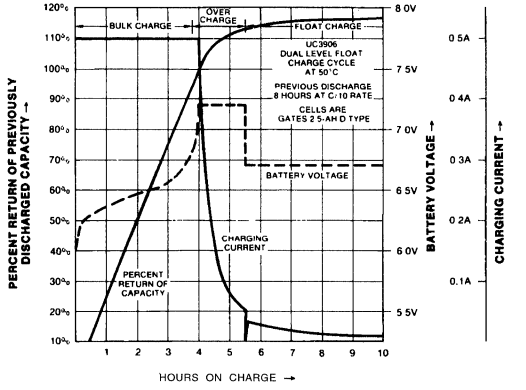


FIGURE 15. At elevated temperatures the maximum capacity of lead-acid cells is increased allowing greater charge acceptance. To prevent excessive over-charging though, the charging voltage levels are reduced.

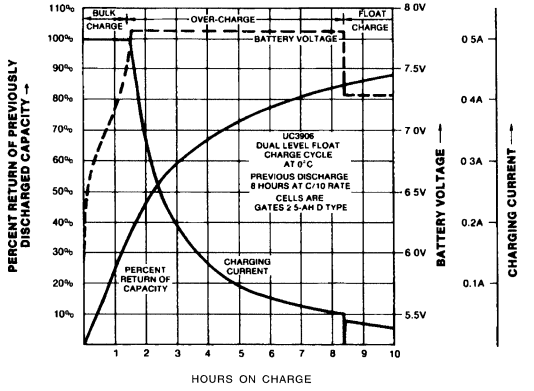


FIGURE 16. At lower temperatures the capacity of lead-acid cells is reduced as reflected by the less-than-100% return of capacity in this 0°C charge cycle, illustrating the need for elevated charging voltages to maximize returned capacity.

The driver on the UC3906 shunts the drive current from the pass device to ground. The 470ohm resistor added between PIN 15 and ground keeps the die dissipation to less than 100mW under worst case conditions, assuming a minimum forward current gain in the pass element of 35 at 500mA.

The charger in figure 13 includes a circuit to detect full charge and gives a visual indication of charge completion with an LED. This circuit turns on the LED when the battery enters the float state. Entering of the float state is detected by sensing when the state level output turns-off.

Figures 14-16 are plots of charge cycles of the circuit at three temperatures, 25°C, 50°C and 0°C. The plots show battery voltage, charge rate, and percent return of previously discharged capacity. This last parameter is the integral of the charge current over the time of the charge cycle, divided by the total charge volume removed since the last full charge. For all of these curves the previous discharge was an 80% discharge, (2amp-hours), at a C/10, (250mA), rate. The discharges were preceded by an over-night charge at 25°C.

The less than 100% return of capacity evident in the charge cycle at 0°C is the result of the battery's reduced capacity at this temperature. The tapering of the charge current in the over-charge state still indicates that the cells are being returned to a full state of charge.

REFERENCES

1. Eagle-Picher Industries, Inc., Battery Notes #200, #205A, #206, #207, #208.
2. Gates Energy Products, Inc., Battery Application Manual, 1982.
3. Panasonic, Sealed Lead-Acid Batteries Technical Handbook.
4. Yuasa Battery Co., Ltd., NP series maintenance-free rechargeable battery Application Manual.

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AN OFF-LINE LEAD ACID CHARGER BASED ON THE UC3909

INTRODUCTION

Lead-acid batteries are the most commonly used batteries where large amounts of energy must be stored and low cost is more important than weight or physical size. Typical applications include UPS systems, alarm system backup power, telephone system backup power and larger portable electronic devices such as a bag-phone. This paper presents an isolated switch-mode charging circuit for lead-acid batteries that operates from a $115V_{ac}$ circuit.

The reader is encouraged to read the references listed at the end of this paper. There is much useful information there that will not be repeated here.

DESIGN REQUIREMENTS

For this design, the goal is to charge an Eagle-Picher HE12V12.7 battery as quickly and safely as possible to the highest practically attainable capacity, and maintain this capacity indefinitely. From the battery manufacturer's data sheet, this battery may be charged from a 14.6 to 15.0 volt source that is current limited to 4.0 amps. Therefore, the bulk charge current for this charger (I_{bulk}) will be 4.0 amps and the maximum overcharge voltage (V_{oc}) will be 14.8 volts. The float voltage is specified to be 13.6 to 13.8 volts. This charger will float the battery at 13.8 volts (V_{float}). The battery is specified to a discharge voltage of 10.5 volts so this value will be used as the bulk charge enable threshold (V_{CHGENB}).

The remaining parameters that must be specified for the circuit (I_{OCT} and I_{TC}) are up to the circuit designer. In this design, the over charge terminate current threshold (I_{OCT}) is picked to be 10% of I_{BULK} or 400mA. The trickle current (I_{TC}) is picked to be 2% of the bulk current or 80mA.

The power source for this charger will be a standard 125 V_{ac} circuit. The tolerances on this input voltage will be +10/–25%. This means that the bulk supply on the primary side can range from 130 to 195 V_{dc}.

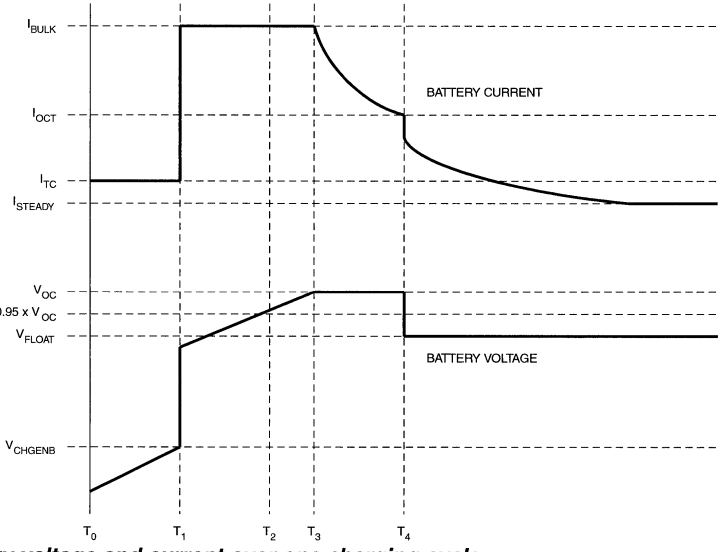

Figure 1. Battery voltage and current over one charging cycle.

DESIGN OVERVIEW

The UC3909 implements a four-stage charging algorithm. The four stages are trickle charge, bulk charge, over charge and float charge. The stages operate as follows in Fig. 1.

Trickle Charge

(T_0 to T_1) The charger will supply a small current, typically C/100 (I_{TC}) to the battery until the battery voltage reaches a predetermined threshold value (V_{CHGENB}). The purpose behind trickle charging is to prevent a potentially hazardous condition caused by continuously pumping bulk charge current into a damaged battery. Note that trickle charging may be skipped depending upon the battery voltage when the charger is powered. In some applications, it may be necessary to disable the trickle charge portion of the algorithm entirely. An example of this might be a device that normally operates from the incoming line and needs more current than can be programmed in the trickle charge state. The trickle charge stage can be permanently disabled by connecting CHGENB to VLOGIC.

Bulk Charge

(T_1 to T_2) The charger will supply a constant current to the battery if the battery voltage is above a given threshold. This current will be applied until the battery voltage rises above 95% of the maximum overcharge voltage.

Over Charge

(T_2 to T_4) During the over charge state, the charger tries to regulate the battery voltage to a constant voltage, V_{OC}. When the charger enters the over charge state, the current control loop will likely be dominant and a constant current will continue to be applied to the battery. As the battery voltage rises, the voltage control loop will begin to take over and regulate the battery voltage to the over charge voltage V_{OC} (Shown at T_3).

Float Charge

(T_4 and beyond) The float charge is entered when the battery current falls below a preset threshold while its voltage is held at V_{OC}. While in the float state, the charger will supply up to I_{bulk} amperes to a load and the battery. The charger will remain in the float state until power to the UC3909 is cycled or until the battery voltage drops below 90% of V_{OC}.

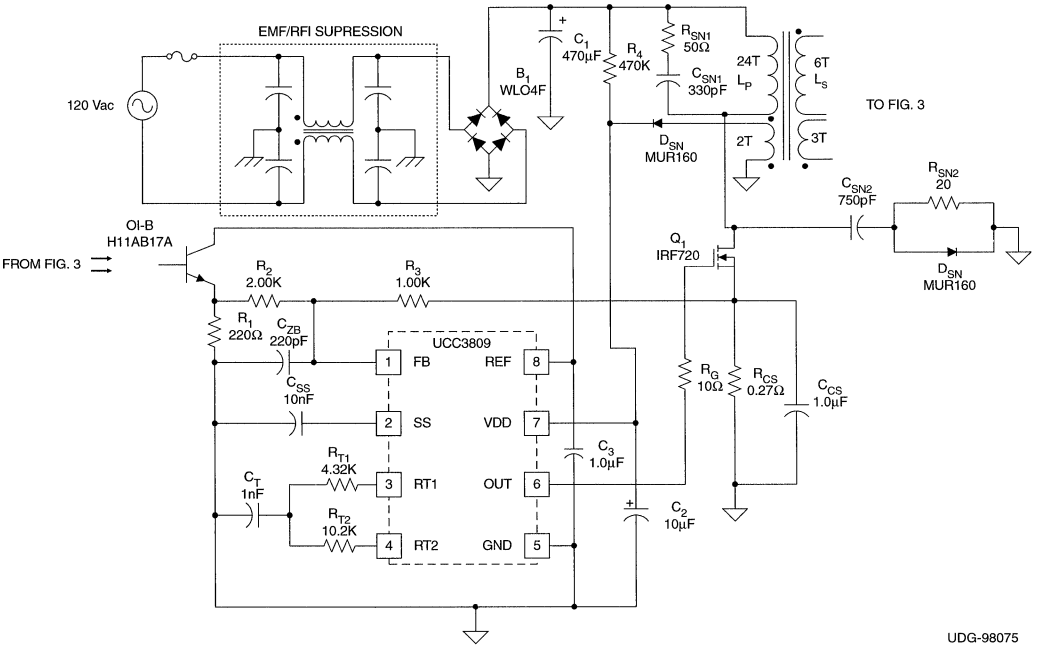

Figure 2. Primary side schematic.

If power is cycled, the charger will wake up in either the trickle or the bulk charge states, depending upon the battery voltage. If the battery voltage drops to 90% of V_{OC}, the charger will re-enter the bulk charge sate.

CIRCUIT DESCRIPTION

The circuit description presented is a discontinuous flyback with peak forward rectifiers on auxiliary windings to derive power for the control IC's. See Figs. 2 and 3.

The primary side schematic Fig. 2 shows a UCC3809 primary side controller being used as a peak current controller. The operating frequency and maximum switch on time are determined by components R_{T1}, R_{T2} and C_T. C_{SS} determines the soft start interval. R_{CS}, R_1, R_2, R_3, C_{ZB} and OI-B form the feedback and ramp circuit. C_3 is simply a bypass capacitor for the chip reference. R_4, D_1 and C_2 form the power supply for the UCC3809. R_{SN1}, C_{SN1}, R_{SN2}, C_{SN2} and D_{SN} are ring and dV/dt snubbers.

The secondary side schematic, Fig. 3, shows the UC3909 and its associated support components. D_4 and C_4 form the power supply circuit for the secondary side electronics. Q_2, Q_3, R_6 and R_7 disconnect the battery from the voltage divider string when the charger is not powered from the line. The resistor divider string R_{S1} through R_{S4} determines all voltage thresholds. R_{OVC1} and R_{OVC2} determine the current level for the transition from bulk charging to float charging.

The nature of the application demands that the UC3909 reside on the secondary side of the circuit with the battery. In order not to cause a current drain on the battery, the UC3909 will not be powered and the resistor divider string will be disconnected when the charger is not powered from the line. When line power is applied to the charger, several events take place. First, the startup resistor, R_4, supplies a small current to charge the supply capacitor, C_2, for the UCC3809. Second, when the voltage on this capacitor reaches the turn-on threshold for the UCC3809, the UCC3809 wakes up and begins charging the soft-start capacitor,

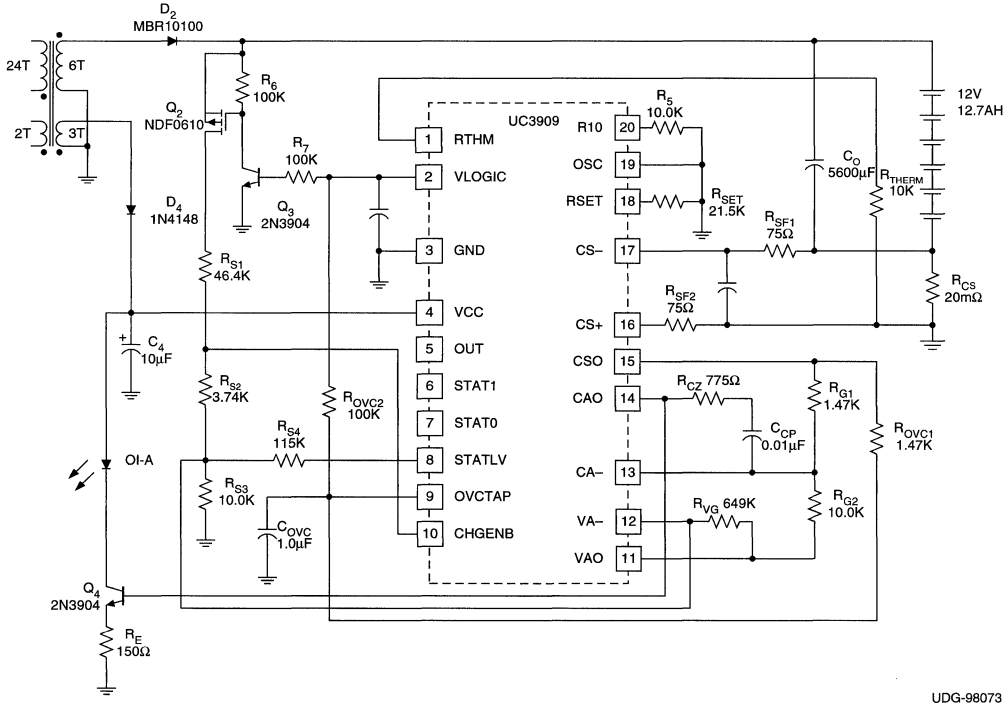

Figure 3. Secondary side schematic.

C_{SS}. Third, the UCC3809 issues no output pulses until the voltage on the soft-start capacitor reaches 0.7V. At this time, the UCC3809 will begin to issue output pulses. These pulses will be clamped to a width that is less than the maximum pulse width until the voltage on C_{SS} reaches 1.7V. Fourth, the bootstrap supplies for both the UCC3809 and the UC3909 come up and the charger begins charging the battery according to the charge algorithm described above and in the references.

The circuit is guaranteed to start (provided that the soft start capacitor is not chosen too large and cannot be charged to the 0.7V level before the voltage on C_4 falls to the UCC38098 UVLO threshold) since the feedback mechanism is commanding maximum pulse width until the opto-isolator is made to pass current into R_1. This cannot happen until the bootstrap supply for the UC3909 comes up. When the bootstrap supplies come up, the feedback circuit can then command shorter pulse widths from the UCC3809 and regulate the current and voltage output.

POWER STAGE DESIGN

Notation

Throughout this paper the following notation will be used.

Overbar: $\overline{V_{dc}}$ – a maximum value

Underbar: $\underline{I_{ls}}$ – a minimum value

Carat: $\hat{I}_{out}$ – an average value

Flyback Inductor Turns Ratio

The maximum turns ratio (N_p/N_s) is determined by the maximum voltage stress that is to be allowed on the power switching device, the maximum voltage that will be seen across the terminals of the secondary inductor winding and the amount of overshoot that will occur on the primary inductor when the power switch turns off. The peak power switch voltage is given by:

$$\overline{V_{ps}} = \overline{V_{dc}} + \overline{V_{ls}}\left(\frac{N_p}{N_s}\right) + V_{spike}$$

Where:

V_{ps} is the maximum power switch voltage (400V)

V_{dc} is the maximum dc voltage on the input filter capacitor C_1 (195V)

V_{ls} is the maximum voltage across the secondary inductor (15V + 1V for the diode)

N_p/N_s is the inductor turns ratio

V_{spike} is the leakage spike expected on switch turn-off (~ 30% of V_{dc})

With these values, taking a maximum N_p/N_s of 4 gives a maximum switch voltage of about 320 volts. This is well within safety margins for a 400 volt power switch.

Power Requirements

The maximum output power required from the flyback inductor is:

$$\overline{P_{out}} = \hat{I}_{out}\left(\overline{V_{batt}} + V_{diode}\right)$$

Where:

P_{out} is the output power of the flyback inductor

I_{out} is the maximum average output current (I_{bulk} or 4A)

V_{batt} is the maximum battery voltage (use 15V to allow for temperature correction)

V_{diode} is the voltage across the rectifier diode (use 1V to be conservative)

The input power to the inductor is the output plus an allowance for losses in the inductor and power switch. A conservative estimate is (based on 80% efficiency up to the output rectifier diode):

$$P_{IN} = \frac{P_{OUT}}{0.8}$$

In this application, the output power is 64W and the input power is 80W.

Inductor Values, Maximum "On" and "Reset" times, Peak Currents and Switching Frequency

The switching frequency was chosen to be 100 kHz as a compromise between switching losses and energy storage component size. To assure that the circuit remains discontinuous, the sum of the maximum on and reset times will only be allowed to be 85% of a switching period. The turns ratio, power requirements, discontinuity requirement and switching frequency define the values of the primary and secondary inductors, the peak currents and the on and reset times. From the following relationships, these values can be determined:

$$P_{in} = \frac{1}{2}\overline{I_p}^2 L_p F_s \quad (1)$$

$$\overline{I_p} = \overline{\tau_{on}}\frac{V_{dc}}{L_p} \quad (2)$$

$$\overline{I_s} = \overline{I_p}\frac{N_p}{N_s} \quad (3)$$

$$L_p = \left(\frac{N_p}{N_s}\right)^2 L_s \quad (4)$$

$$\tau_{rst} = \frac{\overline{I_s} L_s}{V_{batt} + V_{diode}} \quad (5)$$

$$\overline{\tau_{on}} + \overline{\tau_{rst}} \le \frac{0.85}{F_s} \quad (6)$$

Where:

I_p is the primary inductor peak current.

L_p is the primary inductance.

I_s is the secondary inductor peak current.

L_s is the secondary inductance.

τ_{on} is the on time.

τ_{rst} is the reset time.

F_s is the switching frequency

After some algebraic manipulation, it is obvious that (I couldn't resist.):

$$\overline{\tau_{on}} = \left(1 + \frac{V_{dc} N_s}{N_p\left(V_{batt} + V_{diode}\right)}\right) \le \frac{0.85}{F_s} \quad (7)$$

From this, τ_{on} will be less than about 2.97µs and τ_{rst} will be less than about 6.03µs. Note that these numbers are "ideal out of the math" and will change somewhat when the real world primary and secondary inductances are known.

Again, after some manipulation of equations (1) and (2),

$$L_p = \frac{\left(\overline{\tau_{on}} V_{dc}\right)^2 F_s}{2P_{in}} \quad (8)$$

L_p is then about 93µH. From (4), L_s is then about 5.8µH. From (2), the peak primary inductor current is 4.15A. From (3), the peak secondary inductor current is 16.6A.

RMS Inductor Currents

The RMS value of a periodic triangular pulse is:

$$I_{RMS} = I_p\sqrt{\frac{\tau}{3T}} \quad (9)$$

Where:

I_p is the peak value of the current

τ is the width of the base of the pulse

T is the period of the waveform

The RMS primary and secondary currents are then 1.3A and less than 7.44A respectively. At 500A/cm^2, the primary inductor should be wound with #24 or equivalent and the secondary inductor with #15 or equivalent.

Core Selection and Calculations

Inductance may be written as:

$$L = \frac{N\Phi}{I}$$

Where:

L is the inductance in Henries.

N is the number of turns of wire in the inductor.

Φ is the total flux linked by the N turns in Webers.

I is the current in the inductor in Amperes.

Since Φ is also equal to A_eB where A_e is the effective area of the inductor core (m^2) and B is the flux density (Tesla):

$$\overline{B} = \frac{L\overline{I}}{NA_e} \quad (10)$$

From the core data for the Philips EFD30 core:

$$A_e = 69\,mm^2 = 6.9\times10^{-5}\,m^2 \quad (11)$$

If B is limited to 250mT (approaching roll-off in the B-H curve), N_p must be 23 or more turns. If N_p is set to 24, then N_s is 6.

These cores are ordered specifying the gap in terms of nH/Turn^2 (the A_L value). Obtaining an inductance of 93µH from 24 turns requires an A_L of 161nH. Since an A_L of 150nH is a standard value, this is what will be used. Note that since the core is gapped, the remanent flux density in the core will be approximately reduced by the ratio of the un-gapped A_L to the gapped A_L. The un-gapped A_L for the EFD30 is about 2100 in 3C85 material. The remanent flux density in a 3C85 un-gapped core is

about 160mT at room temperature. Therefore the remanent flux density in the gapped core will be:

$$Brem_{gapped} \approx \frac{A_{L\,gapped}}{A_{L\,un-gapped}} Brem_{un-gapped} \quad (12)$$

$$= \frac{150}{2100} 160\,mT = 11.4\,mT$$

Since the saturation flux density of 3C85 material is well above 250mT, a flux swing of 250mT will not saturate the core with a remanent flux density of only 11.4mT.

Windings

The inductor in the schematic shows 4 separate windings. The primary inductor winding is wound from #24 magnet wire. The 2 turn winding that supplies the bootstrap power to the primary side of the circuit can be of practically any small gauge wire as the current level is low. In the prototype inductor this winding was wound with #30 wire simply because it was readily available. The primary side windings were placed side by side against the bobbin with a layer of kapton tape, 3M #5413, to isolate the high voltage primary inductor winding from the low voltage bootstrap winding.

The secondary side of the inductor shows two windings, the secondary inductor winding and a bootstrap winding for the secondary side electronics. The secondary inductor cannot be wound from (at least not easily and maintain creepage distances) from bundles of discrete wires or from litz and still fit the winding in the window of the EFD30 bobbin. Therefore, the secondary inductor was wound from foil. A 0.5 inch wide by 0.007 inch thick strip of copper foil was used. This gives a current density of about 330A/cm^2 in the winding. This low value of current density was used to help offset losses caused by the high number of layers in the winding. The secondary bootstrap winding was wound on top of the secondary inductor.

To satisfy insulation requirements, three layers of kapton tape were used between the primary side and secondary side windings.

The bootstrap windings in Figs. 2 and 3 are connected so that they will supply current when the main power switch is on, not off, as the secondary inductor will. This means that the voltage applied to the primary and secondary electronics will be equal to:

$$V_{boot} = \frac{N_{boot}}{N_p} V_{dc} - V_{diode} \quad (13)$$

For the primary side, the bootstrap voltage will be between 10.1 and 15.5 volts. Likewise, the secondary bootstrap voltage will be between 15.5 and 23.75 volts.

The prototype charger was built using two different inductors using different winding arrangements. One inductor had the primary winding on one layer, and the other sandwiched the secondary between a primary split between two layers. While both arrangements produce satisfactory results, the split primary does have lower leakage inductance and places less stress on the power switch at turn-off. In the prototype, the single layer primary produced leakage spikes that were high enough to make a 400V Vds mosfet a marginal choice. If the single layer primary is used, a 500V Vds mosfet would be a better choice for the power switch.

PRIMARY SIDE COMPONENT VALUES

Current Sensing and Feedback

To be certain that the flyback inductor never saturates, some resistor values on the primary side can be adjusted to limit the primary current to a level on the verge of saturation. If this level is picked to be 300mT (from Philips data for 3C85 material), the peak current (I_P) in the primary must be less than about 5.3A. To limit the current in L_P to 5.3A, the voltage at pin FB of the UCC3809 must be 1V when the current is 5.3A. When the feedback current through the opto-isolator is 0, the following condition must be satisfied:

$$5.3\,R_{CS} \frac{R_2 + R_1}{R_3 + R_2 + R_1} = 1.0 \quad (14)$$

In addition, to be certain that the secondary can command the minimum attainable pulse width, a voltage of 3.0V across R_1 should result in 1V at the UCC3809 FB pin with no current in the current sense resistor (R_{CS}). The value of R_{CS} is so small that it will be ignored in this computation. This gives:

$$3.0 \frac{R_3}{R_3 + R_2} = 1.0 \quad (15)$$

If R_3 is arbitrarily chosen as 1k, R_2 must be 2k. R_1 must be chosen with some consideration to the opto-isolator. The H11A817A has a current transfer ratio of 80% to 160% and is fairly linear over a diode current range of 2mA to 30mA. Picking R_1 to be 220Ω places the operating point of the opto-

isolator into its linear range over most of the operating range of the charger. R_{CS} is then 0.27Ω. The power dissipation in R_{CS} is just over 450mW at full load, so a 1W resistor is recommended here. The UCC3809 needs a capacitor at its FB pin to keep the inevitable current spikes through L_P from causing early pulse termination. Capacitor C_{ZB} serves this purpose in this application. A value of 220pF gives a time constant of about 0.15µs. This will catch the leading current spike noise pulses but still allow adequate current ramp sensing at 100kHz. C_{CS}, across the current sense resistor, also helps to attenuate the large leading current spikes caused by the forward peak rectifiers in the bootstrap power circuits. Some caution must be used when picking the values for C_{ZB} and C_{CS}. The larger the values, the more lag time that there will be when a fault condition is present at the output. On the other hand, picking the values too small can lead to premature pulse termination and erratic charger behavior. Also, the larger the value of C_{ZB}, the longer the minimum achievable pulse width will be.

Timing and Soft-start

The UCC3809 has fully programmable maximum on and minimum off times. The components RT1, RT2 and CT determine these times. Since τ_{on} is at most 2.97τs and the total period, T is 10µs the off time, τoff will be 7.03µs. From the UCC3809 datasheet:

$$\tau_{on} = 0.69 C_T R_{T1} \text{ and } \tau_{off} = 0.69 C_T R_{T2} \quad (16)$$

Picking C_T to be 1nF, R_{T1} is 4.32K and R_{T2} is 10.2K.

The softstart time is controlled by C_{SS}. C_{SS} is charged by a 6µA current source. As the SS pin on the UCC3809 goes from 0V to 0.7V, the output of the UCC3809 is inhibited. As the voltage goes from 0.7V to 1.7V, the duty cycle of the output is allowed to increase from 0 to its maximum value. A 47nF value for C_{SS} gives a soft start time of about 7.5ms. The bulk supply capacitor for the UCC3809 must be able to supply energy to the primary side circuitry while the SS pin makes the transition from 0V to 0.7V.

Other Components

R_4 provides the startup current for the UCC3809. This current must be at least 100µA at minimum line. A value of 470K will give 240µA at minimum line input voltage and maximum startup voltage for the UCC3809. C_1, the bulk filter capacitor, was chosen more for its ripple current handling capability and low ESR more than its capacitance. Capacitors C_2 and C_3 are filter caps for the UCC3809's power supply and reference. R_G is a low value resistor intended to prevent gate oscillations in the power mosfet. The block labeled EMI/RFI suppression in Fig. 2 is a typical suppression network. It was not implemented in the prototype but is shown for completeness.

SETTING CURRENT AND VOLTAGE LEVELS FOR THE UC3909

Charge Current Sense Resistor

The current sense amplifier in the UC3909 does not have the bandwidth to handle a 100kHz flyback current waveform. To get around this limitation, the signal from the current sense resistor was filtered with a simple R-C network (R_{SF1} and C_{SF}). The –3dB frequency of this filter was chosen to be 20kHz to have minimal effect on the feedback loop. Another resistor, R_{SF2}, was added to preserve the 2.3V bias point of the current sense amplifier. When adding a filter like this to an amplifier that has gain and biasing resistors already implemented in silicon, be careful not to significantly change the nominal gain of the amplifier. The reason for this is that the silicon resistors are closely ratio matched to provide an accurate gain, but vary significantly in absolute value. Larger values of filtering resistors introduce larger potential differences in the gain of the sense amplifier from one chip to the next and over temperature for any given chip.

The charge current sense resistor (R_S) should be chosen so that its power dissipation is within acceptable limits and the voltage presented to the current sense amplifier does not cause the amplifier to saturate. The current sense amplifier in the UC3909 is a differential amplifier with a fixed gain of 5, biased to a level of 2.3V. To prevent saturation, the maximum voltage across CA– and CA+ should be no more than 400mV. In this application, power dissipation was the determining factor for selection of R_{CS}. R_{CS} was chosen as 20mΩ and dissipates about 1.1W at maximum output current.

Bulk Current Setting

The bulk current is set by the values of R_{G1} and R_{G2}. When the charger is in the bulk charge state, the voltage error amplifier will be out of compliance and its output (VAO) will be at its positive rail (or nearly so) of 5V. The relevant circuit is shown in Fig. 4.

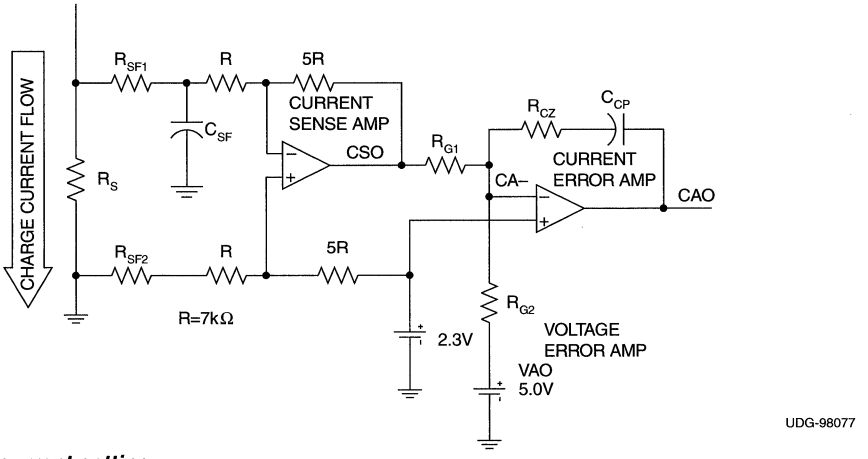

Figure 4. Bulk current setting.

For the current error amp to be in compliance, the voltage at pin CA– must be 2.3V. The desired bulk charging current was 4.0A. The average voltage across R_S is then:

$$V_{RS} = 4.0A \times 0.02\Omega = 80mV \qquad (17)$$

The voltage at the output of the current sense amplifier is then:

$$V_{CSO} = 2.3 - 5V_{RS} = 1.9V \qquad (18)$$

Summing currents at the CA– pin:

$$\frac{5 - 2.3}{R_{G2}} = \frac{4.0A \times 0.02\Omega \times 5}{R_{G1}} \qquad (19)$$

If R_{G2} is set to a value of 10.0k, then R_{G1} is 1.47k.

Trickle Current Setting

When the UC3909 is in the trickle charge state, the Voltage error amplifier output, VAO, goes into a high impedance state, and the trickle control current is directed to the CA– pin of the UC3909. The trickle control current is 5% of the current flowing out of the RSET pin on the UC3909. The trickle control current can only flow through R_{G1} since VAO is high impedance. Therefore, the trickle current will be:

$$I_{TRICKLE} = \frac{I_{TRICKLECONTROL}\, R_{G1}}{5\, R_S} \qquad (20)$$

Recall that the trickle current was to be set to 80mA. This current level will produce an average voltage of 2.292V at the CSO pin. The trickle control current through R_{G1} is then 5.4µA. The current out of the RSET pin is then 108µA. The voltage on the RSET pin is 2.3V, so the value of R_{SET} for 80mA trickle charge current is 21.5k.

Overcharge Taper Current

The overcharge taper current (I_{OCT}) is the current level the UC3909 looks for to make its transition from overcharge to float charge. The transition from overcharge to float charge takes place when the voltage on the OVCTAP pin rises above 2.3V. OVCTAP is the tap of a voltage divider from the VLOGIC to CSO pins, with R_{OVC1} and R_{OVC2} setting the divider ratio. The transition between charging modes takes place when:

$$\frac{5 - 2.3}{R_{OVC1}} = \frac{5I_{OCT}\, R_S}{R_{OVC2}} \qquad (21)$$

If R_{OVC2} is picked to be 100K, R_{OCV1} is 1.47k since I_{OCT} is 400mA.

Float Voltage Level

The float voltage is the voltage that the UC3909 will apply to the battery to maintain the battery's charge level after the overcharge period has ended. The float voltage (as well as the overcharge voltage and bulk charge threshold voltages) is determined by the resistors R_{S1}, R_{S2}, R_{S3} and R_{S4}. In the float state, the STATLV transistor (internal to the UC3909; see data sheet) is off. The float voltage is the voltage across the battery that will produce 2.3V at the VA– pin. Note that for all of the voltage thresholds, the reference voltage is adjusted by –3.9mV/°C while the reference for the

current thresholds is constant over temperature. The float voltage is then:

$$V_{FLOAT} = 2.3\frac{R_{S1} + R_{S2} + R_{S3}}{R_{S3}} \quad (22)$$

If R_{S3} is set to 10.0k, and V_{FLOAT} to 13.8V, the sum of R_{S1} and R_{S2} is 49.99k. The overcharge voltage level (V_{OC}) is the maximum voltage that will be applied to the battery when the charger is in the overcharge state. In this state, the STATLV transistor is on, and V_{OC} is the voltage that produces 2.3V at the VA– pin. V_{OC} is then:

$$V_{OC} = 2.3\frac{R_{S1} + R_{S2} + R_{S3} \,||\, R_{S4}}{R_{S3} \,||\, R_{S4}} \quad (23)$$

Knowing the sum of R_{S1} and R_{S2} is 49.99k, R_{S3} is 10.0k and V_{OC} is 14.8V, R_{S4} is found to be 115k. The bulk charge state is entered when the UC3909 senses that the voltage on its CHGENB pin goes above 2.3V. In the trickle and bulk charge states, the STATLV transistor is on, so the value of V_{CHENB} is then:

$$V_{CHGENB} = 2.3\frac{R_{S1} + R_{S2} + R_{S3} \,||\, R_{S4}}{R_{S2} + R_{S3} \,||\, R_{S4}} \quad (24)$$

Since the sum of R_{S1} and R_{S2}, and the values of R_{S3} and R_{S4}, are known, R_{S2} is 3.74k. From this, R_{S1} must be 46.4k.

Optocoupler LED Current Limit

R_E must be small enough that sufficient current can be put through the LED of the optocoupler to cause the collector on the optocoupler output to go to 3V. The resistance to ground at the collector of the optocoupler is about 205Ω. This means that the emitter current in the optocoupler must be at least 14.6mA. If the optocoupler is at the low end of the current transfer ratio distribution (80%, for the H11A817A), then the LED current must be at least 18.3mA. Allowing 0.7V for the b–e voltage on Q4, and 1.5V of headroom to help prevent saturation, the emitter voltage of Q4 will be 2.8V (5.0 – 0.7 – 1.5 = 2.8) maximum at 18.3mA. R_E is then 150Ω.

CURRENT CONTROL LOOP

There are several "components" in the current control feedback path. Fig. 5 details the feedback path. Component in this context refers to a piece of the overall transfer function, such as a resistor, which transforms a current into a voltage.

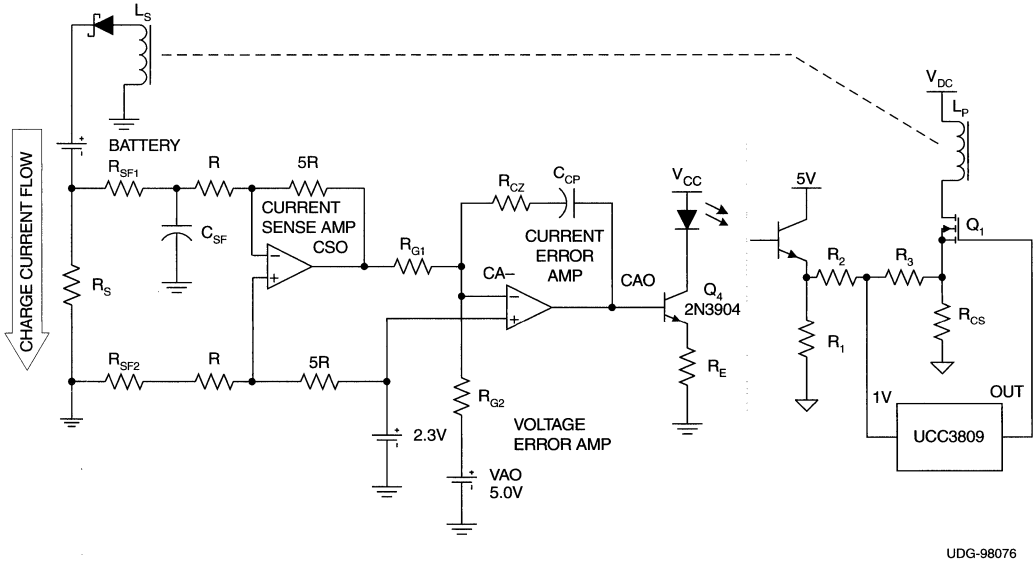

Figure 5. Current control loop components.

The individual components of the feedback path are:

1. Q_4 and R_E which converts V_{CAO} into I_{LED} in the optocoupler.
2. R_1, R_2, R_3, R_{CS} and the optocoupler, which convert I_{LED} into a peak primary inductor current, I_{LP}.
3. The coupled inductor which, along with the output voltage, converts I_{LP} into an average current through R_S.
4. R_S, R_{SF1} and C_{SF}, which converts the average output current into a voltage.
5. The current sense amplifier, which amplifies the voltage across C_{SF}.
6. The current error amplifier, which provides gain and phase compensation for the feedback loop.

These elements will be examined one by one to determine the overall loop characteristics.

Q_4 and R_E

Q_4 is configured as an emitter follower. For all practical purposes, the collector current and the emitter current are equal, and a one volt change in base voltage will produce a one volt change in emitter voltage. Since the emitter voltage and the emitter resistor determine the emitter current and hence the collector current, the gain of this stage is:

$$G_1 = \frac{1}{R_E} = \frac{1}{150} A/V \qquad (25)$$

R_1, R_2, R_3, R_{CS} and the Optocoupler

The optocoupler may have a current gain up to 160%. The current in the primary inductor is the current that results in 1V at the junction of resistors R_2 and R_3. Using the principle of superposition:

$$\left(I_C \bullet \left[R1 \| (R2+R3)\right] \bullet \frac{R_3}{R_2+R_3}\right) + \left(I_{L_P} \bullet R_{CS} \bullet \frac{R_2}{R_2+R_3}\right) = 1.0 \qquad (26)$$

This simplifies to:

$$I_{L_P} = \frac{R_2+R_3}{R_{CS}R_2} - I_C \frac{R_1(R_2+R_3)}{R_1+R_2+R_3} \bullet \frac{R_3}{R_{CS}R_2} \qquad (27)$$

The gain of this stage is the derivative of I_{LP} with respect to IC multiplied by the optocoupler gain or:

$$G_2 = -\frac{R_1(R_2+R_3)}{R_1+R_2+R_3} \bullet \frac{R_3}{R_{CS}R_2} \bullet 1.6 = -607 A/A \qquad (28)$$

Coupled Inductor and Output Voltage

The peak current in the secondary inductor is N_P/N_S times the peak current in the primary inductor. The secondary current waveform is triangular and has the average value, see Fig. 6:

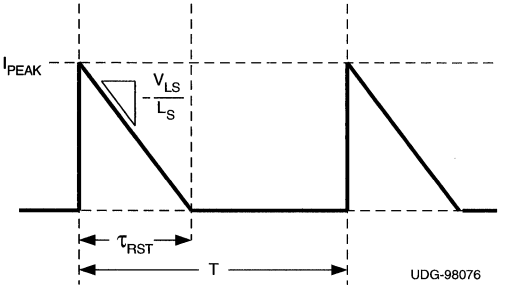

Figure 6. Secondary current waveform.

$$I_{L_S AVG} = \frac{\tau_{rst}}{2T} I_{L_S PEAK} \qquad (29)$$

But since:

$$I_{L_S PEAK} = \frac{N_p}{N_s} I_{L_P PEAK} \qquad (30)$$

and

$$\tau_{rst} = I_{L_S} \frac{V_{L_S}}{L_S} \qquad (31)$$

The average output current is then:

$$I_{L_S AVG} = \frac{1}{2T}\left(I_{L_S PEAK}\right)^2 \frac{L_S}{V_{L_S}} = \frac{1}{2T}\left(\frac{N_p}{N_s}\right)^2 \left(I_{L_P PEAK}\right)^2 \frac{L_S}{V_{L_S}} \qquad (32)$$

The gain of the stage is the derivative of the average secondary current with respect to the peak primary current. Differentiating the above yields:

$$G_3 = \frac{1}{T}\left(\frac{N_p}{N_s}\right)^2 \frac{L_S}{V_{L_S}} I_{L_P PEAK} \; {}^{A}/_{A} \qquad (33)$$

From this, it is seen that the gain depends upon what the load voltage and current are. This differentiation yields the gain of the coupled inductor because from a small signal standpoint, the battery voltage (and hence V_{LS}), switching frequency, turns ratio and secondary inductance are constant. The maximum value of the gain is the only value of interest since this will be the point at which the phase margin will be the lowest (in this circuit). If the battery voltage is 10.5V and the Schottky voltage is 0.5V, the I_{LP} that produces an average I_{LS} of 4.0A is 3.08A. This is the point where the current gain is the highest, at 2.6 A/A.

Current Sense Resistor and Filter

The transfer function of the sense resistor and filter network is:

$$G_4 = \frac{R_S}{1 + sR_{SF1}C_{SF}} \qquad (34)$$
$$= \frac{0.02}{1 + 7.5 \times 10^{-6} s} \; {}^{V}/_{A}$$

Current Sense Amplifier

The output of the current sense amplifier is:

$$V_{CSO} = 2.3 - 5\,V_{CSF} \qquad (35)$$

The gain of this stage is the derivative of V_{CSO} with respect to V_{RCS}. The gain G_5, is –5 V/V.

Total Current Loop Gain

The open loop gain of the current loop (without the current error amplifier) is the product of all of the G terms described above. G_{COL} in this case is 1.05 or 0.44dB, with a single pole at 20kHz.

Current Loop Compensation

Fig. 7 shows the uncompensated and compensated current loop gain characteristics. The compensation goal here is to provide unconditional stability in the loop and to roll the closed loop frequency response off at 1/10th of the switching frequency. To roll the closed loop response off at 10kHz, the open loop crossover frequency must be 10kHz. To do this requires that the current error amplifier have –0.44dB gain at crossover. Although not strictly necessary, a zero will be inserted in the current error amplifier response at 20 kHz to cancel the pole in the current sense filter. The transfer function of the current error amplifier is:

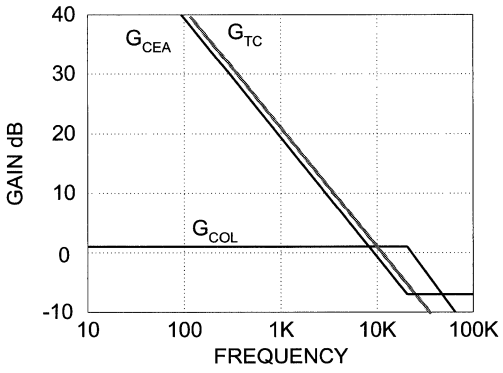

Figure 7. Current loop gain.

$$G(s) = \frac{1 + sR_{CZ}C_{CP}}{sR_{G1}C_{CP}} = G_{CEA} \qquad (36)$$

The R in this integrator has already been determined to be 1.47k (R_{G1}). This leaves the capacitor to set the low frequency gain characteristic. For the gain to be –0.44dB at 10kHz, the capacitor value must be around 10nF. The phase lag through the power stage is small in the frequency range of interest and the origin pole of the current error amplifier contributes only 90° to the loop. The phase lag of the current sense filter is offset by the zero in the current error amplifier response. This means that the loop is unconditionally stable with near 90° of phase margin.

VOLTAGE CONTROL LOOP

The voltage control loop is shown in Fig. 8. The nature of this circuit is such that in the trickle and bulk charge states, the voltage control loop is open. At some point during the overcharge state the voltage loop closes or comes into compliance. For the remainder of the overcharge state and the float charge state, the voltage loop (made up of the resistor divider string R_{S1} through R_{S4}, the voltage error amp and R_{VG} is an outer control loop around the current loop.

The open loop response of the voltage loop is equal to the closed loop current loop response multiplied by the output impedance and the gain of the elements of the voltage loop. In other words:

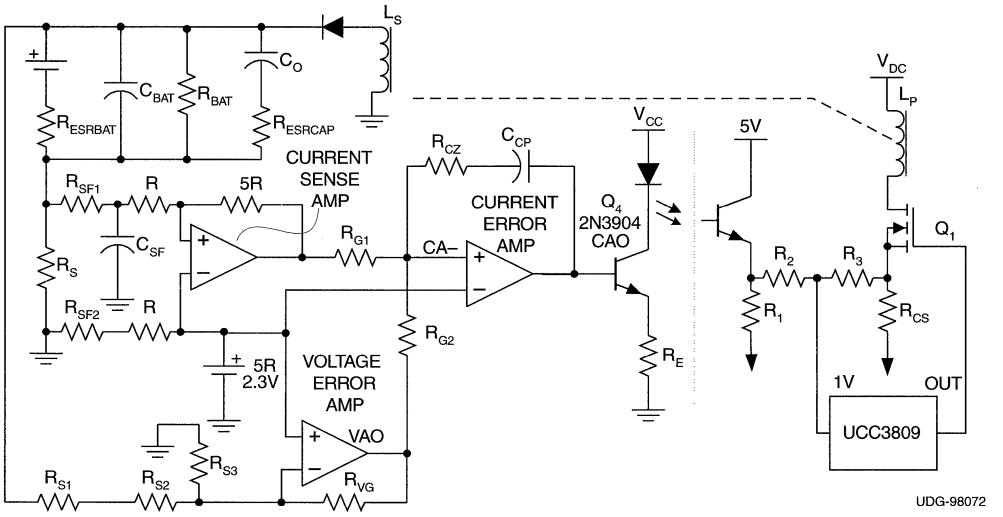

Figure 8. Voltage control loop.

$$G_{VOL} = G_{CCL} Z_L G_{DIV} \frac{R_{G1}}{R_{G2}} G_{VEA} \quad (37)$$

Where:

G_{VOL} is the open loop voltage transfer function

G_{CCL} is the closed loop current transfer function

Z_L is the load impedance

G_{DIV} is the gain of the battery voltage divider looked at from the VA- pin

G_{VEA} is the transfer function of the voltage error amplifier.

The R_{G1}/R_{G2} term is simply the summing ratio of the current sense amplifier output and the voltage error amplifier output. The closed loop current response (change in output current for a given change in current sense amplifier output) is given by:

$$G_{CCL} = \left(\frac{1}{G_4 G_5}\right)\left(\frac{G_{CEA} G_5 G_4 G_3 G_2 G_1}{G_{CEA} G_5 G_4 G_3 G_2 G_1 + 1}\right) \approx \frac{7.143 \times 10^5}{s + 7.143 \times 10^4} \quad (38)$$

The load impedance is difficult to characterize and is greatly dependent upon the battery being used. The battery is a complex device to model and will exhibit parametric shifts depending upon variables like temperature, charge state, age and history. According to the battery manufacturer, R_{ESRBAT}, C_{BATT} and R_{BATT} vary considerably depending upon what the condition of the battery is. To insure that the voltage loop will remain stable, it was assumed that the equivalent load of the battery, filter capacitor and anything else that may be connected to the charger has an extremely low frequency pole. The frequency of this pole is assumed to be much less than the crossover frequency of the voltage loop. This will contribute 90° to the phase lag of G_{VOL} at whatever the crossover frequency turns out to be.

The divider gain (G_{DIV}), is equal to:

$$G_{DIV} = \frac{R_{S3}}{R_{S1} + R_{S2} + R_{S3}} = 0.166 \quad (39)$$

The open loop voltage transfer function for this application is then:

$$G_{VOL} = \frac{1.743 \times 10^4}{7.143 \times 10^4 + s} Z_L G_{VEA} \quad (40)$$

Ignoring the Z_L and G_{VEA} terms, the phase shift of this circuit is 45° at the current control loop crossover frequency (10kHz), and about 22.5° at 3.2kHz. The voltage error amplifier was chosen to be a straight gain amplifier with no complex feedback in order to avoid the additional phase shift that comes with introducing more poles into the system. With the phase shift of the load taken to be 90°, the voltage loop should have a crossover frequency below 3.2kHz to maintain good phase margin. At 3.2kHz, the open loop gain of the voltage control loop is:

$$|G_{VOL}|_{f=3200} = |Z_L\, G_{VEA}|_{f=3200} - 12.6dB \quad (41)$$

Conversations with the battery manufacturer suggested that charging impedance could range from 250mΩ to 10mΩ (almost strictly capacitive) at 3.2kHz. The filter capacitor in the charger is 5600µF with an ESR of less than 13mΩ. This results in a total Z_L of 8mΩ to 15mΩ. The gain of the voltage error amplifier must be less than 49dB in order to insure that the control loop will crossover at less than 3.2kHz. The gain of the amplifier was set at 36dB. Testing on the prototype charger showed no signs of instability in the voltage control loop. While it is not known what the exact impedance on the battery is, the above approach resulted in a robust and stable charger.

OTHER ISSUES

Line Isolation

The transformer design presented here will provide at least $3750V_{RMS}$ of isolation and 8mm of creepage from the primary to the secondary. This is adequate for some applications, but not for others. Check with the regulatory standards for the type of product being built to find out if this isolation level is adequate. If more isolation is required, a core with a larger winding window will have to be used since this design fills the window of the EFD30 almost completely.

Higher power

This paper presents a general scheme for controlling a primary side PWM from an isolated UC3909. The particular PWM used here is a single output device. However, for higher power requirements, 200W, 500W, 1kW and beyond, there is no reason that a higher performance single output PWM or dual output PWM could not be used with suitable design adaptations. At much higher current levels, it may be advantageous to use a small value shunt for current sensing along with an additional amplifier to boost the signal level. If the topology is changed to a forward buck type, the current sense amplifier in the UC3909 will be useful at higher switching frequencies without the aid of an input averaging filter.

Disconnection of Load and Minimum Output Power

If it is possible that the load (battery in this case) could be disconnected from the charger while the charger is powered from the ac mains, the output voltage will run away. A means of controlling output voltage must be supplied if this is the case. The reason for this is that even though the UC3909 would be commanding zero pulse width, the UCC3809 will give a minimum pulse width based upon the values of components R_{CS}, C_{CS}, R_3, R_2, and C_{ZB}. The minimum pulse width arises from the fact that the UCC3809 discharges C_{ZB} through an internal FET when the oscillator starts its down ramp. The internal FET is turned off when the oscillator starts its up ramp and sends an output pulse. Since the output pulse will only terminate when the voltage at FB on the UCC3809 reaches 1V (or when the oscillator again starts its down ramp), the minimum pulse width is determined by the time that it takes to charge C_{ZB} to 1V.

A means of getting a handle on the minimum pulse width can be seen by referring to Fig. 9. When minimum pulse width is being commanded by the UC3909, it is assumed that the voltage across the current sense resistor will not have a significant impact on the time necessary to charge C_{ZB} to 1V. The only source available is the current through the opto-isolator. The voltage V1 is the current out of the opto-isolator multiplied by the equivalent resistance seen at the emitter of the opto-isolator. When this voltage is known, the minimum pulse width is approximately:

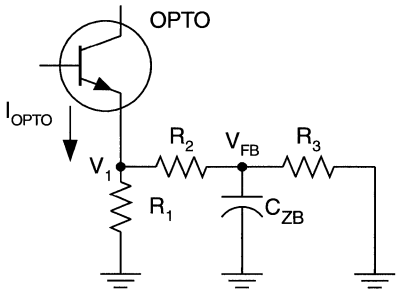

Figure 9. Minimum pulse width determination.

$$\tau_{on} = -ln\left(1 - \frac{R_2 + R_3}{\overline{V_1} \bullet R_3}\right)\frac{C_{ZB}\, R_2\, R_3}{R_2 + R_3} \quad (42)$$

This application circuit was not designed to operate with a disconnected load. Enough load must be applied to dissipate the minimum power output that the circuit will supply at the highest input line voltage (a DC rail of 195V). The particular battery used here was an adequate load to dissipate this power. Minimum pulse width can be reduced by using a smaller C_{ZB}, at the expense of noise immunity or by increasing the ratio of R_3 to R_2. This last solution will affect the feedback loops somewhat.

As a means of controlling the output voltage, a 5W 15V zener diode at the output would work nicely. The STAT0 and STAT1 pins could even be decoded to switch the diode into the circuit only when the charger goes into float mode. This would guarantee that the over charge voltage would not cause a low threshold diode to start conducting and overheat. Alternatively, a dummy load resistor could be placed across the charger output that would dissipate the minimum output power at the minimum temperature compensated float voltage. It will almost certainly be necessary to use the STAT0 and STAT1 pins to switch the resistor into the circuit only when the UC3909 is in the float mode. Otherwise, the dummy load would be applied to the battery and discharge it when the charger is not powered from the line.

Connection of Loads That Bypass the Current Sense Resistor

This technique can be useful if properly applied. The charger current sense loop will adjust the output to a point that will supply the battery with the selected charging current, regardless of what current the load requires. There are some caveats here though. First, the charger power stage must be able to handle the bulk charging current of the battery as well as the maximum current that the load will draw. Second, the load will add a pole into the current control loop, which can complicate the design of the feedback, especially in the voltage control loop. Third, and probably most importantly, the inherent current limiting effect of the current control loop will not be active if a fault occurs at the load. Some other means of over-current protection must be supplied.

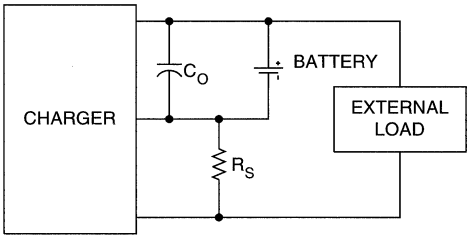

Figure 10. Alternate external load connection.

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Design Note

UCC3956 Switch Mode Lithium-Ion Battery Charger Controller, Evaluation Board, Schematic, and List of Materials

The UCC3956 Evaluation Kit allows the design engineer to evaluate the operation and performance of the Lithium-Ion Battery Charger Controller. The controller is designed to implement a DC to DC buck converter and features a four state charge control algorithm that enables the charger to safely and rapidly restore the battery pack to full capacity. The evaluation board is initially configured to charge a 2-Cell 1200mA Hour battery pack, however, the board can be modified to address a variety of applications. The UCC3956 Data Sheet contains detailed information about the use of the controller.

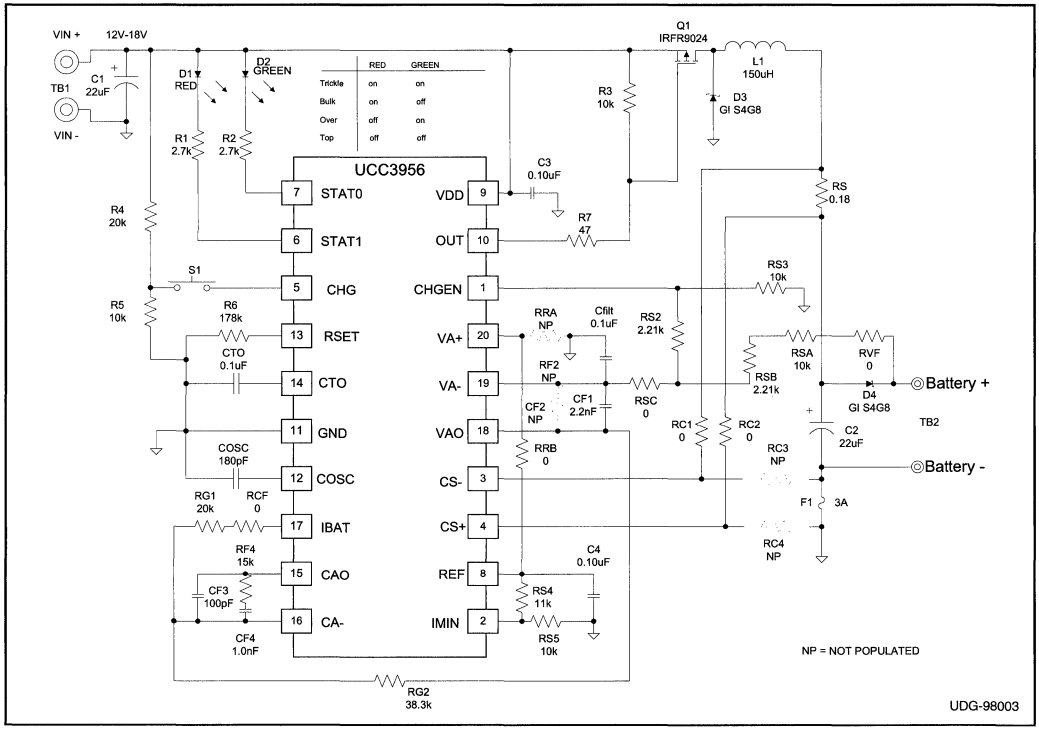

Figure 1. Evaluation Board Schematic

Buck Power Stage

The evaluation board charger schematic is shown in Figure 1. Although the IC will operate with a V_{DD} between 7 and 18 volts, the two cell design will require at least 12 volts to be able to charge the pack to 8.20 volts. To ensure low noise on the board, 22µF Tantalum capacitors (C1,C2) are added to the input and output terminals, while decoupling capacitors (C3, C4) are placed on the controller's reference and V_{DD}. The PWM buck power stage consists of L1, Q1, and D3. The charger is designed to deliver 1.2 amps of bulk current (1C charge rate) and L1 is sized to provide continuous current with 25% ripple. A 3 amp fuse (F1) prevents destructive current from being applied to the battery in the event of a fault, while diode D4 blocks reverse battery current.

Current Sense Circuitry

Inductor current is sensed across RS with a differential amplifier at the CS+ and CS– pins (notice current flows from CS– to CS+). The evaluation board has been configured with a "high side" current sense resistor, which has a DC operating voltage a diode drop above the positive terminal of the pack. This configuration allows the negative terminal of the pack to be referenced to circuit ground. High side current sensing is selected by populating RC1 and RC2 with zero ohm jumpers and by not populating (NP) RC3 and RC4. Certain applications may require a low side current sense solution. Examples include designs where the battery voltage exceeds the controller's V_{DD} rating, or where a high side sense resistor would have excessive common mode noise. Low side current sensing can be implemented by swapping F1 and RS. In this case, RC3 and RC4 would have zero ohm jumpers, while RC1 and RC2 would not be populated.

Feedback Components

The feedback design of the 2 cell charger is presented in the application section of the data sheet and will not be repeated here. Resistors RCF and RVF are initially populated with zero ohm jumpers and are assumed to be zero ohms in the equations that follow. In the evaluation of the charger's control loops, these jumpers can be replaced with low value resistors (50 ohm) to facilitate the use of a network analyzer. The current amplifier network for the two cell design consists of a pole-zero-pole response provided by CF3, CF4, and RF4, resulting in a crossover frequency around 10kHz. The voltage amplifier network consists of a single pole response, provided by CF1, with a crossover frequency of 2kHz. Components CF2 and RF2 are not populated, but allow the voltage feedback network to be modified.

Oscillator Frequency

The PWM frequency is determined by Equation 1. A 180pF COSC and a 178k RSET yield a switching frequency of 100kHz.

$$Frequency = \frac{3.475}{(COSC + 20pF) \bullet RSET} \quad (1)$$

Charge State Logic

A charge cycle is initiated by pressing the momentary push button switch S1. Resistors R4 and R5 keep the CHG pin voltage between 3 and 6 volts when S1 is closed. The controller has two status output pins, STAT0 and STAT1, which drive LEDs to indicate the states of the charger. An LED decode chart is printed on the evaluation board.

- **TR:** The trickle state is indicated when a reduced current is being delivered by the charger because the pack voltage is depleted below the trickle threshold. This state will also be indicated when power is initially applied to the board before a charge cycle is initiated.
- **BLK:** The constant current or bulk state is indicted when bulk current is being delivered by the charger and the pack voltage is between the trickle and the over-charge thresholds.
- **OVER:** The constant voltage or over-charge state is indicated when the pack voltage reaches 95% of its final value and the over-charge timer is initiated. Bulk current will continue being applied by the charger until the pack voltage reaches 100% of its final voltage, at which time the charge current will begin to decrease.
- **TOP:** The top-off state is indicated when the battery is at its final voltage and its current is below the top-off threshold set at the IMIN pin. The top-off indication notifies the user that the pack is near full capacity (maybe 95%) and is ready to be used. If the battery is not pulled from the charger, it will continue charging until the over-charge timer expires. When the over-charge timer expires, the LEDs will indicate the top-off state until a new charge cycle is initiated or power is cycled on the board.

Programming the Trickle State

The charger transitions from the trickle to bulk charge state when the CHGEN pin equals 2.05 volts. The corresponding pack voltage is given in equation 2. With RSA = RS3 = 10.0K and RSB = RS2 = 2.21K, the charger will remain in the trickle state with a pack voltage less than 5.0 volts.

$$V_{PACK\_TRICKLE} = \left(\frac{RSA + RSB + RS2 + RS3}{RS3}\right) \bullet 2.05 \quad (2)$$

The programmed level of the trickle current is expressed in Equation 3. A trickle current of 60mA (C/20) is programmed with RG1=20K, RSET=178K and RS=0.18 ohm.

$$I_{TRICKLE} = \frac{RG1}{10 \bullet RSET \bullet RS} \quad (3)$$

Programming Bulk Current

Bulk current is set by the resistor values at the input to the current error amplifier and the current sense resistor as expressed in Equation 4. A bulk current of 1.2A is programmed with RG1=20K, RG2=38.3K and RS=0.18 ohm.

$$I_{BULK} = \frac{2.05 \bullet RG1}{5 \bullet RG2 \bullet RS} \quad (4)$$

Programming the Over Charge State

The controller indicates the over charge state and timer is initiated when the battery is at 95% of its final voltage (7.80V in this case). The over charge time period is programmed with CTO expressed in equation 5 (minutes). A capacitance of 0.1uF results in a period of 80 minutes. A capacitor in the pF range can be used when evaluating the timer's functionality (i.e. a 220pF CTO will give a 10 second time-out period).

$$TIMEOUT = 4550 \bullet CTO \bullet RSET \quad (5)$$

The charger will transition from a constant current to a constant voltage mode of operation when the voltage amplifier comes into regulation. This occurs when the voltage at the inverting input (VA–) of the amplifier reaches the value set at the non-inverting input (VA+). The voltage at VA+ is set by resistors RRA and RRB as expressed in equation 6. In the case of the 2 cell charger, RRA is not populated and RRB is a zero ohm jumper, yielding a VA+ voltage equal to the 4.1V reference.

$$V+ = 4.1 \bullet \left(\frac{RRA}{RRA + RRB} \right) \quad (6)$$

The final pack voltage is programmed by a resistor divider tied to the VA– input (the resistor values are also used to set the trickle threshold). Equation 7 gives the formula for the final pack voltage. Capacitor Cfilt is connected to the VA– input to suppress a voltage spike that occurs when the charger transitions from the trickle to bulk state, preventing the overcharge timer from being initiated prematurely. A final voltage of 8.2V is achieved by using the resistor values of Figure 1.

$$V_{PACK\_FINAL} = \left(\frac{RSA + RSB + RS2 + RS3}{RS2 + RS3} \right) \bullet V + \quad (7)$$

Programming the Top-off Current Level

The top-off state is indicated when the pack has reached its final voltage and the current to the pack has been reduced below the level set by equation 8. With RS4=11k, RS3=10k, and RS=0.18 ohms, a current level of 120mA (C/10) will turn both LEDs off, indicating the battery is near full charge. Again, if the user does not pull the battery from the charger, it will continue to charge until the timer expires, restoring 100% capacity.

$$I_{TOP\_OFF} = \frac{2.05 \bullet \left(1 - 2 \left[\frac{RS5}{RS4 + RS5} \right] \right)}{5 \bullet RS} \quad (8)$$

Configuring the Charger to Address Different Pack Voltages

A single cell design requires a final pack voltage of 4.1 volts. This can be accomplished with two different approaches. The first approach is to leave VA+ connected to the 4.1V reference and replace RSA and RSB with zero ohm jumpers. An impedance, required for the voltage amplifier network, is provided by populating RSC with a 10K resistor. Resistor values for RS2 and RS3 would need to be changed to set the trickle threshold. The second approach is to maintain the two-cell design values for RSA, RSB and RSC, and to place equal value resistors at RRA and RRB, setting VA+ to 2.05 volts.

Three and four cell designs will require a higher value for RSA+RSB. Since a four cell design will have a final pack voltage of 16.8V, the input voltage of the charger may exceed the maximum rating of the controller. In this case, a level shifting circuit will be needed to drive Q1 and a Zener regulator will be needed at V_{DD}.

For more complete information, pin descriptions and specifications for the UCC3956, please refer to the datasheet or contact your Unitrode Field Applications Engineer.

Reference Designator	Part Description	Distributor or Manufacturer Part Number
C1, C2	22µF Tantalum SMD-7343	Allied 213-6137
C3, C4, CFILT, CTO	0.1µF Ceramic SMD-1206	Digikey PCC104BCT-ND
CF1	2200pF Ceramic SMD-1206	Digikey PCC222BCT-ND
CF3	100pF Ceramic SMD-1206	Digikey PCC101CCT-ND
CF4	1000pF Ceramic SMD-1206	Digikey PCC102BCT-ND
COSC	180pF Ceramic SMD-0805	Digikey PCC181CGCT-ND
D1	Red LED	Digikey HLMP-1700QT-ND
D2	Green LED	Digikey HLMP-1790QT-ND
D3, D4	3A Schottky Diode SMD	General Instruments SS34
F1	3A Slow Blow Fuse SMD-7343	Digikey FF1169CT-ND
L1 (provided)	150µH Inductor, 1.5A	Coilcraft DO-5022P-154
(Alternate for lower current)	150µH Inductor, 1.0A	Coilcraft DO-3316P-154
(Alternate for low noise)	150µH Toridal Inductor, 1.7A	Pulse Engineering (619)674-8100 PE-25645
Q1 (provided)	P-channel 0.28 RDSON SMD	International Rect. IRFR9024
(Alternate thru hole)	P-channel 0.28 Rdson TO-220	International Rect. IRF9Z24
R1,R2	2.67k Resistor SMD-1206	Digikey P2.76KFCT-ND
R3, R5, RSA, RS3, RS5	10.0k Resistor SMD-1206	Digikey P10.0KFCT-ND
R4, RG1	20.0k Resistor SMD-1206	Digikey P20.0KFCT-ND
R6	178k Resistor SMD-1206	Digikey P178KFCT-ND
R7	47Ω Resistor SMD-1206	Digikey P47FCT-ND
RCF, RVF, RRB, RSC, RC1, RC2	0Ω Jumper SMD-1206	Mouser 71-CRCW1206-0
RF4	15.0k Resistor SMD-1206	Digikey P15.0KFCT-ND
RG2	38.3k Resistor SMD-1206	Digikey P38.3KFCT-ND
RS2, RSB	2.21k Resistor SMD-1206	Digikey P2.21KFCT-ND
RS	0.18Ω Resistor SMD-2512	Digikey P.18VCT-ND
RS4	11.0k Resistor SMD-1206	Digikey P11.0KFCT-ND
S1	Momentary Push Switch	Digikey CKN9002CT-ND
TB1, TB2	Terminal Blocks	Digikey ED1601-ND
U1	Charger Controller	Unitrode UCC3965 SOIC-20
CF2, RC3, RC4, RRA, RF2	Not populated	

Table 1. Parts list for the 2 Cell Charger in Figure 1.

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UNITRODE
APPLICATION NOTE

Simple Switchmode Lead-Acid Battery Charger

Abstract

Lead-acid batteries are finding considerable use as both primary and backup power sources. For complete battery utilization, the charger circuit must charge the battery to full capacity, while minimizing over-charging for extended battery life. Since battery capacity varies with temperature, the charger must vary the amount of charge with temperature to realize maximum capacity and life. Simple, low cost circuits are currently available for small, low power requirements, while more complex solutions are affordable only on larger more expensive systems. Often the greatest challenge is in designing mid-size, mid-price systems, where obtaining optimum performance at moderate cost and complexity may be nearly impossible without dedicated integrated circuits. This paper describes a compact lead-acid battery charger, which achieves high efficiency at low cost by utilizing switchmode power circuitry, and provides high charging accuracy by employing a dedicated control IC. The circuit described can be easily adapted to lower or higher power applications.

Lead-Acid Basics

Lead-acid battery chargers typically have two tasks to accomplish. The first is to restore capacity, often as quickly as practical. The second is to maintain capacity by compensating for self discharge. In both instances optimum operation requires accurate sensing of battery voltage and temperature.

When a typical lead-acid cell is charged, lead sulfate is converted to lead on the battery's negative plate and lead dioxide on the positive plate. Over-charge reactions begin when the majority of lead sulfate has been converted, typically resulting in the generation of hydrogen and oxygen gas. At moderate charge rates most of the hydrogen and oxygen will recombine in sealed batteries. In unsealed batteries however, dehydration will occur.

The onset of over-charge can be detected by monitoring battery voltage. Figure 1 shows battery voltage verses percent of previous discharge capacity returned at various charge rates. Over charge reactions are indicated by the sharp rise in cell voltage. The point at which over-charge reactions begin is dependent on charge rate, and as charge rate is increased, the percentage of returned capacity at the onset of over-charge diminishes. For over-charge to coincide with 100% return of capacity, the charge rate must typically be less than C/1 (1/100 amps of its amp-hour capacity). At high charge rates, controlled over-charging is typically

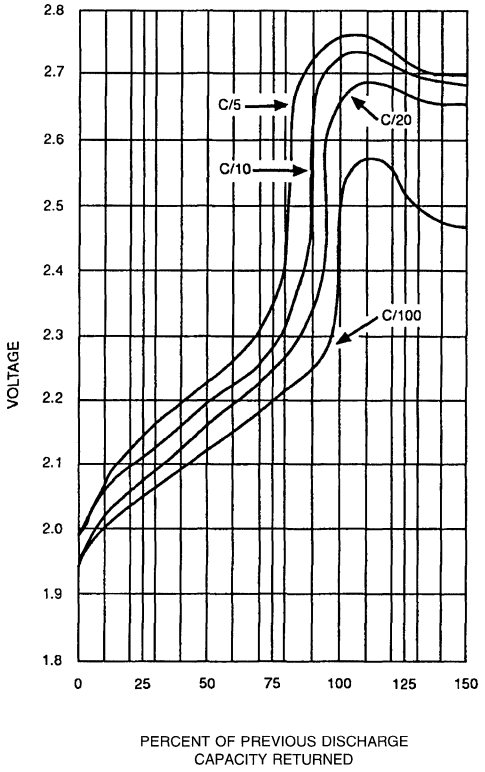

Figure 1. Over-charge reactions begin earlier (indicated by the sharp rise in cell voltage) when charge rate is increased. (Reprinted with the permission of Gates Energy Products, Inc.)

employed with sealed batteries to return full capacity as quickly as possible.

To maintain capacity on a fully charged battery, a constant voltage is applied. The voltage must be high enough to compensate for self discharge, yet not too high as to cause excessive over-charging. While simply maintaining a fixed output voltage is a relatively simple function, the battery's temperature coefficient of -3.9mV/degree C per cell adds complication. If battery temperature is not compensated for, loss of capacity will occur below the nominal design temperature, and over-charging with degradation in life will occur at elevated temperature.

Charging Algorithm

To satisfy the aforementioned requirements and thus provide maximum battery capacity and life, a charging algorithm which breaks the charging cycle down into four states is employed. The charging algorithm is illustrated by the charger state diagram shown in figure 2. Assuming a fully discharged battery, the charger sequences through the states as follows:

1. Trickle-charge If the battery voltage is below a predetermined threshold, indicative of a very deep discharge or one or more shorted cells, a small trickle current is applied to bring the battery voltage up to a level corresponding to near zero capacity (typically 1.7V/cell@ 25 degrees C). Trickle charging at low battery voltages prevents the charger from delivering high currents into a short as well as reducing excessive out-gassing when a shorted cell is present. Note that as battery voltage increases, detection of a shorted cell becomes more difficult.
2. Bulk-charge Once the trickle-charge threshold is exceeded the charger transitions into the bulk-charge state. During this time full current is delivered to the battery and the majority of its capacity is restored.
3. Over-charge Controlled over charging follows bulk-charging to restore full capacity in a minimum amount of time. The over-charge voltage is dependent on the bulk-charge rate as illustrated by figure 1. Note that on unsealed batteries minimal over-charging should be employed to minimize out-gassing and subsequent dehydration. Initially overcharge current is the same as bulk-charge current. As the over-charge voltage is approached, the charge current diminishes. Over-charge is terminated when the current reduces to a low value, typically one-tenth the bulk charge rate.
4. Float-Charge To maintain full capacity a fixed voltage is applied to the battery. The charger will deliver whatever current is necessary to sustain the float voltage and compensate for leakage current. When a load is applied to the battery, the charger will supply the majority of the current up to the bulk-charge current level. It will remain in the float state until the battery voltage drops to 90% of the float voltage, at which point operation will revert to the bulk charge state.

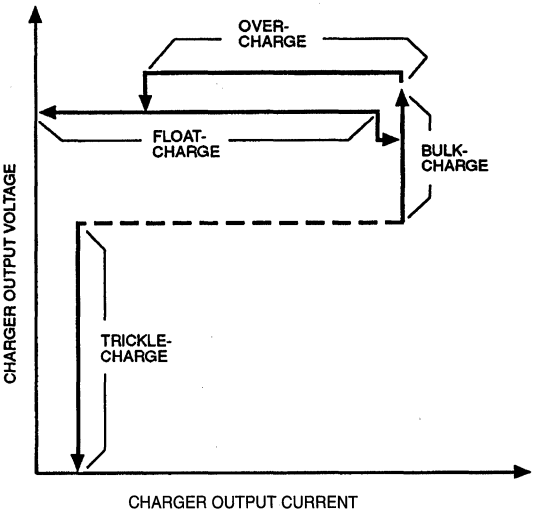

Figure 2. The charging algorithm is broken down into four states

Charger Circuit Design

There are many possible circuit configurations which will provide the necessary control and output charging current. For efficient operation, particularly at higher output currents, switching power circuitry is preferred. To minimize cost as well as complexity each IC used must provide as much functionality as possible. A circuit topology was chosen which utilizes two special purpose ICs and a general purpose op-amp to provide all of the control

functions, while a discrete MOSFET output stage handles the power. The circuit design is modular to simplify modification for different application requirements.

The charger circuit can be divided into three basic blocks. The first is the voltage loop control and state control logic which executes the control algorithm while providing temperature compensation. The second is the switchmode controller which regulates the current to the battery as commanded by the voltage loop control and state control logic. The third is the output power stage which is sized to efficiently deliver the charging current.

Voltage Loop Control and State Control Logic

Initially designed for charging small lead-acid batteries using a linear pass transistor for current control, the UC3906 directly implements the voltage loop control and state control logic while providing the appropriate temperature compensation. The block diagram of the UC3906 is shown in figure 3.

Battery voltage is monitored with a resistor divider string. This network establishes the float voltage, the over-charge voltage, and the trickle-charge threshold voltage by comparing to the precision temperature compensated reference. Since temperature is monitored on chip it is critical that the battery and the UC3906 are in close proximity, and

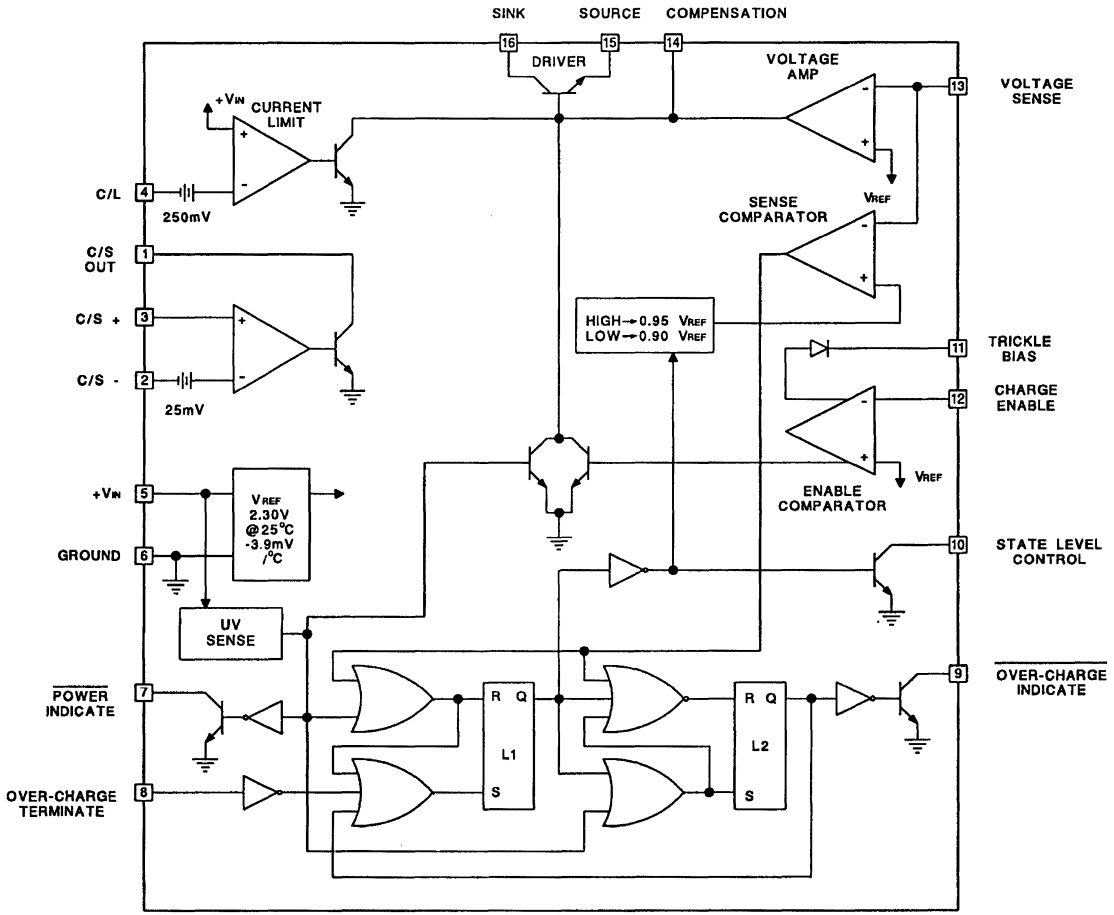

Figure 3. UC3906 Lead-Acid Battery Charger block diagram

that self-heating or heating from other components is minimized.

The differential current sense comparator is used to terminate over-charging and transition to the float state. The voltage amplifier provides gain and compensation for the voltage loop. The UC3906 is covered in detail in reference [3].

Switchmode Current Source

The charging algorithm places great demands on the current loop. during bulk charge full current must be supplied, yet during the float state the current draw may be only a few milliamps. This equates to a dynamic range in excess of 60 dB which can be very difficult to achieve with common peak current mode techniques. The wide dynamic range also requires operation with both continuous and discontinuous inductor current, potentially adding complication to voltage loop stabilization. Although load resistors can be employed to reduce the required dynamic range, their use can significantly degrade efficiency, particularly while in the float state. Note that a high value load resistor (10 k) is employed to assure operation down to zero output current and to provide a discharge path for the output capacitor. Additionally, to provide precise bulk and trickle-charge current levels the closed current loop transconductance must be accurate. Average current feedback will circumvent these potential problems, and is the key to a successful implementation of the switching current source for this application.

Figure 4 shows the basic implementation of average current feedback. While slightly more complicated than typical peak current mode control schemes, average current feedback offers several critical performance enhancements. The high gain of the error amplifier at lower frequencies provides high closed current loop accuracy and accommodates the large output stage nonlinearity which occurs when the inductor current becomes discontinuous. Good switching spike noise immunity is inherent with this technique permitting stable operation at narrow duty cycles.

A UC3823 PWM controller shown in figure 5 was chosen for the current loop control circuit for several reasons. First and most importantly it is capable of operating linearly from very small duty cycles to near

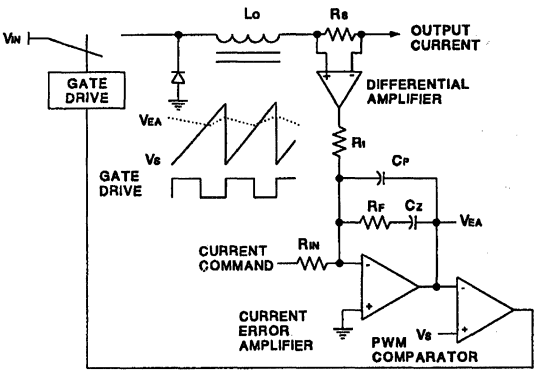

Figure 4. Average Current Feedback Loop

100% duty cycle. Secondly the error amplifier bandwidth and configuration are well suited to the average current loop's requirements. Additionally, the output driver affords a simple interface to most discrete output power stages.

A separate op-amp configured as a differential amplifier senses the output current and level shifts the signal to the appropriate voltage. The offset and common mode rejection of this amplifier are the major source of current loop error.

Output Power Stage

To simplify development a simple buck regulator output stage was used. For further simplicity the high-side switch is implemented using a direct coupled P-channel MOSFET. A switched current sink provides gate charge, turning the MOSFET on while a zener diode limits the gate to source voltage to 12 volts. A second emitter switched current sink drives a PNP which removes gate charge, turning the MOSFET off. Undoubtedly this output stage is suitable for many applications, although higher power capability and efficiency can be achieved using N-channel devices. A relatively low value output inductor was chosen to minimize size and cost since operation in the discontinuous current mode is of no concern with average current feedback. Output ripple voltage is also not critical so the output capacitor was selected for ripple current capability. High frequency ringing caused by circuit parasitics is damped with a small RC snubber across the catch rectifier. A rectifier in series with the output

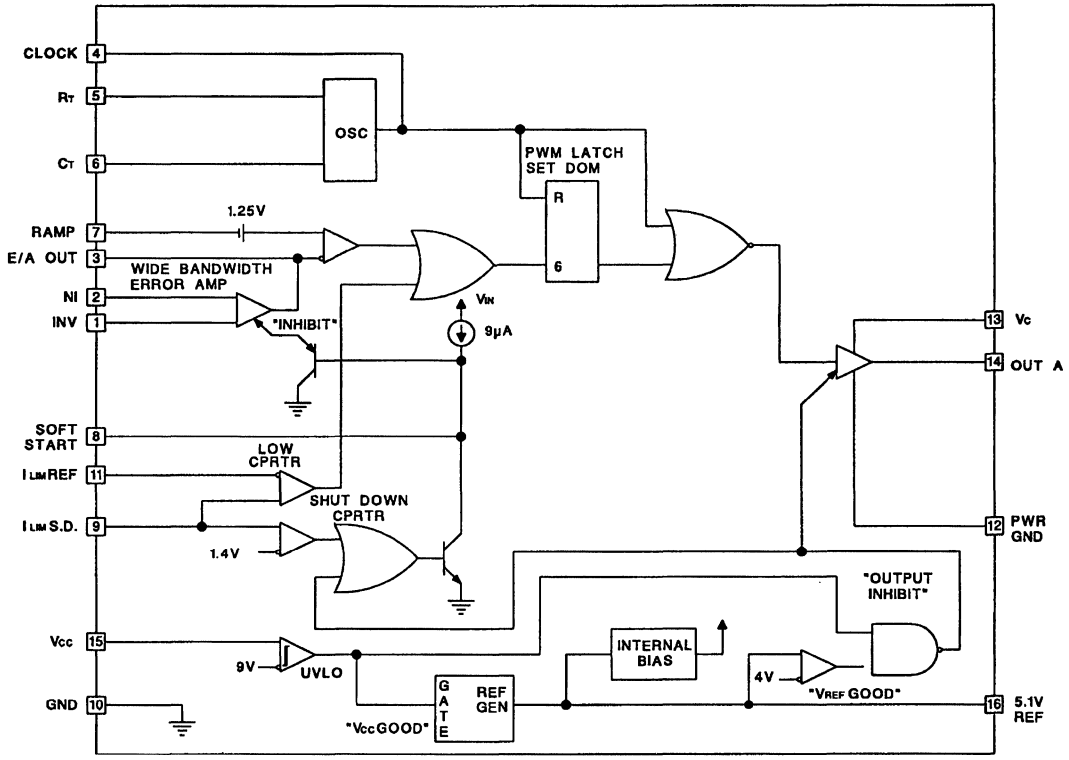

Figure 5. UC3823 High speed PWM Controller Block Diagram

prevents the battery from back driving the charger when input power is disconnected.

Complete Charger Circuit

A complete schematic for the switch-mode charger is shown in figure 6. Control circuit power is supplied from an emitter follower off a zener shunt regulator. The PWM frequency is set to 100 kHz as a reasonable compromise between output filter component size and switching loss. Output current is sensed in the battery return lead to minimize common mode voltage errors. This arrangement also allows direct current sensing for pulse by pulse current limiting adding further protection during abnormal conditions. The differential amplifier is set to a gain of 5 with the output signal referenced to the UC3823s 5.1 V reference.

The current feedback signal is summed with the current command signal at the error amplifier's inverting input. To accommodate worst case offset in both the error amplifier and the differential amplifier and allow zero output current, the non-inverting input of the error amplifier is biased 130 mV below the 5.1 V reference. Trickle bias is accomplished by injecting a small current into the differential amplifier's negative op-amp input, thus causing a proportional output current to balance the loop. Additionally, a 100 pF capacitor across the PWM comparator inputs enhances noise immunity, particularly at low duty cycles.

For maximum control and float voltage accuracy, the UC3906s ground is connected to the battery's negative terminal, thereby rejecting the current sense resistors voltage drop. The internal emitter follower output transistor interfaces to the current source as illustrated in figure 7. The voltage amplifier drives the output current command signal. The current command signal is limited by clamping the voltage amplifier output through a diode to 4.2 V. The clamp also prevents the emitter follower from

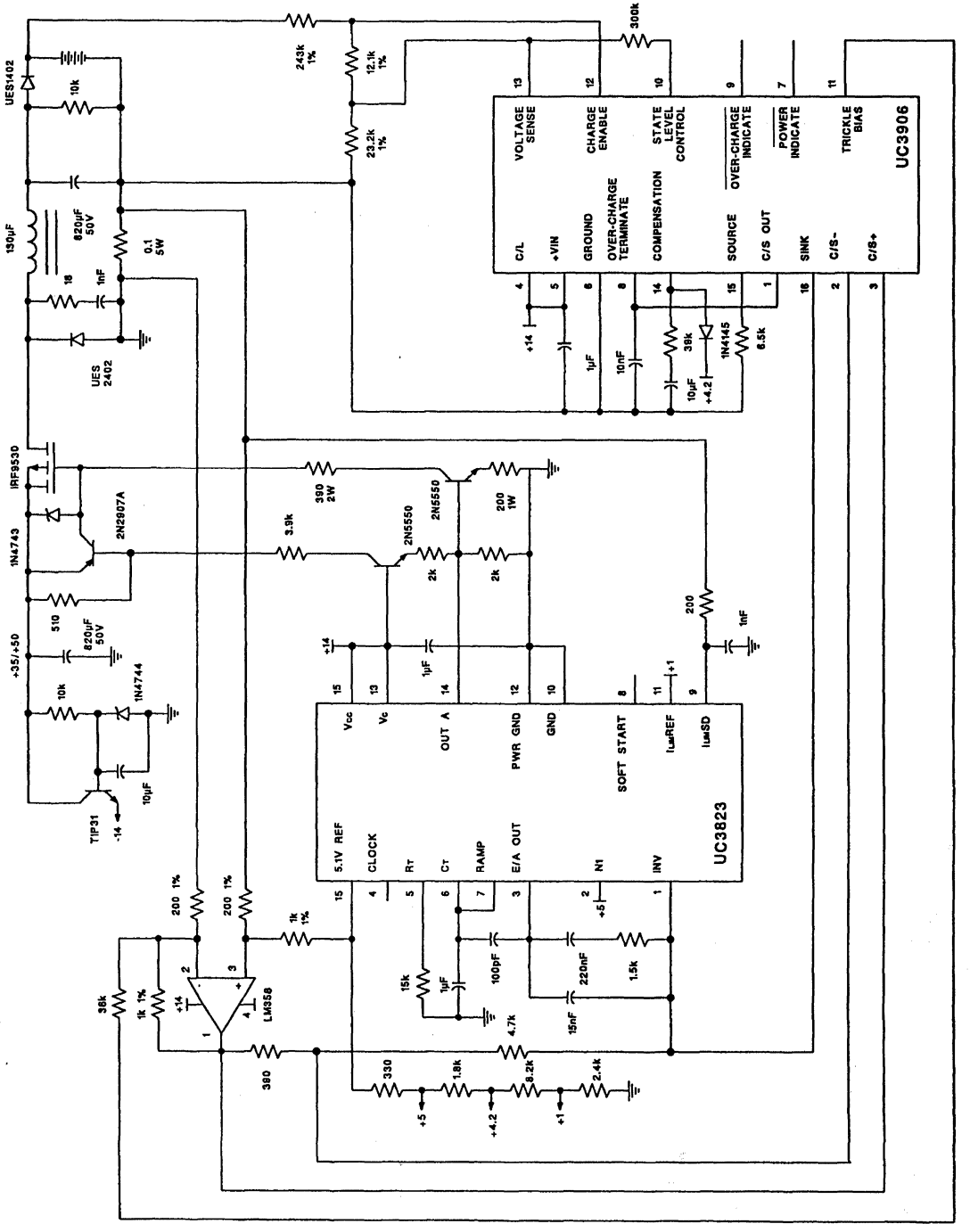

Figure 6. Switchmode Lead-Acid Battery charger schematic

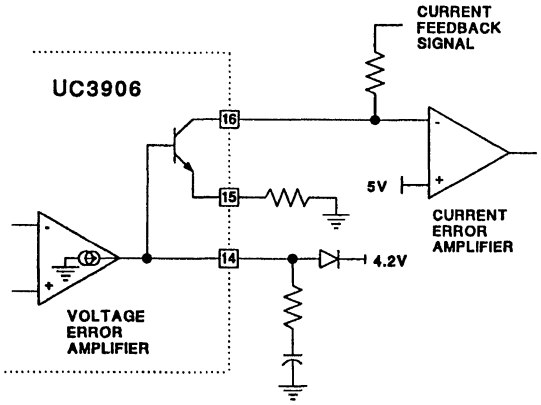

Figure 7. The UC3906's output transistor provides the interface to the switchmode current source.

saturating which would cause a large difference between collector and emitter currents due to excessive base drive.

Battery voltage is sensed by the resistor divider string, with the values shown for a typical **24** V **(12** cell) application. Other battery voltages are easily accommodated by simply changing the divider values using the procedure presented in the UC3906 data sheet, although changes in input voltage may require modification of the output circuit and the control circuit power supply. The resistor divider establishes all of the state transitions with the exception of over-charge terminate, which is determined by detecting when the output current has tapered off to approximately one-tenth the bulk charge level. This is accomplished by the UC3906s current sense comparator which senses the appropriately scaled signal from the differential amplifier output.

Current and Voltage Loop Compensation

The charger circuit implements a two loop control system with the current loop operating inside the voltage loop. During trickle-charge, bulk-charge and the beginning of over-charge the voltage loop is saturated and the current loop is essentially driven from a fixed reference.

With continuous inductor current the control to output gain of the current loop shown in figure 4 exhibits a single pole response from the output inductor. The error amplifier gain at the switching frequency is set such that the amplified inductor current down-slope is less than the oscillator-ramp up-slope as seen by the PWM comparator. By setting the two slopes equal under worst case conditions (at maximum output voltage) maximum closed loop bandwidth is achieved without subharmonic oscillation.

Placing a zero below the minimum loop crossover frequency significantly boosts low frequency gain while a pole placed above the maximum crossover frequency enhances noise immunity. Note that since loop response is not particularly critical for battery charging, conservative compensation with plenty of phase margin is normally employed.

When inductor current becomes discontinuous, the power circuit gain suddenly drops, requiring large duty cycle changes to significantly effect output current. The single pole characteristic of continuous inductor current with its 90 degree phase lag disappears. The current loop becomes more stable, but less responsive. Fortunately the high gain of the error amplifier easily provides the large duty cycle changes necessary to accommodate changes in output current, thereby maintaining good average current regulation.

The block diagram of the voltage loop is shown in figure 8. With an inner transconductance loop the control to output gain of the voltage loop exhibits a single pole response from the output capacitor and equivalent load resistance. While it may initially appear that a simple fixed gain on the voltage amplifier would provide suitable loop compensation, further examination shows a severe drop in voltage gain at high loads, which would drastically reduce DC accuracy. A zero is placed in the voltage amplifier's transfer function to boost low frequency gain and therefore restore DC accuracy.

The current loop's single pole response above its crossover frequency cancels the output stage zero resulting from the output capacitor's capacitance and ESR. Note again that since wide bandwidth is not required for battery charging, the voltage loop crossover frequency is well below both the current loop's pole and the output capacitor's zero. Low leakage capacitors must be used for the compensation network to maintain high DC gain

since the voltage amplifier is a transconductance type. Loop stabilization is covered extensively in references [1] and [2].

Charger Performance Summary

The charger circuit properly executes the charging algorithm, exhibiting stable operation regardless of battery conditions including an open circuit load. The circuit was tested with 6, 12 and 24 V batteries by modifying only the battery voltage sense divider. As would be expected, circuit efficiency was best at high battery voltage, approaching 85% while bulk-charging a 24 V battery with a 40 V input supply voltage.

An analysis of circuit losses indicates several areas where efficiency could be improved. Any accuracy and offset improvement in the differential amplifier will allow a corresponding decrease in current sense resistor value and hence dissipation, while maintaining the same overall current loop accuracy. Replacing the output blocking rectifier with a Schottky would save a few watts if the Schottky's leakage could be tolerated. Further improvement could be made in that area by using a relay to disconnect the charger when input power is removed. A more conservative inductor design with less resistance would save a little over one watt. As expected, the greatest losses occur in the output switch. A lower on resistance FET and a higher peak current gate drive to reduce switching losses could save more than 5 watts. Incorporating a few of these improvements will easily increase circuit efficiency to greater than 90%.

Alternate Circuit Configurations

While the charger circuit as designed may be suitable for many applications, a few modifications should satisfy the majority of additional requirements. Higher voltage batteries can be charged by designing a higher voltage output stage. N-channel MOSFETs are preferable for cost and efficiency reasons, but are more difficult to drive than P-channels. Fortunately, the remainder of the circuit will require minimal modification.

Some applications may require both the battery and charger to share a common ground and thus prohibit current sensing in the batteries negative return. The differential amplifier can sense current at the inductor output if tighter tolerance resistors to improve CMRR are used. While this simple modification renders a suitable signal for closing the current loop, another current sense signal referenced to ground must be developed for pulse by pulse current limiting. This signal is most easily derived by using a PNP level shift transistor, connecting the base to the 5.1 V reference and the emitter through a resistor to the differential amplifier output.

At higher battery voltages it may be desirable to float with a current rather than a voltage. Varying self-discharge rates of individual cells in high voltage batteries causes inevitable differences in cell charge levels. By employing a float current and applying a small continuous overcharge, variation of charge between cells is minimized. Precise output at float current levels places great demands on current loop accuracy, and will add unnecessary expense to the current sensing circuitry. A more cost effective alternative is to use a fixed linear current source which should be small and inexpensive considering the very low output current.

Thus far the input supply has not been addressed and is assumed to be from a voltage required elsewhere in the system or from a typical line frequency transformer, rectify bridge and filter capacitor. This may represent more than half the cost of the charger, and is certainly the majority of its size and weight. An obvious alternative is to replace the buck output section with a transformer coupled output, taking advantage of the switching control circuit already present. Buck derived circuits such as forward, half-bridge and full-bridge easily interface with the existing design, however resonant and flyback circuits are also applicable. A small (0.75 W) auxiliary supply will be required to power the control circuitry since the modulator will output zero at times, prohibiting the use of a bootstrap winding commonly used on switching power supplies. This

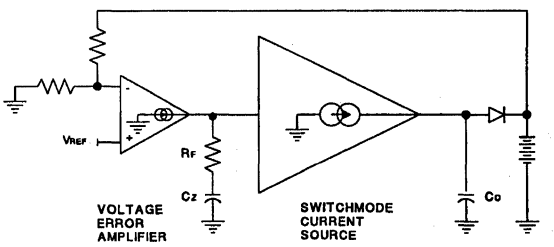

Figure 8. Voltage Control Loop block diagram

approach is particularly cost effective for stand-alone applications, allowing the design of a compact, light weight, high performance charger.

Summary

A practical switchmode lead acid battery charger circuit has been presented which incorporates all of the features necessary to assure long battery life with rapid charging capability. By utilizing special function ICs, component count is minimized, reducing system cost and complexity. With the circuit as presented, or with its many possible variations, designers need no longer compromise charging performance and battery life to achieve a cost effective system.

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IMPLEMENTING MULTI-STATE CHARGE ALGORITHM WITH THE UC3909 SWITCH-MODE LEAD-ACID BATTERY CHARGER CONTROLLER

INTRODUCTION

Applications of lead-acid batteries for primary as well as backup power sources has been increased significantly. The reasons behind this growth are the continuously improving battery technology which provides higher and higher power densities, and the increased demand for wireless operation of different electronic devices and tools. Manufacturers of these equipment are frequently challenged to provide solutions for quick and efficient recharge of the cells and to maximize the capacity and life of the battery.

Although the task sounds simple, satisfying the various requirements associated with charging and maintaining lead-acid batteries often requires considerable intelligence from the battery charger circuit. The implementation of a well optimized charging process requires complex control circuitry, such as microprocessors, DSP chips or state machine type of controllers. Usually, these solutions require custom components, and significant hardware and software development time. The cost of these solutions are penalized, by the higher cost and software of the digital controller, interfacing to the analog part of the circuit, in addition to the increased part count and consequently higher manufacturing expense.

This Application Note will introduce a new, dedicated analog controller. The UC3909 Switchmode Lead-Acid Battery Charger integrated circuit provides a low cost solution to battery charging, without sacrificing the performance of the system.

Additionally, the paper will guide users, whose primary expertise is not switchmode power supply design, how to devise state of the art, multi-state battery charger, using the new IC. The step by step instructions incorporated in this Application Note will provide exact component values, reducing the time of the paper design to merely a few minutes.

BASICS OF LEAD-ACID BATTERIES

In order to efficiently discuss battery properties, some of the common terms used in the battery industry have to be defined.

Ampere-Hour (Ah) - is a measurement of electric charge computed as the integral product of current (in Amperes) and time (in hours).

Capacity - is the ability of the battery to store and discharge a given quantity of current over a specified period of time. The capacity of the battery is expressed in Ampere-Hours (Ah). A cell's capacity is a function of the discharge current and usually increases with lower current levels. The capacity of the battery listed in the datasheet usually corresponds to the measured capacity at C/10 discharge rate.

C Rate - is the charge or discharge current of the battery expressed in multiples of the rated capacity. For example, a 2.5Ah cell will provide 250mA for 10 hours. The C rate in this particular case is C/10. In the real world, however, a cell does not maintain the same rated capacity at all C rates.

Self Discharge - is the loss of useful capacity of a cell on storage due to internal chemical action.

Deep Discharge - is the discharge of the battery below the specified cutoff voltage, typically 1.7V-1.9V per cell at 25°C depending on the C rate, before the battery is recharged. It happens usually upon withdrawal at least 80% of the rated capacity of the cells.

Constant Voltage Charge - is a charging technique during which the voltage across the battery terminals is regulated while the charge current varies according to the state of charge of the battery.

Constant Current Charge - is a charging method during which the current through the battery is maintained at a steady state value while the cell

voltages will vary according to the state of charge of the battery.

Trickle-Charge - is a constant current charge of the battery. In this mode, a low current, typically in the range of C/100 or lower is applied to the battery to raise the voltage to the deep discharge threshold (cutoff voltage), a level corresponding to near zero capacity. The trickle charge current has to be determined to assure continuous operation without damaging the cells.

Bulk-Charge - is also a constant current mode of operation, to quickly replenish the charge to the battery. The battery manufacturers define the bulk charge current as the maximum charge current allowed for the cells. It can be applied to the batteries if their voltage is between the deep discharge and the over-charge limits. Typical bulk charge current varies between C/5 and 2·C depending on manufacturers and battery types.

Over-Charge - the term describes the chemical reactions taking place when the majority of the lead-sulfate has already been converted to lead, resulting in the generation of hydrogen and oxygen. The beginning of the over-charge reactions depends on the C rate, and it is indicated by the sharp rise in cell voltage as illustrated in Figure 1.

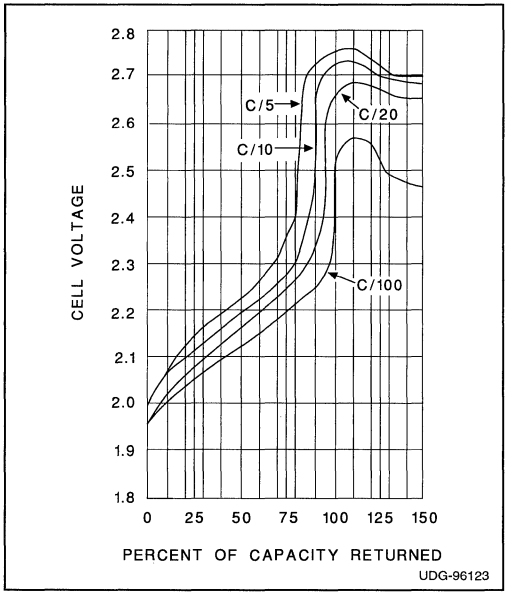

Figure 1. Typical over-charge characteristic at different charge rates.

For over-charge to coincide with the 100% return of capacity, the charge rate must be less than C/100. For higher charge rates, over-charge of lead-acid batteries is necessary to return the full capacity.

In a controlled **over-charge mode**, a constant voltage is applied. Its value is typically set between 2.45 V/cell and 2.65 V/cell, again depending on the C rate. Improper selection of the over-charge voltage will eventually result in dehydration of the battery and reducing its useful life span.

Float-Charge - is a constant voltage charge of the battery, after completing the charging process. This voltage maintains the capacity of the battery against self discharge. Even though providing a fixed output voltage is a simple task, to find the precise value of the float voltage has a profound effect on battery performance. For instance, 5% deviation from the optimum cell voltage in float mode, could result approximately 30% difference in the available capacity of the battery. Furthermore, the battery's temperature coefficient of typically -3.9mV/°C per cell, adds complication. If the float voltage is not compensated according to the battery temperature, loss of capacity will occur below the design temperature, and uncontrolled over-charging with degradation in life will happen at elevated temperature.

BATTERY CHARGER BASICS

What differentiates a battery charger from a conventional power supply is the capability to satisfy the unique requirements of the battery. Lead-acid battery chargers typically have two tasks to accomplish. The most important is to restore capacity as quickly as possible. The second one is to maintain capacity by compensating for self discharge and ambient temperature variations.

There are two fundamentally different charging methods for lead-acid batteries. In constant voltage charge, the voltage across the battery terminals is constant and the condition of the battery determines the charge current. Constant voltage charge is most popular in float mode application. The charging process is usually terminated after a certain time limit is reached.

Another technique is constant current charge, which is often used in cyclic applications because it recharges the battery in a relatively short time. As opposed to constant voltage charge, the constant current charge automatically equalizes the charge in the series cells. There are many varia-

tions of the two basic methods, well suited for switchmode battery charger circuits. Considering that well designed switchmode power converters are inherently current limited, the combination of constant current and constant voltage charge is an obvious choice.

The best performance of the lead-acid cells can be achieved using a four state charge algorithm. This method integrates the advantages of the constant current charge to quickly and safely recharge and equalize the lead-acid cells, with the constant voltage charge to perform controlled over-charge and to retain the battery's full charge capacity in float mode applications. The carefully tailored charging procedure maximizes the capacity and life expectancy of the battery.

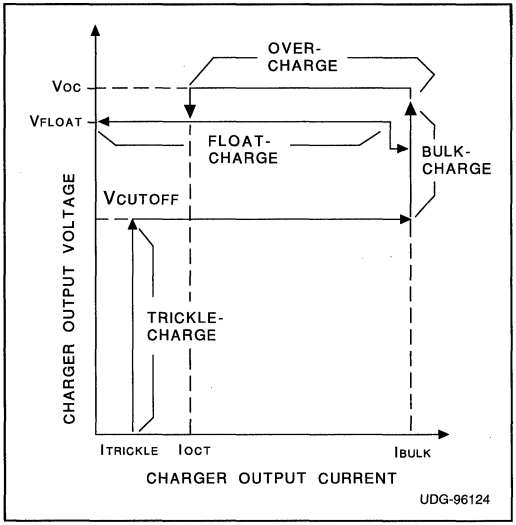

Figure 2. Four-state charge algorithm

The four states of the charger's operation are trickle charge, bulk charge, over-charge and float charge, as they are shown in Figure 2. Assuming a fully discharged battery, the charger sequences through the states as follows:

State 1: Trickle Charge

If the battery voltage is below the cutoff voltage, the charger will apply the preset trickle charge current ($I_{TRICKLE}$). In case of a healthy battery, as the charge is slowly restored, the voltage will increase towards the nominal range until it reaches the cutoff voltage. At that point the charger will advance to the next state, bulk charging.

In case of a damaged battery, e.g. one or more cells are shorted or the internal leakage current of the battery is increased above the trickle current value, the low value of the trickle charge current ensures safe operation of the system. In this case the battery voltage will stay below the deep discharge threshold (V_{CUTOFF}) preventing the charger from proceeding to the bulk charge mode.

When the battery voltage is above the cutoff voltage at the beginning of the charge cycle, the trickle charge state is skipped and the charger starts with the bulk charge mode.

State 2: Bulk Charge

In this mode the maximum allowable current (I_{BULK}) charges the battery. During this time, the majority of the battery capacity is restored as quickly as possible. The bulk charge mode is terminated when the battery voltage reaches the over-charge voltage level (V_{OC}).

State 3: Over-Charge

Controlled over-charge follows bulk charging to restore full capacity in a minimum amount of time. During the over-charge period, the battery voltage is regulated. The initial current value equals the bulk charge current, and as the battery approaches its full capacity the charge current tapers off. When the charge current becomes sufficiently low (I_{OCT}), the charging process is essentially finished and the charger switches over to float charge. The current threshold, I_{OCT}, is user programmable and is typically equals $I_{BULK}/5$.

State 4: Float Charge

This mode is only applicable when the battery is used as a backup power source. The charger will maintain full capacity of the battery by applying a temperature compensated DC voltage across its terminals. In the float mode, the charger will deliver whatever current is needed to compensate for self discharge and might supply the prospective load up to the bulk charge current level. If the primary power source is lost or if the load current exceeds the bulk current limit, the battery will supply the load current. When the battery voltage drops to 90% of the desired float voltage, the operation will revert to the bulk charge state.

The ultimate lead-acid battery charger will combine the above described four state charge algorithm, and particularly at higher output currents, a switchmode power converter. The implementation of a charger of this type usually requires several

integrated circuits. To minimize cost as well as complexity, a new integrated circuit had been developed to provide as much functionality and design flexibility as possible, while achieving these requirements.

THE UC3909 BLOCK DIAGRAM

The UC3909 Switchmode Lead-Acid Battery Charger controller combines the precision sensing and control of battery voltage and current, logic to sequence the charger through its various modes of operation, and the control and supervisory functions of a switching power supply. The integrated circuit comprises of two major sections. A dashed line shown in the middle of Figure 3 divides the circuit into two functional subsections. The PWM control circuit is commanded by the charge state logic depending on the condition of the battery.

The charge state logic is shown in the lower right corner of the block diagram, which is composed of several digital gates. It sequences the charger through the four possible states of operation depending on the battery voltage. Information about the actual operating mode of the charger is also provided. The status information can be easily interfaced to any logic family due to the open collector structure of the outputs of pin STAT0, STAT1, and STATLV. (See the datasheet for detailed pin descriptions.)

The precision voltage and current sensing circuits are shown in the lower left corner of the block diagram. The battery voltage is compared to the temperature compensated reference voltage by the voltage error amplifier and charge enable comparator. Accurate sensing of the charge current is achieved by the uncommitted current sense amplifier, connected to the CS+, CS- and CSO pins. The use of this amplifier requires a low value resistor for current measurement. Output regulation is accomplished by the current error amplifier. Its inverting and noninverting inputs are connected to the output of the current sense and voltage error amplifiers through external resistors. The output of the current error amplifier produces the appropriate control parameter for the PWM controller.

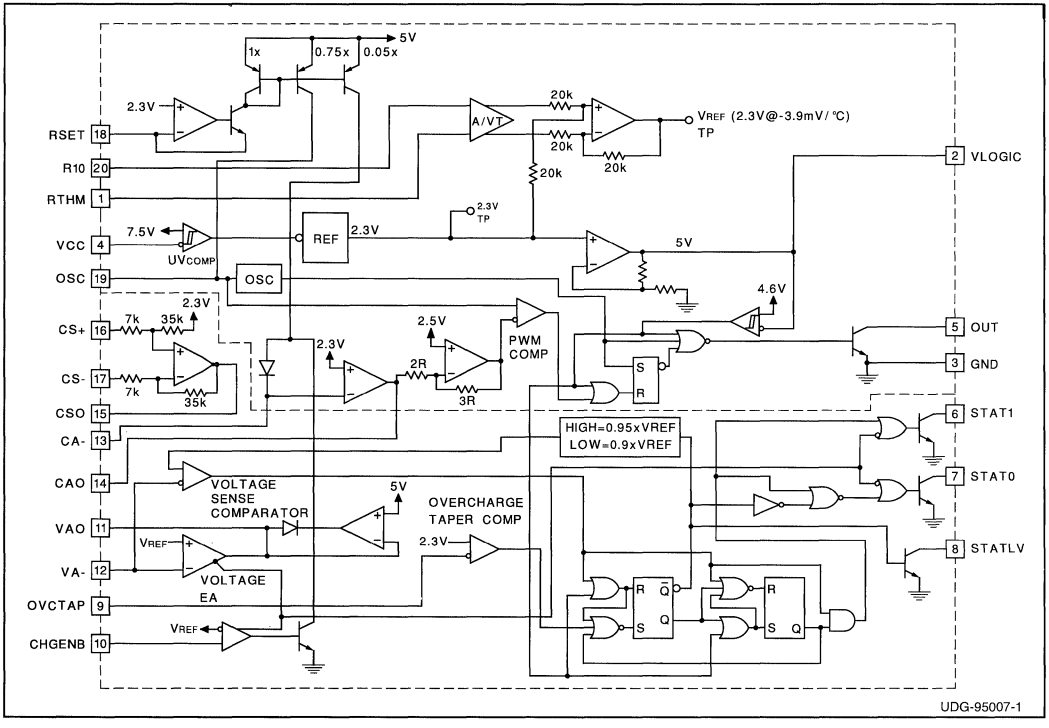

Figure 3. UC3909 Block Diagram

The PWM control section consists of a fast comparator, clock generator, latch and an open collector drive stage. The comparator circuit compares the output of the current error amplifier to the sawtooth derived from the timing capacitor waveform. A latch is set by the clock and reset by the comparator circuit in every switching cycle modulating the pulse width appearing at the output of the controller. This modulation of the output pulse width makes output voltage and output current regulation possible.

The remaining part of the block diagram performs numerous housekeeping functions, such as undervoltage lockout, internal bias and reference generation, temperature sensor linearization and compensation of the internal voltage reference according to the battery temperature.

UC3909 DEMONSTRATION CIRCUIT

To illustrate the capabilities of the new controller, a full featured, switchmode battery charger circuit has been developed and built for evaluation purposes.

The power stage is based on a simple buck topology, reflecting the most common solution used in battery chargers today. The buck converter offers size reduction and high efficiency, two important advantages of switchmode power conversion. Practical output power of this converter type is below 500W. In the case of off-line chargers, line isolation can be provided by 60Hz isolation transformer. For higher power levels the buck converter could be easily replaced by other isolated, buck derived topologies, like any variation of the forward or bridge type converters. Using one of these isolated conversion techniques will eliminate the bulky 60Hz transformer by integrating the isolation into the high frequency power stage. The design procedure, that will be presented in this Application Note for the buck configuration, can be easily adapted to the other power converters.

The usual elements of the buck converter can be recognized in Figure 4. They are Q1, D2, L1 and C5. Other components in the power stage pertain to additional, application specific requirements. D1 prevents the discharge of the battery by the con-

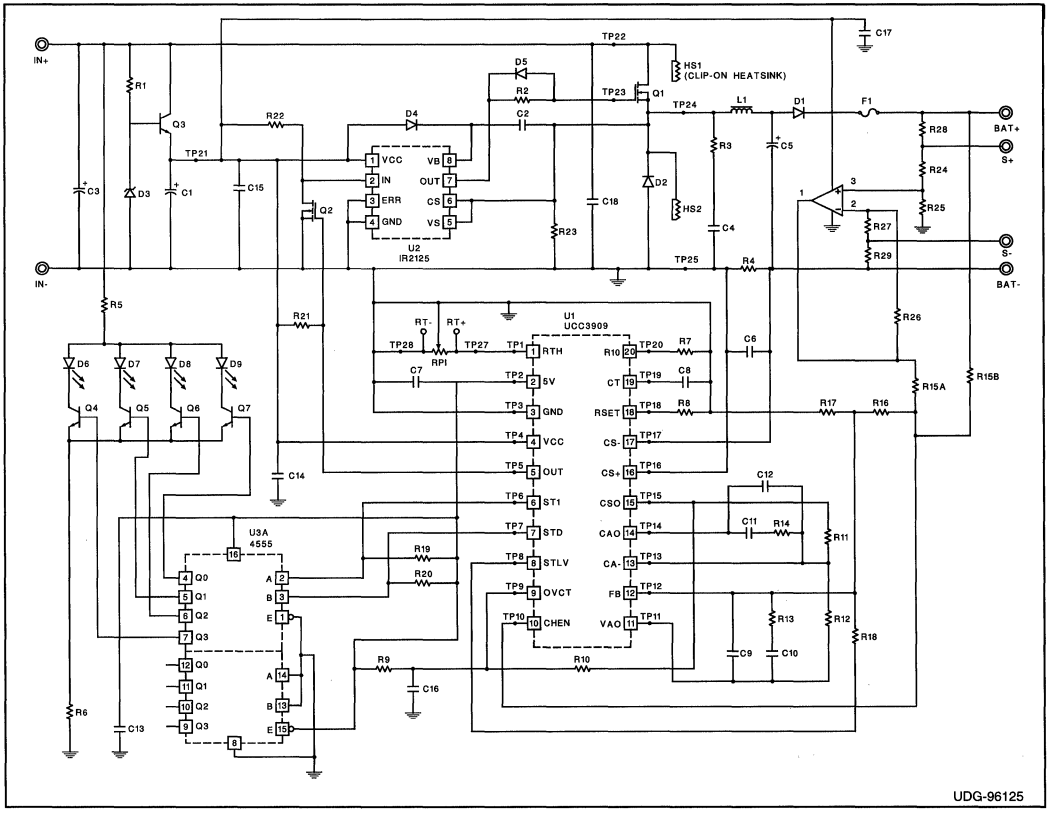

Figure 4. Demonstration Board Schematic

troller, when the primary power source is absent. An output fuse, F1, protects the circuit against the possible hazards when the battery is connected to the output terminals with reverse polarity. The charge current is measured by the resistor, R4 in the ground return path. The controller section consists of four well separable circuits. The first functional block is composed of R1, D3, Q3, and C1. These components provide a stabilized voltage for the rest of the control circuitry.

In the buck converter, the controlled switch, Q1, is located between the positive input terminal and the common node of the freewheeling diode, D2, and the output filter inductor, L1. There are many different components which could be used as a switch, yet for efficient operation and cost considerations, an N-channel MOSFET transistor has been selected. To interface the floating switch to the ground referenced controller, a high side driver is inevitable. The high side driver circuit consists of U2, D4, D5, R2, C2, Q2, R22 and R23. Its purpose is to level shift the output pulse of the control IC to the gate of the MOSFET transistor with minimum delays.

All the functions related to properly charging the battery are integrated in the UC3909 controller. The voltage and current levels which determine the actual values of the cutoff, over-charge and float voltages, as well as the trickle, bulk and taper threshold currents, are scaled appropriately by the resistor networks around the IC. The role of those components will be defined in the next chapter deliberating the design procedure.

The last section is the charge state decoder circuit. The coded information of the two outputs of the UC3909 is translated by U3, to display the actual operating mode of the battery charger.

BATTERY CHARGER DESIGN

The complete schematic drawing of the four state, switchmode battery charger is shown in Figure 4. In order to expedite the paper design, an easy to follow design procedure has been established. The step by step instructions can guide even the novice users through the calculations.

Battery Data

By the time the designer starts the circuit design, the type of the battery is already defined. The battery selection criteria are not detailed in this Application Note. Nevertheless, it is worthwhile to draw attention to some of the circumstances influencing the decision. Naturally, the most important parameters are the voltage and current requirements of the load as well as the time duration while the battery has to be able to supply the load current. Furthermore, the user has to consider whether the application requires frequent charge and discharge cycles or the battery is used in backup mode, where most of the time it will standby in its fully charged state. The available time for recharging the battery is also a significant factor to determine the applicable algorithm, and charge current rates. Combination of all these conditions will define the required battery and some of the battery charger parameters.

Once the battery is defined we can obtain the first set of input data. From the battery manufacturer's data sheet, more frequently through several telephone calls, and considering some application related conditions, the lines of Table 1 can be filled out.

For example, the demonstration circuit has been designed to charge a Dynasty JC1222 type sealed lead-acid battery from Johnson Controls. The nominal voltage is 12V, the capacity of the battery is 2.2Ah. Twelve volt batteries contain six cells connected in series. The battery has a temperature coefficient of -3.9mV/°C. Additional input parameters, like operating temperature range, float, cutoff and over-charge voltages as well as trickle, bulk, and over-charge terminate current levels can be determined from the application requirements and from the battery data sheet.

The completed Battery Data section is shown in Table 1. The trickle current level corresponds to the previously explained safety considerations and it equals C/100. A bulk charge current value of 800mA is given by the battery manufacturer [8] and is used instead of the C/2 value, noted in the respective equation in Table 1.

The over-charge period will be terminated when the current tapers off to one fourth of the bulk current. Maximum output power of the battery charger is listed in the last row of Table 1.

Parameter	Description	Definition	Value/Part#
Battery Data			**JC1222**
V	Nominal Battery Voltage		12V
NC	Number Of Cells	connected in series within the battery	6
C_{RATE}	Battery Capacity	use C/10 capacity; from battery datasheet	2.2 Ah
V_C	Cell Float Voltage	@25°C, fully charged; from battery datasheet	2.275V
$V_{C,MAX}$	Maximum Cell Voltage	@25°C, over-charge limit; from battery datasheet	2.43V
$V_{C,MIN}$	Minimum Cell Voltage	@25°C, fully discharged; from battery datasheet	1.75V
$I_{TRICKLE}$	Trickle Charge Current Limit	$I_{TRICKLE} = 0.01 \cdot C_{RATE}$; typical or use battery datasheet	22mA
I_{BULK}	Bulk Charge Current Limit	$I_{BULK} = 0.5 \cdot C_{RATE}$; typical or use battery datasheet	0.8A
I_{OCT}	Over-Charge Terminate Current Threshold	$I_{OCT} = 0.25 \cdot I_{BULK}$; typical or use battery datasheet	0.2A
TC	Cell Voltage Temperature Coefficient	typical value; the thermistor linearizer circuit is calibrated for this temperature coefficient	-3.9 mV/°C
T_{MIN}	Minimum Operating Battery Temperature	refer to your application requirements	-10°C
T_{MAX}	Maximum Operating Battery Temperature	refer to your application requirements	+50°C
V_{BAT}	Battery Float Voltage	$V_{BAT} = V_C \cdot NC$; nominal, @ 25°C battery temperature	13.65V
$V_{BAT,MIN}$	Minimum Battery Voltage	$V_{BAT,MIN} = \left[V_{C,MIN} + (T_{MAX} - 25) \cdot TC\right] \cdot NC$; @ T_{MAX}; fully discharged	9.92V
$V_{BAT,MAX}$	Maximum Battery Voltage	$V_{BAT,MAX} = \left[V_{C,MAX} + (T_{MIN} - 25) \cdot TC\right] \cdot NC$; @ T_{MIN}; fully charged	15.40V
$P_{CH,MAX}$	Maximum Output Power	$P_{CH,MAX} = I_{BULK} \cdot V_{BAT,MAX}$	12.3W

Table 1. Battery Charger Input Parameters

Buck Converter Operating Conditions

The battery charger circuit of the UC3909 is based on the buck topology. Before the component values of the power stage can be calculated, the basic operating parameters must be defined.

The output voltage range is listed in Table 1 as $V_{BAT,MIN}$ and $V_{BAT,MAX}$ determined primarily by the operating temperature range and the battery technology. On the other hand, input voltage variation depends on the power source. For this particular example, assume a 60Hz line isolation transformer with the optimized step down ratio. At minimum line voltage, it provides 18V DC voltage after rectification. Taking into account nominal tolerances, the input voltage of the converter at high line condition will be approximately 30V DC. From the minimum and maximum values of the input and output voltages, the steady state duty ratio limits are calculated (D=0.37 ... 0.89) as shown in Table 2.

At this point, the switching frequency of the converter has to be chosen. The trade-offs involved in the frequency selection are numerous. The primary factors are the speed of the prospective semiconductors, the capabilities of the controller, maintaining high efficiency in wide load current variations, power level and the size of the output inductor and capacitors.

Parameter	Description	Definition	Value/Part#
Buck Converter Operating Parameters			
$V_{IN,MIN}$	Minimum Input Voltage		18V
$V_{IN,MAX}$	Maximum Input Voltage		30V
f_S	Switching Frequency		50kHz
V_{D1F}	D1 Diode Forward Voltage Drop (estimate)	@100°C with I_{BULK}	0.59V
V_{D2F}	D2 Diode Forward Voltage Drop (estimate)	@100°C with I_{BULK}	0.73V
D_{MAX}	Maximum Duty Ratio	$D_{MAX} = \frac{V_{BAT,MAX} + V_{D1F} + V_{D2F}}{V_{IN,MIN} + V_{D2F}}$	0.89
D_{MIN}	Minimum Duty Ratio	$D_{MIN} = \frac{V_{BAT,MIN} + V_{D1F} + V_{D2F}}{V_{IN,MAX} + V_{D2F}}$	0.37

Table 2. Buck Converter Operating Parameters

For example, the upper limit of the operating frequency is bound to the capabilities of the slowest components. In the demonstration circuit, the high side gate driver circuit can be conveniently operated up to 150kHz operating frequency. Since the buck converter is a hard switched topology, the operating frequency has a significant effect on the efficiency. Considering that most of the time the charger supplies light output load, further reduction of the switching frequency is desirable to maintain decent efficiency in this operating modes.

While reducing the switching frequency has a beneficial effect on efficiency, at the same time the size of the output inductor and capacitors are increasing. The compromise between the size of the reactive circuit components and light load efficiency in trickle and float charge modes led to a moderate switching frequency selection of 50kHz.

Power Stage Design

Table 3 summarizes the design procedure of the power components. The bold entries shall be copied over to the part list directly. The respective equations are included, and they make use of variables defined in Table 1 and Table 2, or by the previous lines in Table 3.

Semiconductors

First, the three semiconductor devices are selected. Their voltage and current ratings are based on the maximum input and output voltages and on the bulk charge current. The minimum current ratings given in Table 3 assure appropriate margins for reliable operation. Using higher current components improves efficiency but also might increase cost.

After the part number is chosen, power dissipation estimates are given based on the actual voltage, current, and device parameters. The diode D1 carries the DC output current, therefore its dissipation is strictly conduction loss. The other two semiconductors are part of the switching circuit, hence their power dissipation is calculated by adding their respective conduction and switching losses.

Note that estimating switching losses on device parameters can be fairly inaccurate. This can cause a significant difference between the estimated and real switching losses especially at higher operating frequencies.

Output Inductor

The inductance of the output choke has been calculated by choosing the maximum ripple component of the inductor current. In a general purpose buck converter, unless extreme noise, core loss or application specific requirements would dictate otherwise, the rule of thumb is 25% to 35% of the DC current value is acceptable for ripple current content. Although battery manufacturers are concerned about using AC currents to charge the battery, they usually refer to frequencies below 1kHz. The DC output current with superimposed AC components of the switchmode chargers, at considerably higher frequencies, will be averaged by the slow chemical processes inside the battery.

Input Capacitor

The value of the input energy storage capacitor depends on the tolerable ripple and noise voltage at the input of the converter, and a function of the hold-up requirements. It is especially important for AC operated chargers where the energy is avail-

able in 120Hz repetitions, while the output has to be supplied continuously.

The situation is somewhat different if the charger is part of a distributed power system where an already regulated voltage with reasonable energy storage capability is available for the circuit. In this case, the ripple current handling capability of C3, and the noise requirements will determine the value of the input capacitor.

In Table 3, the value of the selected input capacitor is based on its rms current handling capability. The UC3909 demonstration circuit will operate properly when it is connected to a laboratory power supply, but will require a larger input capacitance in off-line applications.

Output Capacitor

There are numerous factors determining the output capacitor value. The various noise requirements at the output of the converter, the acceptable output voltage sag during the time interval when the capacitor contributes to supply the load current, and loop stability criteria. Fortunately, for all practical purposes, the output capacitor of a battery charger loses its importance since it is connected in parallel with the battery. The battery is considered as a low impedance voltage source with great high frequency filtering capabilities, taking over the traditional functions of the output capacitor.

The output capacitor, C5 of the demonstration circuit was chosen to handle the rms value of the ripple current component in the output inductor, L1 and to provide appropriate filtering in the absence of the battery.

RC Damping Circuit

Due to the nonideal nature of the switching action in all hard switching topologies, excessive switching spikes can develop across the semiconductors of the circuit during the switching time interval. The reduction of this voltage stress is accomplished by an RC snubber circuit consisting of R3 and C4 of the demonstration circuit. The complex optimization of the RC network is assisted by reference [6]. Proper operation of the snubber circuit also depends on the layout and the parasitic components of the switching circuit. Table 3 gives two equations to calculate the component values of R3 and C4 as a starting point. Further optimization of these component values might be desirable based on measurement results.

Note, that a tight layout of the critical components C18, Q1 and D2, and using an ultra fast rectifier diode are also essential to keep unwanted switching spikes under control.

Current Sense

The accurate control of the output current is one of the most important functions of the battery charger. It is achieved by the UC3909 control IC using average current mode control. An exact measurement of the current flowing in the output inductor, L1 is required. Therefore, a low value current sense resistor, R4 is placed in the ground return path, between the anode of D2 and the negative electrode of the output capacitor, C5. The voltage developed across R4 is proportional to the inductor current, and used by the controller to regulate the trickle and bulk charge current levels as well as to provide current limiting during overload operation.

The value of the current sense resistor is determined to satisfy two conditions. The first constraint is to limit the maximum voltage across R4 below 350mV when full output current is delivered. This is required by the UC3909 to prevent the current sense amplifier from saturation. The second restriction is the power dissipation of R4. In Table 3, the power dissipation of the current sense resistor was set to 1.5% of the maximum output power. This assumption was made to balance between two opposing requirements, namely to maintain high efficiency and to provide the highest signal level across R4, thus to improve noise immunity of the circuit. The maximum power dissipation equation of R4 might have to be revised, especially in higher power applications, due to component ratings and efficiency considerations.

Output Fuse

The fuse in series with the output of the battery charger is intended to prevent catastrophic failure if the battery is connected to the charger with reversed polarity. The fuse has to be selected with sufficient safety margin to carry the full charge current, but disconnect the output quickly in case of excessive currents drawn from the battery.

Parameter	Description	Definition	Value/Part#
Power Stage Design			
V_{RMM} (D1)	Diode Breakdown Voltage (minimum)	$V_{RRM} = 1.5 \cdot V_{BAT,MAX}$ (pick the next higher standard value)	(23.1V) 50V
$I_{O,MIN}$ (D1)	Diode Current Rating (minimum)	$I_{O,MIN} = 2 \cdot I_{BULK}$	1.6A
D1	Discharge Protection Diode	Select general purpose diode.	**GI750CT**
P_{D1}	Diode Power Dissipation (approximate value for heatsink selection)	$P_{D1} = I_{BULK} \cdot V_{D1F}$ (assuming 100°C junction temperature)	0.5W
V_{RMM} (D2)	Diode Breakdown Voltage (minimum)	$V_{RRM} = 1.5 \cdot V_{IN,MAX}$ (pick the next higher standard value)	(45V) 50V
$I_{O,MIN}$ (D2)	Diode Current Rating (minimum)	$I_{O,MIN} = 2 \cdot I_{BULK}$	1.6A
D2	Buck Freewheeling Diode	Select ultra fast switching diode.	**MUR610**
t_{RR}	Diode Reverse Recovery Time	catalog data; @ I_{BULK} ; approximate value	35ns
I_{RRM}	Diode Peak Reverse Recovery Current	catalog data; @ I_{BULK} ; approximate value	0.5A
P_{D2}	Diode Power Dissipation (approximate value for heatsink selection)	$P_{D2} = I_{BULK} \cdot (1 - D_{MIN}) \cdot V_{D2F} + + 0.25 \cdot I_{RRM} \cdot V_{IN,MAX} \cdot t_{RR} \cdot f_S$	0.38W
V_{DSS} (Q1)	Switch Breakdown Voltage (minimum)	$V_{DSS} = 1.5 \cdot V_{IN,MAX}$ (pick the next higher standard value)	(45V) 50V
$I_{D,MIN}$ (Q1)	Transistor Current Rating (minimum)	$I_{D,MIN} = 4 \cdot I_{BULK}$	3.2A
Q1	Buck Main Switch	Select the MOSFET transistor	**IRFZ14**
R_{DSON} (Q1)	Switch ON Resistance	catalog data; @25°C, typical value	200mΩ
C_{OSS} (Q1)	Drain Source Capacitance	catalog data; typical value	160pF
I_{GATE}	Gate Charge/Discharge	approximate, average value	0.8A
Q_{GS} (Q1)	Gate-To-Source Charge	catalog data	3.1nC
Q_{GD} (Q1)	Gate-To-Drain Charge	catalog data	5.8nC
t_{OFF}; t_{ON}	Approximate Switching Times	$t_{OFF} = t_{ON} = \frac{Q_{GS} + Q_{GD}}{I_{GATE}}$	12ns
P_{Q1}	Switch Power Dissipation (approximate value for heatsink selection)	$P_{Q1} = I_{BULK}^2 \cdot D_{MAX} \cdot R_{DSON} \cdot 1.5 + + 0.5 \cdot C_{OSS} \cdot V_{IN,MAX}^2 \cdot f_S + + \frac{V_{IN,MAX} \cdot I_{BULK}}{2} \cdot (t_{OFF} + t_{ON} + t_{RR}) \cdot f_S$	0.21W
P_{HS}	Heatsink Power Dissipation	$P_{HS} = P_{D1} + P_{D2} + P_{Q1}$; worst case, estimate	1.1W
$\Delta I_{L,MAX}$	Inductor Ripple Current	$\Delta I_{L1,MAX} = 0.4 \cdot I_{BULK}$; typical value	0.32A
L1	Buck Inductance	$L1 = \frac{V_{IN,MAX}}{\Delta I_{L1,MAX} \cdot 4 \cdot f_S}$	(0.47mH) **0.4mH**
$I_{L1,PEAK}$	Inductor Peak Current	$I_{L1,PEAK} = I_{BULK} + \frac{V_{IN,MAX}}{8 \cdot L1 \cdot f_S}$	**1A**
L1	Buck Filter Inductor	Check vendor's list for off the shelf part number or design you inductor according to the values above	**PCV-2-400-05** (Coiltronics)

Parameter	Description	Definition	Value/Part#
V_{C3}	Input Capacitor Voltage Rating	$V_{C3} = 1.5 \cdot V_{IN,MAX}$ (pick the next higher standard value)	(45V) 50V
$I_{C3,RMS}$	Input Capacitor RMS Current	$I_{C3,RMS} = 0.5 \cdot I_{BULK}$ (worst case @ f_S; D=0.5)	0.4A
C3	Input Capacitor (electrolytic)	High frequency type, i.e. Panasonic HFQ series (see text for value considerations)	**680µF/35V**
C18	High Frequency Bypass Capacitor For Switches	Polypropylene or stacked metallized film. Minimum voltage rating equals V_{C3}.	**1µF/63V**
V_{C5}	Output Capacitor Voltage Rating	$V_{C5} = 1.5 \cdot V_{BAT,MAX}$ (pick the next higher standard value)	(23.1V) 25V
$I_{C5,RMS}$	Output Capacitor RMS Current	$I_{C5,RMS} = \frac{V_{IN,MAX}}{\sqrt{192} \cdot f_S \cdot L1}$	108mA
C5	Output Capacitor (electrolytic)	High frequency type, i.e. Panasonic HFQ series (see text for value considerations)	**470µF/25V**
$R_{C5,ESR}$	Output Capacitor's ESR	from datasheet	65mΩ
$P_{SN,MAX}$	Snubber Power Dissipation	$P_{SN,MAX} = P_{CH,MAX} \cdot 0.015$ assume 1.5% of full output power	0.185W
V_{C4}	Snubber Capacitor Voltage Rating	$V_{C4} = 1.5 \cdot V_{IN,MAX}$ (pick the next higher standard value)	(45V) 63V
C4	Snubber Capacitor (polypropylene or metallized film)	$C4 = \frac{2 \cdot P_{SN,MAX}}{V_{IN,MAX}^2 \cdot f_S}$ (pick the closest standard value)	(8.2nF) **10nF**
R3	Snubber Resistor (noninductive)	$R3 = \frac{1}{16 \cdot \pi \cdot f_S \cdot C4}$ (pick the closest standard value)	(39.8Ω) **39Ω**
$P_{R4,MAX}$	Current Sense Resistor Power Dissipation	$P_{R4,MAX} = P_{CH,MAX} \cdot 0.015$ assume 1.5% of full output power	0.185W
R4	Current Sense Resistor (RS) (noninductive)	$R4 \le \frac{0.35}{I_{L1,PEAK}}$ *AND* $R4 \le \frac{P_{R4,MAX}}{I_{BULK}^2}$ (pick the next lower standard value)	(291mΩ) **270mΩ** (RCD type: RSF1B)
F1	Output Fuse Rating (fast acting type)	$I_{F1} = 1.25 \cdot I_{BULK}$ (pick the next higher standard value)	(1.0A) **1A**

Table 3. Buck Converter Power Stage Components Design Sheet

Controller Design

The controller design is described in Table 4. Instructions are organized by the functional blocks of the circuit. This procedure is similar to the one explained in the power stage design. All the equations use parameters calculated or entered in the previous three tables or the preceding lines of Table 4.

Auxiliary Power Supply

The purpose of this circuit is to provide a stabilized voltage for the gate drive IC and for the UC3909 controller circuits. The auxiliary voltage has to be higher than 7.8V, the undervoltage lockout of the UC3909. Furthermore, the auxiliary voltage has to be suitable to drive the gate of the MOSFET switch directly, limiting the voltage level below 18V. The auxiliary voltage of the demonstration circuit is approximately 14.5V, to satisfy both requirements with appropriate margins.

The circuit configuration shown in Figure 4 assumes that the minimum input voltage is higher than the auxiliary voltage. In this case, R1 biases D3 to the zener voltage, and provide the base current to Q3. The auxiliary voltage will be equal to the zener voltage minus the base emitter voltage of Q3. The advantage of this solution is that the

controller supply current flowing through Q3, is independent from the input voltage.

For completeness, it should be mentioned that there are other solutions to power the controller section of the battery charger. The actual solution has to take into account the operating input voltage range, the selected gate drive technique and the type of semiconductor used in place of Q1. For example, using a P-channel MOSFET transistor will require a different gate drive technique but will allow the user to omit the auxiliary supply and to power up the UC3909 directly from the input voltage. Note that even in this case auxiliary power supply might be necessary if the maximum input voltage exceeds the VCC rating of the controller.

MOSFET Gate Drive

The gate drive circuit is based on the IR2125, High Voltage High Side Gate Driver integrated circuit from International Rectifier. The different considerations for designing the circuit are outlined in the IR2125 datasheet, [7], and are used in the component selection. The given part values are applicable for switching frequencies above 10kHz and limited below approximately 150kHz. Using the IR2125 is possible for input voltages below 500V due to the voltage rating of the device.

There is one design aspect regarding the gate drive circuit which needs to be clarified. The IR2125 like all other high side driver IC working with the bootstrapping principle monitors the voltage across the bootstrap capacitor to ensure sufficient voltage for turning on the MOSFET transistor. The first pulse appears at the gate when both voltages, VCC with respect to ground and VB with respect to the VS pin are above their respective undervoltage lockout thresholds. Thus, precharging the bootstrap capacitor, C2 is imperative to get the circuit initially running. During normal operation, C2 is charged instantaneously through the conducting rectifier diode, D2. Conversely, at startup D2 will prevent charging the bootstrap capacitor. Fortunately the problem can be solved by a large value resistor, R23 connected between the VS pin of the IR2125 and the ground of the circuit.

Differential Output Voltage Sense

The differential voltage sense block is optional. Several trade-offs will be discussed in a later chapter together with other practical considerations. Adding a simple operational amplifier and a couple of resistors provides tighter output voltage regulation and remote sensing capability to the charger.

The design of the differential voltage sense circuit has to satisfy two conditions. The gain of the amplifier must be higher than the reciprocal value of the number of cells connected in series in the battery. This assures that the output voltage of the differential amplifier is compatible with the voltages expected by the UC3909. A second condition is given in Table 4 ensures that the inputs of the differential amplifier stage will be kept within their common mode voltage range at any possible battery voltage. The actual gain, within these two limits, can be determined by the user.

Note that the gain of the amplifier, "A", will be used in the subsequent lines of Table 4. Therefore, even if the differential amplifier stage is omitted, the value of "A" shall be made equal to 1, and used for the rest of the calculations.

Housekeeping and Battery Temperature Sensing

The oscillator frequency is set by C8 and R8, and the UC3909 datasheet contains the exact timing equations. In Table 4, the timing equation is already solved for easily available capacitor values and for the most common frequency range. First the user selects the appropriate capacitor value based on the switching frequency defined in Table 2. Then the value of R8 is calculated, since resistor values are available in much finer steps than those of the capacitors.

In the demonstration circuit the battery temperature variation is simulated by the RP1 potentiometer. For actual temperature compensation, it shall be substituted by a L1005-5744-103-D1 type thermistor from Keystone Carbon Co. [11] or equivalent. Since the resistance of the thermistor should represent the battery temperature, it is usually mounted on or in the vicinity of the battery. To facilitate this, a two pin header, P4 is provided for convenient connection of the temperature sensor.

Current Limitation

Four resistors R9, R10, R11, and R12 program the three critical current levels, as defined in Table 1. A battery charger operates in current limited mode during trickle and bulk charge. The corresponding two current levels are the trickle current, $I_{TRICKLE}$ and the bulk charge current, I_{BULK}. A third distinct

current level is the taper current threshold, I_{OCT} where the IC will switch from over-charge to float charge regime.

The accuracy of the different current levels depends on component tolerances and on some of the parameters of the control IC. Tolerances of the external resistors can be controlled by the appropriate part selection but the internal offsets and tolerances of the UC3909 are out of hand for the designer. The largest error term inside the IC is the offset of the current sense amplifier. Its effect is especially significant in trickle charge mode and at low current levels when the measured current signal is in the same order of magnitude than the input offset of the operational amplifier. For that reason, the initial accuracy of the trickle charge current limit can be in the neighborhood of ±30%. As the output current increases the accuracy improves rapidly and it is around ±5% at full current assuming 1% resistor tolerances.

Fortunately, in the battery charger application, only the bulk charge current has to be controlled precisely. The tolerances of the other two current values might influence the transitions between the charge regimes but do not represent a danger to the battery.

Setting The Output Voltages

The deep discharge threshold or cutoff voltage, over-charge voltage and float voltage are defined by the resistor network of R15, R16, R17, and R18, connected to the feedback pin of the UC3909. There are two different setup possibilities depending on whether the differential voltage sense circuit is used or omitted. With differential sensing, the calculated value of R15 resistor is placed in the position marked R15A, using the signal of the output of the operational amplifier, U4, for voltage regulation. In case of direct sensing of the output, the position R15B must be used instead. In order to provide tight tolerances of the three voltage levels, using 1% resistors is recommended.

Closing The Current Loop

"Closing the loop" is a frightening topic for many power supply designers. The detailed analysis of how to implement optimum loop compensation of the average current mode controller is beyond the scope of this Application Note. Nevertheless some excellent reference materials and design guide are listed in the Reference section of this paper [3], [4] and [5]. These articles cover not only the design criteria of the average current control loop used in the UC3909, but also explain the critical issues related to closing the voltage loop of the controller.

Using the procedure outlined in [3], closed form equations can be derived for all feedback components and they are given in Table 4.

Voltage Loop Compensation

The voltage loop of the demonstration circuit is compensated very conservatively for stability under wide operating conditions by introducing a dominant, low frequency pole to the system. The voltage loop crossover frequency is designed to be around 1kHz, which will result in a quite slow response to fast output voltage variations. However, the circuit performance is still acceptable since battery charging does not impose severe transient requirements on the power supply.

Note, that the equations given in Table 4 are suitable to implement stable voltage loop compensation but far from achieving the maximum bandwidth or best transient behavior.

Charge State Decoder

The battery charger progresses through four different operating modes which are related to the status of the charging process and to the replaced capacity of the battery. This information can be further processed to reveal vital information about the condition of the battery, to estimate the remaining charge time, and possibly to record the history of the battery. The UC3909 can signal the actual charge state in binary coded form on the STAT0 and STAT1 outputs. A truth table for decoding the status bits is given in the datasheet.

For the users convenience, a simple charge state decoder is implemented in the demonstration circuit. The decoding function is performed by an inexpensive integrated circuit, U3. According to the STAT0 and STAT1 outputs of the UC3909, one of its outputs are activated, which will cause one of the four transistors of Q4 - Q7, and respective light emitting diodes to turn on. Each LED corresponds to one of the four charge states as marked on the printed circuit board. The resistors R6 and R5 are intended to set the LED currents and to reduce the voltage across the collector and the emitter terminals of the transistors.

Parameter	Description	Definition	Value/Part#
Controller Part Values			
C6, C7, C13, C14, C15, C16,C17	Bypass Capacitors	X7R monolithic ceramic capacitors. Minimum voltage rating 25V.	**100nF/63V**
Auxiliary Power Supply			
D3	Auxiliary Voltage Stabilizer	**V_Z = 15V;** zener diode; 1W / 5%	**1N4744A**
V_{CEO} (Q3)	Collector Emitter Breakdown Voltage	$V_{CEO} = 1.5 \cdot (V_{IN,MAX} - V_Z)$ (select the next higher standard value)	(22.5V) 30V
Q3	Auxiliary Power Bypass	Select general purpose NPN transistor.	**2N3904**
R1	Zener Bias Resistor	$R1 = \frac{V_{IN,MIN} - V_Z}{2 \cdot 10^{-3}}$	**1.5kΩ**
P_{R1}	Zener Bias Resistor Power Dissipation	$P_{R1} = \frac{(V_{IN,MAX} - V_Z)^2}{R1}$	0.15W
C1	Auxiliary Power Storage Capacitor	Aluminum electrolytic capacitor. Minimum voltage rating 25V.	**82µF/25V**
Gate Drive			
U2	International Rectifier	High Voltage High Side MOS Gate Driver	**IR2125**
C2	Bootstrap Capacitor	Stacked metallized film capacitor. Minimum voltage rating 25V.	**0.15µF/50V**
D4, D5	Switching Signal Diodes	Select high speed signal switching diodes.	**1N4148**
Q2	Gate Drive Inverter	Select small signal MOSFET transistor.	**2N7000**
R2	Gate Resistor for Q1		**4.7Ω**
R21, R22	Gate Drive Pull Up Resistors		**1kΩ**
R23	Bootstrap Precharger		**1kΩ**
R30	Gate Pull Down Resistor		**10kΩ**
Differential Voltage Sense - Optional			
U4	National Semiconductor	Dual Single Supply Operational Amplifier	**LM358N**
$I_{FB,MAX}$	Maximum Current Through Feedback Resistors		150µA
R24, R27	Voltage Sense Resistors	$R24 = R27 = \frac{V_{BAT}}{I_{FB,MAX}}$	**91kΩ**
R28, R29	Voltage Sense Resistors	$R28 = R29 = 0.001 \cdot R24$	**91Ω**
R25, R26	Voltage Sense Divider	$R25 = R26 = A \cdot R24$; where A must be $\frac{1}{NC} < A < \frac{V_Z - 3}{V_{BAT,MAX}}$	**30kΩ**
A	Gain Of Voltage Sense Amplifier	$A = \frac{R25}{R24 + R28}$; A=1 if amplifier is omitted.	0.3297
Charger Control Section - IC Setup - Housekeeping And Temperature Sensing			
U1	Unitrode	Switchmode Lead-Acid Battery Charger IC	**UC3909N**
C8	Timing Capacitor, CT	$f_S <$ 25 kHz 5.6nF 25 kHz $< f_S <$ 50 kHz 3.3nF 50 kHz $< f_S <$ 110 kHz 1.5nF 110 kHz $< f_S <$ 220 kHz 680pF	**1.5nF**
R8	RSET Oscillator	$R8 = \frac{1}{1.2 \cdot C8 \cdot f_S}$	**11kΩ**

Parameter	Description	Definition	Value/Part#
R7	Reference Resistor For The Thermistor Linearizer	Select 1%, low temperature coefficient type.	**10kΩ**
RP1	Thermistor Emulation Potentiometer	Select 10 turns potentiometer for fine resolution. (Set initial value to 10kΩ before putting it in.)	**50kΩ**
Charger Control Section - IC Setup - Current Levels			
R9	OVCTAP Set Resistor (ROVC2)	Noncritical; use:	**100kΩ**
R10	OVCTAP Set Resistor (ROVC1)	$R10 = 1.8518 \cdot I_{OCT} \cdot R4 \cdot R9$	**10kΩ**
R11	Trickle Current Limit Set Resistor (RG1)	$R11 = 43.4783 \cdot I_{TRICKLE} \cdot R4 \cdot R8$	**2.7kΩ**
R12	Bulk Current Limit Set Resistor (RG2)	$R12 = \frac{0.54 \cdot R11}{I_{BULK} \cdot R4}$	**6.8kΩ**
Charger Control Section - IC Setup - Voltage Levels			
R15	Battery Voltage Divider (RS1) ±1% recommended	$R15 = \frac{V_{C,MAX}}{I_{FB,MAX}} \cdot \frac{V_{C,MIN} \cdot A \cdot NC - 2.3}{V_{C,MIN}}$	**11kΩ**
R16	Battery Voltage Divider (RS2) ±1% recommended	$R16 = \frac{2.3}{I_{FB,MAX}} \cdot \frac{V_{C,MAX} - V_{C,MIN}}{V_{C,MIN}}$	**6.2kΩ**
R17	Battery Voltage Divider (RS3) ±1% recommended	$R17 = \frac{2.3}{I_{FB,MAX}} \cdot \frac{V_{C,MAX} \cdot A \cdot NC - 2.3}{V_C \cdot A \cdot NC - 2.3}$	**18kΩ**
R18	Battery Voltage Float Adj. (RS4) ±1% recommended	$R18 = \frac{2.3}{I_{FB,MAX}} \cdot \frac{V_{C,MAX} \cdot A \cdot NC - 2.3}{(V_{C,MAX} - V_C) \cdot A \cdot NC}$	**130kΩ**
Charger Control Section - IC Setup - Current Error Amplifier			
R14	Current Error Amplifier Compensation Resistor	$R14 = \frac{0.28 \cdot f_S \cdot L1}{V_{BAT,MAX} + V_{D1F} + V_{D2F}} \cdot \frac{R11}{R4}$	**3.3kΩ**
C11	Current Error Amplifier Compensation Capacitor	$C11 = \frac{10}{2 \cdot \pi \cdot f_S \cdot R14}$	**10nF**
C12	Current Error Amplifier Compensation Capacitor	$C12 = \frac{1}{2 \cdot \pi \cdot f_S \cdot R14}$	**1nF**
Charger Control Section - IC Setup - Voltage Error Amplifier			
f_0	Voltage Loop Cross-Over Frequency	Dominant pole; noncritical requirements.	1kHz
R13	Voltage Error Amplifier Compensation Resistor	$R13 = \frac{0.625 \cdot V_{IN,MAX} \cdot (R15 + R16)}{A \cdot I_{BULK} \cdot f_S \cdot L1 \cdot V_{BAT,MAX}} \cdot \sqrt{\frac{1 + \left(16 \cdot \pi \cdot f_0 \cdot f_S \cdot L1 \cdot C5 \cdot \frac{V_{BAT,MAX}}{V_{IN,MAX}}\right)^2}{1 + \left(2 \cdot \pi \cdot f_0 \cdot R_{C5,ESR} \cdot C5\right)^2}}$	**910kΩ**
C9	Voltage Error Amplifier Compensation Capacitor	$C9 = \frac{C5 \cdot R_{C5,ESR}}{R13}$	**33pF**
C10	Voltage Error Amplifier Compensation Capacitor	$C10 = \frac{8 \cdot f_S \cdot L1 \cdot C5 \cdot V_{BAT,MAX}}{R13 \cdot V_{IN,MAX}}$	**47nF**
Charge State Decoder			
U3	Motorola	Dual Binary To 1-of-4 Decoder/Demultiplexer	**MC14555BCP**
D6, D7, D8, D9	Status Indicator LED's	Quad green LED assembly.	**IDI 5640H5**

Parameter	Description	Definition	Value/Part#
Q4, Q5, Q6, Q7	LED Driver Transistors	Minimum V_{CEO} equals $V_{IN,MAX}$ value	**2N3904**
R6	LED Current Set Resistor	$R6 = \frac{4.3}{0.01}$ assuming 10 mA LED current.	**430Ω**
R5	Voltage Limiter of the LED Driver Transistors	$R5 = \frac{V_{IN,MIN} - 7}{0.01}$	**1.1kΩ**
R19, R20	Pull Up Resistors	Noncritical; use:	**10kΩ**

Table 4. Four State Battery Charger Controller Design Sheet

PARTS LIST

The following Bill Of Material was generated from the calculated part values listed in Table 3 and 4. The part designators correspond to the Demonstration Board component positions.

C1	82µF,	25V	electrolytic
C2	0.15µF	50V	met.film / polypropylene
C3	680µF	35V	electrolytic
C4	10nF	50V	met.film / polypropylene
C5	470µF	25V	electrolytic
C6	0.1µF	50V	ceramic
C7	0.1µF	50V	ceramic
C8	1.5nF	50V	ceramic
C9	33pF	50V	ceramic
C10	47nF	50V	ceramic
C11	10nF	50V	ceramic
C12	1.0nF	50V	ceramic
C13	0.1µF	50V	ceramic
C14	0.1µF	50V	ceramic
C15	0.1µF	50V	ceramic
C16	0.1µF	50V	ceramic
C17	0.1µF	50V	ceramic
C18	1.0µF	63V	met.film / polypropylene
D1	GI750CT		100V, 6A, general
D2	MUR610CT		100V, 6A, ultrafast
D3	1N4744A		15V,1W zener
D4	1N4148		75V, 200mA, switching
D5	1N4148		75V, 200mA, switching
D6-D9	L20355		LED assembly,IDI
L1	375µH	4A	Coilcraft
Q1	IRFZ14		60V, 10A, NMOS
Q2	2N7000		60V, 500mA, NMOS
Q3	2N3904		40V, 200mA, NPN
Q4	2N3904		40V, 200mA, NPN
Q5	2N3904		40V, 200mA, NPN
Q6	2N3904		40V, 200mA, NPN
Q7	2N3904		40V, 200mA, NPN

R1	1.5kΩ	5%, 0.25W	
R2	4.7Ω	5%, 0.25W	
R3	39Ω	5%, 0.6W	metal film
R4	270mΩ	5%, 1W	RCD-RSF1B
R5	1.1kΩ	5%, 0.25W	
R6	430Ω	5%, 0.25W	
R7	10kΩ	5%, 0.25W	
R8	11kΩ	5%, 0.25W	
R9	100kΩ	5%, 0.25W	
R10	10kΩ	5%, 0.25W	
R11	2.7kΩ	5%, 0.25W	
R12	6.8kΩ	5%, 0.25W	
R13	910kΩ	5%, 0.25W	
R14	3.3kΩ	5%, 0.25W	
R15A	11kΩ	1%, 0.25W	
R16	6.2kΩ	1%, 0.25W	
R17	18kΩ	1%, 0.25W	
R18	130kΩ	1%, 0.25W	
R19	10kΩ	5%, 0.25W	
R20	10kΩ	5%, 0.25W	
R21	1kΩ	5%, 0.25W	
R22	1kΩ	5%, 0.25W	
R23	1kΩ	5%, 0.25W	
R24	91kΩ	1%, 0.25W	
R25	30kΩ	1%, 0.25W	
R26	30kΩ	1%, 0.25W	
R27	91kΩ	1%, 0.25W	
R28	91Ω	5%, 0.25W	
R29	91Ω	5%, 0.25W	
R30	10 kΩ	5%, 0.25W	
RP1	50kΩ	0.25W	10 turns potentiometer
U1	UC3909N		Battery Charger Controller
U2	IR2125		High Side Driver
U3	MC14555BCP		Binary to 1-of-4 Decoder
U4	LM358N		Operational Amplifier

MEASUREMENT RESULTS

Checking Out The Circuit

To safely bring the circuit into operation, the following precautions shall be exercised to prevent catastrophic failures at the first turn on. Use sockets for all integrated circuits and do not plug them in until the auxiliary power supply is checked.

All voltages given in the rest of this chapter are with respect to circuit ground unless otherwise noted.

Step 1.

Connect the input of the circuit to your DC power source. Increase the input voltage slowly up to the minimum input voltage value used in Table 2. Check the auxiliary supply voltage at the test point, TP21. The correct value should be 0.7V less than the V_Z voltage listed in Table 4, approximately 14.3V for this example. The same voltage should be measured at pin 4 of U4, pin 1 of U2 and pin 8 of U4 integrated circuits. When all voltages are correct, remove the input power.

Step 2.

Install U1, and connect the input voltage again. Measure the reference voltage of the UC3909. The correct voltage on pin 2 (TP2) is 5V. Next, check the oscillator. Measure and compare the timing capacitor and output waveforms, TP19 and TP5 respectively, to the oscillogram shown in Figure 5.

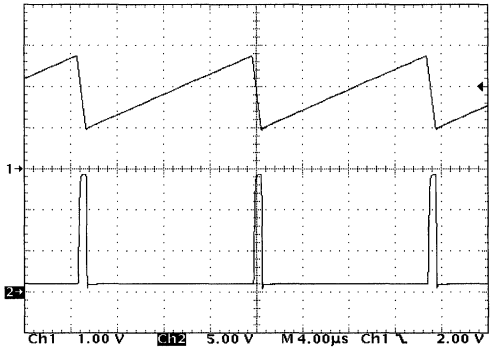

Figure 5. Trace 1: Timing Capacitor Waveform; Trace 2: OUT pin of UC3909

Compare the operating frequency to the expected value listed in Table 2. Disconnect the input voltage.

Step 3.

Populate the remaining of the IC sockets, by installing U2, U3, and U4 integrated circuits. Connect a resistive load to the output terminals. The load resistor shall be calculated as:

$$R_{LOAD} = \frac{2 \cdot V_{BAT}}{I_{OCT}}$$

Slowly raise the input voltage of the circuit while continuously monitoring the output voltage. The output voltage shall increase together with the input voltage until the output equals the float voltage, V_{BAT}. For further increases of the input voltage, the output should be regulated at the float charge voltage. If the output is not regulating, stop increasing the input voltage. Check the component values in the feedback divider, and the operating conditions of the UC3909. Convenient test points are provided in the demonstration board, for easy access to the pins of the integrated controller. The descriptions and typical voltages of the individual pins are included in the datasheet of the UC3909.

Step 4.

Once the output voltage is stabilized, check the switching waveforms of the converter. Typical waveforms of gate drive (U2/pin2), Q1 drain current, TP24, and the output inductor current, measured at full load, are shown in Figure 6.

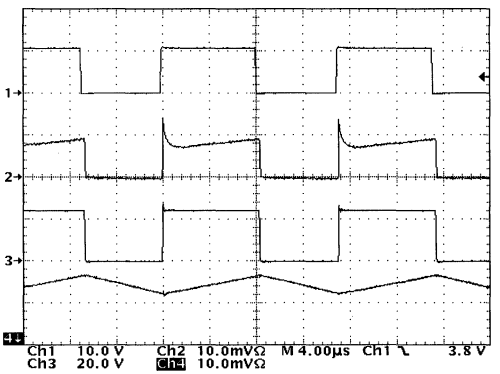

Figure 6. Switching waveforms of the converter: Trace 1: OUT pin; Trace 2: I_{Q1} (1A/div); Trace 3: TP24; Trace 4: I_L (0.5A/div)

Step 5.

The final test of the circuit is to check the bulk charge current limit, the float and over-charge voltage levels. The load resistor defined in step 2 ensures float mode operation of the charger. Note the

float voltage then gradually increase the load current until the charger reverts to bulk charge mode. At this point the output current should be equal to I_{BULK}. By slowly reducing the load current, the charger will sequence to the next state, over-charging. In this mode of operation the output voltage equals to $V_{BAT,MAX}$, the over-charge voltage. Verify the numbers against the values in Table 1.

Charge Characteristic

The ultimate test of the circuit is to charge a battery. The demonstration circuit has been designed to charge a 12V, 2.2Ah sealed lead-acid battery. During the charge cycle, the battery voltage and current, and the displayed operating states have been recorded. The result is shown in Figure 7.

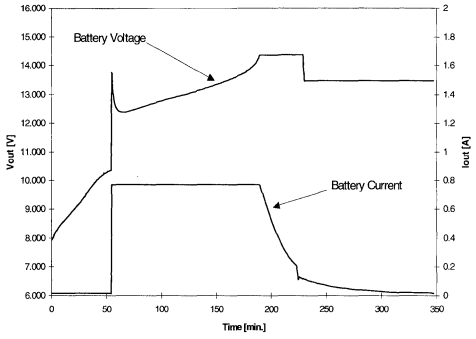

Figure 7. JC1222 Charge Characteristic

The chart shows the change of the battery voltage and charge current as a function of time and the exact values of the characteristic parameters. As can be seen, the charger started with trickle charge mode. When the battery voltage reached the cutoff voltage, the charger switched over to bulk charging. The sharp peak in the battery voltage at the switch over is caused by the high internal impedance of the battery. The majority of the battery capacity is replenished in about two hours in bulk charge mode. Bulk charge is followed by the controlled over-charge of the battery. Note that the over-charge LED is turned on before the voltage loop is satisfied because the threshold of the voltage sense comparator is intentionally set 5% below the reference of the voltage error amplifier. This way, the turn on of the over-charge LED coincides with the onset of the chemical over-charge process indicated by the gradient change in the voltage curve. The battery charging process concludes in float mode when the current tapers off to near zero.

Efficiency

The efficiency of a converter is usually measured as a function of load current at a fixed output voltage and at different input voltages. While this method is really informative in DC-to-DC applications, it is very difficult to assess the efficiency of a battery charger this way. Since the load current and the output voltage of the converter vary continuously during charging, one single efficiency number carries very little information about the circuit.

To demonstrate the effect, three different efficiency graphs are given below. The first one shows the effect of the output voltage variation on the efficiency. The second one is the traditional efficiency chart at a fixed output voltage.

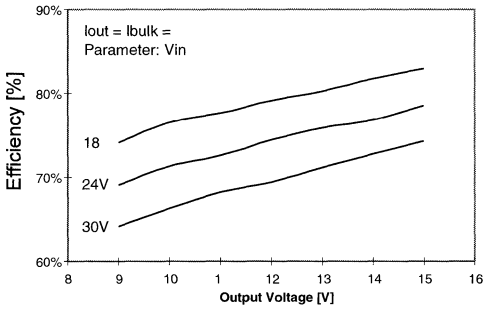

Figure 8. Efficiency vs. Output Voltage

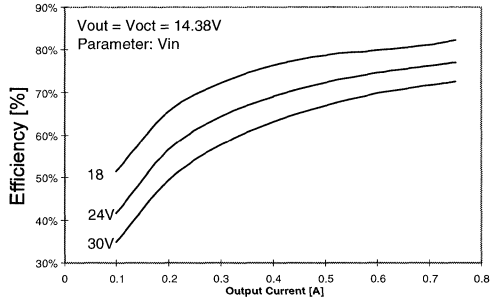

Figure 9. Efficiency vs. Load Current

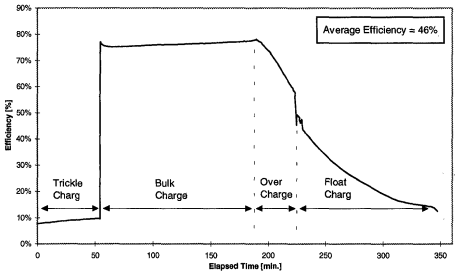

Figure 10. Efficiency vs. Time During Battery Charging

The third one presents the efficiencies during the entire charge cycle and the calculated average efficiency of the battery charger.

The typical efficiency of the demonstration circuit at full load with resistive load is 80%. This figure is useful for heatsink selection, and for comparison purposes.

PRACTICAL CONSIDERATIONS

Current Sense Issues

One of the most critical decisions of the design is how and where to sense the current in the converter. Using current mode control mandates sensing the current during the on-time of the switch Q1. In addition, when precise control of the output current is necessary, knowing the exact output current is inescapable. The output current of the buck converter equals the output inductor current, leaving very little choice to the designer. There are only two locations in the circuit, where the inductor current can be sensed accurately.

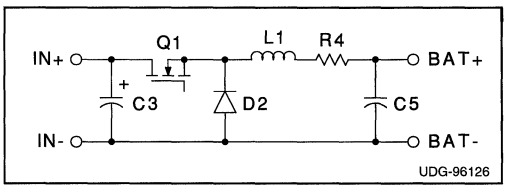

Figure 11. High side current sense technique

One possibility is the so called high side sensing, where the current sense resistor is placed in series with the output inductor as shown in Figure 11. For reliable operation it is important to put the resistor at the output capacitor side of the inductor, to avoid having a large switching component added to the inherently small current sense signal. Even with this precaution taken into account, the signal sits on top of a large common mode DC voltage (appr. V_{BAT}) which represents a problem for the current sense amplifier.

The amplifier has a limited Common Mode Input Voltage Range and a finite Common Mode Rejection Ratio which both confine its capability and its precision when the measured signal contains a significant common mode component. To illustrate the problem, look at the demonstration circuit.

When the battery is close to its fully charged state the current signal is superimposed on a 16V DC signal. At the same time, the supply voltage of the UC3909 is approximately 14.5V. In this case the Common Mode Input Voltage Range of the current sense amplifier is exceeded and the current information is either lost or erroneous. The problem could be addressed by providing a higher supply voltage for the controller but, since VCC is also limited, the problem is just shifted to a higher voltage level.

The other difficulty, related to the finite Common Mode Rejection Ratio, arises at light load. Even if the current signal is kept within the common mode input voltage range sensing small differential voltages are difficult. For instance, the bulk current of the battery charger causes the maximum allowable 350mV voltage drop across the current sense resistor. The trickle charge current is 1% of that current providing only 3.5mV useful signal for the amplifier. Assume that the output voltage is 10V and the CMRR of the current sense circuit is 60dB. There will be two components determining the output voltage of the amplifier. The amplified current signal, 17.5mV, is added to a 10mV error signal, developed from the 10V common mode components, present at the inverting and noninverting inputs of the current sense amplifier. As demonstrated, the error caused by the common mode component is rather significant, it is in the order of 35%.

The other possibility to monitor the inductor current is in the ground return path, as it is done in the demonstration circuit. This solution eliminates both problems related to the common mode properties of the amplifier since one end of the current sense resistor is actually grounded. The disadvantage of this technique is that the input and output grounds of the charger are not the same potential any more.

The low side current sensing offers two places for grounding the controller. The GND pin of the UC3909 can be connected either to the output side of the current sense resistor, or to its node com-

mon to the input of the buck regulator. When the IC is grounded at the output side, the output voltage is regulated perfectly. On the other hand the supply current of the UC3909 has to flow through the current sense resistor causing an error in the current measurement. The ICC of the controller has a wide tolerance which made the design of the trickle charge current very inaccurate.

Finally, the solution used in the demonstration circuit grounds the controller to the input side of the current sense resistor. It gives the best result to closely control the currents from no load to full current. The only factor influencing the accuracy of the current measurement is the input offset voltage of the current sense amplifier.

Until now, the effect of the current sense amplifier was neglected. Note that this offset is not specific to the low side sensing technique, and it would have further deteriorated the accuracy of any previously mentioned current sense method.

The current sense amplifier of the UC3909 possesses a 15mV maximum input offset voltage. This 15mV is comparable to the current signal in trickle charge mode. This explains the rather loose tolerance of the trickle charge current limit, mentioned earlier in the design chapter.

Although this approach exhibits the optimum properties to control the output current, it introduced a problem for the voltage regulation. Since the regulated voltage appears between the positive output terminal and the circuit ground, the output of the battery charger is not tightly controlled. The error is caused by the voltage drop across R4, proportional to the output current. At full current, at the beginning of the over-charge period the output voltage will be 350mV lower than the calculated over-charge voltage level, and as the current tapers off the error is diminishing. In float charge mode the output current, hence the voltage deviation from the designed value is negligible.

Differential Voltage Sense Advantages

By using the two inputs of the differential amplifier stage, the output voltage can be regulated between any two points of the output, independently from the grounding of the controller. When the two inputs are connected to the solder joints of the output connector, the effect of resistive voltage drops across the current sense resistor and on the printed circuit board traces can be eliminated. Furthermore, the user can compensate for the external voltage drop on the wiring between the output of the charger and the battery nodes using the two remote sense connections.

Driving A P-channel MOSFET Switch

The demonstration circuit takes advantage of the lower cost and better efficiency of an N-channel MOSFET. However, using a P-channel transistor can also be accomplished easily. Figure 12 shows a possible implementation of the P-channel MOSFET switch, driven by the UC3909.

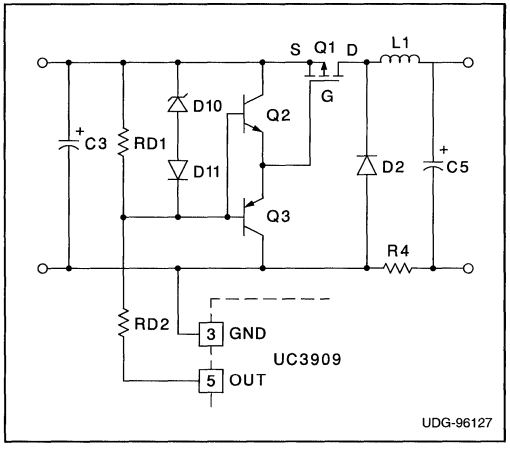

Figure 12. P-channel MOSFET Drive

The disadvantage of this technique is the relatively high power loss in the level shift circuit. The switching speed of the high side P-channel MOSFET is determined by the two series resistors connected to the output of the controller. To achieve acceptable turn-off speed the resistor values can not be increased. Therefore, the losses are especially high at elevated input voltages and at higher switching frequencies.

Skipping The Trickle Charge Mode

Depending on the battery type and the application, the trickle charge mode might not be necessary. Particularly, the new lead-acid batteries built from pure lead plates can accept full charge current from the beginning of the charge cycle. This requirement can be effortlessly accommodated by the UC3909 as shown in Figure 13.

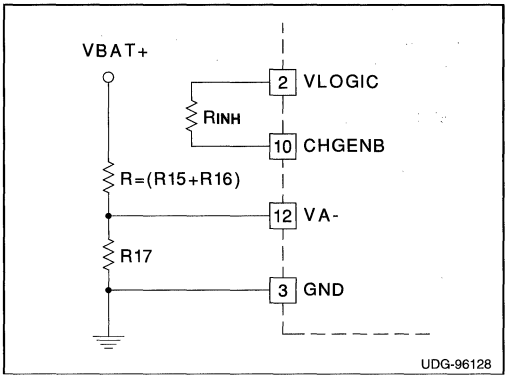

Figure 13. Inhibiting The Trickle Charge Mode

The trickle charge mode is inhibited when the CHGENB pin is connected to the VLOGIC pin of the IC. In this case, the charger will deliver full current, independently from the initial voltage of the battery, until it sequences to over-charge.

Soft-Start

Particularly when the trickle charge mode is eliminated, soft-start of the converter might be desirable. Usually, closed loop soft-start is achieved by gradually increasing the reference voltage of the voltage error amplifier. Open loop soft-start can be implemented by clamping the output of the voltage error amplifier. None of these practices are useful in the battery charger circuit for two reasons. The first obstacle is that the temperature compensated reference of the error amplifier is not available for external manipulations. The second problem is that the battery is already connected at turn on.

Since the battery is discharged at the beginning of the charging process, the voltage error amplifier is saturated and the converter operates in current limited mode. Therefore, soft-start can be introduced only in the current control loop. In general purpose buck converters this would result in output voltage overshoot during start-up, but with the battery connected to the output, this problem does not exist. The following circuit, shown in Figure 14 can be added to provide a simple soft-start solution for the battery charger.

The output current of the buck converter will ramp up gradually to the full bulk current value according to the RC time constant in Figure 14. This solution requires extreme cautions to ensure that precharging of the bootstrap capacitor is accomplished well before the charging of the soft-start capacitor is complete.

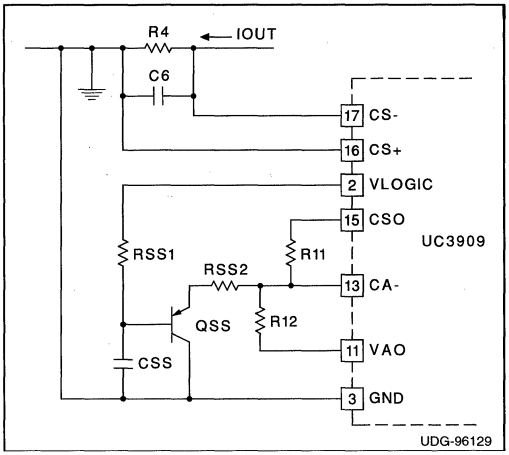

Figure 14. Soft-Start Of The UC3909

Eliminate Float Charge

The majority of the applications use the lead-acid batteries as backup power sources. In case of losing the primary power source, the system relies on the availability of the entire battery capacity. The float mode operation of the battery charger is intended to ensure that the battery is in its fully charged state during the stand by period.

As was mentioned earlier, finding the appropriate float voltage is critical to maintain 100% capacity of the battery. An easy way to avoid the problems related to float charge is to terminate the charging process upon completion of the over-charge process.

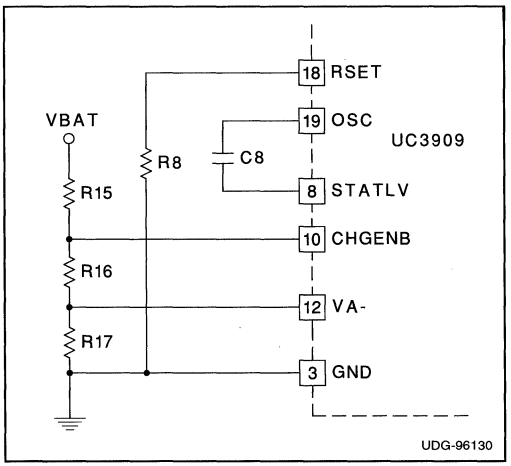

Figure 15. Disabling Float Charge State

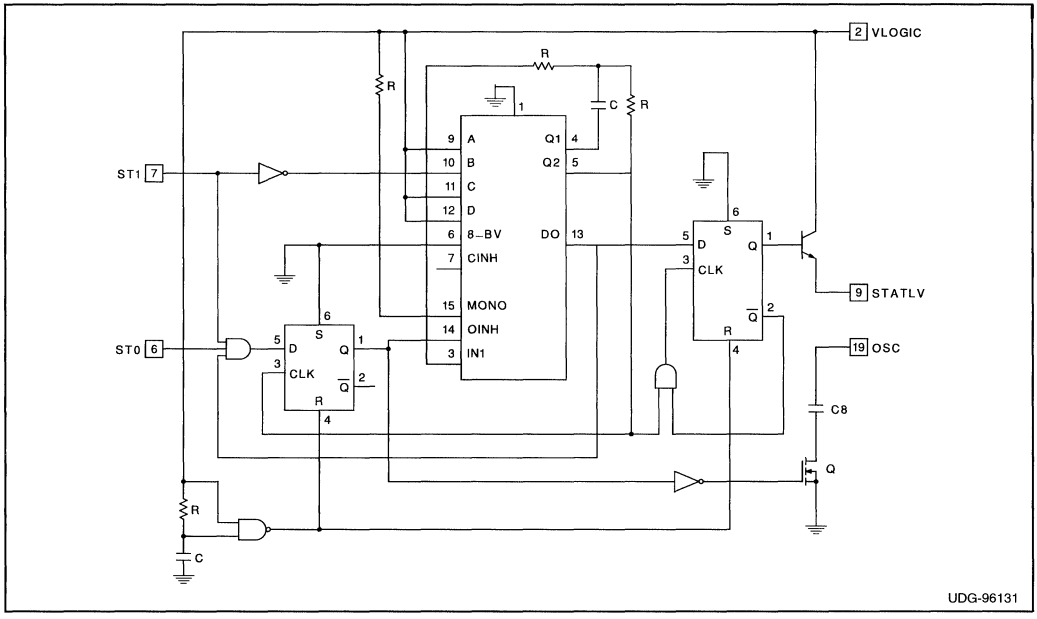

Figure 16. Implementing The Timed Charge Method

The solution shown in Figure 15 eliminates the float mode operation by disabling the oscillator. The advantage of this approach is that the IC will recover to bulk charge mode automatically if the battery voltage drops 10% below its nominal float voltage value.

Note that there are numerous other applications which also do not require float charging the batteries. For instance, batteries in hand held tools and portable equipment are recharged quickly while the primary power source is available, but do not employ float mode operation.

Incorporating Timed Algorithms

The constant voltage charge of the lead-acid batteries necessitates combining voltage monitoring and time measurement. It requires applying constant output voltage across the battery terminals for a certain time interval. Although the UC3909 is not optimized for these algorithms, the circuit diagram in Figure 16 shows how to combine the timer with the controller.

Off-line Configurations

Very often battery chargers are operated from the AC line. Figure 17 shows line isolation with a 60Hz transformer. This technique provides a low cost, competitive solution for low power applications. Furthermore, it can be advantageous for medium power, stationary applications because of its simplicity.

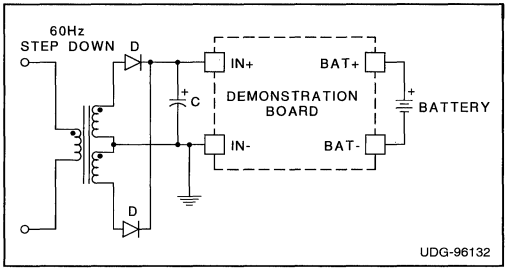

Figure 17. Isolated Off-Line Charger With 60Hz Step-Down Transformer

At higher output power, or in portable applications, the 60Hz isolation transformers become bulky. In this situation, line isolation is frequently obtained in the switchmode power stage. The forward converter, shown in Figure 18 is the isolated version of the buck topology. The components of the demonstration circuit can be easily recognized in the schematic drawing.

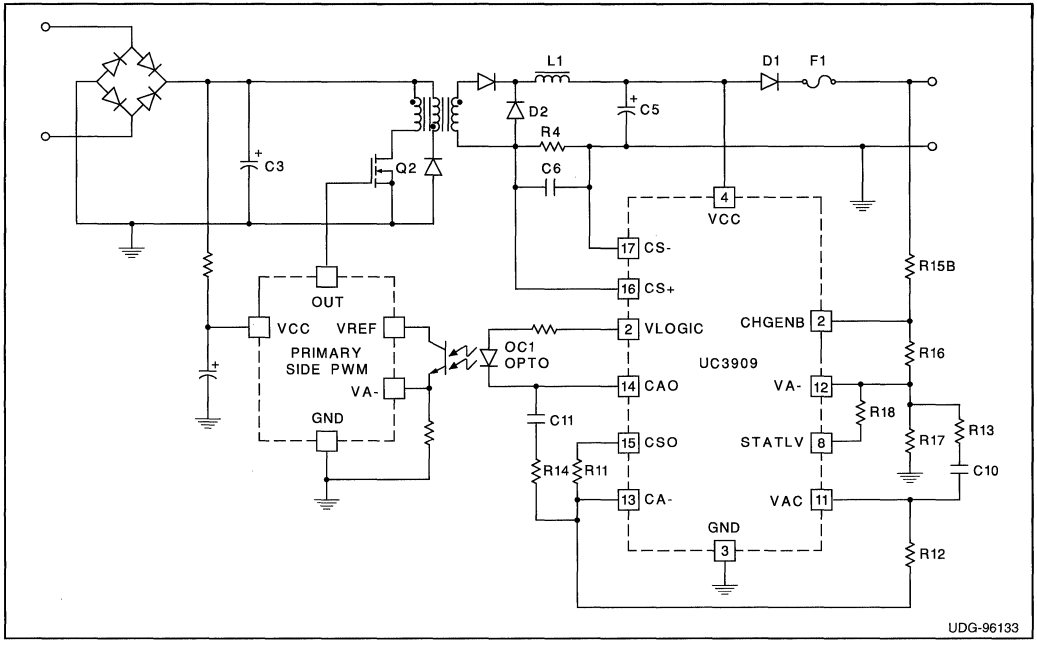

Figure 17. Forward Converter With Line Isolation

SUMMARY

This Application Note introduced the UC3909 Switchmode Lead-Acid Battery Charger controller in detail. A step-by-step design procedure of a buck converter, optimized for battery charger applications has been derived. Complete part list, and measurement results of the demonstration circuit complements the paper. Useful practical considerations are also given to help better understanding the various trade-offs involved in the battery charger design.

ADDITIONAL SUPPORT

Unitrode offers additional support to your battery charger project. The Appendix contains the MathCad® design file used to perform all calculations for Table 1 - 4. In addition, a printed circuit board of the fully functional battery charger circuit, useful upto 4A of continuos charge current is available for further evaluation.

For more information on the UC3909 Switchmode Lead-Acid Battery Charger controller or to order the demonstration circuit, please contact your Unitrode representative or the factory directly at (603) 424-2410.

REFERENCES

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[9] *"Battery Application Manual"*, Gates Energy Products, 1982

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APPENDIX

This MathCad file calculates the parameters and part values of the
UC3909 Switchmode Lead-Acid Battery Charger demonstration circuit.

NOTES:
- names ending to an "E" (i.e. R1E) are results of the respective calculations and they require manual entry of standard component values before continuing the calculations.

TABLE 1.

Input parameters:

NC := 6	Number of cells connected in **series** within the battery.
Cr := 2.2	Capacity of the battery.
Vc := 2.275	Cell float voltage at 25°C.
Vcmax := 2.43	Maximum cell voltage during controlled over-charge at 25°C.
Vcmin := 1.75	Minimum cell voltage at full discharge on 25°C.
It := 0	Trickle charge current. Enter the data from the battery datasheet or 0 for the default value (Itrickle=0.01*Cr).
Ib := 0.8	Bulk charge current. Enter the data from the battery datasheet or 0 for the default value (Ibulk=0.5*Cr).
Io := 0	Over-charge taper current threshold. Enter the data from the battery datasheet or 0 for the default value (Ioct=0.25*Ibulk).
TC := - 0.0039	Battery Temperature coefficient.
Tmin := - 10	Minimum operating temperature of the battery.
Tmax := 50	Maximum operating temperature of the battery.

Equations:	**Calculated paprameters:**
Itrickle := if(It=0, 0.01·Cr, It)	Itrickle = 0.022
Ibulk := if(Ib=0, 0.4·Cr, Ib)	Ibulk = 0.8
Ioct := if(Io=0, 0.25·Ibulk, Io)	Ioct = 0.2
Vbat := Vc·NC	Vbat = 13.65
Vbatmin := (Vcmin + (Tmax − 25)·TC)·NC	Vbatmin = 9.915
Vbatmax := (Vcmax + (Tmin − 25)·TC)·NC	Vbatmax = 15.399
Pchmax := Vbatmax·Ibulk	Pchmax = 12.319

TABLE 2.

Input parameters:

$Vinmin := 18$	Minimum input voltage of the battery charger.
$Vinmax := 30$	Maximum input voltage of the battery charger.
$fs := 50000$	Switching frequency of the converter.
$Vd1f := 0.59$	Forward voltage drop of D1 at Ibulk and 100°C junction temperature.
$Vd2f := 0.73$	Forward voltage drop of D2 at Ibulk and 100°C junction temperature.

Equations: **Calculated paprameters:**

$$Dmax := \frac{Vbatmax + Vd1f + Vd2f}{Vinmin + Vd2f} \qquad Dmax = 0.893$$

$$Dmin := \frac{Vbatmin + Vd1f + Vd2f}{Vinmax + Vd2f} \qquad Dmin = 0.366$$

TABLE 3.

Input parameters:

$trr := 35 \cdot 10^{-9}$	Reverse recovery time of D2 at Ibulk (estimate).
$Irrm := 0.5$	Peak reverse recovery current of D2 (estimate).
$Rdson := 0.2$	Channel resistance of Q1 at 25°C (the catalog data).
$Coss := 160 \cdot 10^{-12}$	Q1 drain source capacitance.
$Igate := 0.8$	Average gate current during turning on and off Q1.
$Qgs := 3.1 \cdot 10^{-9}$	Gate-to-source charge of Q1.
$Qgd := 5.8 \cdot 10^{-9}$	Gate-to-drain charge of Q1.

Equations: **Calculated paprameters:**

$VrmmD1 := 1.5 \cdot Vbatmax$	$VrmmD1 = 23.099$
$IminD1 := 2 \cdot Ibulk$	$IminD1 = 1.6$
$Pd1 := Ibulk \cdot Vd1f$	$Pd1 = 0.472$
$VrmmD2 := 1.5 \cdot Vinmax$	$VrmmD2 = 45$
$IminD2 := 2 \cdot Ibulk$	$IminD2 = 1.6$

$Pd2 := Ibulk \cdot (1 - Dmin) \cdot Vd2f + 0.25 \cdot Irrm \cdot Vinmax \cdot trr \cdot fs$ $Pd2 = 0.377$

$VdssQ1 := 1.5 \cdot Vinmax$ $VdssQ1 = 45$

$Idmin := 4 \cdot Ibulk$ $Idmin = 3.2$

$$tonoff := \frac{Qgs + Qgd}{Igate}$$ $tonoff = 1.113 \cdot 10^{-8}$

$$Pq1 := (Ibulk)^2 \cdot Dmax \cdot Rdson \cdot 1.5 + 0.5 \cdot Coss \cdot (Vinmax)^2 \cdot fs + \frac{Vinmax \cdot Ibulk}{2} \cdot (2 \cdot tonoff + trr) \cdot fs$$ $Pq1 = 0.209$

$Phs := Pd1 + Pd2 + Pq1$ $Phs = 1.058$

$dImax := 0.4 \cdot Ibulk$ $dImax = 0.32$

$$L1E := \frac{Vinmax}{4 \cdot dImax \cdot fs}$$ $L1E = 4.687 \cdot 10^{-4}$ $L1 := 400 \cdot 10^{-6}$

$$IL1peak := Ibulk + \frac{Vinmax}{8 \cdot L1 \cdot fs}$$ $IL1peak = 0.988$

$Vc3 := 1.5 \cdot Vinmax$ $Vc3 = 45$

$Ic3rms := 0.5 \cdot Ibulk$ $Ic3rms = 0.4$

$Vc5 := 1.5 \cdot Vbatmax$ $Vc5 = 23.099$

$$Ic5rms := \frac{Vinmax}{\sqrt{192} \cdot fs \cdot L1}$$ $Ic5rms = 0.108$

$Psn := 0.015 \cdot Pchmax$ $Psn = 0.185$

$Vc4 := 1.5 \cdot Vinmax$ $Vc4 = 45$

$$C4E := \frac{2 \cdot Psn}{(Vinmax)^2 \cdot fs}$$ $C4E = 8.213 \cdot 10^{-9}$ $C4 := 10 \cdot 10^{-9}$

$$R3E := \frac{1}{16 \cdot \pi \cdot fs \cdot C4}$$ $R3E = 39.789$ $R3 := 39$

$Pr4max := 0.015 \cdot Pchmax$ $Pr4max = 0.185$

$$R4E1 := \frac{0.35}{IL1peak}$$ $R4E1 = 0.354$ $$R4E2 := \frac{Pr4max}{(Ibulk)^2}$$ $R4E2 = 0.289$

$R4E := if(R4E1 > R4E2, R4E2, R4E1)$ $R4E = 0.289$ $R4 := 0.27$

$Pr4rated := (Ibulk)^2 \cdot R4 \cdot 5$ $Pr4rated = 0.864$

$If1 := 1.25 \cdot Ibulk$ $If1 = 1$

TABLE 4.

Input parameters:

$Vref := 2.3$	Internal reference voltage of the UC3909.
$Vlogic := 5$	The voltage on the VLOGIC pin of the UC3909.
$Vz := 15$	Zener voltage of D3.
$Ifbmax := 150 \cdot 10^{-6}$	Maximum current of the voltage feedback divider. This current always loads the battery.
$Ae := \frac{30}{91}$	Guess value of the gain (A) of the voltage sense amplifier.
$C8 := 1.5 \cdot 10^{-9}$	Timing capacitor value.
$C5 := 470 \cdot 10^{-6}$	Output capacitor value.
$Rc5esr := 65 \cdot 10^{-3}$	Equivalent series resistance of the output capacitor, C5.
$R9 := 100 \cdot 10^{3}$	Free parameter.
$f0 := 1000$	Voltage loop cross-over frequency.

Equations:		**Calculated paprameters:**
$VceoQ3 := 1.5 \cdot (Vinmax - Vz)$		$VceoQ3 = 22.5$
$R1E := \frac{Vinmin - Vz}{0.002}$	$R1E = 1.5 \cdot 10^{3}$	$R1 := 1500$
$Pr1 := \frac{(Vinmax - Vz)^2}{R1}$		$Pr1 = 0.15$
$R24E := \frac{Vbat}{Ifbmax}$	$R24E = 9.1 \cdot 10^{4}$	$R24 := 91 \cdot 10^{3}$
$R28 := 0.001 \cdot R24$		$R28 = 91$
$R25E := Ae \cdot R24$	$R25E = 3 \cdot 10^{4}$	$R25 := 30 \cdot 10^{3}$
$A := \frac{R25}{R24 + R28}$		$A = 0.329$
$R8E := \frac{1}{1.2 \cdot C8 \cdot fs}$	$R8E = 1.111 \cdot 10^{4}$	$R8 := 11000$
$R10E := 1.8518 \cdot Ioct \cdot R4 \cdot R9$	$R10E = 1 \cdot 10^{4}$	$R10 := 10000$
$R11E := 43.4783 \cdot Itrickle \cdot R4 \cdot R8$	$R11E = 2.841 \cdot 10^{3}$	$R11 := 2700$
$R12E := \frac{0.54 \cdot R11}{Ibulk \cdot R4}$	$R12E = 6.75 \cdot 10^{3}$	$R12 := 6800$

$$R15E := Vcmax \cdot \frac{Vcmin \cdot A \cdot NC - Vref}{Ifbmax \cdot Vcmin} \qquad R15E = 1.072 \cdot 10^{4} \qquad R15 := 11000$$

$$R16E := \frac{Vref}{Ifbmax} \cdot \frac{Vcmax - Vcmin}{Vcmin} \qquad R16E = 5.958 \cdot 10^{3} \qquad R16 := 6200$$

$$R17E := \frac{Vref}{Ifbmax} \cdot \frac{Vcmax \cdot A \cdot NC - Vref}{Vc \cdot A \cdot NC - Vref} \qquad R17E = 1.747 \cdot 10^{4} \qquad R17 := 18000$$

$$R18E := \frac{Vref}{Ifbmax} \cdot \frac{Vcmax \cdot A \cdot NC - Vref}{(Vcmax - Vc) \cdot A \cdot NC} \qquad R18E = 1.252 \cdot 10^{5} \qquad R18 := 130000$$

$$R14E := \frac{0.28 \cdot fs \cdot L1}{Vbatmax + Vd1f + Vd2f} \cdot \frac{R11}{R4} \qquad R14E = 3.349 \cdot 10^{3} \qquad R14 := 3300$$

$$C12E := \frac{1}{2 \cdot \pi \cdot fs \cdot R14} \qquad C12E = 9.646 \cdot 10^{-10} \qquad C12 := 1000 \cdot 10^{-12}$$

$$C11 := 10 \cdot C12 \qquad C11 = 1 \cdot 10^{-8}$$

$$R13E := \frac{0.625 \cdot Vinmax}{A \cdot Ibulk \cdot fs \cdot L1 \cdot Vbatmax} \cdot \sqrt{\frac{1 + \left(16 \cdot \pi \cdot f0 \cdot fs \cdot L1 \cdot C5 \cdot \frac{Vbatmax}{Vinmax}\right)^{2}}{1 + (2 \cdot \pi \cdot f0 \cdot Rc5esr \cdot C5)^{2}}} \cdot (R15 + R16)$$

$$R13E = 9.466 \cdot 10^{5} \qquad R13 := 910 \cdot 10^{3}$$

$$C9E := \frac{C5 \cdot Rc5esr}{R13} \qquad C9E = 3.357 \cdot 10^{-11} \qquad C9 := 33 \cdot 10^{-12}$$

$$C10E := \frac{C5 \cdot Vbatmax}{R13 \cdot Vinmax} \cdot 8 \cdot fs \cdot L1 \qquad C10E = 4.242 \cdot 10^{-8} \qquad C10 := 47 \cdot 10^{-9}$$

$$R6E := \frac{Vlogic - 0.7}{0.01} \qquad R6E = 430 \qquad R6 := 430$$

$$R5E := \frac{Vinmin - 7}{0.01} \qquad R5E = 1.1 \cdot 10^{3} \qquad R5 := 1100$$

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Implementing A Practical Off-line Lithium-Ion Charger Using The UCC3809 Primary Side Controller and The UCC3956 Battery Charger Controller

Introduction

A primary goal in the design of any portable electronic device is to make the product as small and lightweight as possible. When the device is powered by a rechargeable battery, a means of charging the battery from the AC line must be provided. Although battery charging is often thought of as a secondary function, the proper implementation of a charging system can ultimately determine the success of a product.

Off-line charger designs are often based on the use of a 60 Hz transformer; the magnetic is used to provide isolation and transform the line voltage to a lower level. The transformer's output voltage is rectified and fed into a DC/DC converter which provides charge current to the battery. Although this design approach is inherently simple, it can be bulky even at low power levels.

A steel 60Hz transformer used to deliver 10 watts, for example, weighs 0.5 pounds and occupies 5 cubic inches of volume. In contrast, a ferrite transformer at the same power level, operated at a 100kHz switching frequency, weighs only 0.02 pounds and has a volume of 0.25 cubic inches. This 20:1 reduction in size will allow the charger to reside in the portable device in most instances.

This paper will describe a 120VAC off-line charger that is based on a two series cell Lithium-Ion pack with a 1200mA hour capacity rating. The design described here can be modified to address different line and pack voltages. The paper will address the recommended charge algorithm for the pack, primary and secondary circuitry design, feedback loop compensation, and magnetic design for the converter.

Four-State Charge Algorithm for Lithium- Ion Batteries

Lithium-Ion batteries are becoming popular in portable and lap-top applications because of their superior energy density with respect to both weight and volume. Lithium-Ion batteries have higher cell voltages than the Nickel based chemistries they are replacing, averaging 3.6V per Lithium-Ion cell. Lithium-Ion batteries have safety concerns, however, and unique characteristics that require a dedicated charging algorithm. Figure 1 depicts the recommended fast charge algorithm for the two cell Lithium-Ion pack.

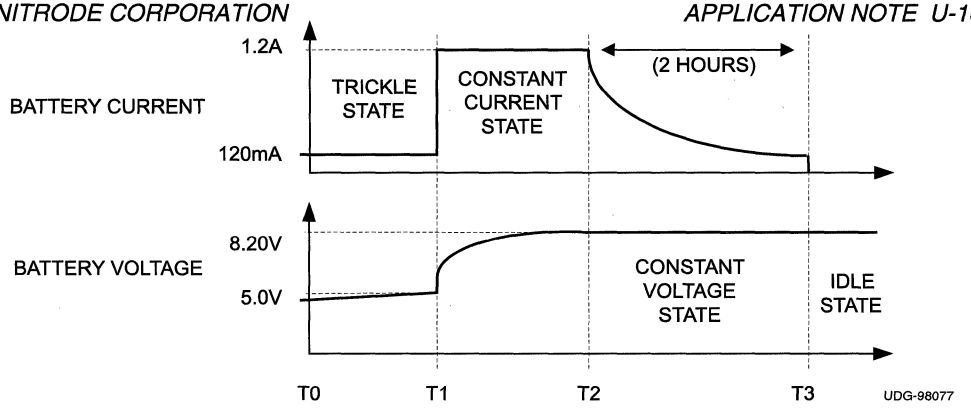

Figure 1. Recommended Charge Profile for Two Cell Lithium-Ion Battery Pack

Trickle State (t0-t1)
If the battery pack's voltage is below 5 volts, the pack is severely depleted and near zero capacity. Since the possibility of a shorted cell exists, the charger should not deliver full current to the battery. A reduced C/10 charge current of 120mA is applied to the cells in an attempt to safely restore capacity. In most cases, the battery will have some initial capacity and the charger will begin operation in the constant current state.

Constant Current State (t1-t2)
When the pack is above the 5 volt threshold, a constant current or "bulk" charge period will restore about 80% capacity to the cells. The current level of the charger will be set at 1.2A, corresponding to a 1C charge rate. The time period of the constant current state will depend on the battery's initial capacity.

Constant Voltage State (t2-t3)
When the pack reaches its final voltage (t2), constant voltage control is initiated, causing the battery current to decrease. Because Lithium-Ion batteries have safety concerns associated with the over-charging of cells, a timed constant voltage period is preferred by battery manufacturers[1][2]. The constant voltage period will regulate the pack to 8.2 volts (1% tolerance) for a duration of 2 hours. The timed constant voltage state will predictably restore the battery to 100% capacity.

Idle State
Once the timer expires (t3), the charge current to the pack is terminated and the fully charged pack is ready for use. The charger electronics will stay powered in the idle state, awaiting the start of a new charge cycle.

Design Overview

Figures 2 and 7 show a complete schematic for the 2 cell off-line charger. Since the peak output power of the charger is only 10 Watts, a flyback topology has been selected, requiring only a single magnetic component. The charger provides 3000 volts of isolation between the input line and battery in order to protect the user. This rating is determined by the optocoupler's pin spacing and transformer's insulation.

The primary side circuitry controls the peak current in the flyback transformer, while the average current delivered to the battery during the various charge states is programmed by the secondary side circuitry. An optocoupler is used to transfer the control signal from secondary to primary. The charger is designed to operate with discontinuous current, eliminating the need for slope compensation.

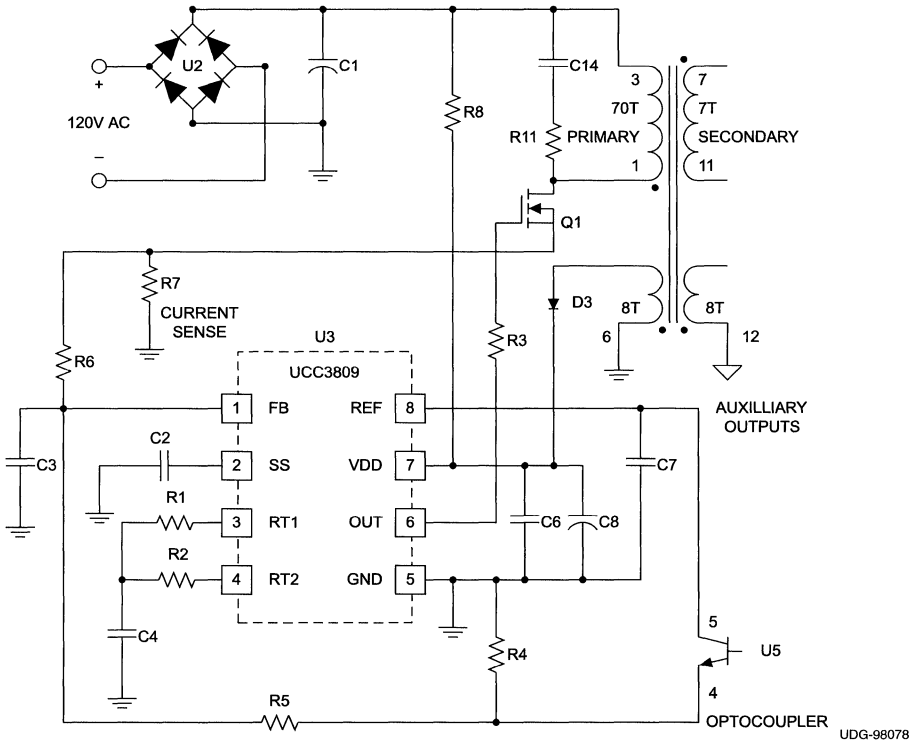

Figure 2. Primary Side Circuitry

Primary "Line" Side Operation

The charger operates off of a 120 volt line with a 10 percent tolerance. As shown in Figure 2, the line voltage is rectified and filtered by C1 to provide a DC voltage that can vary between 130 and 190 volts (depending on line and load conditions). The amount of 120Hz ripple at C1 is a function of the capacitance value selected and the power level of the charger[3]. A 33µF capacitor results in a maximum ripple of 15V at 10 Watts. Peak voltage stress on Q1 is equal to the sum of the maximum input voltage (190V), the maximum secondary voltage reflected by the turns ratio (9V x 10 = 90V), and the voltage spike created by leakage inductance in the transformer. A dissipative snubber (R11 & C14), limits the leakage spike to 100V. A 500V MOSFET (IRF820) was selected for Q1. Fig-

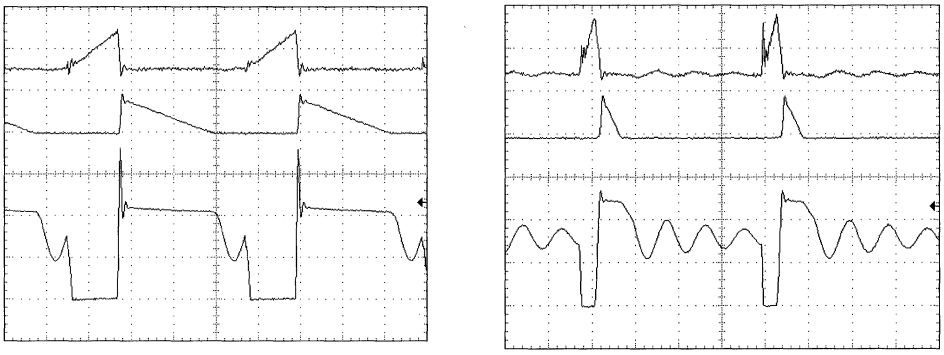

Figure 3. Q1 and D7 waveforms at Full and Light Loads

ure 3 shows the voltage on the drain of Q1 at full and light loads, along with primary and secondary currents.

When line voltage is initially applied to the charger, power is supplied to the primary controller through R8 and an internal 17V zener. A bootstrap winding on the flyback transformer provides additional supply current to C8 through D3 once the converter powers up. The amount of supply energy needed for the primary side circuitry is primarily a function of the MOSFET's capacitance. With a switching frequency of 100kHz, a supply current of 15mA is sufficient.

Unitrode's UCC3809[4] provides peak current control for the charger. Peak current control has the advantage of providing pulse by pulse short circuit protection in the event the output is shorted at the battery. The frequency of operation (100kHz) and maximum duty cycle are set by the component values connected to the RT1 and RT2 pins, while the SS pin sets a soft-start period.

Referring to figure 4, at the beginning of a switching cycle Q1 is turned on and current ramps up in the primary winding of the transformer. This current

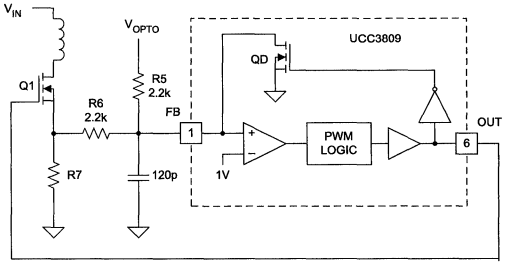

Figure 4. UCC3809 Peak Current Mode Control on Primary

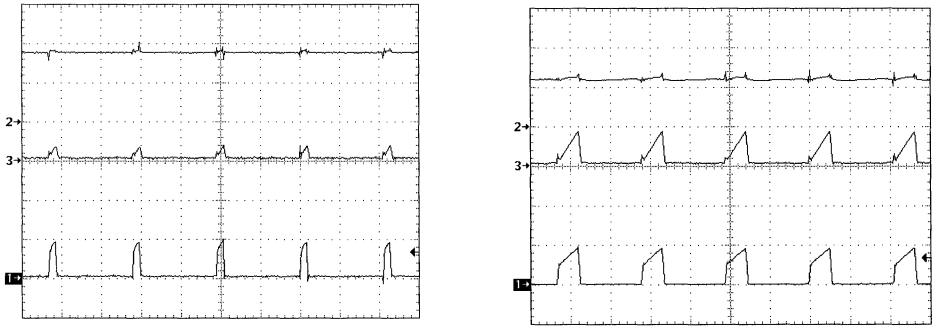

Figure 5. Light Load Operation (A), Full Load Operation (B)

forms a voltage across the current sense resistor (R7). The secondary side circuitry sets a DC voltage level at the emitter of the optocoupler (V_{OPTO}) that is used to control peak current ; when Vopto is decreased peak current will increase. The two voltages are summed into the FB pin of the primary controller through resistors R5 and R6. The FB pin is internally connected to the non-inverting input of a precision comparator, whose output turns Q1 off (via the OUT pin) when FB reaches 1 volt.

Switch Q_D, internal to the UCC3809, pulls the FB pin low when the OUT pin is low. With Q1 off, flyback current is forced out of the secondary winding

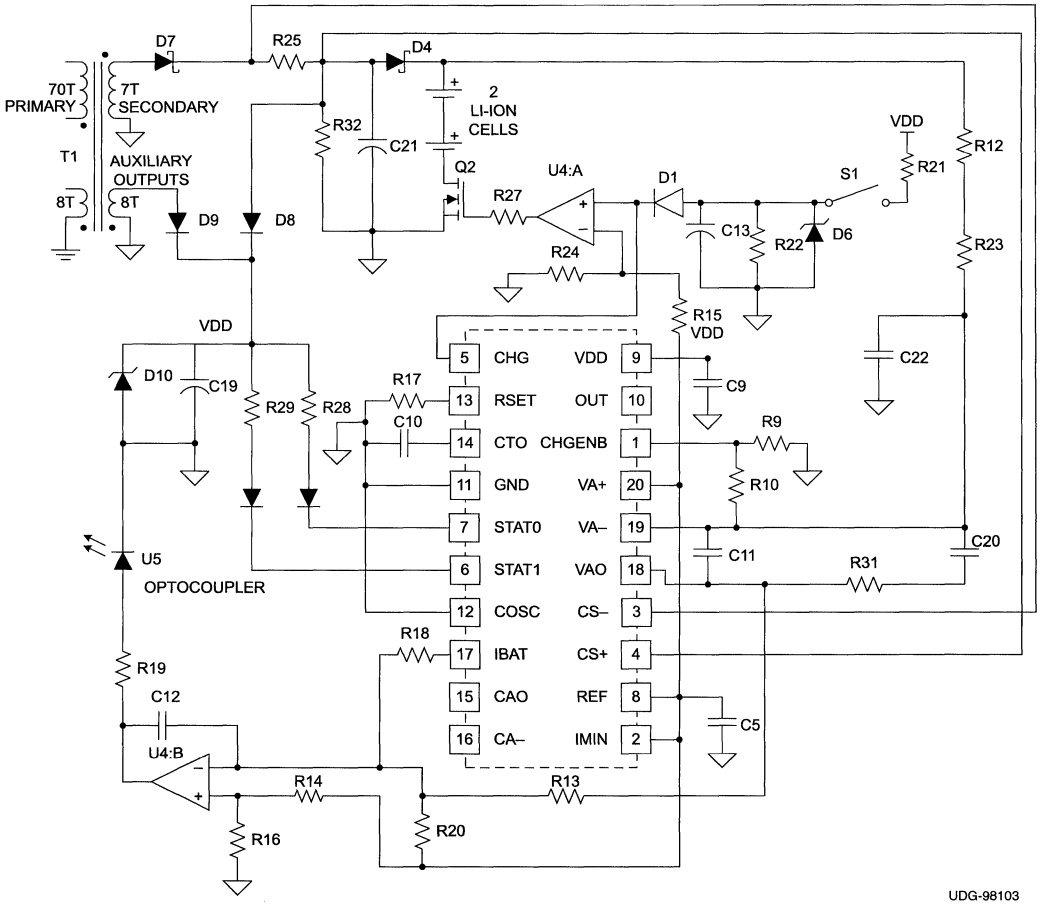

Figure 6. Secondary Side Circuitry

and delivered to the battery. Figure 5 shows the operating voltages at the emitter of the optocoupler and the FB pin at light load and full load respectively, along with primary current.

Secondary Side Operation

Secondary side control is provided by Unitrode's UCC3956 Lithium-Ion charger controller. The IC contains a precision 4.1V reference, an overcharge timer, and the control circuits necessary to implement the recommended charge profile of Figure 1. The controller has two status pins (STAT0, STAT1) which indicate the various states of the charger. A block diagram of the UCC3956 controller IC is shown if Figure 7 for reference.

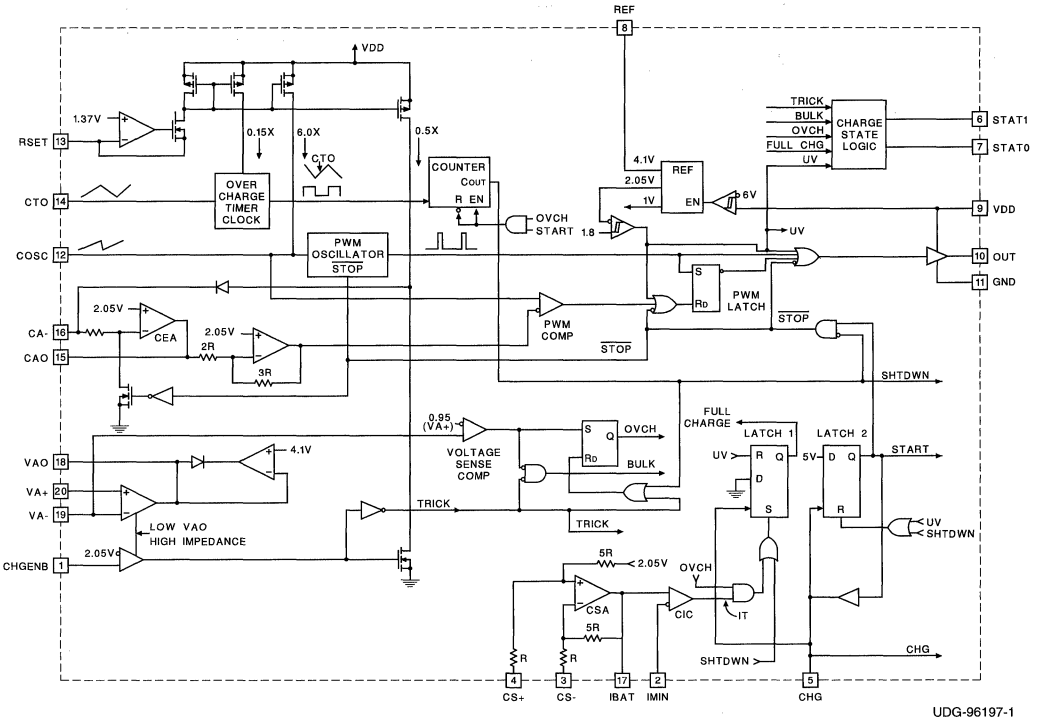

Figure 7. UCC3956 Lithium-Ion Control IC

The complete secondary side schematic for the charger is shown in Figure 6. Secondary current is sensed through R25, which is Kelvin connected to a current sense amplifier at pins CS- and CS+.

Programming the Trickle State. Referring to Figure 6, resistors R9, R10, R12, and R23 set the threshold voltage for trickle charge state at 5.0V (CHGEN pin).

$$V_{TRICKLE} = \frac{R9 + R10 + R12 + R23}{R9} \bullet 2.05 \quad (1)$$

When the battery voltage is below this level, the controller's voltage amplifier output (VAO) is put into a high impedance state. The average battery current is programmed to 120mA by a resistive divider between R20 (connected to Vref) and R18 (connected to the output of the current sense amplifier at IBAT). The external error amplifier produces the appropriate command signal, which is transferred across the optocoupler to the primary.

$$I_{TRICKLE} = \frac{2.05 \bullet R18}{5 \bullet R20 \bullet R25} \text{ (Amps)} \quad (2)$$

Programming the Constant Current "Bulk" State. When battery voltage is between 5.0 and 8.20 volts, the constant current state is activated and the voltage amplifier is internally clamped to 4.1 volts. The average battery current is set at 1.2A by a resistive divider, R18 and R13 between the output of the current sense amplifier and the voltage amplifier.

$$I_{BULK} = \frac{2.05 \bullet R18}{5 \bullet R13 \bullet R25} \text{ (Amps)} \quad (3)$$

Programming the Constant Voltage State. The resistor divider used to set the trickle threshold, also sets the final pack voltage to 8.20 volts at the VA– pin.

$$V_{FINAL} = \frac{R9 + R10 + R12 + R23}{R9 + R10} \bullet 2.05 \quad (4)$$

During the overcharge state, the voltage amplifier comes into regulation and its output voltage decreases, causing the average battery current to decrease. The overcharge timer period is programmed to 2 hours with a 0.18µF capacitor on

the CTO pin. When the charger completes the constant voltage state, a MOSFET in series with the battery is opened, preventing additional charge to the battery.

$$\text{Timeout} = 4500 \bullet R17 \bullet C10 \text{ (min)} \qquad (5)$$

Keeping the Charger Powered. In order to keep the charger powered and intelligent during all modes of operation, a capacitor (C21) and dummy load (R32) are added across the output of the flyback secondary. When the charger is in the idle state (or when the battery is out of the charger) the controller regulates the dummy load to 8.2V plus a diode drop. An additional diode (D4), prevents the pack from discharging in the event the charger is unplugged from the line. An auxiliary winding, similar to the winding on the primary circuit, is used to power the secondary controller. An 18V Zener (D10) assures the controller's maximum voltage specification is not exceeded.

Controller Modifications

The UCC3956 is designed to be a stand-alone controller for a DC to DC buck converter, certain modifications are needed to accommodate the off-line flyback design.

1. Since the MOSFET Q1 is driven by the primary side controller, the PWM output pin (OUT) of the UCC3956 is not connected.
2. The controller's error amplifier (CA) is replaced with an external LM358 Op-Amp (U4:B). This modification is necessary since the UCC3956 disables its error amplifier when the charger is in the idle state and the off-line charger needs the amplifier to keep the dummy load in regulation.
3. The second Op-Amp in the LM358 package (U4:A) is configured as a comparator, which interfaces between a momentary push button switch, the CHG pin, and the MOSFET (Q2) in series with the battery pack as shown in Figure 8a. The momentary push switch (S1) is used to initiate a charge cycle. When S1 is closed, R21 and C13 provide a slowly rising voltage at the CHG pin as shown in the timing waveforms of Figure 8b. At time t1, the comparator turns Q2 on before the CHG pin recognizes a new charge cycle at time (t_2). This allows time for the output voltage (V_{OUT}) to collapse from the idle state voltage (8.5V) to the uncharged battery voltage, preventing the constant voltage state timer from being initiated prematurely. The charger then progresses through its normal charge algorithm programmed with the UCC3956 (t_3-t_4). At the completion of the charge cycle (t_5), the CHG pin pulls low, Q2 is opened, and the charge current to the battery is terminated. The charger then waits in the idle state for the initiation of a new charge cycle.

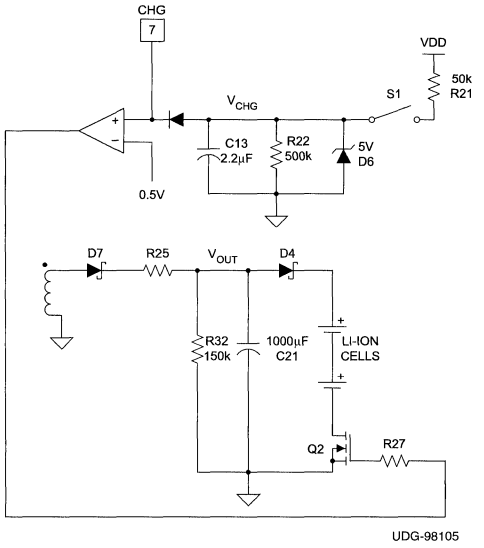

Figure 8a. CHG Pin Interface

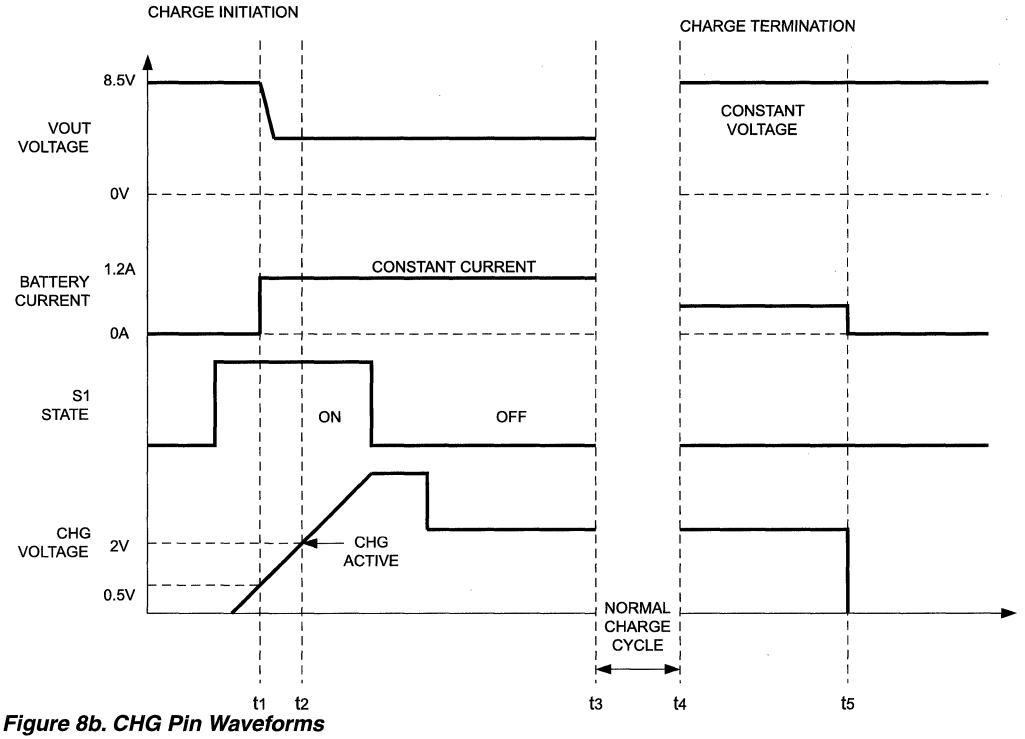

Figure 8b. CHG Pin Waveforms

Feedback Design

Figure 9 depicts the key elements that form the feedback network for the charger.

Referring to Figure 9, the battery current is sensed across R25 and amplified by the **current sense amplifier**. This signal is averaged by the **error amplifier**, and fed across the isolation barrier through the optocoupler circuit. The resulting voltage at the output of the optocoupler sets the peak current in the transformer primary. During the trickle and bulk charge states, the current loop takes exclusive control of the charger.

When the battery voltage approaches its final programmed value, the **voltage amplifier** comes into regulation and begins to reduce the current to the battery. The voltage loop maintains the battery voltage at 8.2V during the constant voltage period of operation. The voltage loop also regulates the dummy load voltage when the charger resides in the idle state.

Closing the Current Loop

A peak current control technique on the primary results in an uncompensated current loop gain that is essentially constant out to half the switching frequency. Referring to Figure 9, (and assuming equal values for R5 and R6) the small signal gain of the uncompensated current loop is determined by the primary sense resistor (1/R7), the transformer turns ratio (N), and the current sense amplifier circuit (5 • R25). Since the converter is run in discontinuous conduction mode, the gain is also a function of load. With the battery at 6 volts and 1.2 amps of bulk current, the current loop has a measured power stage gain of 4db. During trickle and overcharge periods, this loop gain is reduced as the current to the battery is reduced.

The optocoupler circuit adds an additional 5db of gain (R4/R19) to the power stage. The optocoupler has a pole around 50kHz, but this has minimal effect on phase margin, as the compensated current loop will cross unity gain at a much lower frequency.

As shown in Figure 9, the error amplifier is fed from the voltage and current sense amplifiers. When calculating the small signal gain of the current loop, the voltage amplifier output can be viewed as a DC source.

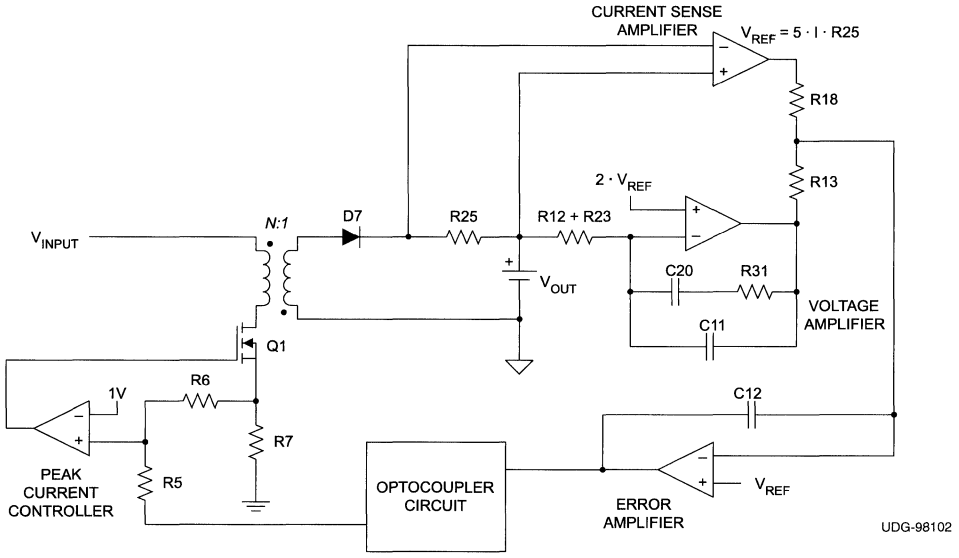

Figure 9. Simplified Charger Feedback Diagram

Single pole compensation (–20dB/decade) is added to the error amplifier to provide good dynamic response and stable operation. The gain of the error amplifier is equal to the impedance of the feedback capacitor C12 divided by R18. With C12 equal to 4700pF and R18 equal to 15K, the resulting cross over frequency is 2kHz (Figure 10, Error Amplifier). Adding the 9db of gain from the power stage and the optocoupler circuit (Figure 10. PWR + OPTO), the total current loop gain crosses unity gain around 6kHz (Figure 10. Total Loop).

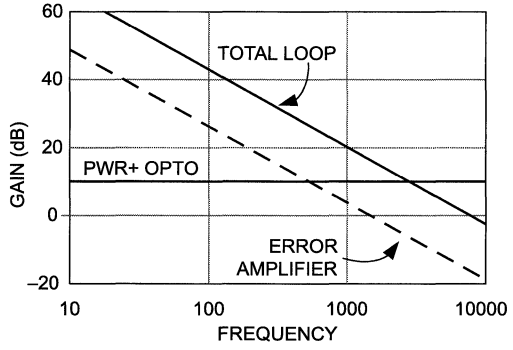

Figure 10. Current Loop Feedback

Adding the Voltage Loop

The gain of the voltage loop consists of the closed current loop gain 1/(5*R25) multiplied by the effective impedance of the output[6]. The voltage amplifier's effect on the current loop is attenuated by the Thevenin network [R18/(R18+R13)].

Although an accurate frequency model for a battery can be complex, the frequency characteristics of the 2 cell pack can be approximated as a constant gain out to 200Hz with a single pole roll-off above 200Hz. When the charger is in the idle state, C31 and R32 form a single pole frequency response at 1Hz. Figure 11A depicts the uncompensated frequency responses of the battery and dummy load voltage loops.

Interactions with the current loop are avoided by designing the total voltage loop to cross unity gain around 500Hz. The frequency characteristics of the voltage amplifier's pole-zero-pole compensation network (R31, C11, C20) are shown in figure 11B. A low frequency pole gives a high gain at DC to produce an accurate final pack voltage. A zero is added near 20Hz to prevent the loop phase from reaching 180 degrees. A final pole is added near 1kHz to provide a high frequency noise filter.

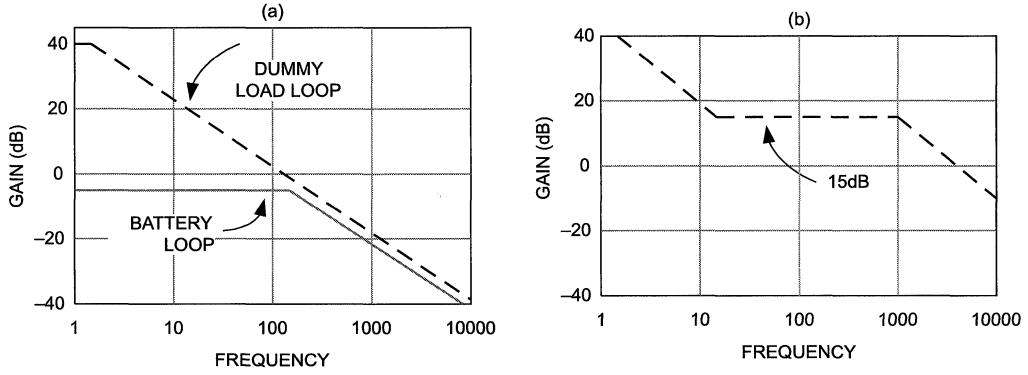

Figure 11. Voltage Feedback. (a) uncompensated voltage loop, (b) voltage amplifier compensation

Transformer Design

The first step in the design of the transformer is to determine the proper cross sectional area of the ferrite core [7]. The required cross sectional area (A_C) of the core is based on the number of turns (N) and the maximum flux density (B_{MAX}) allowed before saturation.

$$V_{IN} \bullet T_{ON} = 4x10^{-4} \bullet B_{MAX} \bullet A_C \bullet N \qquad (6)$$

According to Gauss' Law (equation 6) this occurs when the product of input voltage (V_{IN}) and on-time (T_{ON}) is at a maximum. The required winding area (Aw) of the bobbin is determined from the wire gauge and number of turns for the various windings. Since wire losses are resistive, RMS current should be used when calculating current density in the wires. An EDF20 core set made by Phillips provides adequate core and winding areas for the flyback transformer. The transformer has a small footprint, measuring 20mm per side. Coiltronics (407-241-7876) provided a custom transformer for the charger [Part Number - CTX08 13959].

Minimum inductance values are required on the primary and secondary windings, to assure that the charger always operates with discontinuous current. These inductance values are achieved by adding the proper air gap to the center leg of the flyback transformer's core. The Coiltronics transformer is gapped to give 165mH per 1000 turns (A_L). The transformer primary has 70 turns giving 800µH of primary inductance. The secondary inductance is related to the primary by $1/N^2$, giving 8µH of secondary inductance. Figure 12 illustrates the current in the flyback transformer during a switching period.

The charger operates at 100kHz, leaving 10µSec (T_{PERIOD}) for the primary inductance to charge to a peak current and the secondary inductance to discharge into the load. The converter approaches continuous current conduction when the input voltage and the battery voltage are at a minimum and when the converter is in the bulk charge state. In this state, the pack has a minimum of 5 volts and the transformer secondary will be clamped to 5V plus two diode drops during discharge ($V_{DISCHARGE}$). For an average battery current of 1.2A, the peak secondary current and discharge time can be determined by solving equation 7 and equation 8.

The secondary peak current is calculated to be 4A with a corresponding discharge time of 5.6µS. With 130V DC on the input capacitor, the maximum on-time is calculated to be 2.6µS. This leaves 1.8µS of discontinuous current margin for component variations.

$$I_{BATTERY\_AVERAGE} = \frac{T_{DISCHARGE}}{2 \bullet T_{PERIOD}} \bullet I_{PEAK\_SECONDARY} \qquad (7)$$

$$V_{DISCHARGE} \bullet T_{DISCHARGE} = L_{SECONDARY} \bullet I_{PEAK\_SECONDARY} \qquad (8)$$

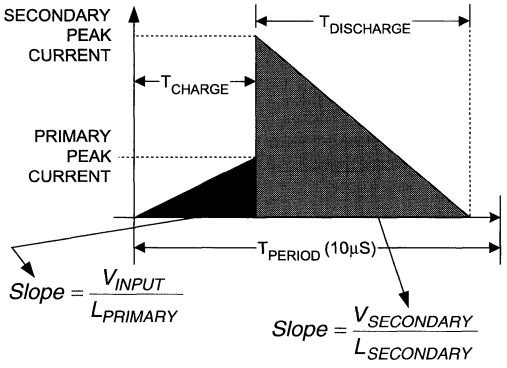

Figure 12. Flyback Transformer Current.

Summary

A high frequency off-line battery charger has been presented that offers a compact and lightweight solution when compared to a design based on a 60Hz transformer. By using dedicated ICs, parts count is minimized, increasing system reliability and reducing cost. The charger incorporates all of the features necessary to assure safety, long life, and rapid charging for Lithium-Ion cells. The final board measurements are shown in figure 13 along with component placement. A parts list for the charger is given in Table 1.

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[1] M. Juzkow and C. St. Louis of Moli Energy, *Designing Lithium-Ion Batteries into Today's Portable Products.* Portable by Design Conference 1996

[2] P. Bennett and G. Braun of Energizer Power Systems, *Introduction to Applying Lithium-Ion Batteries.* Portable by Design Conference 1997

[3] Unitrode Corporation Power Supply Design Seminar 900, *Line input AC to DC Conversion and Input Filter Capacitor Selection*, topic I1.

[4] Unitrode Corporation Product Data Book (1997), *UCC1809 Economy Primary Side Controller.*

[5] Unitrode Corporation Product Data Book (1997), *UCC3956 Switch Mode Lithium-Ion Battery Charger Controller.*

[6]. Lloyd Dixon, Unitrode Corporation Power Supply Design Seminar 1100, *Control Loop Cookbook Appendix C.*

[7] Magnetics Ferrite Cores Catalog (1991), *Transformer Core Size Selection*, Page 4.3.

For more complete information, pin descriptions and specifications for the UCC3809 Primary Side Controller and the UCC3956 Battery Charger Controller see the UCC3809 and/or the UCC3956 data sheet or contact your Unitrode Field Applications Engineer at (603) 424–2410.

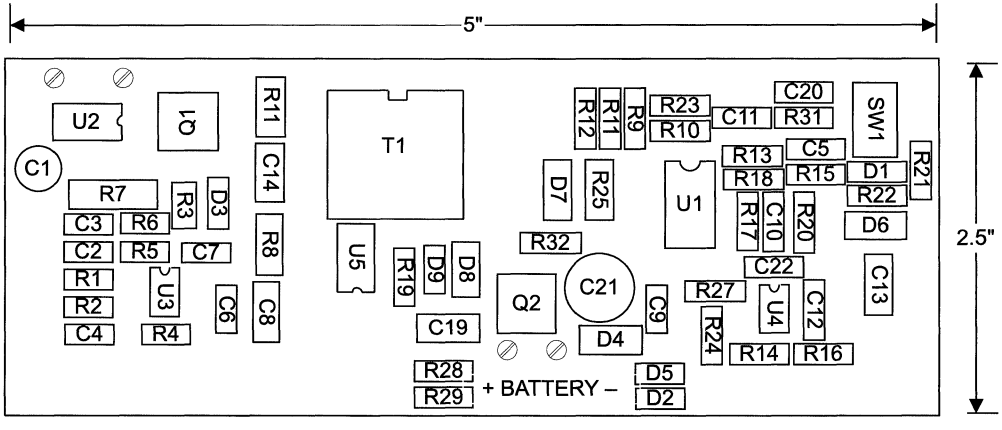

Figure 13. Final Board Size and Component Placement

Table 1. Charger Parts List

Reference Designator	Description	Manufacturer	Part Number
C1	33µF, 250V Aluminum Electrolytic Capacitor	Panasonic	ECA-2EM330
C2, C5, C6, C7, C9, C22	0.1µF, ceramic chip cap, 1206 package		
C3	120pF, ceramic chip cap, 1206 package		
C4	1000pF, ceramic chip cap, 1206 package		
C8	10µF, tantalum capacitor, C case size		
C10	0.18µF, ceramic chip cap, 1206 package		
C11	2200pF, ceramic chip cap, 1206 package		
C12	4700pF, ceramic chip cap, 1206 package		
C13	2.2µF, tantalum capacitor,		
C14	100µF, 500V Mica Capacitor		
C19	22µF, tantalum capacitor,		
C21	1000µF, 16V Aluminum Electrolytic Capacitor	Panasonic	ECE-A1CU102
D1,D3, D8, D9	General purpose diode, mini-melf package	Digikey	DL4148MSCT
D2, D5	SMD LEDs, 1206 package		
D4, D7	3A Schottky Diodes	General Instruments	SK34
D6	5V, 500mW, zener diode		
D10	18V zener diode		
Q1	Surface mount 400V Mosfet	International Rectifier	IRF720S
Q2	Surface mount 55V Mosfet	International Rectifier	IRFR1205
R1, R9, R23, R14, R16	10.0k, SMT resistor, 1206 package		
R2, R28, R29	2.87k, SMT resistor, 1206 package		
R3	10Ω, SMT resistor, 1206 package		
R4	274Ω, SMT resistor, 1206 package		
R5, R6, R24	2.2k, SMT resistor, 1206 package		
R7	2.2Ω, 1W surface mount	Digikey	P2.2UCT
R8	100k, 1W axial		
R10, R12	2.2k, SMT resistor, 1206 package		
R11	750Ω, 1W axial		
R15, R18	15k, SMT resistor, 1206 package		
R17	162k, SMT resistor, 1206 package		
R19, R27	150Ω, SMT resistor, 1206 package		
R20, R22	500k, SMT resistor, 1206 package		
R13,R21	50k, SMT resistor, 1206 package		
R25	0.1Ω, 1W surface mount		
R32	150Ω, 1W axial		

Table 1. Charger Parts List (continued)

S1	Momentary push switch, SMT		
T1	CTX08, 13959-X5	Coiltronics	
U1	UCC3954 in 20 pin SOIC package	Unitrode	
U2	Diode Bridge		

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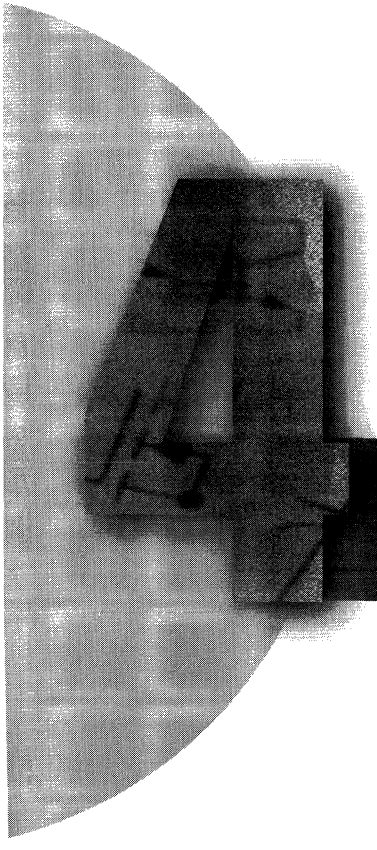


Battery Capacity-Monitoring ICs

Battery Capacity-Monitoring ICs Selection Guide

Unitrode's Gas Gauge ICs measure the available charge, calculate self-discharge, and communicate the available charge of a battery pack over a serial port or by directly driving an LED display.

- ➤ Accurate measurement of available charge for nickel cadmium, nickel metal-hydride, lithium ion, lead-acid batteries, and primary lithium
- ➤ Designed for battery-pack integration
- ➤ 150µA or less typical operating current
- ➤ Serial port or direct LED display for remaining battery capacity indication
- ➤ Available capacity is compensated for charge/discharge rate and temperature
- ➤ Accurately measures across a wide range of currents

Battery Technology	Approximate Pack Capacity (mAh)	Communication Interface	Additional Key Features	Pins / Package	Part Number	Page Number
NiCd/NiMH	800-5000	1-wire DQ	5 or 6 LED outputs	16 /SOIC	bq2010	4-3
			Slow-charge control	16 /SOIC	bq2012	4-81
			External charge-control support	16 /SOIC	bq2014	4-123
		1-wire HDQ	Register-compatible with bq2050H	16 /SOIC	bq2014H+	4-149
NiCd	800-2000	1-wire DQ	See bq2011 Family Selection Guide on page 4-2	16 /SOIC	bq2011 bq2011J bq2011K	4-24, 4-45, 4-63
NiCd/NiMH/ Lead Acid	2000-10,000	1-wire HDQ	Programmable offset and load compensation	16 /SOIC	bq2013H	4-103
Li-Ion	800-5000	1-wire DQ	Remaining power (Wh) indication	16 /SOIC	bq2050	4-215
		1-wire HDQ	Register-compatible with bq2014H	16 /SOIC	bq2050H	4-237
Primary Lithium	800-15,000	1-wire HDQ	Programmable discharge efficiency compensation	16 /SOIC	bq2052+	4-259
NiCd/NiMH Lead Acid/ Li-Ion	800-10,000	2-wire SMBus	SBS rev. 1.0-compliant	16 /SOIC	bq2040	4-185
			SBS rev. 0.95-compliant	16 / SOIC	bq2092	4-314
			SBS rev. 1.0-compliant with 5 LEDs	16 /SOIC	bq2945	4-340
		2-wire SMBus or 1-wire HDQ16	SBS rev. 1.1-compliant	28 / SSOP	bq2060+	4-276
Any	Any	1-wire HDQ	Analog peripheral for µC	8 / SOIC or TSSOP	bq2018	4-170

+ New Product

bq2011 Family Selection Guide

The bq2011 Gas Gauge ICs provide accurate capacity monitoring of rechargeable batteries in high discharge rate environments. The ICs can monitor a wide range of charge/discharge currents using the onboard V-to-F converter and a low-value sense resistor. The ICs track remaining capacity (NAC) and compensate it for battery self-discharge, charge/discharge rate, and temperature. Five LEDs can communicate remaining capacity in 20% increments. A serial port allows a host microcontroller to access the nonvolatile memory registers containing battery capacity, voltage, temperature, and other critical parameters.

- ➤ Accurate measurement of available charge in rechargeable batteries
- ➤ Designed for NiCd high discharge rate applications
- ➤ Drives 5 LEDs for capacity indication
- ➤ Automatic charge self-discharge and discharge compensation
- ➤ Low operating current
- ➤ 16-pin narrow SOIC

Feature	Part Number bq2011	bq2011J	bq2011K
Display	Relative or absolute	Absolute	Absolute
Programmed Full Count (PFC) range	4.5–10.5mVh	2.21–3.81mVh	2.21–3.81mVh
Nominal Available Capacity (NAC) on reset	NAC = 0	NAC = PFC or 0	NAC = PFC or 0
Self-discharge rate	NAC/80	NAC/80 or disabled	NAC/80 or disabled
Charge compensation	75–95% based on rate and temperature	65–95% based on rate and temperature	70–95% based on rate and temperature
Discharge compensation	75–100% plus temperature compensation	75–100% plus temperature compensation	100%
End-of-discharge voltage	0.9V/cell	0.9V/cell	0.96–1.16V/cell
Page number	4-24	4-45	4-63

bq2010

Gas Gauge IC

Features

- Conservative and repeatable measurement of available charge in rechargeable batteries
- Designed for battery pack integration
  - 120µA typical standby current
  - Small size enables implementations in as little as ½ square inch of PCB
- Integrate within a system or as a stand-alone device
  - Display capacity via single-wire serial communication port or direct drive of LEDs
- Measurements compensated for current and temperature
- Self-discharge compensation using internal temperature sensor
- Accurate measurements across a wide range of current (> 500:1)
- 16-pin narrow SOIC

General Description

The bq2010 Gas Gauge IC is intended for battery-pack or in-system installation to maintain an accurate record of a battery's available charge. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery.

NiMH and NiCd battery self-discharge is estimated based on an internal timer and temperature sensor. Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and self-discharge calculations to provide available charge information across a wide range of operating conditions. Battery capacity is automatically recalibrated, or "learned," in the course of a discharge cycle from full to empty.

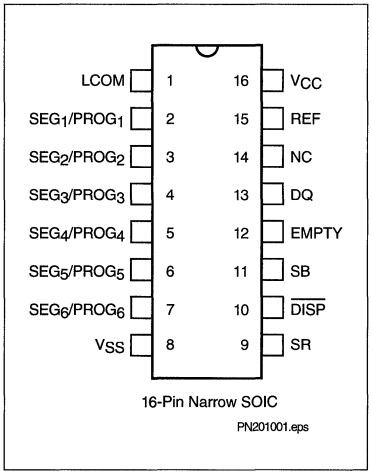
Nominal available charge may be directly indicated using a five- or six-segment LED display. These segments are used to indicate graphically the nominal available charge.

The bq2010 supports a simple single-line bidirectional serial link to an external processor (common ground). The bq2010 outputs battery information in response to external commands over the serial link.

The bq2010 may operate directly from 3 or 4 cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide V_{CC} across a greater number of cells.

Internal registers include available charge, temperature, capacity, battery ID, battery status, and programming pin settings. To support subassembly testing, the outputs may also be controlled. The external processor may also overwrite some of the bq2010 gas gauge data registers.

Pin Connections



16-Pin Narrow SOIC

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Pin Names

LCOM	LED common output
$SEG_1/PROG_1$	LED segment 1/ program 1 input
$SEG_2/PROG_2$	LED segment 2/ program 2 input
$SEG_3/PROG_3$	LED segment 3/ program 3 input
$SEG_4/PROG_4$	LED segment 4/ program 4 input
$SEG_5/PROG_5$	LED segment 5/ program 5 input
$SEG_6/PROG_6$	LED segment 6/ program 6 input
REF	Voltage reference output
NC	No connect
DQ	Serial communications input/output
EMPTY	Empty battery indicator output
SB	Battery sense input
$\overline{DISP}$	Display control input
SR	Sense resistor input
V_{CC}	3.0–6.5V
V_{SS}	System ground

Pin Descriptions

LCOM **LED common output**

Open-drain output switches V_{CC} to source current for the LEDs. The switch is off during initialization to allow reading of the soft pull-up or pull-down program resistors. LCOM is also high impedance when the display is off.

SEG_1–SEG_6 **LED display segment outputs (dual function with $PROG_1$–$PROG_6$)**

Each output may activate an LED to sink the current sourced from LCOM.

$PROG_1$–$PROG_2$ **Programmed full count selection inputs (dual function with SEG_1–SEG_2)**

These three-level input pins define the programmed full count (PFC) thresholds described in Table 2.

$PROG_3$–$PROG_4$ **Gas gauge rate selection inputs (dual function with SEG_3–SEG_4)**

These three-level input pins define the scale factor described in Table 2.

$PROG_5$ **Self-discharge rate selection (dual function with SEG_5)**

This three-level input pin defines the selfdischarge compensation rate shown in Table 1.

$PROG_6$ **Display mode selection (dual function with SEG_6)**

This three-level pin defines the display operation shown in Table 1.

NC **No connect**

SR **Sense resistor input**

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied to the high side of the sense resistor. $V_{SR} < V_{SS}$ indicates discharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2010 is $V_{SR} + V_{OS}$ (see Table 5).

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ tied to V_{CC} allows $PROG_X$ to connect directly to V_{CC} or V_{SS} instead of through a pull-up or pull-down resistor. $\overline{DISP}$ floating allows the LED display to be active during discharge or charge if the NAC registers update at a rate equivalent to $|V_{SRO}| \geq 4mV$. $\overline{DISP}$ low activates the display. See Table 1.

SB **Secondary battery input**

This input monitors the single-cell voltage potential through a high-impedance resistive divider network for end-of-discharge voltage (EDV) thresholds, maximum charge voltage (MCV), and battery removed.

EMPTY **Battery empty output**

This open-drain output becomes high-impedance on detection of a valid end-of-discharge voltage (V_{EDVF}) and is low following the next application of a valid charge.

DQ **Serial I/O pin**

This is an open-drain bidirectional pin.

REF **Voltage reference output for regulator**

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} **Supply voltage input**

V_{SS} **Ground**

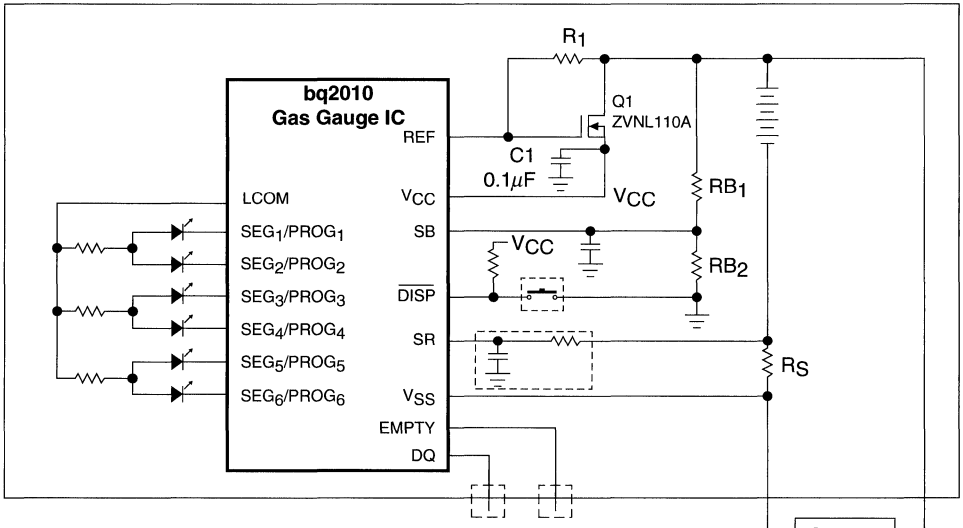
Functional Description

General Operation

The bq2010 determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2010 measures discharge and charge currents, estimates self-discharge, monitors the battery for low-battery voltage thresholds, and compensates for temperature and charge/discharge rates. The charge measurement derives from monitoring the voltage across a small-value series sense resistor between the negative battery terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2010 using the LED display capability as a charge-state indicator. The bq2010 can be configured to display capacity in either a relative or an absolute display mode. The relative display mode uses the last measured discharge capacity of the battery as the battery "full" reference. The absolute display mode uses the programmed full count (PFC) as the full reference, forcing each segment of the display to represent a fixed amount of charge. A push-button display feature is available for momentarily enabling the LED display.

The bq2010 monitors the charge and discharge currents as a voltage across a sense resistor (see R_S in Figure 1). A filter between the negative battery terminal and the SR pin may be required if the rate of change of the battery current is too great.



Indicates optional.

Directly connect to V_{CC} across 3 or 4 cells (3 to 5.6V nominal) with a resistor and a Zener diode to limit voltage during charge. Otherwise, R1, C1, and Q1 are needed for regulation of >4 cells. The value of R1 depends on the number of cells.

Programming resistors (6 max.) and ESD-protection diodes are not shown.

R-C on SR may be required, application-specific.

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Figure 1. Battery Pack Application Diagram—LED Display

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2010 monitors the single-cell battery potential through the SB pin. The single-cell voltage potential is determined through a resistor/divider network according to the following equation:

$$\frac{RB_1}{RB_2} = N - 1$$

where N is the number of cells, RB_1 is connected to the positive battery terminal, and RB_2 is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV) and for maximum cell voltage (MCV). EDV threshold levels are used to determine when the battery has reached an "empty" state, and the MCV threshold is used for fault detection during charging.

Two EDV thresholds for the bq2010 are fixed at:

$$V_{EDV1} \text{ (early warning)} = 1.05V$$

$$V_{EDVF} \text{ (empty)} = 0.95V$$

If V_{SB} is below either of the two EDV thresholds, the associated flag is latched and remains latched, independent of V_{SB}, until the next valid charge. EDV monitoring may be disabled under certain conditions as described in the next paragraph.

During discharge and charge, the bq2010 monitors V_{SR} for various thresholds. These thresholds are used to compensate the charge and discharge rates. Refer to the count compensation section for details. EDV monitoring is disabled if $V_{SR} \leq$ -250mV typical and resumes ½ second after $V_{SR} >$ -250mV.

EMPTY Output

The EMPTY output switches to high impedance when $V_{SB} < V_{EDVF}$ and remains latched until a valid charge occurs. The bq2010 also monitors V_{SB} relative to V_{MCV}, 2.25V. V_{SB} falling from above V_{MCV} resets the device.

Reset

The bq2010 recognizes a valid battery whenever V_{SB} is greater than 0.1V typical. V_{SB} rising from below 0.25V or falling from above 2.25V resets the device. Reset can also be accomplished with a command over the serial port as described in the Reset Register section.

Temperature

The bq2010 internally determines the temperature in 10°C steps centered from -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available charge display translation. The temperature range is available over the serial port in 10°C increments as shown below:

TMPGG (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2010 measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (SB and V_{CC}) should be placed as close as possible to the SB and V_{CC} pins, respectively, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor capacitor should be placed as close as possible to the SR pin.
- The sense resistor (R_{SNS}) should be as close as possible to the bq2010.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2010. The bq2010 accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge and discharge currents are temperature and rate compensated, whereas self-discharge is only temperature compensated.

The main counter, Nominal Available Charge (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2010 adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the Programmed Full Count (PFC) shown in Table 2. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. **Last Measured Discharge (LMD) or learned battery capacity:**

   LMD is the last measured discharge capacity of the battery. On initialization (application of V_{CC} or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register (DCR) representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

2. **Programmed Full Count (PFC) or initial battery capacity:**

   The initial LMD and gas gauge rate values are programmed by using $PROG_1$–$PROG_4$. The PFC also provides the 100% reference for the absolute display mode. The bq2010 is configured for a given application by selecting a PFC value from Table 2. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

   Battery capacity (mAh) * sense resistor (Ω) = PFC (mVh)

   Selecting a PFC slightly less than the rated capacity for absolute mode provides capacity above the full reference for much of the battery's life.

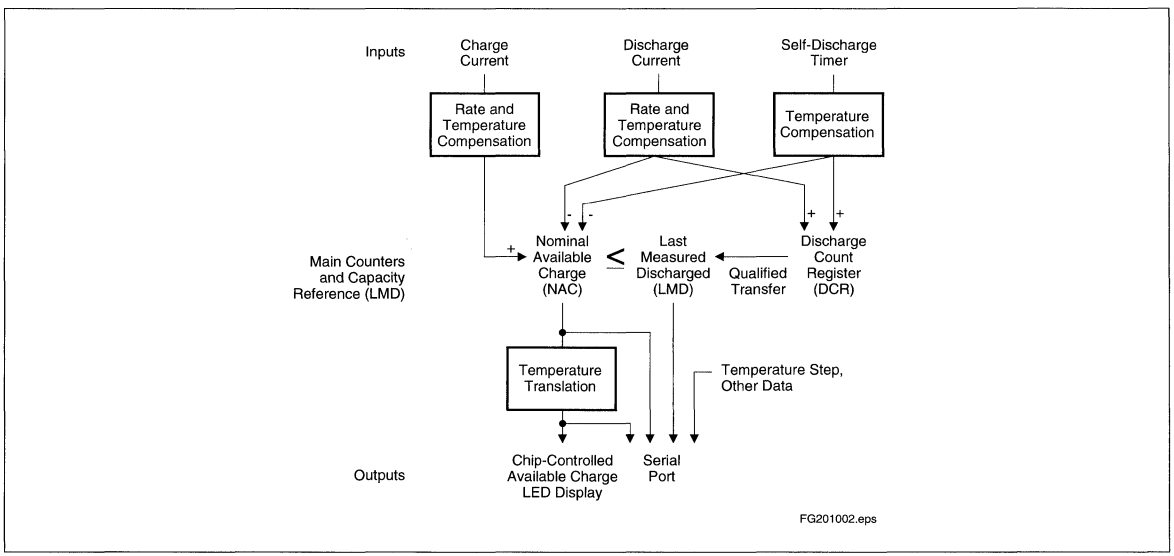


Figure 2. Operational Overview

5/18

Example: Selecting a PFC Value

Given:

Sense resistor = 0.1Ω
Number of cells = 6
Capacity = 2200mAh, NiCd battery
Current range = 50mA to 2A
Absolute display mode
Serial port only
Self-discharge = $^{C}/_{64}$
Voltage drop over sense resistor = 5mV to 200mV

Therefore:

2200mAh * 0.1Ω = 220mVh

Select:

PFC = 33792 counts or 211mVh
$PROG_1$ = float
$PROG_2$ = float
$PROG_3$ = float
$PROG_4$ = low
$PROG_5$ = float
$PROG_6$ = float

The initial full battery capacity is 211mVh (2110mAh) until the bq2010 "learns" a new capacity with a qualified discharge from full to EDV1.

Table 1. bq2010 Programming

Pin Connection	$PROG_5$ Self-Discharge Rate	$PROG_6$ Display Mode	$\overline{DISP}$ Display State
H	Disabled	Absolute NAC = PFC on reset	LED disabled
Z	$^{NAC}/_{64}$	Absolute NAC = 0 on reset	LED-enabled on discharge or charge when equivalent $\lvert V_{SRO} \rvert \geq 4mV$
L	$^{NAC}/_{47}$	Relative NAC = 0 on reset	LED on

Note: $PROG_5$ and $PROG_6$ states are independent.

Table 2. bq2010 Programmed Full Count mVh Selections

$PROG_x$		Programmed Full Count (PFC)	$PROG_4$ = L			$PROG_4$ = Z			Units
1	2		PROG3 = H	PROG3 = Z	PROG3 = L	PROG3 = H	PROG3 = Z	PROG3 = L	
-	-	-	Scale = 1/80	Scale = 1/160	Scale = 1/320	Scale = 1/640	Scale = 1/1280	Scale = 1/2560	mVh/ count
H	H	49152	614	307	154	76.8	38.4	19.2	mVh
H	Z	45056	563	282	141	70.4	35.2	17.6	mVh
H	L	40960	512	256	128	64.0	32.0	16.0	mVh
Z	H	36864	461	230	115	57.6	28.8	14.4	mVh
Z	Z	33792	422	211	106	53.0	26.4	13.2	mVh
Z	L	30720	384	192	96.0	48.0	24.0	12.0	mVh
L	H	27648	346	173	86.4	43.2	21.6	10.8	mVh
L	Z	25600	320	160	80.0	40.0	20.0	10.0	mVh
L	L	22528	282	141	70.4	35.2	17.6	8.8	mVh
VSR equivalent to 2 counts/sec. (nom.)			90	45	22.5	11.25	5.6	2.8	mV

3. **Nominal Available Charge (NAC):**

   NAC counts up during charge to a maximum value of LMD and down during discharge and self-discharge to 0. NAC is reset to 0 on initialization ($PROG_6$ = Z or low) and on the first valid charge following discharge to EDV1. NAC is set to PFC on initialization if $PROG_6$ = high. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = LMD.

4. **Discharge Count Register (DCR):**

   The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC = LMD. The DCR does not roll over but stops counting when it reaches ffffh.

   The DCR value becomes the new LMD value on the first charge after a valid discharge to V_{EDV1} if:

   No valid charge initiations (charges greater than 256 NAC counts, where $V_{SRO} > V_{SRQ}$) occurred during the period between NAC = LMD and EDV1 detected.

   The self-discharge count is not more than 4096 counts (8% to 18% of PFC, specific percentage threshold determined by PFC).

   The temperature is ≥ 0°C when the EDV1 level is reached during discharge.

   The valid discharge flag (VDQ) indicates whether the present discharge is valid for LMD update.

Charge Counting

Charge activity is detected based on a positive voltage on the V_{SR} input. If charge activity is detected, the bq2010 increments NAC at a rate proportional to V_{SRO} and, if enabled, activates an LED display if the rate is equivalent to V_{SRO} > 4mV. Charge actions increment the NAC after compensation for charge rate and temperature.

The bq2010 determines charge activity sustained at a continuous rate equivalent to $V_{SRO} > V_{SRQ}$. A valid charge equates to sustained charge activity greater than 256 NAC counts. Once a valid charge is detected, charge counting continues until V_{SRO} (V_{SR} + V_{OS}) falls below V_{SRQ}. V_{SRQ} is a programmable threshold as described in the Digital Magnitude Filter section. The default value for V_{SRQ} is 375µV.

Discharge Counting

All discharge counts where $V_{SRO} < V_{SRD}$ cause the NAC register to decrement and the DCR to increment. Exceeding the fast discharge threshold (FDQ) if the rate is equivalent to V_{SRO} < -4mV activates the display, if enabled. The display becomes inactive after V_{SRO} rises above -4mV. V_{SRD} is a programmable threshold as described in the Digital Magnitude Filter section. The default value for V_{SRD} is -300µV.

Self-Discharge Estimation

The bq2010 continuously decrements NAC and increments DCR for self-discharge based on time and temperature. The self-discharge count rate is programmed to be a nominal $1/64$ * NAC, $1/47$ * NAC per day, or disabled as selected by $PROG_5$. This is the rate for a battery whose temperature is between 20°–30°C. The NAC register cannot be decremented below 0.

Count Compensations

The bq2010 determines fast charge when the NAC updates at a rate of ≥ 2 counts/sec. Charge and discharge activity is compensated for temperature and charge/discharge rate before updating the NAC and/or DCR. Self-discharge estimation is compensated for temperature before updating the NAC or DCR.

Charge Compensation

Two charge efficiency compensation factors are used for trickle charge and fast charge. Fast charge is defined as a rate of charge resulting in ≥ 2 NAC counts/sec (≥ 0.15C to 0.32C depending on PFC selections; see Table 2). The compensation defaults to the fast charge factor until the actual charge rate is determined.

Temperature adapts the charge rate compensation factors over three ranges between nominal, warm, and hot temperatures. The compensation factors are shown below.

Charge Temperature	Trickle Charge Compensation	Fast Charge Compensation
<30°C	0.80	0.95
30–40°C	0.75	0.90
> 40°C	0.65	0.80

Discharge Compensation

Corrections for the rate of discharge are made by adjusting an internal discharge compensation factor. The discharge compensation factor is based on the namically measured V_{SR}.

7/18

The compensation factors during discharge are:

Approximate V_{SR} Threshold	Discharge Compensation Factor	Efficiency
V_{SR} > -150 mV	1.00	100%
V_{SR} < -150 mV	1.05	95%

Temperature compensation during discharge also takes place. At lower temperatures, the compensation factor increases by 0.05 for each 10°C temperature step below 10°C.

$$\text{Comp. factor} = 1.0 + (0.05 * N)$$

Where N = Number of 10°C steps below 10°C and $-150mV < V_{SR} < 0$.

For example:

T > 10°C : Nominal compensation, N = 0

0°C < T < 10°C: N = 1 (i.e., 1.0 becomes 1.05)

-10°C < T < 0°C: N = 2 (i.e., 1.0 becomes 1.10)

-20°C < T < -10°C: N = 3 (i.e., 1.0 becomes 1.15)

-20°C < T < -30°C: N = 4 (i.e., 1.0 becomes 1.20)

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of $1/64 * NAC$, $1/47 * NAC$ per day, or disabled. This is the rate for a battery within the 20–30°C temperature range (TMPGG = 6x). This rate varies across 8 ranges from <10°C to >70°C, doubling with each higher temperature step (10°C). See Table 3.

Table 3. Self-Discharge Compensation

Temperature Range	Typical Rate	
	$PROG_5$ = Z	$PROG_5$ = L
< 10°C	$NAC/256$	$NAC/188$
10–20°C	$NAC/128$	$NAC/94$
20–30°C	$NAC/64$	$NAC/47$
30–40°C	$NAC/32$	$NAC/23.5$
40–50°C	$NAC/16$	$NAC/11.8$
50–60°C	$NAC/8$	$NAC/5.88$
60–70°C	$NAC/4$	$NAC/2.94$
> 70°C	$NAC/2$	$NAC/1.47$

Digital Magnitude Filter

The bq2010 has a programmable digital filter to eliminate charge and discharge counting below a set threshold. The default setting is -0.30mV for V_{SRD} and +0.38mV for V_{SRQ}. The proper digital filter setting can be calculated using the following equation. Table 4 shows typical digital filter settings.

$$V_{SRD}\ (mV) = -45 / DMF$$

$$V_{SRQ}\ (mV) = -1.25 * V_{SRD}$$

Table 4. Typical Digital Filter Settings

DMF	DMF Hex.	V_{SRD} (mV)	V_{SRQ} (mV)
75	4B	-0.60	0.75
100	64	-0.45	0.56
150 (default)	96	-0.30	0.38
175	AF	-0.26	0.32
200	C8	-0.23	0.28

Error Summary

Capacity Inaccurate

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see the DCR description on page 7). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

A Capacity Inaccurate counter (CPI) is maintained and incremented each time a valid charge occurs (qualified by NAC; see the CPI register description) and is reset whenever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

Current-Sensing Error

Table 5 illustrates the current-sensing error as a function of V_{SR}. A digital filter eliminates charge and discharge counts to the NAC register when V_{SRO} (V_{SR} + V_{OS}) is between V_{SRQ} and V_{SRD}.

Communicating With the bq2010

The bq2010 includes a simple single-pin (DQ plus return) serial data interface. A host processor uses the interface to access various bq2010 registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain DQ pin on

Table 5. bq2010 Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
V_{OS}	Offset referred to V_{SR}	± 50	± 150	µV	$\overline{DISP}$ = V_{CC}.
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

the bq2010 should be pulled up by the host system or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2010. The command directs the bq2010 either to store the next eight bits of data received to a register specified by the command byte or to output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 333 bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2010 may be sampled using the pulse-width capture timers available on some microcontrollers.

Communication is normally initiated by the host processor sending a BREAK command to the bq2010. A BREAK is detected when the DQ pin is driven to a logic-low state for a time, t_B or greater. The DQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2010 is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2010 taking the DQ pin to a logic-low state for a period, $t_{STRH,B}$. The next section is the actual data transmission, where the data should be valid by a period, t_{DSU}, after the negative edge used to start communication. The data should be held for a period, t_{DV}, to allow the host or bq2010 to sample the data bit.

The final section is used to stop the transmission by returning the DQ pin to a logic-high state by at least a period, t_{SSU}, after the negative edge used to start communication. The final logic-high state should be held until a period, t_{SV}, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2010 is always performed with the least-significant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2010 NAC register.

bq2010 Registers

The bq2010 command and status registers are listed in Table 6 and described below.

Command Register (CMDR)

The write-only CMDR register is accessed when eight valid command bits have been received by the bq2010. The CMDR register contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function.

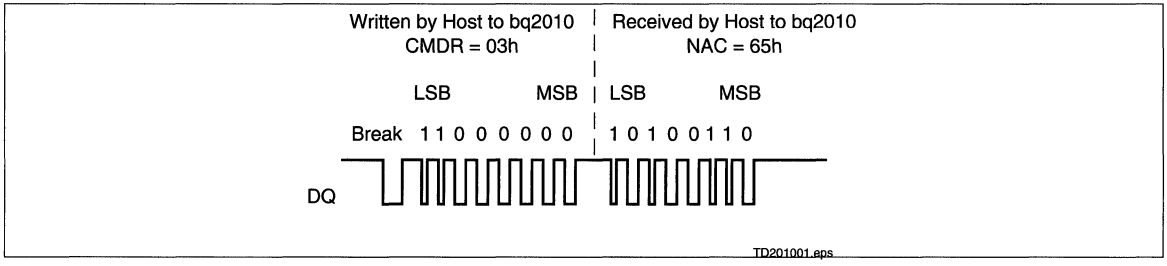


Figure 3. Typical Communication with the bq2010

9/18

Table 6. bq2010 Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	Command register	00h	Write	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
FLGS1	Primary status flags register	01h	Read	CHGS	BRP	BRM	CI	VDQ	n/u	EDV1	EDVF
TMPGG	Temperature and gas gauge register	02h	Read	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available charge high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	Nominal available charge low byte register	17h	Read	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	Read	CR	DR2	DR1	DR0	n/u	n/u	n/u	OVLD
PPD	Program pin pull-down register	07h	Read	n/u	n/u	PPD6	PPD5	PPD4	PPD3	PPD2	PPD1
PPU	Program pin pull-up register	08h	Read	n/u	n/u	PPU6	PPU5	PPU4	PPU3	PPU2	PPU1
CPI	Capacity inaccurate count register	09h	Read	CPI7	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	CPI0
DMF	Digital magnitude filter register	0ah	R/W	DMF7	DMF6	DMF5	DMF4	DMF3	DMF2	DMF1	DMF0
RST	Reset register	39h	Write	RST	0	0	0	0	0	0	0

Note: n/u = not used

The W/$\overline{R}$ values are:

CMDR Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is:

0 The bq2010 outputs the requested register contents specified by the address portion of CMDR.

1 The following eight bits should be written to the register specified by the address portion of CMDR.

The lower seven-bit field of CMDR contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

CMDR Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Primary Status Flags Register (FLGS1)

The read-only FLGS1 register (address=01h) contains the primary bq2010 flags.

The ***charge status*** flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when $V_{SRO} > V_{SRQ}$. A V_{SRO} of less than V_{SRQ} or discharge activity clears CHGS.

The CHGS values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
CHGS	-	-	-	-	-	-	-

Where CHGS is:

0 Either discharge activity detected or $V_{SRO} < V_{SRQ}$

1 $V_{SRO} > V_{SRQ}$

The ***battery replaced*** flag (BRP) is asserted whenever the potential on the SB pin (relative to V_{SS}), V_{SB}, falls from above the maximum cell voltage, MCV (2.25V), or rises above 0.1V. The BRP flag is also set when the bq2010 is reset (see the RST register description). BRP is reset when either a valid charge action increments NAC to be equal to LMD, or a valid charge action is detected after the EDV1 flag is asserted. BRP = 1 signifies that the device has been reset.

The BRP values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	BRP	-	-	-	-	-	-

Where BRP is:

0 Battery is charged until NAC = LMD or discharged until the EDV1 flag is asserted

1 V_{SB} dropping from above MCV, V_{SB} rising from below 0.1V, or a serial port initiated reset has occurred

The ***battery removed*** flag (BRM) is asserted whenever the potential on the SB pin (relative to V_{SS}) rises above MCV or falls below 0.1V. The BRM flag is asserted until the condition causing BRM is removed.

The BRM values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	BRM	-	-	-	-	-

Where BRM is:

0 $0.1V < V_{SB} < 2.25V$

1 $0.1\ V > V_{SB}$ or $V_{SB} > 2.25V$

The ***capacity inaccurate*** flag (CI) is used to warn the user that the battery has been charged a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2010 is reset. The flag is cleared after an LMD update.

The CI values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	CI	-	-	-	-

Where CI is:

0 When LMD is updated with a valid full discharge

1 After the 64th valid charge action with no LMD updates or the bq2010 is reset

The ***valid discharge*** flag (VDQ) is asserted when the bq2010 is discharged from NAC=LMD. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- The self-discharge count register (SDCR) has exceeded the maximum acceptable value (4096 counts) for an LMD update.
- A valid charge action sustained at $V_{SRO} > V_{SRQ}$ for at least 256 NAC counts.
- The EDV1 flag was set at a temperature below 0°C

The VDQ values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

Where VDQ is:

0 SDCR ≥ 4096, subsequent valid charge action detected, or EDV1 is asserted with the temperature less than 0°C

1 On first discharge after NAC = LMD

The ***first end-of-discharge warning*** flag (EDV1) warns the user that the battery is almost empty. The first segment pin, SEG_1, is modulated at a 4Hz rate if the display is enabled once EDV1 is asserted, which should warn the user that loss of battery power is imminent. The EDV1 flag is latched until a valid charge has been detected.

The EDV1 values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV1	-

Where EDV1 is:

0 Valid charge action detected, $V_{SB} \geq 1.05V$

1 $V_{SB} < 1.05V$ providing that OVLD=0 (see FLGS2 register description)

The ***final end-of-discharge warning*** flag (EDVF) is used to warn that battery power is at a failure condition. All segment drivers are turned off. The EDVF flag is latched until a valid charge has been detected. The EMPTY pin is also forced to a high-impedance state on assertion of EDVF. The host system may pull EMPTY high, which may be used to disable circuitry to prevent deep-discharge of the battery.

The EDVF values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	EDVF

Where EDVF is:

0 Valid charge action detected, $V_{SB} \geq 0.95V$

1 $V_{SB} < 0.95V$ providing that OVLD=0 (see FLGS2 register description)

Temperature and Gas Gauge Register (TMPGG)

The read-only TMPGG register (address=02h) contains two data fields. The first field contains the battery temperature. The second field contains the available charge from the battery.

TMPGG Temperature Bits							
7	6	5	4	3	2	1	0
TMP3	TMP2	TMP1	TMP0	-	-	-	

The bq2010 contains an internal temperature sensor. The temperature is used to set charge and discharge efficiency factors as well as to adjust the self-discharge coefficient.

The temperature register contents may be translated as shown below.

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

The bq2010 calculates the available charge as a function of NAC, temperature, and a full reference, either LMD or PFC. The results of the calculation are available via the display port or the gas gauge field of the TMPGG register. The register is used to give available capacity in 1/16 increments from 0 to 15/16.

TMPGG Gas Gauge Bits							
7	6	5	4	3	2	1	0
-	-	-	-	GG3	GG2	GG1	GG0

The gas gauge display and the gas gauge portion of the TMPGG register are adjusted for cold temperature dependencies. A piece-wise correction is performed as follows:

Temperature	Available Capacity Calculation
> 0°C	NAC / "Full Reference"
-20°C < T < 0°C	0.75 * NAC / "Full Reference"
< -20°C	0.5 * NAC / "Full Reference"

The adjustment between > 0°C and -20°C < T < 0°C has a 10°C hysteresis.

Nominal Available Charge Registers (NACH/NACL)

The read/write NACH high-byte register (address=03h) and the read-only NACL low-byte register (address=17h) are the main gas gauging register for the bq2010. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC.

On reset, if $PROG_6$ = Z or low, NACH and NACL are cleared to 0; if $PROG_6$ = high, NACH = PFC and NACL = 0. When the bq2010 detects a valid charge, NACL resets to 0. *Writing to the NAC registers affects the available charge counts and, therefore, affects the bq2010 gas gauge operation. Do not write the NAC registers to a value greater than LMD.*

Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V_{CC} is greater than 2V. The contents of BATID have no effect on the operation of the bq2010. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2010 uses as a measured full reference. The bq2010 adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2010 updates the capacity of the battery. LMD is set to PFC during a bq2010 reset.

Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2010 flags.

The ***charge rate*** flag (CR) is used to denote the fast charge regime. Fast charge is assumed whenever a charge action is initiated. The CR flag remains asserted if the charge rate does not fall below 2 counts/sec.

The CR values are:

FLGS2 Bits							
7	6	5	4	3	2	1	0
CR	-	-	-	-	-	-	-

Where CR is:

0 When charge rate falls below 2 counts/sec

1 When charge rate is above 2 counts/sec

The fast charge regime efficiency factors are used when CR = 1. When CR = 0, the trickle charge efficiency factors are used. The time to change CR varies due to the user-selectable count rates.

The ***discharge rate*** flags, DR2–0, are bits 6–4.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-	-	-	

They are used to determine the current discharge regime as follows:

DR2	DR1	DR0	V_{SR} (V)
0	0	0	V_{SR} > -150mV
0	0	1	V_{SR} < -150mV

The ***overload*** flag (OVLD) is asserted when a discharge overload is detected, V_{SR} < -250mV. OVLD remains asserted as long as the condition persists and is cleared 0.5 seconds after V_{SR} > -250mV. The overload condition is used to stop sampling of the battery terminal characteristics for end-of-discharge determination. Sampling is re-enabled 0.5 secs after the overload condition is removed.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OVLD

DR2–0 and OVLD are set based on the measurement of the voltage at the SR pin relative to V_{SS}. The rate at which this measurement is made varies with device activity.

Program Pin Pull-Down Register (PPD)

The read-only PPD register (address=07h) contains some of the programming pin information for the bq2010. The segment drivers, SEG_{1-6}, have a corresponding PPD register location, PPD_{1-6}. A given location is set if a pull-down resistor has been detected on its corresponding segment driver. For example, if SEG_1 and SEG_4 have pull-down resistors, the contents of PPD are xx001001.

PPD/PPU Bits							
7	6	5	4	3	2	1	0
-	-	PPU_6	PPU_5	PPU_4	PPU_3	PPU_2	PPU_1
-	-	PPD_6	PPD_5	PPD_4	PPD_3	PPD_2	PPD_1

Program Pin Pull-Up Register (PPU)

The read-only PPU register (address=08h) contains the rest of the programming pin information for the bq2010. The segment drivers, SEG_{1-6}, have a corresponding PPU register location, PPU_{1-6}. A given location is set if a pull-up resistor has been detected on its corresponding segment driver. For example, if SEG_3 and SEG_6 have pull-up resistors, the contents of PPU are xx100100.

Capacity Inaccurate Count Register (CPI)

The read-only CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2010 adapts to the changing capacity over time. A complete discharge from full (NAC=LMD) to empty (EDV1=1) is required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and the self-discharge counter is less than 4096 counts.

The CPI register is incremented every time a valid charge is detected. When NAC > 0.94 * LMD, however, the CPI register increments on the first valid charge; CPI does not increment again for a valid charge until NAC < 0.94 * LMD. This prevents continuous trickle charging from incrementing CPI if self-discharge decrements NAC. The CPI register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. The CPI register is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

Digital Magnitude Filter (DMF)

The read-write DMF register (address = 0ah) provides the system with a means to change the default settings of the digital magnitude filter. By writing different values into this register, the limits of V_{SRD} and V_{SRQ} can be adjusted.

Note: Care should be taken when writing to this register. A V_{SRD} and V_{SRQ} below the specified V_{OS} may adversely affect the accuracy of the bq2010. Refer to Table 4 for recommended settings for the DMF register.

Reset Register (RST)

The reset register (address=39h) provides the means to perform a software-controlled reset of the device. By writing the RST register contents from 00h to 80h, a bq2010 reset is performed. *Setting any bit other than the most-significant bit of the RST register is* ***not allowed****, and results in improper operation of the bq2010.*

Resetting the bq2010 sets the following:

- LMD = PFC
- CPI, VDQ, NACH, and NACL = 0
- CI and BRP = 1

Note: NACH = PFC when $PROG_6$ = H. Self-discharge is disabled when $PROG_5$ = H

Display

The bq2010 can directly display capacity information using low-power LEDs. If LEDs are used, the program pins should be resistively tied to V_{CC} or V_{SS} for a program high or program low, respectively.

The bq2010 displays the battery charge state in either absolute or relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD. The sixth segment, SEG_6, is not used.

In absolute mode, each segment represents a fixed amount of charge, based on the initial PFC. In absolute mode, each segment represents 20% of the PFC, with SEG_6 representing "overfull" (charge above the PFC). As the battery wears out over time, it is possible for the LMD to be below the initial PFC. In this case, all of the LEDs may not turn on in absolute mode, representing the reduction in the actual battery capacity.

The capacity display is also adjusted for the present battery temperature. The temperature adjustment reflects the available capacity at a given temperature but does not affect the NAC register. The temperature adjustments are detailed in the TMPGG register description.

When $\overline{DISP}$ is tied to V_{CC}, the SEG_{1-6} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active

whenever the NAC registers are counting at a rate equivalent to $|V_{SRO}| \geq 4mV$. When pulled low, the segment outputs become active immediately. A capacitor tied to $\overline{DISP}$ allows the display to remain active for a short period of time after activation by a push-button switch.

The segment outputs are modulated as two banks of three, with segments 1, 3, and 5 alternating with segments 2, 4, and 6. The segment outputs are modulated at approximately 100Hz with each segment bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV1} (EDV1 = 1), indicating a low-battery condition. V_{SB} below V_{EDVF} (EDVF = 1) disables the display output.

Microregulator

The bq2010 can operate directly from 3 or 4 cells. To facilitate the power supply requirements of the bq2010, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2010 can be inexpensively built using the FET and an external resistor; see Figure 1.

4

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
REF	Relative to V_{SS}	-0.3	+8.5	V	Current limited by R1 (see Figure 1)
V_{SR}	Relative to V_{SS}	-0.3	+7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2010 application note for details).
T_{OPR}	Operating temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	0.93	0.95	0.97	V	SB
V_{EDV1}	First empty warning	1.03	1.05	1.07	V	SB
V_{SR1}	Discharge compensation threshold	-120	-150	-180	mV	SR, $V_{SR} + V_{OS}$
V_{SRO}	SR sense range	-300	-	+2000	mV	SR, $V_{SR} + V_{OS}$
V_{SRQ}	Valid charge	375	-	-	µV	$V_{SR} + V_{OS}$ (see note)
V_{SRD}	Valid discharge	-	-	-300	µV	$V_{SR} + V_{OS}$ (see note)
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	SB
V_{BR}	Battery removed/replaced	-	0.1	0.25	V	SB pulled low
		2.20	2.25	2.30	V	SB pulled high

Note: Default value; value set in DMF register. V_{OS} is affected by PC board layout. Proper layout guidelines should be followed for optimal performance. See "LayoutConsiderations."

15/18

DC Electrical Characteristics (T_A = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V, DQ = 0
		-	120	180	µA	V_{CC} = 4.25V, DQ = 0
		-	170	250	µA	V_{CC} = 6.5V, DQ = 0
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	$0 < V_{SB} < V_{CC}$
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	$V_{DISP} = V_{SS}$
I_{LCOM}	LCOM input leakage	-0.2	-	0.2	µA	$\overline{DISP} = V_{CC}$
R_{DQ}	Internal pulldown	500	-	-	KΩ	
V_{SR}	Sense resistor input	-0.3	-	2.0	V	$V_{SR} < V_{SS}$ = discharge; $V_{SR} > V_{SS}$ = charge
R_{SR}	SR input impedance	10	-	-	MΩ	$-200mV < V_{SR} < V_{CC}$
V_{IH}	Logic input high	V_{CC} - 0.2	-	-	V	$PROG_1$–$PROG_6$
V_{IL}	Logic input low	-	-	V_{SS} + 0.2	V	$PROG_1$–$PROG_6$
V_{IZ}	Logic input Z	float	-	float	V	$PROG_1$–$PROG_6$
V_{OLSL}	SEG_X output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, $I_{OLS} \leq$ 1.75mA SEG_1–SEG_6
V_{OLSH}	SEG_X output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, $I_{OLS} \leq$ 11.0mA SEG_1–SEG_6
V_{OHLCL}	LCOM output high, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{OHLCOM} = -5.25mA
V_{OHLCH}	LCOM output high, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} = 6.5V, I_{OHLCOM} = -33.0mA
I_{IH}	$PROG_{1-6}$ input high current	-	1.2	-	µA	$V_{PROG} = V_{CC}/2$
I_{IL}	$PROG_{1-6}$ input low current	-	1.2	-	µA	$V_{PROG} = V_{CC}/2$
I_{OHLCOM}	LCOM source current	-33	-	-	mA	At $V_{OHLCH} = V_{CC}$ - 0.6V
I_{OLS}	SEG_X sink current	-	-	11.0	mA	At V_{OLSH} = 0.4V
I_{OL}	Open-drain sink current	-	-	5.0	mA	At $V_{OL} = V_{SS}$ + 0.3V DQ, EMPTY
V_{OL}	Open-drain output low	-	-	0.5	V	$I_{OL} \leq$ 5mA, DQ, EMPTY
V_{IHDQ}	DQ input high	2.5	-	-	V	DQ
V_{ILDQ}	DQ input low	-	-	0.8	V	DQ
R_{PROG}	Soft pull-up or pull-down resistor value (for programming)	-	-	200	KΩ	$PROG_1$–$PROG_6$
R_{FLOAT}	Float state external impedance	-	5	-	MΩ	$PROG_1$–$PROG_6$

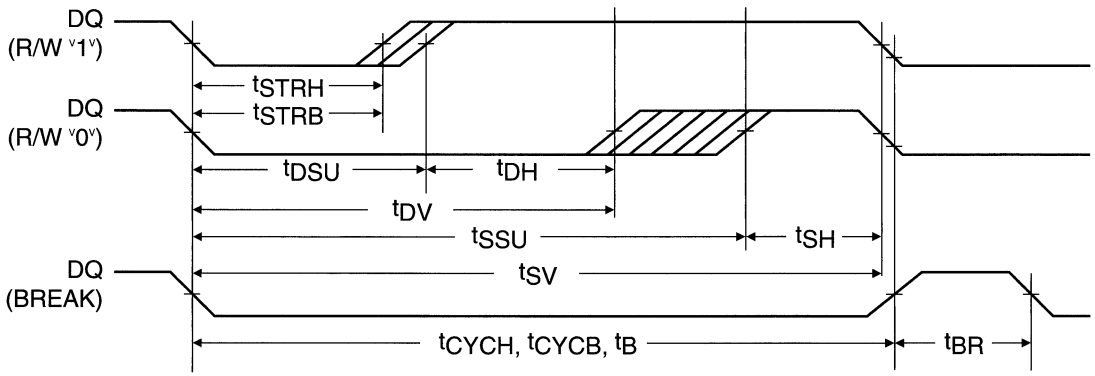
16/18

Serial Communication Timing Specification (T_A = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2010	3	-	-	ms	See note
t_{CYCB}	Cycle time, bq2010 to host	3	-	6	ms	
t_{STRH}	Start hold, host to bq2010	5	-	-	ns	
t_{STRB}	Start hold, bq2010 to host	500	-	-	µs	
t_{DSU}	Data setup	-	-	750	µs	
t_{DH}	Data hold	750	-	-	µs	
t_{DV}	Data valid	1.50	-	-	ms	
t_{SSU}	Stop setup	-	-	2.25	ms	
t_{SH}	Stop hold	700	-	-	µs	
t_{SV}	Stop valid	2.95	-	-	ms	
t_B	Break	3	-	-	ms	
t_{BR}	Break recovery	1	-	-	ms	

Note: The open-drain DQ pin should be pulled to at least V_{CC} by the host system for proper DQ operation. DQ may be left floating if the serial interface is not used.

Serial Communication Timing Illustration



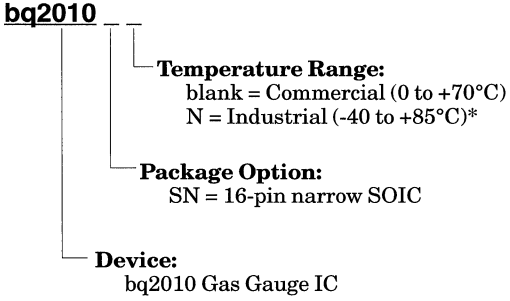
TD201002.eps

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
3	4	EDV monitoring	Was: EDV monitoring is disabled if $V_{SR} \leq$ -150mV; Is: EDV monitoring is disabled if $V_{SR} \leq$ -250mV
3	6	Table 1, $PROG_5$	Was: $PROG_5$ = H = Reserved; Is: $PROG_5$ = H = Disable self-discharge
3	7,8	Self-discharge	Add: or disabled as selected by $PROG_5$
3	11	Capacity inaccurate	Correction: CI is asserted on the 64th charge after the last LMD update or when the bq2010 is reset
3	13	Nominal available charge register	NACL stops counting when NACH reaches zero
3	13	Overload flag	Was: V_{SR} < -150mV Is: V_{SR} < -250mV

Notes: Changes 1 and 2; please refer to the *1995 Data Book*.
Change 3 = Apr. 1995 D changes from Mar. 1994 C.

Ordering Information

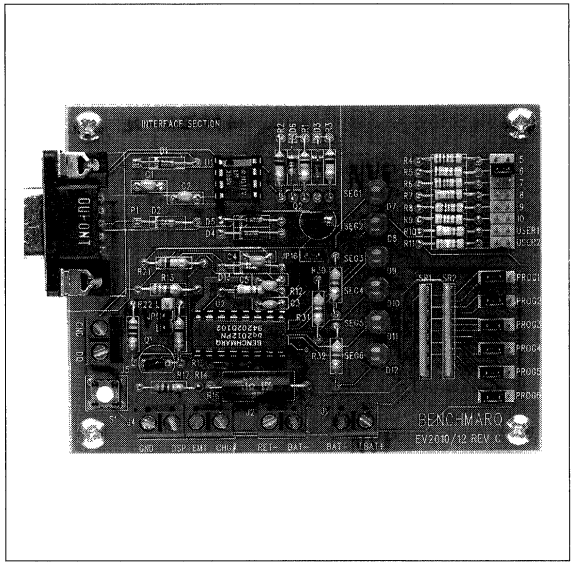


* Contact factory for availability.

bq2010 Evaluation System

Features

- bq2010 Gas Gauge IC evaluation and development system
- PC interface hardware for easy access to state-of-charge information
- Alternative terminal block for direct connection to the serial port
- Battery state-of-charge monitoring for 5- to 10-cell (series) applications (2 user-selectable options for 3, 4, or greater than 10 cells)
- On-board regulator for greater than 4-cell applications
- State-of-charge information displayed on bank of 6 LEDs
- Nominal capacity jumper-configurable
- Cell chemistry jumper-configurable
- Display mode jumper-configurable



General Description

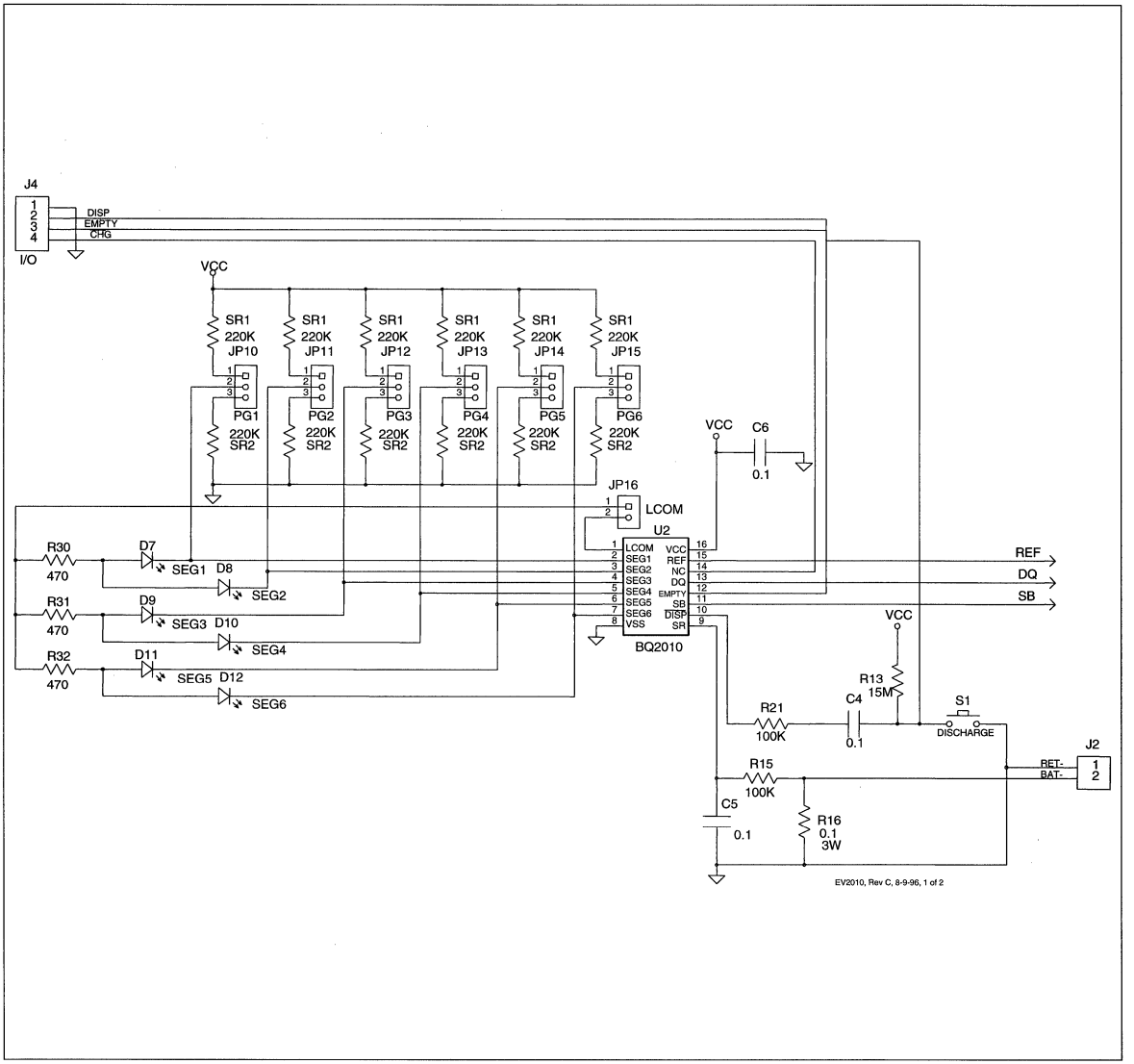
The EV2010 Evaluation System provides a development and evaluation environment for the bq2010 Gas Gauge IC. The EV2010 incorporates a bq2010, a sense resistor, and all other hardware necessary to provide a capacity monitoring function for 3 to 12 series NiCd or NiMH cells.

Hardware for a PC interface is included on the EV2010 so that easy access to the state-of-charge information can be achieved via the serial port of the bq2010. Direct connection to the serial port of the bq2010 is also made available for check-out of the final hardware/software implementation.

The menu-driven software provided with the EV2010 displays charge/discharge activity and allows user interface to the bq2010 from any standard DOS PC.

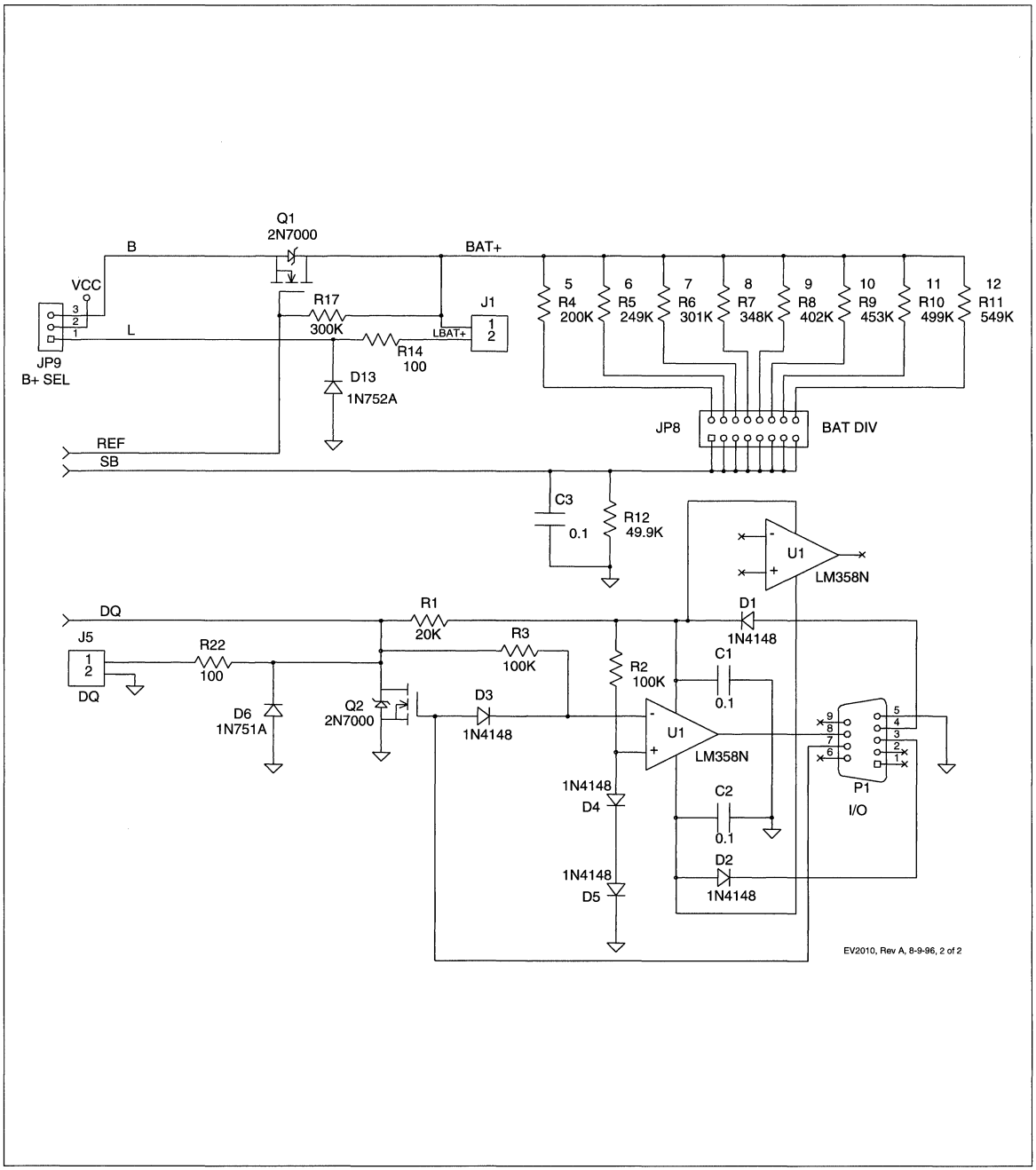
A full data sheet for this product is available on the Unitrode web site, or you may contact the factory for one.

EV2010 Board Schematic



Rev. C Board

EV2010 Board Schematic (Continued)



Rev. C Board

UNITRODE

bq2011

Gas Gauge IC for High Discharge Rates

Features

- Conservative and repeatable measurement of available charge in rechargeable batteries
- Designed for portable equipment such as power tools with high discharge rates
- Designed for battery pack integration
  - 120µA typical standby current (self-discharge estimation mode)
  - Small size enables implementations in as little as ½ square inch of PCB
- Direct drive of LEDs for capacity display
- Self-discharge compensation using internal temperature sensor
- Simple single-wire serial communications port for subassembly testing
- 16-pin narrow SOIC

General Description

The bq2011 Gas Gauge IC is intended for battery-pack installation to maintain an accurate record of available battery charge. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery. The bq2011 is designed for systems such as power tools with very high discharge rates.

Battery self-discharge is estimated based on an internal timer and temperature sensor. Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and selfdischarge calculations to provide available charge information across a wide range of operating conditions. Initial battery capacity is set using the PFC and MODE pins. Actual battery capacity is automatically "learned" in the course of a discharge cycle from full to empty and may be displayed depending on the display mode.

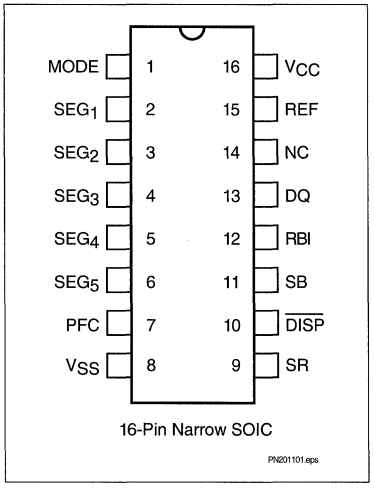
Nominal available charge may be directly indicated using a five-segment LED display. These segments are used to indicate graphically the nominal available charge.

The bq2011 supports a simple single-line bidirectional serial link to an external processor (common ground). The bq2011 outputs battery information in response to external commands over the serial link. To support subassembly testing, the outputs may also be controlled by command. The external processor may also overwrite some of the bq2011 gas gauge data registers.

The bq2011 may operate directly from four cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide V_{CC} from a greater number of cells.

Internal registers include available charge, temperature, capacity, battery ID, and battery status.

Pin Connections



16-Pin Narrow SOIC

Pin Names

MODE	Display mode output	NC	No connect
SEG_1	LED segment 1	DQ	Serial communications input/output
SEG_2	LED segment 2	RBI	Register backup input
SEG_3	LED segment 3	SB	Battery sense input
SEG_4	LED segment 4	$\overline{DISP}$	Display control input
SEG_5	LED segment 5	SR	Sense resistor input
PFC	Programmed full count selection input	V_{CC}	3.0–6.5V
REF	Voltage reference output	V_{SS}	Negative battery terminal

Pin Descriptions

MODE **Display mode output**

When left floating, this output selects relative mode for capacity display. If connected to the anode of the LEDs to source current, absolute mode is selected for capacity display. See Table 1.

SEG_1–SEG_5 **LED display segment outputs**

Each output may activate an LED to sink the current sourced from MODE, the battery, or V_{CC}.

PFC **Programmed full count selection input**

This three-level input pin defines the programmed full count (PFC) thresholds and scale selections described in Table 1. The state of the PFC pin is only read immediately after a reset condition.

SR **Sense resistor input**

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied to the low side of the sense resistor. $V_{SR} > V_{SS}$ indicates discharge, and $V_{SR} < V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2011 is $V_{SR} + V_{OS}$ (see Table 3).

NC **No connect**

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ floating allows the LED display to be active during charge and discharge if $V_{SRO} < -1mV$ (charge) or $V_{SRO} > 2mV$ (discharge). Transitioning $\overline{DISP}$ low activates the display for 4 ± 0.5 seconds.

SB **Secondary battery input**

This input monitors the single-cell voltage potential through a high-impedance resistive divider network for the end-of-discharge voltage (EDV) threshold and maximum cell voltage (MCV).

RBI **Register backup input**

This input is used to provide backup potential to the bq2011 registers during periods when $V_{CC} \leq 3V$. A storage capacitor should be connected to RBI.

DQ **Serial I/O pin**

This is an open-drain bidirectional pin.

REF **Voltage reference output for regulator**

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} **Supply voltage input**

V_{SS} **Ground**

Functional Description

General Operation

The bq2011 determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2011 measures discharge and charge currents, estimates self-discharge, monitors the battery for low-battery voltage thresholds, and compensates for temperature and charge/discharge rates. The charge measurement is made by monitoring the voltage across a small-value series sense resistor between the negative battery terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2011 using the LED display with absolute mode as a charge-state indicator. The bq2011 can be configured to display capacity in either a relative or an absolute display mode. The relative display mode uses the last measured discharge capacity of the battery as the battery "full" reference. The absolute display mode uses the programmed full count (PFC) as the full reference, forcing each segment of the display to represent a fixed amount of charge. A push-button display feature is available for momentarily enabling the LED display.

The bq2011 monitors the charge and discharge currents as a voltage across a sense resistor (see R_S in Figure 1). A filter between the negative battery terminal and the SR pin may be required if the rate of change of the battery current is too great.

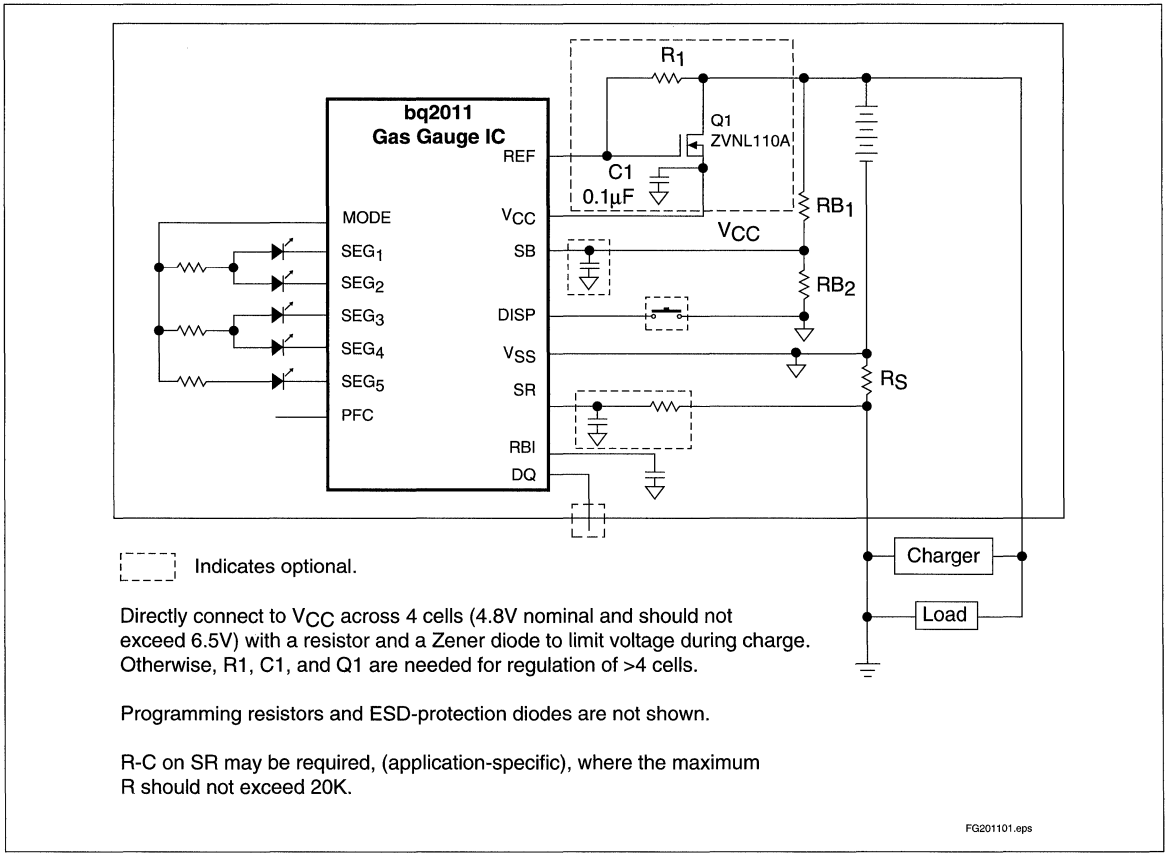


Figure 1. Battery Pack Application Diagram—LED Display, Absolute Mode

Register Backup

The bq2011 RBI input pin is intended to be used with a storage capacitor to provide backup potential to the internal bq2011 registers when V_{CC} momentarily drops below 3.0V. V_{CC} is output on RBI when V_{CC} is above 3.0V.

After V_{CC} rises above 3.0V, the bq2011 checks the internal registers for data loss or corruption. If data has changed, then the NAC and FULCNT registers are cleared, and the LMD register is loaded with the initial PFC.

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2011 monitors the single-cell battery potential through the SB pin. The single-cell voltage potential is determined through a resistor-divider network per the following equation:

$$\frac{RB_1}{RB_2} = N - 1$$

where N is the number of cells, RB_1 is connected to the positive battery terminal, and RB_2 is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV) and for maximum cell voltage (MCV). The EDV threshold level is used to determine when the battery has reached an "empty" state, and the MCV threshold is used for fault detection during charging. The EDV and MCV thresholds for the bq2011 are fixed at:

$$V_{EDV} = 0.90V$$
$$V_{MCV} = 2.00V$$

During discharge and charge, the bq2011 monitors V_{SR} for various thresholds, V_{SR1}–V_{SR4}. These thresholds are used to compensate the charge and discharge rates. Refer to the discharge compensation section for details. EDV monitoring is disabled if $V_{SR} \geq V_{SR1}$ (50mV typical) and resumes 1 second after V_{SR} drops back below V_{SR1}.

Reset

The bq2011 recognizes a valid battery whenever V_{SB} is greater than 0.1V typical. V_{SB} rising from below 0.25V resets the device. Reset can also be accomplished with a command over the serial port as described in the Reset Register section.

Temperature

The bq2011 internally determines the temperature in 10°C steps centered from -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available charge display translation. The temperature range is available over the serial port in 10°C increments as shown below:

TMPGG (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2011 measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (SB and V_{CC}) should be placed as close as possible to the SB and V_{CC} pins, respectively, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor (R_S) should be as close as possible to the bq2011.
- The R-C on the SR pin should be located as close as possible to the SR pin. The maximum R should not exceed 20K.

4/18

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2011. The bq2011 accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge and discharge currents are temperature and rate compensated, whereas self-discharge is only temperature compensated.

The main counter, Nominal Available Charge (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2011 adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the Programmed Full Count (PFC) shown in Table 1. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. **Last Measured Discharge (LMD) or learned battery capacity:**

   LMD is the last measured discharge capacity of the battery. On initialization (application of V_{CC} or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register (DCR) representing a discharge from full to below EDV. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

2. **Programmed Full Count (PFC) or initial battery capacity:**

   The initial LMD and gas gauge rate values are programmed by using PFC. The PFC also provides the 100% reference for the absolute display mode. The bq2011 is configured for a given application by selecting a PFC value from Table 1. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

   Battery capacity (mAh) * sense resistor (Ω) =

   PFC (mVh)

   Selecting a PFC slightly less than the rated capacity for absolute mode provides capacity above the full reference for much of the battery's life.

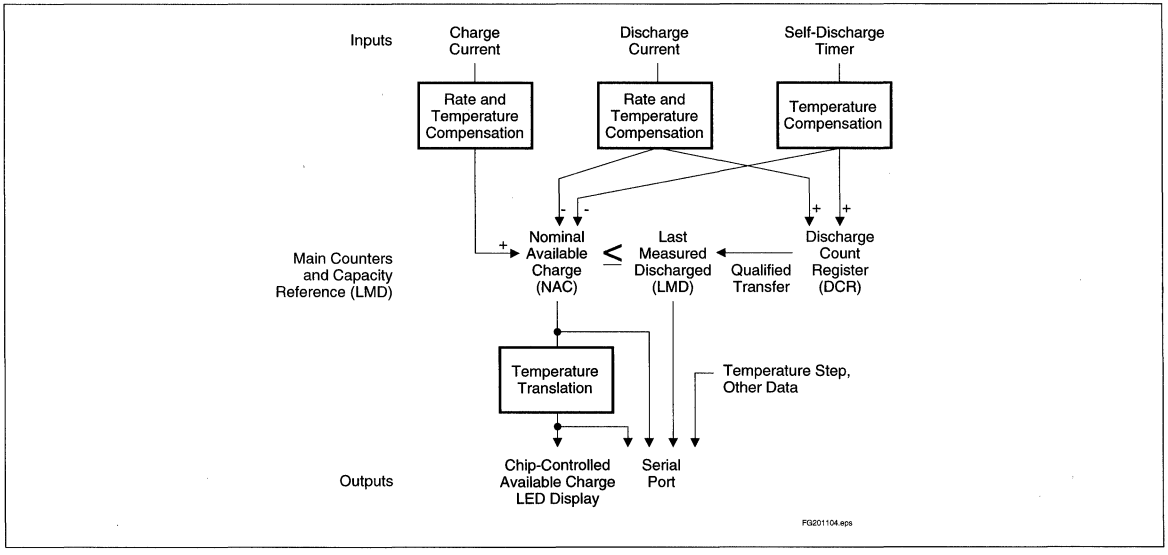


Figure 2. Operational Overview

Example: Selecting a PFC Value

Given:

Sense resistor = 0.005Ω
Number of cells = 6
Capacity = 1300mAh, NiCd cells
Current range = 1A to 80A
Relative display mode
Self-discharge = $^{C}/_{64}$
Voltage drop over sense resistor = 5mV to 400mV

Therefore:

1300mAh * 0.005Ω = 6.5mVh

Select:

PFC = 34304 counts or 6.5mVh
PFC = Z (float)
MODE = not connected

The initial full battery capacity is 6.5mVh (1300mAh) until the bq2011 "learns" a new capacity with a qualified discharge from full to EDV.

4

Table 1. bq2011 Programmed Full Count mVh Selections

PFC	Programmed Full Count (PFC)	mVh	Scale	MODE Pin	Display Mode
H	27648	10.5	$^{1}/_{2640}$	Floating	Relative
Z	34304	6.5	$^{1}/_{5280}$		
L	44800	8.5	$^{1}/_{5280}$		
H	42240	8.0	$^{1}/_{5280}$	Connected to LEDs	Absolute
Z	31744	6.0	$^{1}/_{5280}$		
L	23808	4.5	$^{1}/_{5280}$		

3. **Nominal Available Charge (NAC):**

   NAC counts up during charge to a maximum value of LMD and down during discharge and self discharge to 0. NAC is reset to 0 on initialization and on the first valid charge following discharge to EDV. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = LMD.

   Note: NAC is set to the value in LMD when SEG_5 is pulled low during a reset.

4. **Discharge Count Register (DCR):**

   The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC = LMD. The DCR does not roll over but stops counting when it reaches FFFFh.

   The DCR value becomes the new LMD value on the first charge after a valid discharge to V_{EDV} if:

   - No valid charge initiations (charges greater than 256 NAC counts; or 0.006 – 0.01C) occurred during the period between NAC = LMD and EDV detected.
   - The self-discharge count is not more than 4096 counts (8% to 18% of PFC, specific percentage threshold determined by PFC).
   - The temperature is ≥ 0°C when the EDV level is reached during discharge.

   The valid discharge flag (VDQ) indicates whether the present discharge is valid for LMD update.

Charge Counting

Charge activity is detected based on a negative voltage on the V_{SR} input. If charge activity is detected, the bq2011 increments NAC at a rate proportional to V_{SRO} (V_{SR} + V_{OS}) and, if enabled, activates an LED display if V_{SRO} < -1mV. Charge actions increment the NAC after compensation for charge rate and temperature.

The bq2011 determines a valid charge activity sustained at a continuous rate equivalent to V_{SRO} < -400µV. A valid charge equates to a sustained charge activity greater than 256 NAC counts. Once a valid charge is detected, charge counting continues until V_{SRO} rises above -400µV.

Discharge Counting

All discharge counts where V_{SRO} > 500µV cause the NAC register to decrement and the DCR to increment. Exceeding the fast discharge threshold (FDQ) if the rate is equivalent to V_{SRO} > 2mV activates the display, if enabled. The display becomes inactive after V_{SRO} falls below 2mV.

Self-Discharge Estimation

The bq2011 continuously decrements NAC and increments DCR for self-discharge based on time and temperature. The self-discharge count rate is programmed to be a nominal $\frac{1}{80}$ * NAC rate per day. This is the rate for a battery whose temperature is between 20°–30°C. The NAC register cannot be decremented below 0.

Count Compensations

The bq2011 determines fast charge when the NAC updates at a rate of ≥2 counts/sec. Charge and discharge activity is compensated for temperature and charge/discharge rate before updating the NAC and/or DCR. Self-discharge estimation is compensated for temperature before updating the NAC or DCR.

Charge Compensation

Two charge efficiency factors are used for trickle charge and fast charge. Fast charge is defined as a rate of charge resulting in ≥ 2 NAC counts/sec (≥ 0.15C to 0.32C depending on PFC selections; see Table 2). The compensation defaults to the fast charge factor until the actual charge rate is determined.

Temperature adapts the charge rate compensation factors over three ranges between nominal, warm, and hot temperatures. The compensation factors are shown below.

Charge Temperature	Trickle Charge Compensation	Fast Charge Compensation
<40°C	0.80	0.95
≥ 40°C	0.75	0.90

Discharge Compensation

Corrections for the rate of discharge are made by adjusting an internal discharge compensation factor. The discharge factor is based on the dynamically measured V_{SR}. The compensation factors during discharge are:

Approximate V_{SR} Threshold	Discharge Compensation Factor	Efficiency
$V_{SR} < 50$ mV	1.00	100%
$V_{SR1} > 50$ mV	1.05	95%
$V_{SR2} > 100$ mV	1.15	85%
$V_{SR3} > 150$ mV	1.25	75%
$V_{SR4} > 253$ mV	1.25	75%

Temperature compensation during discharge also takes place. At lower temperatures, the compensation factor increases by 0.05 for each 10°C temperature step below 10°C.

$$\text{Comp. factor} = 1.00 + (0.05 * N)$$

Where N = number of 10°C steps below 10°C and $V_{SR} < 50$mV.

For example:

T > 10°C: Nominal compensation, N = 0

0°C < T < 10°C: N = 1 (i.e., 1.00 becomes 1.05)

-10°C < T < 0°C: N = 2 (i.e., 1.00 becomes 1.10)

-20°C < T < -10°C: N = 3 (i.e., 1.00 becomes 1.15)

-20°C < T < -30°C: N = 4 (i.e., 1.00 becomes 1.20)

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of $1/80$ * NAC per day. This is the rate for a battery within the 20–30°C temperature range (TMPGG = 6x). This rate varies across 8 ranges from <10°C to >70°C, doubling with each higher temperature step (10°C). See Table 2

Table 2. Self-Discharge Compensation

Temperature Range	Self-Discharge Compensation Typical Rate/Day
< 10°C	$NAC/320$
10–20°C	$NAC/160$
20–30°C	$NAC/80$
30–40°C	$NAC/40$
40–50°C	$NAC/20$
50–60°C	$NAC/10$
60–70°C	$NAC/5$
> 70°C	$NAC/2.5$

Error Summary

Capacity Inaccurate

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see the DCR description on page 7). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

A Capacity Inaccurate counter (CPI) is maintained and incremented each time a valid charge occurs and is reset whenever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

Current-Sensing Error

Table 3 illustrates the current-sensing error as a function of V_{SR}. A digital filter eliminates charge and discharge counts to the NAC register when V_{SRO} (V_{SR} + V_{OS}) is between -400µV and 500µV.

Table 3. bq2011 Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

8/18

Communicating with the bq2011

The bq2011 includes a simple single-pin (DQ plus return) serial data interface. A host processor uses the interface to access various bq2011 registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain DQ pin on the bq2011 should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2011. The command directs the bq2011 to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 333 bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2011 may be sampled using the pulse-width capture timers available on some microcontrollers.

Communication is normally initiated by the host processor sending a BREAK command to the bq2011. A BREAK is detected when the DQ pin is driven to a logic-low state for a time, t_B or greater. The DQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2011 is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2011 taking the DQ pin to a logic-low state for a period, $t_{STRH,B}$. The next section is the actual data transmission, where the data should be valid by a period, t_{DSU}, after the negative edge used to start communication. The data should be held for a period, t_{DV}, to allow the host or bq2011 to sample the data bit.

The final section is used to stop the transmission by returning the DQ pin to a logic-high state by at least a period, t_{SSU}, after the negative edge used to start communication. The final logic-high state should be held until a period, t_{SV}, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2011 is always performed with the least-significant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2011 NAC register.

bq2011 Registers

The bq2011 command and status registers are listed in Table 4 and described below.

Command Register (CMDR)

The write-only CMDR register is accessed when eight valid command bits have been received by the bq2011. The CMDR register contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function.

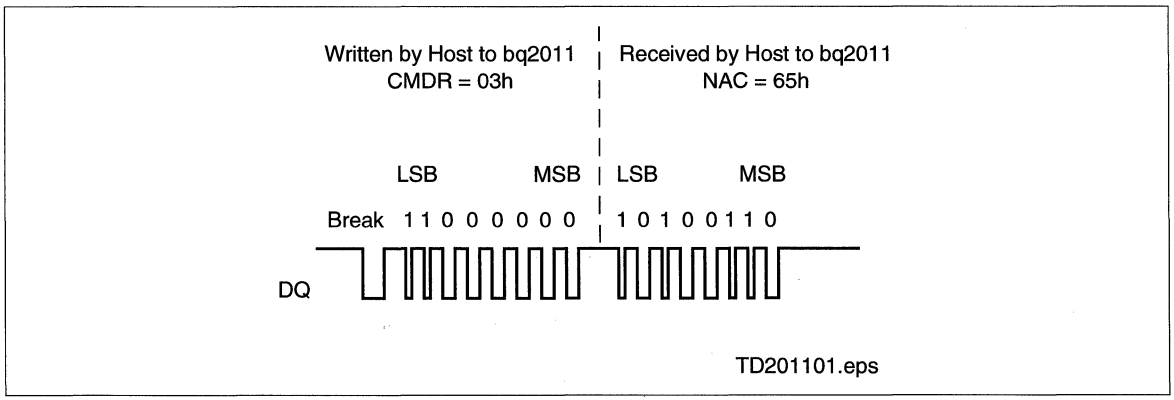


Figure 3. Typical Communication with the bq2011

Table 4. bq2011 Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	Command register	00h	Write	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
FLGS1	Primary status flags register	01h	Read	CHGS	BRP	MCV	CI	VDQ	n/u	EDV	n/u
TMPGG	Temperature and gas gauge register	02h	Read	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available charge high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	Nominal available charge low byte register	17h	Read	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	Read	CR	DR2	DR1	DR0	n/u	n/u	n/u	OVLD
CPI	Capacity inaccurate count register	09h	Read	CPI7	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	CPI0
OCTL	Output control register	0ah	Write	1	OC5	OC4	OC3	OC2	OC1	n/u	OCE
FULCNT	Full count register	0bh	Read	FUL7	FUL6	FUL5	FUL4	FUL3	FUL2	FUL1	FUL0
RST	Reset register	39h	Write	RST	0	0	0	0	0	0	0

Note: n/u = not used

The W/$\overline{R}$ values are:

CMDR Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is:

0 The bq2011 outputs the requested register contents specified by the address portion of CMDR.

1 The following eight bits should be written to the register specified by the address portion of CMDR.

The lower seven-bit field of CMDR contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

CMDR Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Primary Status Flags Register (FLGS1)

The read-only FLGS1 register (address=01h) contains the primary bq2011 flags.

The ***charge status*** flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when V_{SRO} < -400µV. A V_{SRO} of greater than-400µV or discharge activity clears CHGS.

The CHGS values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
CHGS	-	-	-	-	-	-	-

Where CHGS is:

0 Either discharge activity detected or V_{SRO} > -400µV

1 V_{SRO} < -400µV

The ***battery replaced*** flag (BRP) is asserted whenever the potential on the SB pin (relative to V_{SS}), V_{SB}, rises above 0.1V and determines the internal registers have been corrupted. The BRP flag is also set when the bq2011 is reset (see the RST register description). BRP is latched until either the bq2011 is charged until NAC = LMD or discharged until EDV is reached. BRP = 1 signifies that the device has been reset.

The BRP values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	BRP	-	-	-	-	-	-

Where BRP is:

0 bq2011 is charged until NAC = LMD or discharged until the EDV flag is asserted

1 SB rising from below 0.1V, or a serial port initiated reset has occurred

The ***maximum cell voltage*** flag (MCV) is asserted whenever the potential on the SB pin (relative to V_{SS}) is above 2.0V. The MCV flag is asserted until the condition causing MCV is removed.

The MCV values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	MCV	-	-	-	-	-

Where MCV is:

0 V_{SB} < 2.0V

1 V_{SB} > 2.0V

The ***capacity inaccurate*** flag (CI) is used to warn the user that the battery has been charged a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2011 is reset. The flag is cleared after an LMD update.

The CI values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	CI	-	-	-	-

Where CI is:

0 When LMD is updated with a valid full discharge or the bq2011 is reset

1 After the 64th valid charge action with no LMD updates

The ***valid discharge*** flag (VDQ) is asserted when the bq2011 is discharged from NAC=LMD. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- The self-discharge count register (SDCR) has exceeded the maximum acceptable value (4096 counts) for an LMD update.
- A valid charge action equal to 256 NAC counts with $V_{SRO} < -400\mu V$.
- The EDV flag was set at a temperature below 0°C

The VDQ values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

Where VDQ is:

0 SDCR ≥ 4096, subsequent valid charge action detected, or EDV is asserted with the temperature less than 0°C

1 On first discharge after NAC = LMD

The ***end-of-discharge warning*** flag (EDV) warns the user that the battery is empty. SEG1 blinks at a 4Hz rate. EDV detection is disabled if $V_{SR} > V_{SR1}$. The EDV flag is latched until a valid charge has been detected.

The EDV values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV	-

Where EDV is:

0 Valid charge action detected and $V_{SB} \geq 0.90V$

1 $V_{SB} < 0.90V$ providing that $V_{SR} < V_{SR1}$

Temperature and Gas Gauge Register (TMPGG)

The read-only TMPGG register (address=02h) contains two data fields. The first field contains the battery temperature. The second field contains the available charge from the battery.

TMPGG Temperature Bits							
7	6	5	4	3	2	1	0
TMP3	TMP2	TMP1	TMP0	-	-	-	

The bq2011 contains an internal temperature sensor. The temperature is used to set charge and discharge efficiency factors as well as to adjust the self-discharge coefficient. The temperature register contents may be translated as shown below.

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

The bq2011 calculates the available charge as a function of NAC, temperature, and a full reference, either LMD or PFC. The results of the calculation are available via the display port or the gas gauge field of the TMPGG register. The register is used to give available capacity in $1/16$ increments from 0 to $15/16$.

TMPGG Gas Gauge Bits							
7	6	5	4	3	2	1	0
-	-	-	-	GG3	GG2	GG1	GG0

The gas gauge display and the gas gauge portion of the TMPGG register are adjusted for cold temperature dependencies. A piece-wise correction is performed as follows:

Temperature	Available Capacity Calculation
> 0°C	NAC / "Full Reference"
-20°C < T < 0°C	0.75 * NAC / "Full Reference"
< -20°C	0.5 * NAC / "Full Reference"

The adjustment between > 0°C and -20°C < T < 0°C has a 4°C hysteresis.

Nominal Available Charge Register (NAC)

The read/write NACH register (address=03h) and the read-only NACL register (address=17h) are the main gas gauging registers for the bq2011. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC.

On reset, the NACH and NACL registers are cleared to zero. NACL stops counting when NACH reaches zero. When the bq2011 detects a valid charge, NACL resets to zero; *writing to the NAC register affects the available charge counts and, therefore, affects the bq2011 gas gauge operation.*

Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V_{CC} is greater than 2V. The contents of BATID have no effect on the operation of the bq2011. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2011 uses as a measured full reference. The bq2011 adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2011 updates the capacity of the battery. LMD is set to PFC during a bq2011 reset.

Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2011 flags.

The ***charge rate*** flag (CR) is used to denote the fast charge regime. Fast charge is assumed whenever a charge action is initiated. The CR flag remains asserted if the charge rate does not fall below 2 counts/sec.

The CR values are:

FLGS2 Bits							
7	6	5	4	3	2	1	0
CR	-	-	-	-	-	-	-

Where CR is:

0 When charge rate falls below 2 counts/sec

1 When charge rate is above 2 counts/sec

The fast charge regime efficiency factors are used when CR = 1. When CR = 0, the trickle charge efficiency factors are used. The time to change CR varies due to the user-selectable count rates.

The ***discharge rate*** flags, DR2–0, are bits 6–4.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-	-	-	

They are used to determine the present discharge regime as follows:

DR2	DR1	DR0	V_{SR} (V)
0	0	0	V_{SR} < 50mV
0	0	1	50mV < V_{SR} < 100mV (overload, OVLD=1)
0	1	0	100mV < V_{SR} < 150mV
0	1	1	150mV < V_{SR} < 253mV
1	0	0	V_{SRD} > 253mV

The ***overload*** flag (OVLD) is asserted when a discharge overload is detected, V_{SRD} > 50mV. OVLD remains asserted as long as the condition persists and is cleared when V_{SRD} < 50mV.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OVLD

DR2–0 and OVLD are set based on the measurement of the voltage at the SR pin relative to V_{SS}. The rate at which this measurement is made varies with device activity.

Full Count Register (FULCNT)

The read-only FULCNT register (address=0bh) provides the system with a diagnostic of the number of times the battery has been fully charged (NAC = LMD). The number of full occurrences can be determined by multiplying the value in the FULCNT register by 16. Any discharge action other than self-discharge allows detection of another full occurrence during the next valid charge action.

Capacity Inaccurate Count Register (CPI)

The read-only CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2011 adapts to the changing capacity over time. A complete discharge from full (NAC=LMD) to empty (EDV=1) is required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and the self-discharge counter is less than 4096 counts.

The CPI register is incremented every time a valid charge is detected. The register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. CPI is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

Output Control Register (OCTL)

The write-only OCTL register (address=0ah) provides the system with a means to check the display connections for the bq2011. The segment drivers may be overwritten by data from OCTL when the least-significant bit of OCTL, OCE, is set. The data in bits OC_{5-1} of the OCTL register (see Table 4 on page 10 for details) is output onto the segment pins, SEG_{5-1}, respectively if OCE=1. *Whenever OCE is written to 1, the MSB of OCTL should be set to a 1.* The OCE register location must be cleared to return the bq2011 to normal operation. OCE may be cleared by either writing the bit to a logic zero via the serial port or by resetting the bq2011 as explained below. **Note:** Whenever the OCTL register is written, the MSB of OCTL should be written to a logic one.

Reset Register (RST)

The reset register (address=39h) provides the means to perform a software-controlled reset of the device. A full device reset may be accomplished by first writing LMD (address = 05h) to 00h and then writing the RST register contents from 00h to 80h. *Setting any bit other than the most-significant bit of the RST register is* ***not allowed****, and results in improper operation of the bq2011.*

Resetting the bq2011 sets the following:

- LMD = PFC
- CPI, VDQ, NAC, and OCE = 0 or NAC = LMD when SEG5 = L
- CI and BRP = 1

Display

The bq2011 can directly display capacity information using low-power LEDs. If LEDs are used, the segment pins should be tied to V_{CC}, the battery, or the MODE pin for programming the bq2011.

The bq2011 displays the battery charge state in either absolute or relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD.

In absolute mode, each segment represents a fixed amount of charge, based on the initial PFC. In absolute mode, each segment represents 20% of the PFC. As the battery wears out over time, it is possible for the LMD to be below the initial PFC. In this case, all of the LEDs may not turn on, representing the reduction in the actual battery capacity.

The capacity display is also adjusted for the present battery temperature. The temperature adjustment reflects the available capacity at a given temperature but does not affect the NAC register. The temperature adjustments are detailed in the TMPGG register description.

When $\overline{DISP}$ is tied to V_{CC}, the SEG_{1-5} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active during charge if the NAC registers are counting at a rate equivalent to V_{SRO} < -1mV or fast discharge if the NAC registers are counting at a rate equivalent to V_{SRO} > 2mV. When pulled low, the segment output becomes active for 4 seconds, ±0.5 seconds.

The segment outputs are modulated as two banks, with segments 1, 3, and 5 alternating with segments 2 and 4. The segment outputs are modulated at approximately 320Hz, with each bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV} to indicate a low-battery condition or NAC is less than 10% of the LMD or PFC, depending on the display mode.

Microregulator

The bq2011 can operate directly from 4 cells. To facilitate the power supply requirements of the bq2011, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2011 can be inexpensively built using the FET and an external resistor.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
V_{SR}	Relative to V_{SS}	-0.3	+7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2011 application note for details).
T_{OPR}	Operating temperature	0	+70	°C	Commercial
		-40	+85	°C	Industrial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDV}	End-of-discharge warning	0.87	0.90	0.93	V	SB
V_{SR1}	Discharge compensation threshold	20	50	75	mV	SR (see note)
V_{SR2}	Discharge compensation threshold	70	100	125	mV	SR (see note)
V_{SR3}	Discharge compensation threshold	120	150	175	mV	SR (see note)
V_{SR4}	Discharge compensation threshold	220	253	275	mV	SR (see note)
V_{SRQ}	Valid charge	-	-	-400	µV	$V_{SR} + V_{OS}$
V_{SRD}	Valid discharge	500	-	-	µV	$V_{SR} + V_{OS}$
V_{MCV}	Maximum single-cell voltage	1.95	2.0	2.05	V	SB
V_{BR}	Battery removed/replaced	-	0.1	0.25	V	SB

Note: For proper operation of the threshold detection circuit, V_{CC} must be at least 1.5V greater than the voltage being measured.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{OS}	Offset referred to V_{SR}	-	±50	±150	µV	$\overline{DISP} = V_{CC}$
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	$I_{REF} = 5\mu A$
	Reference at -40°C to +85°C	4.5	-	7.5	V	$I_{REF} = 5\mu A$
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	$V_{REF} = 3V$
I_{CC}	Normal operation	-	90	135	µA	$V_{CC} = 3.0V$, DQ = 0
		-	120	180	µA	$V_{CC} = 4.25V$, DQ = 0
		-	170	250	µA	$V_{CC} = 6.5V$, DQ = 0
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	$0 < V_{SB} < V_{CC}$
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	$V_{DISP} = V_{SS}$
I_{MODE}	MODE input leakage	-0.2	-	0.2	µA	$\overline{DISP} = V_{CC}$
I_{RBI}	RBI data-retention current	-	-	100	nA	$V_{RBI} > V_{CC} < 3V$
R_{DQ}	Internal pulldown	500	-	-	KΩ	
V_{SR}	Sense resistor input	-0.3	-	2.0	V	$V_{SR} > V_{SS}$ = discharge; $V_{SR} < V_{SS}$ = charge
R_{SR}	SR input impedance	10	-	-	MΩ	$-200mV < V_{SR} < V_{CC}$
V_{IHPFC}	PFC logic input high	V_{CC} - 0.2	-	-	V	PFC
V_{ILPFC}	PFC logic input low	-	-	V_{SS} + 0.2	V	PFC
V_{IZPFC}	PFC logic input Z	float	-	float	V	PFC
I_{IHPFC}	PFC input high current	-	1.2	-	µA	$V_{PFC} = V_{CC}/2$
I_{ILPFC}	PFC input low current	-	1.2	-	µA	$V_{PFC} = V_{CC}/2$
V_{OLSL}	SEG_X output low, low V_{CC}	-	0.1	-	V	$V_{CC} = 3V$, $I_{OLS} \leq 1.75mA$ SEG_1–SEG_5
V_{OLSH}	SEG_X output low, high V_{CC}	-	0.4	-	V	$V_{CC} = 6.5V$, $I_{OLS} \leq 11.0mA$ SEG_1–SEG_5
V_{OHML}	MODE output high, low V_{CC}	V_{CC} - 0.3	-	-	V	$V_{CC} = 3V$, $I_{OHMODE} = -5.25mA$
V_{OHMH}	MODE output high, high V_{CC}	V_{CC} - 0.6	-	-	V	$V_{CC} = 6.5V$, $I_{OHMODE} = -33.0mA$
I_{OHMODE}	MODE source current	-33	-	-	mA	At $V_{OHMODE} = V_{CC}$ - 0.6V
I_{OLS}	SEG_X sink current	11.0	-	-	mA	At $V_{OLSH} = 0.4V$, $V_{CC} = 6.5V$
I_{OL}	Open-drain sink current	5.0	-	-	mA	At $V_{OL} = V_{SS} + 0.3V$, DQ
V_{OL}	Open-drain output low	-	-	0.5	V	$I_{OL} \leq 5mA$, DQ
V_{IHDQ}	DQ input high	2.5	-	-	V	DQ
V_{ILDQ}	DQ input low	-	-	0.8	V	DQ
R_{FLOAT}	Float state external impedance	-	5	-	MΩ	PFC

Note: All voltages relative to V_{SS}.

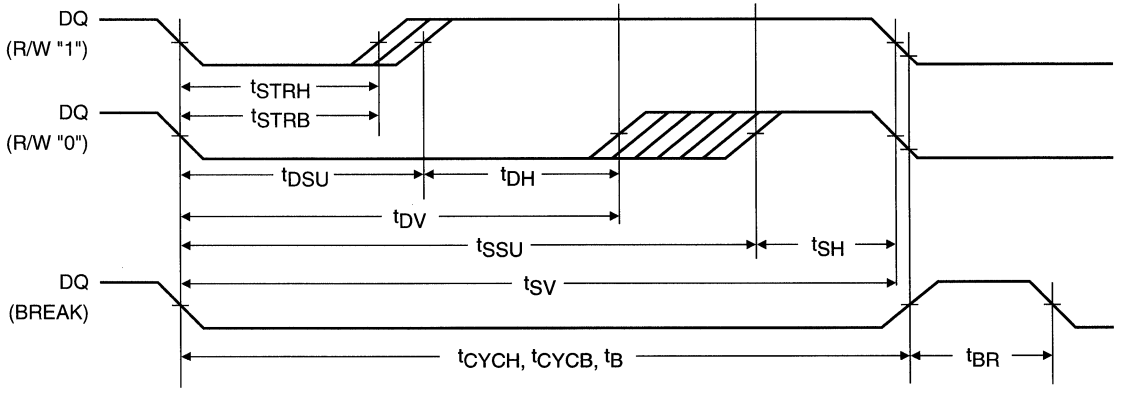
16/18

Serial Communication Timing Specification ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2011	3	-	-	ms	See note
t_{CYCB}	Cycle time, bq2011 to host	3	-	6	ms	
t_{STRH}	Start hold, host to bq2011	5	-	-	ns	
t_{STRB}	Start hold, bq2011 to host	500	-	-	µs	
t_{DSU}	Data setup	-	-	750	µs	
t_{DH}	Data hold	750	-	-	µs	
t_{DV}	Data valid	1.50	-	-	ms	
t_{SSU}	Stop setup	-	-	2.25	ms	
t_{SH}	Stop hold	700	-	-	µs	
t_{SV}	Stop valid	2.95	-	-	ms	
t_B	Break	3	-	-	ms	
t_{BR}	Break recovery	1	-	-	ms	

Note: The open-drain DQ pin should be pulled to at least V_{CC} by the host system for proper DQ operation. DQ may be left floating if the serial interface is not used.

Serial Communication Timing Illustration

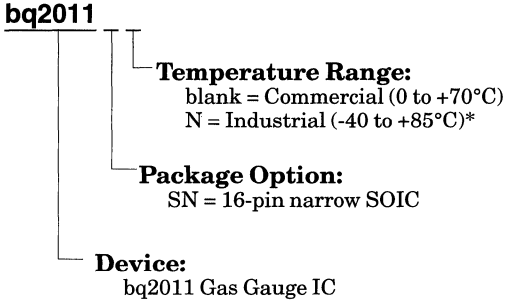


Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
3	7	Self-discharge count rate	Was: $\frac{1}{64}$ * NAC rate per day Is: $\frac{1}{80}$ * NAC rate per day
3	7	Compensation factor 30–40°C	Was: 0.90 Is: 0.95
3	7	Compensation factor >40°C	Was: 0.80 Is: 0.90
4	7	Charge compensation	Changed compensation factor variation with temperature
4	8	Self-discharge compensation	Changed self-discharge compensation rate variation with temperature

Notes: Changes 1 and 2 = See the *1995 Data Book*.
Change 3 = Jan. 1996 D changes from July 1994 C.
Change 4 = Feb. 1996 E changes from Jan. 1996 D.

Ordering Information

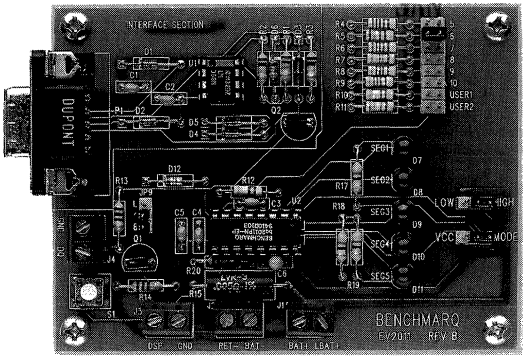


* Contact factory for availability.

bq2011 Evaluation System

Features

- bq2011 Gas Gauge IC evaluation and development system
- PC interface hardware for easy access to state-of-charge information via the serial port
- Alternative terminal block for direct connection to the serial port
- Battery state-of-charge monitoring for 5- to 10-cell (series) applications (2 user-selectable options for 3, 4, or greater than 10 cells)
- On-board regulator for greater than 4-cell applications
- State-of-charge information displayed on bank of 5 LEDs
- Nominal capacity jumper-configurable
- Display mode jumper-configurable



General Description

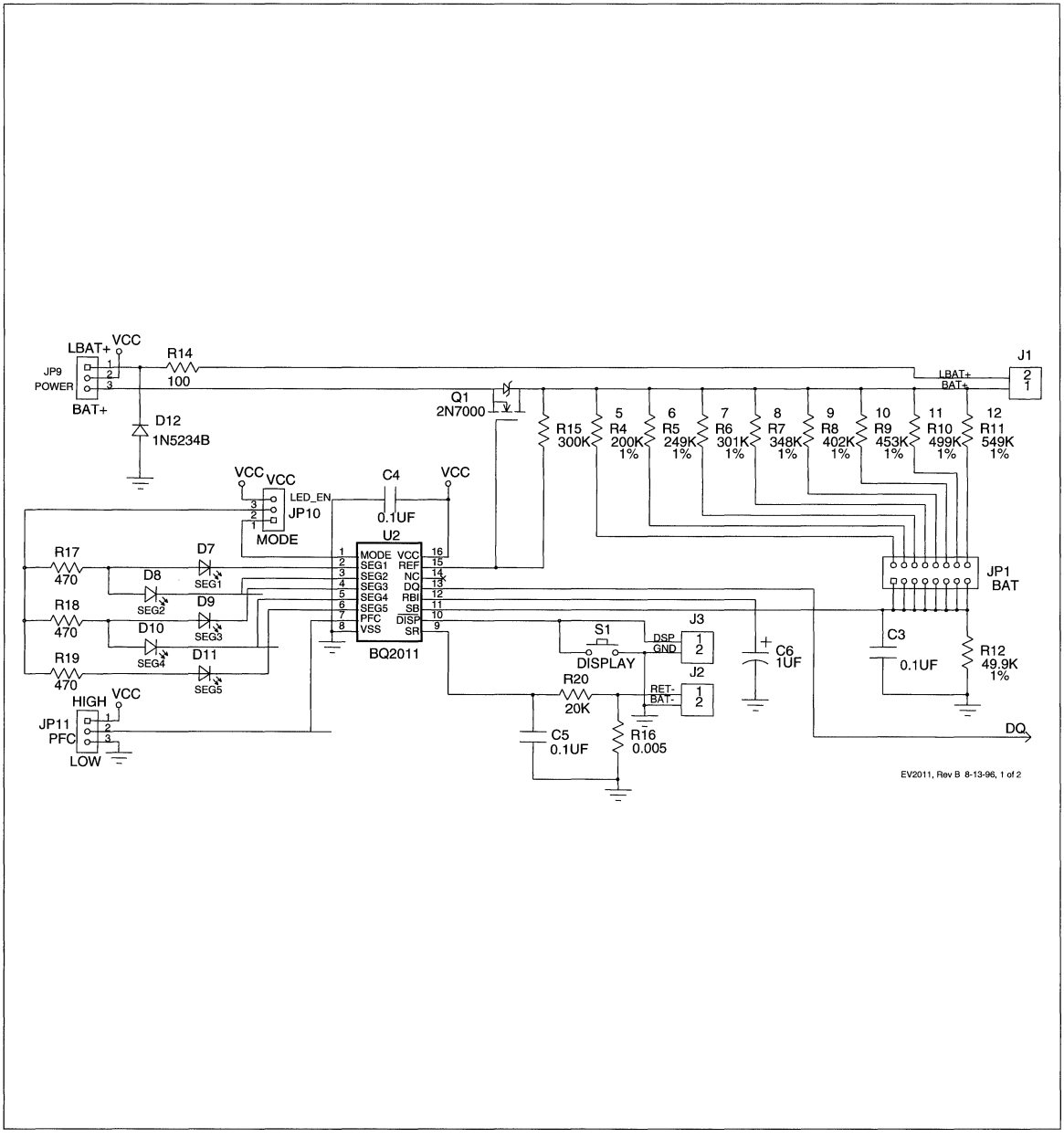
The EV2011 Evaluation System provides a development and evaluation environment for the bq2011 Gas Gauge IC. The EV2011 incorporates a bq2011, a sense resistor, and all other hardware necessary to provide a capacity monitoring function for 3 to 12 series NiCd cells.

Hardware for a PC interface is included on the EV2011 so that easy access to the state-of-charge information can be achieved via the serial port of the bq2011. Direct connection to the serial port of the bq2011 is also made available for check-out of the final hardware/ software implementation.

The menu-driven software provided with the EV2011 displays charge/discharge activity and allows user interface to the bq2011 from any standard DOS PC.

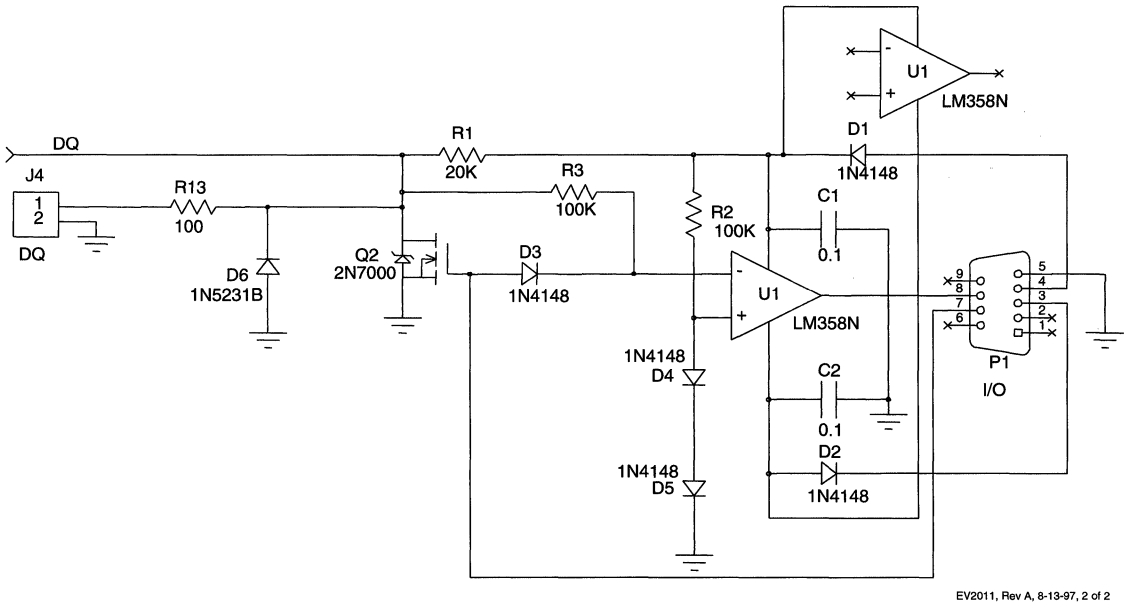
A full data sheet for this product is available on the Unitrode web site, or you may contact the factory for one.

EV2011 Board Schematic



Rev. B Board

EV2011 Board Schematic (Continued)



Rev. B Board

Gas Gauge IC for High Discharge Rates

Features

- Conservative and repeatable measurement of available charge in rechargeable batteries
- Designed for portable equipment such as power tools with high discharge rates
- Designed for battery pack integration
  - 120µA typical standby current (self-discharge estimation mode)
  - Small size enables implementations in as little as ½ square inch of PCB
- Direct drive of LEDs for capacity display
- Self-discharge compensation using internal temperature sensor
- Simple single-wire serial communications port for subassembly testing
- 16-pin narrow SOIC

General Description

The bq2011J Gas Gauge IC is intended for battery-pack installation to maintain an accurate record of available battery charge. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery. The bq2011J is designed for systems such as power tools with very high discharge rates.

Battery self-discharge is estimated based on an internal timer and temperature sensor. Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and selfdischarge calculations to provide available charge information across a wide range of operating conditions. Initial battery capacity is set using the $PROG_{1-4}$ and SPFC pins. Actual battery capacity is automatically "learned" in the course of a discharge cycle from full to empty and may be displayed depending on the display mode.

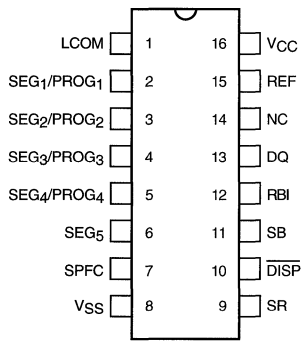
Nominal available charge may be directly indicated using a five-segment LED display. These segments are used to graphically indicate nominal available charge.

The bq2011J supports a simple single-line bidirectional serial link to an external processor (common ground). The bq2011J outputs battery information in response to external commands over the serial link. To support subassembly testing, the outputs may also be controlled by command. The external processor may also overwrite some of the bq2011J gas gauge data registers.

The bq2011J may operate directly from four cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide V_{CC} from a greater number of cells.

Internal registers include available charge, temperature, capacity, battery ID, and battery status.

Pin Connections



16-Pin Narrow SOIC

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Pin Names

LCOM	LED common output
SEG_1/ $PROG_1$	LED segment 1/ Program 1 input
SEG_2/ $PROG_2$	LED segment 2 / Program 2 input
SEG_3/ $PROG_3$	LED segment 3/ Program 3 input
SEG_4/ $PROG_4$	LED segment 4/ Program 4 input
SEG_5	LED segment 5
SPFC	Programmed full count selection input
REF	Voltage reference output
NC	No connect
DQ	Serial communications input/output
RBI	Register backup input
SB	Battery sense input
$\overline{DISP}$	Display control input
SR	Sense resistor input
V_{CC}	3.0–6.5V
V_{SS}	Negative battery terminal

Pin Descriptions

LCOM **LED common**

Open-drain output switches V_{CC} to source current for the LEDs. The switch is off during initialization to allow reading of $PROG_{1-4}$ pull-up or pull-down program resistors. LCOM is high impedance when the display is off.

SEG_1–SEG_5 **LED display segment outputs**

Each output may activate an LED to sink the current sourced from MODE, the battery, or V_{CC}.

$PROG_1$–$PROG_4$ **Programmed full count selection inputs (dual function with SEG_1 - SEG_4)**

These three-level input pins define the programmed full count (PFC) in conjunction with SPFC pin, define the display mode and enable or disable self-discharge.

SPFC **Programmed full count selection input**

This three-level input pin along with $PROG_{1-3}$ define the programmed full count (PFC) thresholds and scale selections described in Table 1 and Table 2. The state of the SPFC pin is only read immediately after a reset condition.

SR **Sense resistor input**

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied to the low side of the sense resistor and battery pack ground (see Figure 1). $V_{SR} > V_{SS}$ indicates discharge, and $V_{SR} < V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2011J is $V_{SR} + V_{OS}$ (see Table 4).

NC **No connect**

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ floating allows the LED display to be active during charge and discharge if V_{SRO} < -1mV (charge) or V_{SRO} > 2mV (discharge). Transitioning $\overline{DISP}$ low activates the display for 4 ± 0.5 seconds.

SB **Secondary battery input**

This input monitors the single-cell voltage potential through a high-impedance resistive divider network for the end-of-discharge voltage (EDV) threshold and maximum cell voltage (MCV).

RBI **Register backup input**

This input is used to provide backup potential to the bq2011J registers during periods when $V_{CC} \leq 3V$. A storage capacitor should be connected to RBI.

DQ **Serial I/O pin**

This is an open-drain bidirectional pin.

REF **Voltage reference output for regulator**

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} **Supply voltage input**

V_{SS} **Ground**

Functional Description

General Operation

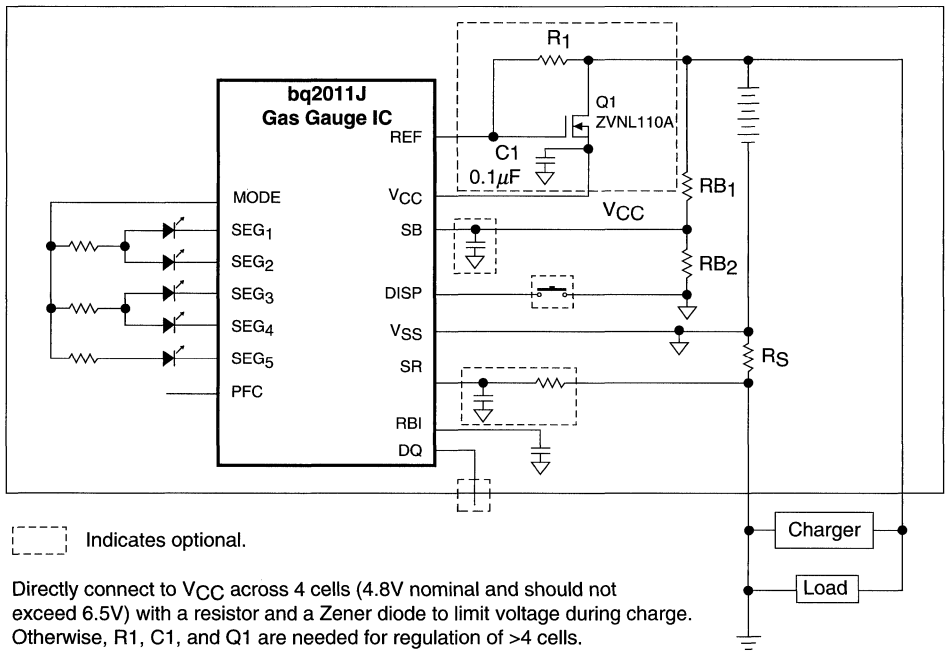
The bq2011J determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2011J measures discharge and charge currents, estimates self-discharge, monitors the battery for low-battery voltage thresholds, and compensates for temperature and charge/discharge rates. The charge measurement is made by monitoring the voltage across a small-value series sense resistor between the negative battery terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2011J using the LED display with absolute mode as a charge-state indicator. The absolute display mode uses the programmed full count (PFC) as the full reference, forcing each segment of the display to represent a fixed amount of charge. A push-button display feature is available for momentarily enabling the LED display.

The bq2011J monitors the charge and discharge currents as a voltage across a sense resistor (see R_S in Figure 1). A filter between the negative battery terminal and the SR pin may be required if the rate of change of the battery current is too great.

Register Backup

The bq2011J RBI input pin is intended to be used with a storage capacitor to provide backup potential to the inter-



Indicates optional.

Directly connect to V_{CC} across 4 cells (4.8V nominal and should not exceed 6.5V) with a resistor and a Zener diode to limit voltage during charge. Otherwise, R1, C1, and Q1 are needed for regulation of >4 cells.

Programming resistors and ESD-protection diodes are not shown.

R-C on SR may be required, (application-specific), where the maximum R should not exceed 20K.

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Figure 1. Battery Pack Application Diagram—LED Display, Absolute Mode

3/18

nal bq2011J registers when V_{CC} momentarily drops below 3.0V. V_{CC} is output on RBI when V_{CC} is above 3.0V.

After V_{CC} rises above 3.0V, the bq2011J checks the internal registers for data loss or corruption. If data has changed, then the NAC and FULCNT registers are cleared, and the LMD register is loaded with the initial PFC.

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2011J monitors the single-cell battery potential through the SB pin. The single-cell voltage potential is determined through a resistor-divider network per the following equation:

$$\frac{RB_1}{RB_2} = N - 1$$

where N is the number of cells, RB_1 is connected to the positive battery terminal, and RB_2 is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV) and for maximum cell voltage (MCV). The EDV threshold level is used to determine when the battery has reached an "empty" state, and the MCV threshold is used for fault detection during charging. The EDV and MCV thresholds for the bq2011J are fixed at:

$$V_{EDV} = 0.90V$$
$$V_{MCV} = 2.00V$$

EDV detection is disabled if the discharge is at a rate equivalent to or greater than 6C (OVLD flag = 1) EDV detection is re-enabled approximately one second after the discharge falls below a rate equivalent to less than 6C (OVLD flag = 0).

Reset

The bq2011J recognizes a valid battery whenever V_{SB} is greater than 0.1V typical. V_{SB} rising from below 0.25V resets the device. Reset can also be accomplished with a command over the serial port as described in the Reset Register section.

Temperature

The bq2011J internally determines the temperature in 10°C steps centered from -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available charge display translation. The temperature range is available over the serial port in 10°C increments as shown in the following chart:

TMPGG (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2011J measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (SB and V_{CC}) should be placed as close as possible to the SB and V_{CC} pins, respectively, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor (R_S) should be as close as possible to the bq2011J.
- The R-C on the SR pin should be located as close as possible to the SR pin. The maximum R should not exceed 20K.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2011J. The bq2011J accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge and discharge currents are temperature and rate compensated, whereas self-discharge is only temperature compensated.

The main counter, Nominal Available Charge (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without

any partial battery charges. Therefore, the bq2011J adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the Programmed Full Count (PFC) shown in Table 1. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. Last Measured Discharge (LMD) or learned battery capacity:

LMD is the last measured discharge capacity of the battery. On initialization (application of V_{CC} or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register (DCR) representing a discharge from full to below EDV. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

2. Programmed Full Count (PFC) or initial battery capacity:

The initial LMD and gas gauge rate values are programmed by using PFC. The PFC also provides the 100% reference for the absolute display mode. The bq2011J is configured for a given application by selecting a PFC value from Table 1. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

Battery capacity (mAh) * sense resistor (Ω) = PFC (mVh)

Selecting a PFC slightly less than the rated capacity for absolute mode provides capacity above the full reference for much of the battery's life.

Example: Selecting a PFC Value

Given:

Sense resistor = 0.002Ω
Number of cells = 6
Capacity = 1800mAh, NiCd cells
Current range = 1A to 80A
Absolute display mode
Self-discharge = $\frac{\%}{80}$
Voltage drop across sense resistor = 2mV to 160mV

Therefore:

1800mAh * 0.002Ω = 3.6mVh

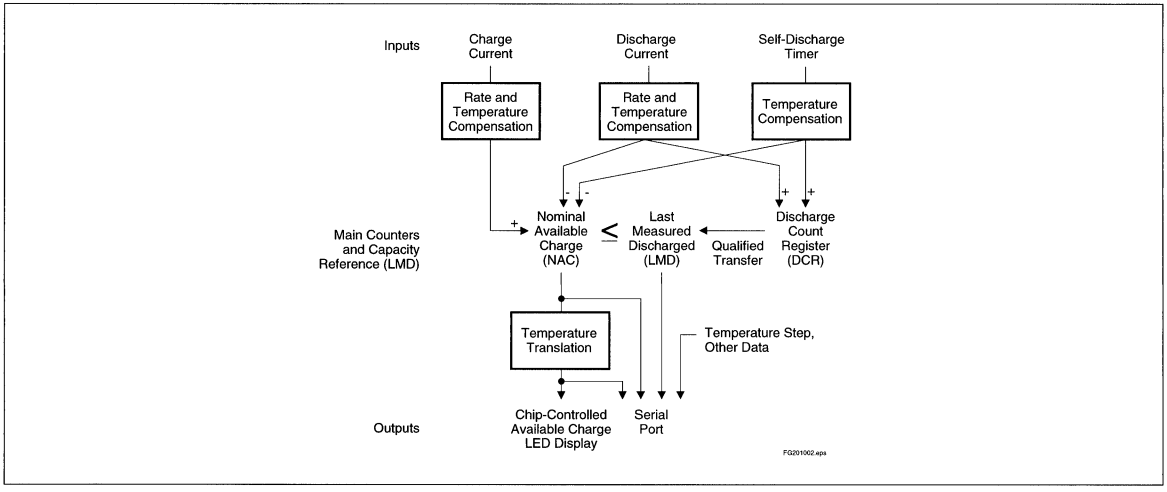


Figure 2. Operational Overview

5/18

Select:

PFC = 35840 counts or 3.39mVh
SPFC = Z (float)
PROG1, PROG2 = H or Z
PROG3 = L
PROG4 = H or Z

The initial full battery capacity is 3.39mVh (1695mAh) until the bq2011J "learns" a new capacity with a qualified discharge from full to EDV.

3. Nominal Available Charge (NAC):

NAC counts up during charge to a maximum value of LMD and down during discharge and self discharge to 0. NAC is reset to 0 on initialization and on the first valid charge following discharge to EDV. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = LMD.

Note: NAC is set to the value in LMD when $PROG_4$ is pulled low during a reset.

Table 1. bq2011J Programmed Full Count mVh Selections

Programmed Full Count (PFC)	mVh	Scale	Display Mode	SPFC	$PROG_1$	$PROG_2$	$PROG_3$
40192	3.81	1/10560	Absolute	H	H or Z	H or Z	H or Z
32256	3.05	1/10560		Z	H or Z	H or Z	H or Z
28928	2.74	1/10560		L	H or Z	H or Z	H or Z
25856	2.45	1/10560		H	L	H or Z	H or Z
35840	3.39	1/10560		Z	L	H or Z	H or Z
23296	2.21	1/10560		L	L	H or Z	H or Z

Table 2. Programmed Self-Discharge

$PROG_4$	NAC Reset Value	Self-Discharge
H or Z	NAC = 0	Enabled
L	NAC = PFC	Disabled

4. Discharge Count Register (DCR):

The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC = LMD. The DCR does not roll over but stops counting when it reaches FFFFh.

The DCR value becomes the new LMD value on the first charge after a valid discharge to V_{EDV} if:

No valid charge initiations (charges greater than 256 NAC counts; or 0.006–0.01C) occurred during the period between NAC = LMD and EDV detected.

The self-discharge count is not more than 4096 counts (8% to 18% of PFC, specific percentage threshold determined by PFC).

The temperature is ≥ 0°C when the EDV level is reached during discharge.

The valid discharge flag (VDQ) indicates whether the present discharge is valid for LMD update.

Charge Counting

Charge activity is detected based on a negative voltage on the V_{SR} input. If charge activity is detected, the bq2011J increments NAC at a rate proportional to V_{SRO} (V_{SR} + V_{OS}) and, if enabled, activates an LED display if V_{SRO} < -1mV. Charge actions increment the NAC after compensation for charge rate and temperature.

The bq2011J determines a valid charge activity sustained at a continuous rate equivalent to V_{SRO} < -400µV. A valid charge equates to a sustained charge activity greater than 256 NAC counts. Once a valid charge is detected, charge counting continues until V_{SRO} rises above -400µV.

Discharge Counting

All discharge counts where V_{SRO} > 500µV cause the NAC register to decrement and the DCR to increment. Exceeding the fast discharge threshold (FDQ) if the rate is equivalent to V_{SRO} > 2mV activates the display, if enabled. The display becomes inactive after V_{SRO} falls below 2mV.

Self-Discharge Estimation

The bq2011J continuously decrements NAC and increments DCR for self-discharge based on time and temperature. The self-discharge count rate is programmed to be a nominal $\frac{1}{80}$ * NAC rate per day or disabled per Table 2. This is the rate for a battery whose temperature is between 20°C–30°C. The NAC register cannot not be decremented below 0.

Count Compensations

The bq2011J determines fast charge when the NAC updates at a rate of ≥2 counts/sec. Charge and discharge activity is compensated for temperature and charge/discharge rate before updating the NAC and/or DCR. Self-discharge estimation is compensated for temperature before updating the NAC or DCR.

Charge Compensation

Two charge efficiency factors are used for trickle charge and fast charge. Fast charge is defined as a rate of charge resulting in ≥ 2 NAC counts/sec (≥ 0.15C to 0.32C depending on PFC selections; see Table 1). The compensation defaults to the fast charge factor until the actual charge rate is determined.

Temperature adapts the charge rate compensation factors over three ranges between nominal, warm, and hot temperatures. The compensation factors are shown below.

Charge Temperature	Trickle Charge Compensation	Fast Charge Compensation
<30°C	0.80	0.95
30–40°C	0.75	0.90
> 40°C	0.65	0.80

Discharge Compensation

Corrections for the rate of discharge are made by adjusting an internal compensation factor. This factor is based upon the number of NAC counts per second. The actual "C" rate may be calculated by using the following formula:

$$C_{RATE} = \frac{K}{N * LMD}$$

where:

K = 66,000

N = Number of samples

LMD = Contents of address 05h

7/18

The compensation factors during discharge are:

Samples	Discharge Compensation Factor	Effective C_{RATE} LMD = 9Dh
N > 70	1.00	C_{RATE} < 6.0C
70 ≥ N > 35	1.05	6.0C ≤ C_{RATE} < 12.0C
35 ≥ N > 23	1.15	12.0C ≤ C_{RATE} < 18.0C
N ≤ 23	1.25	C_{RATE} ≥ 18.0C

Temperature compensation during discharge also takes place. At lower temperatures, the compensation factor increases by 0.05 for each 10°C temperature step below 10°C.

$$\text{Comp. factor} = 1.00 + (0.05 * N)$$

Where N = number of 10°C steps below 10°C and C_{RATE} < 6.0C.

For example:

T > 10°C: Nominal compensation, N = 0

0°C < T < 10°C: N = 1 (i.e., 1.00 becomes 1.05)

-10°C < T < 0°C: N = 2 (i.e., 1.00 becomes 1.10)

-20°C < T < -10°C: N = 3 (i.e., 1.00 becomes 1.15)

-20°C < T < -30°C: N = 4 (i.e., 1.00 becomes 1.20)

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of $\frac{1}{80}$ * NAC per day or disabled. This is the rate for a battery within the 20–30°C temperature range (TMPGG = 6x). This rate varies across 8 ranges from <10°C to >70°C, doubling with each higher temperature step (10°C). See Table 3.

Table 3. Self-Discharge Compensation

Temperature Range	Self-Discharge Compensation Typical Rate/Day
< 10°C	$NAC/_{320}$
10–20°C	$NAC/_{160}$
20–30°C	$NAC/_{80}$
30–40°C	$NAC/_{40}$
40–50°C	$NAC/_{20}$
50–60°C	$NAC/_{10}$
60–70°C	$NAC/_{5}$
> 70°C	$NAC/_{2.5}$

Error Summary

Capacity Inaccurate

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see "4. Discharge Count Register" on the previous page). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

A Capacity Inaccurate counter (CPI) is maintained and incremented each time a valid charge occurs and is reset whenever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

Current-Sensing Error

Table 3 illustrates the current-sensing error as a function of V_{SR}. A digital filter eliminates charge and discharge counts to the NAC register when V_{SRO} (V_{SR} + V_{OS}) is between -400µV and 500µV.

Table 4. bq2011J Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

Communicating With the bq2011J

The bq2011J includes a simple single-pin (DQ plus return) serial data interface. A host processor uses the interface to access various bq2011J registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain DQ pin on the bq2011J should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2011J. The command directs the bq2011J to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 333 bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2011J may be sampled using the pulse-width capture timers available on some microcontrollers.

Communication is normally initiated by the host processor sending a BREAK command to the bq2011J. A BREAK is detected when the DQ pin is driven to a logic-low state for a time, t_B or greater. The DQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2011J is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2011J taking the DQ pin to a logic-low state for a period, $t_{STRH,B}$. The next section is the actual data transmission, where the data should be valid by a period, t_{DSU}, after the negative edge used to start communication. The data should be held for a period, t_{DV}, to allow the host or bq2011J to sample the data bit.

The final section is used to stop the transmission by returning the DQ pin to a logic-high state by at least a period, t_{SSU}, after the negative edge used to start communication. The final logic-high state should be held until a period, t_{SV}, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2011J is always performed with the least-significant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2011J NAC register.

bq2011J Registers

The bq2011J command and status registers are listed in Table 5 and described below.

Command Register (CMDR)

The write-only CMDR register is accessed when eight valid command bits have been received by the bq2011J. The CMDR register contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function.

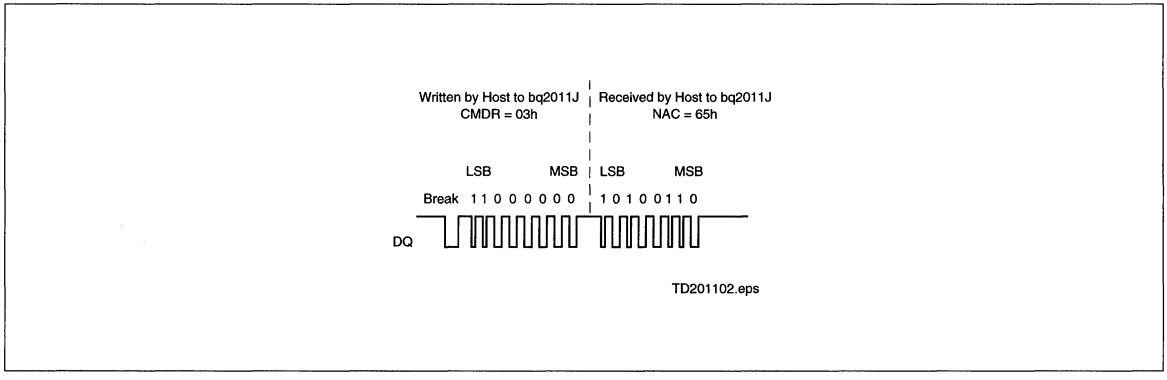


Figure 3. Typical Communication With the bq2011J

Table 5. bq2011J Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	Command register	00h	Write	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
FLGS1	Primary status flags register	01h	Read	CHGS	BRP	MCV	CI	VDQ	n/u	EDV	n/u
TMPGG	Temperature and gas gauge register	02h	Read	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available charge high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	Nominal available charge low byte register	17h	Read	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	Read	CR	DR2	DR1	DR0	n/u	n/u	n/u	OVLD
CPI	Capacity inaccurate count register	09h	Read	CPI7	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	CPI0
OCTL	Output control register	0ah	Write	1	OC5	OC4	OC3	OC2	OC1	n/u	OCE
FULCNT	Full count register	0bh	Read	FUL7	FUL6	FUL5	FUL4	FUL3	FUL2	FUL1	FUL0
RST	Reset register	39h	Write	RST	0	0	0	0	0	0	0

Note: n/u = not used

The W/$\overline{R}$ values are:

CMDR Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is:

0 The bq2011J outputs the requested register contents specified by the address portion of CMDR.

1 The following eight bits should be written to the register specified by the address portion of CMDR.

The lower seven-bit field of CMDR contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

CMDR Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Primary Status Flags Register (FLGS1)

The read-only FLGS1 register (address=01h) contains the primary bq2011J flags.

The ***charge status*** flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when V_{SRO} < -400µV. A V_{SRO} of greater than-400µV or discharge activity clears CHGS.

The CHGS values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
CHGS	-	-	-	-	-	-	-

Where CHGS is:

0 Either discharge activity detected or V_{SRO} > -400µV

1 V_{SRO} < -400µV

The ***battery replaced*** flag (BRP) is asserted whenever the potential on the SB pin (relative to V_{SS}), V_{SB}, rises above 0.1V and determines the internal registers have been corrupted. The BRP flag is also set when the bq2011J is reset (see the RST register description). BRP is cleared if either the bq2011J is charged until NAC = LMD or discharged until EDV is reached. BRP = 1 signifies that the device has been reset.

The BRP values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	BRP	-	-	-	-	-	-

Where BRP is:

0 bq2011J is charged until NAC = LMD or discharged until the EDV flag is asserted

1 SB rising from below 0.1V, or a serial port initiated reset has occurred

The ***maximum cell voltage*** flag (MCV) is asserted whenever the potential on the SB pin (relative to V_{SS}) is above 2.0V. The MCV flag is asserted until the condition causing MCV is removed.

The MCV values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	MCV	-	-	-	-	-

Where MCV is:

0 V_{SB} < 2.0V

1 V_{SB} > 2.0V

The ***capacity inaccurate*** flag (CI) is used to warn the user that the battery has been charged a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2011J is reset. The flag is cleared after an LMD update.

The CI values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	CI	-	-	-	-

Where CI is:

0 When LMD is updated with a valid full discharge

1 After the 64th valid charge action with no LMD updates or the bq2011J is reset

The ***valid discharge*** flag (VDQ) is asserted when the bq2011J is discharged from NAC=LMD. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- The self-discharge count register (SDCR) has exceeded the maximum acceptable value (4096 counts) for an LMD update.
- A valid charge action equal to 256 NAC counts with V_{SRO} < -400µV.
- The EDV flag was set at a temperature below 0°C

The VDQ values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

Where VDQ is:

0 SDCR ≥ 4096, subsequent valid charge action detected, or EDV is asserted with the temperature less than 0°C

1 On first discharge after NAC = LMD

The ***end-of-discharge warning*** flag (EDV) warns the user that the battery is empty. SEG1 blinks at a 4Hz rate. EDV detection is disabled if OVLD = 1. The EDV flag is latched until a valid charge has been detected.

The EDV values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV	-

Where EDV is:

0 Valid charge action detected and V_{SB} ≥ 0.90V

1 V_{SB} < 0.90V providing that OVLD = 0

Temperature and Gas Gauge Register (TMPGG)

The read-only TMPGG register (address=02h) contains two data fields. The first field contains the battery temperature. The second field contains the available charge from the battery.

TMPGG Temperature Bits							
7	6	5	4	3	2	1	0
TMP3	TMP2	TMP1	TMP0	-	-	-	

The bq2011J contains an internal temperature sensor. The temperature is used to set charge and discharge efficiency factors as well as to adjust the self-discharge coefficient. The temperature register contents may be translated as shown below.

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

The bq2011J calculates the available charge as a function of NAC, temperature, and a full reference, either LMD or PFC. The results of the calculation are available via the display port or the gas gauge field of the TMPGG register. The register is used to give available capacity in $\frac{1}{16}$ increments from 0 to $\frac{15}{16}$.

TMPGG Gas Gauge Bits							
7	6	5	4	3	2	1	0
-	-	-	-	GG3	GG2	GG1	GG0

The gas gauge display and the gas gauge portion of the TMPGG register are adjusted for cold temperature dependencies. A piece-wise correction is performed as follows:

Temperature	Available Capacity Calculation
> 0°C	NAC / "Full Reference"
-20°C < T < 0°C	0.75 * NAC / "Full Reference"
< -20°C	0.5 * NAC / "Full Reference"

The adjustment between > 0°C and -20°C < T < 0°C has a 4°C hysteresis.

Nominal Available Charge Register (NAC)

The read/write NACH register (address=03h) and the read-only NACL register (address=17h) are the main gas gauging registers for the bq2011J. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC.

If SEG_4 = 0 on reset, then NACH = PFC and NACL = 0. If SEG_4 = Z or H, the NACH and NACL registers are cleared to zero. NACL stops counting when NACH reaches zero. When the bq2011J detects a valid charge, NACL resets to zero; *writing to the NAC register affects the available charge counts and, therefore, affects the bq2011J gas gauge operation.*

Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V_{CC} is greater than 2V. The contents of BATID have no effect on the operation of the bq2011J. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2011J uses as a measured full reference. The bq2011J adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2011J updates the capacity of the battery. LMD is set to PFC during a bq2011J reset.

Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2011J flags.

The ***charge rate*** flag (CR) is used to denote the fast charge regime. Fast charge is assumed whenever a charge action is initiated. The CR flag remains asserted if the charge rate does not fall below 2 counts/sec.

The CR values are:

FLGS2 Bits							
7	6	5	4	3	2	1	0
CR	-	-	-	-	-	-	-

Where CR is:

0 When charge rate falls below 2 counts/sec

1 When charge rate is above 2 counts/sec

The fast charge regime efficiency factors are used when CR = 1. When CR = 0, the trickle charge efficiency factors are used. The time to change CR varies due to the user-selectable count rates.

The ***discharge rate*** flags, DR2–0, are bits 6–4.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-	-	-	

They are used to determine the present discharge regime as follows:

DR2	DR1	DR0	C_{RATE}@LMD = 90h
0	0	0	C_{RATE} < 6C
0	0	1	6C ≤ C_{RATE} < 12C
0	1	0	12C ≤ C_{RATE} < 18C
0	1	1	C_{RATE} ≥ 18C

The ***overload*** flag (OVLD) is asserted when a discharge overload is detected, C_{RATE} ≥ 6.0C for LMD = 90h (see Discharge Compensation, page 8). OVLD remains asserted as long as the condition is valid.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OVLD

Full Count Register (FULCNT)

The read-only FULCNT register (address=0bh) provides the system with a diagnostic of the number of times the battery has been fully charged (NAC = LMD). The number of full occurrences can be determined by multiplying the value in the FULCNT register by 16. Any dis-

13/18

charge action other than self-discharge allows detection of another full occurrence during the next valid charge action.

Capacity Inaccurate Count Register (CPI)

The read-only CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2011J adapts to the changing capacity over time. A complete discharge from full (NAC=LMD) to empty (EDV=1) is required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and the self-discharge counter is less than 4096 counts.

The CPI register is incremented every time a valid charge is detected. The register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. CPI is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

Output Control Register (OCTL)

The write-only OCTL register (address=0ah) provides the system with a means to check the display connections for the bq2011J. The segment drivers may be overwritten by data from OCTL when the least-significant bit of OCTL, OCE, is set. The data in bits OC_{5-1} of the OCTL register (see Table 5 on page 10 for details) is output onto the segment pins, SEG_{5-1}, respectively if OCE=1. *Whenever OCE is written to 1, the MSB of OCTL should be set to a 1.* The OCE register location must be cleared to return the bq2011J to normal operation. OCE may be cleared by either writing the bit to a logic zero via the serial port or by resetting the bq2011J as explained below. **Note:** Whenever the OCTL register is written, the MSB of OCTL should be written to a logic one.

Reset Register (RST)

The reset register (address=39h) provides the means to perform a software-controlled reset of the device. A full device reset may be accomplished by first writing LMD (address = 05h) to 00h and then writing the RST register contents from 00h to 80h. *Setting any bit other than the most-significant bit of the RST register is* ***not allowed****, and results in improper operation of the bq2011J.*

Resetting the bq2011J sets the following:

- LMD = PFC
- CPI, VDQ, OCE, and NAC = 0
  (NAC = PFC when $PROG_4$ = L)
- CI and BRP = 1

Display

The bq2011J can directly display capacity information using low-power LEDs. If LEDs are used, the segment pins should be tied to V_{CC}, the battery, or the MODE pin for programming the bq2011J.

The bq2011J displays the battery charge state in absolute mode. In absolute mode, each segment represents a fixed amount of charge, based on the initial PFC. In absolute mode, each segment represents 20% of the PFC. As the battery wears out over time, it is possible for the LMD to be below the initial PFC. In this case, all of the LEDs may not turn on, representing the reduction in the actual battery capacity.

The capacity display is also adjusted for the present battery temperature. The temperature adjustment reflects the available capacity at a given temperature but does not affect the NAC register. The temperature adjustments are detailed in the TMPGG register description on page 12.

When $\overline{DISP}$ is tied to V_{CC}, the SEG_{1-5} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active during charge if the NAC registers are counting at a rate equivalent to V_{SRO} < -1mV or fast discharge if the NAC registers are counting at a rate equivalent to V_{SRO} > 2mV. When pulled low, the segment output becomes active for 4 seconds, ±0.5 seconds.

The segment outputs are modulated as two banks, with segments 1, 3, and 5 alternating with segments 2 and 4. The segment outputs are modulated at approximately 320Hz, with each bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV} to indicate a low-battery condition or NAC is less than 10% of PFC.

Microregulator

The bq2011J can operate directly from 4 cells. To facilitate the power supply requirements of the bq2011J, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2011J can be inexpensively built using the FET and an external resistor.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	7.0	V	
All other pins	Relative to V_{SS}	-0.3	7.0	V	
V_{SR}	Relative to V_{SS}	-0.3	7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2011J application note for details).
T_{OPR}	Operating temperature	0	70	°C	Commercial
		-40	85	°C	Industrial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDV}	End-of-discharge warning	0.87	0.90	0.93	V	SB
V_{SRQ}	Valid charge	-	-	-400	µV	$V_{SR} + V_{OS}$
V_{SRD}	Valid discharge	500	-	-	µV	$V_{SR} + V_{OS}$
V_{MCV}	Maximum single-cell voltage	1.95	2.0	2.05	V	SB
V_{BR}	Battery removed/replaced	-	0.1	0.25	V	SB

Note: For proper operation of the threshold detection circuit, V_{CC} must be at least 1.5V greater than the voltage being measured.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{OS}	Offset referred to V_{SR}	-	±50	±150	µV	$\overline{DISP} = V_{CC}$
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V, DQ = 0
		-	120	180	µA	V_{CC} = 4.25V, DQ = 0
		-	170	250	µA	V_{CC} = 6.5V, DQ = 0
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	$0 < V_{SB} < V_{CC}$
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	$V_{DISP} = V_{SS}$
I_{LCOM}	LCOM input leakage	-0.2	-	0.2	µA	$\overline{DISP} = V_{CC}$
I_{RBI}	RBI data-retention current	-	-	100	nA	$V_{RBI} > V_{CC} < 3V$
R_{DQ}	Internal pulldown	500	-	-	KΩ	
V_{SR}	Sense resistor input	-0.3	-	2.0	V	$V_{SR} > V_{SS}$ = discharge; $V_{SR} < V_{SS}$ = charge
R_{SR}	SR input impedance	10	-	-	MΩ	$-200mV < V_{SR} < V_{CC}$
V_{IHPFC}	PROG/SPFC logic input high	V_{CC} - 0.2	-	-	V	SPFC, $PROG_{1-4}$
V_{ILPFC}	PROG/SPFC logic input low	-	-	V_{SS} + 0.2	V	SPFC, $PROG_{1-4}$
V_{IZPFC}	PROG/SPFC logic input Z	float	-	float	V	SPFC, $PROG_{1-4}$
I_{IHPFC}	PROG/SPFC input high current	-	1.2	-	µA	$V_{PFC} = V_{CC}/2$
I_{ILPFC}	PROG/SPFC input low current	-	1.2	-	µA	$V_{PFC} = V_{CC}/2$
V_{OLSL}	SEG_X output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, $I_{OLS} \leq$ 1.75mA SEG_1–SEG_5
V_{OLSH}	SEG_X output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, $I_{OLS} \leq$ 11.0mA SEG_1–SEG_5
V_{OHML}	LCOM output high, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{OHLCOM} = -5.25mA
V_{OHMH}	LCOM output high, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} = 6.5V, I_{OHLCOM} = -33.0mA
I_{OHLCOM}	LCOM source current	-33	-	-	mA	At $V_{OHLCOM} = V_{CC}$ - 0.6V
I_{OLS}	SEG_X sink current	11.0	-	-	mA	At V_{OLSH} = 0.4V, V_{CC} = 6.5V
I_{OL}	Open-drain sink current	5.0	-	-	mA	At $V_{OL} = V_{SS}$ + 0.3V, DQ
V_{OL}	Open-drain output low	-	-	0.5	V	$I_{OL} \leq$ 5mA, DQ
V_{IHDQ}	DQ input high	2.5	-	-	V	DQ
V_{ILDQ}	DQ input low	-	-	0.8	V	DQ
R_{FLOAT}	Float state external impedance	-	5	-	MΩ	SPFC, $PROG_{1-4}$

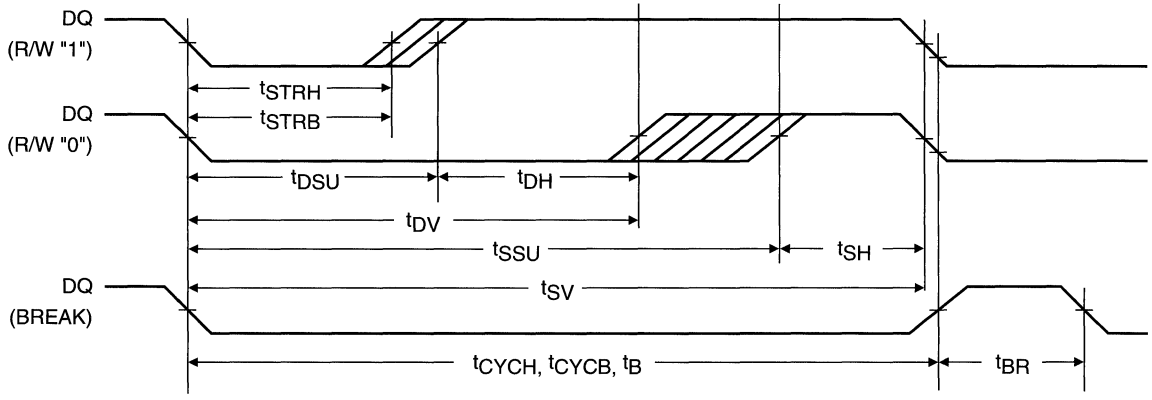
Note: All voltages relative to V_{SS}.

Serial Communication Timing Specification ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2011J	3	-	-	ms	See note
t_{CYCB}	Cycle time, bq2011J to host	3	-	6	ms	
t_{STRH}	Start hold, host to bq2011J	5	-	-	ns	
t_{STRB}	Start hold, bq2011J to host	500	-	-	µs	
t_{DSU}	Data setup	-	-	750	µs	
t_{DH}	Data hold	750	-	-	µs	
t_{DV}	Data valid	1.50	-	-	ms	
t_{SSU}	Stop setup	-	-	2.25	ms	
t_{SH}	Stop hold	700	-	-	µs	
t_{SV}	Stop valid	2.95	-	-	ms	
t_B	Break	3	-	-	ms	
t_{BR}	Break recovery	1	-	-	ms	

Note: The open-drain DQ pin should be pulled to at least V_{CC} by the host system for proper DQ operation. DQ may be left floating if the serial interface is not used.

Serial Communication Timing Illustration



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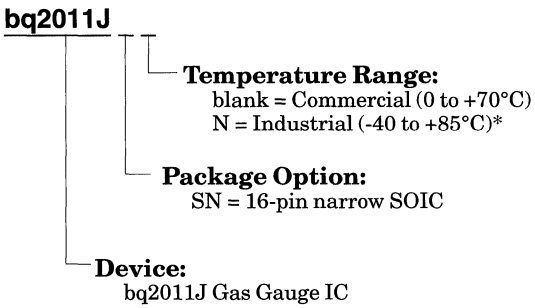
17/18

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	6	Removed relative display mode from Table 1	Correction

Notes: Change 1 = Oct. 1997 B changes from June 1995.

Ordering Information



* Contact factory for availability.

UNITRODE

bq2011K

Gas Gauge IC for High Discharge Rates

Features

- Conservative and repeatable measurement of available charge in rechargeable batteries
- Designed for portable equipment such as power tools with high discharge rates
- Designed for battery pack integration
  - 120µA typical standby current (self-discharge estimation mode)
  - Small size enables implementations in as little as ½ square inch of PCB
- Direct drive of LEDs for capacity display
- Self-discharge compensation using internal temperature sensor
- Simple single-wire serial communications port for subassembly testing
- 16-pin narrow SOIC

General Description

The bq2011K Gas Gauge IC is intended for battery-pack installation to maintain an accurate record of a battery's available charge. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery. The bq2011K is designed for systems such as power tools with very high discharge rates.

Battery self-discharge is estimated based on an internal timer and temperature sensor. Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and selfdischarge calculations to provide available charge information across a wide range of operating conditions. Initial battery capacity is set using the $PROG_{1-4}$ and SPFC pins. Actual battery capacity is automatically "learned" in the course of a discharge cycle from full to empty and may be displayed depending on the display mode.

Nominal available charge may be directly indicated using a five-segment LED display. These segments are used to graphically indicate nominal available charge.

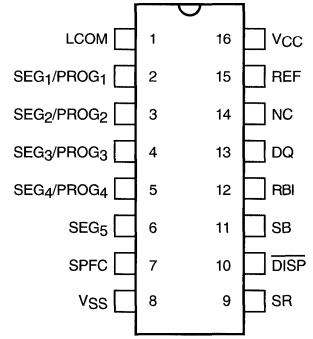
The bq2011K supports a simple single-line bidirectional serial link to an external processor (common ground). The bq2011K outputs battery information in response to external commands over the serial link. To support subassembly testing, the outputs may also be controlled by command. The external processor may also overwrite some of the bq2011K gas gauge data registers.

The bq2011K may operate directly from four cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide V_{CC} from a greater number of cells.

Internal registers include available charge, temperature, capacity, battery ID, and battery status.

4

Pin Connections



16-Pin Narrow SOIC

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Pin Names

LCOM	LED common output
$SEG_1/PROG_1$	LED segment 1/ Program 1 input
$SEG_2/PROG_2$	LED segment 2 / Program 2 input
$SEG_3/PROG_3$	LED segment 3/ Program 3 input
$SEG_4/PROG_4$	LED segment 4/ Program 4 input
SEG_5	LED segment 5
SPFC	Programmed full count selection input
REF	Voltage reference output
NC	No connect
DQ	Serial communications input/output
RBI	Register backup input
SB	Battery sense input
$\overline{DISP}$	Display control input
SR	Sense resistor input
V_{CC}	3.0–6.5V
V_{SS}	Negative battery terminal

Pin Descriptions

LCOM **LED common**

Open-drain output switches V_{CC} to source current for the LEDs. The switch is off during initialization to allow reading of $PROG_{1-4}$ pull-up or pull-down program resistors. LCOM is high impedance when the display is off.

SEG_1–SEG_5 **LED display segment outputs**

Each output may activate an LED to sink the current sourced from LCOM, the battery, or V_{CC}.

$PROG_1$–$PROG_4$ **Programmed full count selection inputs (dual function with SEG_1 - SEG_4)**

These three-level input pins define the programmed full count (PFC) in conjunction with SPFC pin, define the display mode and enable or disable self-discharge.

SPFC **Programmed full count selection input**

This three-level input pin along with $PROG_{1-3}$ define the programmed full count (PFC) thresholds described in Table 1. The state of the SPFC pin is only read immediately after a reset condition.

SR **Sense resistor input**

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied to the low side of the sense resistor and battery pack ground (see Figure 1). $V_{SR} > V_{SS}$ indicates discharge, and $V_{SR} < V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2011K is $V_{SR} + V_{OS}$ (see Table 4).

NC **No connect**

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ floating allows the LED display to be active during certain charge and discharge conditions. Transitioning $\overline{DISP}$ low activates the display for 4 ± 0.5 seconds.

SB **Secondary battery input**

This input monitors the single-cell voltage potential through a high-impedance resistive divider network for the end-of-discharge voltage (EDV) threshold and maximum cell voltage (MCV).

RBI **Register backup input**

This input is used to provide backup potential to the bq2011K registers during periods when $V_{CC} < 3V$. A storage capacitor should be connected to RBI.

DQ **Serial I/O pin**

This is an open-drain bidirectional pin.

REF **Voltage reference output for regulator**

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} **Supply voltage input**

V_{SS} **Ground**

Functional Description

General Operation

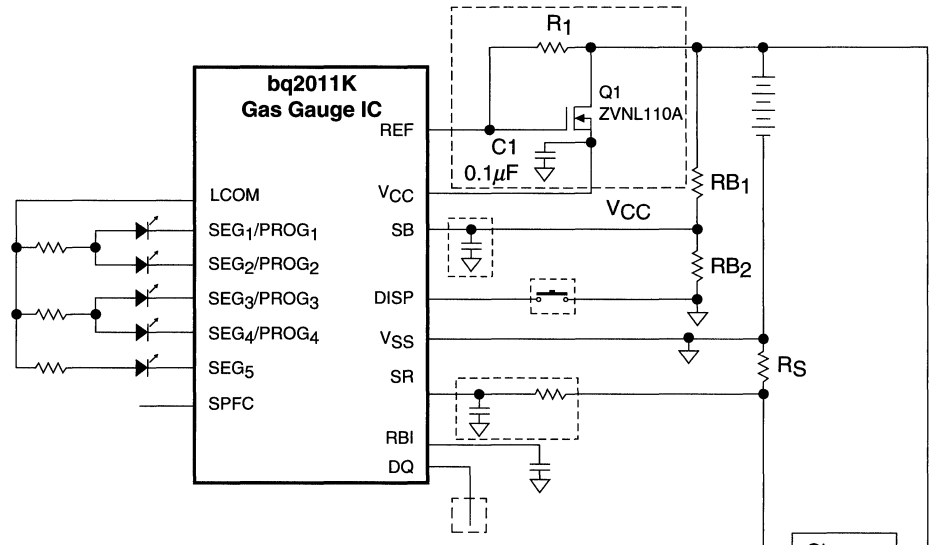
The bq2011K determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2011K measures discharge and charge currents, estimates self-discharge, monitors the battery for low-battery voltage thresholds, and compensates for temperature and charge/discharge rates. The charge measurement is made by monitoring the voltage across a small-value series sense resistor between the battery's negative terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2011K using the LED display with absolute mode as a charge-state indicator. The absolute display mode uses the programmed full count (PFC) as the full reference, forcing each segment of the display to represent a fixed amount of charge. A push-button display feature is available for momentarily enabling the LED display.

The bq2011K monitors the charge and discharge currents as a voltage across a sense resistor (see R_S in Figure 1). A filter between the negative battery terminal and the SR pin may be required if the rate of change of the battery current is too great.

Register Backup

The bq2011K RBI input pin is intended to be used with a storage capacitor to provide backup potential to the in-



Indicates optional.

Directly connect to V_{CC} across 4 cells (4.8V nominal and should not exceed 6.5V) with a resistor and a Zener diode to limit voltage during charge. Otherwise, R1, C1, and Q1 are needed for regulation of >4 cells.

Programming resistors and ESD-protection diodes are not shown.

R-C on SR may be required (application-specific), where the maximum R should not exceed 20K.

FG201103.eps

Figure 1. Application Diagram: LED Display, Absolute Mode

3/18

ternal bq2011K registers when V_{CC} momentarily drops below 3.0V. V_{CC} is output on RBI when V_{CC} is above 3.0V.

After V_{CC} rises above 3.0V, the bq2011K checks the internal registers for data loss or corruption. If data has changed, then the NAC register is cleared, and the LMD register is loaded with the initial PFC.

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2011K monitors the single-cell battery potential through the SB pin. The single-cell voltage potential is determined through a resistor-divider network per the following equation:

$$\frac{RB_1}{RB_2} = N - 1$$

where N is the number of cells, RB_1 is connected to the positive battery terminal, and RB_2 is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV) and for maximum cell voltage (MCV). The EDV threshold level is used to determine when the battery has reached an "empty" state, and the MCV threshold is used for fault detection during charging. The MCV threshold for the bq2011K is fixed at:

$$V_{MCV} = 2.00V$$

The EDV threshold varies as a function of discharge current as follows:

V_{SRO} (mV)	V_{EDV} (V)
$0 < V_{SRO} \leq 10$	1.160
$10 < V_{SRO} \leq 20$	1.124
$20 < V_{SRO} \leq 40$	1.060
$40 < V_{SRO} \leq 60$	0.960
$V_{SRO} > 60$	0 (OVLD)

Reset

Reset can be accomplished with a command over the serial port as described on page 13.

Temperature

The bq2011K internally determines the temperature in 10°C steps centered from -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available charge display translation. The temperature range is available over the serial port in 10°C increments as shown below:

TMPGG (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2011K measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (SB and V_{CC}) should be placed as close as possible to the SB and V_{CC} pins, respectively, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor (R_S) should be as close as possible to the bq2011K.
- The R-C on the SR pin should be located as close as possible to the SR pin. The maximum R should not exceed 20K.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2011K. The bq2011K accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge currents are temperature and rate compensated, whereas self-discharge is only temperature compensated.

The main counter, Nominal Available Charge (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement

the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2011K adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the Programmed Full Count (PFC) shown in Table 1. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. **Last Measured Discharge (LMD) or learned battery capacity:**

   LMD is the last measured discharge capacity of the battery. On initialization (application of V_{CC} or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register (DCR) representing a discharge from full to below EDV. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

2. **Programmed Full Count (PFC) or initial battery capacity:**

   The initial LMD and gas gauge rate values are programmed by using PFC. The PFC also provides the 100% reference for the absolute display mode. The bq2011K is configured for a given application by selecting a PFC value from Table 1. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

   Battery capacity (mAh) * sense resistor (Ω) =

   PFC (mVh)

   Selecting a PFC slightly less than the rated capacity for absolute mode provides capacity above the full reference for much of the battery's life.

Example: Selecting a PFC Value

Given:

Sense resistor = 0.002Ω
Number of cells = 6
Capacity = 1800mAh, NiCd cells
Current range = 1A to 80A
Absolute display mode
Self-discharge = $\frac{\%}{80}$
Voltage drop across sense resistor = 2mV to 160mV

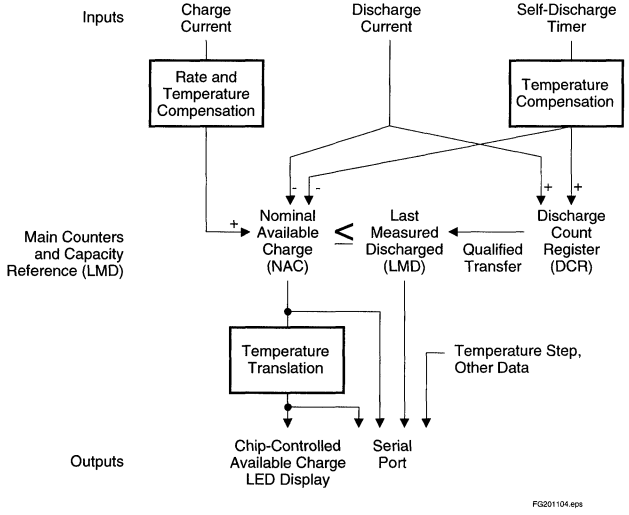


Figure 2. Operational Overview

Therefore:

$$1800mAh * 0.002\Omega = 3.6mVh$$

Select:

PFC = 35840 counts or 3.39mVh
SPFC = Z (float)
PROG1, PROG2 = H or Z
PROG3 = L
PROG4 = H or Z

The initial full battery capacity is 3.39mVh (1695mAh) until the bq2011K "learns" a new capacity with a qualified discharge from full to EDV.

3. Nominal Available Charge (NAC):

NAC counts up during charge to a maximum value of LMD and down during discharge and self discharge to 0. NAC is reset to 0 on initialization and on the first valid charge following discharge to EDV. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = LMD.

Note: NAC is set to the value in LMD when $PROG_4$ is pulled low during a reset.

Table 1. bq2011K Programmed Full Count mVh Selections

Programmed Full Count (PFC)	mVh	Scale	Display Mode	SPFC	$PROG_1$	$PROG_2$	$PROG_3$
40192	3.81	1/10560	Absolute	H	H or Z	H or Z	H or Z
32256	3.05	1/10560		Z	H or Z	H or Z	H or Z
28928	2.74	1/10560		L	H or Z	H or Z	H or Z
25856	2.45	1/10560		H	L	H or Z	H or Z
35840	3.39	1/10560		Z	L	H or Z	H or Z
23296	2.21	1/10560		L	L	H or Z	H or Z

Table 2. Programmed Self-Discharge

$PROG_4$	NAC Reset Value	Self-Discharge
H or Z	NAC = 0	Enabled
L	NAC = PFC	Disabled

4. **Discharge Count Register (DCR):**

   The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC = LMD. The DCR does not roll over but stops counting when it reaches FFFFh.

   The DCR value becomes the new LMD value on the first charge after a valid discharge to V_{EDV} if:

   No valid charge initiations (charges greater than 256 NAC counts; or 0.006 – 0.01C) occurred during the period between NAC = LMD and EDV detected.

   The self-discharge count is not more than 4096 counts (8% to 18% of PFC, specific percentage threshold determined by PFC).

   The temperature is ≥ 0°C when the EDV level is reached during discharge.

   The valid discharge flag (VDQ) indicates whether the present discharge is valid for LMD update.

Charge Counting

Charge activity is detected based on a negative voltage on the V_{SR} input. If charge activity is detected, the bq2011K increments NAC at a rate proportional to V_{SRO} (V_{SR} + V_{OS}) and, if enabled, activates an LED display if V_{SRO} < -2mV. Charge actions increment the NAC after compensation for charge rate and temperature.

The bq2011K determines a valid charge activity sustained at a continuous rate equivalent to V_{SRO} < -400µV. A valid charge equates to a sustained charge activity greater than 256 NAC counts. Once a valid charge is detected, charge counting continues until V_{SRO} rises above -400µV.

Discharge Counting

All discharge counts where V_{SRO} > 500µV cause the NAC register to decrement and the DCR to increment. Exceeding the fast discharge threshold (FDQ) if the rate is equivalent to V_{SRO} > 2mV activates the display, if enabled. The display remains active for 10 seconds after V_{SRO} falls below 2mV.

Self-Discharge Estimation

The bq2011K continuously decrements NAC and increments DCR for self-discharge based on time and temperature. The self-discharge count rate is programmed to be a nominal $\frac{1}{80}$ * NAC rate per day or disabled per Table 2. This is the rate for a battery temperature between 20–30°C. The NAC register cannot not be decremented below 0.

Count Compensations

The bq2011K determines fast charge when the NAC updates at a rate of ≥2 counts/sec. Charge activity is compensated for temperature and rate before updating the NAC and/or DCR. Self-discharge estimation is compensated for temperature before updating the NAC or DCR.

Charge Compensation

Two charge efficiency factors are used for trickle charge and fast charge. Fast charge is defined as a rate of charge resulting in ≥ 2 NAC counts/sec (≥ 0.15C to 0.32C depending on PFC selections; see Table 1). The compensation defaults to the fast charge factor until the actual charge rate is determined.

Temperature adapts the charge rate compensation factors over three ranges between nominal, warm, and hot temperatures. The compensation factors are shown below.

Charge Temperature	Trickle Charge Compensation	Fast Charge Compensation
<30°C	0.80	0.95
30–50°C	0.75	0.90
> 50°C	0.70	0.85

Discharge Compensation

Corrections for the rate of discharge are made by adjusting EDV thresholds. The compensation factor used during discharge is set to 1.00 for all rates and temperatures. The recoverable charge at colder temperatures is adjusted for display purposes only. See page 13.

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of $1/80$ * NAC per day or disabled. This is the rate for a battery within the 20–30°C temperature range (TMPGG = 6x). This rate varies across 8 ranges from <10°C to >70°C, doubling with each higher temperature step (10°C). See Table 3.

Table 3. Self-Discharge Compensation

Temperature Range	Self-Discharge Compensation Typical Rate/Day
< 10°C	$NAC/320$
10–20°C	$NAC/160$
20–30°C	$NAC/80$
30–40°C	$NAC/40$
40–50°C	$NAC/20$
50–60°C	$NAC/10$
60–70°C	$NAC/5$
> 70°C	$NAC/2.5$

Error Summary

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see the DCR description in the "Layout Considerations" section). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

Current-Sensing Error

Table 4 illustrates the current-sensing error as a function of V_{SR}. A digital filter eliminates charge and discharge counts to the NAC register when V_{SRO} (V_{SR} + V_{OS}) is between -400µV and 500µV.

Communicating With the bq2011K

The bq2011K includes a simple single-pin (DQ plus return) serial data interface. A host processor uses the interface to access various bq2011K registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain DQ pin on the bq2011K should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2011K. The command directs the bq2011K to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 333 bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2011K may be sampled using the pulse-width capture timers available on some microcontrollers.

Communication is normally initiated by the host processor sending a BREAK command to the bq2011K. A BREAK is detected when the DQ pin is driven to a logic-low state for a time, t_B or greater. The DQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2011K is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2011K taking the DQ pin to a

Table 4. bq2011K Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

logic-low state for a period, $t_{STRH,B}$. The next section is the actual data transmission, where the data should be valid by a period, t_{DSU}, after the negative edge used to start communication. The data should be held for a period, t_{DV}, to allow the host or bq2011K to sample the data bit.

The final section is used to stop the transmission by returning the DQ pin to a logic-high state by at least a period, t_{SSU}, after the negative edge used to start communication. The final logic-high state should be held until a period, t_{SV}, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2011K is always performed with the least-significant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2011K NAC register.

bq2011K Registers

The bq2011K command and status registers are listed in Table 5 and described below.

Command Register (CMDR)

The write-only CMDR register is accessed when eight valid command bits have been received by the bq2011K. The CMDR register contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function.

The W/$\overline{R}$ values are:

CMDR Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is:

0 The bq2011K outputs the requested register contents specified by the address portion of CMDR.

1 The following eight bits should be written to the register specified by the address portion of CMDR.

The lower seven-bit field of CMDR contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

CMDR Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Primary Status Flags Register (FLGS1)

The read-only FLGS1 register (address=01h) contains the primary bq2011K flags.

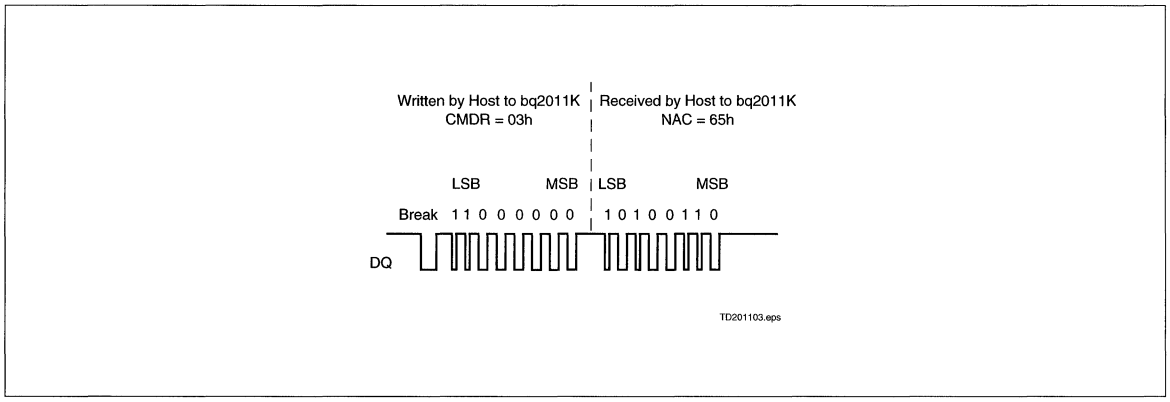


Figure 3. Typical Communication With the bq2011K

Table 5. bq2011K Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	Command register	00h	Write	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
FLGS1	Primary status flags register	01h	Read	CHGS	BRP	MCV	n/u	VDQ	n/u	EDV	n/u
TMPGG	Temperature and gas gauge register	02h	Read	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available charge high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	Nominal available charge low byte register	17h	Read	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	Read	CR	DR2	DR1	DR0	n/u	n/u	n/u	OVLD
OCTL	Output control register	0ah	Write	1	OC5	OC4	OC3	OC2	OC1	n/u	OCE
RST	Reset register	39h	Write	RST	0	0	0	0	0	0	0

Note: n/u = not used

The ***charge status*** flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when V_{SRO} < -400µV. A V_{SRO} of greater than-400µV or discharge activity clears CHGS.

The CHGS values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
CHGS	-	-	-	-	-	-	-

Where CHGS is:

0 Either discharge activity detected or V_{SRO} > -400µV

1 V_{SRO} < -400µV

The ***battery replaced*** flag (BRP) is asserted whenever the potential on the SB pin (relative to V_{SS}), V_{SB}, rises above 0.1V and determines the internal registers have been corrupted. The BRP flag is also set when the bq2011K is reset (see the RST register description). BRP is cleared if either the bq2011K is charged until NAC = LMD or discharged until EDV is reached. BRP = 1 signifies that the device has been reset.

The BRP values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	BRP	-	-	-	-	-	-

Where BRP is:

0 bq2011K is charged until NAC = LMD or discharged until the EDV flag is asserted

1 Initial or full V_{CC} reset, or a serial port initiated reset has occurred

The ***maximum cell voltage*** flag (MCV) is asserted whenever the potential on the SB pin (relative to V_{SS}) is above 2.0V. The MCV flag is asserted until the condition causing MCV is removed.

The MCV values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	MCV	-	-	-	-	-

Where MCV is:

0 V_{SB} < 2.0V

1 V_{SB} > 2.0V

The ***valid discharge*** flag (VDQ) is asserted when the bq2011K is discharged from NAC=LMD. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- The self-discharge count register (SDCR) has exceeded the maximum acceptable value (4096 counts) for an LMD update.
- A valid charge action equal to 256 NAC counts with V_{SRO} < -400µV.
- The EDV flag was set at a temperature below 0°C

The VDQ values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

Where VDQ is:

0 SDCR ≥ 4096, subsequent valid charge action detected, or EDV is asserted with the temperature less than 0°C

1 On first discharge after NAC = LMD

The ***end-of-discharge warning*** flag (EDV) warns the user that the battery is empty. SEG1 blinks at a 4Hz rate. EDV detection is disabled if OVLD = 1. The EDV flag is latched until a valid charge has been detected.

The EDV values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV	-

Where EDV is:

0 Valid charge action detected

1 V_{SB} < V_{EDV}

Temperature and Gas Gauge Register (TMPGG)

The read-only TMPGG register (address=02h) contains two data fields. The first field contains the battery temperature. The second field contains the available charge from the battery.

TMPGG Temperature Bits							
7	6	5	4	3	2	1	0
TMP3	TMP2	TMP1	TMP0	-	-	-	

The bq2011K contains an internal temperature sensor. The temperature is used to set charge efficiency factors as well as to adjust the self-discharge coefficient. The temperature register contents may be translated as shown in Table 6.

11/18

Table 6. Temperature Register Contents

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

The bq2011K calculates the available charge as a function of NAC, temperature, and a full reference, either LMD or PFC. The results of the calculation are available via the display port or the gas gauge field of the TMPGG register. The register is used to give available capacity in $\frac{1}{16}$ increments from 0 to $\frac{15}{16}$.

TMPGG Gas Gauge Bits							
7	6	5	4	3	2	1	0
-	-	-	-	GG3	GG2	GG1	GG0

The gas gauge display and the gas gauge portion of the TMPGG register are adjusted for cold temperature dependencies. A piece-wise correction is performed as follows:

Temperature	Available Capacity Calculation
> 0°C	NAC / "Full Reference"
-20°C < T < 0°C	0.75 * NAC / "Full Reference"
< -20°C	0.5 * NAC / "Full Reference"

The adjustment between > 0°C and -20°C < T < 0°C has a 4°C hysteresis.

Nominal Available Charge Register (NAC)

The read/write NACH register (address=03h) and the read-only NACL register (address=17h) are the main gas gauging registers for the bq2011K. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC.

If SEG_4 = 0 on reset, then NACH = PFC and NACL = 0. If SEG_4 = Z or H, the NACH and NACL registers are cleared to zero. NACL stops counting when NACH reaches zero. When the bq2011K detects a valid charge, NACL resets to zero; *writing to the NAC register affects the available charge counts and, therefore, affects the bq2011K gas gauge operation.*

Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V_{CC} is greater than 2V. The contents of BATID have no effect on the operation of the bq2011K. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2011K uses as a measured full reference. The bq2011K adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2011K updates the capacity of the battery. LMD is set to PFC during a bq2011K reset.

Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2011K flags.

The ***charge rate*** flag (CR) is used to denote the fast charge regime. Fast charge is assumed whenever a charge action is initiated. The CR flag remains asserted if the charge rate does not fall below 2 counts/sec.

The CR values are:

FLGS2 Bits							
7	6	5	4	3	2	1	0
CR	-	-	-	-	-	-	-

Where CR is:

0 When charge rate falls below 2 counts/sec

1 When charge rate is above 2 counts/sec

12/18

The fast charge regime efficiency factors are used when CR = 1. When CR = 0, the trickle charge efficiency factors are used. The time to change CR varies due to the user-selectable count rates.

The ***discharge rate*** flags, DR2–0, are bits 6–4.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-	-	-	

They are used to determine the present discharge regime as follows:

DR2	DR1	DR0	V_{SRO}(mV)
0	0	0	$0 < V_{SRO} \leq 10$
0	0	1	$10 < V_{SRO} \leq 20$
0	1	0	$20 < V_{SRO} \leq 40$
0	1	1	$40 < V_{SRO} \leq 60$
1	0	0	$V_{SRO} > 60$

The ***overload*** flag (OVLD) is asserted when a discharge overload is detected, V_{SRO} > 60mV. OVLD remains asserted as long as the condition is valid.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OVLD

Output Control Register (OCTL)

The write-only OCTL register (address=0ah) provides the system with a means to check the display connections for the bq2011K. The segment drivers may be overwritten by data from OCTL when the least-significant bit of OCTL, OCE, is set. The data in bits OC_{5-1} of the OCTL register (see Table 5 for details) is output onto the segment pins, SEG_{5-1}, respectively if OCE=1. *Whenever OCE is written to 1, the MSB of OCTL should be set to a 1.* The OCE register location must be cleared to return the bq2011K to normal operation. OCE may be cleared by either writing the bit to a logic zero via the serial port or by resetting the bq2011K as explained below. **Note:** Whenever the OCTL register is written, the MSB of OCTL should be written to a logic one.

Reset Register (RST)

The reset register (address=39h) provides the means to perform a software-controlled reset of the device. A full device reset may be accomplished by first writing LMD (address = 05h) to 00h and then writing the RST register contents from 00h to 80h. *Setting any bit other than the most-significant bit of the RST register is* ***not allowed****, and results in improper operation of the bq2011K.*

Resetting the bq2011K sets the following:

- LMD = PFC
- VDQ, OCE, and NAC = 0
  (NAC = PFC when $PROG_4$ = L)
- BRP = 1

Display

The bq2011K can directly display capacity information using low-power LEDs. If LEDs are used, the segment pins should be tied to V_{CC}, the battery, or the LCOM pin through resistors for programming the bq2011K.

The bq2011K displays the battery charge state in absolute mode. In absolute mode, each segment represents a fixed amount of charge, based on the initial PFC. In absolute mode, each segment represents 20% of the PFC. As the battery wears out over time, it is possible for the LMD to be below the initial PFC. In this case, all of the LEDs may not turn on, representing the reduction in the actual battery capacity.

The capacity display is also adjusted for the present battery temperature. The temperature adjustment reflects the available capacity at a given temperature but does not affect the NAC register. The temperature adjustments are detailed in the TMPGG register description.

When $\overline{DISP}$ is tied to V_{CC}, the SEG_{1-5} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active during charge if the NAC registers are counting at a rate equivalent to V_{SRO} < -2mV or fast discharge if the NAC registers are counting at a rate equivalent to V_{SRO} > 2mV. When $\overline{DISP}$ is left floating, the display also becomes active after the detection of a discharge signal with a minimum amplitude of V_{SR} > 20mV (10A for R_S = 0.002Ω) and a minimum pulse width of 25ms. When $\overline{DISP}$ is pulled low, the segment outputs become active for 4s, ±0.5s.

The segment outputs are modulated as two banks, with segments 1, 3, and 5 alternating with segments 2 and 4. The segment outputs are modulated at approximately 320Hz, with each bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV} to indicate a low-battery condition or NAC is less than 10% of PFC.

Microregulator

The bq2011K can operate directly from 4 cells. To facilitate the power supply requirements of the bq2011K, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2011K can be inexpensively built using the FET and an external resistor.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	7.0	V	
All other pins	Relative to V_{SS}	-0.3	7.0	V	
V_{SR}	Relative to V_{SS}	-0.3	7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2011K application note for details).
T_{OPR}	Operating temperature	0	70	°C	Commercial
		-40	85	°C	Industrial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDV}	End-of-discharge warning	0.96 * V_{EDV}	V_{EDV}	1.04 * V_{EDV}	V	SB
V_{SRQ}	Valid charge	-	-	-400	µV	$V_{SR} + V_{OS}$
V_{SRD}	Valid discharge	500	-	-	µV	$V_{SR} + V_{OS}$
V_{MCV}	Maximum single-cell voltage	1.95	2.0	2.05	V	SB

Note: For proper operation of the threshold detection circuit, V_{CC} must be at least 1.5V greater than the voltage being measured.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
VOS	Offset referred to V_{SR}	-	±50	±150	µV	$\overline{DISP} = V_{CC}$
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V, DQ = 0
		-	120	180	µA	V_{CC} = 4.25V, DQ = 0
		-	170	250	µA	V_{CC} = 6.5V, DQ = 0
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	$0 < V_{SB} < V_{CC}$
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	$V_{DISP} = V_{SS}$
I_{LCOM}	LCOM input leakage	-0.2	-	0.2	µA	$\overline{DISP} = V_{CC}$
I_{RBI}	RBI data-retention current	-	-	100	nA	$V_{RBI} > V_{CC} < 3V$
R_{DQ}	Internal pulldown	500	-	-	KΩ	
V_{SR}	Sense resistor input	-0.3	-	2.0	V	$V_{SR} > V_{SS}$ = discharge; $V_{SR} < V_{SS}$ = charge
R_{SR}	SR input impedance	10	-	-	MΩ	$-200mV < V_{SR} < V_{CC}$
V_{IHPFC}	PROG/SPFC logic input high	V_{CC} - 0.2	-	-	V	SPFC, $PROG_{1-4}$
V_{ILPFC}	PROG/SPFC logic input low	-	-	V_{SS} + 0.2	V	SPFC, $PROG_{1-4}$
V_{IZPFC}	PROG/SPFC logic input Z	float	-	float	V	SPFC, $PROG_{1-4}$
I_{IHPFC}	PROG/SPFC input high current	-	1.2	-	µA	$V_{PFC} = V_{CC}/2$
I_{ILPFC}	PROG/SPFC input low current	-	1.2	-	µA	$V_{PFC} = V_{CC}/2$
V_{OLSL}	SEG_X output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, $I_{OLS} \leq$ 1.75mA SEG_1–SEG_5
V_{OLSH}	SEG_X output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, $I_{OLS} \leq$ 11.0mA SEG_1–SEG_5
V_{OHML}	LCOM output high, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{OHLCOM} = -5.25mA
V_{OHMH}	LCOM output high, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} = 6.5V, I_{OHLCOM} = -33.0mA
I_{OHLCOM}	LCOM source current	-33	-	-	mA	At $V_{OHLCOM} = V_{CC}$ - 0.6V
I_{OLS}	SEG_X sink current	11.0	-	-	mA	At V_{OLSH} = 0.4V, V_{CC} = 6.5V
I_{OL}	Open-drain sink current	5.0	-	-	mA	At $V_{OL} = V_{SS}$ + 0.3V, DQ
V_{OL}	Open-drain output low	-	-	0.5	V	$I_{OL} \leq$ 5mA, DQ
V_{IHDQ}	DQ input high	2.5	-	-	V	DQ
V_{ILDQ}	DQ input low	-	-	0.8	V	DQ
R_{FLOAT}	Float state external impedance	-	5	-	MΩ	SPFC, $PROG_{1-4}$

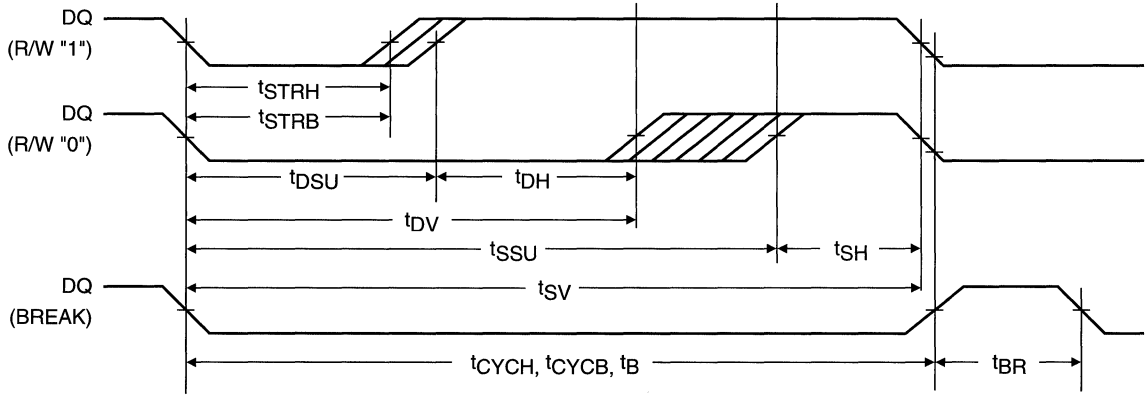
Note: All voltages relative to V_{SS}.

Serial Communication Timing Specification ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2011K	3	-	-	ms	See note
t_{CYCB}	Cycle time, bq2011K to host	3	-	6	ms	
t_{STRH}	Start hold, host to bq2011K	5	-	-	ns	
t_{STRB}	Start hold, bq2011K to host	500	-	-	µs	
t_{DSU}	Data setup	-	-	750	µs	
t_{DH}	Data hold	750	-	-	µs	
t_{DV}	Data valid	1.50	-	-	ms	
t_{SSU}	Stop setup	-	-	2.25	ms	
t_{SH}	Stop hold	700	-	-	µs	
t_{SV}	Stop valid	2.95	-	-	ms	
t_B	Break	3	-	-	ms	
t_{BR}	Break recovery	1	-	-	ms	

Note: The open-drain DQ pin should be pulled to at least V_{CC} by the host system for proper DQ operation. DQ may be left floating if the serial interface is not used.

Serial Communication Timing Illustration



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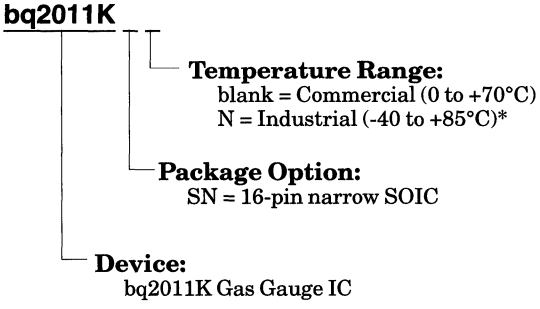
Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	6	Removed relative display mode from Table 1	Correction

Notes: Change 1 = Oct. 1997 B changes from Oct. 1995.

Ordering Information



* Contact factory for availability.

bq2012

Gas Gauge IC With Slow-Charge Control

Features

- Conservative and repeatable measurement of available charge in rechargeable batteries
- Charge control output
- Designed for battery pack integration
  - 120µA typical standby current (self-discharge estimation mode)
  - Small size enables implementations in as little as ½ square inch of PCB
- Integrate within a system or as a stand-alone device
  - Display capacity via single-wire serial communication port or direct drive of LEDs
- Measurements compensated for current and temperature
- Self-discharge compensation using internal temperature sensor
- 16-pin narrow SOIC

General Description

The bq2012 Gas Gauge IC is intended for battery-pack or in-system installation to maintain an accurate record of available battery charge. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery.

Self-discharge of NiMH and NiCd batteries is estimated based on an internal timer and temperature sensor. Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and self-discharge calculations to provide available charge information across a wide range of operating conditions. Battery capacity is automatically recalibrated, or "learned," in the course of a discharge cycle from full to empty.

The bq2012 includes a charge control output that, when used with other full-charge safety termination methods, can provide a cost-effective means of controlling charge based on the battery's charge state.

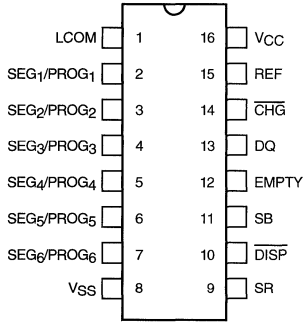
Nominal available charge may be directly indicated using a five- or six-segment LED display. These segments are used to graphically indicate nominal available charge.

The bq2012 supports a simple single-line bidirectional serial link to an external processor (common ground). The bq2012 outputs battery information in response to external commands over the serial link.

Internal registers include available charge, temperature, capacity, battery ID, battery status, and programming pin settings. To support subassembly testing, the outputs may also be controlled. The external processor may also overwrite some of the bq2012 gas gauge data registers.

The bq2012 may operate directly from three or four cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide V_{CC} across a greater number of cells.

Pin Connections



16-Pin Narrow SOIC

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Pin Names

LCOM	LED common output
$SEG_1/PROG_1$	LED segment 1/ program 1 input
$SEG_2/PROG_2$	LED segment 2/ program 2 input
$SEG_3/PROG_3$	LED segment 3/ program 3 input
$SEG_4/PROG_4$	LED segment 4/ program 4 input
$SEG_5/PROG_5$	LED segment 5/ program 5 input
$SEG_6/PROG_6$	LED segment 6/ program 6 input
REF	Voltage reference output
$\overline{CHG}$	Charge control output
DQ	Serial communications input/output
EMPTY	Empty battery indicator output
SB	Battery sense input
$\overline{DISP}$	Display control input
SR	Sense resistor input
V_{CC}	3.0–6.5V
V_{SS}	System ground

Pin Descriptions

LCOM **LED common output**

Open-drain output switches V_{CC} to source current for the LEDs. The switch is off during initialization to allow reading of the soft pull-up or pull-down program resistors. LCOM is also high impedance when the display is off.

SEG_1–SEG_6 **LED display segment outputs (dual function with $PROG_1$–$PROG_6$)**

Each output may activate an LED to sink the current sourced from LCOM.

$PROG_1$–$PROG_2$ **Programmed full count selection inputs (dual function with SEG_1–SEG_2)**

These three-level input pins define the programmed full count (PFC) thresholds described in Table 2.

$PROG_3$–$PROG_4$ **Gas gauge rate selection inputs (dual function with SEG_3–SEG_4)**

These three-level input pins define the scale factor described in Table 2.

$PROG_5$ **Self-discharge rate selection (dual function with SEG_5)**

This three-level input pin defines the selfdischarge compensation rate shown in Table 1.

$PROG_6$ **Display mode selection (dual function with SEG_6)**

This three-level pin defines the display operation shown in Table 1.

$\overline{CHG}$ **Charge control output**

This open-drain output becomes active low when charging is allowed. Valid charging conditions are described in the Charge Control section.

SR **Sense resistor input**

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied to the high side of the sense resistor. $V_{SR} < V_{SS}$ indicates discharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop (V_{SRO}) as seen by the bq2012 is $V_{SR} + V_{OS}$ (see Table 5).

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ tied to V_{CC} allows $PROG_X$ to connect directly to V_{CC} or V_{SS} instead of through a pull-up or pull-down resistor. $\overline{DISP}$ floating allows the LED display to be active during a valid charge or during discharge if the NAC register is updated at a rate equivalent to $V_{SRO} \leq$ -4mV. $\overline{DISP}$ low activates the display. See Table 1.

SB **Secondary battery input**

This input monitors the single-cell voltage potential through a high-impedance resistive divider network for end-of-discharge voltage (EDV) thresholds, maximum charge voltage (MCV), and battery removed.

EMPTY **Battery empty output**

This open-drain output becomes high-impedance on detection of a valid end-of-discharge voltage (V_{EDVF}) and is low following the next application of a valid charge.

DQ **Serial I/O pin**

This is an open-drain bidirectional pin.

REF **Voltage reference output for regulator**

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} **Supply voltage input**

V_{SS} **Ground**

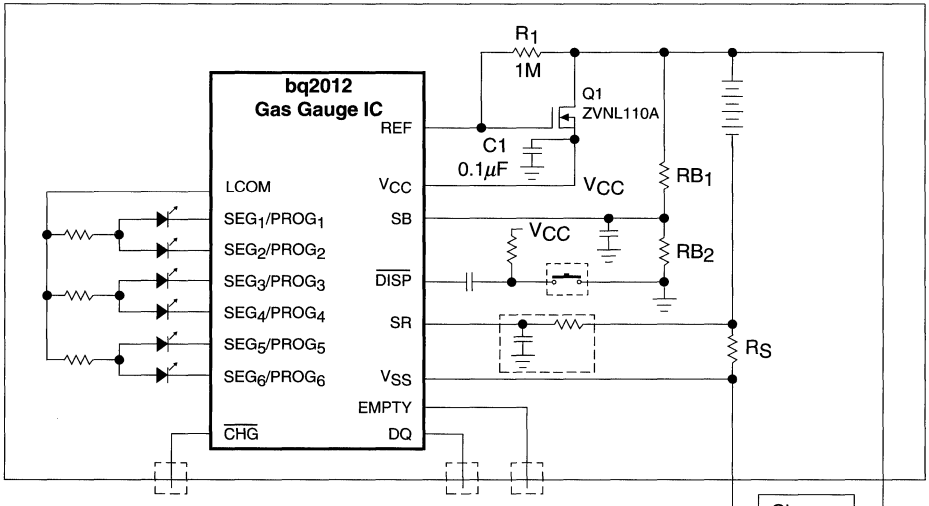
Functional Description

General Operation

The bq2012 determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2012 measures discharge and charge currents, estimates self-discharge, monitors the battery for low-battery voltage thresholds, and compensates for temperature and charge/discharge rates. The charge measurement is made by monitoring the voltage across a small-value series sense resistor between the negative battery terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2012 using the LED display capability as a charge-state indicator. The bq2012 can be configured to display capacity in either a relative or an absolute display mode. The relative display mode uses the last measured discharge capacity of the battery as the battery "full" reference. The absolute display mode uses the programmed full count (PFC) as the full reference, forcing each segment of the display to represent a fixed amount of charge. A push-button display feature is available for momentarily enabling the LED display.

The bq2012 monitors the charge and discharge currents as a voltage across a sense resistor (see R_S in Figure 1). A filter between the negative battery terminal and the SR pin may be required if the rate of change of the battery current is too great.



Indicates optional.

Directly connect to V_{CC} across 3 or 4 cells (3 to 4.8V nominal,should not exceed 6.5V) with a resistor and a Zener diode to limit voltage during charge. Otherwise, R1, C1, and Q1 are needed for regulation of >4 cells. The value of R1 depends on the number of cells.

Programming resistors (6 max.) and ESD-protection diodes are not shown.

R-C on SR may be required (application-specific), where the R should not exceed 100k.

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Figure 1. Battery Pack Application Diagram—LED Display

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2012 monitors the single-cell battery potential through the SB pin. The single-cell voltage potential is determined through a resistor/divider network per the following equation:

$$\frac{RB_1}{RB_2} = N - 1$$

where N is the number of cells, RB_1 is connected to the positive battery terminal, and RB_2 is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV) and for maximum cell voltage (MCV). EDV threshold levels are used to determine when the battery has reached an "empty" state, and the MCV threshold is used for fault detection during charging.

Two EDV thresholds for the bq2012 are fixed at:

EDV1 (early warning) = 1.05V

EDVF (empty) = 0.95V

If V_{SB} is below either of the two EDV thresholds, the associated flag is latched and remains latched, independent of V_{SB}, until the next valid charge.

During discharge and charge, the bq2012 monitors V_{SR} for various thresholds. These thresholds are used to compensate the charge and discharge rates. Refer to the count compensation section for details. EDV monitoring is disabled if $V_{SR} \leq$ -250mV typical and resumes ½ second after $V_{SR} >$ -250mV.

EMPTY Output

The EMPTY output switches to high impedance when $V_{SB} < V_{EDF}$ and remains latched until a valid charge occurs. The bq2012 also monitors V_{SB} relative to V_{MCV}, 2.25V. V_{SB} falling from above V_{MCV} resets the device.

Reset

The bq2012 recognizes a valid battery whenever V_{SB} is greater than 0.1V typical. V_{SB} rising from below 0.25V or falling from above 2.25V resets the device. Reset can also be accomplished with a command over the serial port as described in the Register Reset section.

Temperature

The bq2012 internally determines the temperature in 10°C steps centered from -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available charge display translation. The temperature range is available over the serial port in 10°C increments as shown below:

TMPGG (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2012 measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (SB and V_{CC}) should be placed as close as possible to the SB and V_{CC} pins, respectively, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor (R_S) should be as close as possible to the bq2012.
- The R-C on the SR pin should be located as close as possible to the SR pin. The maximum R should not exceed 100K.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2012. The bq2012 accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge and discharge currents are temperature and rate compensated, whereas self-discharge is only temperature compensated.

The main counter, Nominal Available Charge (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2012 adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the programmed full count (PFC) shown in Table 2. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. **Last Measured Discharge (LMD) or learned battery capacity:**

   LMD is the last measured discharge capacity of the battery. On initialization (application of V_{CC} or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register (DCR) representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

2. **Programmed Full Count (PFC) or initial battery capacity:**

   The initial LMD and gas gauge rate values are programmed by using $PROG_1$–$PROG_4$. The PFC also provides the 100% reference for the absolute display mode. The bq2012 is configured for a given application by selecting a PFC value from Table 2. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

   Battery capacity (mAh) * sense resistor (Ω) =

   PFC (mVh)

   Selecting a PFC slightly less than the rated capacity for absolute mode provides capacity above the full reference for much of the battery's life.

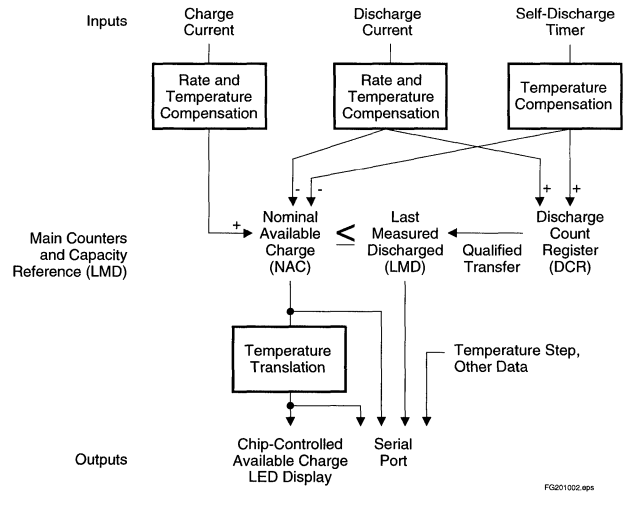


Figure 2. Operational Overview

Example: Selecting a PFC Value

Given:

Sense resistor = 0.1Ω
Number of cells = 6
Capacity = 2200mAh, NiCd battery
Current range = 50mA to 2A
Absolute display mode
Serial port only
Self-discharge = $\frac{6}{64}$
Voltage drop over sense resistor = 5mV to 200mV

Therefore:

2200mAh * 0.1Ω = 220mVh

Select:

PFC = 33792 counts or 211mVh
$PROG_1$ = float
$PROG_2$ = float
$PROG_3$ = float
$PROG_4$ = low
$PROG_5$ = float
$PROG_6$ = float

The initial full battery capacity is 211mVh (2110mAh) until the bq2012 "learns" a new capacity with a qualified discharge from full to EDV1.

Table 1. bq2012 Programming

Pin Connection	$PROG_5$ Self-Discharge Rate	$PROG_6$ Display Mode	$\overline{DISP}$ Display State
H	Self-discharge disabled	NAC = PFC on reset	LED disabled
Z	$\frac{NAC}{64}$	Absolute	LED enabled on discharge when V_{SRO} < -4mV or during a valid charge
L	$\frac{NAC}{47}$	Relative	LED on

Note: $PROG_5$ and $PROG_6$ states are independent.

Table 2. bq2012 Programmed Full Count mVh Selections

$PROG_x$		Programmed Full Count (PFC)	$PROG_4$ = L			$PROG_4$ = Z			Units
1	2		$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	
-	-	-	Scale = 1/80	Scale = 1/160	Scale = 1/320	Scale = 1/640	Scale = 1/1280	Scale = 1/2560	mVh/ count
H	H	49152	614	307	154	76.8	38.4	19.2	mVh
H	Z	45056	563	282	141	70.4	35.2	17.6	mVh
H	L	40960	512	256	128	64.0	32.0	16.0	mVh
Z	H	36864	461	230	115	57.6	28.8	14.4	mVh
Z	Z	33792	422	211	106	53.0	26.4	13.2	mVh
Z	L	30720	384	192	96.0	48.0	24.0	12.0	mVh
L	H	27648	346	173	86.4	43.2	21.6	10.8	mVh
L	Z	25600	320	160	80.0	40.0	20.0	10.0	mVh
L	L	22528	282	141	70.4	35.2	17.6	8.8	mVh
V_{SR} is equivalent to 2 counts/sec. (nom.)			90	45	22.5	11.25	5.56	2.8	mV

3. **Nominal Available Charge (NAC):**

   NAC counts up during charge to a maximum value of LMD and down during discharge and self-discharge to 0. NAC is reset to 0 on initialization ($PROG_6$ = Z or low) and on reaching EDV1. NAC is set to PFC on initialization if $PROG_6$ = high. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = LMD.

4. **Discharge Count Register (DCR):**

   The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0. DCR stops counting when EDV1 is reached. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC = LMD. The DCR does not roll over but stops counting when it reaches FFFFh.

   The DCR value becomes the new LMD value on the first charge after a valid discharge to V_{EDV1} if:

   No valid charge initiations (charges greater than 256 NAC counts; where $V_{SRO} > V_{SRQ}$) occurred during the period between NAC = LMD and EDV1 detected.

   The self-discharge count is not more than 4096 counts (8% to 18% of PFC, specific percentage threshold determined by PFC).

   The temperature is ≥ 0°C when the EDV1 level is reached during discharge.

   The valid discharge flag (VDQ) indicates whether the present discharge is valid for LMD update.

Charge Counting

Charge activity is detected based on a positive voltage on the V_{SR} input. If charge activity is detected, the bq2012 increments NAC at a rate proportional to V_{SRO} (V_{SR} + V_{OS}) and, if enabled, activates the LED display if the rate is equivalent to V_{SRO} > 4mV. Charge actions increment the NAC after compensation for charge rate and temperature.

The bq2012 determines charge activity sustained at a continuous rate equivalent to $V_{SRO} > V_{SRQ}$. A valid charge equates to sustained charge activity greater than 256 NAC counts. Once a valid charge is detected, charge counting continues until V_{SRO} falls below V_{SRQ}. V_{SRQ} is a programmable threshold as described in the Digital Magnitude Filter section. The default value for V_{SRQ} is 375µV.

Charge Control

Charge control is provided by the $\overline{CHG}$ output. This output is asserted continuously when:

NAC < 0.94 * LMD and
0.95V < V_{SB} < 2.25V and
0°C < Temp < 50°C and
BRM = 0

This output is asserted at a 1/16 duty cycle (low for 0.5 sec and high for 7.5 sec) when the above conditions are not met and:

NAC < LMD and
0.95V < V_{SB} < 2.25V and
Temp < 50°C and
BRM = 0

This output is also asserted at a 1/16 duty cycle (low for 0.5 sec and high for 7.5 sec) for a 2-hour top-off period after:

NAC = LMD and
Temp < 50°C and
0.95V < V_{SB} < 2.25V and
BRM = 0

This output is inactive when:

NAC = LMD (after a 2-hour top-off period) or
Temp > 50°C or
V_{SB} < 0.95V or
V_{SB} > 2.25V or
BRM = 1

The top-off timer (2 hours) is reset to allow another top-off after the battery is discharged to 0.8 * LMD ($PROG_6$ = L) or 0.8 * PFC ($PROG_6$ = Z or H).

Caution: The charge control output ($\overline{CHG}$) should be used with other forms of charge termination such as ΔT/Δt and -ΔV.

If charge terminates due to maximum temperature, the battery temperature must fall typically 10°C below 50°C before the charge output becomes active again.

Discharge Counting

All discharge counts where $V_{SRO} < V_{SRD}$ cause the NAC register to decrement and the DCR to increment. Exceeding the fast discharge threshold (FDQ) if the rate is equivalent to V_{SRO} < -4mV activates the display, if enabled. The display becomes inactive after V_{SRO} rises above -4mV. V_{SRD} is a programmable threshold as described in the Digital Magnitude Filter section. The default value for V_{SRD} is -300µV.

Self-Discharge Estimation

The bq2012 continuously decrements NAC and increments DCR for self-discharge based on time and temperature. The self-discharge count rate is programmed to be a nominal $1/64$ * NAC or $1/47$ * NAC per day or disabled as selected by $PROG_5$. This is the rate for a battery whose temperature is between 20°–30°C. The NAC register cannot be decremented below 0.

Count Compensations

The bq2012 determines fast charge when the NAC updates at a rate of ≥2 counts/sec. Charge and discharge are compensated for temperature and charge/discharge rate before updating the NAC and/or DCR. Self-discharge estimation is compensated for temperature before updating the NAC or DCR.

Charge Compensation

Two charge efficiency compensation factors are used for trickle charge and fast charge. Fast charge is defined as a rate of charge resulting in ≥ 2 NAC counts/sec (≥ 0.15C to 0.32C depending on PFC selections; see Table 2). The compensation defaults to the fast charge factor until the actual charge rate is determined.

Temperature adapts the charge rate compensation factors over three ranges between nominal, warm, and hot temperatures. The compensation factors are shown below.

Charge Temperature	Trickle Charge Compensation	Fast Charge Compensation
<30°C	0.80	0.95
30–40°C	0.75	0.90
> 40°C	0.65	0.80

Discharge Compensation

Corrections for the rate of discharge are made by adjusting an internal discharge compensation factor. The discharge factor is based on the dynamically measured V_{SR}. The compensation factors during discharge are:

Approximate V_{SR} Threshold	Discharge Compensation Factor	Efficiency
V_{SR} > -150 mV	1.00	100%
V_{SR} < -150 mV	1.05	95%

Temperature compensation during discharge also takes place. At lower temperatures, the compensation factor increases by 0.05 for each 10°C temperature range below 10°C.

$$\text{Compensation factor} = 1.0 + (0.05 * N)$$

Where N = Number of 10°C steps below 10°C and $-150mV < V_{SR} < 0$.

For example:

T > 10°C : Nominal compensation, N = 0

0°C < T < 10°C: N = 1 (i.e., 1.0 becomes 1.05)

-10°C < T < 0°C: N = 2 (i.e., 1.0 becomes 1.10)

-20°C < T < -10°C: N = 3 (i.e., 1.0 becomes 1.15)

-20°C < T < -30°C: N = 4 (i.e., 1.0 becomes 1.20)

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of $1/64$ * NAC or $1/47$ * NAC per day. This is the rate for a battery within the 20–30°C temperature range (TMPGG = 6x). This rate varies across 8 ranges from <10°C to >70°C, doubling with each higher temperature step (10°C). See Table 3.

Table 3. Self-Discharge Compensation

Temperature Step	Typical Rate	
	$PROG_5$ = Z	$PROG_5$ = L
< 10°C	$NAC/256$	$NAC/188$
10–20°C	$NAC/128$	$NAC/94$
20–30°C	$NAC/64$	$NAC/47$
30–40°C	$NAC/32$	$NAC/23.5$
40–50°C	$NAC/16$	$NAC/11.8$
50–60°C	$NAC/8$	$NAC/5.88$

Digital Magnitude Filter

The bq2012 has a programmable digital filter to eliminate charge and discharge counting below a set threshold. The default setting is -0.30mV for V_{SRD} and +0.38mV for V_{SRQ}. The proper digital filter setting can be calculated using the following equation. Table 4 shows typical digital filter settings.

$$V_{SRD}\ (mV) = -45 / DMF$$

$$V_{SRQ}\ (mV) = -1.25 * V_{SRD}$$

Table 4. Typical Digital Filter Settings

DMF	DMF Hex.	V_{SRD} (mV)	V_{SRQ} (mV)
75	4B	-0.60	0.75
100	64	-0.45	0.56
150 (default)	96	-0.30	0.38
175	AF	-0.26	0.32
200	C8	-0.23	0.28

Error Summary

Capacity Inaccurate

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see DCR description). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

A Capacity Inaccurate counter (CPI) is maintained and incremented each time a valid charge occurs (qualified by NAC; see the CPI register description) and is reset whenever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

Current-Sensing Error

Table 5 illustrates the current-sensing error as a function of V_{SR}. A digital filter eliminates charge and discharge counts to the NAC register when V_{SRO} (V_{SR} + V_{OS}) is between V_{SRQ} and V_{SRD}.

Communicating With the bq2012

The bq2012 includes a simple single-pin (DQ plus return) serial data interface. A host processor uses the interface to access various bq2012 registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain DQ pin on the bq2012 should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2012. The command directs the bq2012 to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 333 bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2012 may be sampled using the pulse-width capture timers available on some microcontrollers.

Communication is normally initiated by the host processor sending a BREAK command to the bq2012. A BREAK is detected when the DQ pin is driven to a logic-low state for a time, t_B or greater. The DQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2012 is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2012 taking the DQ pin to a logic-low state for a period, $t_{STRH,B}$. The next section is the actual data transmission, where the data should be valid by a period, t_{DSU}, after the negative edge used to start communication. The data should be held for a period, t_{DV}, to allow the host or bq2012 to sample the data bit.

The final section is used to stop the transmission by returning the DQ pin to a logic-high state by at least a period, t_{SSU}, after the negative edge used to start communication. The final logic-high state should be held until a period, t_{SV}, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2012 is always performed with the least-significant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2012 NAC register.

bq2012 Registers

The bq2012 command and status registers are listed in Table 6 and described in the following sections.

Table 5. Current-Sensing Error as a Function of V_{SR}

Symbol	Parameter	Typical	Maximum	Units	Notes
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

Table 6. bq2012 Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	Command register	00h	Write	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
FLGS1	Primary status flags register	01h	Read	CHGS	BRP	BRM	CI	VDQ	$\overline{CHG}$	EDV1	EDVF
TMPGG	Temperature and gas gauge register	02h	Read	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available charge high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	Nominal available charge low byte register	17h	Read	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	Read	CR	DR2	DR1	DR0	n/u	n/u	n/u	OVLD
PPD	Program pin pull-down register	07h	Read	n/u	n/u	PPD6	PPD5	PPD4	PPD3	PPD2	PPD1
PPU	Program pin pull-up register	08h	Read	n/u	n/u	PPU6	PPU5	PPU4	PPU3	PPU2	PPU1
CPI	Capacity inaccurate count register	09h	Read	CPI7	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	CPI0
DMF	Digital magnitude filter register	0ah	R/W	DMF7	DMF6	DMF5	DMF4	DMF3	DMF2	DMF1	DMF0
RST	Reset register	39h	Write	RST	0	0	0	0	0	0	0

Note: n/u = not used

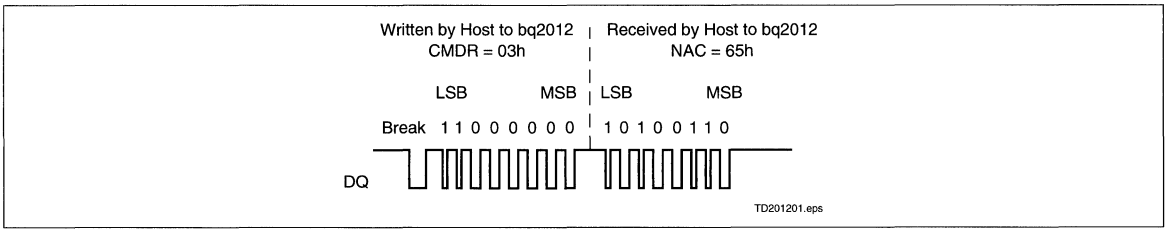


Figure 3. Typical Communication With the bq2012

Command Register (CMDR)

The write-only CMDR register is accessed when eight valid command bits have been received by the bq2012. The CMDR register contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function.

The W/$\overline{R}$ values are:

CMDR Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is:

0 The bq2012 outputs the requested register contents specified by the address portion of CMDR.

1 The following eight bits should be written to the register specified by the address portion of CMDR.

The lower seven-bit field of CMDR contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

CMDR Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Primary Status Flags Register (FLGS1)

The read-only FLGS1 register (address=01h) contains the primary bq2012 flags.

The ***charge status*** flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when $V_{SRO} > V_{SRQ}$. A V_{SRO} of less than V_{SRQ} or discharge activity clears CHGS.

The CHGS values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
CHGS	-	-	-	-	-	-	-

Where CHGS is:

0 Either discharge activity detected or $V_{SRO} < V_{SRQ}$

1 $V_{SRO} > V_{SRQ}$

The ***battery replaced*** flag (BRP) is asserted whenever the potential on the SB pin (relative to V_{SS}), V_{SB}, falls from above the maximum cell voltage, MCV (2.25V), or rises above 0.1V. The BRP flag is also set when the bq2012 is reset (see the RST register description). BRP is reset when either a valid charge action increments NAC to be equal to LMD, or a valid charge action is detected after the EDV1 flag is asserted. BRP = 1 signifies that the device has been reset.

The BRP values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	BRP	-	-	-	-	-	-

Where BRP is:

0 Battery is charged until NAC = LMD or discharged until the EDV1 flag is asserted

1 V_{SB} dropping from above MCV, V_{SB} rising from below 0.1V, or a serial port initiated reset has occurred

The ***battery removed*** flag (BRM) is asserted whenever the potential on the SB pin (relative to V_{SS}) rises above MCV or falls below 0.1V. The BRM flag is asserted until the condition causing BRM is removed.

The BRM values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	BRM	-	-	-	-	-

Where BRM is:

0 $0.1V < V_{SB} < 2.25V$

1 $0.1\ V > V_{SB}$ or $V_{SB} > 2.25V$

The ***capacity inaccurate*** flag (CI) is used to warn the user that the battery has been charged a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2012 is reset. The flag is cleared after an LMD update.

The CI values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	CI	-	-	-	-

Where CI is:

0 When LMD is updated with a valid full discharge

1 After the 64th valid charge action with no LMD updates

The ***valid discharge*** flag (VDQ) is asserted when the bq2012 is discharged from NAC = LMD. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- The self-discharge count register (SDCR) has exceeded the maximum acceptable value (4096 counts) for an LMD update.
- A valid charge action sustained at $V_{SRO} > V_{SRQ}$ for at least 256 NAC counts.
- The EDV1 flag was set at a temperature below 0°C

The VDQ values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

Where VDQ is:

0 SDCR ≥ 4096, subsequent valid charge action detected, or EDV1 is asserted with the temperature less than 0°C

1 On first discharge after NAC = LMD

The ***charge control*** flag, $\overline{CHG}$, is asserted whenever the $\overline{CHG}$ pin is asserted (see the charge control section on page 7 for a description of the $\overline{CHG}$ pin function).

The $\overline{CHG}$ values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	$\overline{CHG}$	-	-

Where $\overline{CHG}$ is:

0 When the $\overline{CHG}$ pin is asserted active low, signifying that the bq2012 is in a state to allow charge activity.

1 When the $\overline{CHG}$ pin is high-impedance, signifying that no charge activity should take place.

The ***first end-of-discharge warning*** flag (EDV1) warns the user that the battery is almost empty. The first segment pin, SEG_1, is modulated at a 4Hz rate if the display is enabled once EDV1 is asserted, which should warn the user that loss of battery power is imminent. The EDV1 flag is latched until a valid charge has been detected.

The EDV1 values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV1	-

Where EDV1 is:

0 Valid charge action detected, $V_{SB} \geq 1.05V$

1 $V_{SB} < 1.05V$ providing that OVLD=0 (see FLGS2 register description)

The ***final end-of-discharge warning*** flag (EDVF) flag is used to warn that battery power is at a failure condition. All segment drivers are turned off. The EDVF flag is latched until a valid charge has been detected. The EMPTY pin is also forced to a high-impedance state on assertion of EDV1. The host system may pull EMPTY high, which may be used to disable circuitry to prevent deep-discharge of the battery.

The EDVF values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	EDVF

Where EDVF is:

0 Valid charge action detected, $V_{SB} \geq 0.95V$

1 $V_{SB} < 0.95V$ providing that OVLD=0 (see FLGS2 register description)

Temperature and Gas Gauge Register (TMPGG)

The read-only TMPGG register (address=02h) contains two data fields. The first field contains the battery temperature. The second field contains the available charge from the battery.

TMPGG Temperature Bits							
7	6	5	4	3	2	1	0
TMP3	TMP2	TMP1	TMP0	-	-	-	

The bq2012 contains an internal temperature sensor. The temperature is used to set charge and discharge efficiency factors as well as to adjust the self-discharge coefficient.

The temperature register contents may be translated as shown in Table 7.

The bq2012 calculates the available charge as a function of NAC, temperature, and a full reference, either LMD or PFC. The results of the calculation are available via the display port or the gas gauge field of the TMPGG register. The register is used to give available capacity in $1/16$ increments from 0 to $15/16$.

TMPGG Gas Gauge Bits							
7	6	5	4	3	2	1	0
-	-	-	-	GG3	GG2	GG1	GG0

The gas gauge display and the gas gauge portion of the TMPGG register are adjusted for cold temperature dependencies. A piece-wise correction is performed as follows:

Temperature	Available Capacity Calculation
> 0°C	NAC / "Full Reference"
-20°C < T < 0°C	0.75 * NAC / "Full Reference"
< -20°C	0.5 * NAC / "Full Reference"

Table 7. Temperature Register Translation

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

The adjustment between > 0°C and -20°C < T < 0°C has a 10°C hysteresis.

Nominal Available Charge Registers (NACH/NACL)

The read/write NACH high-byte register (address=03h) and the read-only NACL low-byte register (address=17h) are the main gas gauging register for the bq2012. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC.

On reset, if $PROG_6$ = Z or low, NACH and NACL are cleared to 0; if $PROG_6$ = high, NACH = PFC and NACL = 0. When the bq2012 detects a valid EDV1, NACH and NACL are reset to 0. *Writing to the NAC registers affects the available charge counts and, therefore, affects the bq2012 gas gauge operation. Do not write the NAC registers to a value greater than LMD.*

Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V_{CC} is greater than 2V. The contents of BATID have no effect on the operation of the bq2012. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2012 uses as a measured full reference. The bq2012 adjusts LMD based on the measured discharge capacity

of the battery from full to empty. In this way the bq2012 updates the capacity of the battery. LMD is set to PFC during a bq2012 reset.

Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2012 flags.

The ***charge rate*** flag (CR) is used to denote the fast charge regime. Fast charge is assumed whenever a charge action is initiated. The CR flag remains asserted if the charge rate does not fall below 2 counts/sec.

The CR values are:

FLGS2 Bits							
7	6	5	4	3	2	1	0
CR	-	-	-	-	-	-	-

Where CR is:

0 When charge rate falls below 2 counts/sec

1 When charge rate is above 2 counts/sec

The fast charge regime efficiency factors are used when CR = 1. When CR = 0, the trickle charge efficiency factors are used. The time to change CR varies due to the user-selectable count rates.

The ***discharge rate*** flags, DR2–0, are bits 6–4.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-	-	-	

They are used to determine the current discharge regime as follows:

DR2	DR1	DR0	V_{SR} (V)
0	0	0	V_{SR} > -150mV
0	0	1	V_{SR} < -150mV

The ***overload*** flag (OVLD) is asserted when a discharge overload is detected, V_{SR} < -250mV. OVLD remains asserted as long as the condition persists and is cleared when V_{SR} > -250mV. The overload condition is used to stop sampling of the battery terminal characteristics for end-of-discharge determination. Sampling is re-enabled 0.5 secs after the overload condition is removed.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OVLD

DR2–0 and OVLD are set based on the measurement of the voltage at the SR pin relative to V_{SS}. The rate at which this measurement is made varies with device activity.

Program Pin Pull-Down Register (PPD)

The read-only PPD register (address=07h) contains some of the programming pin information for the bq2012. The segment drivers, SEG_{1-6}, have a corresponding PPD register location, PPD_{1-6}. A given location is set if a pull-down resistor has been detected on its corresponding segment driver. For example, if SEG_1 and SEG_4 have pull-down resistors, the contents of PPD are xx001001.

Program Pin Pull-Up Register (PPU)

The read-only PPU register (address=08h) contains the rest of the programming pin information for the bq2012. The segment drivers, SEG_{1-6}, have a corresponding PPU register location, PPU_{1-6}. A given location is set if a pull-up resistor has been detected on its corresponding segment driver. For example, if SEG_3 and SEG_6 have pull-up resistors, the contents of PPU are xx100100.

PPD/PPU Bits							
8	7	6	5	4	3	2	1
-	-	PPU_6	PPU_5	PPU_4	PPU_3	PPU_2	PPU_1
-	-	PPD_6	PPD_5	PPD_4	PPD_3	PPD_2	PPD_1

Capacity Inaccurate Count Register (CPI)

The read-only CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2012 adapts to the changing capacity over time. A complete discharge from full (NAC=LMD) to empty (EDV1=1) is required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and the self-discharge counter is less than 4096 counts.

The CPI register is incremented every time a valid charge is detected if NAC < 0.94 * LMD. When NAC ≥ 0.94 * LMD, the CPI register increments on the first valid charge; CPI does not increment again for a valid charge until NAC is discharged below 0.94 * LMD. This prevents continuous trickle charging from incrementing CPI if self-discharge decrements NAC. The CPI register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. The CPI register is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

Digital Magnitude Filter (DMF)

The read-write DMF register (address = 0ah) provides the system with a means to change the default settings of the digital magnitude filter. By writing different values into this register, the limits of V_{SRD} and V_{SRQ} can be adjusted.

Note: Care should be taken when writing to this register. A V_{SRD} and V_{SRQ} below the specified V_{OS} may adversely affect the accuracy of the bq2012. Refer to Table 4 for recommended settings for the DMF register.

Reset Register (RST)

The reset register (address=39h) provides the means to perform a software-controlled reset of the device. By writing the RST register contents from 00h to 80h, a bq2012 reset is performed. *Setting any bit other than the most-significant bit of the RST register is* ***not allowed****, and results in improper operation of the bq2012.*

Resetting the bq2012 sets the following:

- LMD = PFC
- CPI, VDQ, NACH, and NACL = 0
- CI and BRP = 1

Note: NACH = PFC when $PROG_6$ = H.

Display

The bq2012 can directly display capacity information using low-power LEDs. If LEDs are used, the program pins should be resistively tied to V_{CC} or V_{SS} for a program high or program low, respectively.

The bq2012 displays the battery charge state in either absolute or relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD. The sixth segment is not used.

In absolute mode, each segment represents a fixed amount of charge, based on the initial PFC. In absolute mode, each segment represents 20% of the PFC, with the sixth segment representing "overfull" (charge above the PFC). As the battery wears out over time, it is possible for the LMD to be below the initial PFC. In this case, all of the LEDs may not turn on, representing the reduction in the actual battery capacity.

The capacity display is also adjusted for the present battery temperature. The temperature adjustment reflects the available capacity at a given temperature but does not affect the NAC register. The temperature adjustments are detailed in the TMPGG register description.

When $\overline{DISP}$ is tied to V_{CC}, the SEG_{1-6} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active whenever the NAC registers are counting at a rate equivalent to V_{SRO} < -4mV or V_{SRO} > V_{SRQ}. When pulled low, the segment outputs become active immediately. A capacitor tied to $\overline{DISP}$ allows the display to remain active for a short period of time after activation by a push-button switch.

The segment outputs are modulated as two banks of three, with segments 1, 3, and 5 alternating with segments 2, 4, and 6. The segment outputs are modulated at approximately 100Hz with each segment bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV1} (EDV1 = 1), indicating a low-battery condition. V_{SB} below V_{EDVF} (EDVF = 1) disables the display output.

Microregulator

The bq2012 can operate directly from three or four cells. To facilitate the power supply requirements of the bq2012, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2012 can be inexpensively built using the FET and an external resistor; see Figure 1.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	7.0	V	
All other pins	Relative to V_{SS}	-0.3	7.0	V	
REF	Relative to V_{SS}	-0.3	8.5	V	Current limited by R1 (see Figure 1)
V_{SR}	Relative to V_{SS}	-0.3	7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2012 application note for details).
T_{OPR}	Operating temperature	0	70	°C	Commercial
		-40	85	°C	Industrial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	0.93	0.95	0.97	V	SB
V_{EDV1}	First empty warning	1.03	1.05	1.07	V	SB
V_{SR1}	Discharge compensation threshold	-120	-150	-180	mV	SR, $V_{SR} + V_{OS}$ (see note 2)
V_{ORD}	Overload threshold	-230	-250	-280	mV	SR, $V_{SR} + V_{OS}$
V_{SRO}	SR sense range	-300	-	+2000	mV	SR, $V_{SR} + V_{OS}$
V_{SRQ}	Valid charge	375	-	-	µV	$V_{SR} + V_{OS}$ (see note 1)
V_{SRD}	Valid discharge	-	-	-300	µV	$V_{SR} + V_{OS}$ (see note 1)
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	SB
V_{BR}	Battery removed/replaced	-	0.1	0.25	V	SB pulled low
		2.20	2.25	2.30	V	SB pulled high

Notes:
1. Default value; value set in DMF register. V_{OS} is affected by PC board layout. Proper layout guidelines should be followed for optimal performance. See "LayoutConsiderations."
2. Proper threshold measurements require V_{CC} to be more than 1.5V greater than the desired signal value.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{OS}	Offset referred to V_{SR}	-	±50	±150	µV	$\overline{DISP} = V_{CC}$
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	$I_{REF} = 5\mu A$
	Reference at -40°C to +85°C	4.5	-	7.5	V	$I_{REF} = 5\mu A$
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	$V_{REF} = 3V$
I_{CC}	Normal operation	-	90	135	µA	$V_{CC} = 3.0V$
		-	120	180	µA	$V_{CC} = 4.25V$
		-	170	250	µA	$V_{CC} = 6.5V$
V_{SB}	Battery input	-	-	2.4	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	$0 < V_{SB} < V_{CC}$
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	$V_{DISP} = V_{SS}$
I_{LCOM}	LCOM input leakage	-0.2	-	0.2	µA	$\overline{DISP} = V_{CC}$
R_{DQ}	Internal pulldown	500	-	-	KΩ	
V_{SR}	Sense resistor input	-0.3	-	2.0	V	$V_{SR} < V_{SS}$ = discharge; $V_{SR} > V_{SS}$ = charge
R_{SR}	SR input impedance	10	-	-	MΩ	$-200mV < V_{SR} < V_{CC}$
V_{IH}	Logic input high	V_{CC} - 0.2	-	-	V	$PROG_1$–$PROG_6$
V_{IL}	Logic input low	-	-	V_{SS} + 0.2	V	$PROG_1$–$PROG_6$
V_{IZ}	Logic input Z	float	-	float	V	$PROG_1$–$PROG_6$
V_{OLSL}	SEG_X output low, low V_{CC}	-	0.1	-	V	$V_{CC} = 3V$, $I_{OLS} \leq 1.75mA$ SEG_1–SEG_6
V_{OLSH}	SEG_X output low, high V_{CC}	-	0.4	-	V	$V_{CC} = 6.5V$, $I_{OLS} \leq 11.0mA$ SEG_1–SEG_6
V_{OHLCL}	LCOM output high, low V_{CC}	V_{CC} - 0.3	-	-	V	$V_{CC} = 3V$, $I_{OHLCOM} = -5.25mA$
V_{OHLCH}	LCOM output high, high V_{CC}	V_{CC} - 0.6	-	-	V	$V_{CC} = 6.5V$, $I_{OHLCOM} = -33.0mA$
I_{IH}	$PROG_{1-6}$ input high current	-	1.2	-	µA	$V_{PROG} = V_{CC}/2$
I_{IL}	$PROG_{1-6}$ input low current	-	1.2	-	µA	$V_{PROG} = V_{CC}/2$
I_{OHLCOM}	LCOM source current	-33	-	-	mA	At $V_{OHLCH} = V_{CC}$ - 0.6V
I_{OLS}	SEG_X sink current	-	-	11.0	mA	At $V_{OLSH} = 0.4V$
I_{OL}	Open-drain sink current	-	-	5.0	mA	At $V_{OL} = V_{SS} + 0.3V$ DQ, EMPTY, $\overline{CHG}$
V_{OL}	Open-drain output low	-	-	0.5	V	$I_{OL} \leq 5mA$, DQ, EMPTY
V_{IHDQ}	DQ input high	2.5	-	-	V	DQ
V_{ILDQ}	DQ input low	-	-	0.8	V	DQ
R_{PROG}	Soft pull-up or pull-down resistor value (for programming)	-	-	200	KΩ	$PROG_1$–$PROG_6$
R_{FLOAT}	Float state external impedance	-	5	-	MΩ	$PROG_1$–$PROG_6$

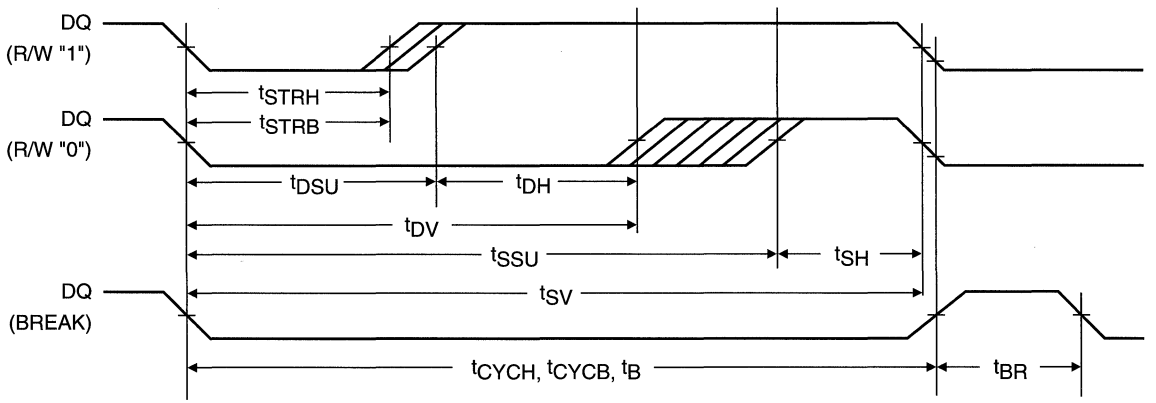
Note: All voltages relative to V_{SS}.

Serial Communication Timing Specification

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2012	3	-	-	ms	See note
t_{CYCB}	Cycle time, bq2012 to host	3	-	6	ms	
t_{STRH}	Start hold, host to bq2012	5	-	-	ns	
t_{STRB}	Start hold, bq2012 to host	500	-	-	µs	
t_{DSU}	Data setup	-	-	750	µs	
t_{DH}	Data hold	750	-	-	µs	
t_{DV}	Data valid	1.50	-	-	ms	
t_{SSU}	Stop setup	-	-	2.25	ms	
t_{SH}	Stop hold	700	-	-	µs	
t_{SV}	Stop valid	2.95	-	-	ms	
t_B	Break	3	-	-	ms	
t_{BR}	Break recovery	1	-	-	ms	

Note: The open-drain DQ pin should be pulled to at least V_{CC} by the host system for proper DQ operation. DQ may be left floating if the serial interface is not used.

Serial Communication Timing Illustration



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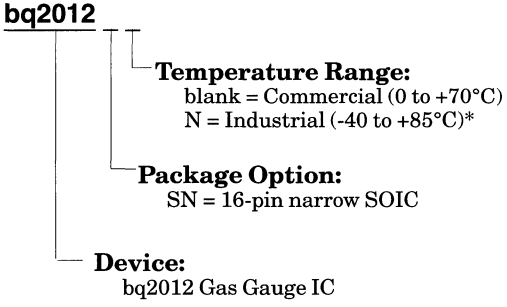
Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	7	Addition to Table 2	Added bottom row

Note: Change 1 = Sept. 1996 B changes from July 1994.

Ordering Information



* Contact factory for availability.

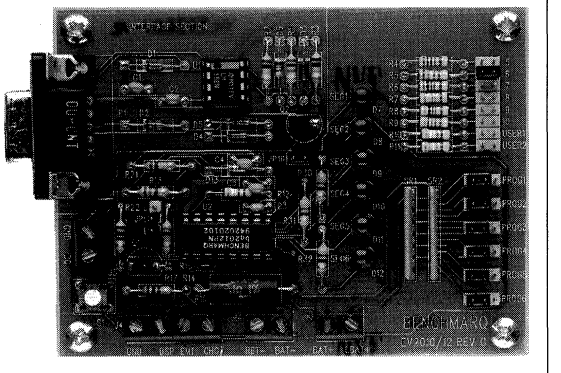
UNITRODE

Product Brief **EV2012**

bq2012 Evaluation System

Features

- bq2012 Gas Gauge IC evaluation and development system
- PC interface hardware for easy access to state-of-charge information via the serial port
- Alternative terminal block for direct connection to the serial port
- Battery state-of-charge monitoring for 5- to 10-cell (series) applications (2 user-selectable options for 3, 4, or greater than 10 cells)
- On-board regulator for greater than 4-cell applications
- State-of-charge information displayed on bank of 6 LEDs
- Nominal capacity jumper-configurable
- Cell chemistry jumper-configurable
- Display mode jumper-configurable



General Description

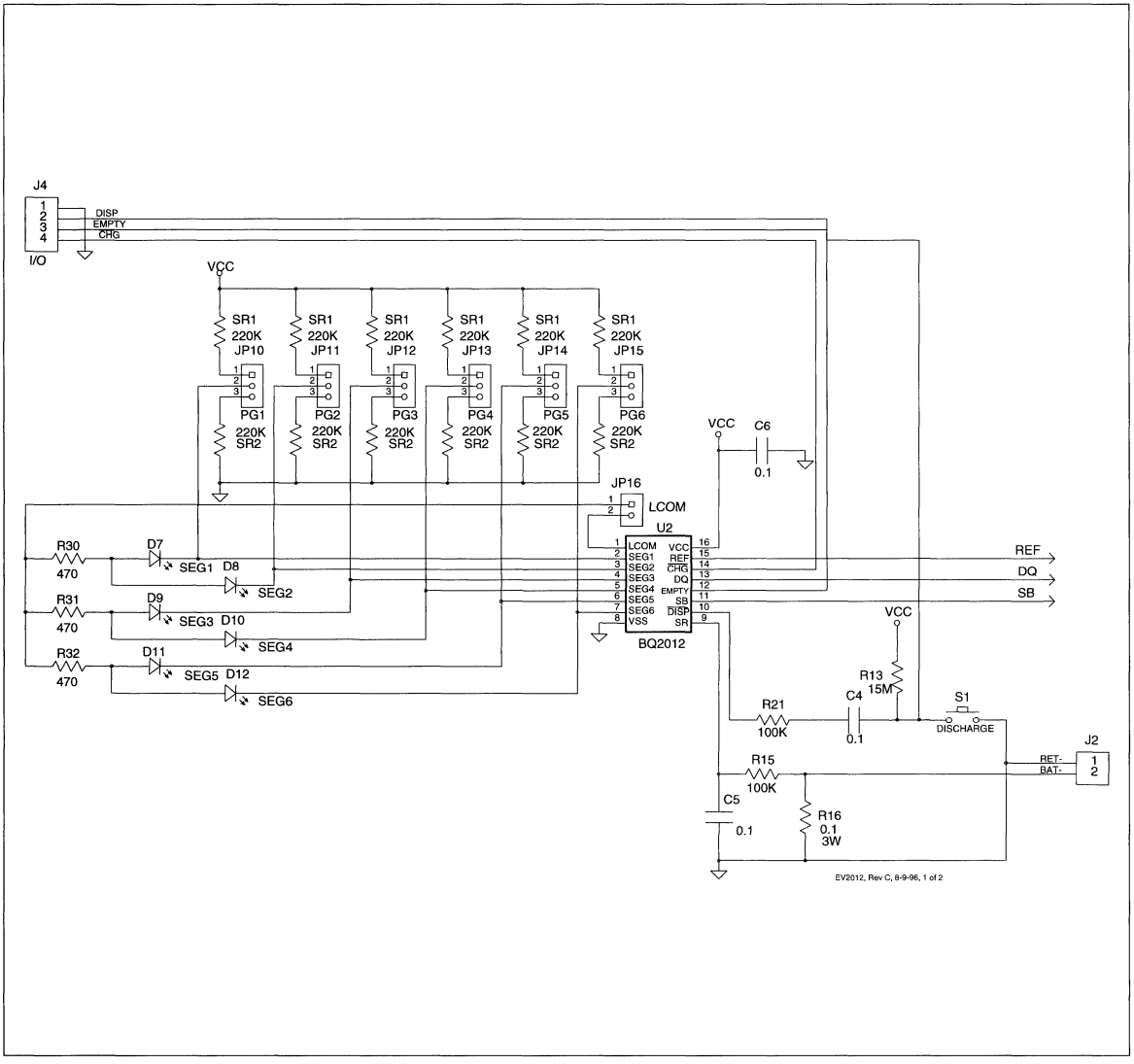
The EV2012 Evaluation System provides a development and evaluation environment for the bq2012 Gas Gauge IC. The EV2012 incorporates a bq2012, a sense resistor, and all other hardware necessary to provide a capacity monitoring function for 3 to 12 series NiCd or NiMH cells.

Hardware for a PC interface is included on the EV2012 so that easy access to the state-of-charge information can be achieved via the serial port of the bq2012. Direct connection to the serial port of the bq2012 is also made available for check-out of the final hardware/software implementation.

The menu-driven software provided with the EV2012 displays charge/discharge activity and allows user interface to the bq2012 from any standard DOS PC.

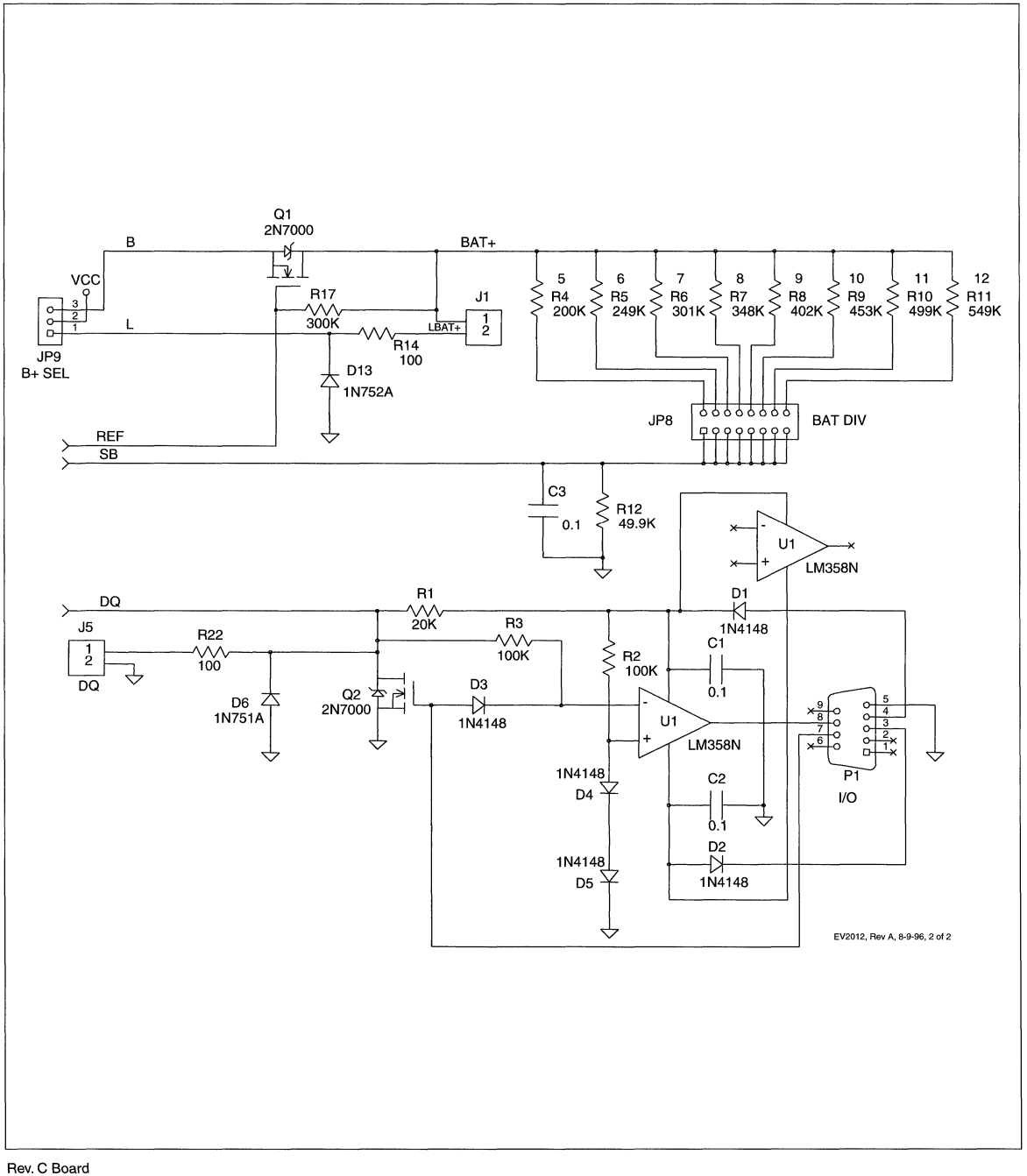
A full data sheet for this product is available on the Unitrode web site, or you may contact the factory for one.

EV2012 Board Schematic



Rev. C Board

EV2012 Board Schematic (Continued)



Rev. C Board

UNITRODE

bq2013H

Gas Gauge IC for Power-Assist Applications

Features

- Accurate measurement of available charge in rechargeable batteries
- Designed for electric assist bicycles and other applications
- Measures a wide dynamic current range
- Supports NiCd, NiMH or lead acid
- Designed for battery pack integration
  - 120µA typical standby current (self-discharge estimation mode)
  - Small size enables implementations in as little as ½ square inch of PCB
- Direct drive of LEDs for capacity display
- Automatic charge and self-discharge compensation using internal temperature sensor
- Simple single-wire serial communications port for subassembly testing
- 16-pin narrow SOIC

General Description

The bq2013H Gas Gauge IC is intended for battery-pack installation to maintain an accurate record of a battery's available charge. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery. The bq2013H is designed for high cpaacity battery packs used in high-discharge rate systems.

Battery self-discharge is estimated based on an internal timer and temperature sensor. Compensations for battery temperature, rate of charge, and self-discharge are applied to the charge counter to provide available capacity information across a wide range of operating conditions. Initial battery capacity, self-discharge rate, display mode, and charge compensation are set using the $PROG_{1-6}$ pins. Actual battery capacity is automatically "learned" in the course of a discharge cycle from full to empty.

Nominal available charge may be directly indicated using a five-segment LED display. These segments are used to graphically indicate nominal available charge.

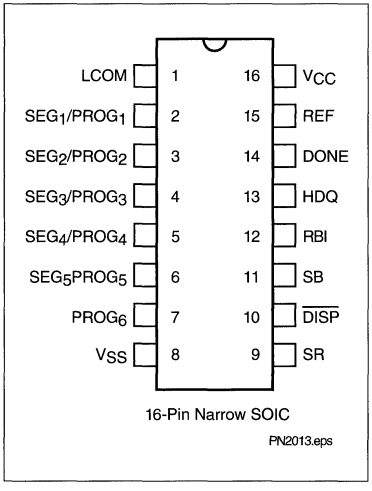
The bq2013H supports a simple single-line bi-directional serial link to an external processor (common ground). The bq2013H outputs battery information in response to external commands over the serial link. To support battery pack testing, the outputs may also be controlled by command. The external processor may also overwrite some of the bq2013H gas gauge data registers.

The bq2013H may operate directly from four nickel cells or three lead acid. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide V_{CC} from a greater number of cells.

Internal registers include available charge, temperature, capacity, battery ID, and battery status.

4

Pin Connections



16-Pin Narrow SOIC

PN2013.eps

Pin Names

LCOM	LED common output	REF	Voltage reference output
$SEG_1/PROG_1$	LED segment 1/ Program 1 input	DONE	Fast charge complete input
$SEG_2/PROG_2$	LED segment 2 / Program 2 input	HDQ	Serial communications input/output
$SEG_3/PROG_3$	LED segment 3/ Program 3 input	RBI	Register backup input
		SB	Battery sense input
$SEG_4/PROG_4$	LED segment 4/ Program 4 input	$\overline{DISP}$	Display control input
$SEG_5/PROG_5$	LED segment 5/ Program 5 input	SR	Sense resistor input
		V_{CC}	Supply voltage
$PROG_6$	Program 6 input		

Pin Descriptions

LCOM **LED common**

This open-drain output switches V_{CC} to source current for the LEDs. The switch is off during initialization to allow reading of $PROG_{1-5}$ pull-up or pull-down program resistors. LCOM is also high impedance when the display is off.

SEG_1–SEG_5 **LED display segment outputs (dual function with $PROG_1$–$PROG_5$**

Each output may activate an LED to sink the current sourced from LCOM.

$PROG_1$–$PROG_6$ **Programmed full count selection inputs (dual function with SEG_1 - SEG_5)**

These three-level input pins define the programmed full-count (PFC), display mode, self-discharge rate, offset compensation, overload threshold, and charge compensation.

SR **Sense resistor input**

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret charge and discharge activity. The SR input (see Figure 1) is connected between the negative terminal of the battery and ground. $V_{SR} > V_{SS}$ indicates charge, and $V_{SR} < V_{SS}$ indicates discharge. The effective voltage drop, V_{SRO}, as seen by the bq2013H is $V_{SR} + V_{OS}$.

DONE **Charge complete input**

This input/output is used to communicate the status of an external charge controller to the bq2013H.

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ pulled high disables the display. $\overline{DISP}$ floating allows the LED display to be active during certain charge and discharge conditions. Transitioning $\overline{DISP}$ low activates the display.

SB **Secondary battery input**

This input monitors the scaled battery voltage through a high-impedance resistive divider network for the end-of-discharge voltage (EDV) thresholds.

RBI **Register backup input**

This input is used to provide backup potential to the bq2013H registers during periods when $V_{CC} < 3V$. A storage capacitor can be connected to RBI.

HDQ **Serial I/O pin**

This is an open-drain bidirectional communications port.

REF **Voltage reference output for regulator**

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} **Supply voltage input**

V_{SS} **Ground**

Functional Description

General Operation

The bq2013H determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2013H measures discharge and charge currents, estimates self-discharge, monitors the battery for low-battery voltage thresholds, and compensates for temperature and charge rates. The charge measurement is made by monitoring the voltage across a small-value series sense resistor between the battery's negative terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2013H using the LED display. The bq2013H can be configured to display capacity in either a relative or an absolute display mode. The relative display mode uses the last measured discharge capacity of the battery as the battery "full" reference. The absolute display mode uses the programmed full count (PFC) as the full reference, forcing each segment of the display to represent a fixed amount of charge. A push-button display feature is available for enabling the LED display.

The bq2013H monitors the charge and discharge currents as a voltage across a sense resistor (see R_S in Figure 1). A filter between the negative battery terminal and the SR pin is required.

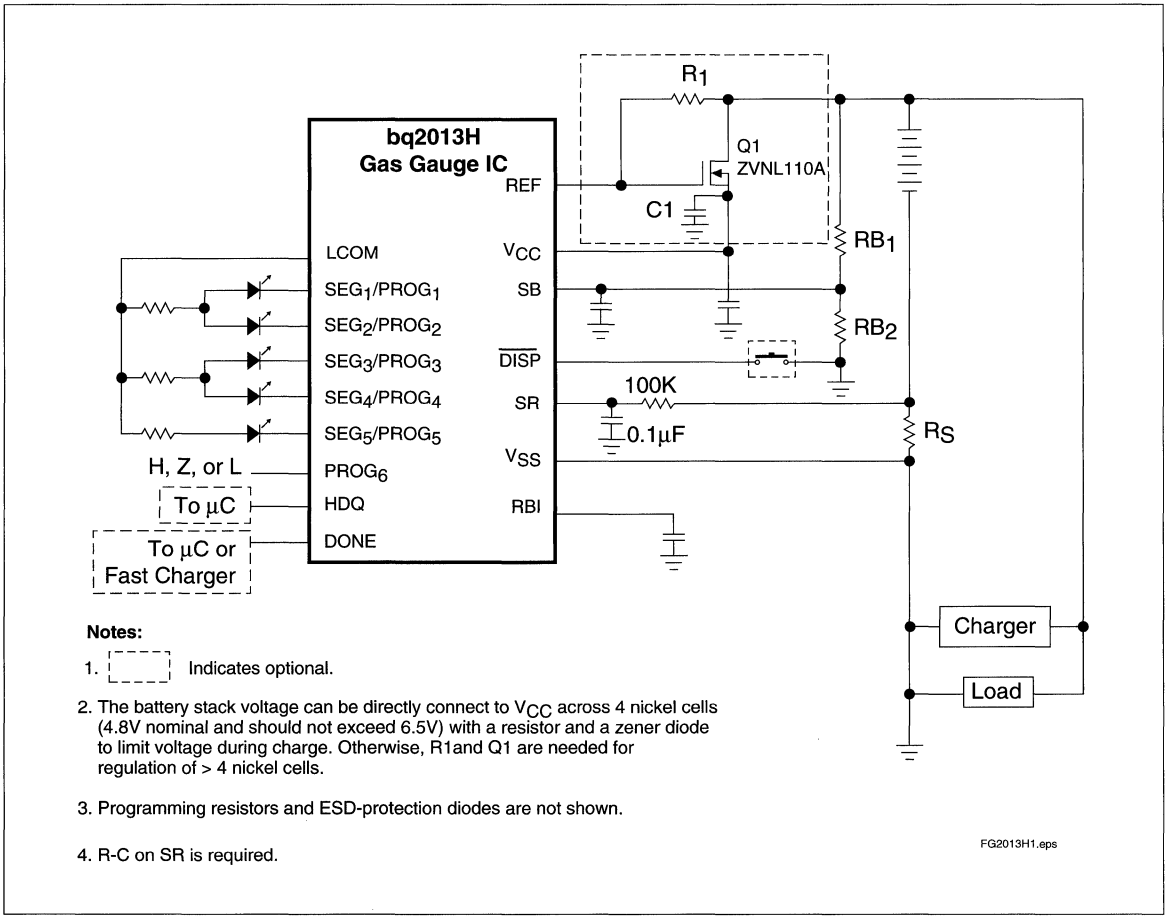


Figure 1. Application Diagram: LED Display

3/20

Register Backup

The bq2013H RBI input pin is intended to be used with a storage capacitor to provide backup potential to the internal bq2013H registers when V_{CC} momentarily drops below 3.0V. V_{CC} is output on RBI when V_{CC} is above 3.0V.

After V_{CC} rises above 3.0V, the bq2013H checks the internal registers for data loss or corruption. If data has changed, then the NAC register is cleared, and the LMD register is loaded with the initial PFC.

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2013H monitors the battery potential through the SB pin for the end-of-discharge voltage (EDV) thresholds.

The EDV threshold levels are used to determine when the battery has reached an "empty" state.

The EDV thresholds for the bq2013H are set as follows:

EDV1 (first) = 1.00V

EDVF (final) = EDV1 - 100mV

The battery voltage divider (RB1 and RB2 in Figure 1) is used to scale these values to the desired threshold.

If VSB is below either of the two EDV thresholds for the specified delay times in Table 1, the associated flag is latched and remains latched, independent of VSB, until the next valid charge. EDV monitoring is disabled if the OVLD bit in FLGS2 is set.

Table 1. Delay Time in Seconds

Capacity	Temperature		
	< 10°C	10°C to 30°C	> 30°C
> 40%	7	6	5
20% to 40%	4	3	2
< 20%	2	2	2

Reset

The bq2013H can be reset by removing V_{CC} and grounding the RBI pin for 15 seconds or with a command over the serial port. The serial port reset command sequence requires writing 00h to register PPFC (address = leh) and the writing 00h to register LMD (address = 05h.)

Temperature

The bq2013H internally determines the temperature in 10°C steps centered from -35°C to +85°C. The temperature steps are used to adapt charge rate compensations and self-discharge counting. The temperature range is available over the serial port in 10°C increments as shown in the following table:

TMPGG (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2013H measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors should be placed as close as possible to the SB and V_{CC} pins and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor (R_S) should be as close as possible to the bq2013H.
- The R-C on the SR pin should be located as close as possible to the SR pin. The maximum R should not exceed 100K.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2013H. The bq2013H accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. The bq2013H compensates charge current for charge rate and tem-

perature. Discharge current is load compensated based on the value stored in location LCOMP (address = 0eh). LCOMP allows the bq2013H to automatically adjust for continuous small discharge currents. The bq2013H compensates self discharge for the load value as well as temperature.

The main counter, Nominal Available Capacity (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging, self-discharge decrement the NAC register and increment the DCR (Discharge Count Register). NAC is also corrected automatically for offset error based on the value in the offset location OFFSET (address = 0bh.)

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2013H adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the Programmed Full Count (PFC) shown in Table 2. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. **Last Measured Discharge (LMD) or learned battery capacity:**

   LMD is the last measured discharge capacity of the battery. On initialization (application of V_{CC} or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register (DCR) representing a discharge from full to below EDV. The maximum decrease in LMD because of a DCR update is 25% of LMD. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

2. **Programmed Full Count (PFC) or initial battery capacity:**

   The initial LMD and gas gauge rate values are programmed by using PFC. The PFC also provides the 100% reference for the absolute display mode. The bq2013H is configured for a given application by selecting a PFC value from Table 2. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

   Battery capacity (mAh) * sense resistor (Ω) =

   PFC (mVh)

   Selecting a PFC slightly less than the rated capacity for absolute mode provides capacity above the full reference for much of the battery's life.

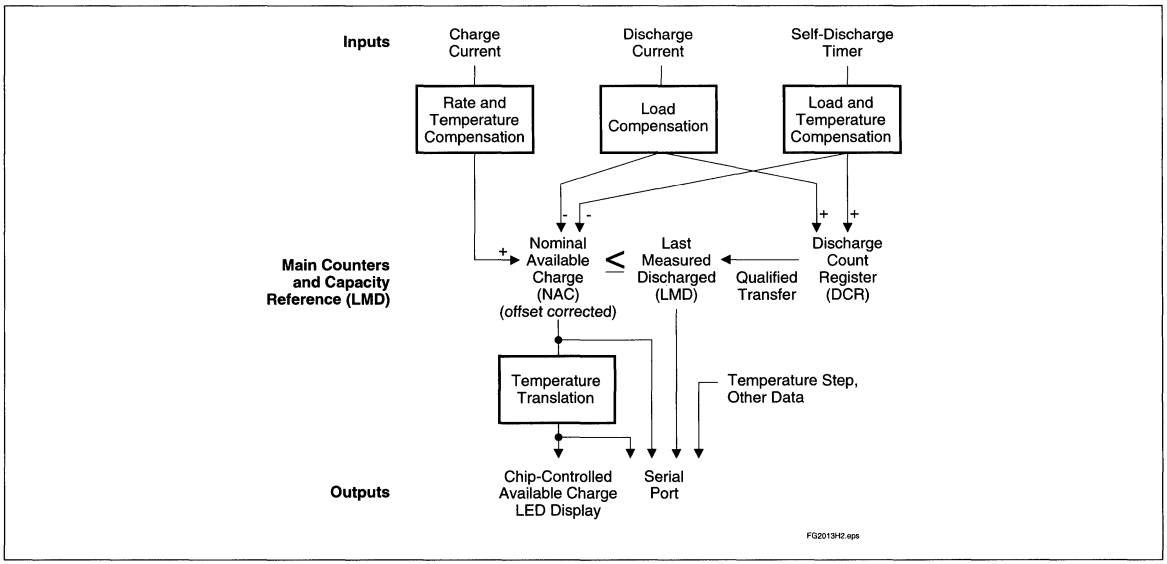


Figure 2. Operational Overview

5/20

Example: Selecting a PFC Value

Given:

Sense resistor = 0.0075Ω
Number of cells = 14
Capacity = 5000mAh, NiCd cells
Current range = 1A to 30A
Relative display mode with 4 second timer
Self-discharge = 1% per day
Trickle charge compensation = 0.85
Typical offset = -75µV
Voltage drop across sense resistor = 5mV to 150mV

Therefore:

$$5000mAh * 0.0075\Omega = 37.5mVh$$

Select:

PFC = 448000 counts or 35mVh
$PROG_1$, $PROG_2$ = Z, L
$PROG_3$ = Z
$PROG_4$ = H
$PROG_5$ = L
$PROG_6$ = Z

Table 2. bq2013H Programmed Full Count mVh Selections

Programmed Full Count (PFC)	mVh	Scale	$PROG_1$	$PROG_2$
27136	84.8	1/320	H	H
24064	75.2	1/320	H	Z
41472	64.8	1/640	H	L
35072	54.8	1/640	Z	H
28672	44.8	1/640	Z	Z
44800	35	1/1280	Z	L
30720	24	1/1280	L	H
38400	15	1/2560	L	Z
12800	5	1/2560	L	L

Table 3. Programmed Self-Discharge

$PROG_3$	Self-Discharge
H	1.6% per day
Z	0.8% per day
L	0.2% per day

Table 4. Programmed Display Mode

$PROG_4$	Overload Threshold	Display Mode
H	V_{OVLD} = -75mV	Relative/4s timer after push-button release
Z	V_{OVLD} = -75mV	Relative/4s timer after push-button release
L	V_{OVLD} = -25mV	Absolute/4s timer after push-button release

Table 5. Programmed Charge Compensation

$PROG_5$	Trickle			Fast		
	<30°C	30°C—50°C	>50°C	<30°C	30°C—50°C	>50°C
H	0.80	0.75	0.70	0.95	0.90	0.85
Z	1.00	1.00	1.00	1.00	1.00	1.00
L	0.85	0.80	0.75	0.95	0.90	0.85

Table 6. Programmed Discharge Offset Adjustment

$PROG_6$	Offset
H	-150µV
Z	-75µV
L	0µV

The initial full battery capacity is 35mVh (4667mAh) until the bq2013H "learns" a new capacity with a qualified discharge from full to EDV1.

3. **Nominal Available Capacity (NAC):**

   NAC counts up during charge to a maximum value of LMD and down during discharge and self discharge to 0. NAC is reset to 0 on initialization and on the first valid charge following discharge to EDV1. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = LMD. When the DONE input is asserted high, indicating full charge completion, NAC is set to LMD.

4. **Discharge Count Register (DCR):**

   The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC = LMD. The DCR does not roll over but stops counting when it reaches FFFFh.

   The DCR value becomes the new LMD value on the first charge after a valid discharge to EDV1 if all of the following conditions are met:

   - No valid charge initiations (charges greater than 2 NAC updates) occurred during the period between NAC = LMD and EDV1.
   - The self-discharge count is less than 6% of NAC.
   - The temperature is ≥ 0°C when the EDV1 level is reached during discharge.
   - VDQ is set.

Charge Counting

Charge activity is detected based on a positive voltage on the V_{SR} input. If charge activity is detected, the bq2013H increments NAC at a rate proportional to V_{SRO} (V_{SR} + V_{OS}) and, if enabled, activates an LED display if V_{SRO} > 500µV. Charge actions increment the NAC after compensation for charge rate and temperature.

The bq2013H detects charge activity with V_{SRO} > 250µV. A valid charge equates to a sustained charge activity greater than 2 NAC updates. Once a valid charge is detected, charge counting continues until V_{SRO} drops below 250µV.

Discharge Counting

All discharge counts where V_{SRO} < -250µV cause the NAC register to decrement and the DCR to increment. If enabled, the display is activated when V_{SRO} < -2mV. The display remains active for 10 seconds after V_{SRO} rises above - 2mV.

Self-Discharge Estimation

The bq2013H decrements NAC and increments DCR for self-discharge based on time and temperature. The self-discharge count rate is programmed per Table 3. This is the rate for a battery temperature between 20–30°C. The NAC register cannot be decremented below 0.

Count Compensations

The bq2013H determines fast charge when the NAC updates at a rate of ≥ 2 counts/s. Charge activity is compensated for temperature and rate before updating NAC. Self-discharge estimation is compensated for temperature before updating NAC or DCR.

Charge Compensation

Charge efficiency factors are selected using Table 5 for trickle charge and fast charge. Fast charge is defined as a rate of charge resulting in ≥ 2 NAC counts/s (0.16C to 0.6C, depending on PFC selections; see Table 2).

Temperature adapts the charge rate compensation factors over three ranges between nominal, warm, and hot temperatures. Program pin 5 is used to select one of three compensation programs. These values are shown in Table 5.

Self-Discharge Compensation

The self-discharge compensation can be programmed for three different rates. The rates vary across 8 ranges from <10°C to >70°C, doubling with each higher temperature step (10°C). See Table 7.

Table 7. Self-Discharge Compensation

Temperature Range	Self-Discharge Compensation Typical Rate/Day		
	$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L
< 10°C	NAC/256	NAC/512	NAC/2048
10–20°C	NAC/128	NAC/256	NAC/1024
20–30°C	NAC/64	NAC/128	NAC/512
30–40°C	NAC/32	NAC/64	NAC/256
40–50°C	NAC/16	NAC/32	NAC/128
50–60°C	NAC/8	NAC/16	NAC/64
60–70°C	NAC/4	NAC/8	NAC/32
> 70°C	NAC/2	NAC/4	NAC/16

Offset Compensation

The bq2013H uses a voltage to frequency converter to measure the voltage across a resistor used to monitor the current into and out of the battery. This converter has an offset value that can be influenced by the V_{CC} supply and the bypassing of this supply. The typical value found on a well designed PCB is about -75µV. Program pin 6 can be used to compensate for this offset, reducing the effective V_{OS}. Offset compensation occurs when V_{SRO} < -250µV or V_{SRO} > 250µV.

Error Summary

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see the DCR description in the "Layout Considerations" section). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

DONE Input

A fast-charge controller IC or micro-controller uses the DONE input to communicate charge status to the bq2013H. When the DONE input is asserted high on fast-charge completion, the bq2013H sets NAC = LMD and VDQ = 1. The DONE input should be maintained high as long as the fast-charge controller or microcontroller keeps the batteries full; otherwise the pin should be held low.

Communicating With the bq2013

The bq2013H includes a simple single-pin (HDQ plus return) serial data interface. A host processor uses the interface to access various bq2013H registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain HDQ pin on the bq2013H should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2013H. The command directs the bq2013H to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte. (See Figure 3.)

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 5K bits/s. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2013H may be sampled using the pulse-width capture timers available on some microcontrollers.

If a communication error occurs, e.g., t_{CYCB} > 250µs, the bq2013H should be sent a BREAK to reinitiate the serial interface. A BREAK is detected when the HDQ pin is driven to a logic-low state for a time, t_B or greater. The HDQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2013H is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2013H taking the HDQ pin to a logic-low state for a period, $t_{STRH;B}$. The next section is the actual data transmission, where the data should be valid by a period, $t_{DSU;B}$, after the negative edge used to start communication. The data should be held for a period, $t_{DH;DV}$, to allow the host or bq2013H to sample the data bit.

The final section is used to stop the transmission by returning the HDQ pin to a logic-high state by at least a period, $t_{SSU;B}$, after the negative edge used to start communication. The final logic-high state should be until a period $t_{CYCH;B}$, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial com-

Table 8. bq2013H Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

munication timing specification and illustration sections.

Communication with the bq2013H is always performed with the least-significant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2013H NACH register.

bq2013H Command Code and Registers

The bq2013H status registers are listed in Table 9 and described below.

Command Code

The bq2013H latches the command code when eight valid command bits have been received by the bq2013H. The command code register contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command code is used to select whether the received command is for a read or a write function.

The W/$\overline{R}$ location is:

Command Code Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is:

0 The bq2013H outputs the requested register contents specified by the address portion of command code.

1 The following eight bits should be written to the register specified by the address portion of command code.

The lower seven-bit field of command code contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

Command Code Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

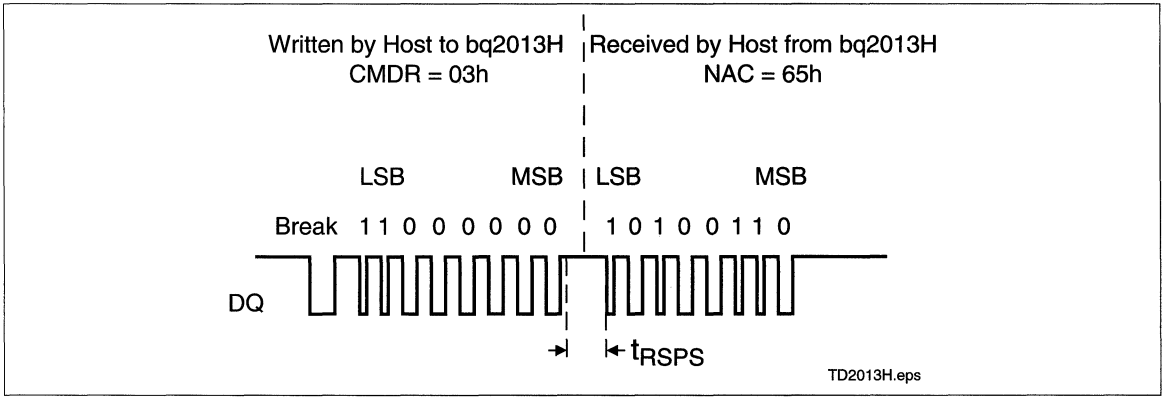


Figure 3. Typical Communication With the bq2013H

Table 9. bq2013H Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
FLGS1	Primary status flags register	01h	R	CHGS	BRP	RSVD	RSVD	VDQ	RSVD	EDV1	EDVF
TMPGG	Temperature and gas gauge register	02h	R	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available capacity high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	Nominal available capacity low byte register	17h	R/W	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	R	CR	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	OVLD
PPD	Program pull down register	07h	R	RSVD	RSVD	PPD6	PPD5	PPD4	PPD3	PPD2	PPD1
PPU	Program pull up register	08h	R	RSVD	RSVD	PPU6	PPU5	PPU4	PPU3	PPU2	PPU1
OCTL	Output control register	0ah	R/W	1	OC5	OC4	OC3	OC2	OC1	OCE	OCC
OFFSET	Offset adjustment regisiter	0bh	R/W	OFS7	OFS6	OFS5	OFS4	OFS3	OFS2	OFS1	OFS0
SDR	Self discharge rate	0ch	R/W	SDR7	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0
DMF	Digital magnitude filter	0dh	R/W	DMF7	DMF6	DMF5	DMF4	DMF3	DMF2	DMF1	DMF0
LCOMP	Load compensation	0eh	R/W	LC7	LC6	LC5	LC4	LC3	LC2	LC1	LC0
CCOMP	Fast charge compensation	0fh	R/W	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0
PPFC	Program pin data	leh	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
VSB	Battery voltage register	7eh	R	VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0

Notes: RSVD = reserved.
All other registers not documented are reserved.

Primary Status Flags Register (FLGS1)

The FLGS1 register (address=01h) contains the primary bq2013H flags.

The ***charge status*** flag (CHGS) is asserted when a valid charge rate is detected. The bq2013H deems the charge valid if it results in two NAC updates with V_{SRO} > 250µV. A V_{SRO} of less than 250µV or discharge activity clears CHGS.

The CHGS location is:

FLGS1 Bits							
7	6	5	4	3	2	1	0
CHGS	-	-	-	-	-	-	-

where CHGS is

0 Either discharge activity detected or V_{SRO} < 250µV

1 Two NAC updates with V_{SRO} > 250µV

The ***battery replaced*** flag (BRP) is asserted whenever the bq2013H is reset by application of V_{CC} or by a serial port command. BRP is reset when either a valid charge action increments NAC to be equal to LMD, or when a valid charge action is detected after the EDV1 flag is asserted. BRP = 1 signifies that the device has been reset.

The BRP location is:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	BRP	-	-	-	-	-	-

where BRP is

0 bq2013H is charged until NAC = LMD or on the first charge after or a discharge which sets the EDV1 flag

1 bq2013H is reset

The ***valid discharge*** flag (VDQ) is asserted when the bq2013H is discharged from NAC=LMD. The flag remains set until either LMD is updated or until one of three actions that can clear VDQ occurs:

- NAC has been reduced by more than 6% during because of self-discharge since VDQ was set
- A valid charge action sustained at V_{SRO} > V_{SRQ} for at least two NAC updates
- The EDV1 flag was set at a temperature below 0°C.

The VDQ location is:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

where VDQ is

0 Self-discharge reduces NAC by 6%, valid charge action detected, EDV1 asserted with the temperature less than 0°C, or reset

1 On first discharge after NAC = LMD

The first ***end-of-discharge warning*** flag (EDV1) warns the user that the battery is empty. SEG1 blinks at a 4Hz rate and DONE is asserted low. EDV1 detection is disabled if OVLD = 1. The EDV flag is latched until a valid charge has been detected.

The EDV1 location is:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV1	-

where EDV1 is

0 Valid charge action detected or $V_{SB} \geq V_{EDV1}$

1 $V_{SB} < V_{EDV1}$ for the delay time, provided that the OVLD bit is not set

The ***final end-of-discharge warning*** flag (EDVF) flag is used to warn that battery power is at a failure condition. All segment drivers are turned off. The EDVF flag is latched until a valid charge has been detected. The EDVF threshold is set 100mV below the EDV1 threshold.

The EDVF location is:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	EDVF

Where EDVF is:

0 Valid charge action detected or $V_{SB} \geq V_{EDVF}$

1 $V_{SB} < V_{EDVF}$, providing the OVLD bit is not set

Table 10. Temperature Register Contents

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

Temperature and Gas Gauge Register (TMPGG)

TMPGG Temperature Bits							
7	6	5	4	3	2	1	0
TMP3	TMP2	TMP1	TMP0	-	-	-	

The read-only TMPGG register (address=02h) contains two data fields. The first field contains the battery temperature. The second field contains the available charge from the battery.

The bq2013H contains an internal temperature sensor. The temperature is used to set charge efficiency factors as well as to adjust the self-discharge coefficient. The temperature register contents may be translated as shown in Table 10.

The bq2013H calculates the available charge as a function of NAC and a full reference, either LMD or PFC. The results of the calculation are available via the display port or the gas gauge field of the TMPGG register. The register is used to give available capacity in $\frac{1}{16}$ increments from 0 to $\frac{15}{16}$.

TMPGG Gas Gauge Bits							
7	6	5	4	3	2	1	0
-	-	-	-	GG3	GG2	GG1	GG0

Nominal Available Charge Register (NAC)

The NACH register (address=03h) and the NACL register (address=17h) are the main gas gauging registers for the bq2013H. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC. NACH and NACL are set to 0 during a bq2013H reset.

Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V_{RBI} is greater than 2V. The contents of BATID have no effect on the operation of the bq2013H. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2013H uses as a measured full reference. The bq2013H adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2013H updates the capacity of the battery. LMD is set to PFC during a bq2013H reset.

Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2013H flags.

The ***charge rate*** flag (CR) is used to denote the fast charge regime. Fast charge is assumed whenever a charge action is initiated. The CR flag remains asserted if the charge rate does not fall below 2 NAC counts/s.

The CR location is:

FLGS2 Bits							
7	6	5	4	3	2	1	0
CR	-	-	-	-	-	-	-

Where CR is:

0 When charge rate falls below 2 counts/sec

1 When charge rate is above 2 counts/sec

The fast charge regime efficiency factors are used when CR = 1. When CR = 0, the trickle charge efficiency fac-

tors are used. The time to change CR varies due to the user-selectable count rates.

The ***overload*** flag (OVLD) is asserted when a discharge overload is detected. PROG4 defines the overload threshold, as defined in Table 4. OVLD remains asserted as long as the condition is valid.

The OVLD location is:

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OVLD

Where OVLD is:

0 If $V_{SRO} > V_{OVLD}$

1 If $V_{SRO} < V_{OVLD}$

Program Pin Pull-Down Register (PPD)

The PPD register (address=07h) contains some of the programming pin information for the bq2013H. The program pins have a corresponding PPD bit location, PPD_{1-6}. A given location is set if a pull-down resistor has been detected on its corresponding segment driver. For example, if $PROG_1$ and $PROG_4$ have pull-down resistors, the contents of PPD are xx001001.

PPD/PPU Bits							
7	6	5	4	3	2	1	0
RSVD	RSVD	PPU_6	PPU_5	PPU_4	PPU_3	PPU_2	PPU_1
RSVD	RSVD	PPD_6	PPD_5	PPD_4	PPD_3	PPD_2	PPD_1

Program Pin Pull-Up Register (PPU)

The PPU register (address=08h) contains the rest of the programming pin information for the bq2013H. The program pins have a corresponding PPU bit location, PPU_{1-6}. A given location is set if a pull-up resistor has been detected on its corresponding segment driver. For example, if $PROG_3$ and $PROG_5$ have pull-up resistors, the contents of PPU are xx010100.

Output Control Register (OCTL)

The write-only OCTL register (address=0ah) provides the system with a means to check the display connections for the bq2013H. The segment drivers may be overwritten by data from OCTL when bit 1 of OCTL, OCE, is set. The data in bits OC_{5-1} of the OCTL register (see Table 9 for details) is output onto the segment pins, SEG_{5-1}, respectively if OCE=1. *Whenever OCE is written to 1, the MSB of OCTL should be set to a 1.* The OCE register location must be cleared to return the bq2013H to normal operation. OCE may be cleared by either writing the bit to a logic zero via the serial port or by resetting the bq2013H.

Offset Adjustment Register

The value in this register (address = 0bh) is used to correct NAC for the offset of the VFC. This register is initialized from the state of $PROG_6$. The following are the initial values:

- 0 = no offset correction
- 46 = -75µV correction
- 23 = -150µV correcton

The value is set by the equation:

$$\text{Offset} = \frac{1}{289 * V_{COS}}$$

where V_{COS} is the desired offset correction in volts.

Self-Discharge Rate Compensation

This register contains the value used to correct for the self-discharge compensation. This value is initialized from the state of $PROG_3$. The following are the initial values:

- 235 = 1.6% per day $\left(\frac{1}{64}\right)$
- 214 = 0.8% per day $\left(\frac{1}{128}\right)$
- 88 = 0.2% per day $\left(\frac{1}{512}\right)$

The value is set by the equation:

$$\text{SDR} = 256 - \left(\frac{0.3296}{C_{SD}}\right)$$

where C_{SD} is the self-discharge rate per day.

Digital Magnitude Filter (DMF)

The read-write DMF register (address=0dh) provides the system with a means to change the default settings of the digital magnitude filter. By writing different values into this register, the limits of V_{SRD} and V_{SRQ} can be adjusted. The default value for the DMF is 250µV. The value is set by the equation:

$$\text{DMF} = \frac{45}{V_{SRD,Q}}$$

where $V_{SRD,Q}$ is the desired filter threshold in mV.

Note: Care should be taken when writing to this register. A V_{SRD} and V_{SRQ} below the specified V_{OS} may adversely affect the accuracy of the bq2013H.

Load Compensation

The load compensation value (address = 0eh) allows the bq2013H to compensate for small discharge loads that are below the digital filter. Each increment in the LCOMP register represents 2µVh. The value in LCOMP represents the additional amount of discharge applied to NAC and DCR at a constant rate when $V_{SRO} < V_{SRQ}$. LCOMP compensation is applied in addition to self-discharge. LCOMP is set to 0 on a full reset. The value is set by the equation:

$$LCOMP = \frac{1}{289 * V_{CLD}}$$

where V_{CLD} is the desired load correction in volts.

Charge Compensation

The charge-compensation value (address = 0fh) allows the bq2013H to compensate for battery charge inefficiencies. This value is initialized from the state of $PROG_5$ and represents the fast-charge compensation factor for < 30°C. The value can be overwritten via the serial port and is stored in percent. The bq2013H scales the value in 0fh to determine the compensation at other rates and temperatures. For example, if $PROG_5$ = H, the applied efficiency drops by 5% for each temperature range, and the trickle rates are 15% below the fast-charge rates. If the value 55h (85%) is written to CCOMP, the compensation for trickle charge at > 50°C is 60%.

Program Pin Data (PPFC)

The PPFC register provides the means to perform a software controlled reset of the device. The recommended reset method for the bq2013H is:

- Write PPFC to zero
- Write LMD to zero

After these operations, a software reset occurs.

Resetting the bq2013H sets the following:

- LMD = PFC
- VDQ, OCE, LCOMP, and NAC = 0
- BRP = 1

Battery Voltage Register (VSB)

The battery voltage register is used to read the battery voltage on the SB pin. The VSB register (address = 7eh) is updated approximately once per second with the present value of the battery voltage. The battery voltage on the SB pin is determined by the equation:

$$V_{SB} = 1.2V * \left(\frac{VSB}{256}\right)$$

Display

The bq2013H can directly display capacity information using low-power LEDs. If LEDs are used, the segment pins should be tied to V_{CC}, the battery, or the LCOM pin through resistors for programming the bq2013H.

The bq2013H displays the battery charge state in either absolute or relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD.

In absolute mode, each segment represents a fixed amount of charge, based on the initial PFC. In absolute mode, each segment represents 20% of the PFC. As the battery wears out over time, it is possible for the LMD to be below the initial PFC. In this case, all of the LEDs may not turn on, representing the reduction in the actual battery capacity.

When $\overline{DISP}$ is tied to V_{CC}, the SEG_{1-5} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active during charge if the NAC registers are counting at a rate equivalent to V_{SRO} > 500µV or fast discharge if the NAC registers are counting at a rate equivalent to V_{SRO} < -2mV. When $\overline{DISP}$ is pulled low and held, the segment outputs become active continuously. When released to high Z, the segment outputs will remain active for 4 seconds.

The segment outputs are modulated as two banks, with segments 1, 3, and 5 alternating with segments 2 and 4. The segment outputs are modulated at approximately 320Hz, with each bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV1} to indicate a low-battery condition or NAC is less than 10% of the LMD or PFC, depending on the display mode.

Microregulator

The bq2013H can operate directly from 4 nickel or 3 lead acid cells. To facilitate the power supply requirements of the bq2013H, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2013H can be inexpensively built using the FET and an external resistor.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
REF	Relative to V_{SS}	-0.3	+8.5	V	Current limited by R1 (see Figure 1)
V_{SR}	Relative to V_{SS}	-0.3	Vcc+0.7	V	100kΩ series resistor should be used to protect SR in case of a shorted battery.
T_{OPR}	Operating temperature	0	+70	°C	Commercial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDV}	End-of-discharge warning	0.96 * V_{EDV}	V_{EDV}	1.04 * V_{EDV}	V	SB
V_{SRO}	SR sense range	-300	-	+500	mV	SR, $V_{SR} + V_{OS}$
V_{SRQ}	Valid charge	250	-	-	µV	$V_{SR} + V_{OS}$
V_{SRD}	Valid discharge	-	-	-250	µV	$V_{SR} + V_{OS}$

Note: VOS is affected by PC board layout. Proper layout guidelines should be followed for optimal performance. See "LayoutConsiderations."

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
VOS	Offset referred to V_{SR}	-	±50	±150	µV	$\overline{DISP} = V_{CC}$
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	$I_{REF} = 5\mu A$
	Reference at -40°C to +85°C	4.5	-	7.5	V	$I_{REF} = 5\mu A$
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	$V_{REF} = 3V$
I_{CC}	Normal operation	-	90	135	µA	$V_{CC} = 3.0V$, HDQ = 0
		-	120	180	µA	$V_{CC} = 4.25V$, HDQ = 0
		-	170	250	µA	$V_{CC} = 6.5V$, HDQ = 0
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	$0 < V_{SB} < V_{CC}$
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	$V_{DISP} = V_{SS}$
I_{LCOM}	LCOM input leakage	-0.2	-	0.2	µA	$\overline{DISP} = V_{CC}$
I_{RBI}	RBI data-retention current	-	-	100	nA	$V_{RBI} > V_{CC} < 3V$
R_{HDQ}	Internal pulldown	500	-	-	KΩ	
R_{SR}	SR input impedance	10	-	-	MΩ	$-200mV < V_{SR} < V_{CC}$
V_{IHPFC}	PROG logic input high	V_{CC} - 0.2	-	-	V	$PROG_{1-6}$
V_{ILPFC}	PROG logic input low	-	-	V_{SS} + 0.2	V	$PROG_{1-6}$
V_{IZPFC}	PROG logic input Z	float	-	float	V	$PROG_{1-6}$
V_{OLSL}	SEG output low, low V_{CC}	-	0.1	-	V	$V_{CC} = 3V$, $I_{OLS} \leq 1.75mA$ SEG_1–SEG_5, DONE
V_{OLSH}	SEG output low, high V_{CC}	-	0.4	-	V	$V_{CC} = 6.5V$, $I_{OLS} \leq 11.0mA$ SEG_1–SEG_5, DONE
V_{OHML}	LCOM output high, low V_{CC}	V_{CC} - 0.3	-	-	V	$V_{CC} = 3V$, $I_{OHLCOM} = -5.25mA$
V_{OHMH}	LCOM output high, high V_{CC}	V_{CC} - 0.6	-	-	V	$V_{CC} > 3.5V$, $I_{OHLCOM} = -33.0mA$
I_{OLS}	SEG sink current	11.0	-	-	mA	At $V_{OLSH} = 0.4V$, $V_{CC} = 6.5V$
I_{OL}	Open-drain sink current	5.0	-	-	mA	At $V_{OL} = V_{SS} + 0.3V$, HDQ
V_{OL}	Open-drain output low	-	-	0.3	V	$I_{OL} \leq 5mA$, HDQ
V_{IHDQ}	HDQ input high	2.5	-	-	V	HDQ
V_{ILDQ}	HDQ input low	-	-	0.8	V	HDQ
V_{IH}	DONE input high	2.5	-	-	V	DONE
V_{IL}	DONE input low	-	-	0.5	V	DONE
R_{PROG}	Soft pull-up or pull-down resistor value (for programming)	-	-	200	kΩ	$PROG_{1-6}$
R_{FLOAT}	Float state external impedance	-	5	-	MΩ	$PROG_{1-6}$

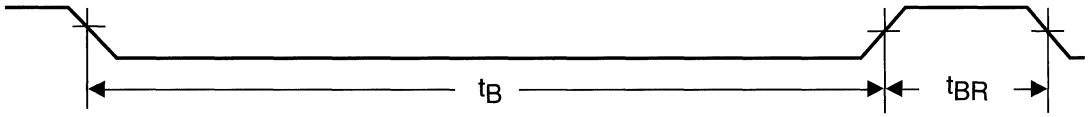
Note: All voltages relative to V_{SS}.

High-Speed Serial Communication Timing Specification ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2013H (write)	190	-	-	µs	See note
t_{CYCB}	Cycle time, bq2013H to host (read)	190	205	250	µs	
t_{STRH}	Start hold, host to bq2013H (write)	5	-	-	ns	
t_{STRB}	Start hold, bq2013H to host (read)	32	-	-	µs	
t_{DSU}	Data setup	-	-	50	µs	
t_{DSUB}	Data setup	-	-	50	µs	
t_{DH}	Data hold	90	-	-	µs	
t_{DV}	Data valid	-	-	80	µs	
t_{SSU}	Stop setup	-	-	145	µs	
t_{SSUB}	Stop setup	-	-	145	µs	
t_{RSPS}	Response time, bq2013H to host	190	-	320	µs	
t_B	Break	190	-	-	µs	
t_{BR}	Break recovery	40	-	-	µs	

Note: The open-drain HDQ pin should be pulled to at least V_{CC} by the host system for proper HDQ operation. HDQ may be left floating if the serial interface is not used.

Break Timing



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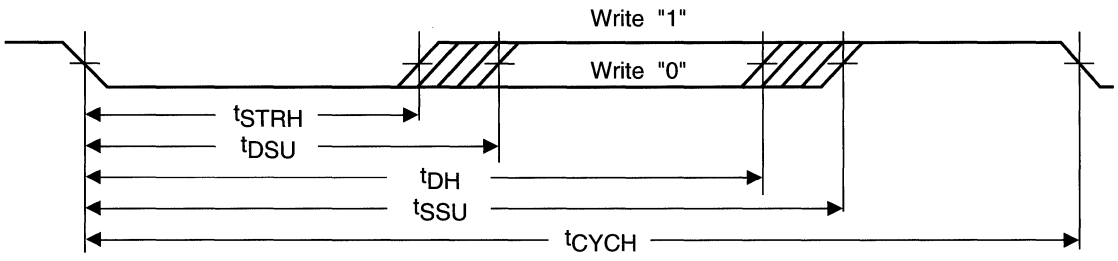
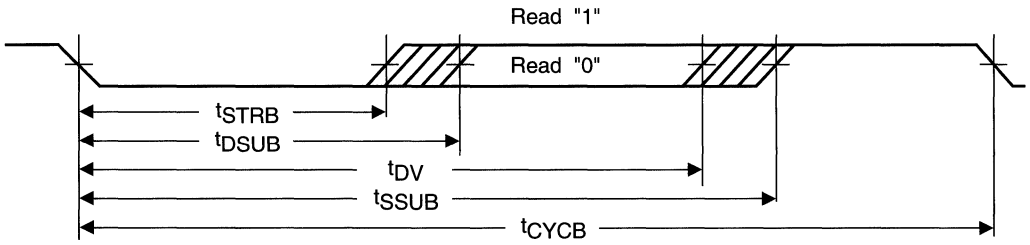
Host to bq2013H



bq2013H to Host

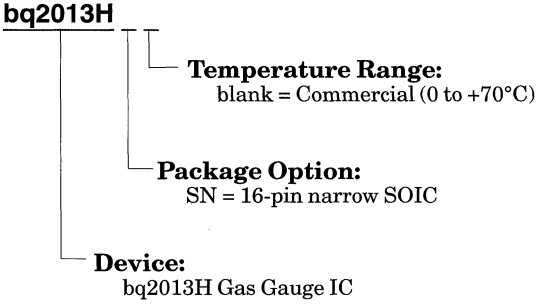


Data Sheet Revision History

ChangeNo.	Page No.	Description of Change
1	All	"Final" changes from "Preliminary" version
2	3	Updated application diagram
2	8	Changed charge/discharge default threshold from 200µV to 250µV.
2	9	Changed offset compensation window range from ±200µV to ±250µV
2	11	Designated appropriate locations from "R/W" to "R"
2	12	Changed charge threshold from 200µV to 250µV
2	14	Changed default DMF from 200µV to 250µV
2	16	Added REF absolute maximum rating
2	16	Changed charge/discharge default threshold from 200µV to 250µV
2	16	Added V_{SRO} parameter
2	17	Changed DQ designation to HDQ
2	17	Changed V_{OL} from 0.5V to 0.3V (max.)
2	17	Added R_{PROG}

Note: Change 1 = Dec. 1998 changes from July 1998 "Preliminary."
Change 2 = May 1999 B changes from Dec. 1998.

Ordering Information



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Gas Gauge IC with External Charge Control

Features

- Conservative and repeatable measurement of available charge in rechargeable batteries
- Charge control output operates an external charge controller such as the bq2004 Fast Charge IC
- Designed for battery pack integration
  - 120µA typical standby current
- Display capacity via single-wire serial communication port or direct drive of LEDs
- Measurements compensated for current and temperature
- Self-discharge compensation using internal temperature sensor
- User-selectable end-of-discharge threshold
- Battery voltage, nominal available charge, temperature, etc. available over serial port
- 16-pin narrow SOIC

General Description

The bq2014 Gas Gauge IC is intended for battery-pack or in-system installation to maintain an accurate record of available battery charge. The IC monitors the voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery.

Self-discharge of NiMH and NiCd batteries is estimated based on an internal timer and temperature sensor. Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and self-discharge calculations to provide available charge information across a wide range of operating conditions. Battery capacity is automatically recalibrated, or "learned," in the course of a discharge cycle from full to empty.

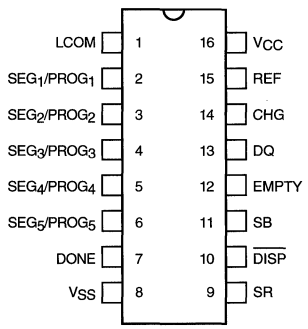
The bq2014 includes a charge control output that controls an external Fast Charge IC such as the bq2004. Nominal Available Charge (NAC) may be directly indicated using a five-segment LED display.

The bq2014 supports a simple single-line bidirectional serial link to an external processor (with a common ground). The bq2014 outputs battery information in response to external commands over the serial link.

Internal registers include available charge, temperature, capacity, battery voltage, battery ID, battery status, and programming pin settings. To support subassembly testing, the outputs may also be controlled. The external processor may also overwrite some of the bq2014 gas gauge data registers.

The bq2014 may operate directly from three or four cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide V_{CC} across a greater number of cells.

Pin Connections



16-Pin Narrow SOIC

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Pin Names

LCOM	LED common output
$SEG_1/PROG_1$	LED segment 1/ program 1 input
$SEG_2/PROG_2$	LED segment 2/ program 2 input
$SEG_3/PROG_3$	LED segment 3/ program 3 input
$SEG_4/PROG_4$	LED segment 4/ program 4 input
$SEG_5/PROG_5$	LED segment 5/ program 5 input
DONE	Fast charge complete
REF	Voltage reference output
CHG	Charge control output
DQ	Serial communications input/output
EMPTY	Empty battery indicator output
SB	Battery sense input
$\overline{DISP}$	Display control input
SR	Sense resistor input
V_{CC}	3.0–6.5V
V_{SS}	System ground

Pin Descriptions

LCOM **LED common output**

Open-drain output switches V_{CC} to source current for the LEDs. The switch is off during initialization to allow reading of the soft pull-up or pull-down programming resistors. LCOM is also in a high impedance state when the display is off.

SEG_1–SEG_5 **LED display segment outputs (dual function with $PROG_1$—$PROG_5$)**

Each output may activate an LED to sink the current sourced from LCOM.

$PROG_1$–$PROG_5$ **Programmed full count selection imputs (dual function with SEG_1—SEG_5)**

These three-level input pins define the programmed full count (PFC) thresholds described in Table 2.

$PROG_3$–$PROG_4$ **Gas gauge rate selection inputs (dual function with SEG_3—SEG_4)**

These three-level input pins define the programmed full count (PFC) thresholds described in Table 2.

$PROG_5$ **Self-discharge rate selection (dual function with SEG_5)**

This three-level input pin defines the self-discharge compensation rate shown in Table 1.

CHG **Charge control output**

This open-drain output becomes active high when charging is allowed.

DONE **Fast charge complete**

This input is used to communicate the status of an external charge controller such as the bq2004 Fast Charge IC. Note: This pin must be pulled down to V_{SS} using a 200KΩ resistor.

SR **Sense resistor input**

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied to the high side of the sense resistor. $V_{SR} < V_{SS}$ indicates discharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop V_{SRO}, as seen by the bq2014, is $V_{SR} + V_{OS}$ (see Table 5).

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ tied to V_{CC} allows $PROG_X$ to connect directly to V_{CC} or V_{SS} instead of through a pull-up or pull-down reistor. $\overline{DISP}$ floating allows the LED display to be active during a valid charge or during discharge if the NAC register is updated at a rate equivalent to $V_{SRO} \leq$ -4mV. $\overline{DISP}$ low activates the display. See Table 1.

SB **Secondary battery input**

This input monitors the single-cell voltage potential through a high-impedance resistive divider network for the end-of-discharge voltage (EDV) thresholds,maximum charge voltage (MCV), and battery removed.

EMPTY **Battery empty output**

This open-drain output becomes high-impedance on detection of a valid final end-of-discharge voltage (V_{EDVF}) and is low following the next application of a valid charge.

DQ **Serial I/O pin**

This is an open-drain bidirectional pin.

REF **Voltage reference output for regulator**

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} **Supply voltage input**

V_{SS} **Ground**

Functional Description

General Operation

The bq2014 determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2014 measures discharge and charge currents, estimates self-discharge, monitors the battery for low-battery voltage thresholds, and compensates for temperature and charge/discharge rates. The charge measurement is made by monitoring the voltage across a small-value series sense resistor between the battery's negative terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2014 using the LED display capability as a charge-state indicator. The bq2014 is configured to display capacity in a relative display mode. The relative display mode uses the last measured discharge capacity of the battery as the battery "full" reference. The LED segments output a percentage of the available charge based on NAC and LMD. A push-button display feature is available for momentarily enabling the LED display.

The bq2014 monitors the charge and discharge currents as a voltage across a sense resistor (see R_S in Figure 1). A filter between the negative battery terminal and the SR pin is required.

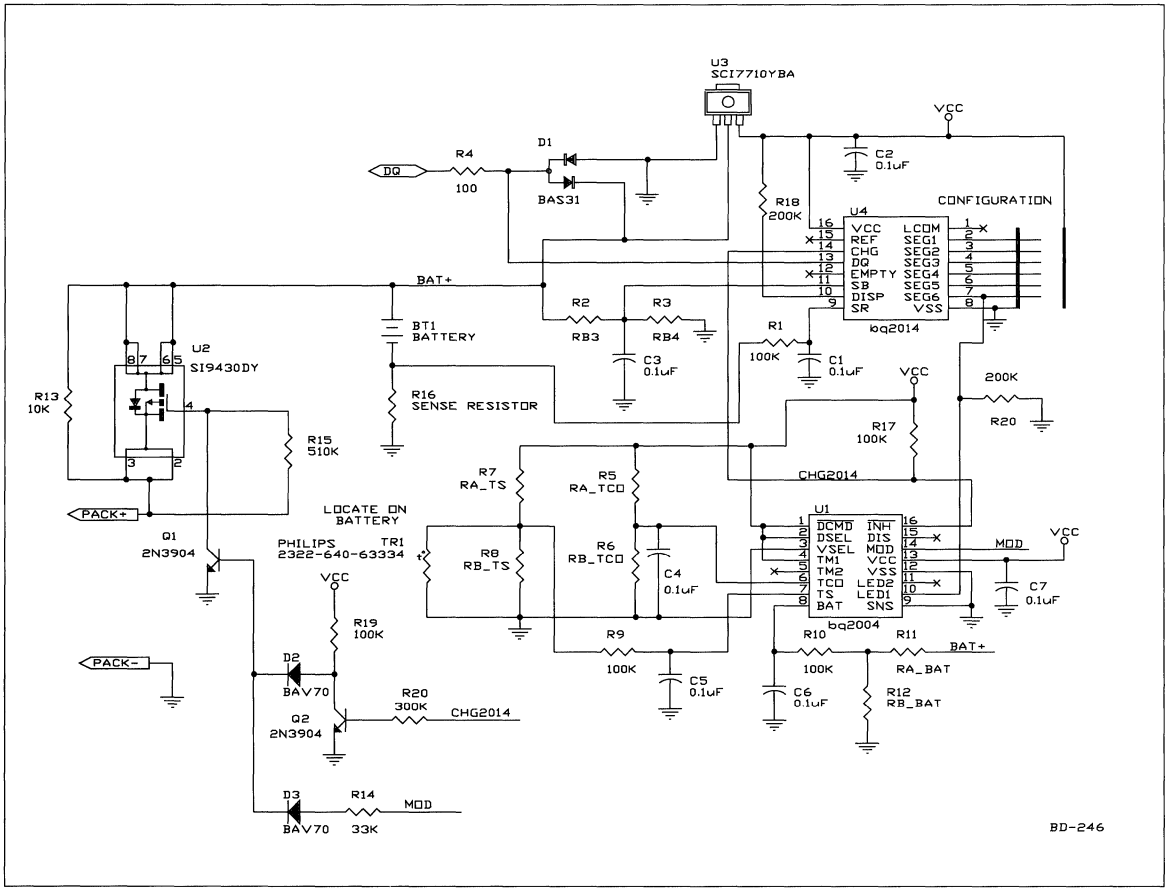


Figure 1. Battery Pack Application Diagram—LED Display,

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2014 monitors the single-cell battery potential through the SB pin. The single-cell voltage potential is determined through a resistor/divider network per the following equation:

$$\frac{R2}{R3} = N - 1$$

where N is the number of cells, R2 is connected to the positive battery terminal, and R3 is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV) and for maximum cell voltage (MCV). EDV threshold levels are used to determine when the battery has reached an "empty" state, and the MCV threshold is used for fault detection during charging.

Two EDV thresholds for the bq2014 are programmable with the default values fixed at:

EDV1 (early warning) = 1.05V

EDVF (empty) = 0.95V

If V_{SB} is below either of the two EDV thresholds, the associated flag is latched and remains latched, independent of V_{SB}, until the next valid charge (as defined in the section entitled "Gas Gauge Operation"). The V_{SB} value is also available over the serial port.

During discharge and charge, the bq2014 monitors V_{SR} for various thresholds. These thresholds are used to compensate the charge and discharge rates. Refer to the count compensation section for details. EDV monitoring is disabled if $V_{SR} \leq$ -250mV typical and resumes ½ second after $V_{SR} >$ -250mV.

EMPTY Output

The EMPTY output switches to high impedance when $V_{SB} < V_{EDF}$ and remains latched until a valid charge occurs.

Reset

The bq2014 recognizes a valid battery whenever V_{SB} is greater than 0.1V typical. V_{SB} rising from below 0.25V or falling from above 2.25V (V_{MCV}) resets the device. Reset can also be accomplished with a command over the serial port as described in the Reset Register section.

Temperature

The bq2014 internally determines the temperature in 10°C steps centered from -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available charge display translation. The temperature range is available over the serial port in 10°C increments as shown below:

TMPGG (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2014 measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (C2 and C3) should be placed as close as possible to the SB and V_{CC} pins, respectively, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor (R1, C1) should be placed as close as possible to the SR pin.
- The sense resistor (R16) should be as close as possible to the bq2014.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2014. The bq2014 accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge and discharge currents are temperature and rate compensated, whereas self-discharge is only temperature compensated.

The main counter, Nominal Available Charge (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2014 adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the Programmed Full Count (PFC) shown in Table 2. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

Many actions in the bq2014 are triggered by detection of a "valid charge." NAC is stored in an asynchronous, 2-byte counter; the lower byte is NACL and the upper byte is NACH. A valid charge has occurred anytime the charge lasts long enough to cause an increment in NACH. Small increments of charging are not considered "valid" if they result in counts in NACL but do not generate a roll-over (carry) that increments NACH. NACL is reset anytime the counter direction changes from down to up, so the number of counts required to cause a roll-over and a valid charge is always 256. The counter may be incrementing by 2, 4, 8, or more counts per increment, however, depending on the scaling factors selected. Therefore, a valid charge may be constituted by a smaller number of counter increments.

1. **Last Measured Discharge (LMD) or learned battery capacity:**

   LMD is the last measured discharge capacity of the battery. On initialization (application of V_{CC} or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register (DCR) representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

2. **Programmed Full Count (PFC) or initial battery capacity:**

   The initial LMD and gas gauge rate values are programmed by using $PROG_1$—$PROG_4$. The bq2014 is configured for a given application by selecting a PFC value from Table 2. The correct PFC may be

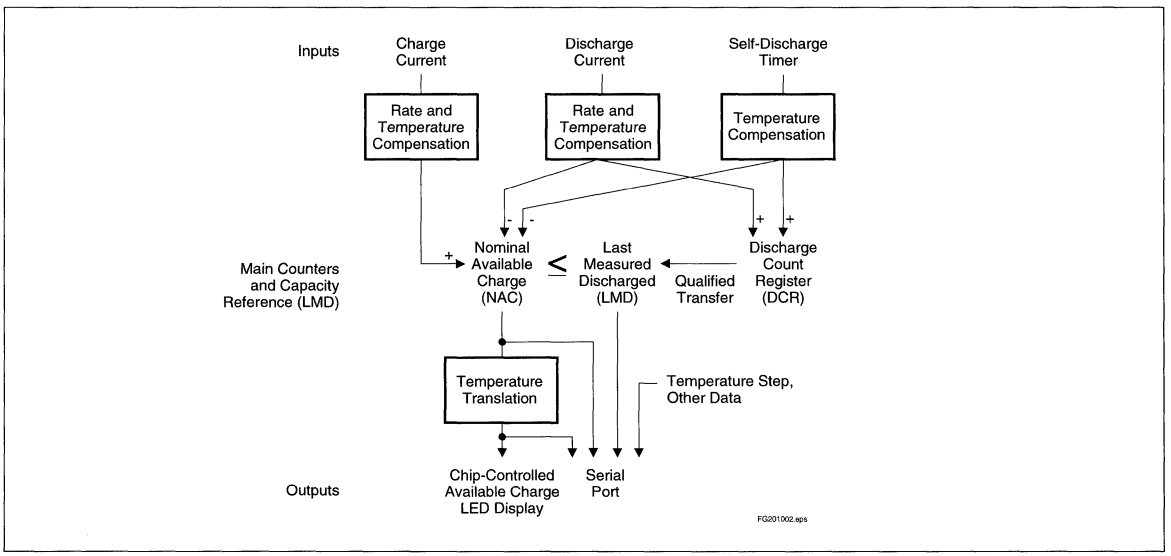


Figure 2. Operational Overview

determined by multiplying the rated battery capacity in mAh by the sense resistor value:

Battery capacity (mAh) * sense resistor (Ω) =

PFC (mVh)

Selecting a PFC slightly less than the rated capacity for absolute mode provides capacity above the full reference for much of the battery's life.

Example: Selecting a PFC Value

Given:

Sense resistor = 0.1Ω
Number of cells = 6
Capacity = 2200mAh, NiCd battery
Current range = 50mA to 2A
Relative display mode
Serial port only
Self-discharge = $^{C}/_{64}$
Voltage drop over sense resistor = 5mV to 400mV

Therefore:

2200mAh * 0.1Ω = 220mVh

Select:

PFC = 33792 counts or 211mVh
$PROG_1$ = float
$PROG_2$ = float
$PROG_3$ = float
$PROG_4$ = low
$PROG_5$ = float
DONE = low

Table 1. bq2014 Programming

Pin Connection	$PROG_5$ Self-Discharge Rate	$\overline{DISP}$ Display State
H	Disabled	LED disabled
Z	$^{NAC}/_{64}$	LED enabled on discharge when V_{SRO} < -4mV or during a valid charge
L	$^{NAC}/_{47}$	LED on

Table 2. bq2014 Programmed Full Count mVh Selections

$PROG_x$		Programmed Full Count (PFC)	$PROG_4$ = L			$PROG_4$ = Z			Units
1	2		PROG3 = H	PROG3 = Z	PROG3 = L	PROG3 = H	PROG3 = Z	PROG3 = L	
-	-	-	Scale = 1/80	Scale = 1/160	Scale = 1/320	Scale = 1/640	Scale = 1/1280	Scale = 1/2560	mVh/ count
H	H	49152	614	307	154	76.8	38.4	19.2	mVh
H	Z	45056	563	282	141	70.4	35.2	17.6	mVh
H	L	40960	512	256	128	64.0	32.0	16.0	mVh
Z	H	36864	461	230	115	57.6	28.8	14.4	mVh
Z	Z	33792	422	211	106	53.0	26.4	13.2	mVh
Z	L	30720	384	192	96.0	48.0	24.0	12.0	mVh
L	H	27648	346	173	86.4	43.2	21.6	10.8	mVh
L	Z	25600	320	160	80.0	40.0	20.0	10.0	mVh
L	L	22528	282	141	70.4	35.2	17.6	8.8	mVh
VSR equivalent to 2 counts/s (nom.)			90	45	22.5	11.25	5.6	2.8	mV

The initial full battery capacity is 211mVh (2110mAh) until the bq2014 "learns" a new capacity with a qualified discharge from full to EDV1.

3. **Nominal Available Charge (NAC):**

   NAC counts up during charge to a maximum value of LMD and down during discharge and self-discharge to 0. NAC is reset to 0 on initialization and on the first valid charge after EDV = 1. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = LMD.

4. **Discharge Count Register (DCR):**

   The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0 until V_{SB} < EDV1. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC = LMD. The DCR does not roll over but stops counting when it reaches FFFFh.

   The DCR value becomes the new LMD value on the first charge after a valid discharge to V_{EDV1} if:

   - No valid charges have occurred during the period between NAC = LMD and EDV1 detected.
   - The self-discharge count is not more than 4096 counts (8% to 18% of PFC, specific percentage threshold determined by PFC).
   - The temperature is ≥ 0°C when the EDV1 level is reached during discharge.

   The valid discharge flag (VDQ) indicates whether the present discharge is valid for LMD update.

Charge Counting

Charge activity is detected based on a positive voltage on the V_{SR} input. The bq2014 determines charge activity sustained at a continuous rate equivalent to V_{SRO} (V_{SR} + V_{OS}) > V_{SRQ}. Once a valid charge is detected, charge counting continues until V_{SRO} falls below V_{SRQ}. V_{SRQ} is a programmable threshold (as described in the Digital Magnitude Filter section) and has a default value of 375µV. If charge activity is detected, the bq2014 increments the NAC at a rate proportional to V_{SRO}. If enabled, the bq2014 then activates an LED display. Charge actions increment the NAC after compensation for charge rate and temperature.

Charge Control

Charge control is provided by the CHG output. This output is asserted continuously when NAC > 0.94 * LMD. CHG is also asserted when a valid charge is detected (CHGS in the FLGS1 register is also set). CHG is low when NAC < 0.94 * LMD and there is no valid charge activity.

DONE Input

When the bq2014 detects a valid charge complete with an active-high signal on the DONE input, NAC is set to LMD for $NAC/_{64}$ (NiCd) self-discharge setting. NAC is set to 94% of LMD (if NAC is below 94%) for $NAC/_{47}$ (NiMH) self-discharge setting. VDQ is set along with DONE.

Discharge Counting

All discharge counts where V_{SRO} < V_{SRD} cause the NAC register to decrement and the DCR to increment if EDV1 = 0. Exceeding the fast discharge threshold (FDQ) if the rate is equivalent to V_{SRO} < -4mV activates the display, if enabled. The display becomes inactive after V_{SRO} rises above -4mV. V_{SRD} is a programmable threshold as described in the Digital Magnitude Filter section. The default value for V_{SRD} is -300µV.

Self-Discharge Estimation

The bq2014 continuously decrements NAC and increments DCR for self-discharge based on time and temperature. The self-discharge count rate is programmed to be a nominal $1/_{64}$ * NAC or $1/_{47}$ * NAC per day or disabled as selected by $PROG_5$. This is the rate for a battery whose temperature is between 20°C–30°C. The NAC register cannot be decremented below 0.

Count Compensations

The bq2014 determines fast charge when the NAC updates at a rate of ≥ 2 counts/sec. Charge and discharge activity is compensated for temperature and charge/discharge rate before updating the NAC and/or DCR. Self-discharge estimation is compensated for temperature before updating the NAC or DCR.

Charge Compensation

Two charge efficiency compensation factors are used for trickle charge and fast charge. Fast charge is defined as a rate of charge resulting in ≥ 2 NAC counts/sec (≥ 0.15C to 0.32C depending on PFC selections; see Table 2). The compensation defaults to the fast charge factor until the actual charge rate is determined.

Temperature adapts the charge rate compensation factors over three ranges between nominal, warm, and hot temperatures. The compensation factors are shown below.

Charge Temperature	Trickle Charge Compensation	Fast Charge Compensation
< 40°C	0.80	0.95
> 40°C	0.75	0.90

Discharge Compensation

Corrections for the rate of discharge are made by adjusting an internal discharge compensation factor. The discharge factor is based on the dynamically measured V_{SR}.

The compensation factors during discharge are:

Approximate V_{SR} Threshold	Discharge Compensation Factor	Efficiency
V_{SR} > -150 mV	1.00	100%
V_{SR} < -150 mV	1.05	95%

Temperature compensation during discharge also takes place. At lower temperatures, the compensation factor increases by 0.05 for each 10°C temperature range below 10°C.

$$\text{Comp. factor} = 1.00 + (0.05 * N)$$

Where N = number of 10°C steps below 10°C and -150mV < V_{SR} < 0.

For example:

T > 10°C: Nominal compensation, N = 0

0°C < T < 10°C: N = 1 (i.e., 1.00 becomes 1.05)

-10°C < T < 0°C: N = 2 (i.e., 1.00 becomes 1.10)

-20°C < T < -10°C: N = 3 (i.e., 1.00 becomes 1.15)

-20°C < T < -30°C: N = 4 (i.e., 1.00 becomes 1.20)

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of $1/64$ * NAC per day, $1/47$ * NAC per day, or disabled. This is the rate for a battery within the 20°C–30°C temperature range (TMPGG = 6x). This rate varies across 8 ranges from <10°C to >70°C, doubling with each higher temperature step (10°C). See Table 3

Table 3. Self-Discharge Compensation

Temperature Step	Typical Rate	
	$PROG_5$ = Z	$PROG_5$ = L
< 10°C	NAC/256	NAC/188
10–20°C	NAC/128	NAC/94
20–30°C	NAC/64	NAC/47
30–40°C	NAC/32	NAC/23.5
40–50°C	NAC/16	NAC/11.8
50–60°C	NAC/8	NAC/5.88
60–70°C	NAC/4	NAC/2.94
> 70°C	NAC/2	NAC/1.47

Digital Magnitude Filter

The bq2014 has a programmable digital filter to eliminate charge and discharge counting below a set threshold. The default setting is -0.30mV for V_{SRD} and +0.38mV for V_{SRQ}. The proper digital filter setting can be calculated using the following equation. Table 4 shows typical digital filter settings.

$$V_{SRD}\,(mV) = \frac{-45}{DMF}$$

$$V_{SRQ}\,(MV) = -125 * V_{SRD}$$

Table 4. Typical Digital Filter Settings

DMF	DMF Hex.	V_{SRD} (mV)	V_{SRQ} (mV)
75	4B	-0.60	0.75
100	64	-0.45	0.56
150 (default)	96	-0.30	0.38
175	AF	-0.26	0.32
200	C8	-0.23	0.28

Error Summary

Capacity Inaccurate

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see the DCR description on page 7). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

A Capacity Inaccurate counter (CPI) is maintained and incremented each time a valid charge occurs (qualified by NAC; see the CPI register description) and is reset

Table 5. Current-Sensing Error as a Function of V_{SR}

Symbol	Parameter	Typical	Maximum	Units	Notes
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

whenever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

Current-Sensing Error

Table 5 illustrates the current-sensing error as a function of V_{SR}. A digital filter eliminates charge and discharge counts to the NAC register when V_{SRO} (V_{SR} + V_{OS}) is between V_{SRQ} and V_{SRD}.

Communicating With the bq2014

The bq2014 includes a simple single-pin (DQ plus return) serial data interface. A host processor uses the interface to access various bq2014 registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain DQ pin on the bq2014 should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2014. The command directs the bq2014 to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 333 bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2014 may be sampled using the pulse-width capture timers available on some microcontrollers.

Communication is normally initiated by the host processor sending a BREAK command to the bq2014. A BREAK is detected when the DQ pin is driven to a logic-low state for a time, t_B or greater. The DQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2014 is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2014 taking the DQ pin to a logic-low state for a period, $t_{STRH,B}$. The next section is the actual data transmission, where the data should be valid by a period, t_{DSU}, after the negative edge used to start communication. The data should be held for a period, t_{DV}, to allow the host or bq2014 to sample the data bit.

The final section is used to stop the transmission by returning the DQ pin to a logic-high state by at least a period, t_{SSU}, after the negative edge used to start communication. The final logic-high state should be held until a period, t_{SV}, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2014 is always performed with the least-significant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2014 NAC register.

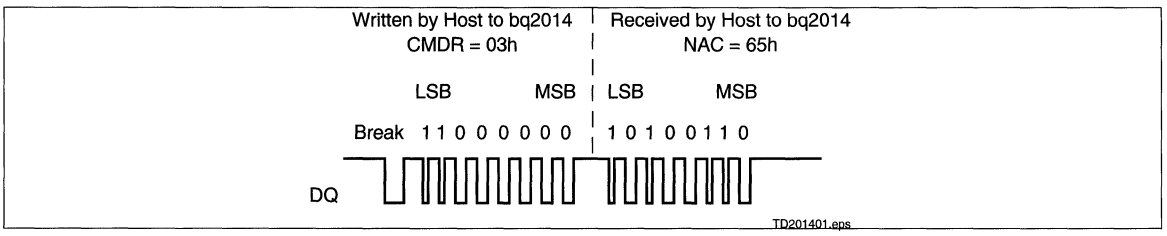


Figure 3. Typical Communication With the bq2014

9/19

bq2014 Registers

The bq2014 command and status registers are listed in Table 6 and described below.

Command Register (CMDR)

The write-only CMDR register is accessed when eight valid command bits have been received by the bq2014. The CMDR register contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function.

The W/$\overline{R}$ values are:

CMDR Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is:

0 The bq2014 outputs the requested register contents specified by the address portion of CMDR.

1 The following eight bits should be written to the register specified by the address portion of CMDR.

The lower seven-bit field of CMDR contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

CMDR Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Primary Status Flags Register (FLGS1)

The read-only FLGS1 register (address=01h) contains the primary bq2014 flags.

The ***charge status*** flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when $V_{SRO} > V_{SRQ}$. A V_{SRO} of less than V_{SRQ} or discharge activity clears CHGS.

The CHGS values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
CHGS	-	-	-	-	-	-	-

Where CHGS is:

0 Either discharge activity detected or $V_{SRO} < V_{SRQ}$

1 $V_{SRO} > V_{SRQ}$

The ***battery replaced*** flag (BRP) is asserted whenever the potential on the SB pin (relative to V_{SS}), V_{SB}, falls from above the maximum cell voltage, MCV (2.25V), or rises above 0.1V. The BRP flag is also set when the bq2014 is reset (see the RST register description). BRP is reset when either a valid charge action increments NAC to be equal to LMD, or a valid charge action is detected after the EDV1 flag is asserted. BRP = 1 signifies that the device has been reset.

The BRP values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	BRP	-	-	-	-	-	-

Where BRP is:

0 Battery is charged until NAC = LMD or discharged until the EDV1 flag is asserted

1 V_{SB} dropping from above MCV, V_{SB} rising from below 0.1V, or a serial port initiated reset has occurred

The ***battery removed*** flag (BRM) is asserted whenever the potential on the SB pin (relative to V_{SS}) rises above MCV or falls below 0.1V. The BRM flag is asserted until the condition causing BRM is removed. Because of signal filtering, 30 seconds may have to transpire for BRM to react to battery insertion or removal.

The BRM values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	BRM	-	-	-	-	-

Where BRM is:

0 $0.1V < V_{SB} < 2.25V$

1 $0.1V > V_{SB}$ or $V_{SB} > 2.25V$

The ***capacity inaccurate*** flag (CI) is used to warn the user that the battery has been charged a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2014 is reset. The flag is cleared after an LMD update.

Table 6. bq2014 Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	Command register	00h	Write	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
FLGS1	Primary status flags register	01h	Read	CHGS	BRP	BRM	CI	VDQ	n/u	EDV1	EDVF
TMPGG	Temperature and gas gauge register	02h	Read	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available charge high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	Nominal available charge low byte register	17h	Read	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	Read	CR	DR2	DR1	DR0	n/u	n/u	n/u	OVLD
PPD	Program pin pull-down register	07h	Read	n/u	n/u	PPD6	PPD5	PPD4	PPD3	PPD2	PPD1
PPU	Program pin pull-up register	08h	Read	n/u	n/u	PPU6	PPU5	PPU4	PPU3	PPU2	PPU1
CPI	Capacity inaccurate count register	09h	Read	CPI7	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	CPI0
DMF	Digital magnitude filter register	0Ah	R/W	DMF7	DMF6	DMF5	DMF4	DMF3	DMF2	DMF1	DMF0
VSB	Battery voltage	0Bh	Read	VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0
VTS	End-of-discharge threshold select	0Ch	R/W	VTS7	VTS6	VTS5	VTS4	VTS3	VTS2	VTS1	VTS0
RST	Reset register	39h	Write	RST	0	0	0	0	0	0	0

Note: n/u = not used

The CI values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	CI	-	-	-	-

Where CI is:

0 When LMD is updated with a valid full discharge

1 After the 64th valid charge action with no LMD updates or when the device is reset

The ***valid discharge*** flag (VDQ) is asserted when the bq2014 is discharged from NAC = LMD or DONE is valid. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- The self-discharge count register (SDCR) has exceeded the maximum acceptable value (4096 counts) for an LMD update.
- A valid charge action sustained at $V_{SRO} > V_{SRQ}$ for at least 256 NAC counts.
- The EDV flag was set at a temperature below 0°C

The VDQ values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

Where VDQ is:

0 SDCR ≥ 4096, subsequent valid charge action detected, or EDV1 is asserted with the temperature less than 0°C

1 On first discharge after NAC = LMD or DONE is valid

The ***first end-of-discharge warning*** flag (EDV1) warns the user that the battery is almost empty. The first segment pin, SEG_1, is modulated at a 4Hz rate if the display is enabled once EDV1 is asserted, which should warn the user that loss of battery power is imminent. The EDV1 flag is latched until a valid charge has been detected. The EDV1 threshold is externally controlled via the VTS register (see Voltage Threshold Register on this page).

The EDV1 values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV1	-

Where EDV1 is:

0 Valid charge action detected, $V_{SB} \geq V_{TS}$

1 $V_{SB} < V_{TS}$ providing that OVLD=0 (see FLGS2 register description)

The ***final end-of-discharge warning*** flag (EDVF) flag is used to warn that battery power is at a failure condition. All segment drivers are turned off. The EDVF flag is latched until a valid charge has been detected. The EMPTY pin is also forced to a high-impedance state on assertion of EDVF. The host system may pull EMPTY high, which may be used to disable circuitry to prevent deep-discharge of the battery. The EDVF threshold is set 100mV below the EDV1 threshold.

The EDVF values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	EDVF

Where EDVF is:

0 Valid charge action detected, $V_{SB} \geq V_{TS}$ - 100mV

1 $V_{SB} < V_{TS}$ - 100mV providing that OVLD=0 (see FLGS2 register description)

Voltage Threshold Register (VTS)

The end-of-discharge threshold voltages (EDV1 and EDVF) can be set using the VTS register (address=0ch). The read/write VTS register sets the EDV1 trip point. EDVF is set 100mV below EDV1. The default value in the VTS register is 70h, representing EDV1 = 1.05V and EDVF = 0.95V. EDV1 = 2.4V * (VTS/256).

VTS Register Bits							
7	6	5	4	3	2	1	0
VTS7	VTS6	VTS5	VTS4	VTS3	VTS2	VTS1	VTS0

Battery Voltage Register (VSB)

The read-only battery voltage register is used to read the single-cell battery voltage on the SB pin. The VSB register is updated approximately once per second with the present value of the battery voltage.
V_{SB} = 2.4V * (VSB/256)

VSB Register Bits							
7	6	5	4	3	2	1	0
VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0

Temperature and Gas Gauge Register (TMPGG)

The read-only TMPGG register (address=02h) contains two data fields. The first field contains the battery temperature. The second field contains the available charge from the battery.

TMPGG Temperature Bits							
7	6	5	4	3	2	1	0
TMP3	TMP2	TMP1	TMP0	-	-	-	

The bq2014 contains an internal temperature sensor. The temperature is used to set charge and discharge efficiency factors as well as to adjust the self-discharge coefficient. The temperature register contents may be translated as shown in Table 7.

The bq2014 calculates the available charge as a function of NAC, temperature, and LMD. The results of the calculation are available via the display port or the gas gauge field of the TMPGG register. The register is used to give available capacity in $\frac{1}{16}$ increments from 0 to $\frac{15}{16}$.

TMPGG Gas Gauge Bits							
7	6	5	4	3	2	1	0
-	-	-	-	GG3	GG2	GG1	GG0

The gas gauge display and the gas gauge portion of the TMPGG register are adjusted for cold temperature dependencies. A piece-wise correction is performed as follows:

Temperature	Available Capacity Calculation
> 0°C	NAC / "Full Reference"
-20°C < T < 0°C	0.75 * NAC / "Full Reference"
< -20°C	0.5 * NAC / "Full Reference"

The adjustment between > 0°C and -20°C < T < 0°C has a 10°C hysteresis.

Nominal Available Charge Register (NACH/NACL)

The read/write NACH register (address=03h) and the read-only NACL low-byte register (address=17h) are the main gas gauging registers for the bq2014. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC.

Table 7. Temperature Register Translation

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

On reset, NACH and NACL are cleared to 0. When the bq2014 detects a charge, NACL resets to 0. NACH and NACL are reset to 0 on the first valid charge after V_{SB} = EDV1. *Writing to the NAC registers affects the available charge counts and, therefore, affects the bq2014 gas gauge operation. Do not write the NAC registers to a value greater than* LMD.

Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V_{CC} is greater than 2V. The contents of BATID have no effect on the operation of the bq2014. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2014 uses as a measured full reference. The bq2014 adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2014 updates the capacity of the battery. LMD is set to PFC during a bq2014 reset.

Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2014 flags.

The ***charge rate*** flag (CR) is used to denote the fast charge regime. Fast charge is assumed whenever a charge action is initiated. The CR flag remains asserted if the charge rate does not fall below 2 counts/sec.

The CR values are:

FLGS2 Bits							
7	6	5	4	3	2	1	0
CR	-	-	-	-	-	-	-

Where CR is:

0 When charge rate falls below 2 counts/sec

1 When charge rate is above 2 counts/sec

The fast charge regime efficiency factors are used when CR = 1. When CR = 0, the trickle charge efficiency factors are used. The time to change CR varies due to the user-selectable count rates.

The ***discharge rate*** flags, DR2–0, are bits 6–4.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-	-	-	

They are used to determine the current discharge regime as follows:

DR2	DR1	DR0	V_{SR} (V)
0	0	0	V_{SR} > -150mV
0	0	1	V_{SR} < -150mV

The ***overload*** flag (OVLD) is asserted when a discharge overload is detected, V_{SR} < -250mV. OVLD remains asserted as long as the condition persists and is cleared after V_{SR} > -150mV. The overload condition is used to stop sampling of the battery terminal characteristics for end-of-discharge determination when excessive discharges occur.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OVLD

DR2–0 and OVLD are set based on the measurement of the voltage at the SR pin relative to V_{SS}. The rate at which this measurement is made varies with device activity.

Program Pin Pull-Down Register (PPD)

The read-only PPD register (address=07h) contains some of the programming pin information for the bq2014. The segment drivers, SEG_{1-5} and DONE, have corresponding PPD register locations, PPD_{1-6}. A given location is set if a pull-down resistor has been detected on its corresponding segment driver. For example, if SEG_1 and SEG_4 have pull-down resistors, the contents of PPD are xx101001. (**Note:** DONE must be pulled down for proper operation.)

Program Pin Pull-Up Register (PPU)

The read-only PPU register (address=08h) contains the rest of the programming pin information for the bq2014. The segment drivers, SEG_{1-5} and DONE, have corresponding PPU register locations, PPU_{1-6}. A given location is set if a pull-up resistor has been detected on its corresponding segment driver. For example, if SEG_3 and DONE have pull-up resistors, the contents of PPU are xx100100.

PPD/PPU Bits							
8	7	6	5	4	3	2	1
-	-	PPU_6	PPU_5	PPU_4	PPU_3	PPU_2	PPU_1
-	-	PPD_6	PPD_5	PPD_4	PPD_3	PPD_2	PPD_1

Capacity Inaccurate Count Register (CPI)

The read-only CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2014 adapts to the changing capacity over time. A complete discharge from full (NAC=LMD) to empty (EDV1=1) is required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and the self-discharge counter is less than 4096 counts.

The CPI register is incremented every time a valid charge is detected. When NAC > 0.94 * LMD, however, the CPI register increments on the first valid charge; CPI does not increment again for a valid charge until NAC < 0.94 * LMD. This prevents continuous trickle charging from incrementing CPI if self-discharge decrements NAC. The CPI register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. The CPI register is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

Digital Magnitude Filter (DMF)

The read-write DMF register (address=0Ah) provides the system with a means to change the default settings of the digital magnitude filter. By writing different values into this register, the limits of V_{SRD} and V_{SRQ} can be adjusted.

Note: Care should be taken when writing to this register. A V_{SRD} and V_{SRQ} below the specified V_{OS} may adversely affect the accuracy of the bq2014. Refer to Table 4 for recommended settings for the DMF register.

Reset Register (RST)

The reset register (address=39h) provides the means to perform a software-controlled reset of the device. By writing the RST register contents from 00h to 80h, a bq2014 reset is performed. *Setting any bit other than the most-significant bit of the RST register is* ***not allowed****, and results in improper operation of the bq2014.*

Resetting the bq2014 sets the following:

- LMD = PFC
- CPI, VDQ, NAC, and NACL = 0
- CI and BRP = 1

Note: Self-discharge is disabled when $PROG_5$ = H.

Display

The bq2014 can directly display capacity information using low-power LEDs. If LEDs are used, the program pins should be resistively tied to V_{CC} or V_{SS} for a program high or program low, respectively..

The bq2014 displays the battery charge state in relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD.

The capacity display is also adjusted for the present battery temperature. The temperature adjustment reflects the available capacity at a given temperature but does not affect the NAC register. The temperature adjustments are detailed in the TMPGG register description.

When $\overline{DISP}$ is tied to V_{CC}, the SEG_{1-5} outputs are inactive. **Note: $\overline{DISP}$ must be tied to V_{CC} if the LEDs are not used.** When $\overline{DISP}$ is left floating, the display becomes active whenever the NAC registers are counting at a rate equivalent to V_{SRO} < -4mV or charge current is detected, $V_{SRO} > V_{SRQ}$. When pulled low, the segment outputs become active immediately. A capacitor tied to $\overline{DISP}$ allows the display to remain active for a short period of time after activation by a push-button switch.

The segment outputs are modulated as two banks of three, with segments 1, 3, and 5 alternating with segments 2 and 4. The segment outputs are modulated at approximately 100Hz, with each segment bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV1} (EDV1 = 1), indicating a low-battery condition. V_{SB} below V_{EDVF} (EDVF = 1) disables the display output.

Microregulator

The bq2014 can operate directly from 3 or 4 cells. To facilitate the power supply requirements of the bq2014, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2014 can be inexpensively built using the FET and an external resistor; see Figure 1.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	7.0	V	
All other pins	Relative to V_{SS}	-0.3	7.0	V	
REF	Relative to V_{SS}	-0.3	8.5	V	Current limited by R1 (see Figure 1)
V_{SR}	Relative to V_{SS}	-0.3	7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2014 application note for details).
T_{OPR}	Operating temperature	0	70	°C	Commercial
		-40	85	°C	Industrial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning, default	0.92	0.95	0.98	V	SB
V_{EDV1}	First empty warning, default	1.02	1.05	1.08	V	SB
V_{SR1}	Discharge compensation threshold	-120	-150	-180	mV	SR
V_{SRO}	SR sense range	-300	-	2000	mV	SR
V_{OVLD}	Overload threshold	-220	-250	-280	mV	SR
V_{SRQ}	Valid charge	375	-	-	µV	$V_{SR} + V_{OS}$ (see note 1)
V_{SRD}	Valid discharge	-	-	-300	µV	$V_{SR} + V_{OS}$ (see note 1)
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	SB
V_{BR}	Battery removed/replaced	-	0.1	0.25	V	SB pulled low
		2.20	2.25	2.30	V	SB pulled high

Notes:
1. Default value; value set in DMF register. V_{OS} is affected by PC board layout. Proper layout guide lines should be followed for optimal performance.
2. To ensure correct threshold determination and proper operation, $V_{CC} > V_{SB} + 1.5V$

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{OS}	Offset referred to V_{SR}	-	±50	±150	µV	$\overline{DISP} = V_{CC}$
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	$I_{REF} = 5\mu A$
	Reference at -40°C to +85°C	4.5	-	7.5	V	$I_{REF} = 5\mu A$
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	$V_{REF} = 3V$
I_{CC}	Normal operation	-	90	135	µA	$V_{CC} = 3.0V$
		-	120	180	µA	$V_{CC} = 4.25V$
		-	170	250	µA	$V_{CC} = 6.5V$
V_{SB}	Battery input	-	-	2.4	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	$0 < V_{SB} < V_{CC}$
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	$V_{DISP} = V_{SS}$
I_{LCOM}	LCOM input leakage	-0.2	-	0.2	µA	$\overline{DISP} = V_{CC}$
R_{DQ}	Internal pulldown	500	-	-	KΩ	
V_{SR}	Sense resistor input	-0.3	-	2.0	V	$V_{SR} < V_{SS}$ = discharge; $V_{SR} > V_{SS}$ = charge
R_{SR}	SR input impedance	10	-	-	MΩ	$-200mV < V_{SR} < V_{CC}$
V_{IH}	Logic input high	V_{CC} - 0.2	-	-	V	$PROG_1$–$PROG_5$
V_{IL}	Logic input low	-	-	V_{SS} + 0.2	V	$PROG_1$–$PROG_5$; note 2
V_{IZ}	Logic input Z	float	-	float	V	$PROG_1$–$PROG_5$
V_{OLSL}	SEG_X output low, low V_{CC}	-	0.1	-	V	$V_{CC} = 3V$, $I_{OLS} \leq 1.75mA$ SEG_1–SEG_5
V_{OLSH}	SEG_X output low, high V_{CC}	-	0.4	-	V	$V_{CC} = 6.5V$, $I_{OLS} \leq 11.0mA$ SEG_1–SEG_5
V_{OHLCL}	LCOM output high, low V_{CC}	V_{CC} - 0.3	-	-	V	$V_{CC} = 3V$, $I_{OHLCOM} = -5.25mA$
V_{OHLCH}	LCOM output high, high V_{CC}	V_{CC} - 0.6	-	-	V	$V_{CC} = 6.5V$, $I_{OHLCOM} = -33.0mA$
I_{IH}	$PROG_{1-5}$ input high current	-	1.2	-	µA	$V_{PROG} = V_{CC}/2$
I_{IL}	$PROG_{1-5}$ input low current	-	1.2	-	µA	$V_{PROG} = V_{CC}/2$
I_{OHLCOM}	LCOM source current	-33	-	-	mA	At $V_{OHLCH} = V_{CC} - 0.6V$
I_{OLS}	SEG_X sink current	-	-	11.0	mA	At $V_{OLSH} = 0.4V$
I_{OL}	Open-drain sink current	-	-	5.0	mA	At $V_{OL} = V_{SS} + 0.3V$ DQ, EMPTY, CHG
V_{OL}	Open-drain output low	-	-	0.5	V	$I_{OL} \leq 5mA$, DQ, EMPTY
V_{IHDQ}	DQ input high	2.5	-	-	V	DQ
V_{ILDQ}	DQ input low	-	-	0.8	V	DQ
R_{PROG}	Soft pull-up or pull-down resistor value (for programming)	-	-	200	KΩ	$PROG_1$–$PROG_5$
R_{FLOAT}	Float state external impedance	-	5	-	MΩ	$PROG_1$–$PROG_5$

Notes: 1. All voltages relative to V_{SS}.

2. DONE must be pulled low for proper operation.

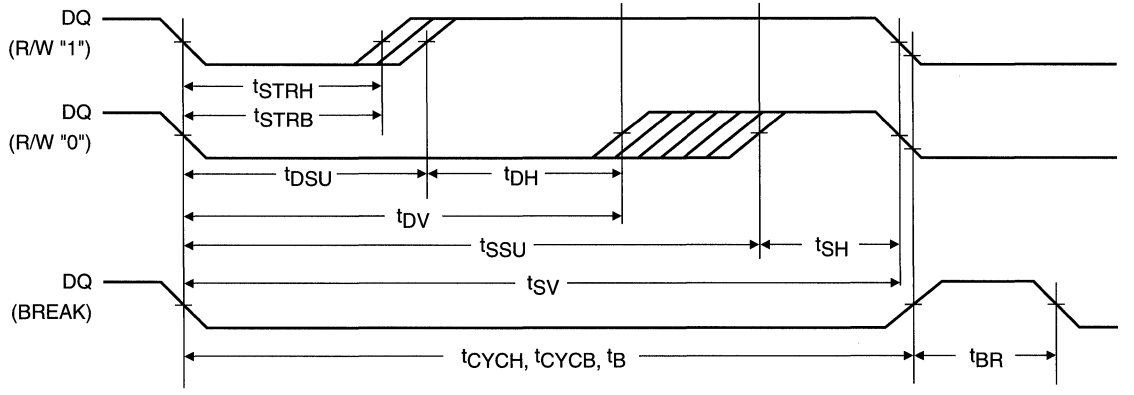
17/19

Serial Communication Timing Specification

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2014	3	-	-	ms	See note
t_{CYCB}	Cycle time, bq2014 to host	3	-	6	ms	
t_{STRH}	Start hold, host to bq2014	5	-	-	ns	
t_{STRB}	Start hold, bq2014 to host	500	-	-	µs	
t_{DSU}	Data setup	-	-	750	µs	
t_{DH}	Data hold	750	-	-	µs	
t_{DV}	Data valid	1.50	-	-	ms	
t_{SSU}	Stop setup	-	-	2.25	ms	
t_{SH}	Stop hold	700	-	-	µs	
t_{SV}	Stop valid	2.95	-	-	ms	
t_B	Break	3	-	-	ms	
t_{BR}	Break recovery	1	-	-	ms	

Note: The open-drain DQ pin should be pulled to at least V_{CC} by the host system for proper DQ operation. DQ may be left floating if the serial interface is not used.

Serial Communication Timing Illustration



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Data Sheet Revision History

ChangeNo.	Page No.	Description	Nature of Change
1	1, 3, 5, 6, 7, 13, 15	Changed display mode	Relative display mode only
1	1, 17	DONE pin	Removed $PROG_6$
1	2, 17	DONE pin	Added: DONE pin must be pulled to V_{SS} with a 200KΩ resistor
1	6	Table 1	Removed $PROG_6$
1	7	DONE input	Was: NAC is set to 90%... Is: NAC is set to 94%...
1	8, Table 3	$PROG_5$ = Z	Was: $PROG_5$ = Z or H Is: $PROG_5$ = Z
2	8	Temperature Compensation table	Replaced
2	6	Table 2	Added V_{SR} definition
2	6	Valid charge definition	Added definition
2	14	Overload flag	Was: 0.5sec. after V_{SR}> -250mV Is: after V_{SR} = -150mV

Notes: Change 1 = Dec. 1994 B "Final" changes from Aug. 1994 A "Preliminary."
Change 2 = Dec. 1995 C from Dec. 1994 B.

Ordering Information

bq2014 _ _

Temperature Range:
blank = Commercial (0 to +70°C)
N = Industrial (-40 to +85°C)*

Package Option:
SN = 16-pin narrow SOIC

Device:
bq2014 Gas Gauge IC

* Contact factory for availability.

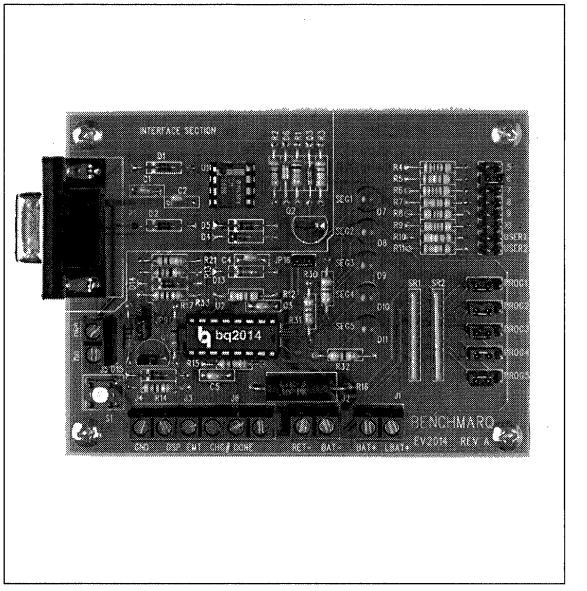
UNITRODE

Product Brief **EV2014**

bq2014 Evaluation Board

Features

- bq2014 Gas Gauge IC evaluation and development system
- PC interface hardware for easy access to state-of-charge information via the serial port
- Alternative terminal block for direct connection to the serial port
- Battery state-of-charge monitoring for 5- to 10-cell (series) applications (2 user-selectable options for 3, 4, or greater than 10 cells)
- On-board regulator for greater than 4-cell applications
- State-of-charge information displayed on bank of 5 LEDs
- Nominal capacity jumper-configurable
- Cell chemistry jumper-configurable



General Description

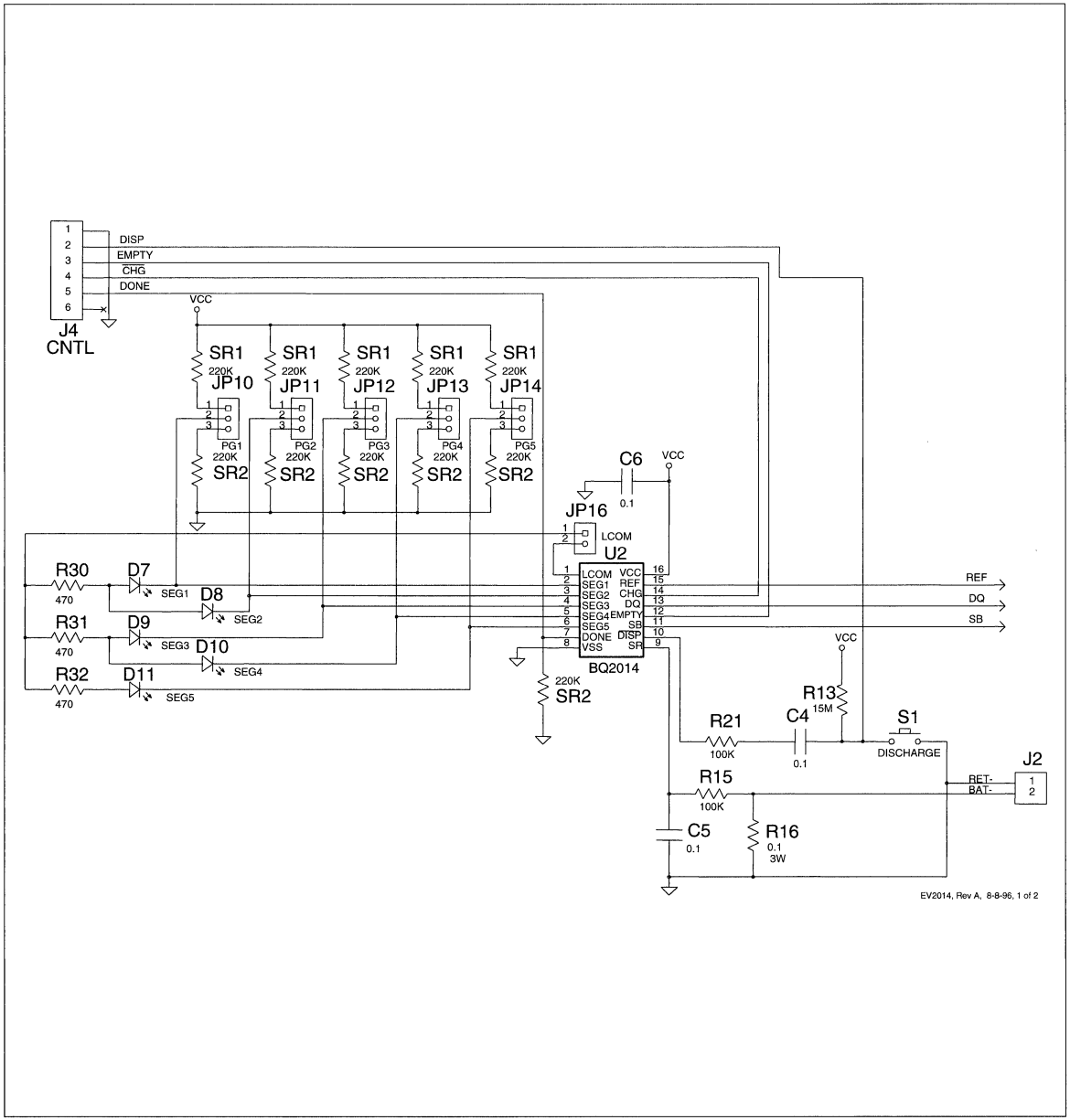
The EV2014 evaluation system provides a development and evaluation environment for the bq2014 Gas Gauge IC. The EV2014 incorporates a bq2014, a sense resistor, and all other hardware necessary to provide a capacity monitoring functiion for 3 to 12 series NiCd or NiMH cells.

Hardware for an PC interface is included on the EV2014 so that easy access to the battery state-of-charge information can be achieved via the serial port of the bq2014. Direct connection to the serial port of the bq2014 is also made available for check-out of the final hardware/software implementation.

The menu-driven software provided with the EV2014 displays charge/discharge activity and allows user interface to the bq2014 from any standard DOS PC.

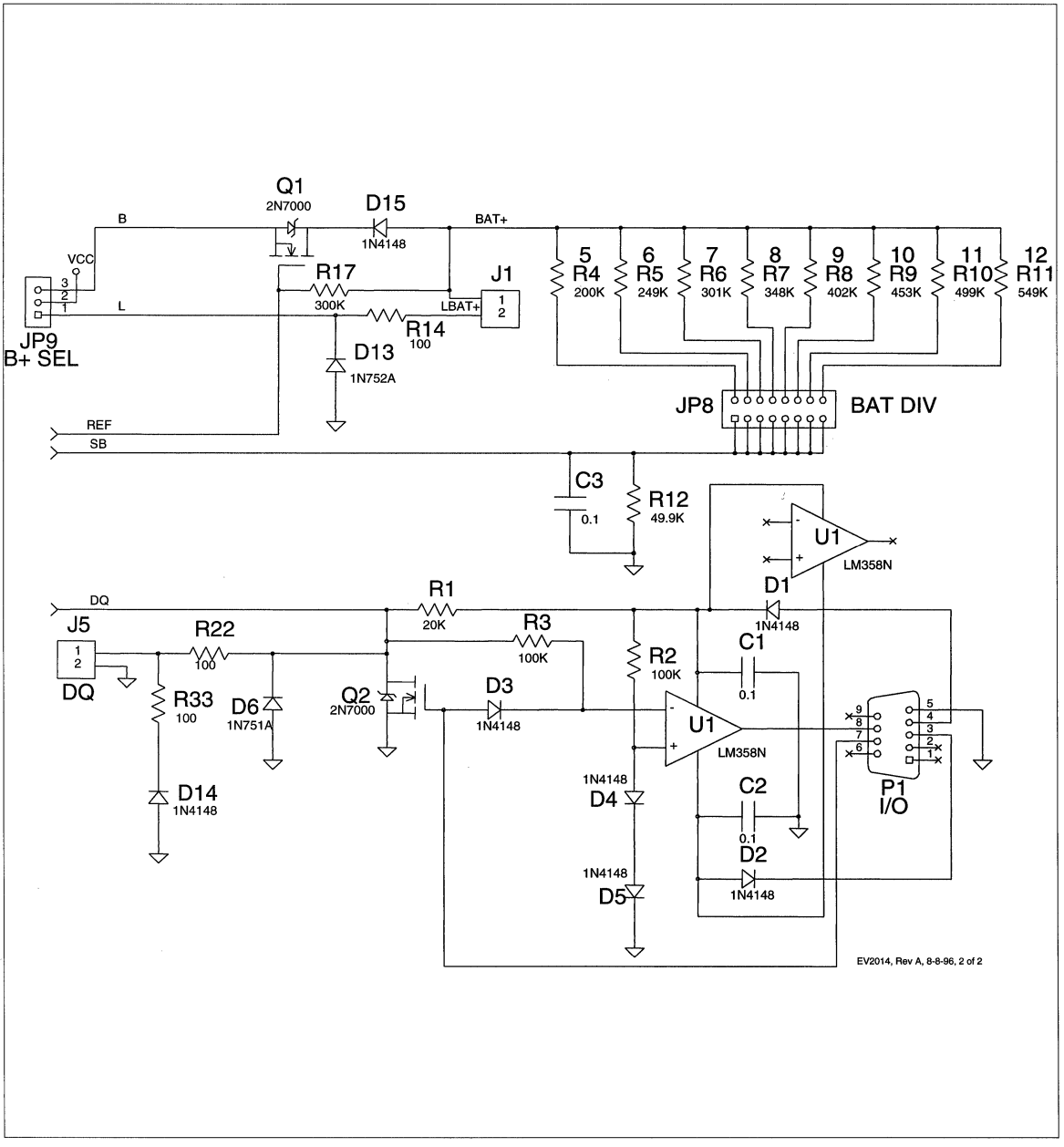
A full data sheet for this product is available on the Unitrode web site, or you may contact the factory for one.

EV2014 Board Schematic



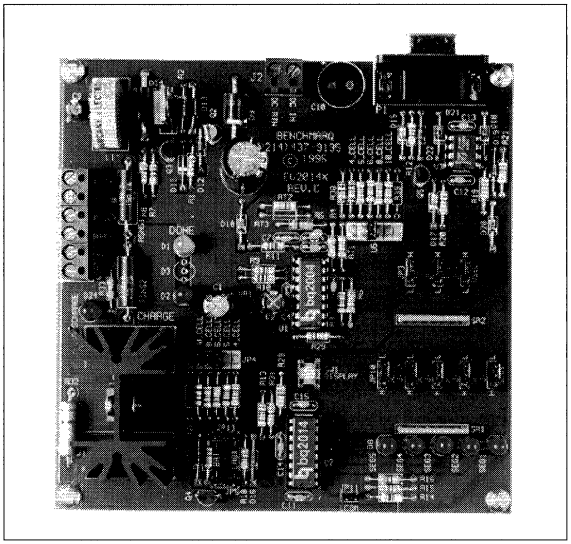
Rev. A Board

EV2014 Board Schematic (Continued)



Rev. A Board

Gas Gauge and Fast Charge Evaluation System



Features

- bq2014 Gas Gauge and bq2004 Fast Charge evaluation and development system
- Battery state-of-charge monitoring and fast charge control of four to ten NiCd or NiMH cells
- Charge current sourced from an on-board switch-mode regulator (up to 3.0A)
- Fast charge termination by $\Delta T/\Delta t$, $-\Delta V$, PVD, maximum temperature, maximum time, and maximum voltage
- PC interface hardware for easy access to state-of-charge information
- Nominal capacity and cell chemistry are jumper configurable

General Description

The EV2014x evaluation system provides a development and evaluation environment for the bq2014 Gas Gauge IC and the bq2004 Fast Charge IC. The EV2014x incorporates a bq2014, a bq2004, and all the external components required to reliably fast charge and accurately monitor the capacity of four to ten NiCd or NiMH cells.

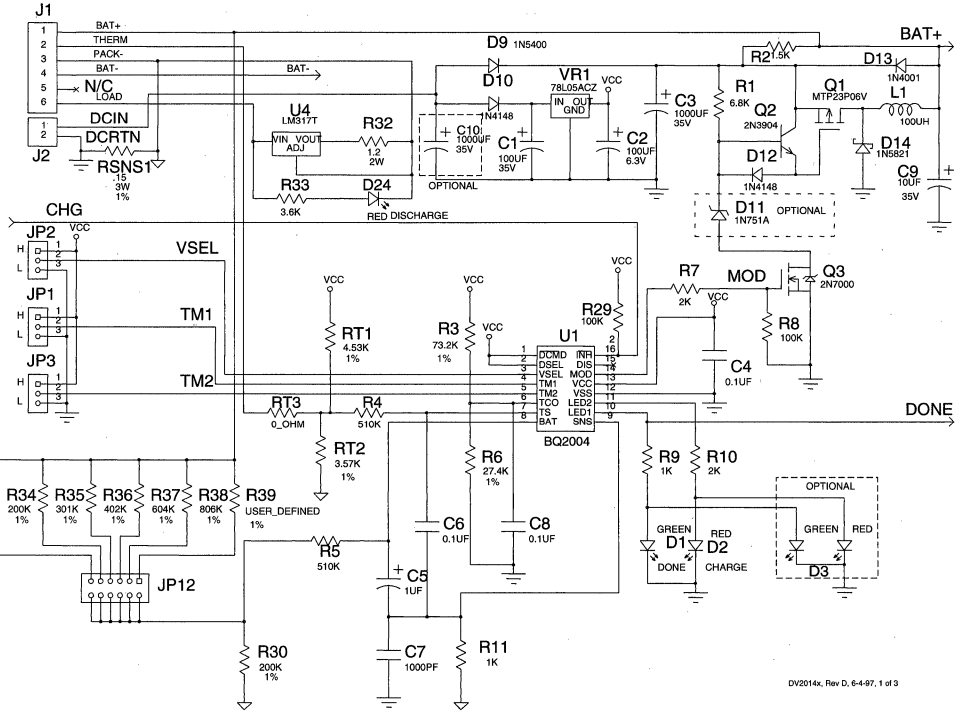
The bq2004 regulates the fast charge current. Fast charge is terminated by any of the following: $\Delta T/\Delta t$ (the rate of change in temperature versus time), $-\Delta V$ (negative voltage change) or PVD (peak voltage detect), maximum temperature, maximum time, and maximum voltage. The board provides a direct connection for an NTC thermistor. Jumper settings select the voltage termination mode, the termination hold-off time, top-off, and maximum charge time limits.

The EV2014x includes a PC interface for easy access to the battery state of charge information via the serial port of the bq2014. The menu-driven gas gauge software provided displays charge/discharge activity and allows user interface to the bq2014 from any standard DOS PC.

The user supplies the power supply and the batteries. The user configures the EV2014x board for the number of cells, nominal battery capacity, and cell chemistry. On-board LEDs indicate charging status and remaining capacity. The capacity LEDs are activated by the push button switch.

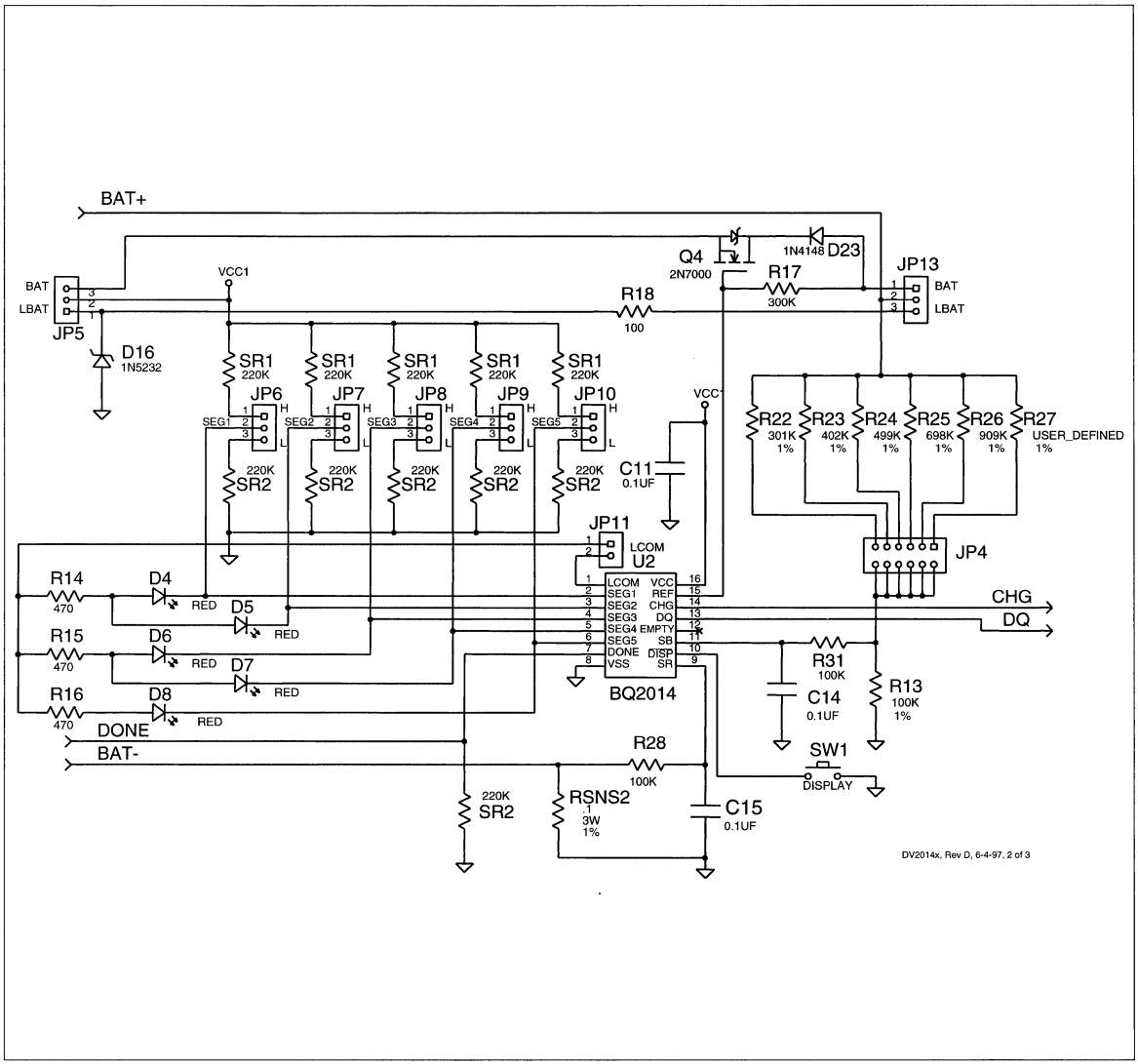
A full data sheet for this product is available on the Unitrode web site, or you may contact the factory for one.

EV2014x Board Schematic



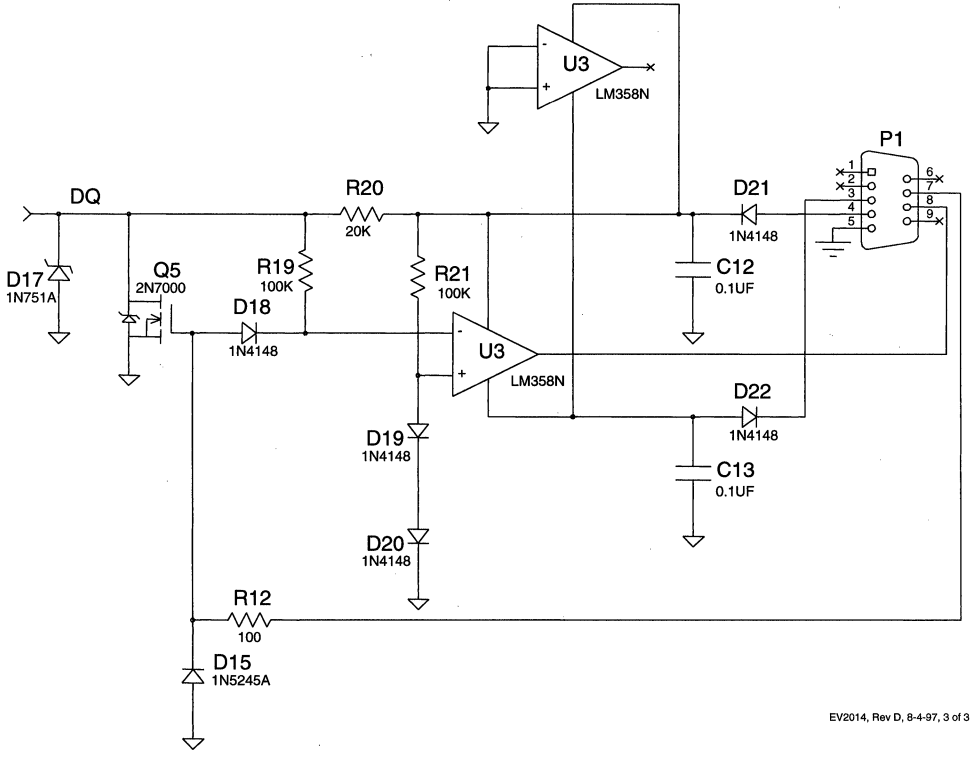
Rev. C Board

EV2014x Board Schematic (Continued)



Rev. C Board

EV2014x Board Schematic (Continued)



Rev. C. Board

Preliminary bq2014H

Low-Cost NiCd/NiMH Gas Gauge IC

Features

- Accurate measurement of available capacity in NiCd or NiMH batteries
- Low-cost battery management solution for pack integration
  - As little as ½ square inch of PCB for complete circuit
  - Low operating current (120µA typical)
  - Less than 100nA of data retention current
- High-speed (5kb/s) single-wire communication interface (HDQ bus) for critical battery parameters
- Communication with an external charge controller such as the bq2004
- Direct drive of remaining capacity LEDs
- Automatic rate and temperature compensation of measurements
- 16-pin narrow SOIC

General Description

The bq2014H NiCd/NiMH Gas Gauge IC is intended for battery-pack or in-system installation to maintain an accurate record of available battery capacity. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery. Compensations for battery temperature, self-discharge, and rate of discharge are applied to the charge counter to provide available capacity information across a wide range of operating conditions. Battery capacity is automatically recalibrated, or "learned," in the course of a discharge cycle from full to empty.

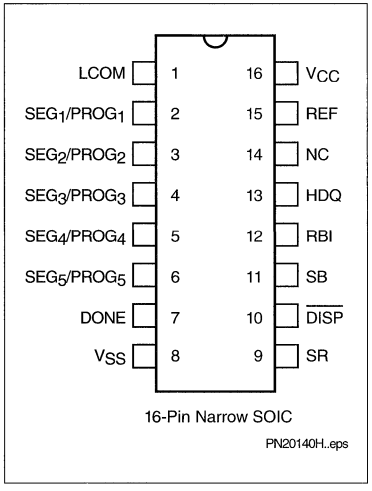
Nominal available capacity may be directly indicated using a five-segment LED display. The bq2014H also supports a simple single-line bidirectional serial link to an external processor (common ground). The 5kb/s HDQ bus interface reduces communications overhead in the external microcontroller.

Internal registers include available capacity and energy, temperature, voltage and current, and battery status. The external processor may also overwrite some of the bq2014H gas gauge data registers.

The bq2014H can operate from the batteries in the pack. The REF output and an external transistor allow a simple, inexpensive voltage regulator to supply power to the circuit from the cells.

4

Pin Connections



16-Pin Narrow SOIC

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Pin Names

LCOM	LED common output
$SEG_1/PROG_1$	LED segment 1/ program 1 input
$SEG_2/PROG_2$	LED segment 2/ program 2 input
$SEG_3/PROG_3$	LED segment 3/ program 3 input
$SEG_4/PROG_4$	LED segment 4/ program 4 input
$SEG_5/PROG_5$	LED segment 5/ program 5 input
DONE	Charge complete input
V_{SS}	System ground
SR	Sense resistor input
$\overline{DISP}$	Display control input
SB	Battery sense input
RBI	Register backup input
HDQ	Serial communications input/output
NC	No connect
REF	Voltage reference output
V_{CC}	Supply voltage

Pin Descriptions

LCOM **LED common output**

Open-drain output that switches V_{CC} to source current for the LEDs. The switch is off during initialization to allow reading of the soft pull-up or pull-down program resistors. LCOM is also high impedance when the display is off.

SEG_1–SEG_5 **LED display segment outputs (dual function with $PROG_1$–$PROG_5$)**

Outputs that each may activate an LED to sink the current sourced from LCOM.

$PROG_1$–$PROG_2$ **Programmed full count selection inputs (dual function with SEG_1–SEG_2)**

Three-level input pins that define the programmed full count (PFC) thresholds described in Table 2.

$PROG_3$–$PROG_4$ **Power gauge scale selection inputs (dual function with SEG_3–SEG_4)**

Three-level input pins that define the scale factor described in Table 2.

$PROG_5$ **Self-discharge rate selection (dual function with SEG_5)**

Three-level input pin that defines the self-discharge and battery-compensation factors as shown in Table 1.

DONE **Charge complete input**

Communicates the status of an external charge-controller such as the bq2004 Fast-Charge IC to the bq2014H. Note: This pin must be pulled down to V_{SS} using a 200kΩ resistor.

V_{SS} **Ground**

SR **Sense resistor input**

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret charge and discharge activity. $V_{SR} < V_{SS}$ indicates discharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2014H is $V_{SR} + V_{OS}$.

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ tied to V_{CC} allows $PROG_X$ to connect directly to V_{CC} or V_{SS} instead of through a pull-up or pull-down resistor. $\overline{DISP}$ floating allows the LED display to be active during charge. $\overline{DISP}$ low activates the display. See Table 1.

SB **Secondary battery input**

Monitors the battery cell-voltage potential through a high-impedance resistive divider network for end-of-discharge voltage (EDV) thresholds and for battery-removed detection.

RBI **Register backup input**

Provides backup potential to the bq2014H registers while $V_{CC} \leq 3V$. A storage capacitor or a battery can be connected to RBI.

HDQ **Serial communication input/output**

This is the open-drain bidirectional communications port.

NC **No connect**

REF **Voltage reference output**

REF provides a voltage reference output for an optional microregulator.

V_{CC} **Supply voltage input**

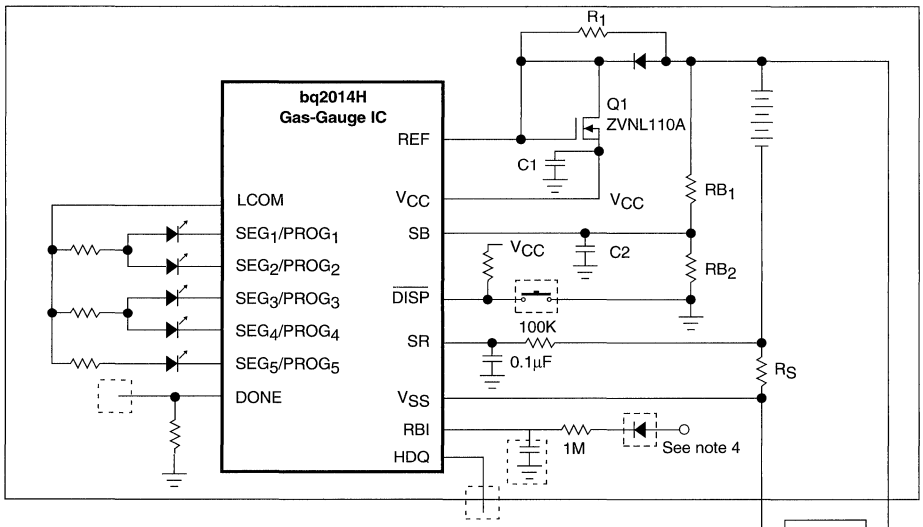
Functional Description

General Operation

The bq2014H determines battery capacity by monitoring the amount of current input to or removed from a rechargeable battery. The bq2014H measures discharge and charge currents, measures battery voltage, estimates self-discharge, monitors the battery for low battery-voltage thresholds, and compensates for temperature and charge/discharge rate. Current measurement is made by monitoring the voltage across a small-value series sense resistor between the negative battery terminal and ground. The bq2014H compensates the nominal available capacity register for discharge rate and temperature and reports the compensated available capacity. The bq2014H uses the compensated available capacity to drive the LED display. In addition, the bq2014H estimates the available energy using the average battery voltage during the discharge cycle and remaining compensated available capacity.

Figure 1 shows a typical battery pack application of the bq2014H using the LED display capability as a charge-state indicator. The bq2014H is configured to display capacity in relative display mode. The relative display mode uses the last measured discharge capacity of the battery as the battery "full" reference. A push-button display feature is available for momentarily enabling the LED display.

The bq2014H monitors the charge and discharge currents as a voltage across a sense resistor. (See R_S in Figure 1.) A filter between the negative battery terminal and the SR pin is required.



Notes:

1. [ ] Indicates optional.
2. Programming resistors (5 max.) and ESD-protection diodes are not shown.
3. RC on SR is required.
4. A series diode is required on RBI if the bottom series cell is used as the backup source. If the cell is used, the backup capacitor is not required, and the anode is connected to the positive terminal of the cell.

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Figure 1. Battery Pack Application Diagram—LED Display

3/21

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2014H monitors the battery potential through the SB pin for the end-of-discharge voltage (EDV) thresholds.

The EDV threshold levels are used to determine when the battery has reached an "empty" state.

The EDV thresholds for the bq2014H are programmable with the default values fixed as follows:

EDV1 (first) = 0.76V

EDVF (final) = EDV1 - 0.025V = 0.735V

The battery voltage divider (RB1 and RB2 in Figure 1) is used to scale these values to the desired threshold.

If V_{SB} is below either of the two EDV thresholds, the associated flag is latched and remains latched, independent of V_{SB}, until the next valid charge.

EDV monitoring is disabled if the discharge rate is greater than 2C (OVLD Flag = 1) and resumes ½ second after the rate falls below 2C. The V_{SB} value is available over the serial port.

RBI Input

The RBI input pin is used with a storage capacitor or external supply to provide backup potential to the internal bq2014H registers when V_{CC} drops below 3.0V. V_{CC} is output on RBI when V_{CC} is above 3.0V. If using an external supply (such as the bottom series cell) as the backup source, an external diode is required for isolation.

Reset

The bq2014H can be reset by removing V_{CC} and grounding the RBI pin for 15 seconds or by commands over the serial port. The serial port reset command sequence requires writing 00h to register PPFC (address = 1Eh) and then writing 00h to register LMD (address = 05h).

Temperature

The bq2014H internally determines the temperature in 10°C steps centered from approximately -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available charge display translation.

The temperature range is available over the serial port in 10°C increments, as shown in the following table

TMP (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2014H measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small-signal ground causes undesirable noise on the small-signal nodes. Additionally:

- The capacitors (C1 and C2) should be placed as close as possible to the V_{CC} and SB pins, respectively, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µF is recommended for V_{CC}.
- The sense-resistor capacitor should be placed as close as possible to the SR pin.
- The sense resistor (R_S) should be as close as possible to the bq2014H.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2014H. The bq2014H accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. The accumulated charge and discharge currents are adjusted for temperature and rate to provide the indication of compensated available capacity to the host system or user.

The main counter, Nominal Available Capacity (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2014H adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity equals the Programmed Full Count (PFC) shown in Table 2. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. **Last Measured Discharge (LMD) or learned battery capacity:**

   LMD is the last measured discharge capacity of the battery. On initialization (application of V_{CC} or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

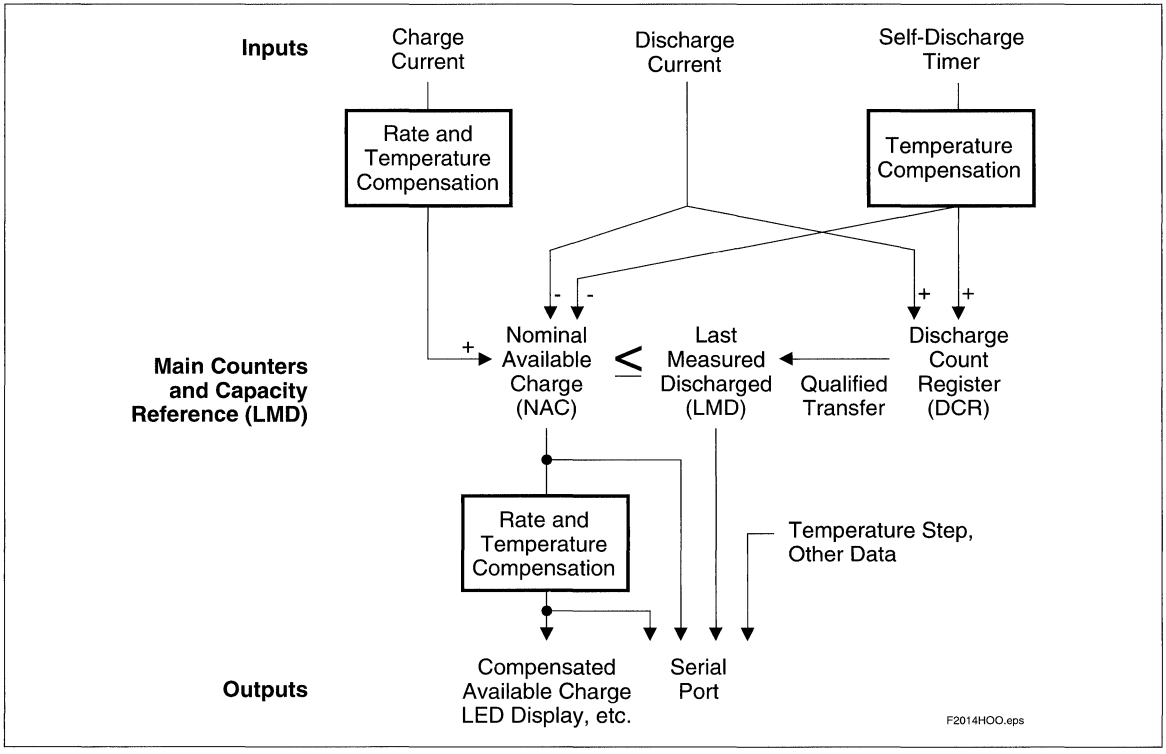


Figure 2. Operational Overview

5/21

2. Programmed Full Count (PFC) or initial battery capacity:

The initial LMD and gas gauge rate values are programmed by using $PROG_1$–$PROG_4$. The bq2014H is configured for a given application by selecting a PFC value from Table 2. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

Battery capacity (mAh) * sense resistor (Ω) =

PFC (mVh)

Selecting a PFC slightly less than the rated capacity provides a conservative capacity reference until the bq2014H "learns" a new capacity reference.

Example: Selecting a PFC Value

Given:

Sense resistor = 0.05Ω
Number of cells = 10
Capacity = 3500mAh, NiMH
Current range = 50mA to 1A
Relative display mode
Self-discharge = $NAC/_{47}$ per day @ 25°C
Voltage drop over sense resistor = 2.5mV to 50mV
Nominal discharge voltage = 1.2V

Therefore:

3500mAh * 0.05Ω = 175mVh

Table 1. Self-Discharge and Capacity Compensation

Pin Connection	$PROG_5$ Self-Discharge Rate	$\overline{DISP}$ Display State
H	Disabled	LEDs disabled
Z	$NAC/_{64}$	LEDs on when charging
L	$NAC/_{47}$	LEDs on for 4s

Table 2. bq2014H Programmed Full Count mVh, V_{SR} Gain Selections

$PROG_x$		Programmed Full Count (PFC)	$PROG_4$ = L			$PROG_4$ = Z or H			Units
1	2		$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	
-	-	-	SCALE = 1/80	SCALE = 1/160	SCALE = 1/320	SCALE = 1/640	SCALE = 1/1280	SCALE = 1/2560	mVh/ count
H	H	49152	614	307	154	76.8	38.4	19.2	mVh
H	Z	45056	563	282	141	70.4	35.2	17.6	mVh
H	L	40960	512	256	128	64.0	32.0	16.0	mVh
Z	H	36864	461	230	115	57.6	28.8	14.4	mVh
Z	Z	33792	422	211	106	53.0	26.4	13.2	mVh
Z	L	30720	384	192	96.0	48.0	24.0	12.0	mVh
L	H	27648	346	173	86.4	43.2	21.6	10.8	mVh
L	Z	25600	320	160	80.0	40.0	20.0	10.0	mVh
L	L	22528	282	141	70.4	35.2	17.6	8.8	mVh
V_{SR} equivalent to 2 counts/s (nom.)			90	45	22.5	11.25	5.6	2.8	mV

Select:

PFC = 27648 counts or 173mVh
$PROG_1$ = low
$PROG_2$ = high
$PROG_3$ = float
$PROG_4$ = low
$PROG_5$ = low

The initial full battery capacity is 173mVh (3460mAh) until the bq2014H "learns" a new capacity with a qualified discharge from full to EDV1.

3. Nominal Available Capacity (NAC):

NAC counts up during charge to a maximum value of LMD and down during discharge and self-discharge to 0. NAC is reset to 0 on initialization and on the first valid charge following discharge to EDV1. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = LMD or 0.94 * LMD if T < 0°C.

4. Discharge Count Register (DCR):

The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC ≥ 0.94 * LMD and a discharge is detected. The DCR does not roll over but stops counting when it reaches FFh.

The DCR value becomes the new LMD value on the first charge after a valid discharge to V_{EDV1} if all the following conditions are met:

- No valid charge initiations (charges greater than 2 NAC updates where $V_{SRO} > V_{SRQ}$) occurred during the period between NAC ≥ 0.94 * LMD and EDV1.
- The self-discharge is less than 6.25% of NAC.
- The temperature is ≥ 0°C when the EDV1 level is reached during discharge.
- The discharge begins when NAC ≥ 0.94 * LMD.
- VDQ is set.

The valid discharge flag (VDQ) indicates whether the present discharge is valid for LMD update. If the DCR update value is less than 0.94 * LMD, LMD will only be modified by 0.94 * LMD. This prevents invalid DCR values from corrupting LMD.

5. Scaled Available Energy (SAE):

SAE is useful in determining the available energy within the battery, and may provide a more useful capacity reference in battery chemistries with sloped voltage profiles during discharge. SAE may be converted to an mWh value using the following formula:

$$E(mWh) = (SAEH * 256 + SAEL) * \frac{1.2 * SCALE * (R_{B1} + R_{B2})}{R_S * R_{B2}}$$

where R_{B1}, R_{B2}, and R_S are resistor values in ohms, as shown in Figure 1. SCALE is the selected scale from Table 2.

6. Compensated Available Capacity (CACT)

CACT counts similarly to NAC, but contains the available capacity compensated for discharge rate and temperature.

Charge Counting

Charge activity is detected based on a positive voltage on the SR input. If charge activity is detected, the bq2014H increments NAC at a rate proportional to V_{SR} and, if enabled, activates the LED display.

The bq2014H counts charge activity when the voltage at the SR input (V_{SRO}) exceeds the minimum charge threshold (V_{SRQ}). A valid charge is detected when NAC has been updated twice without discharging or reaching the digital magnitude filter time-out. Once a valid charge is detected, charge counting continues until V_{SR}, including offset, falls below V_{SRQ}.

Discharge Counting

Discharge activity is indicated by a negative voltage on the SR input. All discharge counts where V_{SRO} is less than the minimum discharge threshold (V_{SRD}) cause the NAC register to decrement and the DCR to increment.

Self-Discharge Counting

The bq2014H continuously decrements NAC and increments DCR for self-discharge on the basis of time and temperature.

Charge/Discharge Current

The bq2014H current-scale registers, VSRH and VSRL, can be used to determine the battery charge or discharge current. See the Current Scale Register description for details.

Count Compensations

Charge Compensation

Two charge efficiency compensation factors are used for trickle and fast charge. Trickle charge is defined as a rate of charge < C/3. The compensation defaults to the fast-charge factor until the actual charge rate is determined.

Temperature adapts the charge rate compensation factors over two ranges between nominal and hot temperatures. The compensation factors are shown below.

Charge Temperature	Trickle-Charge Compensation	Fast-Charge Compensation
< 40°C	0.81	0.94
> 40°C	0.75	0.88

Compensated Available Capacity

NAC is adjusted for rate of discharge and temperature to derive the CACD and CACT values.

Corrections for the rate of discharge are made by adjusting an internal discharge compensation factor. The discharge factor is based on the discharge rate. This compensation is applied to NAC to derive the value in the CACD register.

The compensation factors during discharge are:

Approximate Discharge Rate	Rate Efficiency Factor
< 2C	100%
> 2C	95%

Temperature compensation during discharge also takes place. At lower temperatures, the compensation factor increases by 0.05 for each 10°C temperature range below 10°C. This compensation is applied to CACD to derive the value in the CACT register. The temperature compensation factor follows the equation

Temperature Efficiency Factor = 1.00 - (0.05 * N)

where N = number of 10°C steps below 10°C.

For example,

T > 10°C: Nominal compensation, N = 0

0°C < T < 10°C: N = 1 (temperature efficiency = 95%)

-10°C < T < 0°C: N = 2 (temperature efficiency = 90%)

-20°C < T < -10°C: N = 3 (temperature efficiency = 85%)

-20°C < T < -30°C: N = 4 (temperature efficiency = 80%)

8/21

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of $1/64$ * NAC per day, $1/47$ * NAC per day, or disabled. This is the rate for a battery within the 20°C–30°C temperature range (TMPGG = 6x). This rate varies across 8 ranges from <10°C to >70°C, doubling with each higher temperature step (10°C). See Table 3.

Table 3. Self-Discharge Compensation

Temperature Step	Typical Rate	
	$PROG_5$ = Z	$PROG_5$ = L
< 10°C	NAC/256	NAC/188
10–20°C	NAC/128	NAC/94
20–30°C	NAC/64	NAC/47
30–40°C	NAC/32	NAC/23.5
40–50°C	NAC/16	NAC/11.8
50–60°C	NAC/8	NAC/5.88
60–70°C	NAC/4	NAC/2.94
> 70°C	NAC/2	NAC/1.47

Digital Magnitude Filter

The bq2014H has a digital filter to eliminate charge and discharge counting below a set threshold. The threshold for both V_{SRD} and V_{SRQ} is 250µV.

Table 6. bq2014H Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

Error Summary

Capacity Inaccurate

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated. (See the DCR description.) The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

A Capacity Inaccurate counter (CPI) is maintained and incremented each time a valid charge occurs (qualified by NAC; see the CPI register description). It is reset whenever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

Current-Sensing Error

Table 6 shows the non-linearity and non-repeatability errors associated with the bq2014H current sensing.

Table 7 illustrates the current-sensing error as a function of V_{OS}. A digital filter prevents charge and discharge counts to the NAC register when V_{SRO} is between V_{SRQ} and V_{SRD}.

Table 7. V_{OS}-Related Current Sense Error (Current = 1A)

V_{OS} (µV)	Sense Resistor			
	20	50	100	mΩ
50	0.25	0.10	0.05	%
100	0.50	0.20	0.10	%
150	0.75	0.30	0.15	%
180	0.90	0.36	0.18	%

Done Input

A charge-control IC or a microcontroller uses the DONE input to communicate charge status to the bq2014H. When the DONE input is asserted high on charge completion, the bq2014H sets NAC = LMD and VDQ = 1. The DONE input should be maintained high as long as the charge controller or microcontroller keeps the batteries full; otherwise, the pin should be held low.

Communicating with the bq2014H

The bq2014H includes a simple single-pin (HDQ plus return) serial data interface. A host processor uses the interface to access various bq2014H registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain HDQ pin on the bq2014H should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, in which the host processor sends a command byte to the bq2014H. The command directs the bq2014H to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte. (See Figure 4.)

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 5K bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2014H may be sampled using the pulse-width capture timers available on some microcontrollers.

If a communication error occurs (e.g., t_{CYCB} > 250µs), the bq2014H should be sent a BREAK to reinitiate the serial interface. A BREAK is detected when the HDQ pin is driven to a logic-low state for a time, t_B or greater. The HDQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2014H is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections:

1. The first section is used to start the transmission by either the host or the bq2014H taking the HDQ pin to a logic-low state for a period, $t_{STRH;B}$.
2. The next section is the actual data transmission, where the data should be valid by a period, $t_{DSU;B}$, after the negative edge used to start communication. The data should be held for a period, $t_{DH;DV}$, to allow the host or bq2014H to sample the data bit.
3. The final section is used to stop the transmission by returning the HDQ pin to a logic-high state by at least a period, $t_{SSU;B}$, after the negative edge used to start communication. The final logic-high state should be until a period $t_{CYCH;B}$, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2014H is always performed with the bit transmitted first. Figure 5 shows an example of a communication sequence to read the bq2014H NACH register.

bq2014H Command Code and Registers

The bq2014H status registers are listed in Table 8 and described below. All registers are Read/Write in the bq2014H. **Caution: When writing to bq2014H registers ensure that proper data are written. A write-verify read is recommended.**

Command Code

The bq2014H latches the command code when eight valid command bits have been received by the bq2014H. The command code contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command code is used to select whether the received command is for a read or a write function:

The W/$\overline{R}$ values are

Command Code Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

where W/$\overline{R}$ is

0 The bq2014H outputs the requested register contents specified by the address portion of command code.

1 The following eight bits should be written to the register specified by the address portion of command code.

The lower 7-bit field of the command code contains the address portion of the register to be accessed:

Command Code Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Primary Status Flags Register (FLGS1)

The FLGS1 register (address = 01h) contains the primary bq2014H flags.

The ***charge status*** flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when $V_{SRO} > V_{SRQ}$. A V_{SRO} of less than V_{SRQ} or discharge activity clears CHGS.

The CHGS values are

FLGS1 Bits							
7	6	5	4	3	2	1	0
CHGS	-	-	-	-	-	-	-

where CHGS is

0 Either discharge activity detected or $V_{SRO} \leq V_{SRQ}$

1 $V_{SRO} > V_{SRQ}$

The ***battery replaced*** flag (BRP) is asserted whenever the bq2014H is reset either by application of V_{CC} or by a serial port command. BRP is reset when either a valid charge action increments NAC to be equal to LMD, or a valid charge action is detected after the EDV1 flag is asserted. BRP = 1 signifies that the device has been reset.

The BRP values are

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	BRP	-	-	-	-	-	-

where BRP is

0 Battery is charged until NAC = LMD or discharged until the EDV1 flag is asserted

1 bq2014H is reset

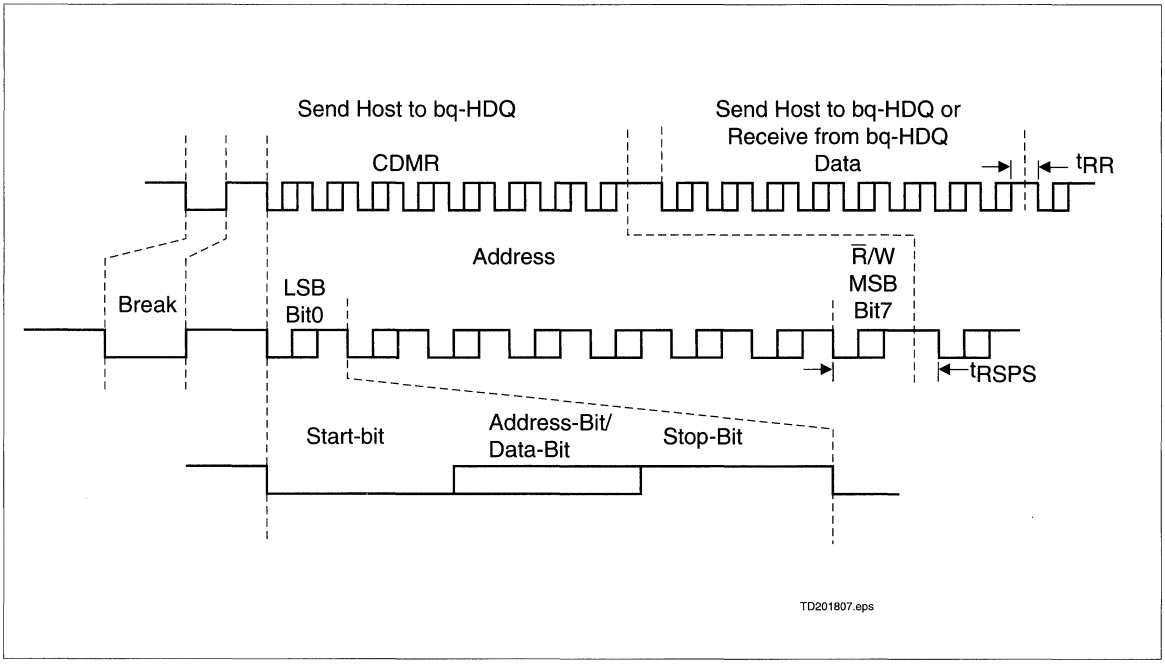


Figure 4. bq2014H Communication Example

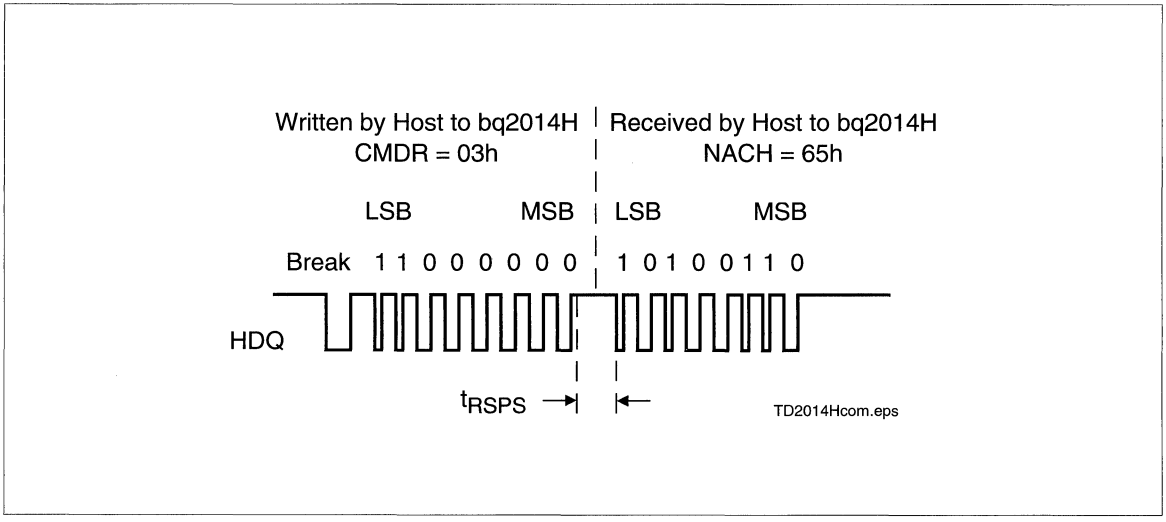


Figure 5. Typical Communication with the bq2014H

11/21

Table 8. bq2014H Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
FLGS1	Primary status flags register	01h	R	CHGS	BRP	0	CI	VDQ	1	EDV1	EDVF
TMP	Temperature register	02h	R	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available capacity high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	Nominal available capacity low byte register	17h	R/W	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	R	RSVD	DR2	DR1	DR0	ENINT	VQ	RSVD	OVLD
PPD	Program pin pull-down register	07h	R	RSVD	RSVD	RSVD	PPD5	PPD4	PPD3	PPD2	PPD1
PPU	Program pin pull-up register	08h	R	RSVD	RSVD	RSVD	PPU5	PPU4	PPU3	PPU2	PPU1
CPI	Capacity inaccurate count register	09h	R/W	CPI7	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	CPI0
VSB	Battery voltage register	0bh	R	VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0
VTS	End-of-discharge threshold select register	0ch	R/W	VTS7	VTS6	VTS5	VTS4	VTS3	VTS2	VTS1	VTS0
CACT	Temperature and discharge rate compensated available capacity	0dh	R/W	CACT7	CACT6	CACT5	CACT4	CACT3	CACT2	CACT1	CACT0
CACD	Discharge rate compensated available capacity	0eh	R/W	CACD7	CACD6	CACD5	CACD4	CACD3	CACD2	CACD1	CACD0
SAEH	Scaled available energy high byte register	0fh	R	SAEH7	SAEH6	SAEH5	SAEH4	SAEH3	SAEH2	SAEH1	SAEH0
SAEL	Scaled available energy low byte register	10h	R	SAEL7	SAEL6	SAEL5	SAEL4	SAEL3	SAEL2	SAEL1	SAEL0
RCAC	Relative CAC	11h	R	-	RCAC6	RCAC5	RCAC4	RCAC3	RCAC2	RCAC1	RCAC0
VSRH	Current scale high	12h	R	VSRH7	VSRH6	VSRH5	VSRH4	VSRH3	VSRH2	VSRH1	VSRH0
VSRL	Current scale low	13h	R	VSRL7	VSRL6	VSRL5	VSRL4	VSRL3	VSRL2	VSRL1	VSRL0
DCR	Discharge register	18h	R/W	DCR7	DCR6	DCR5	DCR4	DCR3	DCR2	DCR1	DCR0
PPFC	Program pin data	1eh	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
INTSS	V_{OS} Interrupt	38h	R/W	RSVD	RSVD	RSVD	RSVD	DCHGI	RSVD	RSVD	CHGI

Notes: RSVD = reserved.

All other registers not documented are reserved.

The ***capacity inaccurate*** flag (CI) is used to warn the user that the battery has been charged a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2014H is reset. The flag is cleared after an LMD update.

The CI values are

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	CI	-	-	-	-

where CI is

0 When LMD is updated with a valid full discharge

1 After the 64th valid charge action with no LMD updates or the bq2014H is reset

The ***valid discharge*** flag (VDQ) is asserted when the bq2014H is discharged from NAC = 0.94 * LMD. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- When NAC has been reduced by more than 6.25% because of self-discharge since VDQ was set.
- A valid charge action is sustained at $V_{SRO} > V_{SRQ}$ for at least 2 NAC updates.
- The EDV1 flag was set at a temperature below 0°C

The VDQ values are

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

where VDQ is

0 Self-discharge of more than 6.25% of NAC, valid charge action detected, EDV1 asserted with the temperature less than 0°C, or reset

1 On first discharge after NAC ≥ 0.94 * LMD

The ***first end-of-discharge warning*** flag (EDV1) warns the user that the battery is almost empty. The first segment pin, SEG_1, is modulated at a 4Hz rate if the display is enabled once EDV1 is asserted, which should warn the user that loss of battery power is imminent. The EDV1 flag is latched until a valid charge has been detected. The EDV1 threshold is externally controlled via the VTS register (see Voltage Threshold Register).

The EDV1 values are

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV1	-

where EDV1 is

0 Valid charge action detected, $V_{SB} \geq V_{TS}$

1 $V_{SB} < V_{TS}$ providing that the discharge rate is < 2C (OVLD not set)

The ***final end-of-discharge warning*** flag (EDVF) flag is used to warn that battery power is at a failure condition. All segment drivers are turned off. The EDVF flag is latched until a valid charge has been detected. The EDVF threshold is set 25mV below the EDV1 threshold.

The EDVF values are

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	EDVF

where EDVF is

0 Valid charge action detected, $V_{SB} \geq (V_{TS} - 25mV)$

1 $V_{SB} < (V_{TS} - 25mV)$ providing the discharge rate is < 2C

Temperature Register (TMP)

The TMP register (address=02h) contains the battery temperature.

The bq2014H contains an internal temperature sensor. The temperature is used to set charge and discharge efficiency factors as well as to adjust the self-discharge coefficient. The temperature register contents may be translated as shown in Table 9.

TMP Temperature Bits							
7	6	5	4	3	2	1	0
TMP3	TMP2	TMP1	TMP0	-	-	-	-

The bq2014H calculates the gas gauge bits, GG3-GG0 as a function of CACT and LMD. The results of the calculation give available capacity in $1/16$ increments from 0 to $15/16$.

TMP Gas Gauge Bits							
7	6	5	4	3	2	1	0
-	-	-	-	GG3	GG2	GG1	GG0

Table 9. Temperature Register

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

Nominal Available Capacity Registers (NACH/NACL)

The NACH high-byte register (address=03h) and the NACL low-byte register (address=17h) are the main gas gauging registers for the bq2014H. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. NACH and NACL are set to 0 during a bq2014H reset.

Writing to the NAC registers affects the available charge counts and, therefore, affects the bq2014H gas gauge operation. Do not write the NAC registers to a value greater than LMD.

Battery Identification Register (BATID)

The BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V_{RBI} is greater than 2V. The contents of BATID have no effect on the operation of the bq2014H. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is the register (address=05h) that the bq2014H uses as a measured full reference. The bq2014H adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2014H updates the capacity of the battery. LMD is set to PFC during a bq2014H reset.

LMD is set to DCR upon the first valid charge after EDV is set if VDQ is set.

If DCR < 0.94 LMD, then LMD is set to 0.94 * LMD.

Secondary Status Flags Register (FLGS2)

The FLGS2 register (address=06h) contains the secondary bq2014H flags.

Bit 7 and bit 1 of FLGS2 are reserved. Do not write to these bits.

The ***discharge rate*** flags, DR2–0, are bits 6–4.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-	-	-	

They are used to determine the current discharge regime as follows:

DR2	DR1	DR0	Discharge Rate
0	0	0	DRATE < 0.5C
0	0	1	0.5C ≤ DRATE < 2C
0	1	0	2C < DRATE

The ***enable interrupt*** flag (ENINT) is a test bit used to determine V_{SR} activity sensed by the bq2014H. The state of this bit will vary and should be ignored by the system.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	ENINT	-	-	

The ***valid charge*** flag (VQ), bit 2 of FLGS2, is used to indicate whether the bq2014H recognizes a valid charge condition. This bit is reset on the first discharge after NAC = LMD.

The VQ values are

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	VQ	-	

where VQ is

0 Valid charge action not detected between a discharge from NAC = LMD and EDV1

1 Valid charge action detected

The ***overload*** flag (OVLD) is asserted when a discharge rate in excess of 2C is detected. OVLD remains asserted as long as the condition persists and is cleared 0.5 seconds after the rate drops below 2C. The overload condition is used to stop sampling of the battery terminal characteristics for end-of-discharge determination.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OVLD

Program Pin Pull-Down Register (PPD)

The PPD register (address=07h) contains some of the programming pin information for the bq2014H. The segment drivers, SEG_{1-5}, have a corresponding PPD register location, PPD_{1-5}. A given location is set if a pull-down resistor has been detected on its corresponding segment driver. For example, if SEG_1 and SEG_4 have pull-down resistors, the contents of PPD are xxx01001.

Program Pin Pull-Up Register (PPU)

The PPU register (address=08h) contains the rest of the programming pin information for the bq2014H. The segment drivers, SEG_{1-5}, have a corresponding PPU register location, PPU_{1-5}. A given location is set if a pull-up resistor has been detected on its corresponding segment driver. For example, if SEG_3 and SEG_5 have pull-up resistors, the contents of PPU are xxx10100.

PPD/PPU Bits							
7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	PPU_5	PPU_4	PPU_3	PPU_2	PPU_1
RSVD	RSVD	RSVD	PPD_5	PPD_4	PPD_3	PPD_2	PPD_1

Capacity Inaccurate Count Register (CPI)

The CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2014H adapts to the changing capacity over time. A complete discharge from full (NAC ≥ 0.94 * LMD) to empty (EDV1=1) is required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and there has been no more than a 6% self-discharge reduction.

The CPI register is incremented every time a valid charge is detected. When NAC ≥ 0.94 * LMD, however, the CPI register increments on the first valid charge; CPI does not increment again for a valid charge until NAC < 0.94 * LMD. This prevents continuous trickle charging from incrementing CPI if self-discharge decrements NAC. The CPI register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. The CPI register is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

Battery Voltage Register (VSB)

The battery voltage register is used to read the single-cell battery voltage on the SB pin. The VSB register (address = 0Bh) is updated approximately once per second with the present value of the battery voltage.
$V_{SB} = 1.2V * (VSB/256)$.

VSB Register Bits							
7	6	5	4	3	2	1	0
VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0

Voltage Threshold Register (VTS)

The end-of-discharge threshold voltages (EDV1 and EDVF) can be set using the VTS register (address = 0Ch). The VTS register sets the EDV1 trip point. EDVF is set 25mV below EDV1. The default value in the VTS register is A2h, representing EDV1 = 0.76V and EDVF = 0.735V. EDV1 = 1.2V * (VTS/256).

VTS Register Bits							
7	6	5	4	3	2	1	0
VTS7	VTS6	VTS5	VTS4	VTS3	VTS2	VTS1	VTS0

Compensated Available Charge Registers (CACT/CACD)

The CACD register (address = 0Eh) contains the NAC value compensated for discharge rate. This is a monotonicly decreasing value during discharge. If the discharge rate is > 2C then this value is lower than NAC. CACD is updated only when the discharge rate compensated NAC value is a lower value than CACD during discharge. During charge, CACD is continuously updated with the NAC value.

The CACT register (address = 0Dh) contains the CACD value compensated for temperature. CACT will contain a value lower than CACD when the battery temperature is below 10°C. The CACT value is also used in calculating the LED display pattern.

Scaled Available Energy Registers (SAEH/SAEL)

The SAEH high-byte register (address = 0Fh) and the SAEL low-byte register (address = 10h) are used to scale battery voltage and CACT to a value that can be translated to watt-hours remaining under the present conditions.

Relative CAC Register (RCAC)

The RCAC register (address = 11h) provides the relative battery state-of-charge by dividing CACT by LMD.

RCAC varies from 0 to 64h representing relative state-of-charge from 0 to 100%.

Current Scale Register (VSRH/VSRL)

The VSRH register (address = 12h) and the VSRL register (address = 13h) report the average signal across the SR and V_{SS} pins. The bq2050H updates this register pair every 22.5s. V_{SRH} (high-byte) and V_{SRL} (low-byte) form a 16-bit signed integer value representing the average current during this time. The battery pack current can be calculated from:

$$|I(mA)| = (V_{SRH} * 256 + V_{SRL})/(8 * R_S)$$

where:

R_S = sense resistor value in Ω.
V_{SRH} = high-byte value of battery current
V_{SRL} = low-byte value of battery current

The bq2014H indicates an average discharge current with a "1" in the MSB position of the VSRH register. To calculate discharge current, use the 2's complement if the concatenated register contents in the above equation.

Discharge Count Register (DCR)

The DCR register (address = 18h) stores the high-byte of the discharge count. DCR is reset to zero at the start of a valid discharge cycle and can count to a maximum of FFh. DCR will not increment if EDV1 = 1 and will not roll over from FFh.

Program Pin Full Count (PPFC)

The PPFC register contains information concerning the program pin configuration. This information is used to determine the data integrity of the bq2014H. **The only approved user application for this register is to write a zero to this register as part of a reset request.**

The recommended reset method for the bq2014H is

- Write PPFC to zero
- Write LMD to zero

After these operations, a software reset will occur.

Resetting the bq2014H sets the following:

- LMD = PFC
- CPI, VDQ, RCAC, NACH/L, CACH/L, SAEH/L, NMCV = 0
- CI and BRP = 1

Voltage Offset (V_{OS}) Interrupt (INTSS)

The INTSS register (address = 38h) is useful during intial characterization of bq2014H designs. When the bq2014H counts a charge pulse, CHGI (bit 0) will be set to 1. When the bq2014H counts a discharge pulse, DCHGI (bit 3) will be set to 1. All other locations in the INTSS register are reserved.

Display

The bq2014H can directly display capacity information using low-power LEDs. If LEDs are used, the program pins should be resistively tied to V_{CC} or V_{SS} for a program high or program low, respectively.

The bq2014H displays the battery charge state in relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD.

The capacity display is also adjusted for the present battery temperature and discharge rate. The temperature adjustment reflects the available capacity at a given temperature but does not affect the NAC register. The temperature adjustments are detailed in the CACT and CACD register descriptions.

When $\overline{DISP}$ is tied to V_{CC}, the SEG_{1-5} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active whenever the bq2014H detects a charge in progress $V_{SRO} > V_{SRQ}$. When pulled low, the segment outputs become active for a period of four seconds, ± 0.5 seconds.

The segment outputs are modulated as two banks, with segments 1, 3, and 5 alternating with segments 2 and 4. The segment outputs are modulated at approximately 100Hz with each segment bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV1} (EDV1 = 1), indicating a low-battery condition. V_{SB} below V_{EDVF} (EDVF = 1) disables the display output.

Microregulator

A micropower source for the bq2014H can be inexpensively built using a FET and an external resistor. (See Figure 1.)

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
REF	Relative to V_{SS}	-0.3	+8.5	V	Current limited by R1 (see Figure 1)
V_{SR}	Relative to V_{SS}	-0.3	Vcc+0.7	V	100kΩ series resistor should be used to protect SR in case of a shorted battery.
T_{OPR}	Operating temperature	0	+70	°C	Commercial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDV1}	First empty warning	0.73	0.76	0.79	V	SB, default
V_{EDVF}	Final empty warning	V_{EDV1} - 0.035	V_{EDV1} - 0.025	V_{EDV1} - 0.015	V	SB, default
V_{SRO}	SR sense range	-300	-	+500	mV	SR, $V_{SR} + V_{OS}$
V_{SRQ}	Valid charge	250	-	-	µV	$V_{SR} + V_{OS}$ (see note)
V_{SRD}	Valid discharge	-	-	-250	µV	$V_{SR} + V_{OS}$ (see note)

Note: V_{OS} is affected by PC board layout. Proper layout guidelines should be followed for optimal performance. See "LayoutConsiderations."

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{OS}	Offset referred to V_{SR}	-	±50	±150	µV	$\overline{DISP}$ = VCC
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V, HDQ = 0
		-	120	180	µA	V_{CC} = 4.25V, HDQ = 0
		-	170	250	µA	V_{CC} = 6.5V, HDQ = 0
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	0 < V_{SB} < V_{CC}
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	V_{DISP} = V_{SS}
I_{LCOM}	LCOM input leakage	-0.2	-	0.2	µA	$\overline{DISP}$ = V_{CC}
I_{RBI}	RBI data retention current	-	-	100	nA	V_{RBI} > V_{CC} < 3V
R_{HDQ}	Internal pulldown	500	-	-	KΩ	
R_{SR}	SR input impedance	10	-	-	MΩ	-200mV < V_{SR} < V_{CC}
V_{IHPFC}	Logic input high	V_{CC} - 0.2	-	-	V	$PROG_{1–5}$
V_{ILPFC}	Logic input low	-	-	V_{SS} + 0.2	V	$PROG_{1–5}$
V_{IZPFC}	Logic input Z	float	-	float	V	$PROG_{1–5}$
V_{OLSL}	SEG output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, I_{OLS} ≤ 1.75mA SEG_1–SEG_5
V_{OLSH}	SEG output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, I_{OLS} ≤ 11.0mA SEG_1–SEG_5
V_{OHML}	LCOM output high, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{OHLCOM} = -5.25mA
V_{OHMH}	LCOM output high, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} > 3.5V, I_{OHLCOM} = -33.0mA
I_{OLS}	SEG sink current	11.0	-	-	mA	At V_{OLSH} = 0.4V, V_{CC} = 6.5V
I_{OL}	Open-drain sink current	5.0	-	-	mA	At V_{OL} = V_{SS} + 0.3V, HDQ
V_{OL}	Open-drain output low	-	-	0.3	V	I_{OL} ≤ 5mA, HDQ
V_{IHDQ}	HDQ input high	2.5	-	-	V	HDQ
V_{ILDQ}	HDQ input low	-	-	0.8	V	HDQ
R_{PROG}	Soft pull-up or pull-down resistor value (for programming)	-	-	200	KΩ	$PROG_{1–5}$
R_{FLOAT}	Float state external impedance	-	5	-	MΩ	$PROG_{1–5}$

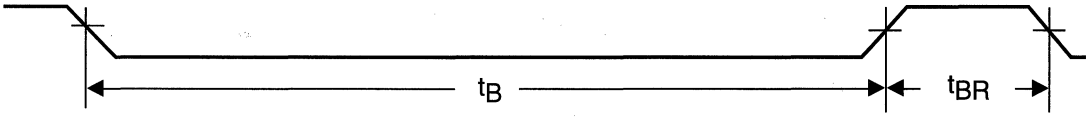
Note: All voltages relative to V_{SS}.

High-Speed Serial Communication Timing Specification ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2014H (write)	190	-	-	µs	See note
t_{CYCB}	Cycle time, bq2014H to host (read)	190	205	250	µs	
t_{STRH}	Start hold, host to bq2014H (write)	5	-	-	ns	
t_{STRB}	Start hold, bq2014H to host (read)	32	-	-	µs	
t_{DSU}	Data setup	-	-	50	µs	
t_{DSUB}	Data setup	-	-	50	µs	
t_{DH}	Data hold	90	-	-	µs	
t_{DV}	Data valid	-	-	80	µs	
t_{SSU}	Stop setup	-	-	145	µs	
t_{SSUB}	Stop setup	-	-	145	µs	
t_{RSPS}	Response time, bq2014H to host	190	-	320	µs	
t_B	Break	190	-	-	µs	
t_{BR}	Break recovery	40	-	-	µs	

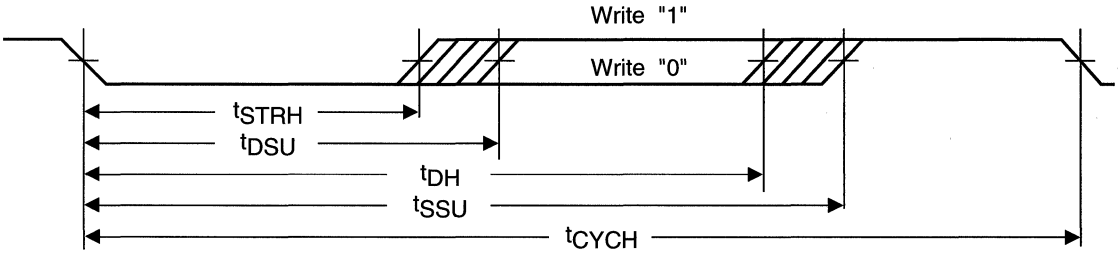
Note: The open-drain HDQ pin should be pulled to at least V_{CC} by the host system for proper HDQ operation. HDQ may be left floating if the serial interface is not used.

Break Timing

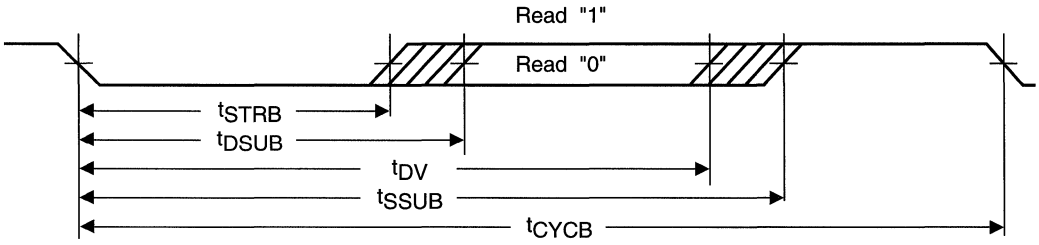


TD201803.eps

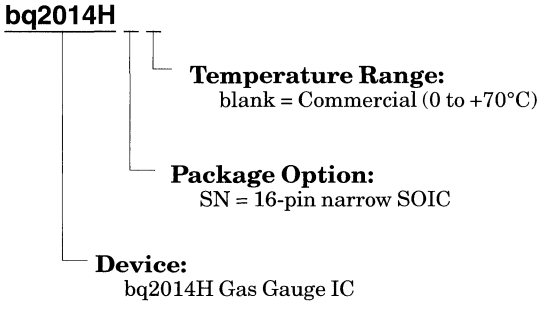
Host to bq2014H



bq2014H to Host



Ordering Information



UNITRODE

bq2018

Power Minder™ IC

Features

- Multifunction charge/discharge counter
- Resolves signals less than 12.5µV
- Internal offset calibration improves accuracy
- 1024 bits of NVRAM configured as 128 x 8
- Internal temperature sensor for self-discharge estimation
- Single-wire serial interface
- Dual operating modes:
  - Operating: <80µA
  - Sleep: <10µA
- REG output for low-cost microregulation
- Internal timebase eliminates external components
- 8-pin TSSOP or SOIC allows battery pack integration

General Description

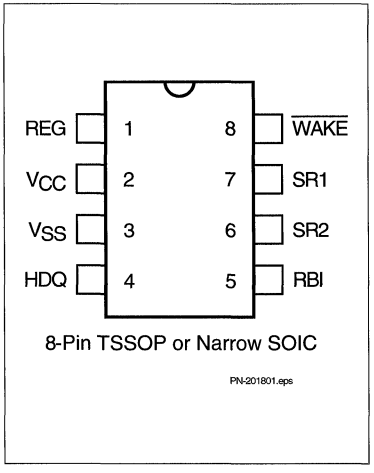
The bq2018 is a low-cost charge/discharge counter peripheral packaged in an 8-pin TSSOP or SOIC. It works with an intelligent host controller, providing state-of-charge information for rechargeable batteries.

The bq2018 measures the voltage drop across a low-value series sense resistor between the negative terminal of the battery and the battery pack ground contact. By using the accumulated counts in the charge, discharge, and self-discharge registers, an intelligent host controller can determine battery state-of-charge information. To improve accuracy, an offset count register is available. The system host controller is responsible for the register maintenance by resetting the charge in/out and self-discharge registers as needed.

The bq2018 also features 128 bytes of NVRAM registers. The upper 13 bytes of NVRAM contain the capacity monitoring and status information. The RBI input operates from an external power storage source such as a capacitor or a series cell in the battery pack, providing register nonvolatility for periods when the battery is shorted to ground or when the battery charge state is not sufficient to operate the bq2018. During this mode, the register backup current is less than 100nA.

Packaged in an 8-pin TSSOP or SOIC, the bq2018 is small enough to fit in the crevice between two A-size cells or within the width of a prismatic cell.

Pin Connections



8-Pin TSSOP or Narrow SOIC

PN-201801.eps

Pin Names

REG	Regulator output	$\overline{WAKE}$	Wake-up output
V_{CC}	Supply voltage input	SR1	Current sense input 1
V_{SS}	Ground	SR2	Current sense input 2
HDQ	Data input/output	RBI	Register backup input

Pin Descriptions

REG **Regulator output**

REG is the output of the operational transconductance amplifier (OTA) that drives an external pass n-channel JFET to provide an optional regulated supply. The supply is regulated at 3.7V nominal.

V_{CC} **Supply voltage input**

When regulated by the REG output, V_{CC} is 3.7V ±200mV. When the REG output is not used, the valid operating range is 2.8V to 5.5V.

V_{SS} **Ground**

SR1–SR2 **Current sense inputs**

The bq2018 interprets charge and discharge activity by monitoring and integrating the voltage drop (V_{SR}) across pins SR1 and SR2. The SR1 input connects to the sense resistor and the negative terminal of the battery. The SR2 input connects to the sense resistor and the negative terminal of the pack. $V_{SR1} < V_{SR2}$ indicates discharge, and $V_{SR1} > V_{SR2}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2018, is $V_{SR} + V_{OS}$. Valid input range is ± 200mV.

HDQ **Data input/output**

This bi-directional input/output communicates the register information to the host system. HDQ is open drain and requires a pullup/down resistor in the battery pack to disable/enable sleep mode if the pack is removed from the system.

RBI **Register backup input**

This input maintains the internal register states during periods when V_{CC} is below the minimum operating voltage.

$\overline{WAKE}$ **Wake-up output**

When asserted, this output is used to indicate that the charge or discharge activity is above a programmed minimal level.

Functional Description

General Operation

A host can use the bq2018 internal counters and timers to measure battery state-of-charge, estimate self-discharge, and calculate the average charge and discharge current into and out of a rechargeable battery. The bq2018 needs an external host system to perform all register maintenance. Using information from the bq2018, the system host can determine the battery state-of-charge, estimate self-discharge, and calculate the average charge and discharge currents. During pack storage periods, the use of an internal temperature sensor doubles the self-discharge count rate every 10° above 25°C.

To reduce cost, power to the bq2018 may be derived using a low-cost external FET in conjunction with the REG pin. The bq2018 operating current is less than 80µA. When the HDQ line remains low for greater than ten seconds and V_{SRO} ($V_{SR} + V_{OS}$ where V_{SR} is the voltage drop between SR1 and SR2 and V_{OS} is the offset voltage) is below the programmed minimal level ($\overline{WAKE}$ is in High Z), the bq2018 enters a sleep mode of <10µA where all operations are suspended. HDQ transitioning high reinitiates the bq2018.

A register is available to store the calculated offset, allowing current calibration. The offset cancellation register is written by the bq2018 during pack assembly and is available to the host system to adjust the current measurements. By adding or subtracting the offset value stored in the OFR, the true charge and discharge counts can be calculated to a high degree of certainty.

Figure 1 shows a block diagram of the bq2018, and Table 1 outlines the bq2018 operational states.

REG Output

The bq2018 can operate directly from three or four nickel-chemistry cells or a single Li-Ion cell as long as V_{CC} is limited to 2.8 to 5.5V. To facilitate the power supply requirements of the bq2018, a REG output is present to regulate an external low-threshold n-JFET. A micropower V_{CC} source for the bq2018 can inexpensively be built using this FET.

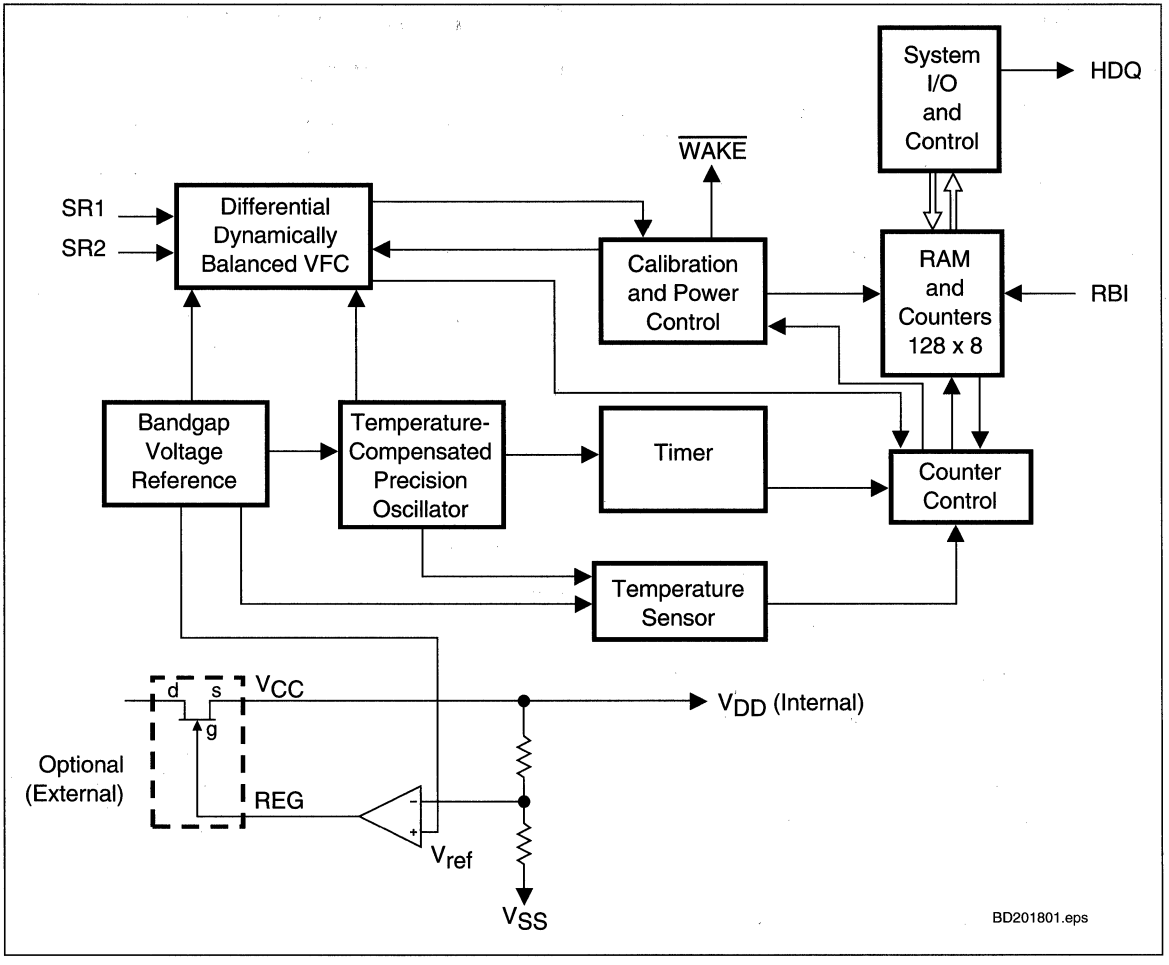


Figure 1. bq2018 Block Diagram

Table 1. Operational States

HDQ Pin	DCR/CCR/SCR	WOE	$\overline{\text{WAKE}}$	Operating State
HDQ High	yes	$\lvert V_{SRO} \rvert > V_{WOE}$	Low	Normal
HDQ High	yes	$\lvert V_{SRO} \rvert < V_{WOE}$	High Z	Normal
HDQ Low	no	$\lvert V_{SRO} \rvert < V_{WOE}$	High Z	Sleep

Note: V_{SRO} is the voltage difference between SR1 and SR2 plus the offset voltage V_{OS}.

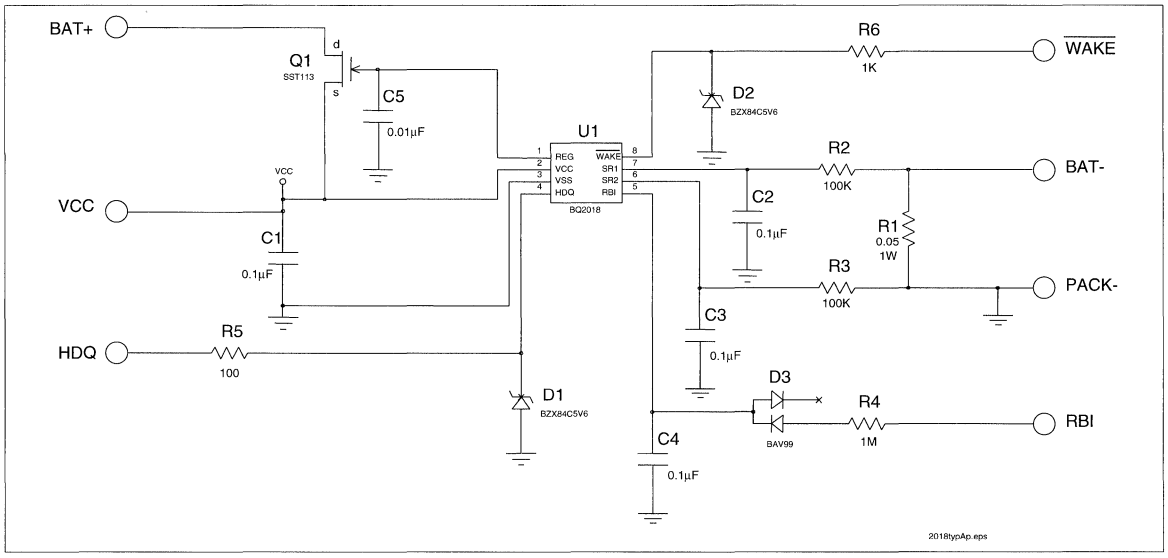


Figure 2. Typical Application

RBI Input

The RBI input pin is used with a storage capacitor or external supply to provide back-up potential to the internal RAM when V_{CC} drops below 2.4V. The maximum discharge current is 100nA in this mode. The bq2018 outputs V_{CC} on RBI when the supply is above 2.4V, so a diode is required to isolate an external supply.

Charge/Discharge Count Operation

Table 2 shows the main counters and registers of the bq2018. The bq2018 accumulates charge and discharge counts into two main count registers, the Discharge Count Register (DCR) and the Charge Count Register (CCR). The bq2018 produces charge and discharge counts by sensing the voltage difference across a low-value resistor between the negative terminal of the battery pack and the negative terminal of the battery. The DCR or CCR counts depending on the signal between SR1 and SR2.

During discharge, the DCR and the Discharge Time Counter (DTC) are active. If V_{SR1} is less than V_{SR2}, indicating a discharge, the DCR counts at a rate equivalent to 12.5µV every hour, and the DTC counts at a rate of 1 count/0.8789 seconds (4096 counts per 1 hour). For example, a -100mV signal produces 8000 DCR counts and 4096 DTC counts each hour. The amount of charge removed from the battery can easily be calculated.

Table 2. bq2018 Counters

Name	Description	Range	RAM Size
DCR	Discharge count register	$V_{SR1} < V_{SR2}$ (Max. =-200mV) 12.5µVh increments	16-bit
CCR	Charge count register	$V_{SR1} > V_{SR2}$ (Max. = +200mV) 12.5µVh increments	16-bit
SCR	Self-discharge count register	1 count/hour @ 25°C	16-bit
DTC	Discharge time counter	1 count/0.8789s default 1 count/225s if STD is set	16-bit
CTC	Charge time counter	1 count/0.8789s default 1 count/225s if STC is set	16-bit
MODE/ WOE	MODE/ Wake output enable	—	8-bit

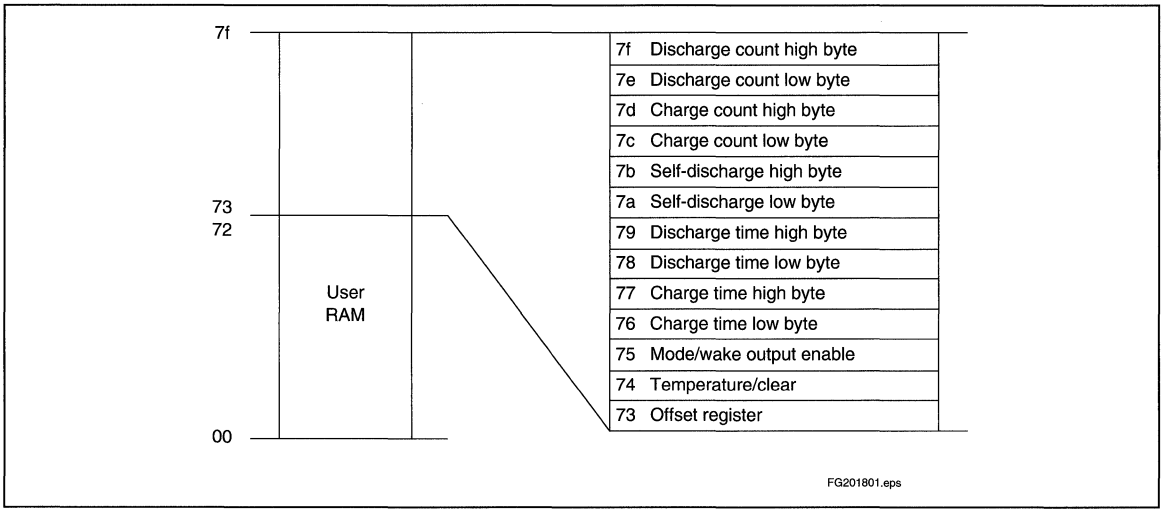


Figure 3. Address Map

During charge, the CCR and the Charge Time Counter (CTC) are active. If V_{SR1} is greater than V_{SR2}, indicating a charge, the CCR counts at a rate equivalent to 12.5µV every hour, and the CTC counts at a rate of 1 count/0.8789 seconds. For example, a +100mV signal produces 8000 CCR counts and 4096 CTC counts each hour. The amount of charge added to the battery can easily be calculated.

The DTC and the CTC are 16-bit registers, and roll over beyond ffffh. If a rollover occurs, the corresponding bit in the MODE/WOE register is set, and the counter will subsequently increment at 1/256 of the normal rate (16 counts/hr.).

Whenever the signal between SR1 and SR2 is above the Wakeup Output Enable (WOE) threshold and the HDQ pin is high, the bq2018 is in its full operating state. In this state, the DCR, CCR, DTC, CTC, and SCR are fully operational, and the $\overline{\text{WAKE}}$ output is low. During this mode, the internal RAM registers of the bq2018 may be accessed over the HDQ pin, as described in the section "Communicating With the 2018."

If the signal between SR1 and SR2 is below the WOE threshold (refer to the $\overline{\text{WAKE}}$ section for details) and HDQ remains low for greater than 10 seconds, the bq2018 enters a sleep mode where all register counting is suspended. The bq2018 remains in this mode until HDQ returns high.

For self-discharge calculation, the self-discharge count register (SCR) counts at a rate equivalent to 1 count every hour at a nominal 25°C and doubles approximately every 10°C up to 60°C. The SCR count rate is halved every 10 °C below 25°C down to 0°C. The value in SCR is useful in determining an estimation of the battery self-discharge based on capacity and storage temperature conditions.

The bq2018 may be programmed to measure the voltage offset between SR1 and SR2 during pack assembly or at any time by invoking the Calibration mode. The Offset Register (OFR) is used to store the bq2018 offset. The 8-bit 2's complement value stored in the OFR is scaled to the same units as the DCR and CCR, representing the amount of positive or negative offset in the bq2018. The maximum offset for the bq2018 is specified as ± 500µV. Care should be taken to ensure proper PCB layout. Using OFR, the system host can cancel most of the effects of bq2018 offset for greater resolution and accuracy.

Figure 3 shows the bq2018 register address map. The bq2018 uses the upper 13 locations. The remaining memory can store user-specific information such as chemistry, serial number, and manufacturing date.

$\overline{\text{WAKE}}$ Output

This output is used to inform the system that the voltage difference between SR1 and SR2 is above or below the Wake Output Enable (WOE) threshold programmed in the MODE/WOE register. When the voltage difference between SR1 and SR2 is below V_{WOE}, the $\overline{\text{WAKE}}$ output goes into High Z and remains in this state until the discharge or charge current increases above the specified value. The MODE/WOE resets to 0eh after a power-on reset. V_{WOE} is set by dividing 3.84mV by a value between 1 and 7 (1–7h) according to Table 3.

Table 3. WOE Thresholds

WOE_{3-1} (hex)	V_{WOE} (mV)
0h	n/a
1h	3.840
2h	1.920
3h	1.280
4h	0.960
5h	0.768
6h	0.640
7h*	0.549

* Default value after POR.

Table 4. Temperature Steps

Temp	Value (hex)	SDR Count Rate
<0°	0h	× 1/8
0–10°	1h	× 1/4
10–20°	2h	× 1/2
20–30°	3h	1 count/hr.
30–40°	4h	× 2
40–50°	5h	× 4
50–60°	6h	× 8
>60°	7h	× 16

Temperature

The bq2018 has an internal temperature sensor which is used to set the value in the temperature register (TMP/CLR) and set the self-discharge count rate value. The register reports the temperature in 8 steps of 10°C from <0°C to >60°C as Table 4 specifies. The bq2018 temperature sensor has typical accuracy of ±2°C at 25°C. See the TMP/CLR register description for more details.

Clear Register

The host system is responsible for register maintenance. To facilitate this maintenance, the bq2018 has a Clear Register (TMP/CLR) designed to reset the specific counter or register pair to zero. The host system clears a register by writing the corresponding register bit to 1. When the bq2018 completes the reset, the corresponding bit in the TMP/CLR register is automatically reset to 0, which saves the host an extra write/read cycle. Clearing the DTC register clears the STD bit and sets the DTC count rate to the default value of 1 count per 0.8789s. Clearing the CTC register clears the STC bit and sets the CTC count rate to the default value of 1 count per 0.8789s.

Calibration Mode

The system can enable bq2018 V_{OS} calibration by setting the calibration bit in the MODE/WOE register (Bit 6) to 1. The bq2018 then enters calibration mode when the HDQ line is low for greater than 10 seconds and when the signal between SR1 and SR2 is below V_{WOE}. **Caution: Take care to ensure that no low-level external signal is present between SR1 and SR2 because this affects the calibration value that the bq2018 calculates.**

If HDQ remains low for one hour and $|V_{SR}| < V_{WOE}$ for the entire time, the measured V_{OS} is latched into the OFR register, and the calibration bit is reset to zero, indicating to the system that the calibration cycle is complete. Once calibration is complete, the bq2018 enters a

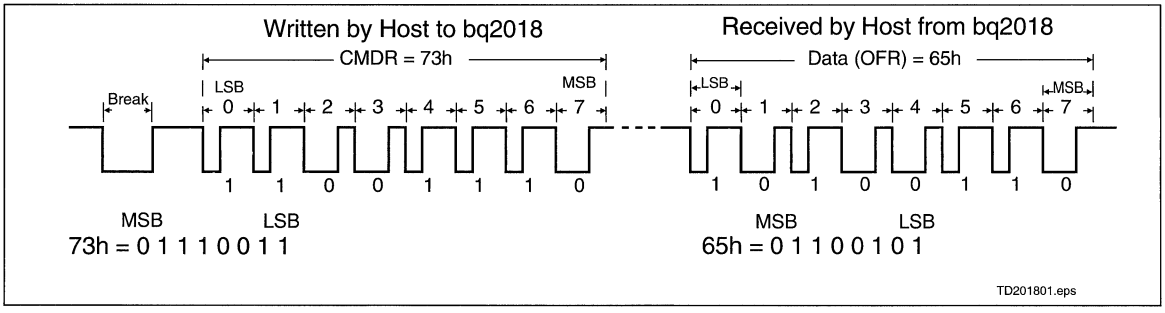


Figure 4. Typical Communication with the bq2018

Table 5. bq2018 Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	Command register	-	Write	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
DCRH	Discharge count register high byte	7f	Read	DCRH7	DCRH6	DCRH5	DCRH4	DCRH3	DCRH2	DCRH1	DCRH0
DCRL	Discharge count register low byte	7e	Read	DCRL7	DCRL6	DCRL5	DCRL4	DCRL3	DCRL2	DCRL1	DCRL0
CCRH	Charge count register high byte	7d	Read	CCRH7	CCRH6	CCRH5	CCRH4	CCRH3	CCRH2	CCRH1	CCRH0
CCRL	Charge count register low byte	7c	Read	CCRL7	CCRL6	CCRL5	CCRL4	CCRL3	CCRL2	CCRL1	CCRL0
SCRH	Self-discharge count register high byte	7b	Read	SCRH7	SCRH6	SCRH5	SCRH4	SCRH3	SCRH2	SCRH1	SCRH0
SCRL	Self-discharge count register low byte	7a	Read	SCRL7	SCRL6	SCRL5	SCRL4	SCRL3	SCRL2	SCRL1	SCRL0
DTCH	Discharge time count high byte	79	Read	DTCH7	DTCH6	DTCH5	DTCH4	DTCH3	DTCH2	DTCH1	DTCH0
DTCL	Discharge time count low byte	78	Read	DTCL7	DTCL6	DTCL5	DTCL4	DTCL3	DTCL2	DTCL1	DTCL0
CTCH	Charge time count high byte	77	Read	CTCH7	CTCH6	CTCH5	CTCH4	CTCH3	CTCH2	CTCH1	CTCH0
CTCL	Charge time count low byte	76	Read	CTCL7	CTCL6	CTCL5	CTCL4	CTCL3	CTCL2	CTCL1	CTCL0
MODE/ WOE	MODE/ wake-up output enable	75	Read/ write	OVRDQ	CAL	STC	STD	WOE3	WOE2	WOE1	0
TMP/CLR	Tempera-ture/Clear register	74	Read/ write	TMP2	TMP1	TMP0	CTC	DTC	SCR	CCR	DCR
OFR	Offset register	73	Read/ write	OFR7	OFR6	OFR5	OFR4	OFR3	OFR2	OFR1	OFR0
RAM	User memory	72-00	Read/ write	-	-	-	-	-	-	-	-

Notes: 1. MODE/WOE register bit 0 is set to zero at startup and should not be written to 1 for proper bq2018 operation.

2. OFR value is in two's complement.

low-power mode until HDQ goes high, indicating an external system is ready to access the bq2018. If HDQ transitions high prior to completion of the V_{OS} calculation or if $|V_{SR}| > V_{WOE}$, then the calibration cycle is reset. The bq2018 then postpones the calibration cycle until the conditions are met. The calibration bit does not reset to zero until a valid calibration cycle is completed. The requirement for HDQ to remain low for the calibration cycle can be disabled by setting the OVRDQ bit to 1. In this case, calibration continues as long as $|V_{SR}| < V_{WOE}$. The OVRDQ bit is reset to zero at the end of a valid calibration cycle.

Communicating with the bq2018

The bq2018 includes a simple single-pin (referenced to V_{SS}) serial data interface. A host processor uses the interface to access various bq2018 registers. Battery activity may be easily monitored by adding a single contact to the battery pack. **Note: The HDQ pin requires an external pull-up or pull-down resistor.**

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2018. The command directs the bq2018 either to store the next eight bits of data received to a register specified by the command byte or to output the eight bits of data from a register specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 5K bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2018 may be sampled using the pulse-width capture timers available on some microcontrollers. A UART may also be used to communicate through the HDQ pin.

If a communication time-out occurs, e.g., the host waits longer than t_{CYCB} for the bq2018 to respond or if this is the first access command, then a BREAK should be sent by the host. The host may then resend the command. The bq2018 detects a BREAK when the HDQ pin is driven to a logic-low state for a time, t_B or greater. The HDQ pin then returns to its normal ready-high logic state for a time, t_{BR}. The bq2018 is then ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2018 taking the HDQ pin to a logic-low state for a period, $t_{STRH,B}$. The next section is the actual data transmission, where the data should be valid by a period, $t_{DSU,B}$, after the negative edge used to start communication. The data should be held for a period, t_{DV}/t_{DH}, to allow the host or bq2018 to sample the data bit.

The final section is used to stop the transmission by returning the HDQ pin to a logic-high state by at least a period, $t_{SSU,B}$, after the negative edge used to start communication. The final logic-high state should be held until a period, $t_{CYCH,B}$, to allow time to ensure that the bit transmission ceased properly. The serial communication timing specification and illustration sections give the timings for data and break communication.

Communication with the bq2018 always occurs with the least-significant bit being transmitted first. Figure 4 shows an example of a communication sequence to read the bq2018 OFR register.

bq2018 Registers

The bq2018 command and status registers are listed in Table 5 and described below.

Command (CMDR)

The write-only command register is accessed when the bq2018 has received eight contiguous valid command bits. The command register contains two fields:

- W/$\overline{R}$
- Command address

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function. The W/$\overline{R}$ values are

CMDR Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is

0 The bq2018 outputs the requested register contents specified by the address portion of the CMDR

1 The following eight bits should be written to the register specified by the address portion of the CMDR

The lower seven-bit field of CMDR contains the address portion of the register to be accessed.

CMDR Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Discharge Count Registers (DCRH/DCRL)

The DCRH high-byte register (address = 7fh) and the DCRL low-byte register (address = 7eh) contain the count

of the discharge, and are incremented whenever $V_{SR1} < V_{SR2}$. These registers continue to count beyond ffffh, so proper register maintenance should be done by the host system. The TMP/CLR register is used to force the reset of both the DCRH and DCRL to zero.

Charge Count Registers (CCRH/CCRL)

The CCRH high-byte register (address = 7dh) and the CCRL low-byte register (address = 7ch) contain the count of the charge, and are incremented whenever $V_{SR1} > V_{SR2}$. These registers continue to count beyond ffffh, so proper register maintenance should be done by the host system. The TMP/CLR register is used to force the reset of both the CCRH and CCRL to zero.

Self-discharge Count Registers (SCRH/SCRL)

The SCRH high-byte register (address = 7bh) and the SCRL low-byte register (address = 7ah) contain the self-discharge count. This register is continually updated whenever the bq2018 is in its normal operating mode. The counts in these registers are incremented based on time and temperature. The SCR counts at a rate of 1 count per hour at 20–30°C and doubles every 10°C to greater than 60°C (16 counts/hour). The count will half every 10°C below 20–30°C to less than 0°C (1 count/8 hours). These registers continue to count beyond ffffh, so proper register maintenance should be done by the host system. The TMP/CLR register is used to force the reset of both the SCRH and SCRL to zero.

Discharge Time Count Registers (DTCH/DTCL)

The DTCH high-byte register (address = 79h) and the DTCL low-byte register (address = 78h) are used to determine the length of time the $V_{SR1} < V_{SR2}$ indicating a discharge. The counts in these registers are incremented at a rate of 4096 counts per hour. If the DTCH/DTCL register continues to count beyond ffffh, the STD bit is set in the MODE/WOE register indicating a rollover. Once set, DTCH and DTCL increment at a rate of 16 counts per hour. **Note: If a second rollover occurs, STD is cleared. Access to the bq2018 should be timed to clear DTCH/DTCL more often than every 170 days.** The TMP/CLR register is used to force the reset of both the DTCH and DTCL to zero.

Charge Time Count Registers (CTCH/CTCL)

The CTCH high-byte register (address = 77h) and the CTCL low-byte register (address = 76h) are used to determine the length of time the $V_{SR1} > V_{SR2}$ indicating a charge. The counts in these registers are incremented at a rate of 4096 counts per hour. If the CTCH/CTCL registers continue to count beyond ffffh, the STC bit is set in the MODE/WOE register indicating a rollover. Once set, DTCH and DTCL increment at a rate of 16 counts per hour. **Note: If a second rollover occurs, STC is cleared. Access to the bq2018 should be timed to clear CTCH/CTCL more often than every 170 days.** The TMP/CLR register is used to force the reset of both the CTCH and CTCL to zero.

Mode/Wake-up Enable Register

The Mode/WOE register (address = 75h) contains the calibration, wakeup enable information, and the STC and STD bits as described below.

The Override DQ(OVRDQ) bit (bit 7) is used to override the requirement for HDQ to be low prior to initiating V_{OS} calibration. This bit is normally set to zero. If OVRDQ is written to one, the bq2018 begins offset calibration when $|V_{SR}| < V_{WOE}$ where HDQ = Don't care.

The OVRDQ location is

MODE/WOE Bits							
7	6	5	4	3	2	1	0
OVRDQ	-	-	-	-	-	-	-

Where OVRDQ is

0 HDQ = 0 and $|V_{SR}| < V_{WOE}$ for V_{OS} calibration to begin

1 HDQ = Don't care and $|V_{SR}| < V_{WOE}$ for V_{OS} calibration to begin

Note: The OVRDQ bit should only be used in conjunction with a calibration cycle. Normal operation of the bq2018 cannot be guaranteed when this bit is set. After a valid calibration cycle, bit 7 is reset to zero.

The calibration (CAL) bit 6 is used to enable the bq2018 offset calibration test. Setting this bit to 1 enables a V_{OS} calibration whenever HDQ is low (default), and $|V_{SRO}| < V_{WOE}$. This bit is cleared to 0 by the bq2018 whenever a valid V_{OS} calibration is completed, and the OFR register is updated with the new calculated offset. The bit remains 1 if the offset calibration was not completed.

The CAL location is

MODE/WOE Bits							
7	6	5	4	3	2	1	0
-	CAL	-	-	-	-	-	-

Where CAL is

0 Valid offset calibration

1 Offset calibration pending

The slow time charge (STC) and slow time discharge (STD) flags indicate if the CTC or DTC registers have rolled over beyond ffffh. STC set to 1 indicates a CTC rollover; STD set to 1 indicates a DTC rollover.

The STC and STD locations are

MODE/WOE Bits							
7	6	5	4	3	2	1	0
-	-	STC	STD	-	-	-	-

Where STC/STD is

0 No rollover

1 Rollover occurred in the corresponding CTC/DTC register.

The Wake Up Output Enable (WOE) bits (bits 3–1) are used to set the Wake-Up Enable signal level. Whenever $|V_{SRO}| < V_{WOE}$, the $\overline{WAKE}$ output is in High Z. If $|V_{SRO}|$ is greater than V_{WOE}, $\overline{WAKE}$ transitions low. On bq2018 initialization (power-on reset) these bits are set to 1. Setting all of these bits to zero is not valid. Refer to Table 3 for the various WOE values.

The WOE 3–1 locations are

MODE/WOE Bits							
7	6	5	4	3	2	1	0
-	-	-	-	WOE3	WOE2	WOE1	-

Where WOE3–1 is determined by dividing 3.84mV by the value in WOE.

Bit 0 is reserved and must remain 0.

Temperature and Clear Register

The TMP/CLR register (address = 74h) is used to give the present temperature step between < 0°C to > 60°C and clear the various count registers. The values of the TMP0–TMP2 (bits 5–7) denote the current temperature step sense by the bq2018 as outlined in Table 4. The bq2018 temperature sense is trimmed to ± 2°C typical (± 4°C maximum).

The TMP2–0 locations are

TMP/CLR Bits							
7	6	5	4	3	2	1	0
TMP2	TMP1	TMP0	-	-	-	-	-

Where TMP2–0 is the temperature step sensed by this bq2018.

The Clear bits (Bits 0–4) are used to reset the various bq2018 counters and STC and STD bits to zero. Writing the bits to 1 resets the corresponding register to 0. The clear bit resets to 0 indicating a successful register reset. Each clear bit is independent, so it is possible to clear the DCRH/DCRL registers without affecting the values in any other bq2018 register. The high-byte and low-byte registers are both cleared when the corresponding bit is written to 1 per the figure below.

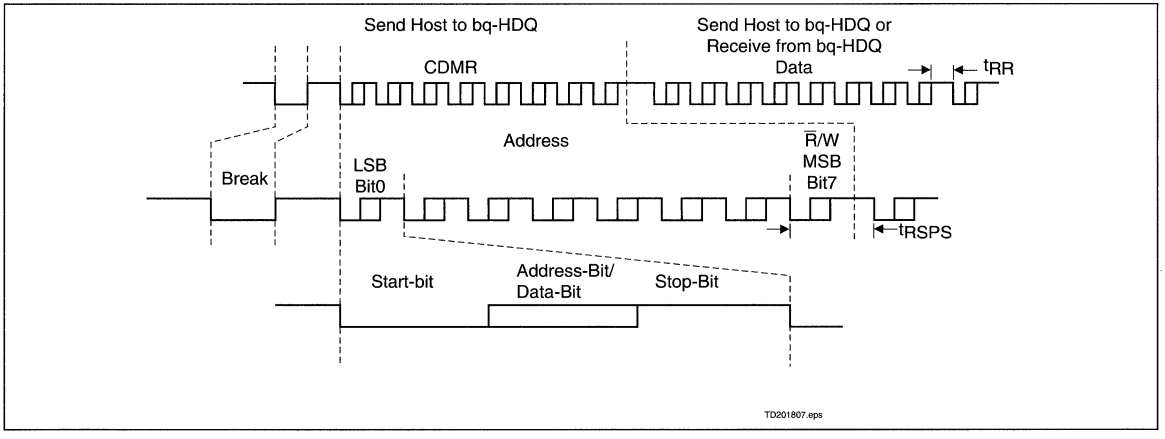


Figure 5. Communications Frame Example

The Clear bit locations are

TMP/CLR Bits							
7	6	5	4	3	2	1	0
-	-	-	CTC	DTC	SCR	CCR	DCR

Where:

CTC bit (bit 4) resets both the CTCH and CTCL registers and the STC bit to 0.

The DTC bit (bit 3) resets both the DTCH and DTCL registers and the STD bit to 0.

The SCR bit (bit 2) resets both the SCRH and SCRL registers to 0.

The CCR bit (bit 1) resets both the CCRH and CCRL registers to 0.

The DCR bit (bit 0) resets both the DCRH and DCRL registers to 0.

Offset Register (OFR)

The OFR register (address = 73h) is used to store the calculated V_{OS} of the bq2018. The OFR value can be used to cancel the voltage offset between V_{SR1} and V_{SR2}. The up/down offset counter is centered at zero. The actual offset is an 8-bit two's complement value located in OFR.

The OFR locations are

OFR Bits							
7	6	5	4	3	2	1	0
OFR7	OFR6	OFR5	OFR4	OFR3	OFR2	OFR1	OFR0

Where OFR7 is

1 Discharge

0 Charge

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+6.0	V	
HDQ	Relative to V_{SS}	-0.3	+6.0	V	
All other pins		V_{SS} -0.3V	V_{CC} +3.0V	V	
I_{REG}	REG to V_{SS}		1.0	mA	
V_{SR1} / V_{SR2}	Relative to V_{SS}	-0.3	+6.0	V	A 100kΩ series resistor is recommended to protect SR1 / SR2 in case of a shorted battery.
T_{OPR}	Operating temperature	- 20	+70	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	2.8	4.25	5.5	V	REG = No connect
		3.5	3.7	3.9	V	V_{CC} derived from REG, Note 3
I_{CC}	Operating current	-	60	70	µA	$V_{CC,HDQ}$ = 3.7V
		-	70	80	µA	$V_{CC,HDQ}$ = 5.5V
I_{CC2}	Sleep	-	-	10	µA	V_{CC} = 5.5V
I_{RBI}	RBI current	-	-	100	nA	V_{CC} < 2.4V
V_{SR}	Sense resistor input	-200	-	200	mV	$V_{SR1} < V_{SR2}$ = discharge; $V_{SR1} > V_{SR2}$ = charge Note 2
R_{SR}	SR1 / SR2 input impedance	10	-	-	MΩ	-200mV < V_{SR} < 200mV
I_{OL}	Open-drain sink current	-	-	2.0	mA	$V_{OL} = V_{SS} + 0.3V$ $\overline{WAKE}$, HDQ
V_{IHDQ}	HDQ input high	2.5	-	-	V	
V_{ILDQ}	HDQ input low	-	-	0.8	V	

Notes:
1. All voltages relative to V_{SS}.
2. $V_{SR1/SR2} + V_{OS}$. V_{OS} is affected by PC board layout. Follow proper layout guidelines for optimal performance.
3. Can be guaranteed by design when using an SST108 or equivalent JFET.

12/15

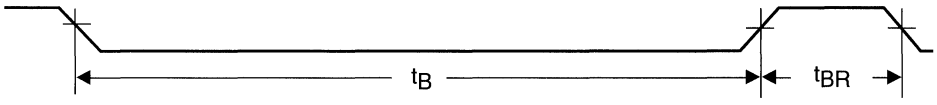
Performance Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Typical	Maximum	Unit	Notes
V_{OS}	Offset voltage		±500	µV	Voltage offset between SR1 and SR2
OSC	Timer accuracy	1.5	±3.0	%	V_{CC} =3.5 - 3.9V (T_A = 0–70°C)
INR	Integrated non-repeatability error	0.5	1.0	%	Measured repeatability given similar operating conditions
INL	Integrated non-linearity	1.0	2.0	%	Add 0.05% per °C above or below 25°C and 0.5% per volt above or below 3.7V.

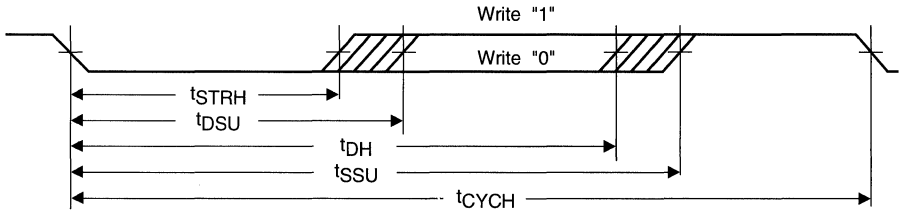
Standard Serial Communication Timing Specification ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2018 (write)	190	-	-	µs	
t_{CYCB}	Cycle time, bq2018 to host (read)	190	205	250	µs	
t_{STRH}	Start hold, host to bq2018 (write)	5	-	-	ns	
t_{STRB}	Start hold, bq2018 to host (read)	32	-	-	µs	
$t_{DSU,B}$	Data setup	-	-	50	µs	
t_{DH}	Data hold	90	-	-	µs	
t_{DV}	Data valid	-	-	80	µs	
t_{SSUB}	Stop setup (bq2018 to host)	-	-	95	µs	
t_{SSU}	Stop setup (host to bq2018)	-	-	145	µs	
t_B	Break	190	-	-	µs	
t_{BR}	Break recovery	40	-	-	µs	
t_{RSPS}	Response time, bq2018 to host	190	-	320	µs	
t_{RR}	Read recovery	40	-	-	µs	Host read to next cycle

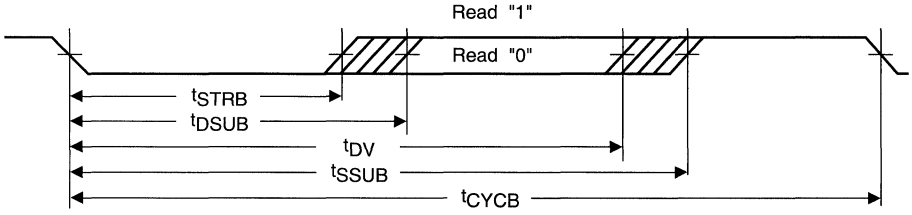
Break Timing



Host to bq2018



bq2018 to Host



Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	All		
2	12		Clarification of absolute maximum pin ratings

Note: Change 1 = Jan. 1999 B changes to Final from Dec. 1998 Preliminary data sheet.

Change 2 = June 1999 C changes from Jan. 1999 B.

Ordering Information

bq2018

Temperature Range:
blank = Commercial (-20 to +70°C)

Package Option:
SN = 8-pin narrow SOIC
TS = 8 pin TSSOP

Device:
bq2018 Power Minder IC

UNITRODE

bq2040

Gas Gauge IC With SMBus Interface

Features

- Provides accurate measurement of available charge in NiCd, NiMH, and Li-Ion batteries
- Supports SBS v1.0 data set and two-wire interface
- Monitors charge FET in Li-Ion pack protection circuit
- Designed for battery pack integration
  - Low operating current
  - Complete circuit can fit on less than ¾ square inch of PCB space
- Supports SBS charge control commands for NiCd, NiMH, and Li-Ion
- Drives a four-segment LED display for remaining capacity indication
- 16-pin narrow SOIC

General Description

The bq2040 Gas Gauge IC With SMBus Interface is intended for battery-pack or in-system installation to maintain an accurate record of available battery charge. The bq2040 directly supports capacity monitoring for NiCd, NiMH, and Li-Ion battery chemistries.

The bq2040 uses the System Management Bus v1.0 (SMBus) protocol and supports the Smart Battery Data (SBData) commands. The bq2040 also supports the SBData charge control functions. Battery state-of-charge, remaining capacity, remaining time, and chemistry are available over the serial link. Battery-charge state can be directly indicated using a four-segment LED display to graphically depict battery full-to-empty in 25% increments.

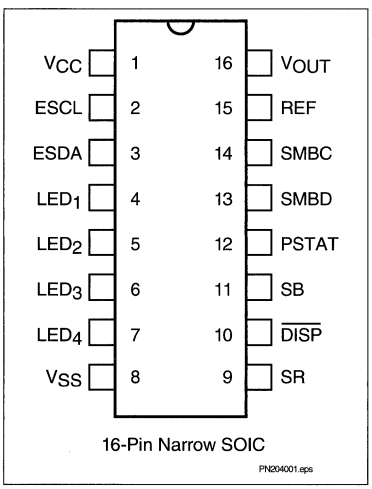
The bq2040 estimates battery self-discharge based on an internal timer and temperature sensor and user-programmable rate information stored in external EEPROM. The bq2040 also automatically recalibrates or "learns" battery capacity in the full course of a discharge cycle from full to empty.

The bq2040 may operate directly from three nickel chemistry cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide V_{CC} for other battery cell configurations.

An external EEPROM is used to program initial values into the bq2040 and is necessary for proper operation.

4

Pin Connections



16-Pin Narrow SOIC

PN204001.eps

Pin Names

V_{CC}	3.0–6.5V	SB	Battery sense input
ESCL	EEPROM clock	PSTAT	Protector status input
ESDA	EEPROM data	SMBD	SMBus data input/output
LED_{1-4}	LED segment 1-4	SMBC	SMBus clock
V_{SS}	System ground	REF	Voltage reference output
SR	Sense resistor input	V_{OUT}	EEPROM supply output
$\overline{DISP}$	Display control input		

Pin Descriptions

V_{CC} **Supply voltage input**

ESCL **Serial memory clock**

Output used to clock the data transfer between the bq2040 and the external nonvolatile configuration memory.

ESDA **Serial memory data and address**

Bidirectional pin used to transfer address and data to and from the bq2040 and the external nonvolitile configuration memory.

LED_1–LED_4 **LED display segment outputs**

Each output may drive an external LED.

V_{SS} **Ground**

SR **Sense resistor input**

The voltage drop (V_{SR}) across pins SR and V_{SS} is monitored and integrated over time to interpret charge and discharge activity. The SR input is connected to the sense resistor and the negative terminal of the battery. $V_{SR} < V_{SS}$ indicates discharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2040 is $V_{SR} + V_{OS}$. (See Table 3.)

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ floating allows the LED display to be active during charge if the rate is greater than 100mA. $\overline{DISP}$ low activates the display for 4 seconds.

SB **Secondary battery input**

Monitors the pack voltage through a high-impedance resistor divider network. The pack voltage is reported in the SBD register function Voltage (0x09) and is monitored for end-of-discharge voltage and charging voltage parameters.

PSTAT **Protector status input**

Provides overvoltage status from the Li-Ion protector circuit and can initiate a charge suspend request.

SMBD **SMBus data**

Open-drain bidirectional pin used to transfer address and data to and from the bq2040.

SMBC **SMBus clock**

Open-drain bidirectional pin used to clock the data transfer to and from the bq2040.

REF **Reference output for regulator**

REF provides a reference output for an optional FET-based micro-regulator.

V_{OUT} **Supply output**

Supplies power to the external EEPROM configuration memory.

Functional Description

General Operation

The bq2040 determines battery capacity by monitoring the amount of charge put into or removed from a rechargeable battery. The bq2040 measures discharge and charge currents, estimates self-discharge, and monitors the battery for low-battery voltage thresholds. The charge is measured by monitoring the voltage across a small-value series sense resistor between the battery's negative terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2040 using the LED capacity display, the serial port, and an external EEPROM for battery pack programming information. The bq2040 must be configured and calibrated for the battery-specific information to ensure proper operation. Table 1 outlines the configuration information that must be programmed in the EEPROM.

An internal temperature sensor eliminates the need for an external thermistor—reducing cost and components. An internal, temperature-compensated timebase eliminates the need for an external resonator, further reducing cost and components. The entire circuit in Figure 1 can occupy less than ¾ square inch of board space.

4

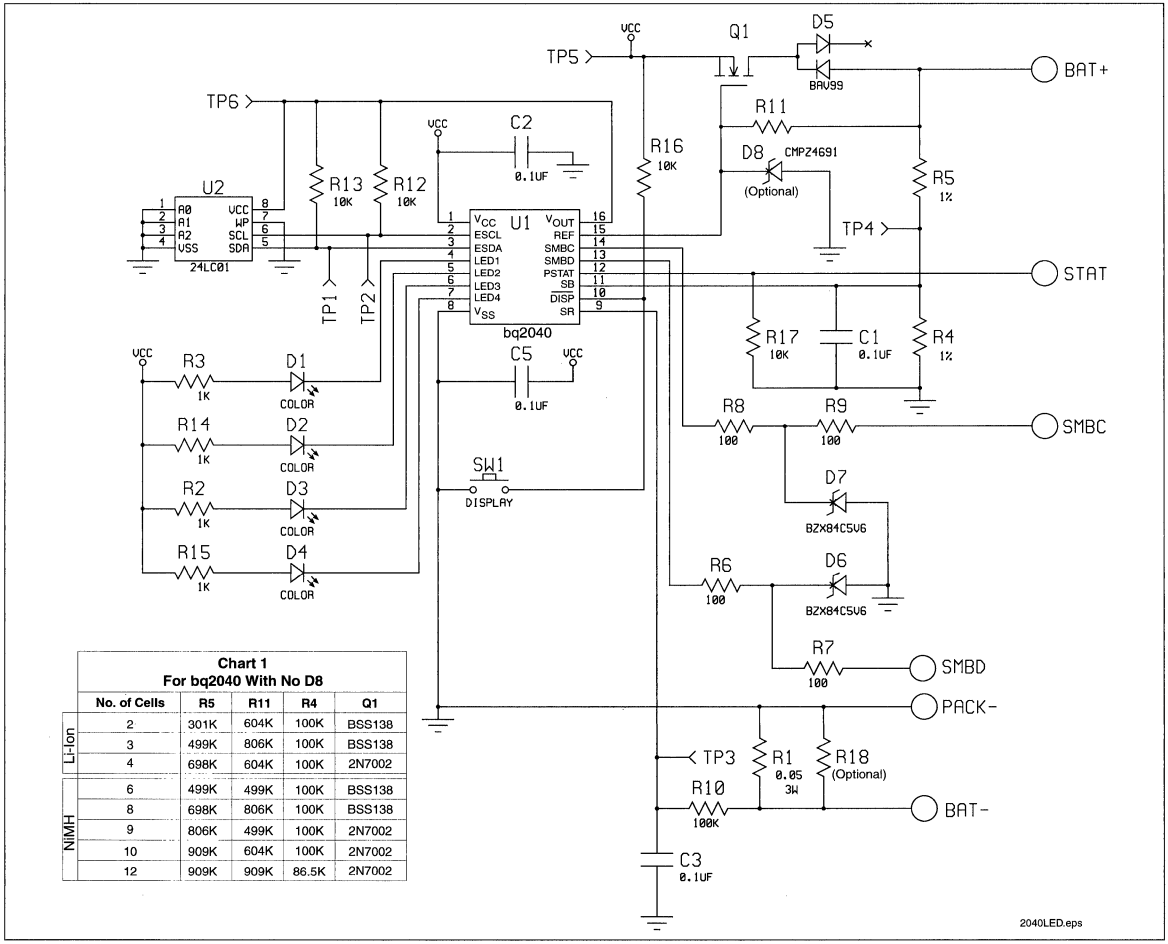


Chart 1
For bq2040 With No D8

	No. of Cells	R5	R11	R4	Q1
Li-ion	2	301K	604K	100K	BSS138
	3	499K	806K	100K	BSS138
	4	698K	604K	100K	2N7002
NiMH	6	499K	499K	100K	BSS138
	8	698K	806K	100K	BSS138
	9	806K	499K	100K	2N7002
	10	909K	604K	100K	2N7002
	12	909K	909K	86.5K	2N7002

Figure 1. Battery Pack Application Diagram—LED Display

3/30

Table 1. Configuration Memory Map

Parameter Name	Address	Description	Length	Units
EEPROM length	0x00	Number of EEPROM data locations must = 0x64	8 bits	NA
EEPROM check1	0x01	EEPROM data integrity check byte, must = 0x5b	8 bits	NA
Remaining time alarm	0x02/0x03	Sets RemainingTimeAlarm (0x02)	16 bits	minutes
Remaining capacity alarm	0x04/0x05	Sets RemainingCapacityAlarm (0x01)	16 bits	mAh
Reserved	0x06/0x07	Reserved for future use	16 bits	NA
Initial charging current	0x08/0x09	Sets the initial charging current	16 bits	mA
Charging voltage	0x0a/0x0b	Sets ChargingVoltage (0x15)	16 bits	mV
Battery status	0x0c/0x0d	Initializes BatteryStatus (0x16)	16 bits	NA
Cycle count	0x0e/0x0f	Initializes and stores CycleCount (0x17)	16 bits	cycles
Design capacity	0x10/0x11	Sets DesignCapacity (0x18)	16 bits	mAh
Design voltage	0x12/0x13	Sets DesignVoltage (0x19)	16 bits	mV
Specification information	0x14/0x15	Programs SpecificationInfo (0x1a)	16 bits	NA
Manufacture date	0x16/0x17	Programs ManufactureDate (0x1b)	16 bits	NA
Serial number	0x18/0x19	Programs SerialNumber (0x1c)	16 bits	NA
Fast-charging current	0x1a/0x1b	Sets ChargingCurrent (0x14)	16 bits	mA
Maintenance-charge current	0x1c/0x1d	Sets the trickle current request	16 bits	mA
Reserved	0x1e/0x1f	Reserved must = 0x0000	16 bits	mAh
Manufacturer name	0x20-0x2b	Programs ManufacturerName (0x20)	96 bits	NA
Current overload	0x2c/0x2d	Sets the overload current threshold	16 bits	mA
Battery low %	0x2e	Sets the battery low amount	8 bits	%
Reserved	0x2f	Reserved for future use	8 bits	NA
Device name	0x30-0x37	Programs DeviceName (0x21)	64 bits	NA
Li-Ion taper current	0x38/0x39	Sets the upper limit of the taper current for charge termination	16 bits	mA
Maximum overcharge limit	0x3a/0x3b	Sets the maximum amount of overcharge	16 bits	NA
Reserved	0x3c	Reserved must = 0x00	8 bits	NA
Access protect	0x3d	Locks commands outside of the SBS data set	8 bits	NA
FLAGS1	0x3e	Initializes FLAGS1	8 bits	NA
FLAGS2	0x3f	Initializes FLAGS2	8 bits	NA
Device chemistry	0x40-0x45	Programs DeviceChemistry (0x22)	48 bits	NA
Current measurement gain	0x46/0x47	Sense resistor calibration value	16 bits	NA
Battery voltage offset	0x48	Voltage calibration value	8 bits	NA
Temperature offset	0x49	Temperature calibration value	8 bits	NA
Maximum temperature and ΔT step	0x4a	Sets the maximum charge temperature and the ΔT step for $\Delta T/\Delta t$ termination	8 bits	NA

Table 1. Configuration Memory Map (Continued)

Parameter Name	Address	Description	Length	Units
Charge efficiency	0x4b	Sets the high/low charge rate efficiencies	8 bits	NA
Full charge percentage	0x4c	Sets the percent at which the battery is considered fully charged	8 bits	NA
Digitial filter	0x4d	Sets the minimum charge/discharge threshold	8 bits	NA
Current integration gain	0x4e	Programs the current integration gain to the sense resistor value	8 bits	NA
Self-discharge rate	0x4f	Sets the battery's self-discharge rate	8 bits	NA
Manufacturer data	0x50-0x55	Programs ManufacturerData (0x23)	48 bits	NA
Voltage gain1	0x56/0x57	Battery divider calibration value	16 bits	NA
Reserved	0x58-0x59	Reserved	16 bits	NA
EDVF charging current	0x5a/0x5b	Sets the charge current request when the battery voltage is less than EDVF	16 bits	NA
End of discharge voltage1	0x5c/0x5d	Sets EDV1	16 bits	NA
End of discharge voltage final	0x5e/0x5f	Sets EDVF	16 bits	NA
Full-charge capacity	0x60/0x61	Initializes and stores FullChargeCapacity (0x10)	16 bits	mAh
Δt step	0x62	Sets the Δt step for $\Delta T/\Delta t$ termination	8 bits	NA
Hold-off time	0x63	Sets $\Delta T/\Delta t$ hold-off timer	8 bits	NA
EEPROM check 2	0x64	EEPROM data integrity check byte must = 0xb5	8 bits	NA
Reserved	0x65-0x7f	Reserved for future use		NA

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2040 monitors the battery potential through the SB pin. The voltage potential is determined through a resistor-divider network per the following equation:

$$\frac{R_5}{R_4} = \frac{MBV}{2.25} - 1$$

where MBV is the maximum battery voltage, R_5 is connected to the positive battery terminal, and R_4 is connected to the negative battery terminal. R_5/R_4 should be rounded to the next higher integer. The voltage at the SB pin (V_{SB}) should never exceed 2.4V.

The battery voltage is monitored for the end-of-discharge voltages (EDV1 and EDVF) and for alarm warning conditions. EDV threshold levels are used to determine when the battery has reached a programmable "empty" state. The bq2040 generates an alarm warning when the battery voltage exceeds the maximum charging voltage by 5% or if the voltage is below EDVF. The battery voltage gain, the two EDV thresholds, and the charging voltage are programmable in the EEPROM.

If V_{SB} is below either of the two EDV thresholds, the associated flag is latched and remains latched, independent of V_{SB}, until the next valid charge.

EDV monitoring may be disabled under certain conditions. If the discharge current is greater than the value stored in location 0x2c and 0x2d in the EEPROM (EE 0x2c/0x2d), EDV monitoring is disabled and resumes after the current falls below the programmed value.

Reset

The bq2040 is reset when first connected to the battery pack. On power-up, the bq2040 initializes and reads the EEPROM configuration memory. The bq2040 can also be reset with a command over the SMBus. The software reset sequence is the following: (1) write MaxError (0x0c) to 0x0000; (2) write the reset register (0x64) to 0x8009. A software reset can only be performed if the bq2040 is in an unlocked state as defined by the value in location 0x3d of the EEPROM (EE 0x3d) on power-up.

Temperature

The bq2040 monitors temperature sensing using an internal sensor. The temperature is used to adapt charge and self-discharge compensations as well as to monitor for maximum temperature and $\Delta T/\Delta t$ during a bq2040 controlled charge. Temperature may also be accessed over the SMBus with command 0x08.

Layout Considerations

The bq2040 measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally, in reference to Figure 1:

- The capacitors (C1 and C2) should be placed as close as possible to the SB and V_{CC} pins, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor capacitor (C3) should be placed as close as possible to the SR pin.
- The bq2040 should be in thermal contact with the cells for optimum temperature measurement.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2040. The bq2040 accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge currents are compensated for temperature and state-of-charge of the battery. Self-discharge is temperature-compensated.

The main counter, RemainingCapacity (RM), represents the available battery capacity at any given time. Battery charging increments the RM register, whereas battery discharging and self-discharge decrement the RM register and increment the internal Discharge Count Register (DCR).

The Discharge Count Register is used to update the FullChargeCapacity (FCC) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2040 adapts its capacity determination based on the actual conditions of discharge.

The battery's initial full capacity is set to the value stored in EE 0x60-0x61. Until FCC is updated, RM counts up to, but not beyond, this threshold during subsequent charges.

The battery's empty state is also programmed in the EEPROM. The battery low percentage (EE 0x2e) stores the percentage of FCC that will be written to RM when the battery voltage drops below the EDV1 threshold.

1. **FullChargeCapacity or learned-battery capacity:**

   FCC is the last measured discharge capacity of the battery. On initialization (application of V_{CC} or reset), FCC is set to the value stored in the EEPROM. Dur-

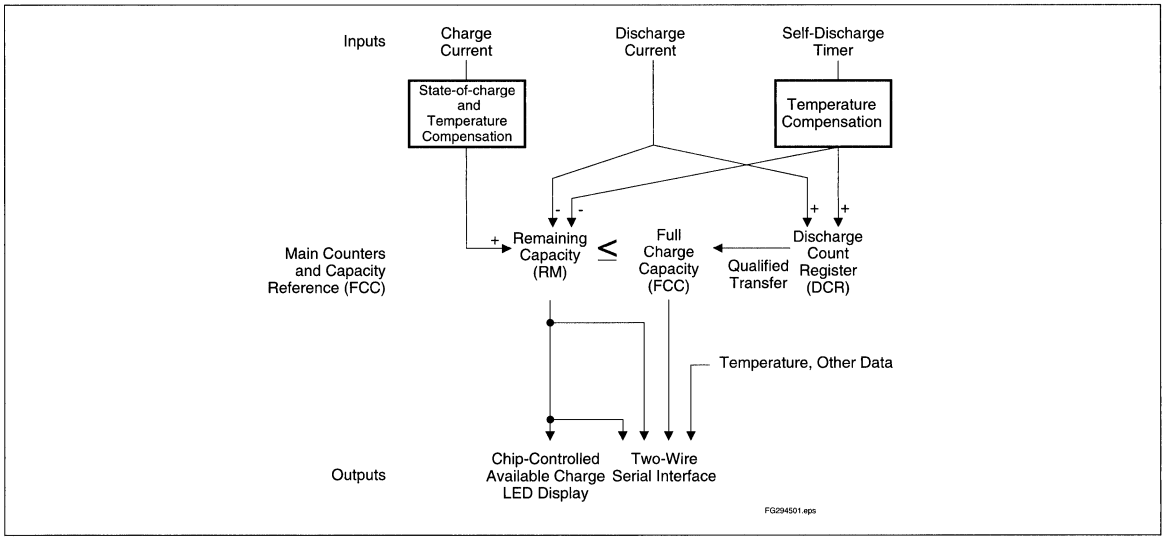


Figure 2. Operational Overview

ing subsequent discharges, FCC is updated with the latest measured capacity in the Discharge Count Register plus the battery low amount, representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the FCC register. Once updated, the bq2040 writes the new FCC to the EEPROM. The FCC also serves as the 100% reference threshold used by the relative state-of-charge calculation and display.

2. DesignCapacity (DC):

The DC is the user-specified battery capacity and is programmed from external EEPROM. The DC also provides the 100% reference for the absolute display mode.

3. RemainingCapacity (RM):

RM counts up during charge to a maximum value of FCC and down during discharge and self-discharge to 0. RM is set to the battery low amount after the EDV1 threshold has been reached. If RM is already equal to or less than the battery low amount, RM is not modified. If RM reaches the battery low amount before the battery voltage falls below EDV1 on discharge, RM stops counting down until the EDV1 threshold is reached. RM is set to 0 when the battery voltage reaches EDVF. To prevent overstatement of charge during periods of overcharge, RM stops incrementing when RM = FCC. RM may optionally be written to a user-defined value when fully charged if the battery pack is under bq2040 charge control. On initialization, RM is set to 0.

4. Discharge Count Register (DCR):

The DCR counts up during discharge independent of RM and can continue increasing after RM has decremented to 0. Prior to RM = 0, both discharge and self-discharge increment the DCR. After RM = 0, only discharge increments the DCR. The DCR resets to 0 when RM = FCC and stops counting at EDV1 on discharge. The DCR does not roll over but stops counting when it reaches FFFFh.

FCC is updated on the first charge after a qualified discharge to EDV1. The updated FCC equals the battery low percentage times the current FCC plus the DCR value. A qualified discharge to EDV1 occurs if all of the following conditions exist:

- No valid charge initiations (charges greater than 10mAh, where $V_{SRO} > +V_{SRD}$ occurred during the period between RM = FCC and EDV1 detected.
- The self-discharge count is not more than 256mAh.
- The low temperature fault bit in FLAGS2 is not set when the EDV1 level is reached during discharge.
- Battery voltage is not more than 256mV below the EDV1 threshold when EDV1 is set.

The valid discharge flag (VDQ) in FLAGS1 indicates whether the present discharge is valid for an FCC update. FCC cannot be reduced by more than 256mAh during any single cycle.

7/30

Charge Counting

Charge activity is detected based on a positive voltage on the SR input. If charge activity is detected, the bq2040 increments RM at a rate proportional to V_{SRO} and, if enabled, activates an LED display. Charge actions increment the RM after compensation for charge state and temperature.

The bq2040 determines charge activity sustained at a continuous rate equivalent to $V_{SRO} > +V_{SRD}$. **A valid charge equates to sustained charge activity greater than 10 mAh**. Once a valid charge is detected, charge threshold counting continues until V_{SRO} falls below V_{SRD}. V_{SRD} is a programmable threshold as described in the Digital Magnitude Filter section.

Discharge Counting

All discharge counts where $V_{SRO} < -V_{SRD}$ cause the RM register to decrement and the DCR to increment. V_{SRD} is a programmable threshold as described in the Digital Magnitude Filter section.

Self-Discharge Estimation

The bq2040 continuously decrements RM and increments DCR for self-discharge based on time and temperature provided that the discharge flag in BatteryStatus is set (charge not detected). The bq2040 self-discharge estimation rate is programmed in EE 0x4f and can be set from 0 to 25% per day for 20–30°C. This rate approximately doubles for every 10°C increase until the temperature is ≥ 70°C or halves every 10°C decrease until the temperature is < 10°C.

Charge Control

The bq2040 supports SBS charge control by broadcasting the ChargingCurrent and the ChargingVoltage to the Smart Charger address. The bq2040 broadcasts charging commands every 10 seconds; the broadcasts can be disabled by writing bit 14 of BatteryMode to 1. On reset, the initial charging current broadcast to the charger is set to the value programmed in EE 0x08-0x09. The bq2040 updates the value used in the charging current broadcasts based on the battery's state of charge, voltage, and temperature.

The bq2040 internal charge control is compatible with nickel-based and Li-Ion chemistries. The bq2040 uses current taper detection for Li-Ion primary charge termination and ΔT/Δt for nickel based primary charge termination. The bq2040 also provides a number of safety terminations based on battery capacity, voltage, and temperature.

Current Taper

For Li-Ion charge control, the ChargingVoltage must be set to the desired pack voltage during the constant voltage charge phase. The bq2040 detects a current taper termination when it measures the pack voltage to be within 128mV of the requested charging voltage and when the AverageCurrent is less than the programmed threshold in EE 0x38—0x39 and non-zero for at least 100s.

ΔT/Δt

The ΔT/Δt used by the bq2040 is programmable in both the temperature step (1.6°C–4.6°C) and time step (20 seconds–320seconds). Typical settings for 1°C/min include 2°C over 120 seconds and 3°C over 180 seconds. Longer times are required for increased slope resolution.

$\frac{\Delta T}{\Delta t}$ is set by the formula: $\frac{\Delta T}{\Delta t} =$

$$\frac{[(\text{lower nibble of EE 0x4a}) * 2 + 16] / 10}{[320 - (\text{EE 0x62}) * 20)]} \left[\frac{°C}{s}\right]$$

In addition to the ΔT/Δt timer, there is a hold-off timer, which starts when the battery is being charged at more than 255mA and the temperature is above 25°C. Until this timer expires, ΔT/Δt is suspended. If the temperature falls below 25°C, or if charging current falls below 255mA, the timer is reset and restarts only if these conditions are once again within range. The hold-off time is programmed in EE 0x63.

Charge Termination

Once the bq2040 detects a valid charge termination, the Fully_Charged, Terminate_Charge_Alarm, and the Over_Charged_Alarm bits are set in BatteryStatus, and the requested charge current is set to zero. Once the terminating conditions cease, the Terminate_Charge_Alarm and the Over_Charged_Alarm are cleared, and the requested charging current is set to the maintenance rate. The bq2040 requests the maintenance rate until RM falls below the amount determined by the programmable full- charge percentage. Once this occurs, the Fully_Charged bit is cleared, and the requested charge current and voltage are set to the fast-charge rate.

Bit 4 (CC) in FLAGS2 determines whether RM is modified after a ΔT/Δt or current taper termination occurs. If CC = 1, RM may be set from 0 to 100% of the FullChargeCapacity as defined in EE 0x4c. If RM is below the full-charge percentage, RM is set to the full-charge percentage of FCC. If RM is above the full-charge percentage, RM is not modified.

Charge Suspension

The bq2040 may temporarily suspend charge if it detects a charging fault. The charging faults include the following conditions:

- **Maximum Overcharge:** If charging continues for more than the programmed maximum overcharge limit as defined in EE 0x3a—0x3b beyond RM=FCC, the Fully_Charged bit is set, and the requested charging current is set to the maintenance rate.
- **Overvoltage:** An over-voltage fault exists when the bq2040 measures a voltage more than 5% above the ChargingVoltage. When the bq2040 detects an overvoltage condition, the requested charge current is set to 0 and the Terminate_Charge_Alarm bit is set in BatteryStatus. The alarm bit is cleared when the current drops below 256mA and the voltage is less than 105% of ChargingVoltage.
- **Overcurrent:** An overcurrent fault exists when the bq2040 measures a charge current more than 25% above the ChargingCurrent. If the ChargingCurrent is less than 1024mA, an overcurrent fault exists if the charge current is more than 1mA above the lowest multiple of 256mA that exceeds the ChargingCurrent. When the bq2040 detects an overcurrent condition, the requested charge current is set to 0 and the Terminate_Charge_Alarm bit is set in Battery Status. The alarm bit is cleared when the current drops below 256mA.
- **Maximum Temperature**: When the battery temperature equals the programmed maximum temperature, the requested charge current is set to zero and the Over_Temp_Alarm and the Terminate_Charge_Alarm bits are set in Battery Status. The Over_Temp_Alarm bit is cleared when the temperature drops to 43°C below the maximum temperature threshold minus 5°C.
- **PSTAT:** When the PSTAT input is ≥1.5V, the requested charge current is set to 0 and the Terminate_Charge_Alarm bit is set in BatteryStatus if the Discharging flag is not set. The alarm bit is cleared when the PSTAT input is <1.0V or the Discharging flag is set.
- **Low Temperature:** When the battery temperature is less than 12°C (LTF bit in FLAGS2 set), the requested charge current is set to the maintenance rate. Once the temperature is above 15°C, the requested charge current is set to the fast rate.
- **Undervoltage:** When the battery voltage is below the EDVF threshold, the requested charge current is set to the EDVF rate stored in EE0x5a/0x5b. Once the voltage is above EDVF, the requested charge current is set to the fast or maintenance rate depending on the state of the LTF bit.

Count Compensations

Charge activity is compensated for temperature and state-of-charge before updating the RM and/or DCR. Self-discharge estimation is compensated for temperature before updating RM or DCR.

Charge Compensation

Charge efficiency is compensated for state-of-charge, temperature, and battery chemistry. The charge efficiency is adjusted using the following equations:

$$1.)\,RM = RM * (Q_{EFC} - Q_{ET})$$

where RelativeStateOfCharge < FullChargePercentage, and Q_{EFC} is the programmed fast-charge efficiency varying from 0.75 to 1.0.

$$2.)\,RM = RM * (Q_{ETC} - Q_{ET})$$

where RelativeStateOfCharge ≥ FullChargePercentage and Q_{ETC} is the programmed maintenance (trickle) charge efficiency varying from 0.75 to 1.0.

Q_{ET} is used to adjust the charge efficiency as the battery temperature increases according to the following:

$Q_{ET} = 0$ if $T < 30°C$

$Q_{ET} = 0.02$ if $30°C \le T < 40°C$

$Q_{ET} = 0.05$ if $T \ge 40°C$

Q_{ET} is 0 over the entire temperature range for Li-Ion.

Digital Magnitude Filter

The bq2040 has a programmable digital filter to eliminate charge and discharge counting below a set threshold, V_{SRD}. Table 2 shows typical digital filter settings. The proper digital filter setting can be calculated using the following equation.

$$DMF = \frac{45}{V_{SRD}}$$

Table 2. Typical Digital Filter Settings

DMF	DMF Hex.	V_{SRD} (mV)
75	4B	0.60
100	64	0.45
150	96	0.30
175	AF	0.26
200	C8	0.23

9/30

Table 3. bq2040 Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
V_{OS}	Offset referred to V_{SR}	± 75	± 150	µV	$\overline{DISP}$ = V_{CC}.
INL	Integrated non-linearity error	± 1	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 0.5	± 1	%	Measurement repeatability given similar operating conditions.

Error Summary

Capacity Inaccurate

The FCC is susceptible to error on initialization or if no updates occur. On initialization, the FCC value includes the error between the design capacity and the actual capacity. This error is present until a qualified discharge occurs and FCC is updated (see the DCR description). The other cause of FCC error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity. Periodic qualified discharges from full to empty will minimize errors in FCC.

Current-Sensing Error

Table 3 illustrates the current-sensing error as a function of V_{SR}. A digital filter eliminates charge and discharge counts to the RM register when $-V_{SRD} < V_{SRO} < +V_{SRD}$.

Display

The bq2040 can directly display capacity information using low-power LEDs. The bq2040 displays the battery charge state in either absolute or relative mode. In relative mode, the battery charge is represented as a percentage of the FCC. Each LED segment represents 25% of the FCC.

In absolute mode, each segment represents a fixed amount of charge, 25% of the DesignCapacity. As the battery wears out over time, it is possible for the FCC to be below the design capacity. In this case, all of the LEDs may not turn on in absolute mode, representing the reduction in the actual battery capacity.

When $\overline{DISP}$ is tied to V_{CC}, the LED_{1-4} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active whenever the bq2040 detects a charge rate of 100mA or more. When pulled low, the segment outputs become active immediately for a period of approximately 4 seconds. The $\overline{DISP}$ pin must be returned to float or V_{CC} to reactivate the display.

LED_1 blinks at a 4Hz rate indicating a low battery condition whenever the display is active, EDVF is not set, and Remaining_Capacity_Alarm is set. V_{SB} below EDVF (EDVF = 1) disables the display output.

Microregulator

The bq2040 can operate directly from three nickel chemistry cells. To facilitate the power supply requirements of the bq2040, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2040 can be built inexpensively using a 2N7002 or BSS138 FET and an external resistor. (See Figure 1.) The value of R11 depends on the battery pack's nominal voltage.

Communicating With the bq2040

The bq2040 includes a simple two-pin (SMBC and SMBD) bi-directional serial data interface. A host processor uses the interface to access various bq2040 registers; see Table 4. This method allows battery characteristics to be monitored easily. The open-drain SMBD and SMBC pins on the bq2040 are pulled up by the host system, or may be connected to V_{SS}, if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends the battery address and an eight-bit command byte to the bq2040. The command directs the bq2040 to either store the next data received to a register specified by the command byte or output the data specified by the command byte.

bq2040 Data Protocols

The host system, acting in the role of a Bus master, uses the read word and write word protocols to communicate integer data with the bq2040. (See Figure 3).

Host-to-bq2040 Message Protocol

The Bus Host communicates with the bq2040 using one of three protocols:

- Read word
- Write word

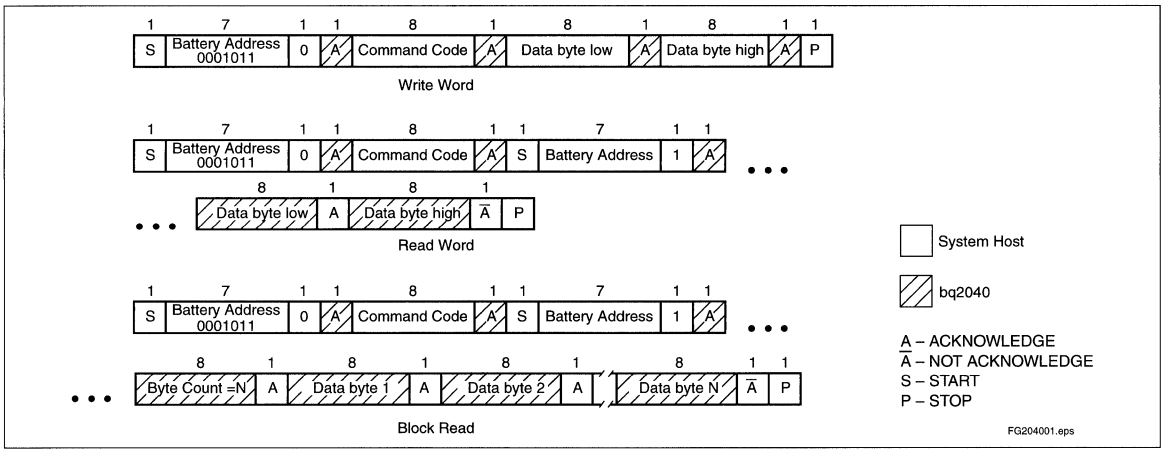


Figure 3. Host Communication Protocols

- Read block

The particular protocol used is a function of the command. The protocols used are shown in Figure 3.

Host-to-bq2040 Messages (see Table 4)

ManufacturerAccess() (0x00)

This read/write word is an open location.

Input/Output: word.

RemainingCapacityAlarm() (0x01)

This function sets or returns the low-capacity alarm value. When RM falls below the RemainingCapacityAlarm value initialized from the external EEPROM, the Remaining_Capacity_Alarm bit is set in BatteryStatus. The system may alter this alarm during operation.

Input/Output: unsigned integer. This sets/returns the value where the Remaining_Capacity_Alarm bit is set in Battery Status.

Units: mAh

Range: 0 to 65,535mAh

RemainingTimeAlarm() (0x02)

This function sets or returns the low remaining time alarm value. When the AverageTimeToEmpty falls below this value, the Remaining_Time_Alarm bit in BatteryStatus is set. The default value for this register is programmed in EE 0x02-0x03.. The system may alter this alarm during operation.

Input/Output: unsigned integer. This sets/returns the value where the Remaining_Time_Alarm bit is set in Battery Status.

Units: minutes

Range: 0 to 65,535 minutes

BatteryMode() (0x03)

This read/write word selects the various battery operational modes. The bq2040 supports the battery capacity information specified in mAh. This function also determines whether the bq2040 charging values are broadcasted to the Smart Battery Charger address.

Writing bit 14 to 1 disables voltage and current Master Mode broadcasts to the Smart Battery Charger. Bit 14 is automatically reset to 0 if SMBC and SMBD = 0 for greater than 2 seconds (i.e. pack removal).

Writing bit 13 to 1 disables all Master Mode broadcasts including alarm messages to the Smart Battery Charger and Host. The bit remains set until overwritten. Programming bit 3 of FLAGS2 in the EEPROM (EE0x3f) initializes this bit to a 1.

Bit 7 is the condition request flag. It is set when the bq2040 is initialized from the EEPROM and reset when a learning cycle has been completed. It is also set to a 1 if CycleCount increases by 32 without a new learning cycle.

AtRate() (0x04)

This read/write word is the first half of a two-function set used to set the AtRate value used in calculations made by the AtRateTimeToFull and AtRateTimeToEmpty.

Table 4. bq2040 Register Functions

Function	Code	Access	Units	Defaults[1]
ManufacturerAccess	0x00	read/write	-	-
RemaningCapacityAlarm	0x01	read/write	mAh	E^2
RemainingTimeAlarm	0x02	read/write	minutes	E^2
BatteryMode	0x03	read/write	bit flag	-
AtRate	0x04	read/write	mA	-
AtRateTimeToFull	0x05	read	minutes	-
AtRateTimeToEmpty	0x06	read	minutes	-
AtRateOK	0x07	read	Boolean	-
Temperature	0x08	read	0.1°K	2930
Voltage	0x09	read	mV	E^2
Current	0x0a	read	mA	0
AverageCurrent	0x0b	read	mA	0
MaxError	0x0c	read	percent	100
RelativeStateOfCharge	0x0d	read	percent	-
AbsoluteStateOfCharge	0x0e	read	percent	-
RemainingCapacity	0x0f	read	mAh	E^2
FullChargeCapacity	0x10	read	mAh	E^2
RunTimeToEmpty	0x11	read	minutes	-
AverageTimeToEmpty	0x12	read	minutes	-
AverageTimeToFull	0x13	read	minutes	-
ChargingCurrent	0x14	read	mA	E^2
ChargingVoltage	0x15	read	mV	E^2
Battery Status	0x16	read	bit flags	E^2
CycleCount	0x17	read	cycle	E^2
DesignCapacity	0x18	read	mAh	E^2
DesignVoltage	0x19	read	mV	E^2
SpecificationInfo	0x1a	read	-	E^2
ManufactureDate	0x1b	read	-	E^2
SerialNumber	0x1c	read	integer	E^2
Reserved	0x1d - 0x1f	-	-	-
ManufacturerName	0x20	read	string	E^2
DeviceName	0x21	read	string	E^2

Note: 1. Defaults after reset or power-up.

Table 4. bq2040 Register Functions (Continued)

Function	Code	Access	Units	Defaults[1]
DeviceChemistry	0x22	read	string	E^2
ManufacturerData	0x23	read	string	E^2
FLAG1 and FLAG2	0x2f	read	bit flags	E^2
End of Discharge Voltage 1 (EDV1)	0x3e	read	-	E^2
End of Discharge Voltage Final (EDVF)	0x3f	read	-	E^2

Note: 1. Defaults after reset or power-up.

- When the AtRate value is positive, the AtRateTimeToFull function returns the predicted time to full-charge at the AtRate value of charge.
- When the AtRate value is negative, the AtRateTimeToEmpty function returns the predicted operating time at the AtRate value of discharge.

Input/Output: signed integer. AtRate is positive for charge and negative for discharge.

Units: mA

Range: -32,768mA to 32,767mA

AtRateTimeToFull() (0x05)

This read-only word returns the predicted remaining time to fully charge the battery at the AtRate value (mA) and is valid only if read immediately after an AtRate command.

Output: unsigned integer. Returns the predicted time to full charge.

Units: minutes

Range: 0 to 65,534min

Granularity: 2 min or better

Invalid Data Indication: 65,535 indicates that the AtRate value is negative.

AtRateTimeToEmpty() (0x06)

This read-only word returns the predicted remaining operating time if the battery is discharged at the AtRate value and is valid only if read immediately after an AtRate command.

Output: unsigned integer. Returns the predicted time to empty.

Units: minutes

Range: 0 to 65,534min

Granularity: 2min or better

Invalid Data Indication: 65,535 indicates that the AtRate value is not negative.

AtRateOK() (0x07)

This read-only word returns a Boolean value that indicates whether or not the EDVF flag has been set.

Boolean: Indicates if the battery can supply additional energy.

Units: Boolean

Range: TRUE $\neq 0$, FALSE = 0

Temperature() (0x08)

This read-only word returns the cell-pack's internal temperature.

Output: unsigned integer. Returns the cell temperature in tenths of degrees Kelvin increments.

Units: 0.1°K

Range: 0 to +500.0°K

Granularity: 0.5°K or better

Accuracy: ±3°K after calibration

Voltage() (0x09)

This read-only word returns the cell-pack voltage (mV).

Output: unsigned integer. Returns the battery terminal voltage in mV.

Units: mV

Range: 0 to 65,535mV

Granularity: 0.2% of DesignVoltage

Accuracy: ±1% of DesignVoltage after calibration

Current() (0x0a)

This read-only word returns the current through the battery's terminals (mA).

Output: signed integer. Returns the charge/discharge rate in mA, where positive is for charge and negative is for discharge

Units: mA

Range: 0 to 32,767mA for charge or 0 to –32,768mA for discharge

Granularity: 0.2% of the DesignCapacity or better

Accuracy: ±1% of the DesignCapacity after calibration

AverageCurrent() (0x0b)

This read-only word returns a rolling average of the current through the battery's terminals. The AverageCurrent function returns meaningful values after the battery's first minute of operation.

Output: signed integer. Returns the charge/discharge rate in mA, where positive is for charge and negative is for discharge

Units: mA

Range: 0 to 32,767mA for charge or 0 to –32,768mA for discharge

Granularity: 0.2% of the DesignCapacity or better

Accuracy: ±1% of the DesignCapacity after calibration

MaxError() (0x0c)

Returns the expected margin of error (%) in the state of charge calculation.

Output: unsigned integer. Returns the percent uncertainty for selected information.

Units: %

Range: 0 to 100%

RelativeStateOfCharge() (0x0d)

This read-only word returns the predicted remaining battery capacity expressed as a percentage of FullChargeCapacity (%). **RelativeStateOfCharge is only valid for battery capacities more than 1504mAh and less than 10,400mAh.**

Output: unsigned integer. Returns the percent of remaining capacity.

Units: %

Range: 0 to 100%

Granularity: 1%

Accuracy: ±MaxError after circuit and capacity calibration

AbsoluteStateOfCharge() (0x0e)

This read-only word returns the predicted remaining battery capacity expressed as a percentage of DesignCapacity (%). Note that AbsoluteStateOfCharge can return values greater than 100%. **Absolute StateOfCharge is only valid for battery capacities more than 1504mAh and less than 10,400mAh**.

Output: unsigned integer. Returns the percent of remaining capacity.

Units: %

Range: 0 to 65,535%

Granularity: 1%

Accuracy: ±MaxError after circuit and capacity calibration

RemainingCapacity() (0x0f)

This read-only word returns the predicted remaining battery capacity. The RemainingCapacity value is expressed in mAh.

Output: unsigned integer. Returns the estimated remaining capacity in mAh.

Units: mAh

Range: 0 to 65,535mAh

Granularity: 0.2% of DesignCapacity or better

Accuracy: ±MaxError * FCC after circuit and capacity calibration

FullChargeCapacity() (0x10)

This read-only word returns the predicted pack capacity when it is fully charged. FullChargeCapacity defaults to the value programmed in the external EEPROM until a new pack capacity is learned. The new FCC is stored to EEPROM within 400ms of a valid charge after a qualified discharge.

Output: unsigned integer. Returns the estimated full charge capacity in mAh.

Units: mAh

Range: 0 to 65,535mAh

Granularity: 0.2% of DesignCapacity or better

Accuracy: ±MaxError * FCC after circuit and capacity calibration

RunTimeToEmpty() (0x11)

This read-only word returns the predicted remaining battery life at the present rate of discharge (minutes). The RunTimeToEmpty value is calculated based on Current.

Output: unsigned integer. Returns the minutes of operation left.

Units: minutes

Range: 0 to 65,534min

Granularity: 2min or better

Invalid data indication: 65,535 indicates battery is not being discharged.

AverageTimeToEmpty() (0x12)

This read-only word returns the predicted remaining battery life at the present average discharge rate (minutes). The AverageTimeToEmpty is calculated based on AverageCurrent.

Output: unsigned integer. Returns the minutes of operation left.

Units: minutes

Range: 0 to 65,534min

Granularity: 2min or better

Invalid data indication: 65,535 indicates battery is not being discharged.

AverageTimeToFull() (0x13)

This read-only word returns the predicted time until the Smart Battery reaches full charge at the present average charge rate (minutes).

Output: unsigned integer. Returns the remaining time in minutes to full.

Units: minutes

Range: 0 to 65,534min

Granularity: 2min or better

Invalid data indication: 65,535 indicates battery is not being charged.

ChargingCurrent() (0x14)

If enabled, the bq2040 sends the desired charging rate in mA to the Smart Battery Charger.

Output: unsigned integer. Transmits/returns the maximum charger output current in mA.

Units: mA

Range: 0 to 65,534mA

Granularity: 0.2% of the design capacity or better

Invalid data indication: 65,535 indicates that the Smart Charger should operate as a voltage source outside its maximum regulated current range.

ChargingVoltage() (0x15)

If enabled, the bq2040 sends the desired voltage in mV to the Smart Battery Charger.

Output: unsigned integer. Transmits/returns the charger voltage output in mV.

Units: mV

Range: 0 to 65,534mV

Granularity: 0.2% of the DesignVoltage or better

Invalid data indication: 65,535 indicates that the Smart Battery Charger should operate as a current source outside its maximum regulated voltage range.

16/30

BatteryStatus() (0x16)

This read-only word returns the battery status word.

Output: unsigned integer. Returns the status register with alarm conditions bitmapped as shown in Table 5.

Some of the BatteryStatus flags (Remaining_Capacity_Alarm and Remaining_Time_Alarm) are calculated based on current. See Table 8 and 9 for definitions.

Table 5. Status Register

Alarm Bits	
0x8000	Over_Charged_Alarm
0x4000	Terminate_Charge_Alarm
0x2000	Reserved
0x1000	Over_Temp_Alarm
0x0800	Terminate_Discharge_Alarm
0x0400	Reserved
0x0200	Remaining_Capacity_Alarm
0x0100	Remaining_Time_Alarm
Status Bits	
0x0080	Initialized
0x0040	Discharging
0x0020	Fully_Charged
0x0010	Fully_Discharged
Error Code	
0x0000-0x000f	Reserved for error codes

CycleCount() (0x17)

This read-only word returns the number of charge/discharge cycles the battery has experienced. A charge/discharge cycle starts from a base value equivalent to the battery's state-of-charge on completion of a charge cycle. The bq2040 increments the cycle counter during the current charge cycle if the battery has been discharged 15% below the state-of-charge at the end of the last charge cycle. This prevents false reporting of small charge/discharge cycles. The cycle count is stored in EEPROM within 400ms of an update.

Output: unsigned integer. Returns the count of charge/discharge cycles the battery has experienced.

Units: cycles

Table 6. Bit Descriptions for FLAGS1 and FLAGS2

	(MSB) 7	6	5	4	3	2	1	0 (LSB)
FLAGS2	DMODE	PSTAT	CHM	CC	-	OV	LTF	OC
FLAGS1	ΔT/Δt	I_{MIN}	VQ	-	VDQ	OVLD	EDV1	EDVF

Note: - = Reserved

Range: 0 to 65,535 cycles; 65,535 indicates battery has experienced 65,535 or more cycles.

Granularity: 1 cycle

DesignCapacity() (0x18)

This read-only word returns the theoretical capacity of a new pack. The DesignCapacity value is expressed in mAh at the nominal discharge rate.

Output: unsigned integer. Returns the battery capacity in mAh.

Units: mAh

Range: 0 to 65,535mAh

DesignVoltage() (0x19)

This read-only word returns the theoretical voltage of a new pack in mV.

Output: unsigned integer. Returns the battery's normal terminal voltage in mV.

Units: mV

Range: 0 to 65,535mV

SpecificationInfo() (0x1a)

This read-only word returns the specification revision the bq2040 supports.

ManufactureDate() (0x1b)

This read-only word returns the date the cell was manufactured in a packed integer word. The date is packed as follows: (year - 1980) * 512 + month * 32 + day.

Field	Bits Used	Format	Allowable Value
Day	0–4	5-bit binary value	1–31 (corresponds to date)
Month	5–8	4-bit binary value	1–12 (corresponds to month number)
Year	9–15	7-bit binary value	0–127 (corresponds to year biased by 1980)

SerialNumber() (0x1c)

This read-only word returns a serial number. This number, when combined with the ManufacturerName, the DeviceName, and the ManufactureDate, uniquely identifies the battery.

Output: unsigned integer

ManufacturerName() (0x20)

This read-only string returns a character string where the first byte is the number of characters available. The maximum number of characters is 11. The character string contains the battery manufacturer's name. For example, "Benchmarq" identifies the battery pack manufacturer as Benchmarq.

Output: string or ASCII character string

DeviceName() (0x21)

This read-only string returns a character string where the first byte is the number of characters available. The maximum number of characters is 7. The 7-byte character string contains the battery's name. For example, a DeviceName of "bq2040" indicates that the battery is a model bq2040.

Output: string or ASCII character string

DeviceChemistry() (0x22)

This read-only string returns a character string where the first byte is the number of characters available. The maximum number of characters is 5. The 5-byte character string contains the battery's chemistry. For example, if the DeviceChemistry function returns "NiMH," the battery pack contains nickel-metal hydride cells.

Output: string or ASCII character string

ManufacturerData() (0x23)

This read-only string allows access to an up to 5-byte manufacturer data string.

Output: block data—data whose meaning is assigned by the Smart Battery's manufacturer.

End of Discharge Voltage1 (0x3e)

This read-only word returns the first end-of-discharge voltage programmed for the pack.

Output: two's complemented unsigned integer. Returns battery end-of-discharge voltage programmed in EEPROM in mV.

End of Discharge VoltageF (0x3f)

This read-only word returns the final end-of-discharge voltage programmed for the pack.

Output: two's complemented unsigned integer. Returns battery final end-of-discharge voltage programmed in EEPROM in mV.

FLAGS1&2() (0x2f)

This read-only register returns an unsigned integer representing the internal status registers of the bq2040. The MSB represents FLAGS2, and the LSB represents FLAGS1. See Table 6 for the bit description for FLAGS1 and FLAGS2.

FLAGS2

The *Display Mode* flag (DMODE), bit 7 determines whether the bq2040 displays Relative or Absolute capacity.

The DMODE value is:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
DMODE	-	-	-	-	-	-	-

Where DMODE is:

0 Selects Absolute display

1 Selects Relative display

Bit 6 reflects the high/low state of PSTAT. PSTAT ≥1.5V generates a charge suspend condition.

The PSTAT value is:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
-	PSTAT	-	-	-	-	-	-

Where PSTAT is:

0 PSTAT input < 1.0V

1 PSTAT input ≥ 1.5V

The *Chemistry* flag (CHM), bit 5, selects Li-Ion or nickel compensation factors.

The CHM value is:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
-	-	CHM	-	-	-	-	-

Where CHM is:

0 Selects Nickel

1 Selects Li-Ion

Bit 4, the *Charge Control* flag (CC), determines whether a bq2040-based charge termination will set RM to a user-defined programmable full charge capacity.

The CC value is:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	CC	-	-	-	-

Where CC is:

0 RM is not modified on valid bq2040 charge termination

1 RM is set to a programmable percentage of the FCC when a valid bq2040 charge termination occurs

Bit 3 is reserved.

Bit 2, the *Overvoltage* flag (OV), is set when the bq2040 detects a pack voltage 5% greater than the programmed charging voltage. This bit is cleared when the pack voltage falls 5% below the programmed charging voltage.

The OV value is:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	OV	-	-

Where OV is:

0 Voltage < 1.05 * ChargingVoltage

1 Voltage ≥ 1.05 * ChargingVoltage

Bit 1, the *Low Temperature Fault* flag (LTF), is set when Temperature is < 12°C and cleared when Temperature is ≥ 15°C.

The LTF value is:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	LTF	-

Where LTF is:

0 Temperature > 15°C

1 Temperature < 12°C

Bit 0, the *Overcurrent* flag (OC), is set when Current is 25% greater than the programmed charging current. If the charging current is programmed less than 1024mA, overcurrent is set if Current is 256mA greater than the programmed charging current. This flag is cleared when Current falls below 256mA.

The OC value is:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OC

Where OC is:

0 Current is less than 1.25 * ChargingCurrent or less than 256mA if charging current is programmed less than 1024mA

1 Current exceeds 1.25 * ChargingCurrent or 256mA if the charging current is programmed less than 1024mA. This bit is cleared if Current < 256mA.

FLAGS1

Bits 7 indicates that a ΔT/Δt termination condition exists.

The ΔT/Δt value is:

FLAGS1 Bits							
7	6	5	4	3	2	1	0
ΔT/Δt	-	-	-	-	-	-	-

Where ΔT/Δt is:

0 The ΔT/Δt rate drops below the programmed rate.

1 The ΔT/Δt rate exceeds the programmed rate.

Bit 6 indicates that a current taper termination condition exists.

FLAGS1 Bits							
7	6	5	4	3	2	1	0
-	I_{MIN}	-	-	-	-	-	-

The I_{MIN} value is:

Where I_{MIN} is:

0 A valid current taper termination condition is not present.

1 Valid current taper termination condition detected.

The *Valid Charge* flag (VQ), bit 5, is set when $V_{SRO} \geq |V_{SRD}|$ and 10mAh of charge has accumulated. This bit is cleared during a discharge and when $V_{SRO} \leq |V_{SRD}|$.

FLAGS1 Bits							
7	6	5	4	3	2	1	0
-	-	VQ	-	-	-	-	-

The VQ value is:

Where VQ is:

0 $V_{SRO} \leq |V_{SRD}|$

1 $V_{SRO} \geq |V_{SRD}|$ and 10mAh of charge has accumulated

Bit 4 is reserved.

The *Valid Discharge* flag (VDQ), bit 3, is set when a valid discharge is occurring (discharge cycle valid for learning new full charge capacity) and cleared if a partial charge is detected, EDV1 is asserted when T < 0°C, or self-discharge accounts for more than 256mAh of the discharge.

FLAGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

The VDQ value is:

Where VDQ is:

0 Self-discharge is greater than 256mAh, EDV1 = 1 when T < 0°C or VQ = 1

1 On first discharge after RM=FCC

The Overload flag (OVLD), bit 2, is set when the discharge current is greater than the programmed rate and cleared when the discharge current falls below the programmed rate.

FLAGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	OVLD	-	-

The OVLD value is:

Where OVLD is:

0 Current < programmed rate

1 Current > programmed rate

The *First End-of-Discharge Voltage* flag (EDV1), bit 1, is set when Voltage < EDV1 and OVLD = 0 and cleared when VQ = 1 and Voltage > EDV1.

FLAGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV1	-

The EDV1 value is:

Where EDV1 is:

0 VQ = 1 and Voltage > EDV1

1 Voltage < EDV1 and OVLD = 0

The *Final End-of-Discharge Voltage* flag (EDVF), bit 0, is set when Voltage < EDVF and OVLD = 0 and cleared when VQ = 1 and Voltage > EDVF.

FLAGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	EDVF

The EDVF value is:

Where EDVF is:

0 VQ = 1 and Voltage > EDVF

1 Voltage < EDVF and OVLD = 0

Error Codes and Status Bits

Error codes and status bits are listed in Table 8 and Table 9, respectively.

SBD Seal

The bq2040 address space can be "locked" to enforce the SBS specified access to each command code. To lock the address space, the bq2040 must be initialized with EE 0x3d set to b0h. Once this is done, only commands 0x00-0x04 may be written. Attempting to write to any other address will cause a "no acknowledge" of the data. Reading will only be permitted from the command codes listed in the SBD specification plus the five locations designated as optional manufacturing functions 1–5 (0x2f, 0x3c–0x3f).

Programming the bq2040

The bq2040 requires the proper programming of an external EEPROM for proper device operation. Each module can be calibrated for the greatest accuracy, or general "default" values can be used. An EV2200-40 programming kit (interface board, software, and cable) for an IBM-compatible PC is available from Benchmarq.

The bq2040 uses a 24LC01 or equivalent serial EEPROM (capable of read operation to 2.0V) for storing the various initial values, calibration data, and string information. Table 1 outlines the parameters and addresses for this information. Tables 10 and 11 detail the various register contents and show an example program value for an 2400mAh 4-series Li-Ion battery pack, using a 50mΩ sense resistor.

Table 8. Error Codes (BatteryStatus() (0x16))

Error	Code	Access	Description
OK	0x0000	read/write	bq2040 processed the function code without detecting any errors.
Busy	0x0001	read/write	bq2040 is unable to process the function code at this time.
ReservedCommand	0x0002	read/write	bq2040 cannot read or write the data at this time—try again later.
UnsupportedCommand	0x0003	read/write	bq2040 does not support the requested function code.
AccessDenied	0x0004	write	bq2040 detected an attempt to write to a read-only function code.
Overflow/Underflow	0x0005	read/write	bq2040 detected a data overflow or underflow.
BadSize	0x0006	write	bq2040 detected an attempt to write to a function code with an incorrect size data block.
UnknownError	0x0007	read/write	bq2040 detected an unidentifiable error.

Note: Reading the bq2040 after an error clears the error code.

Table 9. BatteryStatus Bits

Alarm Bits		
Bit Name	**Set When:**	**Reset When:**
OVER_CHARGED_ALARM	The bq2040 detects a ΔT/Δt or current taper termination. (**Note: ΔT/Δt and current taper are valid charge terminations.**)	A discharge occurs or when the ΔT/Δt or current taper termination condition ceases during charge.
TERMINATE_CHARGE_ALARM	The bq2040 detects an over-current, over-voltage, over-temperature, ΔT/Δt, or current taper condition during charge.	A discharge occurs or when all conditions causing the event cease.
OVER_TEMP_ALARM	The bq2040 detects that its internal temperature is greater than the programmed value.	Internal temperature falls to 43°C or the maximum temperature threshold minus 5°C.
TERMINATE_DISCHARGE_ALARM	The bq2040 determines that it has supplied all the charge that it can without being damaged (Voltage < EDVF).	Voltage > EDVF signifies that the battery has reached a state of charge sufficient for it to once again safely supply power.
REMAINING_CAPACITY_ALARM	The bq2040 detects that the RemainingCapacity is less than that set by the RemainingCapacityAlarm function.	Either the value set by the RemainingCapacityAlarm function is lower than the Remaining Capacity or the RemainingCapacity is increased by charging.
REMAINING_TIME_ALARM	The bq2040 detects that the estimated remaining time at the present discharge rate is less than that set by the RemainingTimeAlarm function.	Either the value set by the RemainingTimeAlarm function is lower than the AverageTimeToEmpty or a valid charge is detected.
Status Bits		
Bit Name	**Set When:**	**Reset When:**
INITIALIZED	The bq2040 loads from the EEPROM (bit 7 set in EE0x0c).	A bad EEPROM load is detected.
DISCHARGING	The bq2040 determines that it is not being charged.	Battery detects that it is being charged.
FULLY_CHARGED	The bq2040 determines a valid charge termination or a maximum overcharge state.	RM discharges below the full charge percentage.
FULLY_DISCHARGED	bq2040 determines that it has supplied all the charge that it can without being damaged.	RelativeStateOfCharge is greater than or equal to 20%

Table 10. Example Register Contents

Description	EEPROM Address		EEPROM Hex Contents		Example Values	Notes
	Low Byte	High Byte	Low Byte	High Byte		
EEPROM length	0x00		64		100	Must be equal to 0x64.
EEPROM check 1	0x01		5b		91	Must be equal to 0x5b.
Remaining time alarm	0x02	0x03	0a	00	10 minutes	Sets the low time alarm level.
Remaining capacity alarm	0x04	0x05	f0	00	240mAh	Sets the low capacity alarm level.
Reserved	0x06	0x07	00	00	0	Not currently used by the bq2040.
Initial charging current	0x08	0x09	60	09	2400mA	Sets the initial charge request.
Charging voltage	0x0a	0x0b	d8	40	16600mV	Used to set the fast-charge voltage for the Smart Charger.
Battery status	0x0c	0x0d	80	00	128	Initializes BatteryStatus.
Cycle count	0x0e	0x0f	00	00	0	Contains the charge cycle count and can be set to zero for a new battery.
Design capacity	0x10	0x11	60	09	2400mAh	Normal battery pack capacity.
Design voltage	0x12	0x13	40	38	14400mV	Nominal battery pack voltage.
Specification information	0x14	0x15	10	00	1.0	Default value for this register in a 1.0 part.
Manufacture date	0x16	0x17	a1	20	May 1, 1996 = 8353	Packed per the ManufactureDate description.
Serial number	0x18	0x19	12	27	10002	Contains the optional pack serial number.
Fast-charging current	0x1a	0x1b	60	09	2400mA	Used to set the fast-charge current for the Smart Charger.
Maintenance charge current	0x1c	0x1d	00	00	0mA	Contains the desired maintenance current after fast-charge termination by the bq2040.
Reserved	0x1e	0x1f	00	00	0	Must be programmed to 0x00.
Current overload	0x2c	0x2d	70	17	6000mA	Sets the discharge current at which EDV threshold monitoring is disabled.
Battery low %	0x2e		08		3%	Sets the battery capacity that RemainingCapacity is reduced to at EDV1. The value equals 2.56 * (%RM at EDV1)

Table 10. Example Register Contents (Continued)

Description	EEPROM Address		EEPROM Hex Contents		Example Values	Notes
	Low Byte	High Byte	Low Byte	High Byte		
Reserved	0x2f		00		0	Not currently used by the bq2040.
Li-Ion taper current	0x38	0x39	10	ff	240mA	Sets the upper taper limit for Li-Ion charge termination. Stored in 2's complement.
Maximum overcharge limit	0x3a	0x3b	9c	ff	100mAh	Sets the maximum amount of overcharge before a maximum overcharge charge suspend occurs. Stored in 2's complement.
Reserved	0x3c		00		0	Must be programmed to 0.
Access protect	0x3d		b0		SBD access only	If the bq2040 is reset and bit 3 of this location is 0, the bq2040 locks access to any command outside of the SBS data set. Program to 0xb8 for full R/W access, 0xb0 for SBD access only.
FLAGS1	0x3e		00		0	Initializes FLAGS1
FLAGS2	0x3f		b0		Relative display Li-Ion chemistry bq2040 charge control	Initializes FLAGS2.
Current measurement gain[1]	0x46	0x47	00	0f	3840	The current gain measurement and current integration gain are related and defined for the bq2040 current measurement. This word equals 192/sense resistor value in ohms.
Battery voltage offset[1]	0x48		fe		-2mV	Used to adjust the battery voltage offset according to the following: Voltage = (V_{SB}(mV) + V_{OFF}) * Voltage gain
Temperature offset[1]	0x49		8a		13.8°C	The default value (zero adjustment) for the offset is 12.8°C or 0x80. $TOFF_{NEW}$ = $TOFF_{CURRENT}$ + ($TEMP_{ACTUAL}$ - $TEMP_{REPORTED}$)* 10
Maximum temperature and ΔT step	0x4a		5f		Maximum temperature = 61.0°C ΔT step = 4.6°C	Maximum charge temperature is 69- (mt * 1.6)°C (mt = upper nibble). The ΔT step is (dT * 2 + 16)/10°C (dT = lower nibble).
Charge efficiency	0x4b		ff		Maintenance compensation = 100% Fast compensation = 100%	Sets the fast-charge (high) and maintenance charge (low) efficiencies. The upper nibbles sets the low efficiency and the lower nibble adjusts the high efficiency according to the equation: Nibble = (efficiency% * 256 - 196)/4
Full-charge percentage	0x4c		9c		100%	This packed field is the two's complement of the desired value in RM when the bq2040 determines a full-charge termination. If RM is below this value, RM is set to this value. If RM is above this value, then RM is not adjusted.

Note: 1. Can be adjusted to calibrate the battery pack.

24/30

Table 10. Example Register Contents (Continued)

Description	EEPROM Address		EEPROM Hex Contents		Example Values	Notes
	Low Byte	High Byte	Low Byte	High Byte		
Digital filter	0x4d		96		0.30mV	Used to set the digital magnitude filter as described in Table 2.
Current integration gain[1]	0x4e		40	0	3.2/0.05	Represents the following: 3.2/sense resistor in ohms. It is used by the bq2040 to scale the measured voltage values on the SR pin in mA and mAh. This register also compensates for variations in the reported sense resistor value.
Self-discharge rate	0x4f		2d		0.25%	This packed field is the two's complement of (52.73/x) where x is the desired self-discharge rate per day (%) at room temperature.
Voltage gain[1]	0x56	0x57	17	07	7.09	Voltage gain is packed as two units. For example, (R4 + R5)/R4 = 7.09 would be stored as: whole number stored in 0x57 as 7 and the decimal component stored in 0x56 as 256 x 0.09 = 23(= 17h).
Reserved	0x58	0x59	00	00	0	Should be programmed to 0.
EDVF charging current	0x5a	0x5b	64	00	100mA	Contains the desired charge current below EDVF.
End of discharge voltage 1	0x5c	0x5d	20	d1	12000mV	The value programmed is the two's complement of the threshold voltage in mV.
End-of-discharge voltage final	0x5e	0x5f	40	d4	11200mV	The value programmed is the two's complement of the threshold voltage in mV.
Full charge capacity	0x60	0x61	d0	07	2000mA	This value sets the initial estimated pack capacity.
Δt step	0x62		0f		20s	The Δt step for $\Delta T/\Delta t$ termination equals 320 - (byte value * 20).
Hold-off time	0x63		00		320s hold-off	The hold-off time is 320 - (byte value * 20).
EEPROM check 2	0x64		b5		181	Must be equal to 0xb5.
Reserved	0x65	0x7f			NA	Not currently used by the bq2040.

Note: 1. Can be adjusted to calibrate the battery pack.

Table 11. Example Register Contents (String Data)

String Description	Address	0x X0	0x X1	0x X2	0x X3	0x X4	0x X5	0x X6	0x X7	0x X8	0x X9	0x Xa	0x Xb
Manufacturer name	0x20- 0x2b	09	42 B	45 E	4e N	43 C	48 H	4d M	41 A	52 R	51 Q	-	-
Device name	0x30- 0x37	06	42 B	51 Q	32 2	30 0	34 4	30 0	-				
Device chemistry	0x40- 0x45	04	6c L	69 I	4f O	4e N	-						
Manufacturer data	0x50- 0x55	05	42 B	51 Q	32 2	30 0	32 2						

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
REF	Relative to V_{SS}	-0.3	+8.5	V	Current limited by R11 (see Figure 1)
V_{SR}	Relative to V_{SS}	-0.3	+7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery.
T_{OPR}	Operating temperature	0	+70	°C	Commercial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 5.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
E_{VSB}	Battery voltage error relative to SB	-50mV	-	50mV	V	See note

Note: The accuracy of the voltage measurement may be improved by adjusting the battery voltage offset and gain, stored in external EEPROM. For best operation, V_{CC} should be 1.5V greater than V_{SB}.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V
		-	120	180	µA	V_{CC} = 4.25V
		-	170	250	µA	V_{CC} = 5.5V
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	0 < V_{SB} < V_{CC}
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	V_{DISP} = V_{SS}
I_{LVOUT}	V_{OUT} output leakage	-0.2	-	0.2	µA	EEPROM off
V_{SR}	Sense resistor input	-0.3	-	2.0	V	V_{SR} < V_{SS} = discharge; V_{SR} > V_{SS} = charge
R_{SR}	SR input impedance	10	-	-	MΩ	-200mV < V_{SR} < V_{CC}
V_{IH}	Logic input high	0.5 * V_{CC}	-	V_{CC}	V	ESCL, ESDA
		1.4	-	5.5	V	SMBC, SMBD
V_{IL}	Logic input low	0	-	0.3 * V_{CC}	V	ESCL, ESDA
		-0.5		0.6	V	SMBC, SMBD
V_{OL}	Data, clock output low	-	-	0.4	V	I_{OL}=350µA, SMBC, SMBD
I_{OL}	Sink current	100	-	350	µA	V_{OL}≤0.4V, SMBC, SMBD
V_{OLSL}	LED_X output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, I_{OLS} ≤ 1.75mA LED_1–LED_4
V_{OLSH}	LED_X output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, I_{OLS} ≤ 11.0mA LED_1–LED_4
V_{OHVL}	V_{OUT} output, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{VOUT} = -5.25mA
V_{OHVH}	V_{OUT} output, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} = 6.5V, I_{VOUT} = -33.0mA
I_{VOUT}	V_{OUT} source current	-33	-	-	mA	At V_{OHVH} = V_{CC} - 0.6V
I_{OLS}	LED_X sink current	11.0	-		mA	At V_{OLSH} = 0.4V

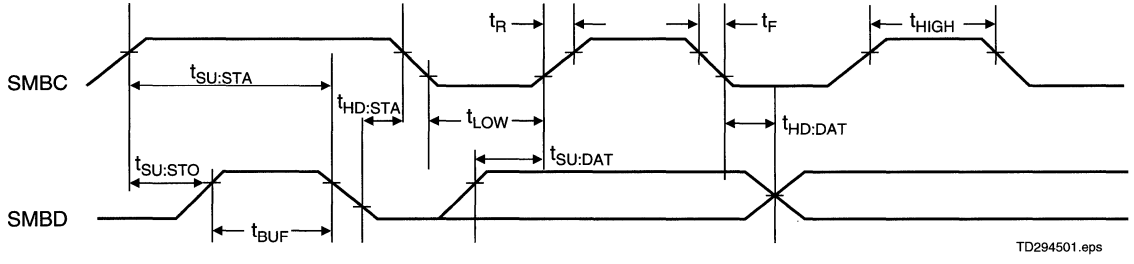
Note: All voltages relative to V_{SS}.

AC Specifications

Symbol	Parameter	Min	Max	Units	Notes
F_{SMB}	SMBus operating frequency	10	100	KHz	
T_{BUF}	Bus free time between stop and start condition	4.7		µs	
$T_{HD:STA}$	Hold time after (repeated) start condition	4.0		µs	
$T_{SU:STA}$	Repeated start condition setup time	4.7		µs	
$T_{SU:STO}$	Stop condition setup time	4.0		µs	
$T_{HD:DAT}$	Data hold time	300		ns	
$T_{SU:DAT}$	Data setup time	250		ns	
T_{LOW}	Clock low period	4.7		µs	
T_{HIGH}	Clock high period	4.0		µs	
T_F	Clock/data fall time		300	ns	
T_R	Clock/data rise time		1000	ns	
$T_{LOW:SEXT}$	Cumulative clock low extend time (slave)		25	ms	
$T_{TIMEOUT}$		25	35	ms	

4

Bus Timing Data



Data Sheet Revision History

Change No.	Page No.	Description of Change
3	3	Updated recommended application schematic.
3	9	Changed overcurrent fault conditon for ChargingCurrent < 1024mA.
3	10	4Hz operation of LED clarification.
3	11	Added descriptions for bits 7 and 13 of BatteryMode.
3	14	AtRateTimeToEmpty and AtRateTimeToFull invalid data indication correction.
3	15, 16	RunTimeToEmpty, AverageTimeToEmpty and AverageTimeToFull invalid data indication corrections.
3	23	Changed typical Battery low % value for Li-Ion with EDV1 = 3.0V/cell.
3	24	Li-Ion taper current is stored in 2's complement.
3	24	Changed typical ΔT step and Full-charge percentage for Li-Ion.
3	25	Voltage gain is (R4 + R5)/R4.
3	25	Changed typical EDV1 and EDVF values for Li-Ion.
4	6	Added V_{SB} should not exceed 2.4V
4	8	The self discharge rate *approximately* doubles or halves
4	11	Changed cycle count increase from 30 to 32 for condition request.
4	14	Changed AtRateOK() indication from EDV1 to EDVF
4	25	Changed self-discharge programming from 52.75/x to 52.73/x.
4	25	Changed recommended EDVF charging current from 0mA to 100mA

Notes: Changes 1 and 2 refer to the 1998 Data Book
Change 3 = June1998 D changes from Jan. 1998 C.
Change 4 = June 1999 E changes from June 1998 D.

Ordering Information

bq2040

Temperature Range:
blank = Commercial (0 to 70°C)

Package Option:
SN = 16-pin narrow SOIC

Device:
bq2040 Gas Gauge IC With SMBus Interface

30/30

UNITRODE

bq2050

Lithium Ion Power Gauge™ IC

Features

- Conservative and repeatable measurement of available capacity in Lithium Ion rechargeable batteries
- Designed for battery pack integration
  - 120µA typical operating current
  - Small size enables implementations in as little as ½ square inch of PCB
- Integrate within a system or as a stand-alone device
  - Display capacity via single-wire serial communication port or direct drive of LEDs
- Measurements compensated for current and temperature
- Self-discharge compensation using internal temperature sensor
- 16-pin narrow SOIC

General Description

The bq2050 Lithium Ion Power Gauge™ IC is intended for battery-pack or in-system installation to maintain an accurate record of available battery capacity. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery. Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and self-discharge calculations to provide available capacity information across a wide range of operating conditions. Battery capacity is automatically recalibrated, or "learned," in the course of a discharge cycle from full to empty.

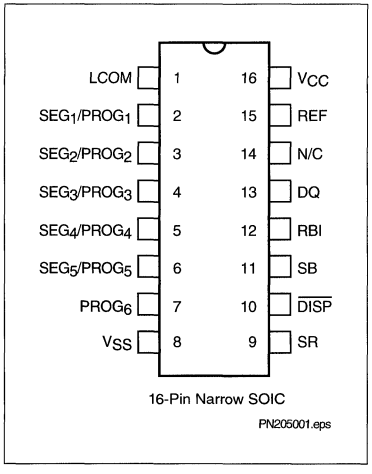
Nominal available capacity may be directly indicated using a five-segment LED display. These segments are used to graphically indicate available capacity. The bq2050 supports a simple single-line bidirectional serial link to an external processor (common ground). The bq2050 outputs battery information in response to external commands over the serial link.

The bq2050 may operate directly from one cell (V_{BAT} > 3V). With the REF output and an external transistor, a simple, inexpensive regulator can be built for systems with more than one series cell.

Internal registers include available capacity, temperature, scaled available energy, battery ID, battery status, and programming pin settings. To support subassembly testing, the outputs may also be controlled. The external processor may also overwrite some of the bq2050 power gauge data registers.

4

Pin Connections



16-Pin Narrow SOIC

PN205001.eps

Pin Names

LCOM	LED common output	REF	Voltage reference output
$SEG_1/PROG_1$	LED segment 1/ program 1 input	N/C	No connect
$SEG_2/PROG_2$	LED segment 2/ program 2 input	DQ	Serial communications input/output
$SEG_3/PROG_3$	LED segment 3/ program 3 input	RBI	Register backup input
$SEG_4/PROG_4$	LED segment 4/ program 4 input	SB	Battery sense input
$SEG_5/PROG_5$	LED segment 5/ program 5 input	$\overline{DISP}$	Display control input
$PROG_6$	Program 6 input	SR	Sense resistor input
		V_{CC}	3.0–6.5V
		V_{SS}	System ground

Pin Descriptions

LCOM **LED common output**

Open-drain output switches V_{CC} to source current for the LEDs. The switch is off during initialization to allow reading of the soft pull-up or pull-down program resistors. LCOM is also high impedance when the display is off.

SEG_1–SEG_5 **LED display segment outputs (dual function with $PROG_1$–$PROG_6$)**

Each output may activate an LED to sink the current sourced from LCOM.

$PROG_1$–$PROG_2$ **Programmed full count selection inputs (dual function with SEG_1–SEG_2)**

These three-level input pins define the programmed full count (PFC) thresholds described in Table 2.

$PROG_3$–$PROG_4$ **Power gauge rate selection inputs (dual function with SEG_3–SEG_4)**

These three-level input pins define the scale factor described in Table 2.

$PROG_5$ **Self-discharge rate selection (dual function with SEG_5)**

This three-level input pin defines the selfdischarge and battery compensation factors as shown in Table 1.

$PROG_6$ **Capacity initialization selection**

This three-level pin defines the battery state of charge at reset as shown in Table 1.

N/C **No connect**

SR **Sense resistor input**

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied between the negative terminal of the battery and the sense resistor. $V_{SR} < V_{SS}$ indicates discharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2050 is $V_{SR} + V_{OS}$.

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ tied to V_{CC} allows $PROG_X$ to connect directly to V_{CC} or V_{SS} instead of through a pull-up or pull-down resistor. $\overline{DISP}$ floating allows the LED display to be active during charge. $\overline{DISP}$ low activates the display. See Table 1.

SB **Secondary battery input**

This input monitors the battery cell voltage potential through a high-impedance resistive divider network for end-of-discharge voltage (EDV) thresholds, and battery removed.

RBI **Register backup input**

This pin is used to provide backup potential to the bq2050 registers during periods when $V_{CC} \leq 3V$. A storage capacitor or a battery can be connected to RBI.

DQ **Serial I/O pin**

This is an open-drain bidirectional pin.

REF **Voltage reference output for regulator**

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} **Supply voltage input**

V_{SS} **Ground**

Functional Description

General Operation

The bq2050 determines battery capacity by monitoring the amount of current input to or removed from a rechargeable battery. The bq2050 measures discharge and charge currents, measures battery voltage, estimates self-discharge, monitors the battery for low battery voltage thresholds, and compensates for temperature and charge/discharge rates. The current measurement is made by monitoring the voltage across a small-value series sense resistor between the negative battery terminal and ground. The estimate of scaled available energy is made using the remaining average battery voltage during the discharge cycle and the remaining nominal available charge. The scaled available energy measurement is corrected for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2050 using the LED display capability as a charge-state indicator. The bq2050 is configured to display capacity in relative display mode. The relative display mode uses the last measured discharge capacity of the battery as the battery "full" reference. A push-button display feature is available for momentarily enabling the LED display.

The bq2050 monitors the charge and discharge currents as a voltage across a sense resistor (see R_S in Figure 1). A filter between the negative battery terminal and the SR pin may be required if the rate of change of the battery current is too great.

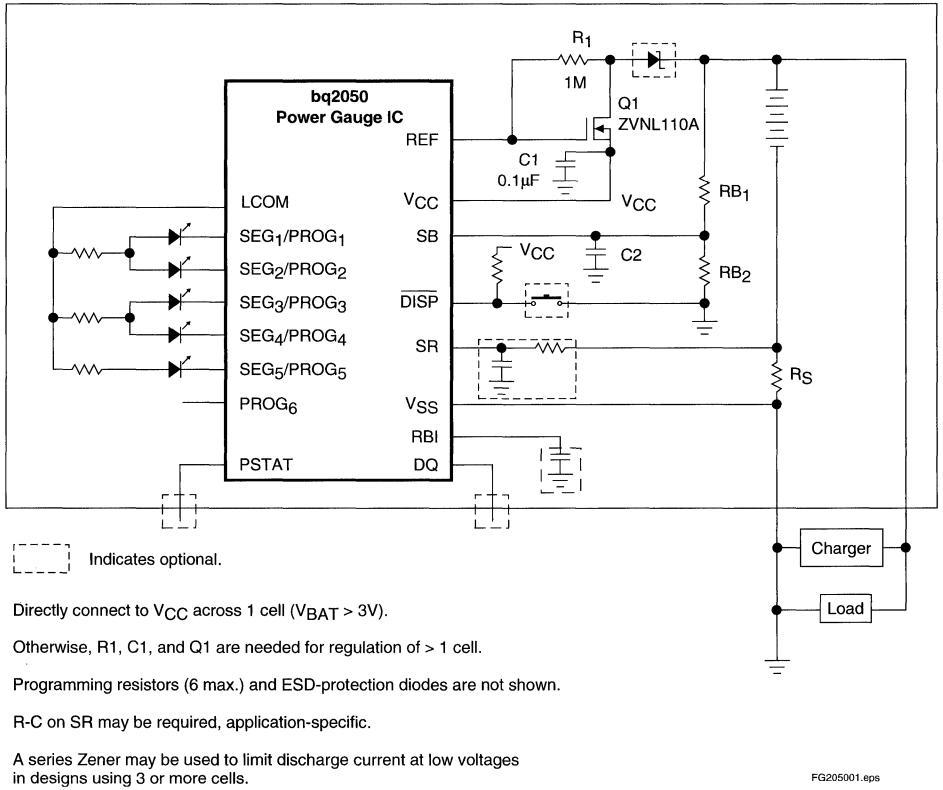


Figure 1. Battery Pack Application Diagram—LED Display

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2050 monitors the battery potential through the SB pin. The voltage is determined through a resistor-divider network per the following equation:

$$\frac{RB1}{RB2} = 2N - 1$$

where N is the number of cells, RB1 is connected to the positive battery terminal, and RB2 is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV). EDV threshold levels are used to determine when the battery has reached an "empty" state.

Two EDV thresholds for the bq2050 are programmable with the default values fixed at:

EDV1 (early warning) = 1.52V

EDVF (empty) = 1.47V

If V_{SB} is below either of the two EDV thresholds, the associated flag is latched and remains latched, independent of V_{SB}, until the next valid charge. The V_{SB} value is also available over the serial port.

During discharge and charge, the bq2050 monitors V_{SR} for various thresholds used to compensate the charge and discharge rates. Refer to the count compensation section for details. EDV monitoring is disabled if the discharge rate is greater than 2C (typical) and resumes ½ second after the rate falls below 2C.

RBI Input

The RBI input pin is intended to be used with a storage capacitor or external supply to provide backup potential to the internal bq2050 registers when V_{CC} drops below 3.0V. V_{CC} is output on RBI when V_{CC} is above 3.0V. A diode is required to isolate the external supply.

Reset

The bq2050 can be reset either by removing V_{CC} and grounding the RBI pin for 15 seconds or by writing 0x80 to register 0x39.

Temperature

The bq2050 internally determines the temperature in 10°C steps centered from approximately -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available charge display translation. The temperature range is available over the serial port in 10°C increments as shown in the following table:

TMP (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2050 measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (C1 and C2) should be placed as close as possible to the V_{CC} and SB pins, respectively, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor capacitor should be placed as close as possible to the SR pin.
- The sense resistor (R_S) should be as close as possible to the bq2050.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2050. The bq2050 accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge and discharge currents are temperature and rate compensated, whereas self-discharge is only temperature compensated.

The main counter, Nominal Available Capacity (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2050 adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the Programmed Full Count (PFC) shown in Table 2. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. **Last Measured Discharge (LMD) or learned battery capacity:**

   LMD is the last measured discharge capacity of the battery. On initialization (application of V_{CC} or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register (DCR) representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

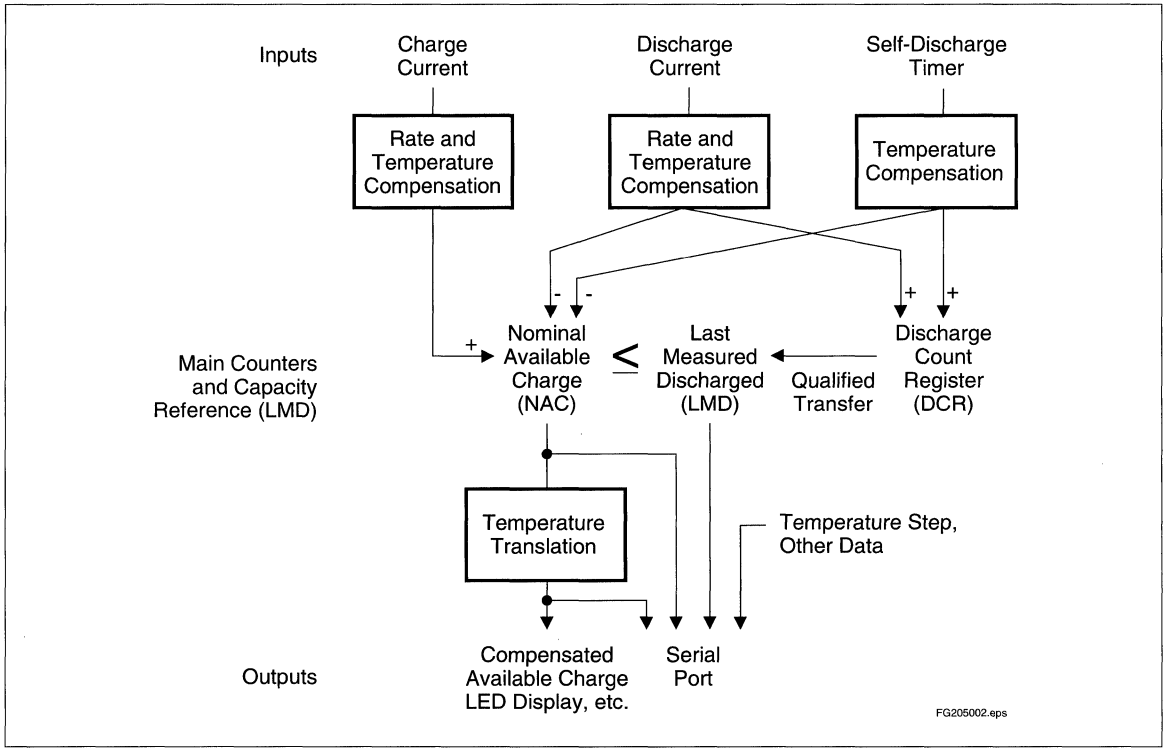


Figure 2. Operational Overview

5/19

2. Programmed Full Count (PFC) or initial battery capacity:

The initial LMD and gas gauge rate values are programmed by using $PROG_1$–$PROG_4$. The bq2050 is configured for a given application by selecting a PFC value from Table 2. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

Battery capacity (mAh) * sense resistor (Ω) =

PFC (mVh)

Selecting a PFC slightly less than the rated capacity provides a conservative capacity reference until the bq2050 "learns" a new capacity reference.

Example: Selecting a PFC Value

Given:

Sense resistor = 0.05Ω
Number of cells = 2
Capacity = 1000mAh, Li-Ion battery, coke-anode
Current range = 50mA to 1A
Relative display mode
Serial port only
Self-discharge = $NAC/_{512}$ per day @ 25°C
Voltage drop over sense resistor = 2.5mV to 50mV
Nominal discharge voltage = 3.6V

Therefore:

1000mAh * 0.05Ω = 50mVh

Table 1. bq2050 Programming

Pin Connection	$PROG_5$ Compensation/ Self-Discharge	$PROG_6$ NAC on Reset	$\overline{DISP}$ Display State
H	Table 4/Disabled	PFC	LEDs disabled
Z	Table 4/ $NAC/_{512}$	0	LEDs on when charging
L	Table 3/ $NAC/_{512}$	0	LEDs on for 4 sec.

Note: $PROG_5$ and $PROG_6$ states are independent.

Table 2. bq2050 Programmed Full Count mVh Selections

$PROG_x$		Programmed Full Count (PFC)	$PROG_4$ = L			$PROG_4$ = Z			Units
1	2		PROG3 = H	PROG3 = Z	PROG3 = L	PROG3 = H	PROG3 = Z	PROG3 = L	
-	-	-	SCALE = 1/80	SCALE = 1/160	SCALE = 1/320	SCALE = 1/640	SCALE = 1/1280	SCALE = 1/2560	mVh/ count
H	H	49152	614	307	154	76.8	38.4	19.2	mVh
H	Z	45056	563	282	141	70.4	35.2	17.6	mVh
H	L	40960	512	256	128	64.0	32.0	16.0	mVh
Z	H	36864	461	230	115	57.6	28.8	14.4	mVh
Z	Z	33792	422	211	106	53.0	26.4	13.2	mVh
Z	L	30720	384	192	96.0	48.0	24.0	12.0	mVh
L	H	27648	346	173	86.4	43.2	21.6	10.8	mVh
L	Z	25600	320	160	80.0	40.0	20.0	10.0	mVh
L	L	22528	282	141	70.4	35.2	17.6	8.8	mVh
VSR equivalent to 2 counts/sec. (nom.)			90	45	22.5	11.25	5.6	2.8	mV

Select:

PFC = 30720 counts or 48mVh
$PROG_1$ = float
$PROG_2$ = low
$PROG_3$ = high
$PROG_4$ = float
$PROG_5$ = float
$PROG_6$ = float

The initial full battery capacity is 48mVh (960mAh) until the bq2050 "learns" a new capacity with a qualified discharge from full to EDV1.

3. Nominal Available Capacity (NAC):

NAC counts up during charge to a maximum value of LMD and down during discharge and self-discharge to 0. NAC is reset to 0 on initialization and on the first valid charge following discharge to EDV1. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = LMD.

4. Discharge Count Register (DCR):

The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC = LMD. The DCR does not roll over but stops counting when it reaches FFFFh.

The DCR value becomes the new LMD value on the first charge after a valid discharge to V_{EDV1} if:

No valid charge initiations (charges greater than 256 NAC counts, where $V_{SRO} > V_{SRQ}$) occurred during the period between NAC = LMD and EDV1 detected.

The self-discharge count is not more than 4096 counts (8% to 18% of PFC, specific percentage threshold determined by PFC).

The temperature is ≥ 0°C when the EDV1 level is reached during discharge.

The valid discharge flag (VDQ) indicates whether the present discharge is valid for LMD update.

5. Scaled Available Energy (SAE):

SAE is useful in determining the available energy within the battery, and may provide a more useful capacity reference in battery chemistries with sloped voltage profiles during discharge. SAE may be converted to a mWh value using the following formula:

$$E(mWh) = (SAEH * 256 + SAEL) * \frac{2.4 * SCALE * (R_{B1} + R_{B2})}{R_S * R_{B2}}$$

where R_{B1}, R_{B2} and R_S are resistor values in ohms. SCALE is the selected scale from Table 2. SAEH and SAEL are digital values read via DQ.

6. Compensated Available Capacity (CAC)

CAC counts similar to NAC, but contains the available capacity compensated for discharge rate and temperature.

Charge Counting

Charge activity is detected based on a positive voltage on the V_{SR} input. If charge activity is detected, the bq2050 increments NAC at a rate proportional to V_{SR} and, if enabled, activates an LED display. Charge actions increment the NAC after compensation for temperature.

The bq2050 determines charge activity sustained at a continuous rate equivalent to $V_{SRO} > V_{SRQ}$. A valid charge equates to sustained charge activity greater than 256 NAC counts. Once a valid charge is detected, charge counting continues until V_{SRO} ($V_{SR} + V_{OS}$) falls below V_{SRQ}. V_{SRQ} is 210µV, and is described in the Digital Magnitude Filter section.

Discharge Counting

Discharge activity is detected based on a negative voltage on the V_{SR} input. All discharge counts where $V_{SRO} < V_{SRD}$ cause the NAC register to decrement and the DCR to increment. V_{SRD} is -200µV, and is described in the Digital Magnitude Filter section.

Self-Discharge Estimation

The bq2050 continuously decrements NAC and increments DCR for self-discharge based on time and temperature. The self-discharge count rate is programmed to be a nominal $1/512$ * NAC per day or disabled. This is the rate for a battery whose temperature is between 20°–30°C. The NAC register cannot be decremented below 0.

Count Compensations

Discharge Compensation

Corrections for the rate of discharge, temperature, and anode type are made by adjusting an internal compensation factor. This factor is based on the measured rate of discharge of the battery. Tables 3A and 3B outline the correction factor typically used for graphite anode Li-Ion batteries, and Tables 4A and 4B outline the factors typically used for coke anode Li-Ion batteries. The compensation factor is applied to CAC and is based on discharge rate and temperature.

Table 3A. Graphite Anode

Approximate Discharge Rate	Discharge Compensation Factor	Efficiency
< 0.5C	1.00	100%
≥ 0.5C	1.05	95%

Table 3B. Graphite Anode

Temperature	Temperature Compensation Factor	Efficiency
≥ 10°C	1.00	100%
0°C to 10°C	1.10	90%
-10°C to 0°C	1.35	74%
≤ -10°C	2.50	40%

Table 4A. Coke Anode

Approximate Discharge Rate	Discharge Compensation Factor	Efficiency
<0.5C	1.00	100%
≥ 0.5C	1.15	86%

Table 4B. Coke Anode

Temperature	Temperature Compensation Factor	Efficiency
≥ 10°C	1.00	100%
0°C to 10°C	1.25	80%
-10°C to 0°C	2.00	50%
≤ -10°C	8.00	12%

Charge Compensation

The bq2050 applies the following temperature compensation to NAC during charge:

Temperature	Temperature Compensation Factor	Efficiency
< 10°C	0.95	95%
≥ 10°C	1.00	100%

This compensation applies to both types of Li-Ion cells.

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of $\frac{1}{512}$ * NAC per day. This is the rate for a battery within the 20°C–30°C temperature range. This rate varies across 8 ranges from < 10°C to > 70°C, changing with each higher temperature (approximately 10°C). See Table 5 below:

Table 5. Self-Discharge Compensation

Temperature Range	Typical Rate PROG5 = Z or L
< 10°C	$NAC/_{2048}$
10–20°C	$NAC/_{1024}$
20–30°C	$NAC/_{512}$
30–40°C	$NAC/_{256}$
40–50°C	$NAC/_{128}$
50–60°C	$NAC/_{64}$
60–70°C	$NAC/_{32}$
> 70°C	$NAC/_{16}$

Self-discharge may be disabled by connecting $PROG_5$ = H.

Digital Magnitude Filter

The bq2050 has a digital filter to eliminate charge and discharge counting below a set threshold. The bq2050 setting is 200µV for V_{SRD} and 210µV for V_{SRQ}.

Table 6. bq2050 Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

Error Summary

Capacity Inaccurate

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see the DCR description on page 7). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

A Capacity Inaccurate counter (CPI) is maintained and incremented each time a valid charge occurs (qualified by NAC; see the CPI register description) and is reset whenever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

Current-Sensing Error

Table 5 illustrates the current-sensing error as a function of V_{SRO}. A digital filter eliminates charge and discharge counts to the NAC register when V_{SRO} is between V_{SRQ} and V_{SRD}.

Communicating With the bq2050

The bq2050 includes a simple single-pin (DQ plus return) serial data interface. A host processor uses the interface to access various bq2050 registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain DQ pin on the bq2050 should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2050. The command directs the bq2050 to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 333 bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2050 may be sampled using the pulse-width capture timers available on some microcontrollers.

If a communication error occurs, e.g. t_{CYCB} > 6ms, the bq2050 should be sent a BREAK to reinitiate the serial interface. A BREAK is detected when the DQ pin is driven to a logic-low state for a time, t_B or greater. The DQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2050 is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2050 taking the DQ pin to a logic-low state for a period, $t_{STRH,B}$. The next section is the actual data transmission, where the data should be valid by a period, t_{DSU}, after the negative edge used to start communication. The data should be held for a period, t_{DV}, to allow the host or bq2050 to sample the data bit.

The final section is used to stop the transmission by returning the DQ pin to a logic-high state by at least a period, t_{SSU}, after the negative edge used to start communication. The final logic-high state should be held until a period, t_{SV}, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2050 is always performed with the least-significant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2050 NAC register.

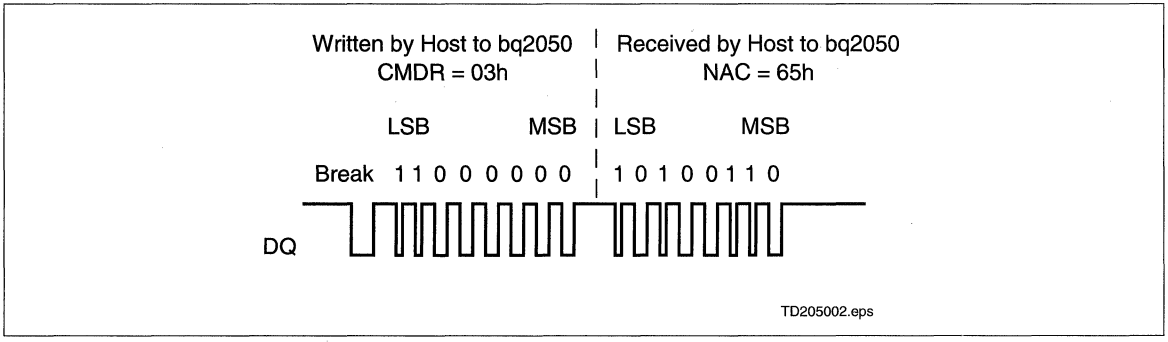


Figure 3. Typical Communication With the bq2050

bq2050 Registers

The bq2050 command and status registers are listed in Table 7 and described below.

Command Register (CMDR)

The write-only CMDR register is accessed when eight valid command bits have been received by the bq2050. The CMDR register contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function.

The W/$\overline{R}$ values are:

CMDR Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is:

0 The bq2050 outputs the requested register contents specified by the address portion of CMDR.

1 The following eight bits should be written to the register specified by the address portion of CMDR.

The lower seven-bit field of CMDR contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

CMDR Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Primary Status Flags Register (FLGS1)

The read-only FLGS1 register (address=01h) contains the primary bq2050 flags.

The ***charge status*** flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when $V_{SRO} > V_{SRQ}$. A V_{SRO} of less than V_{SRQ} or discharge activity clears CHGS.

The CHGS values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
CHGS	-	-	-	-	-	-	-

Where CHGS is:

0 Either discharge activity detected or $V_{SRO} < V_{SRQ}$

1 $V_{SRO} > V_{SRQ}$

The ***battery replaced*** flag (BRP) is asserted whenever the bq2050 is reset either by application of V_{CC} or by a serial port command. BRP is reset when either a valid charge action increments NAC to be equal to LMD, or a valid charge action is detected after the EDV1 flag is asserted. BRP = 1 signifies that the device has been reset.

The BRP values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	BRP	-	-	-	-	-	-

Where BRP is:

0 Battery is charged until NAC = LMD or discharged until the EDV1 flag is asserted

1 bq2050 is reset

Table 7. bq2050 Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	Command register	00h	Write	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
FLGS1	Primary status flags register	01h	Read	CHGS	BRP	n/u	CI	VDQ	n/u	EDV1	EDVF
TMP	Temperature register	02h	Read	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available capacity high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	Nominal available capacity low byte register	17h	Read	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	Read	n/u	DR2	DR1	DR0	n/u	n/u	n/u	OVLD
PPD	Program pin pull-down register	07h	Read	n/u	n/u	PPD6	PPD5	PPD4	PPD3	PPD2	PPD1
PPU	Program pin pull-up register	08h	Read	n/u	n/u	PPU6	PPU5	PPU4	PPU3	PPU2	PPU1
CPI	Capacity inaccurate count register	09h	Read	CPI7	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	CPI0
VSB	Battery voltage register	0Bh	Read	VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0
VTS	End-of-discharge threshold select register	0Ch	R/W	VTS7	VTS6	VTS5	VTS4	VTS3	VTS2	VTS1	VTS0
CACH	Compensated available capacity high byte register	0Dh	Read	CACH7	CACH6	CACH5	CACH4	CACH3	CACH2	CACH1	CACH0
CACL	Compensated available capacity low byte register	0Eh	Read	CACL7	CACL6	CACL5	CACL4	CACL3	CACL2	CACL1	CACL0
SAEH	Scaled available energy high byte register	0Fh	Read	SAEH7	SAEH6	SAEH5	SAEH4	SAEH3	SAEH2	SAEH1	SAEH0
SAEL	Scaled available energy low byte register	10h	Read	SAEL7	SAEL6	SAEL5	SAEL4	SAEL3	SAEL2	SAEL1	SAEL0
RST	Reset register	39h	Write	RST	0	0	0	0	0	0	0

Note: n/u = not used

The ***capacity inaccurate*** flag (CI) is used to warn the user that the battery has been charged a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2050 is reset. The flag is cleared after an LMD update.

The CI values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	CI	-	-	-	-

Where CI is:

0 When LMD is updated with a valid full discharge

1 After the 64th valid charge action with no LMD updates or the bq2050 is reset

The ***valid discharge*** flag (VDQ) is asserted when the bq2050 is discharged from NAC=LMD. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- The self-discharge count register (SDCR) has exceeded the maximum acceptable value (4096 counts) for an LMD update.
- A valid charge action sustained at $V_{SRO} > V_{SRQ}$ for at least 256 NAC counts.
- The EDV1 flag was set at a temperature below 0°C

The VDQ values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

Where VDQ is:

0 SDCR ≥ 4096, subsequent valid charge action detected, or EDV1 is asserted with the temperature less than 0°C

1 On first discharge after NAC = LMD

The ***first end-of-discharge warning*** flag (EDV1) warns the user that the battery is almost empty. The first segment pin, SEG_1, is modulated at a 4Hz rate if the display is enabled once EDV1 is asserted, which should warn the user that loss of battery power is imminent. The EDV1 flag is latched until a valid charge has been detected. The EDV1 threshold is externally controlled via the VTS register (see Voltage Threshold Register on this page).

The EDV1 values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV1	-

Where EDV1 is:

0 Valid charge action detected, $V_{SB} \geq V_{TS}$

1 $V_{SB} < V_{TS}$ providing that the discharge rate is < 2C

The ***final end-of-discharge warning*** flag (EDVF) flag is used to warn that battery power is at a failure condition. All segment drivers are turned off. The EDVF flag is latched until a valid charge has been detected. The EDVF threshold is set 50mV below the EDV1 threshold.

The EDVF values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	EDVF

Where EDVF is:

0 Valid charge action detected, $V_{SB} \geq (V_{TS}$ - 50mV)

1 $V_{SB} < (V_{TS}$ - 50mV) providing the discharge rate is < 2C

Temperature Register (TMP)

The read-only TMP register (address=02h) contains the battery temperature.

TMP Temperature Bits							
7	6	5	4	3	2	1	0
TMP4	TMP3	TMP2	TMP1	-	-	-	-

The bq2050 contains an internal temperature sensor. The temperature is used to set charge and discharge efficiency factors as well as to adjust the self-discharge coefficient. The temperature register contents may be translated as shown in Table 7.

The bq2050 calculates the gas gauge bits, GG3-GG0 as a function of CACH and LMD. The results of the calculation give available capacity in $\frac{1}{16}$ increments from 0 to $\frac{15}{16}$.

Table 7. Temperature Register

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

TMPGG Gas Gauge Bits							
7	6	5	4	3	2	1	0
-	-	-	-	GG3	GG2	GG1	GG0

Nominal Available Charge Registers (NACH/NACL)

The read/write NACH high-byte register (address=03h) and the read-only NACL low-byte register (address=17h) are the main gas gauging register for the bq2050. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC. NACH and NACL are set to 0 during a bq2050 reset.

Writing to the NAC registers affects the available charge counts and, therefore, affects the bq2050 gas gauge operation. Do not write the NAC registers to a value greater than LMD.

Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V_{CC} is greater than 2V. The contents of BATID have no effect on the operation of the bq2050. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2050 uses as a measured full reference. The bq2050 adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2050 updates the capacity of the battery. LMD is set to PFC during a bq2050 reset.

Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2050 flags.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-	-	-	

The ***discharge rate*** flags, DR2–0, are bits 6–4.

DR2	DR1	DR0	Discharge Rate
0	0	0	DRATE < 0.5C
0	0	1	0.5C ≤ DRATE < 2C
0	1	0	DRATE ≥ 2C (OVLD = 1)

They are used to determine the current discharge regime as follows:

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OVLD

The ***overload*** flag (OVLD) is asserted when a discharge rate in excess of 2C is detected. OVLD remains asserted as long as the condition persists and is cleared 0.5 seconds after the rate drops below 2C. The overload condition is used to stop sampling of the battery terminal characteristics for end-of-discharge determination.

Program Pin Pull-Down Register (PPD)

The read-only PPD register (address=07h) contains some of the programming pin information for the bq2050. The segment drivers, SEG_{1-6}, have a corresponding PPD register location, PPD_{1-6}. A given location is set if a pull-down resistor has been detected on its corresponding segment driver. For example, if SEG_1 and SEG_4 have pull-down resistors, the contents of PPD are xx001001.

Program Pin Pull-Up Register (PPU)

The read-only PPU register (address=08h) contains the rest of the programming pin information for the bq2050. The segment drivers, SEG_{1-6}, have a corresponding PPU register location, PPU_{1-6}. A given location is set if a pull-up resistor has been detected on its corresponding segment

driver. For example, if SEG_3 and SEG_6 have pull-up resistors, the contents of PPU are xx100100.

PPD/PPU Bits							
7	6	5	4	3	2	1	0
-	-	PPU_6	PPU_5	PPU_4	PPU_3	PPU_2	PPU_1
-	-	PPD_6	PPD_5	PPD_4	PPD_3	PPD_2	PPD_1

Capacity Inaccurate Count Register (CPI)

The read-only CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2050 adapts to the changing capacity over time. A complete discharge from full (NAC=LMD) to empty (EDV1=1) is required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and the self-discharge counter is less than 4096 counts.

The CPI register is incremented every time a valid charge is detected. When NAC > 0.94 * LMD, however, the CPI register increments on the first valid charge; CPI does not increment again for a valid charge until NAC < 0.94 * LMC. This prevents continuous trickle charging from incrementing CPI if self-discharge decrements NAC. The CPI register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. The CPI register is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

Battery Voltage Register (VSB)

The read-only battery voltage register is used to read the single-cell battery voltage on the SB pin. The VSB register (address = 0Bh) is updated approximately once per second with the present value of the battery voltage. V_{SB} = 2.4V * (VSB/256).

VSB Register Bits							
7	6	5	4	3	2	1	0
VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0

Voltage Threshold Register (VTS)

The end-of-discharge threshold voltages (EDV1 and EDVF) can be set using the VTS register (address = 0Ch). The read/write VTS register sets the EDV1 trip point. EDVF is set 50mV below EDV1. The default value in the VTS register is A2h, representing EDV1 = 1.52V and EDVF = 1.47V. EDV1 = 2.4V * (VTS/256).

VTS Register Bits							
7	6	5	4	3	2	1	0
VTS7	VTS6	VTS5	VTS4	VTS3	VTS2	VTS1	VTS0

Compensated Available Charge Registers (CACH/CACL)

The read-only CACH high-byte register (address = 0Dh) and the read-only CACL low-byte register (address = 0Eh) represent the available charge compensated for discharge rate and temperature. CACH and CACL use piece-wise corrections as outlined in Tables 3A, 3B, 4A, and 4B, and will vary as conditions change. The NAC and LMD registers are not affected by the discharge rate and temperature.

Scaled Available Energy Registers (SAEH/SAEL)

The read-only SAEH high-byte register (address = 0Fh) and the read only SAEL low-byte register (address = 10h) are used to scale battery voltage and CAC to a value which can be translated to watt-hours remaining under the present conditions. SAEL and SAEH may be converted to mWh using the formula on page 7.

Reset Register (RST)

The reset register (address = 39h) enables a software-controlled reset of the device. By writing the RST register contents from 00h to 80h, a bq2050 reset is performed. *Setting any bit other than the most-significant bit of the RST register is* ***not allowed*** *and results in improper operation of the bq2050.*

Resetting the bq2050 sets the following:

- LMD = PFC
- CPI, VDQ, NACH, and NACL = 0
- CI and BRP = 1

Note: Self-discharge is disabled when $PROG_5$ = H.

Display

The bq2050 can directly display capacity information using low-power LEDs. If LEDs are used, the program pins should be resistively tied to V_{CC} or V_{SS} for a program high or program low, respectively.

The bq2050 displays the battery charge state in relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD.

The capacity display is also adjusted for the present battery temperature. The temperature adjustment reflects the available capacity at a given temperature but does

not affect the NAC register. The temperature adjustments are detailed in the CACH and CACL register descriptions.

When $\overline{DISP}$ is tied to V_{CC}, the SEG_{1-5} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active whenever the bq2050 detects a charge in progress $V_{SRO} > V_{SRQ}$. When pulled low, the segment outputs become active for a period of four seconds, ± 0.5 seconds.

The segment outputs are modulated as two banks, with segments 1, 3, and 5 alternating with segments 2 and 4. The segment outputs are modulated at approximately 100Hz with each segment bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV1} (EDV1 = 1), indicating a low-battery condition. V_{SB} below V_{EDVF} (EDVF = 1) disables the display output.

Microregulator

The bq2050 can operate directly from one cell. A micropower source for the bq2050 can be inexpensively built using the FET and an external resistor to accommodate a greater number of cells; see Figure 1.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	7.0	V	
All other pins	Relative to V_{SS}	-0.3	7.0	V	
REF	Relative to V_{SS}	-0.3	8.5	V	Current limited by R1 (see Figure 1)
V_{SR}	Relative to V_{SS}	-0.3	7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2050 application note for details).
T_{OPR}	Operating temperature	0	70	°C	Commercial
		-40	85	°C	Industrial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	1.44	1.47	1.50	V	SB
V_{EDV1}	First empty warning	1.49	1.52	1.55	V	SB
V_{SRO}	SR sense range	-300	-	2000	mV	SR, $V_{SR} + V_{OS}$
V_{SRQ}	Valid charge	210	-	-	µV	$V_{SR} + V_{OS}$ (see note)
V_{SRD}	Valid discharge	-	-	-200	µV	$V_{SR} + V_{OS}$ (see note)
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	SB

Note: V_{OS} is affected by PC board layout. Proper layout guidelines should be followed for optimal performance. See "Layout Considerations."

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{OS}	Offset referred to V_{SR}	-	±50	±150	µV	$\overline{DISP} = V_{CC}$
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	$I_{REF} = 5\mu A$
	Reference at -40°C to +85°C	4.5	-	7.5	V	$I_{REF} = 5\mu A$
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	$V_{REF} = 3V$
I_{CC}	Normal operation	-	90	135	µA	$V_{CC} = 3.0V$, DQ = 0
		-	120	180	µA	$V_{CC} = 4.25V$, DQ = 0
		-	170	250	µA	$V_{CC} = 6.5V$, DQ = 0
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	$0 < V_{SB} < V_{CC}$
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	$V_{DISP} = V_{SS}$
I_{LCOM}	LCOM input leakage	-0.2	-	0.2	µA	$\overline{DISP} = V_{CC}$
I_{RBI}	RBI data retention current	-	-	100	nA	$V_{RBI} > V_{CC} < 3V$
R_{DQ}	Internal pulldown	500	-	-	KΩ	
V_{SR}	Sense resistor input	-0.3	-	2.0	V	$V_{SR} < V_{SS}$ = discharge; $V_{SR} > V_{SS}$ = charge
R_{SR}	SR input impedance	10	-	-	MΩ	$-200mV < V_{SR} < V_{CC}$
V_{IH}	Logic input high	V_{CC} - 0.2	-	-	V	$PROG_1$–$PROG_6$
V_{IL}	Logic input low	-	-	V_{SS} + 0.2	V	$PROG_1$–$PROG_6$
V_{IZ}	Logic input Z	float	-	float	V	$PROG_1$–$PROG_6$
V_{OLSL}	SEG_X output low, low V_{CC}	-	0.1	-	V	$V_{CC} = 3V$, $I_{OLS} \leq 1.75mA$ SEG_1–SEG_5
V_{OLSH}	SEG_X output low, high V_{CC}	-	0.4	-	V	$V_{CC} = 6.5V$, $I_{OLS} \leq 11.0mA$ SEG_1–SEG_5
V_{OHLCL}	LCOM output high, low V_{CC}	V_{CC} - 0.3	-	-	V	$V_{CC} = 3V$, $I_{OHLCOM} = -5.25mA$
V_{OHLCH}	LCOM output high, high V_{CC}	V_{CC} - 0.6	-	-	V	$V_{CC} = 6.5V$, $I_{OHLCOM} = -33.0mA$
I_{IH}	$PROG_{1-6}$ input high current	-	1.2	-	µA	$V_{PROG} = V_{CC}/2$
I_{IL}	$PROG_{1-6}$ input low current	-	1.2	-	µA	$V_{PROG} = V_{CC}/2$
I_{OHLCOM}	LCOM source current	-33	-	-	mA	At $V_{OHLCH} = V_{CC}$ - 0.6V
I_{OLS}	SEG_{1-5} sink current	-	-	11.0	mA	At $V_{OLSH} = 0.4V$
I_{OL}	Open-drain sink current	-	-	5.0	mA	At $V_{OL} = V_{SS} + 0.3V$ DQ
V_{OL}	Open-drain output low	-	-	0.5	V	$I_{OL} \leq 5mA$, DQ
V_{IHDQ}	DQ input high	2.5	-	-	V	DQ
V_{ILDQ}	DQ input low	-	-	0.8	V	DQ
R_{PROG}	Soft pull-up or pull-down resistor value (for programming)	-	-	200	KΩ	$PROG_1$–$PROG_6$
R_{FLOAT}	Float state external impedance	-	5	-	MΩ	$PROG_1$–$PROG_6$

Note: All voltages relative to V_{SS}.

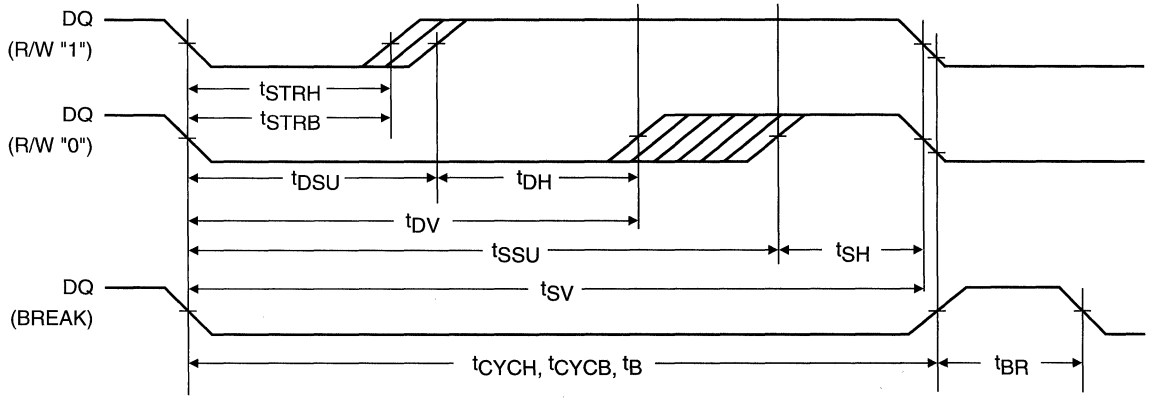
17/19

Serial Communication Timing Specification ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2050	3	-	-	ms	See note
t_{CYCB}	Cycle time, bq2050 to host	3	-	6	ms	
t_{STRH}	Start hold, host to bq2050	5	-	-	ns	
t_{STRB}	Start hold, bq2050 to host	500	-	-	µs	
t_{DSU}	Data setup	-	-	750	µs	
t_{DH}	Data hold	750	-	-	µs	
t_{DV}	Data valid	1.50	-	-	ms	
t_{SSU}	Stop setup	-	-	2.25	ms	
t_{SH}	Stop hold	700	-	-	µs	
t_{SV}	Stop valid	2.95	-	-	ms	
t_B	Break	3	-	-	ms	
t_{BR}	Break recovery	1	-	-	ms	

Notes: The open-drain DQ pin should be pulled to at least V_{CC} by the host system for proper DQ operation. DQ may be left floating if the serial interface is not used.

Serial Communication Timing



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Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	4	Changed reset procedure	Was: Reset by issuing command over serial port Is: Reset by removing V_{CC} and grounding RBI for 15 s.
1	11, 14	Deleted reset register	
2	16	Changed values	V_{EDVF}: Min. was 1.45; Max. was 1.49 Min. now is 1.44; Max. now is 1.50 V_{EDV1}: Min. was 1.50; Min. now is 1.49
2	17	Changed values	V_{CC}: Min. was 2.5; Min. now is 3.0
2	4, 11, 13, 14	Reinserted reset register	
2	9	Maximum offset	V_{OS}: Max. was 150 Max. now is 180

Notes: Change 1 = June 1995 B changes from Dec. 1994.
Change 2 = Sept. 1996 C changes from June 1995 B.

Ordering Information

bq2050 _ _

Temperature Range:
blank = Commercial (0 to 70°C)
N = Industrial (-40 to +85°C)*

Package Option:
SN = 16-pin narrow SOIC

Device:
bq2050 Power Gauge IC

* Contact factory for availability.

Power Gauge™ Evaluation Board

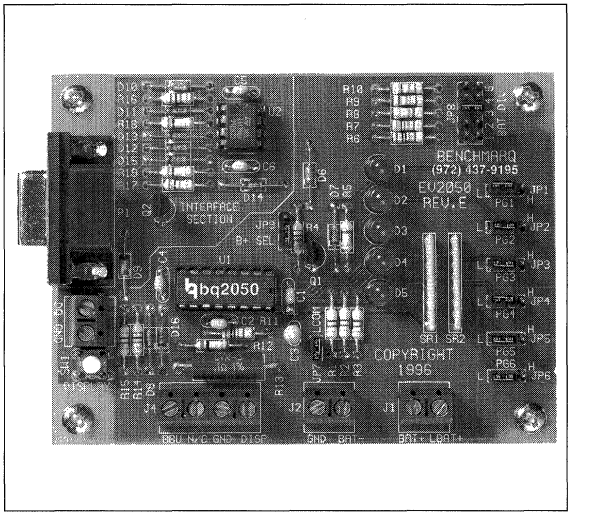
Features

- bq2050 Power Gauge™ IC evaluation and development system
- PC interface hardware for easy access to state-of-charge information via the serial port
- Battery state-of-charge monitoring for 1- to 5-cell (series) applications
- On-board voltage regulator for Power Gauge operation
- State-of-charge information displayed on bank of 5 LEDs
- Nominal capacity jumper-configurable
- Cell anode type (coke or graphite) jumper-configurable

General Description

The EV2050 Evaluation System provides a development and evaluation environment for the bq2050 Power Gauge IC. The EV2050 incorporates a bq2050 sense resistor, and all other hardware necessary to provide a power monitoring function for 1 to 5 series Li-Ion cells.

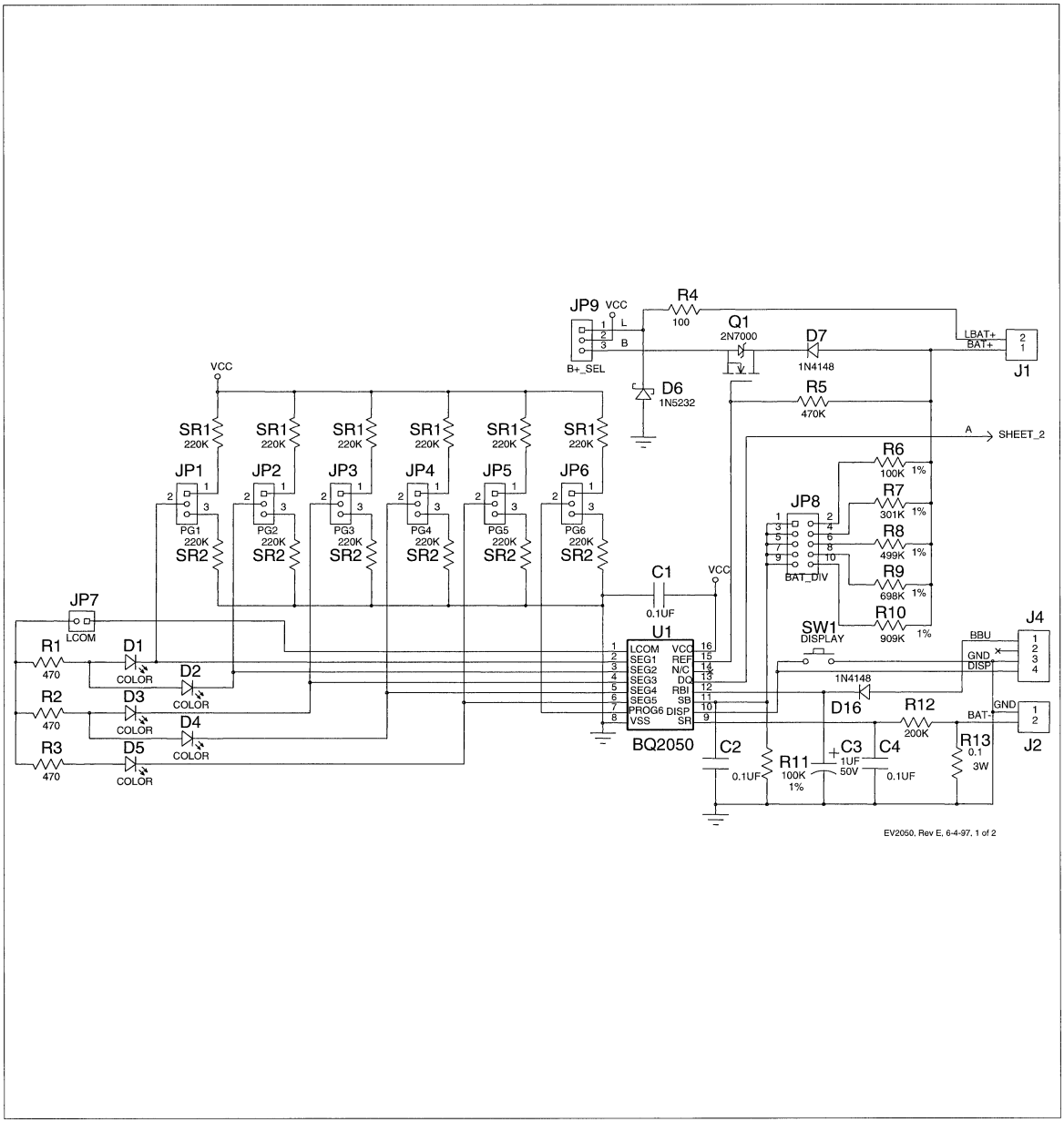
Hardware for an PC interface is included on the EV2050 so that easy access to the state-of-charge information can be achieved via the serial port of the bq2050. Direct connection to the serial port of the bq2050 is also made available for check-out of the final hardware/software implementation.



The menu-driven software provided with the EV2050 displays charge/discharge activity and allows user interface to the bq2050 from any standard DOS PC.

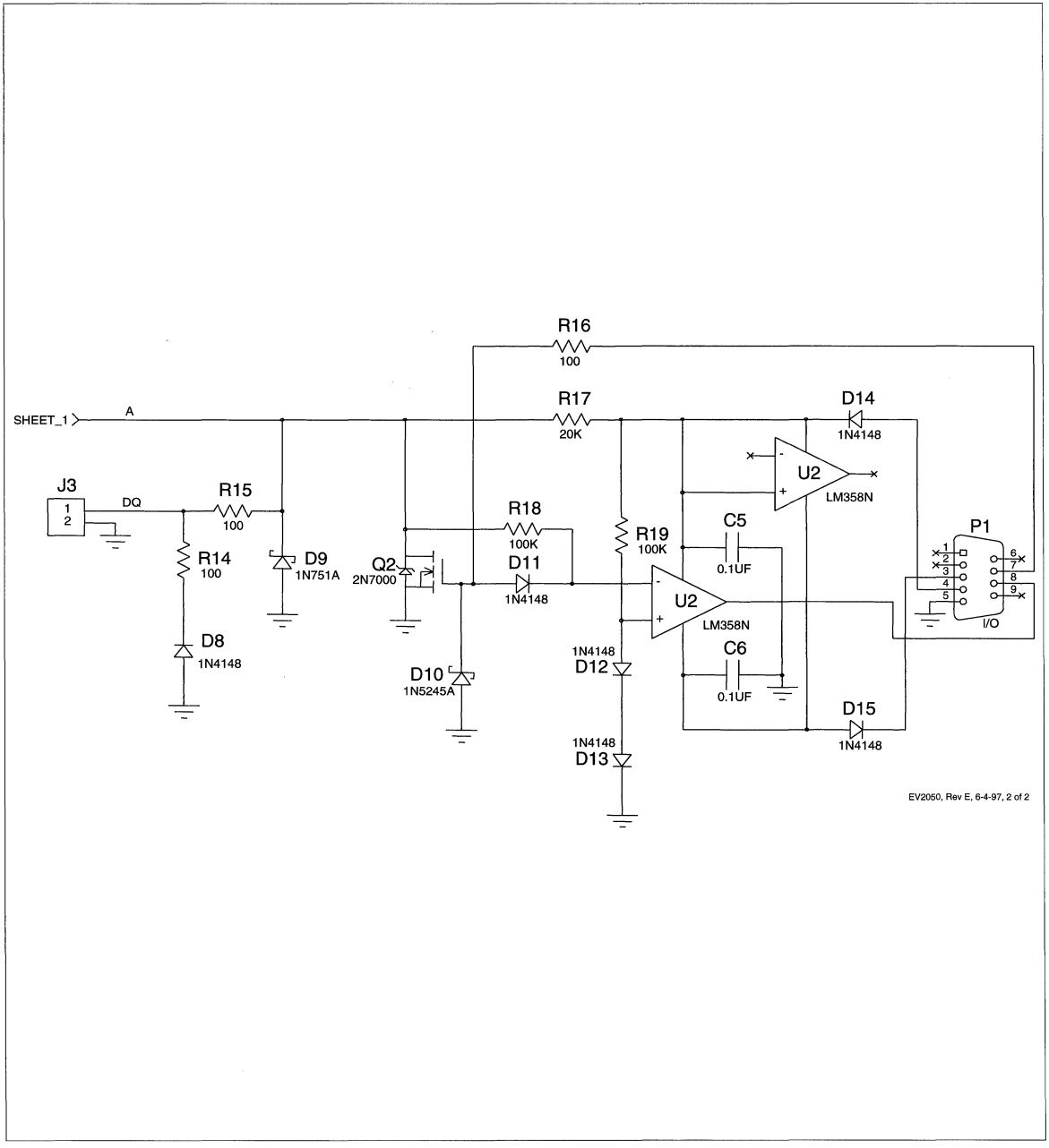
A full data sheet for this product is available from the Unitrode web site, or you may contact the factory for one.

EV2050 Board Schematic



Rev. E Board

EV2050 Board Schematic (Continued)



Rev E Board

bq2050H

Low-Cost Lithium Ion Power Gauge™ IC

Features

- Accurate measurement of available capacity in Lithium Ion batteries
- Provides a low-cost battery management solution for pack integration
  - Complete circuit can fit in as little as ½ square inch of PCB
  - Low operating current (120µA typical)
  - Less than 100nA of data retention current
- High-speed (5kb) single-wire communication interface (HDQ bus) for critical battery parameters
- Monitors and controls charge FET in Li-Ion pack protection circuit
- Direct drive of remaining capacity LEDs
- Measurements automatically compensated for rate and temperature
- 16-pin narrow SOIC

General Description

The bq2050H Lithium Ion Power Gauge™ IC is intended for battery-pack or in-system installation to maintain an accurate record of available battery capacity. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery. Compensations for battery temperature, self discharge, and rate of discharge are applied to the charge counter to provide available capacity information across a wide range of operating conditions. Battery capacity is automatically re-calibrated, or "learned," in the course of a discharge cycle from full to empty.

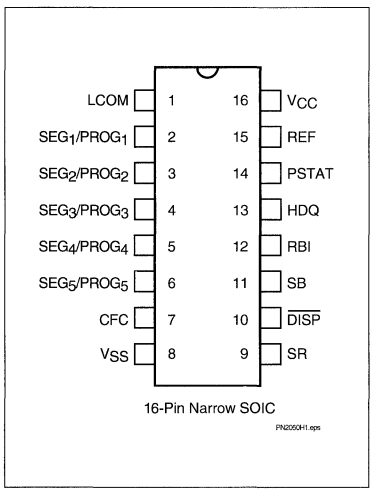
Nominal available capacity may be directly indicated using a five-segment LED display. These segments are used to graphically indicate available capacity. The bq2050H also supports a simple single-line bidirectional serial link to an external processor (common ground). The 5kb HDQ bus interface reduces communications overhead in the external microcontroller.

Internal registers include available capacity, temperature, scaled available energy, battery ID, battery status, and Li-Ion charge FET status. The external processor may also overwrite some of the bq2050H power gauge data registers.

The bq2050H can operate from the batteries in the pack. The REF output and an external transistor allow a simple, inexpensive voltage regulator to supply power to the circuit from the cells.

4

Pin Connections



16-Pin Narrow SOIC

Pin Names

LCOM	LED common output
$SEG_1/PROG_1$	LED segment 1/ program 1 input
$SEG_2/PROG_2$	LED segment 2/ program 2 input
$SEG_3/PROG_3$	LED segment 3/ program 3 input
$SEG_4/PROG_4$	LED segment 4/ program 4 input
$SEG_5/PROG_5$	LED segment 5/ program 5 input
CFC	Charge FET control output
V_{SS}	System ground
SR	Sense resistor input
$\overline{DISP}$	Display control input
SB	Battery sense input
RBI	Register backup input
HDQ	Serial communications input/output
PSTAT	Protector status input
REF	Voltage reference output
V_{CC}	Supply voltage

Pin Descriptions

LCOM **LED common output**

This open-drain output switches V_{CC} to source current for the LEDs. The switch is off during initialization to allow reading of the soft pull-up or pull-down program resistors. LCOM is also high impedance when the display is off.

SEG_1–SEG_5 **LED display segment outputs (dual function with $PROG_1$–$PROG_5$)**

Each output may activate an LED to sink the current sourced from LCOM.

$PROG_1$–$PROG_2$ **Programmed full count selection inputs (dual function with SEG_1–SEG_2)**

These three-level input pins define the programmed full count (PFC) thresholds described in Table 2.

$PROG_3$–$PROG_4$ **Power gauge scale selection inputs (dual function with SEG_3–SEG_4)**

These three-level input pins define the scale factor described in Table 2.

$PROG_5$ **Self-discharge rate selection (dual function with SEG_5)**

This three-level input pin defines the self-discharge and battery compensation factors as shown in Table 1.

CFC **Charge FET control output**

This pin can be used as an additional control to the charge FET of the Li-Ion pack protection circuitry.

V_{SS} **Ground**

SR **Sense resistor input**

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied between the negative terminal of the battery and the sense resistor. $V_{SR} < V_{SS}$ indicates discharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2050H is $V_{SR} + V_{OS}$.

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ tied to V_{CC} allows $PROG_X$ to connect directly to V_{CC} or V_{SS} instead of through a pull-up or pull-down resistor. $\overline{DISP}$ floating allows the LED display to be active during charge. $\overline{DISP}$ low activates the display. See Table 1.

SB **Secondary battery input**

This input monitors the battery cell voltage potential through a high-impedance resistive divider network for end-of-discharge voltage (EDV) thresholds and battery-removed detection.

RBI **Register backup input**

This pin is used to provide backup potential to the bq2050H registers during periods when $V_{CC} \leq 3V$. A storage capacitor or a battery can be connected to RBI.

HDQ **Serial communication input/output**

This is the open-drain bidirectional communications port.

PSTAT **Protector status input**

This input provides overvoltage status from the Li-Ion protector circuit. It should connect to V_{SS} when not used.

REF **Voltage reference output for regulator**

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} **Supply voltage input**

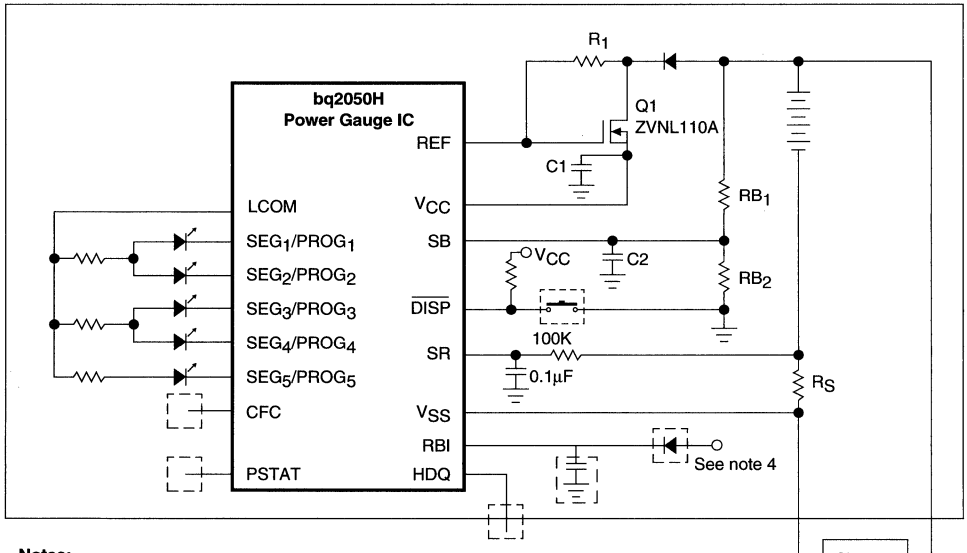
Functional Description

General Operation

The bq2050H determines battery capacity by monitoring the amount of current input to or removed from a rechargeable battery. The bq2050H measures discharge and charge currents, measures battery voltage, estimates self-discharge, monitors the battery for low battery-voltage thresholds, and compensates for temperature and discharge rate. Current measurement is measured by monitoring the voltage across a small-value series sense resistor between the negative battery terminal and ground. Scaled available energy is estimated using the remaining average battery voltage during the discharge cycle and the remaining nominal available capacity. The scaled available energy measurement is corrected for environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2050H using the LED display capability as a charge-state indicator. The bq2050H is configured to display capacity in relative display mode. The relative display mode uses the last measured discharge capacity of the battery as the battery "full" reference. A push-button display feature is available for momentarily enabling the LED display.

The bq2050H monitors the charge and discharge currents as a voltage across a sense resistor. (See R_S in Figure 1.) A filter between the negative battery terminal and the SR pin is required.



Notes:

1. [ ] Indicates optional.
2. Programming resistors and ESD-protection diodes are not shown.
3. RC on SR is required.
4. A series diode is required on RBI if the bottom series cell is used as the backup source. If the cell is used, the backup capacitor is not required, and the anode is connected to the positive terminal of the cell.

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Figure 1. Battery Pack Application Diagram—LED Display

3/22

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2050H monitors the battery potential through the SB pin. The voltage is determined through a resistor-divider network per the following equation:

$$\frac{RB1}{RB2} = 4N - 1$$

where N is the number of cells, RB1 is connected to the positive battery terminal, and RB2 is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV) thresholds. The EDV threshold levels are used to determine when the battery has reached an "empty" state.

The EDV thresholds for the bq2050H are programmable with the default values fixed at:

EDV1 (first) = 0.76V

EDVF (final) = EDV1-0.025V = 0.735V

If V_{SB} is below either of the two EDV thresholds, the associated flag is latched and remains latched, independent of V_{SB}, until the next valid charge. The V_{SB} value is also available over the serial port.

During discharge and charge, the bq2050H monitors V_{SR} for various thresholds used to compensate the charge counter. EDV monitoring is disabled if the discharge rate is greater than 2C (OVLD Flag = 1) and resumes ½ second after the rate falls below 2C.

RBI Input

The RBI input pin is intended to be used with a storage capacitor or external supply to provide backup potential to the internal bq2050H registers when V_{CC} drops below 3.0V. V_{CC} is output on RBI when V_{CC} is above 3.0V. If using an external supply (such as the bottom series cell) as the backup source, an external diode is required for isolation.

Reset

The bq2050H can be reset by removing V_{CC} and grounding the RBI pin for 15 seconds or by commands over the serial port. The serial port reset command sequence requires writing 00h to register PPFC (address = 1Eh) and then writing 00h to register LMD (address = 05h).

Temperature

The bq2050H internally determines the temperature in 10°C steps centered from approximately -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available charge display translation. The temperature range is available over the serial port in 10°C increments as shown in the following table:

TMP (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2050H measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (C1 and C2) should be placed as close as possible to the V_{CC} and SB pins, respectively, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µF is recommended for V_{CC}.
- The sense-resistor capacitor should be placed as close as possible to the SR pin.
- The sense resistor (R_S) should be as close as possible to the bq2050H.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2050H. The bq2050H accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. The accumulated charge and discharge currents are adjusted for temperature and rate to provide the indication of compensated available capacity to the host system or user.

The main counter, Nominal Available Capacity (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2050H adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity equals the Programmed Full Count (PFC) shown in Table 2. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. **Last Measured Discharge (LMD) or learned battery capacity:**

   LMD is the last measured discharge capacity of the battery. On initialization (application of V_{CC} or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

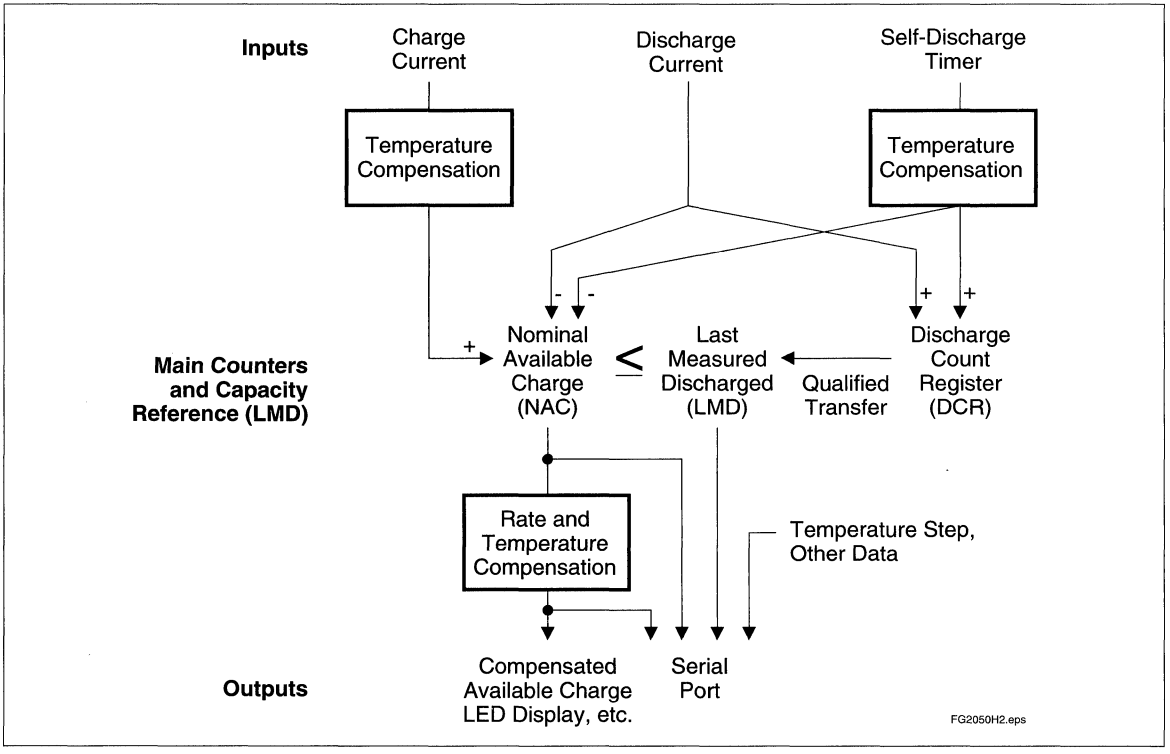


Figure 2. Operational Overview

5/22

2. Programmed Full Count (PFC) or initial battery capacity:

The initial LMD and gas gauge rate values are programmed by using $PROG_1$–$PROG_4$. The bq2050H is configured for a given application by selecting a PFC value from Table 2. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

Battery capacity (mAh) * sense resistor (Ω) =

PFC (mVh)

Selecting a PFC slightly less than the rated capacity provides a conservative capacity reference until the bq2050H "learns" a new capacity reference.

Example: Selecting a PFC Value

Given:

Sense resistor = 0.05Ω
Number of cells = 2
Capacity = 1000mAh, Li-Ion battery, coke-anode
Current range = 50mA to 1A
Relative display mode
Self-discharge = $^{NAC}/_{512}$ per day @ 25°C
Voltage drop over sense resistor = 2.5mV to 50mV
Nominal discharge voltage = 3.6V

Therefore:

1000mAh * 0.05Ω = 50mVh

Table 1. Self-Discharge and Capacity Compensation

Pin Connection	$PROG_5$ Compensation/Self-Discharge (See Tables 3 and 4)	$\overline{DISP}$ Display State
H	Coke anode/disabled	LEDs disabled
Z	Coke anode/ $^{NAC}/_{512}$	LEDs on when charging
L	Graphite anode/ $^{NAC}/_{512}$	LEDs on for 4 s

Table 2. bq2050H Programmed Full Count mVh, V_{SR} Gain Selections

$PROG_x$		Programmed Full Count (PFC)	$PROG_4$ = L			$PROG_4$ = Z or H			Units
1	2		$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	
-	-	-	SCALE = 1/80	SCALE = 1/160	SCALE = 1/320	SCALE = 1/640	SCALE = 1/1280	SCALE = 1/2560	mVh/ count
H	H	49152	614	307	154	76.8	38.4	19.2	mVh
H	Z	45056	563	282	141	70.4	35.2	17.6	mVh
H	L	40960	512	256	128	64.0	32.0	16.0	mVh
Z	H	36864	461	230	115	57.6	28.8	14.4	mVh
Z	Z	33792	422	211	106	53.0	26.4	13.2	mVh
Z	L	30720	384	192	96.0	48.0	24.0	12.0	mVh
L	H	27648	346	173	86.4	43.2	21.6	10.8	mVh
L	Z	25600	320	160	80.0	40.0	20.0	10.0	mVh
L	L	22528	282	141	70.4	35.2	17.6	8.8	mVh
V_{SR} equivalent to 2 counts/s (nom.)			90	45	22.5	11.25	5.6	2.8	mV

Select:

PFC = 30720 counts or 48mVh
$PROG_1$ = float
$PROG_2$ = low
$PROG_3$ = high
$PROG_4$ = float
$PROG_5$ = float

The initial full battery capacity is 48mVh (960mAh) until the bq2050H "learns" a new capacity with a qualified discharge from full to EDV1.

3. **Nominal Available Capacity (NAC):**

NAC counts up during charge to a maximum value of LMD and down during discharge and self-discharge to 0. NAC is reset to 0 on initialization and on the first valid charge following discharge to EDV1. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = LMD.

4. **Discharge Count Register (DCR):**

The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC = LMD. The DCR does not roll over but stops counting when it reaches FFh.

The DCR value becomes the new LMD value on the first charge after a valid discharge to V_{EDV1} if all the following conditions are met:

- No valid charge initiations (charges greater than 2 NAC updates where $V_{SRO} > V_{SRQ}$) occurred during the period between NAC = LMD and EDV1.
- The self-discharge is less than 6% of NAC.
- The temperature is ≥ 0°C when the EDV1 level is reached during discharge.
- VDQ is set

The valid discharge flag (VDQ) indicates whether the present discharge is valid for LMD update. If the DCR update value is less than 0.94 * LMD, LMD will only be modified by 0.94 * LMD. This prevents invalid DCR values from corrupting LMD.

5. **Scaled Available Energy (SAE):**

SAE is useful in determining the available energy within the battery, and may provide a more useful capacity reference in battery chemistries with sloped voltage profiles during discharge. SAE may be converted to an mWh value using the following formula:

$$E(mWh) = (SAEH * 256 + SAEL) * \frac{1.2 * SCALE * (R_{B1} + R_{B2})}{R_S * R_{B2}}$$

where R_{B1}, R_{B2}, and R_S are resistor values in ohms, as shown in Figure 1. SCALE is the selected scale from Table 2.

6. **Compensated Available Capacity (CACT)**

CACT counts similarly to NAC, but contains the available capacity compensated for discharge rate and temperature.

Charge Counting

Charge activity is detected based on a positive voltage on the SR input. If charge activity is detected, the bq2050H increments NAC at a rate proportional to V_{SR} and, if enabled, activates an LED display.

The bq2050H counts charge activity when the voltage at the SR input (V_{SRO}) exceeds the minimum charge threshold (V_{SRQ}). A valid charge is detected when NAC has been updated twice without discharging or reaching the digital magnitude filter time-out. Once a valid charge is detected, charge counting continues until V_{SR}, including offset, falls below V_{SRQ}.

Discharge Counting

Discharge activity is detected based on a negative voltage on the SR input. All discharge counts where V_{SRO} is less than the minimum discharge threshold (V_{SRD}) cause the NAC register to decrement and the DCR to increment.

Self-Discharge Counting

The bq2050H continuously decrements NAC and increments DCR for self-discharge based on time and temperature.

Charge/Discharge Current

The bq2050H current-scale registers, VSRH and VSRL, can be used to determine the battery charge or discharge current. See the Current Scale Register description for details.

Count Compensations

Compensated Available Capacity

Compensated Available Capacity compensation is based on the rate of discharge, temperature, and negative electrode type. Tables 3A and 3B outline the correction factor typically used for graphite-anode Li-Ion batteries, and Tables 4A and 4B outline the factors typically used for coke-anode Li-Ion batteries. The compensation factor is applied to NAC to derive the CACD and CACT values.

7/22

Table 3A. Graphite Anode

Approximate Discharge Rate	Available Capacity Reduction
< 0.5C	0
≥ 0.5C	0.05 * LMD

Table 3B. Graphite Anode

Temperature	Available Capacity Reduction
≥ 10°C	0
0°C to 10°C	0.05 * LMD
-20°C to 0°C	0.15 * LMD
≤ -20°C	0.37 * LMD

Table 4A. Coke Anode

Approximate Discharge Rate	Available Capacity Reduction
<0.5C	0
≥ 0.5C	0.10 * LMD

Table 4B. Coke Anode

Temperature	Available Capacity Reduction
≥ 10°C	0
0°C to 10°C	0.10 * LMD
-20°C to 0°C	0.30 * LMD
≤ -20°C	0.60 * LMD

The CACD value is the available charge compensated for the rate of discharge. At high discharge rates, CACD is reduced. The reduction is maintained until a valid charge is detected. The CACT value is the available charge compensated for the rate of discharge and temperature. The CACT value is used to drive the LED display.

Charge Compensation

The bq2050H also monitors temperature during charge. If the temperature is <0°C, NAC will only increment up to 0.94 * LMD, inhibiting VDQ from being set. This keeps a "learn" cycle from occurring when the battery is charged at very low temperatures. If the temperature rises above 0°C, NAC will be allowed to count up to NAC = LMD.

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of $1/512$ * NAC per day. This is the rate that NAC is reduced for a battery within the 20–30°C temperature range. This rate varies across 8 ranges from <10°C to >70°C, as shown in Table 5.

Table 5. Self-Discharge Compensation

Temperature Range	Typical Rate PROG5 = Z or L
< 10°C	$NAC/2048$
10–20°C	$NAC/1024$
20–30°C	$NAC/512$
30–40°C	$NAC/256$
40–50°C	$NAC/128$
50–60°C	$NAC/64$
60–70°C	$NAC/32$
> 70°C	$NAC/16$

Self-discharge may be disabled by connecting $PROG_5$ = H.

Digital Magnitude Filter

The bq2050H has a digital filter to eliminate charge and discharge counting below a set threshold. The minimum charge (V_{SRQ}) and discharge (V_{SRD}) threshold for the bq2050H is 250µV.

Pack Protection Supervision

The bq2050H can monitor the charge FET in a Li-Ion pack protector circuit as shown in Figure 3. If the battery voltage is too high or the temperature is out of the 0—60°C range, the bq2050H disables the charge FET with the CFC output, which turns off the charge to the pack.

The PSTAT input is used to monitor the protector state. If PSTAT is above 2.5V, bit 5 of FLGS1 is set to 1. If PSTAT is below 0.5V, bit 5 of FLGS1 is cleared to zero. Using this input, the system can monitor the state of the charge con-

Table 6. bq2050H Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

trol FET signal and can quickly determine if the protector circuit is operating properly during charge.

Register 15h, NMCV, is used to set the maximum battery voltage for the battery stack. If V_{SB} > NMCV or the battery temperature is < 0°C or > 60°C, then CFC is driven low.

Error Summary

Capacity Inaccurate

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see the DCR description). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

A Capacity Inaccurate counter (CPI) is maintained and incremented each time a valid charge occurs (qualified by NAC; see the CPI register description). It is reset whenever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

Current-Sensing Error

Table 6 shows the non-linearity and non-repeatability errors associated with the bq2050H current sensing.

Table 7 illustrates the current-sensing error as a function of V_{OS}. A digital filter prevents charge and discharge counts to the NAC register when V_{SRO} is between V_{SRQ} and V_{SRD}.

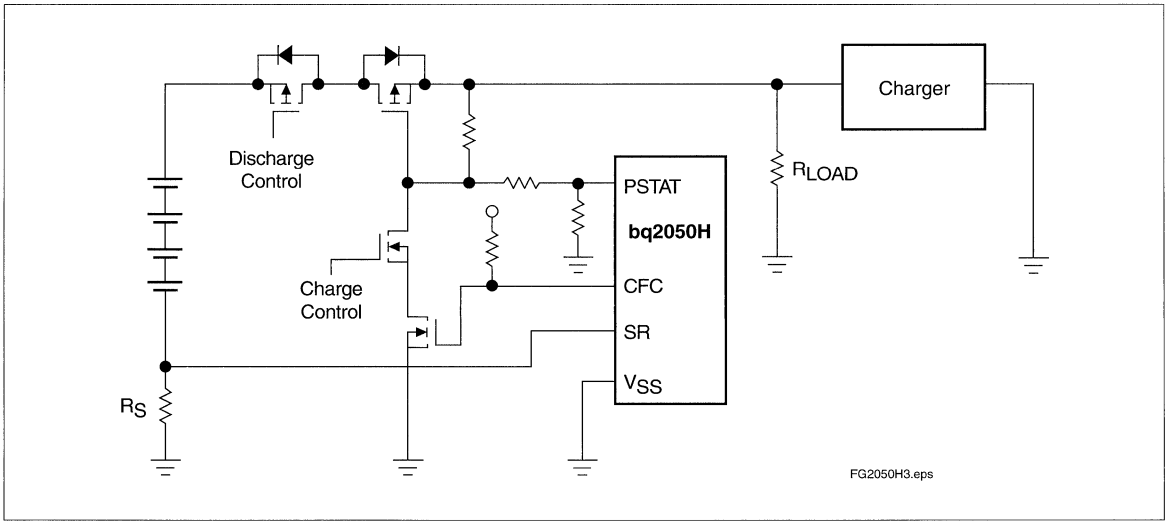


Figure 3. bq2050H Pack Supervision

9/22

Table 7. V_{OS}-Related Current Sense Error (Current = 1A)

V_{OS} (μV)	Sense Resistor			
	20	50	100	mΩ
50	0.25	0.10	0.05	%
100	0.50	0.20	0.10	%
150	0.75	0.30	0.15	%
180	0.90	0.36	0.18	%

Communicating With the bq2050H

The bq2050H includes a simple single-pin (HDQ plus return) serial data interface. A host processor uses the interface to access various bq2050H registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain HDQ pin on the bq2050H should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2050H. The command directs the bq2050H to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte. (See Figure 4.)

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 5K bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2050H may be sampled using the pulse--width capture timers available on some microcontrollers.

If a communication error occurs (e.g., t_{CYCB} > 250μs), the bq2050H should be sent a BREAK to reinitiate the serial interface. A BREAK is detected when the HDQ pin is driven to a logic-low state for a time, t_B or greater. The HDQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2050H is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2050H taking the HDQ pin to a logic-low state for a period, $t_{STRH;B}$. The next section is the actual data transmission, where the data should be valid by a period, $t_{DSU;B}$, after the negative edge used to start communication. The data should be held for a period, $t_{DH;DV}$, to allow the host or bq2050H to sample the data bit.

The final section is used to stop the transmission by returning the HDQ pin to a logic-high state by at least a period, $t_{SSU;B}$, after the negative edge used to start communication. The final logic-high state should be until a period $t_{CYCH;B}$, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2050H is always performed with the least-significant bit being transmitted first. Figure 5 shows an example of a communication sequence to read the bq2050H NACH register.

bq2050H Command Code and Registers

The bq2050H status registers are listed in Table 8 and described below. All registers are Read/Write in the bq2050H. **Caution: When writing to bq2050H registers ensure that proper data is written. A write-verify read is recommended.**

Command Code

The bq2050H latches the command code when eight valid command bits have been received by the bq2050H. The command code contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command code is used to select whether the received command is for a read or a write function.

The W/$\overline{R}$ values are:

Command Code Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is:

0 The bq2050H outputs the requested register contents specified by the address portion of command code.

1 The following eight bits should be written to the register specified by the address portion of command code.

The lower seven-bit field of the command code contains the address portion of the register to be accessed.

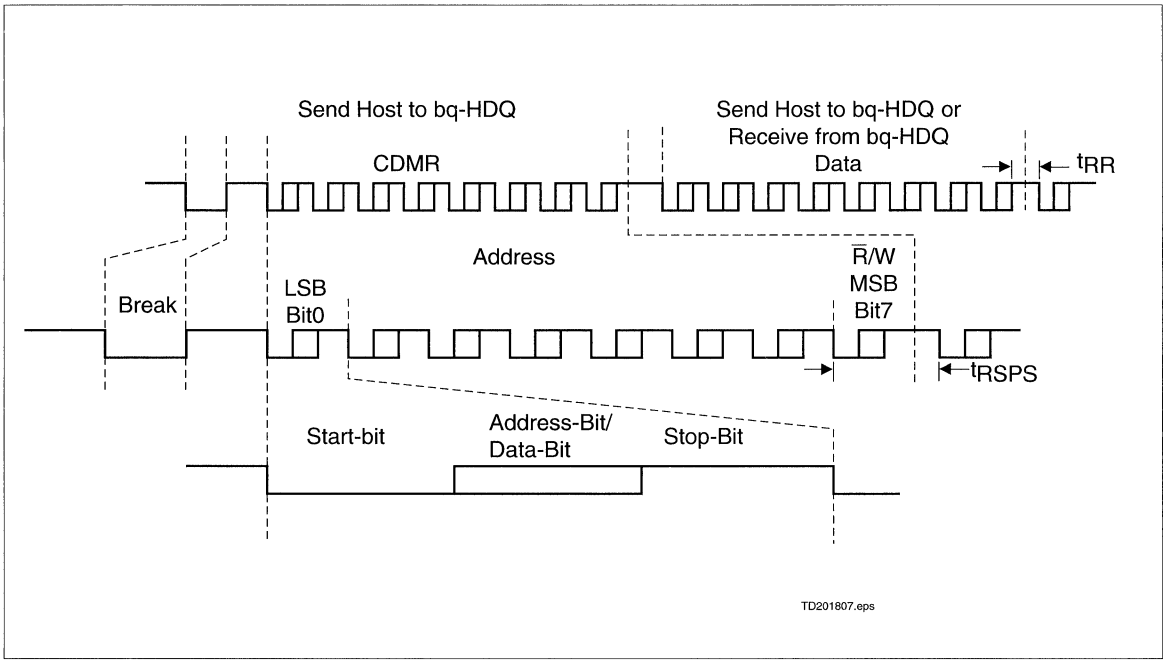


Figure 4. bq2050H Communication Example

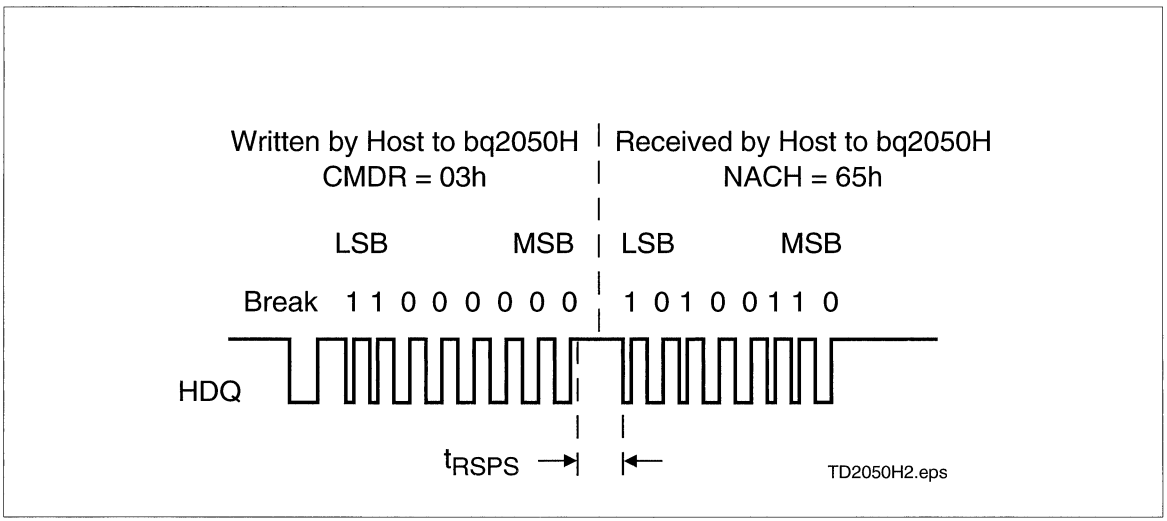


Figure 5. Typical Communication With the bq2050H

Table 8. bq2050H Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
FLGS1	Primary status flags register	01h	R	CHGS	BRP	PSTAT	CI	VDQ	1	EDV1	EDVF
TMP	Temperature register	02h	R	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available capacity high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	Nominal available capacity low byte register	17h	R/W	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	R	RSVD	DR2	DR1	DR0	ENINT	VQ	RSVD	OVLD
PPD	Program pin pull-down register	07h	R	RSVD	RSVD	RSVD	PPD5	PPD4	PPD3	PPD2	PPD1
PPU	Program pin pull-up register	08h	R	RSVD	RSVD	RSVD	PPU5	PPU4	PPU3	PPU2	PPU1
CPI	Capacity inaccurate count register	09h	R/W	CPI7	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	CPI0
VSB	Battery voltage register	0bh	R	VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0
VTS	End-of-discharge threshold select register	0ch	R/W	VTS7	VTS6	VTS5	VTS4	VTS3	VTS2	VTS1	VTS0
CACT	Temperature and Discharge Rate compensated available capacity	0dh	R/W	CACT7	CACT6	CACT5	CACT4	CACT3	CACT2	CACT1	CACT0
CACD	Discharge Rate compensated available capacity	0eh	R/W	CACD7	CACD6	CACD5	CACD4	CACD3	CACD2	CACD1	CACD0
SAEH	Scaled available energy high byte register	0fh	R	SAEH7	SAEH6	SAEH5	SAEH4	SAEH3	SAEH2	SAEH1	SAEH0
SAEL	Scaled available energy low byte register	10h	R	SAEL7	SAEL6	SAEL5	SAEL4	SAEL3	SAEL2	SAEL1	SAEL0
RCAC	Relative CAC	11h	R	-	RCAC6	RCAC5	RCAC4	RCAC3	RCAC2	RCAC1	RCAC0
VSRH	Current scale high	12h	R	VSRH7	VSRH6	VSRH5	VSRH4	VSRH3	VSRH2	VSRH1	VSRH0
VSRL	Current scale low	13h	R	VSRL7	VSRL6	VSRL5	VSRL4	VSRL3	VSRL2	VSRL1	VSRL0
NMCV	Maximum cell voltage	15h	R/W	NMCV7	NMCV6	NMCV5	NMCV4	NMCV3	NMCV2	NMCV1	NMCV0
DCR	Discharge register	18h	R/W	DCR7	DCR6	DCR5	DCR4	DCR3	DCR2	DCR1	DCR0
PPFC	Program pin data	1eh	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
INTSS	V_{OS} Interrupt	38h	R	RSVD	RSVD	RSVD	RSVD	DCHGI	RSVD	RSVD	CHGI
RST	Reset register	39h	R/W	RST	0	0	0	0	0	0	0
HEXFF	Check register	3fh	R/W	1	1	1	1	1	1	1	1

Notes: RSVD = reserved.
All other registers not documented are reserved.

Command Code Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Primary Status Flags Register (FLGS1)

The FLGS1 register (address = 01h) contains the primary bq2050H flags.

The ***charge status*** flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when $V_{SRO} > V_{SRQ}$. A V_{SRO} of less than V_{SRQ} or discharge activity clears CHGS.

The CHGS values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
CHGS	-	-	-	-	-	-	-

Where CHGS is:

0 Either discharge activity detected or $V_{SRO} \leq V_{SRQ}$

1 $V_{SRO} > V_{SRQ}$

The ***battery replaced*** flag (BRP) is asserted whenever the bq2050H is reset either by application of V_{CC} or by a serial port command. BRP is reset when either a valid charge action increments NAC to be equal to LMD, or a valid charge action is detected after the EDV1 flag is asserted. BRP = 1 signifies that the device has been reset.

The BRP values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	BRP	-	-	-	-	-	-

Where BRP is:

0 Battery is charged until NAC = LMD or discharged until the EDV1 flag is asserted

1 bq2050H is reset

The *protector status* flag (PSTAT) provides information on the state of the overvoltage protector within the Li-Ion battery pack. The PSTAT flag is asserted whenever this input is high and is cleared when the input is low.

The PSTAT values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	PSTAT	-	-	-	-	-

Where PSTAT is:

0 PSTAT input is low (PSTAT < 0.5V)

1 PSTAT input is high (PSTAT > 2.5V)

The ***capacity inaccurate*** flag (CI) is used to warn the user that the battery has been charged a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2050H is reset. The flag is cleared after an LMD update.

The CI values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	CI	-	-	-	-

Where CI is:

0 When LMD is updated with a valid full discharge

1 After the 64th valid charge action with no LMD updates or the bq2050H is reset

The ***valid discharge*** flag (VDQ) is asserted when the bq2050H is discharged from NAC=LMD. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- When NAC has been reduced by more than 6% because of self-discharge since VDQ was set.
- A valid charge action sustained at $V_{SRO} > V_{SRQ}$ for at least 2 NAC updates.
- The EDV1 flag was set at a temperature below 0°C

The VDQ values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

Where VDQ is:

0 Self-discharge of 6% of NAC, valid charge action detected, EDV1 asserted with the temperature less than 0°C, or reset

1 On first discharge after NAC = LMD

13/22

The ***first end-of-discharge warning*** flag (EDV1) warns the user that the battery is almost empty. The first segment pin, SEG_1, is modulated at a 4Hz rate if the display is enabled once EDV1 is asserted, which should warn the user that loss of battery power is imminent. The EDV1 flag is latched until a valid charge has been detected. The EDV1 threshold is externally controlled via the VTS register (see Voltage Threshold Register).

The EDV1 values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV1	-

Where EDV1 is:

0 Valid charge action detected, $V_{SB} \geq V_{TS}$

1 $V_{SB} < V_{TS}$ providing that the discharge rate is < 2C

The ***final end-of-discharge warning*** flag (EDVF) flag is used to warn that battery power is at a failure condition. All segment drivers are turned off. The EDVF flag is latched until a valid charge has been detected. The EDVF threshold is set 25mV below the EDV1 threshold.

The EDVF values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	EDVF

Where EDVF is:

0 Valid charge action detected, $V_{SB} \geq (V_{TS} - 25mV)$

1 $V_{SB} < (V_{TS} - 25mV)$ providing the discharge rate is < 2C

Temperature Register (TMP)

The TMP register (address=02h) contains the battery temperature.

The bq2050H contains an internal temperature sensor. The temperature is used to set charge and discharge efficiency factors as well as to adjust the self-discharge coefficient. The temperature register contents may be translated as shown in Table 9.

TMP Temperature Bits							
7	6	5	4	3	2	1	0
TMP3	TMP2	TMP1	TMP0	-	-	-	-

The bq2050H calculates the gas gauge bits, GG3-GG0 as a function of CACT and LMD. The results of the calculation give available capacity in $1/16$ increments from 0 to $15/16$.

TMP Gas Gauge Bits							
7	6	5	4	3	2	1	0
-	-	-	-	GG3	GG2	GG1	GG0

Table 9. Temperature Register

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

Nominal Available Capacity Registers (NACH/NACL)

The NACH high-byte register (address=03h) and the NACL low-byte register (address=17h) are the main gas gauging registers for the bq2050H. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. NACH and NACL are set to 0 during a bq2050H reset.

Writing to the NAC registers affects the available charge counts and, therefore, affects the bq2050H gas gauge operation. Do not write the NAC registers to a value greater than LMD.

Battery Identification Register (BATID)

The BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V_{RBI} is greater than 2V. The contents of BATID have no effect on the operation of the bq2050H. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is the register (address=05h) that the bq2050H uses as a measured full reference. The bq2050H adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2050H updates the capacity of the battery. LMD is set to PFC during a bq2050H reset.

LMD is set to DCR upon the first valid charge after EDV is set if VDQ is set.

If DCR < 0.94 LMD, then LMD is set to 0.94 * LMD.

Secondary Status Flags Register (FLGS2)

The FLGS2 register (address=06h) contains the secondary bq2050H flags.

Bit 7 and bit 1 of FLGS2 are reserved. Do not write to these bits.

The ***discharge rate*** flags, DR2–0, are bits 6–4.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-	-	-	

They are used to determine the current discharge regime as follows:

DR2	DR1	DR0	Discharge Rate
0	0	0	DRATE < 0.5C
0	0	1	0.5C ≤ DRATE < 2C
0	1	0	2C < DRATE

The ***enable interrupt*** flag (ENINT) is a test bit used to determine V_{SR} activity sensed by the bq2050H. The state of this bit will vary and should be ignored by the system.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	ENINT	-	-	

The ***valid charge*** flag (VQ), bit 2 of FLGS2, is used to indicate whether the bq2050H recognizes a valid charge condition. This bit is reset on the first discharge after NAC = LMD.

The VQ values are:

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	VQ	-	

Where VQ is:

0 Valid charge action not detected between a discharge from NAC = LMD and EDV1

1 Valid charge action detected

The ***overload*** flag (OVLD) is asserted when a discharge rate in excess of 2C is detected. OVLD remains asserted as long as the condition persists and is cleared 0.5 seconds after the rate drops below 2C. The overload condition is used to stop sampling of the battery terminal characteristics for end-of-discharge determination.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OVLD

Program Pin Pull-Down Register (PPD)

The PPD register (address=07h) contains some of the programming pin information for the bq2050H. The segment drivers, SEG_{1-5}, have a corresponding PPD register location, PPD_{1-5}. A given location is set if a pull-down resistor has been detected on its corresponding segment driver. For example, if SEG_1 and SEG_4 have pull-down resistors, the contents of PPD are xxx01001.

Program Pin Pull-Up Register (PPU)

The PPU register (address=08h) contains the rest of the programming pin information for the bq2050H. The segment drivers, SEG_{1-5}, have a corresponding PPU register location, PPU_{1-5}. A given location is set if a pull-up resistor has been detected on its corresponding segment driver. For example, if SEG_3 and SEG_5 have pull-up resistors, the contents of PPU are xxx10100.

PPD/PPU Bits							
7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	PPU_5	PPU_4	PPU_3	PPU_2	PPU_1
RSVD	RSVD	RSVD	PPD_5	PPD_4	PPD_3	PPD_2	PPD_1

Capacity Inaccurate Count Register (CPI)

The CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2050H adapts to the changing capacity over time. A complete discharge from full (NAC=LMD) to empty (EDV1=1) is required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and there has been no more than a 6% self-discharge reduction.

The CPI register is incremented every time a valid charge is detected. When NAC > 0.94 * LMD, however, the CPI register increments on the first valid charge; CPI does not increment again for a valid charge until NAC < 0.94 * LMD. This prevents continuous trickle charging from incrementing CPI if self-discharge decrements NAC. The CPI register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. The CPI register is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

Battery Voltage Register (VSB)

The battery voltage register is used to read the single-cell battery voltage on the SB pin. The VSB register (address = 0Bh) is updated approximately once per second with the present value of the battery voltage.
$V_{SB} = 1.2V * (VSB/256)$.

VSB Register Bits							
7	6	5	4	3	2	1	0
VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0

Voltage Threshold Register (VTS)

The end-of-discharge threshold voltages (EDV1 and EDVF) can be set using the VTS register (address = 0Ch). The VTS register sets the EDV1 trip point. EDVF is set 25mV below EDV1. The default value in the VTS register is A2h, representing EDV1 = 0.76V and EDVF = 0.735V. EDV1 = 1.2V * (VTS/256).

VTS Register Bits							
7	6	5	4	3	2	1	0
VTS7	VTS6	VTS5	VTS4	VTS3	VTS2	VTS1	VTS0

Compensated Available Charge Registers (CACT/CACD)

The CACD register (address = 0Eh) contains the NAC value compensated for discharge rate. This is a monotonicly decreasing value during discharge. If the discharge rate is > 0.5C then this value is lower than NAC. CACD is updated only when the discharge rate compensated NAC value is a lower value than CACD during discharge. During charge, CACD is continuously updated with the NAC value.

The CACT register (address = 0Dh) contains the CACD value compensated for temperature. CACT will contain a value lower than CACD when the battery temperature is below 10°C. The CACT value is also used in calculating the LED display pattern.

Scaled Available Energy Registers (SAEH/SAEL)

The SAEH high-byte register (address = 0Fh) and the SAEL low-byte register (address = 10h) are used to scale battery voltage and CACT to a value that can be translated to watt-hours remaining under the present conditions.

Relative CAC Register (RCAC)

The RCAC register (address = 11h) provides the relative battery state-of-charge by dividing CACT by LMD. RCAC varies from 0 to 64h representing relative state-of-charge from 0 to 100%.

Current Scale Register (VSRH/VSRL)

The VSRH register (address = 12h) and the VSRL register (address = 13h) report the average signal across the SR and V_{SS} pins. The bq2050H updates this register pair every 22.5s. V_{SRH} (high-byte) and V_{SRL} (low-byte) form a 16-bit signed integer value representing the average current during this time. The battery pack current can be calculated from:

$$I(mA) = (V_{SRH} * 256 + V_{SRL})/(8 * R_S)$$

where:

R_S = sense resistor value in Ω.
V_{SRH} = high-byte value of battery current
V_{SRL} = low-byte value of battery current

The bq2050H indicates an average discharge current with a "1" in the MSB position of the VSRH register. To calculate discharge current, use the 2's complement if the concatenated register contents in the above equation.

Maximum Cell Voltage Register (NMCV)

The NMCV register (address 15h) is used to set the maximum battery pack voltage for control of the CFC pin. If desired, the system can write a value to NMCV to enable CFC to go low if V_{SB} exceeds this value. This may be useful as a secondary protection of the Li-Ion battery pack. NMCV should be set to the following equation:

$$NMCV = 2s\ complement\ of\left(\frac{256 * MCV * RB2}{1.2 * (RB1 + RB2)}\right)$$

Where:

MCV = maximum desired battery stack voltage.

NMCV = set to 00h on power up or reset and should be programmed to the desired value by the host system.

Discharge Count Register (DCR)

The DCR register (address = 18h) stores the high-byte of the discharge count. DCR is reset to zero at the start of a valid discharge cycle and can count to a maximum of FFh. DCR will not increment if EDV1 = 1 and will not roll over from FFh.

Program Pin Full Count (PPFC)

The PPFC register contains information concerning the program pin configuration. This information is used to determine the data integrity of the bq2050H. **The only approved user application for this register is to write a zero to this register as part of a reset request.**

Voltage Offset (V_{OS}) Interrupt (INTSS)

The INTSS register (address = 38h) is useful during intial characterization of bq2050H designs. When the bq2050H counts a charge pulse, CHGI (bit 0) will be set to 1. When the bq2050H counts a discharge pulse, DCHGI (bit 3) will be set to 1. All other locations in the INTSS register are reserved.

Reset Register (RST)

The reset register (address = 39h) provides an alternate means of initializing the bq2050H via software. Since this register contains device test bits, it is recommended to use the PPFC and LMD registers to reset the bq2050H. **Setting any bits in the reset register is not allowed and will result in improper bq2050H operation.** The recommended reset method for the bq2050H is :

- Write PPFC to zero
- Write LMD to zero

After these operations, a software reset will occur.

Resetting the bq2050H sets the following:

- LMD = PFC
- CPI, VDQ, RCAC, NACH/L, CACH/L, SAEH/L, NMCV = 0
- CI and BRP = 1

Check Register (HEXFF)

The HEXFF register (address = 3F) is useful in determing if the device is a bq2050H or a bq2050. This register is always set to FFh for the bq2050H. The bq2050 returns data other than FFh.

Display

The bq2050H can directly display capacity information using low-power LEDs. If LEDs are used, the program pins should be resistively tied to V_{CC} or V_{SS} for a program high or program low, respectively.

The bq2050H displays the battery charge state in relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD.

The capacity display is also adjusted for the present battery temperature and discharge rate. The temperature adjustment reflects the available capacity at a given temperature but does not affect the NAC register. The temperature adjustments are detailed in the CACT and CACD register descriptions.

When $\overline{DISP}$ is tied to V_{CC}, the SEG_{1-5} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active whenever the bq2050H detects a charge in progress $V_{SRO} > V_{SRQ}$. When pulled low, the segment outputs become active for a period of four seconds, ± 0.5 seconds.

The segment outputs are modulated as two banks, with segments 1, 3, and 5 alternating with segments 2 and 4. The segment outputs are modulated at approximately 100Hz with each segment bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV1} (EDV1 = 1), indicating a low-battery condition. V_{SB} below V_{EDVF} (EDVF = 1) disables the display output.

Microregulator

A micropower source for the bq2050H can be inexpensively built using a FET and an external resistor. (See Figure 1.)

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
REF	Relative to V_{SS}	-0.3	+8.5	V	Current limited by R1 (see Figure 1)
V_{SR}	Relative to V_{SS}	-0.3	Vcc+0.7	V	100kΩ series resistor should be used to protect SR in case of a shorted battery.
T_{OPR}	Operating temperature	0	+70	°C	Commercial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDV1}	First empty warning	0.73	0.76	0.79	V	SB, default
V_{EDVF}	Final empty warning	V_{EDV1} - 0.035	V_{EDV1} - 0.025	V_{EDV1} - 0.015	V	SB, default
V_{SRO}	SR sense range	-300	-	+500	mV	SR, V_{SR} + V_{OS}
V_{SRQ}	Valid charge	250	-	-	µV	V_{SR} + V_{OS} (see note)
V_{SRD}	Valid discharge	-	-	-250	µV	V_{SR} + V_{OS} (see note)
V_{MCV}	Maximum SB voltage	1.10	1.12	1.15	V	SB pin

Note: V_{OS} is affected by PC board layout. Proper layout guidelines should be followed for optimal performance. See "Layout Considerations."

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{OS}	Offset referred to V_{SR}	-	±50	±150	µV	$\overline{DISP}$ = VCC
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V, HDQ = 0
		-	120	180	µA	V_{CC} = 4.25V, HDQ = 0
		-	170	250	µA	V_{CC} = 6.5V, HDQ = 0
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	0 < V_{SB} < V_{CC}
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	V_{DISP} = V_{SS}
I_{LCOM}	LCOM input leakage	-0.2	-	0.2	µA	$\overline{DISP}$ = V_{CC}
I_{RBI}	RBI data retention current	-	-	100	nA	V_{RBI} > V_{CC} < 3V
R_{HDQ}	Internal pulldown	500	-	-	KΩ	
R_{SR}	SR input impedance	10	-	-	MΩ	-200mV < V_{SR} < V_{CC}
V_{IHPFC}	Logic input high	V_{CC} - 0.2	-	-	V	$PROG_{1–5}$
V_{ILPFC}	Logic input low	-	-	V_{SS} + 0.2	V	$PROG_{1–5}$
V_{IZPFC}	Logic input Z	float	-	float	V	$PROG_{1–5}$
V_{OLSL}	SEG output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, I_{OLS} ≤ 1.75mA SEG_1–SEG_5, CFC
V_{OLSH}	SEG output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, I_{OLS} ≤ 11.0mA SEG_1–SEG_5, CFC
V_{OHML}	LCOM output high, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{OHLCOM} = -5.25mA
V_{OHMH}	LCOM output high, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} > 3.5V, I_{OHLCOM} = -33.0mA
I_{OLS}	SEG sink current	11.0	-	-	mA	At V_{OLSH} = 0.4V, V_{CC} = 6.5V
I_{OL}	Open-drain sink current	5.0	-	-	mA	At V_{OL} = V_{SS} + 0.3V, HDQ
V_{OL}	Open-drain output low	-	-	0.3	V	I_{OL} ≤ 5mA, HDQ
V_{IHDQ}	HDQ input high	2.5	-	-	V	HDQ
V_{ILDQ}	HDQ input low	-	-	0.8	V	HDQ
V_{IH}	Logic input high	2.5	-	-	V	PSTAT
V_{IL}	Logic input low	-	-	0.5	V	PSTAT
R_{PROG}	Soft pull-up or pull-down resistor value (for programming)	-	-	200	KΩ	$PROG_{1–5}$
R_{FLOAT}	Float state external impedance	-	5	-	MΩ	$PROG_{1–5}$

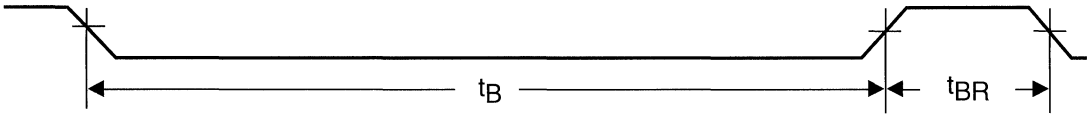
Note: All voltages relative to V_{SS}.

High-Speed Serial Communication Timing Specification ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2050H (write)	190	-	-	µs	See note
t_{CYCB}	Cycle time, bq2050H to host (read)	190	205	250	µs	
t_{STRH}	Start hold, host to bq2050H (write)	5	-	-	ns	
t_{STRB}	Start hold, bq2050H to host (read)	32	-	-	µs	
t_{DSU}	Data setup	-	-	50	µs	
t_{DSUB}	Data setup	-	-	50	µs	
t_{DH}	Data hold	90	-	-	µs	
t_{DV}	Data valid	-	-	80	µs	
t_{SSU}	Stop setup	-	-	145	µs	
t_{SSUB}	Stop setup	-	-	145	µs	
t_{RSPS}	Response time, bq2050H to host	190	-	320	µs	
t_B	Break	190	-	-	µs	
t_{BR}	Break recovery	40	-	-	µs	

Note: The open-drain HDQ pin should be pulled to at least V_{CC} by the host system for proper HDQ operation. HDQ may be left floating if the serial interface is not used.

Break Timing



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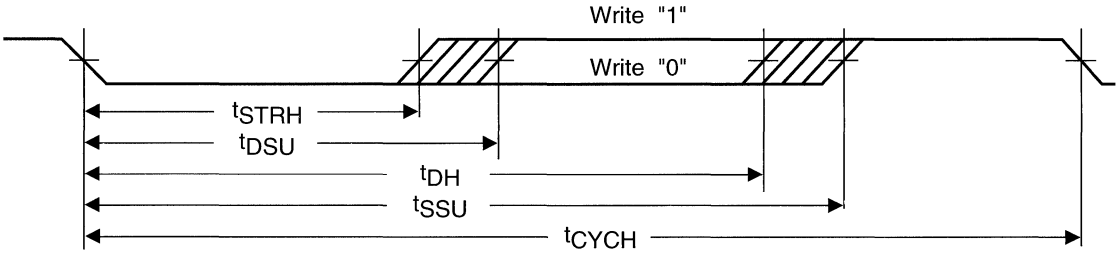
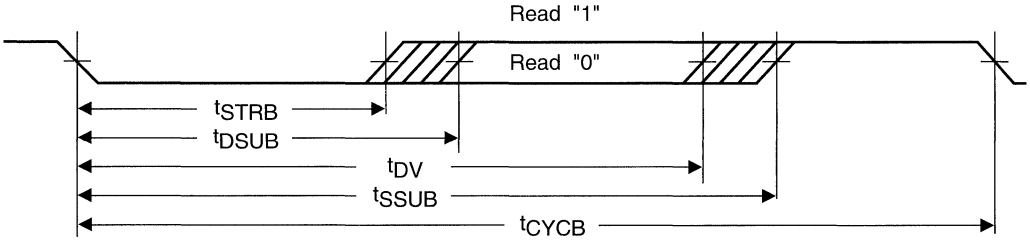
Host to bq2050H



bq2050H to Host

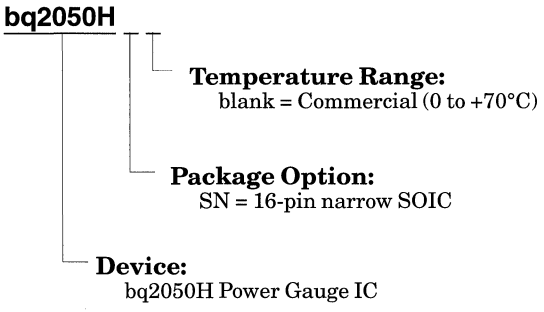


Data Sheet Revision History

ChangeNo.	Page No.	Description of Change
1	All	"Final" changes from "Preliminary" version
2	8	Digital magnitude filter changed from 200µV to 250µV.
2	18	VSRQ changed from 200µV(min) to 250µV(min).
2	18	VSRD changed from -200µV(max) to -250µV(max).
3	3	Updated application diagram
3	12	Changed designation on appropriate locations from "R/W" to "R"
3	16	Clarified current scale register description
3	18	Changed V_{SRO} max. from +2000mV to +500mV
3	19	Changed V_{OL} max. from 0.5V to 0.3V
3	20	Changed t_{SSUB} max. from 95µs to 145µs

Notes: Change 1 = Aug. 1997 B changes from June 1996 "Preliminary."
Change 2 = June 1998 C changes from Aug. 1997 B.
Change 3 = May 1999 D changes from June 1998 C.

Ordering Information



Preliminary **bq2052**

Gas Gauge IC for Lithium Primary Cells

Features

- Accurate measurement of available capacity in Lithium primary batteries such as Lithium Sulphur Dioxide and Lithium Manganese Dioxide
- Provides a low-cost battery monitor solution for pack integration
  - Complete circuit can fit less than 1 square inch of PCB space
  - Low operating current
  - Less than 100nA of data retention current
- Single-wire communication interface (HDQ bus) for critical battery parameters
- Communicates remaining capacity with direct drive of LEDs in 3 selectable modes
- Measurements automatically compensated for discharge rate and temperature
- 16-pin narrow SOIC

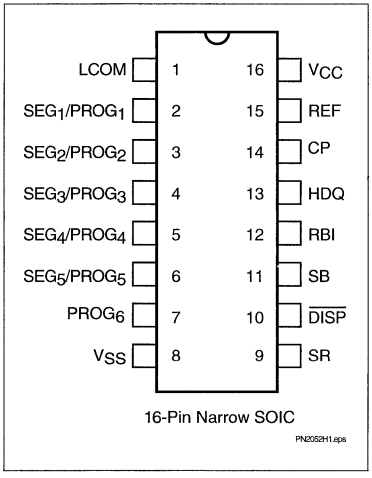
General Description

The bq2052 Lithium Primary Gas Gauge IC is intended for battery-pack or in-system installation to maintain an accurate record of available battery capacity. The IC monitors a voltage drop across a sense resistor connected in series with the cells to determine discharge activity of the battery. The bq2052 applies compensations for battery temperature and discharge rate to the available charge counter to provide available capacity information across a wide range of operating conditions.

Compensated available capacity may be directly indicated using an LED display. The LED display is programmable and can be configured as two, four, or five segments. These segments are used to depict available battery capacity. The bq2052 supports a single-wire serial communications link to an external micro-controller. The link allows the micro-controller to read and write the internal registers of the bq2052. The internal registers include available battery capacity, voltage, temperature, current, and battery status. The controller may also overwrite some of the bq2052 gas gauge data registers.

The bq2052 can operate from the batteries in the pack. The REF output and an external FET provide a simple, inexpensive voltage regulator to supply power to the circuit from the cells.

Pin Connections



16-Pin Narrow SOIC

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Pin Names

LCOM	LED common output
$SEG_1/PROG_1$	LED segment 1/ program 1 input
$SEG_1/PROG_2$	LED segment 2/ program 2 input
$SEG_1/PROG_3$	LED segment 3/ program 3 input
$SEG_1/PROG_4$	LED segment 4/ program 4 input
$SEG_1/PROG_5$	LED segment 5/ program 5 input
CP	Control port
V_{SS}	System ground
SR	Sense resistor input
$\overline{DISP}$	Display control input
SB	Battery sense input
RBI	Register backup input
HDQ	Serial communications input/output
$PROG_6$	Program 6 input
REF	Voltage reference output
V_{CC}	Supply voltage

Pin Descriptions

LCOM **LED common output**

This open-drain output switches V_{CC} to source current for the LEDs. The switch is off during initialization to allow reading of the soft pull-up or pull-down program resistors. LCOM is also high impedance when the display is off.

SEG_1–SEG_5 **LED display segment outputs (dual function with $PROG_1$–$PROG_5$)**

Each output may activate an LED to sink the current sourced from LCOM.

$PROG_1$–$PROG_2$ **Programmed full count selections**

These three-level input pins define the programmed full count.

$PROG_3$ **Power gauge scale selection inputs (dual function with SEG_3–SEG_4)**

This three-level input pin defines the scale factor.

$PROG_4$ **Programmed compensation factors**

This three-level input pin defines the battery discharge compensation factors.

$PROG_5$ **Programmed display mode**

This three-level input pin defines the capacity indication display mode.

$PROG_6$ **Programmed initial capacity state**

This input defines the initial battery capacity indication state. When tied to V_{CC}, the bq2052 sets the available capacity to full on reset. When tied to V_{SS}, the bq2052 sets the available capacity to zero on reset.

V_{SS} **Ground**

SR **Sense resistor input**

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret discharge activity. $V_{SR} > V_{SS}$ indicates discharge. The effective voltage drop, V_{SRO}, as seen by the bq2052 is $V_{SR} + V_{OS}$.

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ tied to V_{CC} (no display LEDs in the circuit) allows $PROG_X$ to connect directly to V_{CC} or V_{SS} instead of through a pull-up or pull-down resistor. $\overline{DISP}$ low activates the display.

SB **Secondary battery input**

This input monitors the battery cell voltage potential through a high-impedance resistive divider network for the end-of-discharge voltage (EDV) thresholds.

RBI **Register backup input**

This pin is used to provide backup potential to the bq2052 registers during periods when $V_{CC} \leq 3V$. A storage capacitor or a battery can be connected to RBI.

HDQ **Serial communication input/output**

This is the open-drain bidirectional communications port.

CP **Control port**

This open drain output may be controlled by serial port commands and its state is reflected in the CPIN bit in FLGS1.

REF **Voltage reference output for regulator**

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} **Supply voltage input**

Functional Description

General Operation

The bq2052 determines battery capacity by monitoring the amount of charge removed from a primary battery. The bq2052 measures discharge currents and battery voltage, monitors the battery for the low battery-voltage thresholds, and compensates available capacity for temperature and discharge rate. The bq2052 measures capacity by monitoring the voltage across a small-value series sense resistor between the negative battery terminal and ground.

Figure 1 shows a typical battery pack application of the bq2052 using the LED display capability as a charge-state indicator. The bq2052 displays capacity with two, four, or five LEDs using the programmed full count (PFC) as the battery's "full" reference. The bq2052 has a push-button input for momentarily enabling the LED display.

Measurements

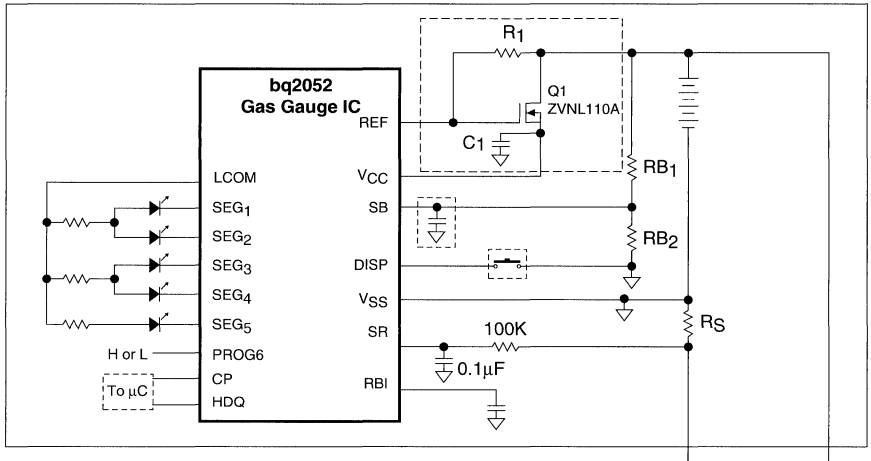
The bq2052 uses a voltage-to-frequency converter (VFC) for discharge measurement and an analog-to-digital converter (ADC) for battery voltage measurement.

Discharge Counting

The VFC measures the discharge flow of the battery by monitoring a small value sense resistor between the SR pin and V_{SS} as shown in Figure 1. The bq2052 detects "discharge" activity when the potential at the SR input, V_{SRO}, is positive. The bq2052 integrates the signal over time using an internal counter. The fundamental rate of the counter is 3.125µVh. The VFC measures signals up to 0.5V in magnitude.

Digital Magnitude Filter

The bq2052 has a digital filter to eliminate discharge counting below a set threshold. The minimum discharge threshold, V_{SRD}, for the bq2052 is 250µV.



Notes:

1. Indicates optional.
2. V_{CC} can connect directly to two lithium primary cells (6.0V nominal and should not exceed 6.5V). Otherwise, R1, C1, and Q1 are needed for regulation of > 2 cells.
3. Programming resistors and ESD-protection diodes are not shown.
4. R-C on SR is required.
5. A series diode is required on RBI if the bottom series cell is used as the backup source. If the cell is used, the backup capacitor is not required, and the anode is connected to the positive terminal of the cell.

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Figure 1. Application Diagram—5-Segment LED Display

3/17

Table 1. bq2052 Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

Voltage Monitoring and Thresholds

In conjunction with monitoring the SR input for discharge currents, the bq2052 monitors the battery potential through the SB pin. The voltage at the SB pin, V_{SB}, is developed through a high impedance resistor network connect across the battery. The bq2052 monitors the voltage at the SB pin and reports the voltage in the VSB register (address = 0bh).

The bq2052 compares the V_{SB} reading to two end-of-discharge voltage (EDV) thresholds. The EDV threshold levels are used to determine when the battery has reached an "empty" state. The EDV thresholds for the bq2052 are programmable with the default values fixed at:

EDV1 (first) = 0.76V
EDVF (final) = EDV1 - 0.10V = 0.66V

If V_{SB} is below either of the two EDV thresholds for 8 consecutive samples over a 4 second period, the bq2052 sets the associated flag in the FLGS1 register (address = 01h). Once set, the EDV flags remain set, independent of V_{SB}.

Temperature

The bq2052 has an internal temperature sensor to measure temperature. The bq2052 determines the temperature and stores it in the TEMP register (address = 02h). The bq2052 uses temperature to adapt remaining capacity for the battery's discharge efficiency.

Gas Gauge Operation

General

The operational overview diagram in Figure 2 illustrates the operation of the bq2052. The bq2052 accumulates a measure of discharge currents and calculates available capacity. The bq2052 compensates available capacity for discharge rate and temperature and provides the information in the Compensated Available Capacity (CAC) registers (address = 0eh–0fh). The main counter, Discharge Count Register (DCR) (address = 2eh), represents the cumulative amount of charge removed from the battery. Battery discharging increments the DCR register.

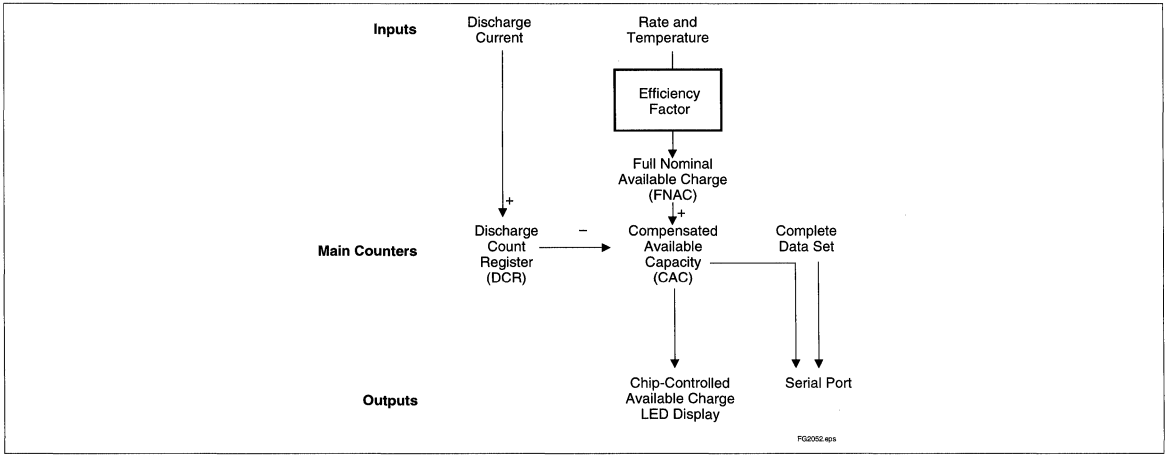


Figure 2. Operational Overview

Table 2. bq2052 Programmed Full Count mVh

$PROG_x$		Programmed Full Count (PFC)	$PROG_3$			Units
1	2		H	Z	L	
-	-	-	SCALE = 1/40	SCALE = 1/80	SCALE = 1/160	mVh/ count
H	H	48128	1203	602	301	mVh
H	Z	46080	1152	576	288	mVh
H	L	43264	1082	541	271	mVh
Z	H	39936	998	499	250	mVh
Z	Z	38400	960	480	240	mVh
Z	L	36096	902	451	226	mVh
L	H	31744	794	397	199	mVh
L	Z	28928	723	362	181	mVh
L	L	26112	653	327	164	mVh

Main Gas-Gauge Registers

Programmed Full Count

The PFC register stores the user-specified battery full capacity. The 8-bit PFC registers stores the full capacity in mVh scaled as shown in Table 2.

Full Nominal Available Capacity

The FNAC register stores the full capacity reference of the battery. It can be programmed to initialize to PFC or zero. The 8-bit FNAC register stores data scaled to the same units as PFC. The bq2052 does not update FNAC during the course of operation; therefore, if it is programmed to 0 on initialization, it must be written to full using the serial port.

Discharge Count Register

The DCR is the main gas gauging register and contains the cumulative amount of discharge counted by the bq2052. The 16-bit register stores data scaled to the same units as PFC.

Compensated Available Capacity

The CAC registers contain the current available capacity of the battery. The data stored in CAC represents the amount of remaining capacity of the battery compensated for rate and temperature use conditions. Tables 3, 4, and, 5 outline the options for typical efficiency compensation factors for lithium primary batteries. The bq2052 applies the efficiency factors to FNAC to derive CAC.

The bq2052 applies the compensation according to the formula:

$$CAC = [F_{CE} * FNAC] - DCR$$

Where F_{CE} is the calculated efficiency compensation factor, FNAC = Full Nominal Available Capacity and DCR = Discharge Count Register.

The bq2052 calculates an F_{CE} based on the battery discharge rate and temperature. The discharge rate portion of the F_{CE} compensation is a "peak hold" function; therefore, the bq2052 latches the highest discharge rate it has measured and uses the highest rate to calculate F_{CE} throughout the complete discharge cycle. The highest discharge rate measured by the bq2052 is stored in MRATE (address = 12h).

The bq2052 does not latch the temperature portion of an F_{CE} calculation. Therefore, CAC may increase or decrease during the course of a complete discharge cycle if a temperature shift causes a change in the calculated F_{CE} value.

Programming the bq2052

The bq2052 is programmed with the $PROG_{1-6}$ pins. During power-up or initialization, the bq2052 reads the state of these six three-level inputs and latches in the programmable configuration settings.

Programmable Configuration Settings

Design Capacity

The battery's rated design capacity or Programmed Full Count (PFC) is programmed with the $PROG_1$–$PROG_3$ pins as shown in Table 2, and represents the battery's full reference.

The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

Battery capacity (mAh) * sense resistor (Ω) = PFC (mVh)

Selecting a PFC slightly less than the rated capacity provides a conservative capacity reference. The bq2052 stores the selected PFC in the PFC register (address = 10h).

Discharge Rate and Temperature Compensation

The discharge rate and temperature compensations are selected using the $PROG_4$ pin. The level of $PROG_4$ on power-up or initialization determines which compensation table the bq2052 uses for the discharge cycle. The following tables illustrate the calculated efficiency compensation factors at selected discharge rates and temperatures.

Table 3. Discharge Efficiency Factor Table PROG4 = Z

	Discharge Rage					
TEMP	0	C/80	C/25	C/10	C/5	C/3
-20	97	99	96	92	85	81
-10	98	98	97	94	89	85
0	98	98	97	94	90	87
21	99	99	98	96	92	89
55	99	99	98	96	93	90
70	99	99	98	96	93	90

Table 4. Discharge Efficiency Factor Table PROG4 = L

	Discharge Rage					
TEMP	0	C/80	C/25	C/10	C/5	C/3
-20	87	85	80	70	53	50
-10	93	91	88	80	68	51
0	96	94	91	85	74	60
21	99	97	95	89	81	68
55	100	99	97	92	85	74
70	101	100	98	93	86	76

Table 5. Discharge Efficiency Factor Table PROG4 = H

	Discharge Rage					
TEMP	0	C/80	C/25	C/10	C/5	C/3
-20	92	93	92	88	83	75
-10	98	98	97	93	89	81
0	100	100	99	96	91	84
21	104	104	102	99	95	88
55	106	106	105	100	97	90
70	107	107	105	101	98	91

Display Mode

The display mode is selected using the $PROG_5$ pin. The three options include a two, four, or five segment display mode as described in Tables 7, 8, and 9.

Initial Capacity Setting

The PFC value is copied to the FNAC register if $PROG_6$ is programmed high, otherwise FNAC defaults to 0. FNAC may be written to the desired full capacity to initialize the pack manually.

Programming Example

Given:

Sense resistor = 0.05mΩ
Number of cells = 5 in series
Capacity = 7000mAh,
Chemistry = $LiSO_2$
Discharge current range = 250mA to 2A
Voltage drop over sense resistor = 12.5mV to 100mV
Display mode = 5 segment bar graph display

Therefore:

7000mAh * 0.05 = 350mVh

Select:

PFC = 26112 counts or 327mVh
$PROG_1$ = low
$PROG_2$ = low
$PROG_3$ = float
$PROG_4$ = float, high, or low depending on desired compensation factors
$PROG_5$ = float selects five segment display
$PROG_6$ = high sets FNAC to PFC

With these selections, the full battery capacity is 327mVh (6540mAh).

Table 6. bq2052 Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7	6	5	4	3	2	1	0
CMDWD	Command word	00h	W	CMD7	CMD6	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0
FLGS1	Primary status flags	01h	R	INIT	RSVD	RSVD	CPIN	RSVD	RSVD	EDV1	EDVF
TEMP	Temperature (°C)	02h	R	TEMP7	TEMP6	TEMP5	TEMP4	TEMP3	TEMP2	TEMP1	TEMP0
NAC	Nominal available capacity	03h	R/W	NAC7	NAC6	NAC5	NAC4	NAC3	NAC2	NAC1	NAC0
BATID	Battery identification	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
VSRL	Current scale (Low)	05h	R	VSRL7	VSRL6	VSRL5	VSRL4	VSRL3	VSRL2	VSRL1	VSRL0
VSRH	Current scale (High)	06h	R	VSRH7	VSRH6	VSRH5	VSRH4	VSRH3	VSRH2	VSRH1	VSRH0
PPD	Program pin pull-down	07h	R	RSVD	RSVD	PPD6	PPD5	PPD4	PPD3	PPD2	PPD1
PPU	Program pin pull-up	08h	R	RSVD	RSVD	PPU6	PPU5	PPU4	PPU3	PPU2	PPU1
VSB	Battery voltage register	0bh	R	VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0
VTS	End-of-discharge threshold select register	0ch	R/W	VTS7	VTS6	VTS5	VTS4	VTS3	VTS2	VTS1	VTS0
RCAC	Relative compensated capacity	0dh	R	RSVD	RCAC6	RCAC5	RCAC4	RCAC3	RCAC2	RCAC1	RCAC0
CACL	Compensated available capacity low byte	0eh	R	CACL7	CACL6	CACL5	CACL4	CACL3	CACL2	CACL1	CACL0
CACH	Compensated available capacity high byte	0fh	R	CACH7	CACH6	CACH5	CACH4	CACH3	CACH2	CACH1	CACH0
PFC	Program pin full count	10h	R	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0
FNAC	Full nominal available capacity	11h	R/W	FNAC7	FNAC6	FNAC5	FNAC4	FNAC3	FNAC2	FNAC1	FNAC0
MAX RATE	Maximum discharge rate	12h	R	MAX7	MAX6	MAX5	MAX4	MAX3	MAX2	MAX1	MAX0
RATE	Discharge rate	13h	R	RATE7	RATE6	RATE5	RATE4	RATE3	RATE2	RATE1	RATE0
DCRL	Discharge count register (low byte)	2eh	R/W	DCRL7	DCRL6	DCRL5	DCRL4	DCRL3	DCRL2	DCRL1	DCRL0
DCRH	Discharge count register (high byte)	2fh	R/W	DCRH7	DCRH6	DCRH5	DCRH4	DCRH3	DCRH2	DCRH1	DCRH0

Notes: RSVD = reserved.
All other registers not documented are reserved.

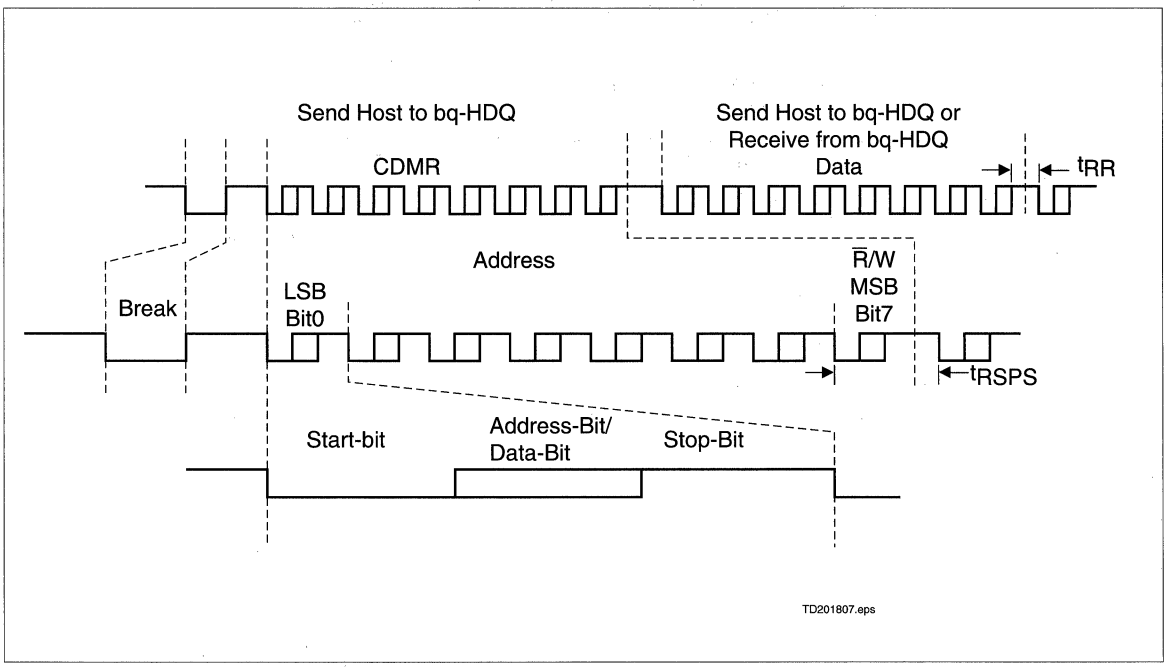


Figure 4. bq2052 Communication Example

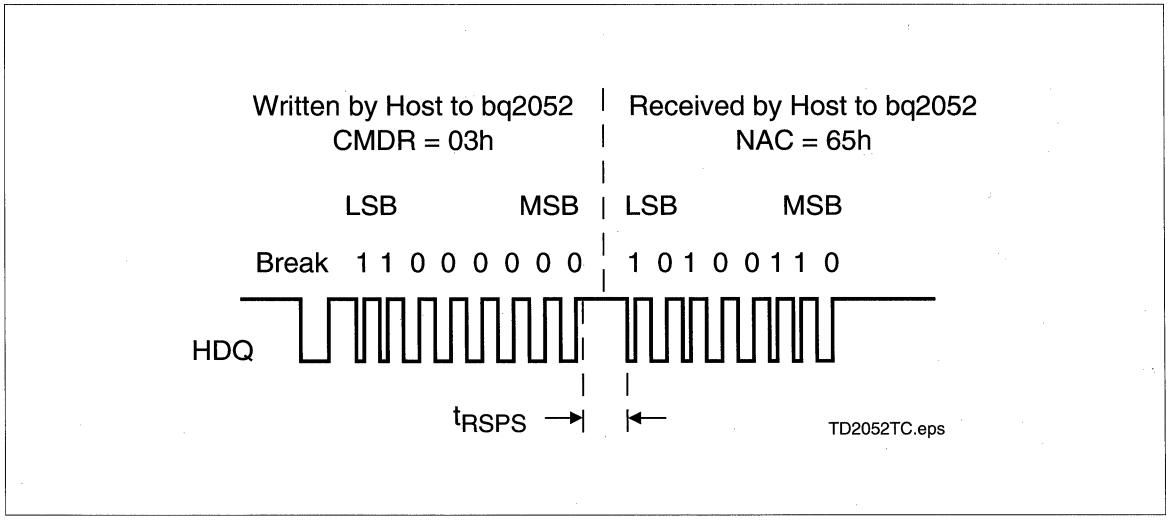


Figure 5. Typical Communication with the bq2052

Communicating With the bq2052

The bq2052 includes a simple single-pin (HDQ plus return) serial data interface. A host processor uses the interface to access various bq2052 registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain HDQ pin on the bq2052 should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2052. The command directs the bq2052 to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 5K bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2052 may be sampled using the pulse-width capture timers available on some microcontrollers.

If a communication error occurs, e.g., $t_{CYCB} > 250\mu s$, the bq2052 should be sent a BREAK to reinitiate the serial interface. A BREAK is detected when the HDQ pin is driven to a logic-low state for a time, t_B or greater. The HDQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2052 is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2052 taking the HDQ pin to a logic-low state for a period, $t_{STRH;B}$. The next section is the actual data transmission, where the data should be valid by a period, $t_{DSU;B}$, after the negative edge used to start communication. The data should be held for a period, $t_{DH;DV}$, to allow the host or bq2052 to sample the data bit.

The final section is used to stop the transmission by returning the HDQ pin to a logic-high state by at least a period, $t_{SSU;B}$, after the negative edge used to start communication. The final logic-high state should be until a period $t_{CYCH;B}$, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2052 is always performed with the least-significant bit being transmitted first. Figure 5 shows an example of a communication sequence to read the bq2052 NAC register.

bq2052 Command Code and Registers

The bq2052 status registers are listed in Table 6 and described below.

Command Code

The bq2052 latches the command code when eight valid command bits have been received by the bq2052. The command code contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command code is used to select whether the received command is for a read or a write function.

The W/$\overline{R}$ values are:

Command Code Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is:

0 The bq2052 outputs the requested register contents specified by the address portion of command code.

1 The following eight bits should be written to the register specified by the address portion of command code.

The lower seven-bit field of the command code contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

Command Code Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Command Word (CMDWD)

The CMDWD register (address = 00h) is used by the external host to control the CP pin and to reset the bq2052.

CMDWD	Action
0x55	CP high impedence, CPIN bit in FLGS1 set
0x66	CP driven low, CPIN bit in FLGS1 cleared
0x78	bq2052 reset

Primary Status Flags Register (FLGS1)

The FLGS1 register (address = 01h) contains the primary bq2052 flags.

The ***initialized*** flag (INIT) is asserted to a 1 or 0 whenever the bq2052 is initialized either by the application of Vcc or by a serial port command. INIT = 1 signifies that the device has been reset with FNAC set to PFC. INIT = 0 signifies that the battery has been reset with FNAC = 0.

The INIT location is:

FLGS1 Bits							
7	6	5	4	3	2	1	0
INIT	-	-	-	-	-	-	-

where INIT is:

0 The bq2052 initialized with FNAC = 0.

1 The bq2052 initialized with FNAC = PFC.

The CPIN but reflects the state of the CP output. If set, the CP output is high impedance. If cleared, the CP output is asserted low. The CP output is an open drain output and requires an external pull-up register.

The CPIN location is

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	CPIN	-	-	-	-

Where CPIN is:

0 CP is low

1 CP is high impedance

The bq2052 sets the ***first end-of-discharge warning*** flag (EDV1) when the battery voltage VSB is less than the EDV1 threshold VTS. The flag warns the user that the battery is almost empty. The bq2052 modulates the first segment pin, SEG1, at a 4Hz rate if the 4 or 5 segment display mode is enabled and EDV1 is asserted.

The EDV1 threshold has a default value of 0.76V but can be adjusted by writing the VTS register .

The EDV1 location is

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV1	-

Where EDV1 is:

0 $V_{SB} \geq V_{TS}$

1 $V_{SB} < V_{TS}$

The bq2052 sets the ***final end-of-discharge warning*** flag (EDVF) when VSB is less than the EDVF threshold. The EDVF threshold is set 100mV below the EDV1 threshold. The EDVF flag is used to warn the system or user that battery power is at a failure condition. The bq2052 turns all segment drivers off upon EDVF detection.

The EDVF location is:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	EDVF

Where EDVF is:

0 $V_{SB} \geq (V_{TS} - 100mV)$

1 $V_{SB} < (V_{TS} - 100mV)$

Temperature Register (TEMP)

The 8-bit TEMP register (address=02h) contains the battery temperature in degrees C. The bq2052 contains an internal temperature sensor. The temperature is used to set discharge efficiency factors. The temperature register contents are store in 2's complement form and represent the temperature ± 5°C.

Nominal Available Capacity Register (NAC)

The NAC register contains the uncompensated remaining capacity of the battery. The bq2052 determines NAC as

$$NAC = FNAC - DCR$$

Battery Identification Register (BATID)

The 8-bit BATID register (address=04h) is a general purpose memory register that can be used to uniquely identify a battery pack. The bq2052 maintains the BATID contents as long as VRBI is greater than 2V. The contents of this register have no effect on the operation of the bq2052.

Current Scale Registers (VSRL/VSRH)

The VSRH high-byte register and the VSRL low-byte register are used to calculate the average signal across the SR and VSS pins. This register pair is updated every 5.625 seconds. VSRH and VSRL form a 16-bit value representing the average current over this time. The battery pack current can be calculated by:

$$|I(mA)| = \frac{(VSRH * 256 + VSRL)}{(Rs)}$$

where

R_S = sense resistor value in Ω.

VSRH = high-byte value of current scale

VSRL = low-byte value of current scale

Program Pin Pull-Down Register (PPD)

The PPD register (address = 07h) contains the pull-down programming pin information for the bq2052. The program pins, $PROG_{1-6}$, have a corresponding PPD register location, PPD_{1-6}. A given location is set if the bq2052 detects a pull-down resistor on its corresponding segment driver. For example, if $PROG_1$ and $PROG_4$ have pull-down resistors, the contents of PPD are xx001001.

Program Pin Pull-Up Register (PPU)

The PPU register (address = 08h) contains the pull-up programming pin information for the bq2052. The segment drivers, $PROG_{1-6}$, have a corresponding PPU register location, PPU_{1-6}. A given location is set if a pull-up resistor has been detected on its corresponding segment driver. For example, if $PROG_3$ and $PROG_5$ have pull-up resistors, the contents of PPU are xx010100.

Battery Voltage (VSB)

The battery voltage register (address = 0bh) stored the voltage detected on the SB pin. The bq2052 updates the VSB register approximately once per second with the present value of the battery voltage.

$$V_{SB} = 1.2V * \left(\frac{VSB}{256}\right)$$

Voltage Threshold Register (VTS)

The end-of-discharge threshold voltages (EDV1 and EDVF) can be set using the VTS register. The VTS register sets the EDV1 trip point. EDVF is set 100mV below EDV1. The default value in the VTS register is A2h, representing EDV1 = 0.76V and EDVF = 0.66V.

$$EDV1 = 1.2V * \left(\frac{VTS}{256}\right).$$

Relative CAC Register (RCAC)

The RCAC register (address = 0dh) provides the relative battery state-of-charge by dividing CAC by FNAC. RCAC varies from 0 to 7dh representing relative state-of-charge from 0 to 125%.

Compensated Available Capacity (CAC)

The CAC registers (address = 0eh–0fh) contain the available capacity compensated for discharge rate and temperature. The CAC value is also used in calculating the LED display pattern relative to PFC.

Program Full Count (PFC)

The PFC register (address = 10h) contains the user selected programmed full count (PFC) setting.

Full Nominal Available Capacity (FNAC)

The FNAC (address = 11h) contains the full capacity reference of the battery.

Maximum Discharge Rate (MAXRATE)

The MAXRATE register (address = 12h) stores the highest discharge rate detected by the bq2052. The bq2052 uses the MAXRATE value to calculate the efficiency compensation factors.

Discharge Rate (RATE)

The RATE register (address = 13h) provides the current discharge rate of the battery.

Discharge Count Registers (DCRH/DCRL)

The DCRH high-byte register and the DCRL low-byte register are the main gas gauging registers for the bq2052. The DCR registers are incremented during discharge.

Writing to the DCR registers affects the available charge counts and, therefore, affects the bq2052 gas gauge operation.

Display

The bq2052 can directly display remaining capacity information using low-power LEDs. The bq2052 uses the CAC value in relation to FNAC as the basis for the display activity. The bq2052 displays the battery's remaining capacity in either of three modes selected with program pin $PROG_5$. The display is activated using the $\overline{DISP}$ input. When $\overline{DISP}$ is connected to V_{CC}, the SEG outputs are OFF. When pulled low, the segment outputs turn ON for a period of 4 ± 0.5s, depending on the selected mode.

The segment outputs are modulated as two banks, with segments 1, 3, and 5 alternating with segments 2 and 4. The segment outputs are modulated at approximately 100Hz with each segment bank active for 30% of the period. In incremental and bar graph modes, SEG1 blinks at a 4Hz rate whenever VSB is below VEDV1 (EDV1 flag bit set in FLGS1), indicating a low-battery condition. When VSB is below VEDVF (EDVF flag bit set in FLGS1) the display outputs are disabled in all modes.

In incremental mode ($PROG_5$ = L), the battery charge state is displayed on pins SEG1–SEG4. The charge state condition indicated by each segment is shown in Table 7. Only the segment pin representing the present remaining capacity is ON (low); all other segments are OFF (high impedance). When $\overline{DISP}$ is pulled low, the display is active for 10s.

Table 7. Incremental Display Mode
$PROG_5$ = L

SEG Pin ON	Remaining Capacity
SEG4	90 -100%
SEG3	50 - < 90%
SEG2	20 - < 50%
SEG1	< 20%
SEG1—BLINK	$V_{SB} < V_{EDV1}$

In binary mode (PROG5 = H), the battery charge state is displayed using only pins SEG1 and SEG2, with the remaining capacity indication defined as in Table 8. When $\overline{DISP}$ is pulled low, the display is active for 4s.

Table 8. Binary Display Mode
$PROG_5$ = H

SEG 1	SEG 2	Remaining Capacity
ON	ON	70 -100%
ON	OFF	40 - < 70%
OFF	ON	10 - < 40%
OFF	OFF	< 10% or $V_{SB} < V_{EDVF}$

In bar graph mode ($PROG_5$ = Z), the battery charge state is displayed using pins SEG1 through SEG 5 according to Table 9. When $\overline{DISP}$ is pulled low, the display is active for 4s.

Microregulator

A micro-power source for the bq2052 can be inexpensively built using a FET and an external resistor as shown in Figure 1.

RBI Input

The RBI input pin should be used with a storage capacitor or external supply to provide backup potential to the internal bq2052 registers when V_{CC} drops below 3.0V. V_{CC} is output on RBI when V_{CC} is above 3.0V. If using an external supply (such as the bottom series cell) as the backup source, an external diode is required for isolation.

Initialization

The bq2052 can be initialized by removing V_{CC} and grounding the RBI pin for 5s or by a command over the serial port. The serial port reset command requires writing 78h to register CMDWD (address = 00h).

On initialization with PROG6 = H, the bq2052 sets the registers as

FNAC = PFC
CACH = PFC
CACL = 0x00
RCAC = 0x64
FLGS1 = 0x90

Table 9. Bar Graph Display Mode
$PROG_5$ = Z

SEG1	SEG2	SEG3	SEG4	SEG5	Remaining Capacity
ON	ON	ON	ON	ON	80 - 100%
ON	ON	ON	ON	OFF	60 - < 80%
ON	ON	ON	OFF	OFF	40 - < 60%
ON	ON	OFF	OFF	OFF	20 - < 40%
ON	OFF	OFF	OFF	OFF	< 20%
BLINK	OFF	OFF	OFF	OFF	VSB < VEDV1

On initialization with PROG6=L, the bq2052 sets the registers as

FNAC = 0x00
CACH = 0x00
CACL = 0x00
RCAC = 0x00
FLGS1 = 0x10

Layout Considerations

The bq2052 measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
REF	Relative to V_{SS}	-0.3	+8.5	V	Current limited by R1 (see Figure 1)
V_{SR}	Relative to V_{SS}	-0.3	Vcc+0.7	V	Recommended 100KΩ series resistor should be used to protect SR in case of a shorted battery.
T_{OPR}	Operating temperature	-20	+70	°C	Commercial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDV1}	First empty warning	0.73	0.76	0.79	V	SB, default
V_{EDVF}	Final empty warning	-	V_{EDV1} - 0.10	-	V	SB, default
V_{SRO}	SR sense range	-300	-	+500	mV	SR, V_{SR} + V_{OS}
V_{SRD}	Valid discharge	-	-	-250	µV	V_{SR} + V_{OS} (see note)

Note: V_{OS} is affected by PC board layout. Proper layout guidelines should be followed for optimal performance. See "Layout Considerations."

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{OS}	Offset referred to V_{SR}	-	±50	±150	µV	$\overline{DISP} = V_{CC}$
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V, HDQ = 0
		-	120	180	µA	V_{CC} = 4.25V, HDQ = 0
		-	170	250	µA	V_{CC} = 6.5V, HDQ = 0
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	$0 < V_{SB} < V_{CC}$
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	$V_{DISP} = V_{SS}$
I_{LCOM}	LCOM input leakage	-0.2	-	0.2	µA	$\overline{DISP} = V_{CC}$
I_{RBI}	RBI data retention current	-	-	100	nA	$V_{RBI} > V_{CC} < 3V$
R_{HDQ}	Internal pulldown	500	-	-	KΩ	
R_{SR}	SR input impedance	10	-	-	MΩ	$V_{SR} < V_{CC}$
V_{IHPFC}	PROG logic input high	V_{CC} - 0.2	-	-	V	$PROG_{1-6}$
V_{ILPFC}	PROG logic input low	-	-	V_{SS} + 0.2	V	$PROG_{1-6}$
V_{IZPFC}	PROG logic input Z	float	-	float	V	$PROG_{1-6}$
V_{OLSL}	SEG output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, $I_{OLS} \leq$ 1.75mA SEG_{1-5}, CP
V_{OLSH}	SEG output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, $I_{OLS} \leq$ 11.0mA SEG_{1-5}, CP
V_{OHML}	LCOM output high, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{OHLCOM} = -5.25mA
V_{OHMH}	LCOM output high, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} > 3.5V, I_{OHLCOM} = -33.0mA
I_{OLS}	SEG sink current	11.0	-	-	mA	At V_{OLSH} = 0.4V, V_{CC} = 6.5V
I_{OL}	Open-drain sink current	5.0	-	-	mA	At $V_{OL} = V_{SS}$ + 0.3V, HDQ
V_{OL}	Open-drain output low	-	-	0.3	V	$I_{OL} \leq$ 5mA, HDQ
V_{IHDQ}	HDQ input high	2.5	-	-	V	HDQ
V_{ILDQ}	HDQ input low	-	-	0.8	V	HDQ
R_{PROG}	Soft pull-up or pull-down resistor value (for programming)	-	-	200	KΩ	$PROG_1$–$PROG_6$
R_{FLOAT}	Float state external impedance	-	5	-	MΩ	$PROG_{1-6}$

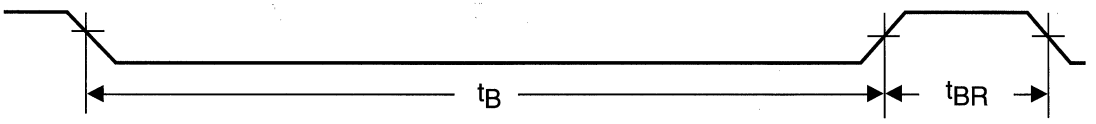
Note: All voltages relative to V_{SS}.

Serial Communication Timing Specification ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2052 (write)	190	-	-	µs	See note
t_{CYCB}	Cycle time, bq2052 to host (read)	190	205	250	µs	
t_{STRH}	Start hold, host to bq2052 (write)	5	-	-	ns	
t_{STRB}	Start hold, bq2052 to host (read)	32	-	-	µs	
t_{DSU}	Data setup	-	-	50	µs	
t_{DSUB}	Data setup	-	-	50	µs	
t_{DH}	Data hold	90	-	-	µs	
t_{DV}	Data valid	-	-	80	µs	
t_{SSU}	Stop setup	-	-	145	µs	
t_{SSUB}	Stop setup	-	-	145	µs	
t_{RSPS}	Response time, bq2052 to host	190	-	320	µs	
t_B	Break	190	-	-	µs	
t_{BR}	Break recovery	40	-	-	µs	

Note: The open-drain HDQ pin should be pulled to at least V_{CC} by the host system for proper HDQ operation. HDQ may be left floating if the serial interface is not used.

Break Timing



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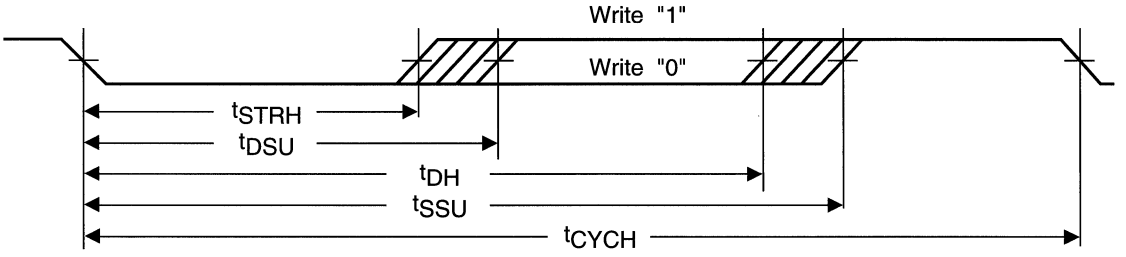
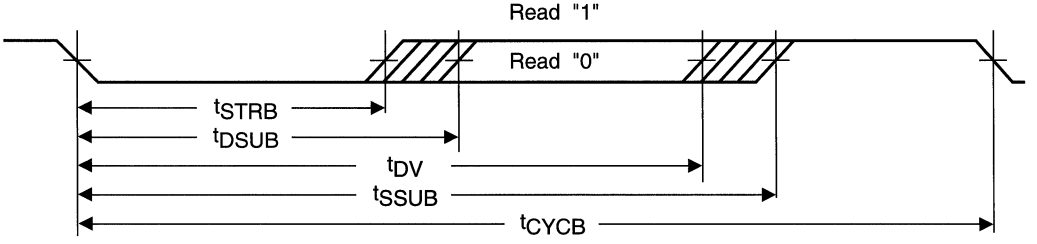
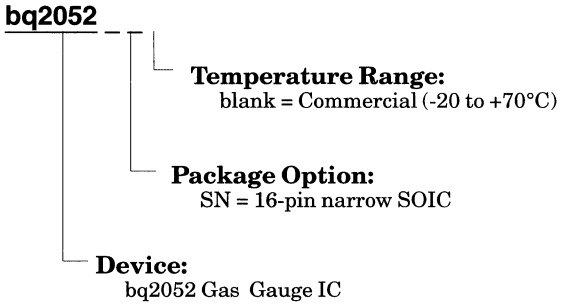
Host to bq2052



bq2052 to Host



Ordering Information



UNITRODE

Preliminary **bq2060**

SBS v1.1-Compliant Gas Gauge IC

Features

- Provides accurate measurement of available charge in NiCd, NiMH, Li-Ion, and Lead Acid batteries
- Supports SBS Smart Battery Data Specification v1.1
- Supports the two wire SMBus v1.1 interface or 1-wire HDQ16
- Reports individual cell voltages
- Monitors and provides control to charge and discharge FETs in Li-Ion protection circuit
- Provides 11-bit resolution on voltage, temperature, and current function reporting
- Measures charge flow using a V-to-F converter with offset of less than 25µV after calibration
- Consumes less than 0.5mW operating
- Drives a five-segment LED display for remaining capacity indication
- 28-pin 150-mil SSOP

General Description

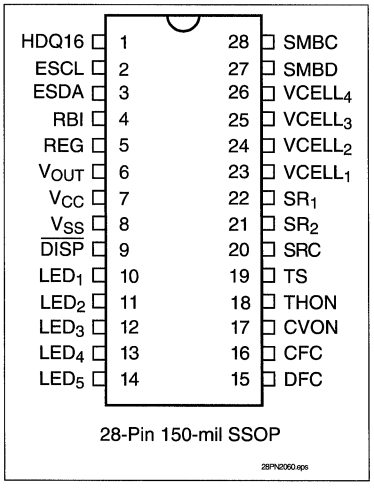
The bq2060 SBS-Compliant Gas Gauge IC is intended for battery pack or in-system installation to maintain an accurate record of available charge in rechargeable batteries. The bq2060 monitors capacity and other critical battery parameters for NiCd, NiMH, Li-Ion, and Lead Acid chemistries. The bq2060 uses a V-to-F converter with automatic offset correction for charge and discharge counting. For voltage, temperature, and current reporting, the bq2060 uses an A-to-D converter. The onboard ADC also monitors individual cell voltages in a Li-Ion battery pack and allows the bq2060 to generate control signals that may be used in conjunction with a pack supervisor to enhance pack safety.

The bq2060 supports the Smart Battery Data (SBData) commands and charge-control functions. It communicates data using the System Management Bus (SMBus) 2-wire protocol or the Unitrode 1-wire HDQ16 protocol. The data available include the battery's remaining capacity, temperature, voltage, current, and remaining run-time predictions. The bq2060 provides LED drivers and a push-button input to depict remaining battery capacity from full to empty in 20% increments with a 5-segment display.

The bq2060 works with an external EEPROM. The EEPROM stores the configuration information for the bq2060, such as the battery's chemistry, self-discharge rate, rate compensation factors, measurement calibration, and design voltage and capacity. The bq2060 uses the programmable self-discharge rate and other compensation factors stored in the EEPROM to accurately adjust remaining capacity for use and standby conditions based on time, rate, and temperature. The bq2060 also automatically calibrates or "learns" the true battery capacity in the course of a discharge cycle from a programmable level of full to empty.

The bq2060 may operate directly from three or four series nickel cells. The REG output can be used to regulate the operating voltage from other battery pack configurations using an external JFET.

Pin Connections



28-Pin 150-mil SSOP

Pin Names

HDQ16	Serial communicaton input/output
ESCL	Serial memory clock
ESDA	Serial memory data and address
RBI	Register backup input
REG	Regulator output
V_{OUT}	EEPROM supply output
V_{CC}	Supply voltage
V_{SS}	Ground
$\overline{DISP}$	Display control input
LED_1–LED_5	LED display segment outputs
DFC	Discharge FET control
CFC	Charge FET control
CVON	Cell voltage divider control
THON	Thermistor bias control
TS	Thermistor voltage input
SRC	Current sense input
SR_1–SR_2	Charge-flow sense resistor inputs
$VCELL_1$–$VCELL_4$	Single-cell voltage inputs
SMBD	SMBus data
SMBC	SMBus clock

Pin Descriptions

HDQ16 **Serial communication input/output**

Open-drain bi-directional communications port.

ESCL **Serial memory clock**

Output to clock the data transfer between the bq2060 and the external nonvolatile configuration memory.

ESDA **Serial memory data and address**

Bi-directional pin used to transfer address and data to and from the bq2060 and the external nonvolatile configuration memory.

RBI **Register backup input**

Input that provides backup potential to the bq2060 registers during periods of low operating voltage. RBI accepts a storage capacitor or a battery input.

REG **Regulator output**

Output that provides a reference to control an n-JFET for V_{CC} regulation to the bq2060 from the battery potential.

V_{OUT} **Supply output**

Output that supplies power to the external EEPROM configuration memory.

V_{CC} **Supply voltage input**

V_{SS} **Ground**

$\overline{DISP}$ **Display control input**

Input that controls the LED drivers LED_1–LED_5

LED_1–LED_5 **LED display segment outputs**

Outputs that each may drive an external LED.

DFC **Discharge FET control output**

Output to control the discharge FET in the Li-Ion pack protection circuitry.

CFC **Charge FET control output**

Output to control the charge FET in the Li-Ion pack protection circuitry.

CVON **Cell voltage divider control output**

Output to connect the cells to the external voltage dividers during cell voltage measurements.

THON **Thermistor bias control output**

Output to connect the thermistor bias resistor during a temperature measurement.

TS **Thermistor voltage input**

Input connection for a thermistor to monitor temperature.

SRC **Current sense voltage input**

Input to monitor instantaneous current.

SR_1–SR_2 **Sense resistor inputs**

Input connections for a small value sense resistor to monitor the battery charge and discharge current flow.

$VCELL_1$–$VCELL_4$ **Single-cell voltage inputs**

Inputs that monitor the series element cell voltages.

SMBD **SMBus data**

Open-drain bi-directional pin used to transfer address and data to and from the bq2060.

SMBC **SMBus clock**

Open drain bi-directional pin used to clock the data transfer to and from the bq2060.

Functional Description

General Operation

The bq2060 determines battery capacity by monitoring the amount of charge input or removed from a rechargeable battery. In addition to measuring charge and discharge, the bq2060 measures battery voltage, temperature, and current, estimates battery self-discharge, and monitors the battery for low-voltage thresholds. The bq2060 measures charge and discharge activity by monitoring the voltage across a small-value series sense resistor between the battery's negative terminal and the negative terminal of the battery pack. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for environmental and operating conditions.

Figure 1 shows a typical bq2060-based battery pack application. The circuit consists of the LED display, voltage and temperature measurement networks, EEPROM connections, serial port, and the sense resistor. The EEPROM stores basic battery pack configuration information and measurement calibration values. The EEPROM must be programmed properly for bq2060 operation. Table 8 shows the EEPROM memory map and outlines the programmable functions available in the bq2060.

The bq2060 accepts an NTC thermistor (Semitec 103AT) for temperature measurement. The bq2060 uses the thermistor to monitor battery pack temperature, detect a battery full charge condition, and compensate for self-discharge and charge/discharge battery efficiencies.

Measurements

The bq2060 uses a fully differential, dynamically balanced voltage-to-frequency converter (VFC) for charge measurement and a sigma delta analog-to-digital converter (ADC) for battery voltage, current, and temperature measurement.

Charge and Discharge Counting

The VFC measures the charge and discharge flow of the battery by monitoring a small-value sense resistor between the SR_1 and SR_2 pins as shown in Figure 1. The VFC measures bipolar signals up to 300mV in magnitude. The bq2060 detects "charge" activity when $V_{SR} = V_{SR2} - V_{SR1}$ is positive and a "discharge" activity when $V_{SR} = V_{SR2} - V_{SR1}$ is negative. The bq2060 integrates the signal over time using an internal counter. The fundamental rate of the counter is 3.125µVh.

Offset Calibration

The bq2060 provides an auto-calibration feature to cancel the voltage offset across SR_1 and SR_2 for maximum charge measurement accuracy. The calibration routine is initiated by issuing a command to ManufacturerAccess(). The bq2060 is capable of canceling an offset down to 4µV.

Digital Filter

The bq2060 does not integrate charge or discharge counts below the digital filter threshold. The digital filter threshold is programmed in the EEPROM.

Voltage

In conjunction with monitoring SR_1 and SR_2 for charge and discharge currents, the bq2060 monitors the battery pack potential and the individual cell voltages through the $VCELL_1$-$VCELL_4$ pins. The bq2060 measures the pack voltage and reports the result in Voltage(). For nickel chemistries, the bq2060 measures the pack voltage with $VCELL_4$. For Li-Ion, the bq2060 measures the pack voltage with the most positive VCELL input. The bq2060 can also measure the voltage at up to four series elements in a battery pack. The individual cell voltages are stored in the Manufacturer Data area. The bq2060 converts the signals at the $VCELL_1$–$VCELL_4$ inputs every 2 seconds.

The $VCELL_1$-$VCELL_4$ inputs are divided down from the cells using high-tolerance resistors, as shown in Figure 1. The maximum input for $VCELL_1$–$VCELL_4$ is 1.25V. The voltage dividers for the inputs must be set so that the voltages at the inputs do not exceed the 1.25V limit under all operating conditions. Also, the dividers on $VCELL_1$–$VCELL_2$ must be half of that of $VCELL_3$–$VCELL_4$. To reduce current consumption from the battery, the CVON output may used to connect the divider to the cells only during measurement period. CVON is high impedance when the cells are measured, and driven low otherwise. See Table 1.

Table 1. Example $VCELL_1$–$VCELL_4$ Divider and Input Range

Voltage Input	Fixed Divider Ratio	Full-Scale Input (V)
$VCELL_4$	16	20.0
$VCELL_3$	16	20.0
$VCELL_2$	8	10.0
$VCELL_1$	8	10.0

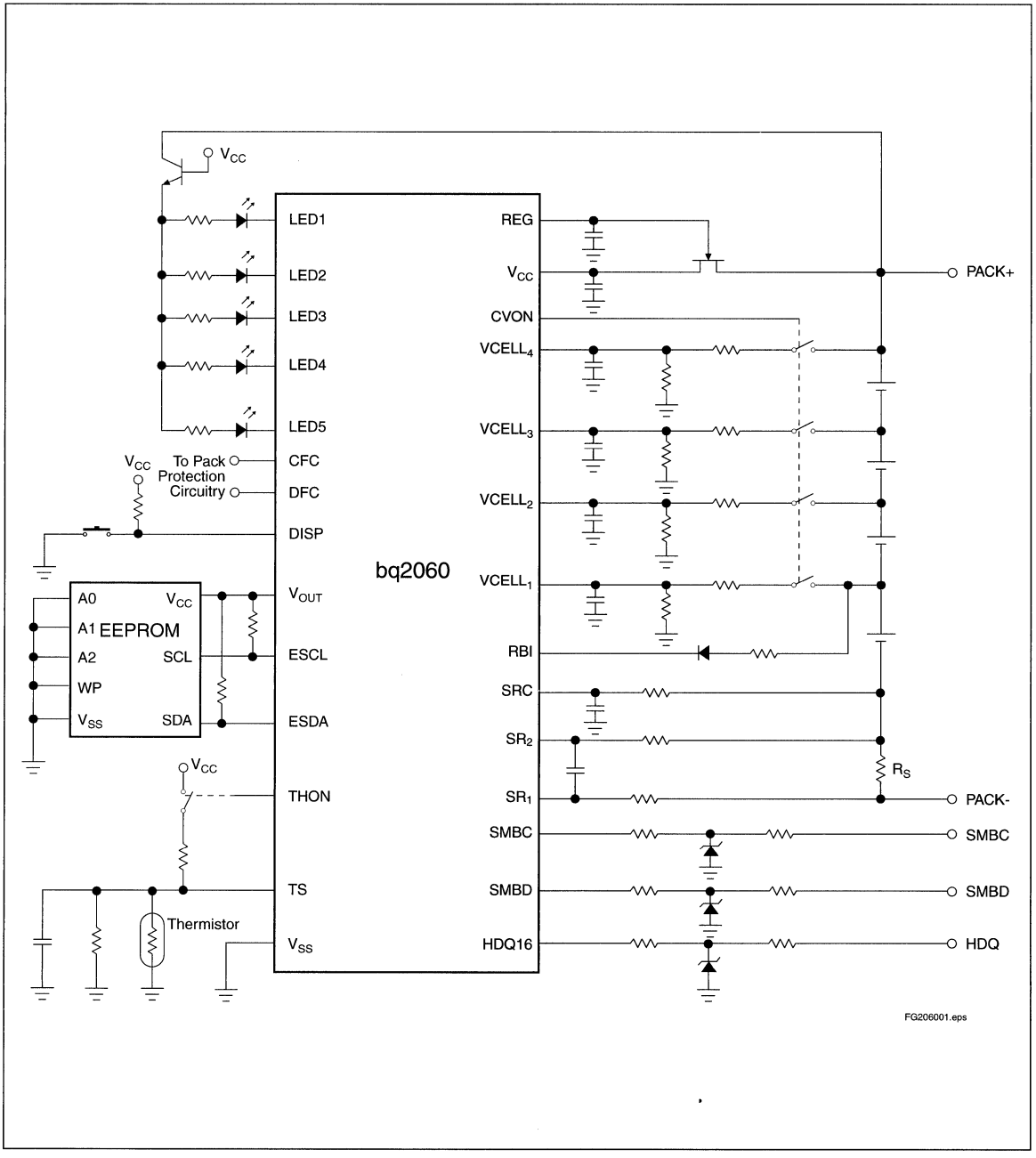


Figure 1. Battery Pack Application Diagram–LED Display and Series Cell Monitoring

Table 2. SRC Input Range

Sense Resistor (Ω)	Current() 1 LSB Accuracy (mA)	Full-Scale Input (A)
0.02	30.5	±15.0
0.03	20.4	±10.0
0.05	12.2	±6.0
0.10	6.1	±3.0

Current

The SRC input of the bq2060 measures battery charge and discharge current. The SRC ADC input converts the current signal from the series sense resistor every 2 seconds and stores the result in Current(). The full-scale input range to SBC is limited to ±300mV as shown in Table 2.

Temperature

The TS input of the bq2060 in conjunction with an NTC thermistor measure the battery temperature as shown in Figure 1. The bq2060 reports temperature in Temperature(). THON may be used to connect the bias source to the thermistor when the bq2060 samples the TS input. THON is high impedance when the temperature is measured, and driven low otherwise.

Gas Gauge Operation

General

The operational overview in Figure 2 illustrates the gas gauge operation of the bq2060. Table 3 describes the bq2060 registers.

The bq2060 accumulates a measure of charge and discharge currents and estimates self-discharge of the battery. The bq2060 compensates the charge current measurement for temperature and state-of-charge of the battery. The bq2060 also adjusts the self-discharge estimation based on temperature.

The main counter RemainingCapacity() (RM) represents the available capacity or energy in the battery at any given time. The bq2060 adjusts RM for charge and self-discharge compensation factors. The information in the RM register is accessible through the communications ports and is also represented through a 5-segment LED display.

The FullChargeCapacity() (FCC) register represents the last measured full discharge of the battery. It is used as the battery's full-charge reference for relative capacity indication. The bq2060 updates FCC when the battery undergoes a qualified discharge from nearly full to a low battery level. FCC is accessible through the serial communications ports.

The Discharge Count Register (DCR) is a non-accessible register that only tracks discharge of the battery. The bq2060 uses the DCR register to update the FCC regis-

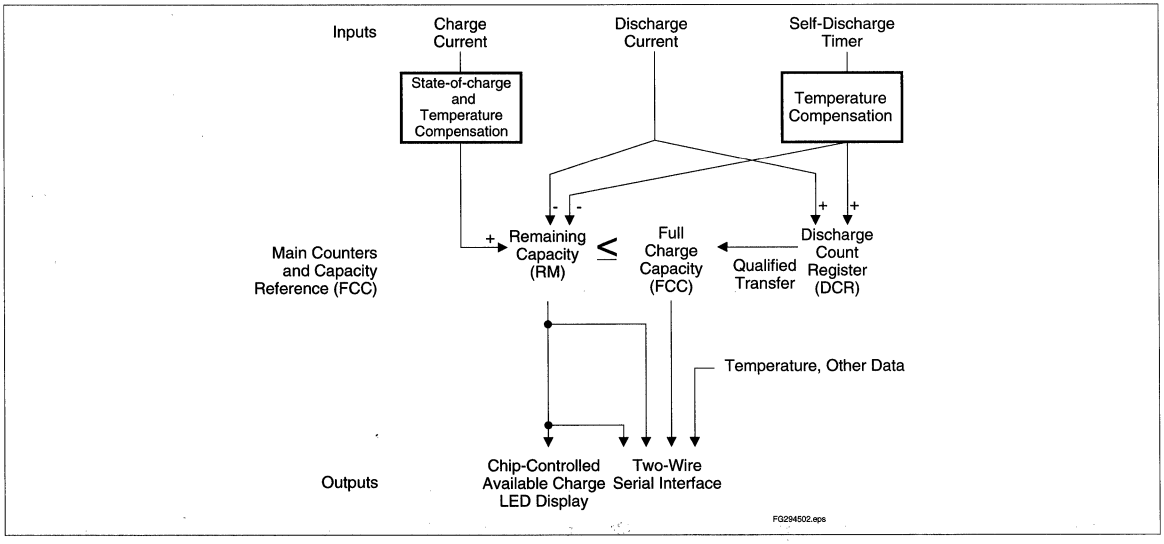


Figure 2. Operational Overview

Table 3. bq2060 Register Functions

Function	Command Code		Access	Units
	SMBus	HDQ16		
ManufacturerAccess	0x00	0x00	read/write	n/a
RemainingCapacityAlarm	0x01	0x01	read/write	mAh, mWh
RemainingTimeAlarm	0x02	0x02	read/write	minutes
BatteryMode	0x03	0x03	read/write	n/a
AtRate	0x04	0x04	read/write	mA, mW
AtRateTimeToFull	0x05	0x05	read	minutes
AtRateTimeToEmpty	0x06	0x06	read	minutes
AtRateOK	0x07	0x07	read	Boolean
Temperature	0x08	0x08	read	0.1°K
Voltage	0x09	0x09	read	mV
Current	0x0a	0x0a	read	mA
AverageCurrent	0x0b	0x0b	read	mA
MaxError	0x0c	0x0c	read	percent
RelativeStateOfCharge	0x0d	0x0d	read	percent
AbsoluteStateOfCharge	0x0e	0x0e	read	percent
RemainingCapacity	0x0f	0x0f	read	mAh, 10mWh
FullChargeCapacity	0x10	0x10	read	mAh, 10mWh
RunTimeToEmpty	0x11	0x11	read	minutes
AverageTimeToEmpty	0x12	0x12	read	minutes
AverageTimeToFull	0x13	0x13	read	minutes
ChargingCurrent	0x14	0x14	read	mA
ChargingVoltage	0x15	0x15	read	mV
Battery Status	0x16	0x16	read	n/a
CycleCount	0x17	0x17	read	cycles
DesignCapacity	0x18	0x18	read	mAh, 10mWh
DesignVoltage	0x19	0x19	read	mV
SpecificationInfo	0x1a	0x1a	read	n/a
ManufactureDate	0x1b	0x1b	read	n/a
SerialNumber	0x1c	0x1c	read	integer
Reserved	0x1d–0x1f	0x1d - 0x1f	-	-
ManufacturerName	0x20	0x20–0x25	read	string
DeviceName	0x21	0x28–0x2b	read	string
DeviceChemistry	0x22	0x30–0x32	read	string
ManufacturerData	0x23	0x38–0x3a	read	string
Pack Status	0x2f (LSB)	0x2f (LSB)	read	n/a
Pack Configuration	0x2f (MSB)	0x2f (MSB)	read	n/a
VCELL4	0x3c	0x3c	read	mV
VCELL3	0x3d	0x3d	read	mV
VCELL2	0x3e	0x3e	read	mV
VCELL1	0x3f	0x3f	read	mV

ter if the battery undergoes a qualified discharge from nearly full to a low battery level. In this way, the bq2060 learns the true discharge capacity of the battery under system use conditions.

Main Gas Gauge Registers

RemainingCapacity() (RM)

On initialization, the bq2060 sets RM to 0. RM counts up during charge to a maximum value of FCC and down during discharge and self-discharge to 0. In addition to charge and self-discharge compensation, the bq2060 calibrates RM at three different low battery voltage thresholds, EDV2, EDV1, and EDV0. This provides a voltage-based calibration to the RM counter.

DesignCapacity() (DC)

The DC is the user-specified battery full capacity. It is programmed from the EEPROM and represents the full-battery reference for the absolute display mode.

FullChargeCapacity() (FCC)

FCC is the last measured discharge capacity of the battery. On initialization, the bq2060 sets FCC to the value stored in EEPROM. During subsequent discharges, the bq2060 updates FCC with the last measured discharge capacity of the battery. The last measured discharge of the battery is based on the value in the DCR register after a qualified discharge occurs. Once updated, the bq2060 writes the new FCC value to EEPROM. FCC represents the full battery reference for the relative display mode and relative state of charge calculations.

Discharge Count Register (DCR)

The DCR register counts up during discharge, independent of RM. DCR can continue to count after RM has counted down to 0. Prior to RM = 0, both discharge activity and self-discharge increment DCR. After RM = 0, only discharge activity increments DCR. DCR resets to 0 when RM = FCC and stops counting when the battery voltage reaches the EDV2 threshold on discharge.

Capacity Learning (FCC Update) and Qualified Discharge

The bq2060 updates FCC with an amount based on the value in DCR if a qualified discharge occurs. The new value for FCC equals the DCR value plus the programmable nearly full and low battery levels, according to the following equation.

$$FCC\ (New) = DCR + FCC * [(100 - \textit{Near Full \%}) + \textit{Battery Low \%}], \quad (1)$$

where

Near Full % = value stored in EE 0x46
Battery Low % = value stored in EE 0x68

A qualified discharge occurs if the battery discharges from RM = FCC * *Near Full %* to the EDV2 voltage threshold with the following conditions:

- No valid charge activity occurs during the discharge period. A valid charge is defined as an input of 10mAh into the battery.
- No more than 256mAh of self-discharge occurs during the discharge period.
- The battery voltage reaches the EDV2 threshold during the discharge period.

FCC cannot be reduced by more than 256mAh during any single update cycle. The bq2060 saves the new FCC value to the EEPROM within 2s of it being updated.

End-of-Discharge Thresholds and Capacity Correction

The bq2060 monitors the battery for three compensated low-voltage thresholds based on the EDV values (*EDV0*, *EDV1*, and *EDV2*) stored in EEPROM. The bq2060 disables EDV detection if Current() exceeds the *Overload Current* threshold programmed in EE 0x38. The bq2060 resumes EDV threshold detection after Current() drops below the overload current threshold.

The bq2060 uses the thresholds to apply voltage-based corrections to the RM register according to Table 4. The EDV thresholds are set by the values programmed in EEPROM locations EDV0 in EE 0x4a–0x4b, *EDV1* in EE 0x4c–0x4d, and *EDV2* in EE 0x4e–0x4f.

Table 4. State of Charge Based on Low Battery Voltage

Threshold	State of Charge in RM
EDV0	0%
EDV1	3%
EDV2	*Battery Low %*

The bq2060 adjusts RM as it detects each threshold. If the voltage threshold is reached before the corresponding capacity on discharge, the bq2060 reduces RM to the appropriate amount as shown in Table 3. If RM reaches the capacity level before the voltage threshold is reached on discharge, the bq2060 prevents RM from decreasing until the battery voltage reaches the corresponding threshold.

For Li-Ion packs, the bq2060 compensates the end-of-discharge thresholds for the battery temperature and discharge rate. The compensation model is based on the following formulas where T = temperature in °C; R = discharge rate; EDV_n = nominal EDV0, EDV1, or EDV2; $EDVC_n$ = compensated EDV0, EDV1, EDV2.

(2)

Case 1: $T \geq 15°C$

$$EDVC_n = EDV_n + X_1 * (T - 15) - X_2 * R$$

Case 2: $T < 15°C, R \geq 0.5C$

$$EDVC_n = EDV_n * X_3 * (T - 15) - X_2 * R$$

Case 3: $T < 15°C, R < 0.5C$

$$EDVC_n = EDV_n + 2 * R * X_3 * (T - 15) - X_2 * R$$

The EDV compensation factors stored in EEPROM, *EDV0F, EDV1F,* and *EDV2F,* determine X_1, X_2, and X_3. For the ideal model, $X_1 = 0.002$, $X_2 = 0.3$, and $X_3 = 0.01$. With these factors, the voltage correction applied at room temperature and a low rate is small but increases at higher rate and temperature. The bq2060 applies no EDV compensation in nickel packs.

Charge Control

Charging Voltage and Current Broadcasts

The bq2060 supports SBS charge control by broadcasting the ChargingCurrent() and ChargingVoltage() to the Smart Charger address. The bq2060 broadcasts the requests every 10s. The bq2060 updates the values used in the charging current and voltage broadcasts based on the battery's state of charge, voltage, and temperature. The fast-charge rate is programmed in *Fast-Charging Current* EE 0x1a - 0x1b while the charge voltage is programmed in *Charging Voltage* EE 0x0a-0x0b.

The bq2060 internal charge control is compatible with popular rechargeable chemistries. The primary charge-termination techniques include a change in temperature over a change in time ($\Delta T/\Delta t$) and current taper, for nickel-based and Li-Ion chemistries, respectively. The bq2060 also provides pre-charge qualification and a number of safety charge suspensions based on current, voltage, temperature, and state of charge.

Alarm Broadcasts to Smart Charger and Host

If any of the bits 8–15 in BatteryStatus() is set, the bq2060 broadcasts an AlarmWarning() message to the Host address. If any of the bits 12–15 in BatteryStatus() are set, the bq2060 also sends an AlarmWarning() message to the Smart Charger address. The bq2060 repeats the AlarmWarning() message every 10s until the bits are cleared.

Pre-Charge Qualification

The bq2060 sets ChargingCurrent() to the pre-charge rate as programmed in *Pre-Charge Current* EE 0x1e-0x1f under the following conditions:

- **Voltage:** The bq2060 requests the pre-charge charge rate when Voltage() is below the EDV0 threshold.
- **Temperature:** The bq2060 requests the pre-charge rate when Temperature() is less than 12°C. If this occurs, Temperature() must rise above 15°C before the bq2060 requests the fast charge rate.

Charge Suspension

The bq2060 may temporarily suspend charge if it detects a charging fault. A charging fault includes the following conditions.

- **Overcurrent:** An overcurrent condition exists when the bq2060 measures the charge current to be more than the *Overcurrent Margin* above the ChargingCurrent(). *Overcurrent Margin* is programmed in EE 0x3c. On detecting an overcurrent condition, the bq2060 sets the ChargingCurrent() to zero and sets the TERMINATE_CHARGE_ALARM bit in BatteryStatus(). The overcurrent condition is cleared when the measured current drops below the ChargingCurrent plus the *Overcurrent Margin.*
- **Overvoltage:** An overvoltage condition exists when the bq2060 measures the battery voltage to be more than the *Overvoltage Margin* above the ChargingVoltage(). Overvoltage Margin is programmed in EE 0x3b. On detecting an overvoltage condition, the bq2060 sets the ChargingCurrent() to zero and sets the TERMINATE_CHARGE_ALARM bit in BatteryStatus(). The overvoltage condition is cleared when the measured voltage drops below the ChargingVoltage() plus the *Overvoltage Margin.*
- **Over-Temperature:** An over-temperature condition exists when Temperature() exceeds the *Max T* value programmed in EE 0x60. On detecting an over-temperature condition, the bq2060 sets the ChargingCurrent() to zero and sets the OVER_TEMP_ALARM bit in BatteryStatus(). The over-temperature condition is cleared when Temperature() drops 3 degrees C below the *Max T* value.
- **Overcharge:** An overcharge condition exists if the battery is charged more than the *Maxmum Overcharge* value after RM = FCC. *Maximum Overcharge* is programmed in EE 0x2e–0x2f. On detecting an overcharge condition, the bq2060 sets the ChargingCurrent() to the maintenance charge rate and sets the FULLY_CHARGED bit in BatteryStatus(). The maintenance charge rate,

Maintenance Charging Current, is programmed in EE 0x1c - 0x1d.

Primary Charge Termination

The bq2060 terminates charge if it detects a charge-termination condition. A charge-termination condition includes the following.

- **ΔT/Δt:** For ΔT/Δt, the bq2060 detects a change in temperature over many seconds. The ΔT/Δt setting is programmable in both the temperature step, *DeltaT* (1.6°C - 4.6°C), and the time step, *DeltaT Time* (20s-300s). Typical settings for 1°C/minute include 2°C/120s and 3°C/180s. Longer times are required for increased slope resolution. The *DeltaT* value is programmed in EE 0x60 and the *Delta T Time* in EE 0x61.

  In addition to the ΔT/Δt timer, a hold-off timer starts when the battery is being charged at more than 255mA and the temperature is above 25°C. Until this timer expires, ΔT/Δt detection is suspended. If Current() drops below 256mA or Temperature() below 25°C, the hold-off timer resets and restarts only when the current and temperature conditions are met again. The hold-off timer is programmable (20s – 300s) with *DeltaT Holdoff Time* value in EE 0x62.

- **Current Taper:** For current taper, ChargingVoltage() must be set to the pack voltage desired during the constant-voltage phase of charging. The bq2060 detects a current taper termination when it measures the highest cell voltage in the pack to be greater than the voltage determined by *Current Taper Cell Voltage* and the charging current is below a threshold determined by *Current Taper Threshold*, for at least 40s. The bq2060 uses the VFC to measure current-for-current taper termination. The current polarity must remain positive as measured by the VFC during this time period.

Once the bq2060 detects a primary charge termination, the bq2060 sets the OVER_CHARGED_ALARM, TERMINATE_CHARGE_ALARM and FULLY_CHARGED bits in BatteryStatus(), and sets the ChargingCurrent() to zero. The bq2060 sets the ChargingCurrent() to the maintenance charge rate when it no longer detects the primary charge termination condition. On termination, the bq2060 also sets RM to a programmed percentage of FCC, provided that RelativeStateOfCharge() is below the desired percentage of FCC and the CSYNC bit in *Pack Configuration* EE 0x3f is set. If the CSYNC bit is not set and RelativeStateOfCharge() is less than the programmed percentage of FCC, the bq2060 clears the FULLY_CHARGED bit in BatteryStatus(). The programmed percentage of FCC, *Fast Charge Termination %*, is set in EE 0x3d. The bq2060 clears the alarm bits when Current() drops below 256mA. The bq2060 also clears the FULLY-CHARGED bit when RelativeStateOfCharge() is less than *Fully Charged Clear %* programmed in EE 0x69.

Display Port

General

The display port drives a 5-LED bar graph display. The display is activated either by a logic signal on the $\overline{DISP}$ input or by the detection of charge current. The bq2060 can display RM in either a relative or absolute mode with each LED representing a percentage of the full battery reference. In relative mode, the bq2060 uses FCC as the full battery reference; in absolute mode, it uses DC.

Activation

The display may be activated at any time by a high-to-low transition on the $\overline{DISP}$ input. This is usually accomplished with a pull-up resistor and a pushbutton switch. Detection of the transition activates the display and starts a display timer that advances for four seconds. The timer expires and turns off the display whether $\overline{DISP}$ was brought low momentarily or held low indefinitely. Reactivation of the display requires that the $\overline{DISP}$ input return to a logic-high state and then transition low again. The second high-to-low transition must occur after the display timer expires. The bq2060 requires the $\overline{DISP}$ input to remain stable for a minimum of 250ms to detect the logic state.

The display activates automatically when the battery is being charged at 100mA or more. This activation mechanism overrides the push-button activation conditions and has no time-out associated with it. When Current() is less than 100mA, the display turns off unless the $\overline{DISP}$ input has been forced low.

If Voltage() is less than the EDV0 threshold, the bq2060 disables the LED display.

Display Modes

In relative mode, each LED output represents 20% of the RelativeStateOfCharge() value. Table 5 shows the relative display operation. Unless noted, Voltage() is greater than the EDV0 threshold.

The bq2060 blinks LED1 if RelativeStateOfCharge() is less than 10%.

In absolute mode, each LED output represents 20% of the AbsoluteStateOfCharge() value. Table 6 shows the absolute display operation. Unless noted, Voltage() is greater than the EDV0 threshold.

The bq2060 blinks LED1 if AbsoluteStateOfCharge() is less than 10%.

Table 5. Relative Display Mode

Condition Relative StateOfCharge()	LED1	LED2	LED3	LED4	LED5
Voltage()<EDV0	OFF	OFF	OFF	OFF	OFF
<10%	BLINK	OFF	OFF	OFF	OFF
≥10%, ≤20%	ON	OFF	OFF	OFF	OFF
>20%, ≤40%	ON	ON	OFF	OFF	OFF
>40%, ≤60%	ON	ON	ON	OFF	OFF
>60%, ≤80%	ON	ON	ON	ON	OFF
>80%, ≤100%	ON	ON	ON	ON	ON

Table 6. Absolute Display Mode

Condition Relative StateOfCharge()	LED1	LED2	LED3	LED4	LED5
Voltage()<EDV0	OFF	OFF	OFF	OFF	OFF
<10%	BLINK	OFF	OFF	OFF	OFF
≥10%, ≤20%	ON	OFF	OFF	OFF	OFF
>20%, ≤40%	ON	ON	OFF	OFF	OFF
>40%, ≤60%	ON	ON	ON	OFF	OFF
>60%, ≤80%	ON	ON	ON	ON	OFF
>80%	ON	ON	ON	ON	ON

Communication

The bq2060 includes two types of communication ports: SMBus and HDQ16. The SMBus interface is a two-wire bi-directional protocol utilizing the SMBC (clock) and SMBD (data) pins. The HDQ16 interface is a one-wire bi-directional protocol utilizing the HDQ16 pin.

The communication ports allow a host controller, an SMBus-compatible device, or other processor to access the memory registers of the bq2060. In this way a system can efficiently monitor and manage the battery.

SMBus

The SMBus interface is a command-based protocol. A processor acting as the bus master initiates communication to the bq2060 by generating a START condition. A START condition consists of a high-to-low transition of the SMBD line while the SMBC is high. The processor then sends the bq2060 device address of 0001011 (bits 7–1) plus a R/$\overline{W}$ bit (bit 0) followed by an SMBus command code. The R/$\overline{W}$ bit (LSB) and the command code instruct the bq2060 to either store the forthcoming data to a register specified by the SMBus command code or output the data from the specified register. The processor completes the access with a STOP condition. A STOP condition consists of a low-to-high transition of the SMBD line while the SMBC is high. With SMBus, the most-significant bit (MSB) of a data byte is transmitted first.

In some instances, the bq2060 acts as the bus master. This occurs when the bq2060 broadcasts charging requirements and alarm conditions to device addresses 0x12 (SBS Smart Charger) and 0x10 (SBS Host Controller.)

SMBus Protocol

The bq2060 supports the following SMBus protocols:

- Read Word
- Write Word
- Read Block

A processor acting as the bus master uses the three protocols to communicate with the bq2060. The bq2060 acting as the bus master uses the Write Word protocol.

The SMBD and SMBC pins are open drain and require external pull-up resistors.

SMBus Packet Error Checking

The bq2060 supports Packet Error Checking as a mechanism to confirm proper communication between it and another SMBus device. Packet Error Checking requires that both the transmitter and receiver calculate a Packet Error Code (PEC) for each communication message. The device that supplies the last byte in the communication message appends the PEC to the message. The receiver compares the transmitted PEC to its PEC result to determine if there is a communication error.

PEC Protocol

The bq2060 can receive or transmit data with or without PEC. Figure 3 shows the communication protocol for the Read Word, Write Word, and Read Block messages without PEC. Figure 4 includes PEC.

In the Write Word protocol, the bq2060 receives the PEC after the last byte of data from the host. If the host does not support PEC, the last byte of data is followed by a STOP condition. After receipt of the PEC, the bq2060 compares the value to its calculation. If the PEC is correct, the bq2060 responds with an ACKNOWLEDGE. If it is not correct, the bq2060 responds with a NOT ACKNOWLEDGE and sets an error code.

In the Read Word and Block Read, the host generates an ACKNOWLEDGE after the last byte of data sent by the

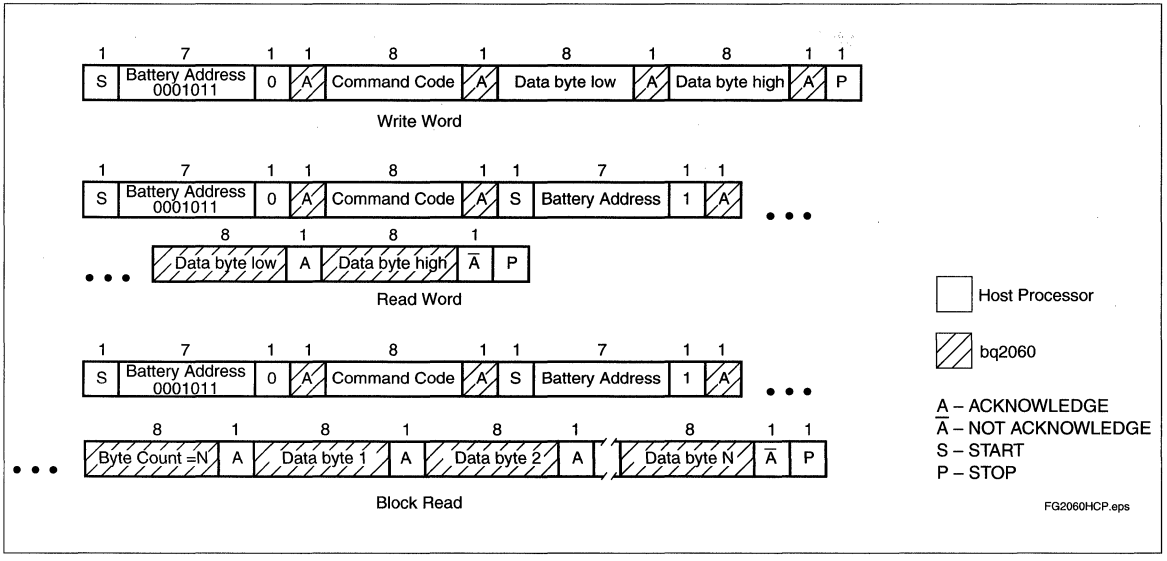


Figure 3. SMBus Communication Protocol without PEC

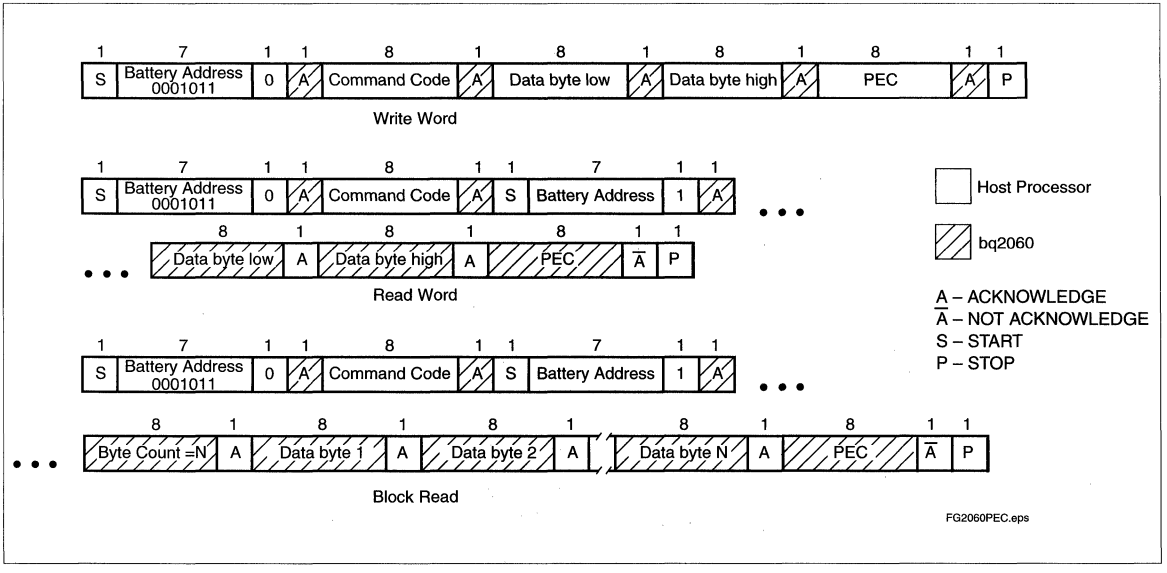


Figure 4. SMBus Communication Protocol with PEC

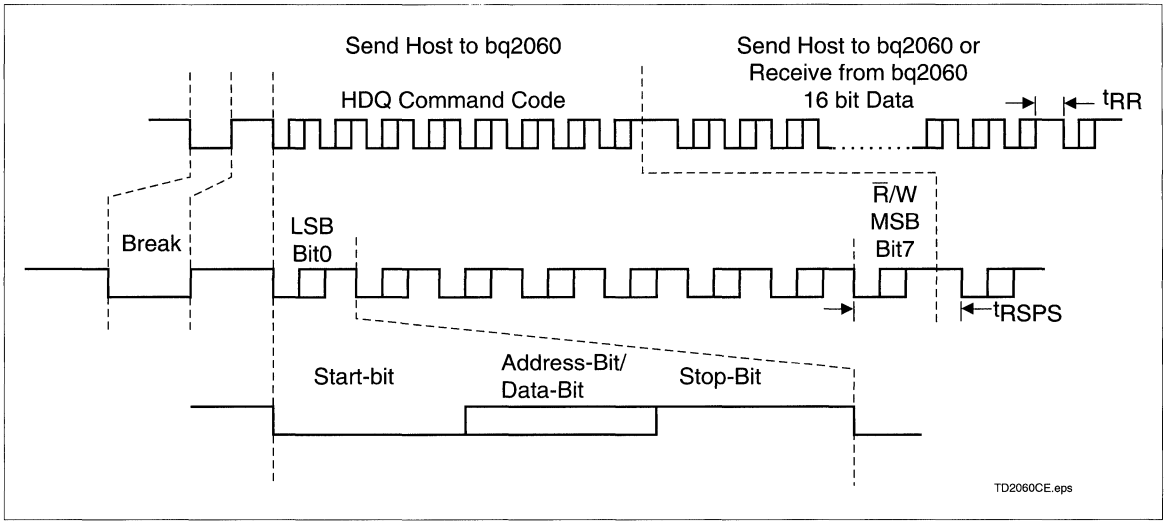


Figure 5. HDQ16 Communication Example

bq2060. The bq2060 then sends the PEC and the host acting as a master-receiver generates a NOT ACKNOWLEDGE and a STOP condition.

PEC Calculation

The basis of the PEC calculation is an 8-bit Cyclic Redundancy Check (CRC-8) based on the polynomial C(X) = $X^8 + X^2 + X^1 + 1$. The PEC calculation includes all bytes in the transmission, including address, command, and data. The PEC calculation does not include ACKNOWLEDGE, NOT ACKNOWLEDGE, START, STOP, and Repeated START bits.

For example, the host requests RemainingCapacity() from the bq2060. This includes the host folloing the Read Word protocol. The bq2060 calculates the PEC based on the following 5 bytes of data, assuming the remaining capacity of the battery is 1001mAh.

- Battery Address with R/$\overline{W}$ = 0: 0x16
- Command Code for RemainingCapacity(): 0x0f
- Battery Address with R/$\overline{W}$ = 1: 0x17
- RemainingCapacity(): 0x03e9

For 0x160f17e903, the bq2060 transmits a PEC of 0xe8 to the host.

SMBus On and Off State

The bq2060 detects whether the SMBus enters the "Off State" by monitoring the SMBC and SMBD lines. When both signals are low for 2s, the bq2060 detects the "Off State". When the SMBC and SMBD lines go high, the bq2060 detects the "On State" and can begin communication within 1ms.

HDQ16

The HDQ16 interface is a command-based protocol. See Figure 5. A processor sends the command code to the bq2060. The 8-bit command code consists of two fields, the 7-bit HDQ16 command code (bits 0–6) and the 1-bit R/$\overline{W}$ field (MSB bit 7). The R/$\overline{W}$ field directs the bq2060 either to

- Store the next 16 bits of data to a specified register or
- Output 16 bits of data from the specified register

With HDQ16, the least-significant bit (LSB) of a data byte (command) or word (data) is transmitted first.

A bit transmission consists of three distinct sections. The first section starts the transmission by either the host or the bq2060 taking the HDQ16 pin to a logic-low state for a period $t_{STRH;B}$. The next section is the actual data-transmission, where the data bit is valid by the time, $t_{DSU;B}$ after the negative edge used to start communication. The data bit is held for a period $t_{DH;DV}$ to allow the host processor or bq2060 to sample the data bit.

The final section is used to stop the transmission by returning the HDQ16 pin to a logic-high state by at least the time $t_{SSU;B}$ after the negative edge used to start communication. The final logic-high state should be until a period $t_{CYCH;B}$ to allow time to ensure that the bit transmission was stopped properly.

If a communication error occurs (e.g., $t_{CYCB} > 250\mu s$), the host sends the bq2060 a BREAK to reinitiate the serial interface. The bq2060 detects a BREAK when the HDQ16 pin is in a logic-low state for a time t_B or greater. The HDQ16 pin is then returned to its normal ready-high logic state for a time t_{BR}. The bq2060 is then ready to receive a command from the host processor.

The HDQ16 pin is open drain and requires an external pull-up resistor.

Command Codes

The SMBus Command Codes are in ( ), the HDQ16 in [ ].

ManufacturerAccess() (0x00); [0x00–0x01]

Description:
This function provides writable command codes to control the bq2060 during normal operation and pack manufacture. The following list of commands are available.

0x0618 Enable Low Power Storage Mode: Activates the low-power storage mode. The bq2060 enters the storage mode after a 10s delay.

0x064d Charge Synchronization: Enables the bq2060 to update RM when an external charger detects a fast charge termination. The bq2060 sets RM to a percentage of FCC as defined in *Fast Charge Termination %*.

0x0653 Enable VFC Calibration: Instructs the bq2060 to begin VFC calibration.

0x0780 SMBus Slave: Configures the bq2060 as an SMBus slave only to disable all broadcasts such as ChargingCurrent(), ChargingVoltage(), and AlarmWarning().

0x079e SMBus Master: Enables the bq2060 to act as an SMBus master to broadcast ChargingCurrent(), ChargingVoltage(), and AlarmWarning().

Purpose:
The ManufacturerAccess() function provides the system host access to bq2060 functions that are not defined by the SBD.

SMBus Protocol: Read or Write Word

Input/Output: Word

RemainingCapacityAlarm() (0x01); [0x01]

Description:
Sets or gets the low-capacity threshold value. Whenever the RemainingCapacity() falls below the low capacity value, the bq2060 sends AlarmWarning() messages to the SMBus Host with the REMAINING_CAPACITY_ALARM bit set. A low-capacity value of 0 disables this alarm. The bq2060 initially sets the low-capacity value to *Remaining Capacity Alarm* value programmed in EE 0x04 - 0x05. The low-capacity value remains unchanged until altered by the RemainingCapacityAlarm() function. The low-capacity value may be expressed in either current (mA) or power (10mWh) depending on the setting of the BatteryMode()'s CAPACITY_MODE bit.

Purpose:
The RemainingCapacityAlarm() function can be used by systems that know how much power they require to save their operating state. It enables those systems to more finely control the point at which they transition into suspend or hibernate state. The low-capacity value can be read to verify the value in use by the Smart Battery's low capacity alarm.

SMBus Protocol: Read or Write Word

Input/Output: Unsigned integer—value below which Low Capacity messages are sent.

Battery Modes		
	CAPACITY_MODE bit = 0	CAPACITY_MODE bit = 1
Units	mAh @ C/5	10mWh @ P/5
Range	0–65,535mAh	0–65,535 10mWh
Granularity	Not applicable	
Accuracy	See RemainingCapacity()	

RemainingTimeAlarm() (0x02); [0x02]

Description:
Sets or gets the remaining time alarm value. Whenever the AverageTimeToEmpty() falls below the remaining time value, the bq2060 sends AlarmWarning() messages to the SMBus Host with the REMAINING_TIME_ALARM bit set. A remaining time value of 0 effectively disables this alarm. The bq2060 initially sets the remaining time value to the *Remaining Time* value programmed in EE 0x02 - 0x03. The remaining time value remains unchanged until altered by the RemainingTimeAlarm() function.

Purpose:
The RemainingTimeAlarm() function can be used by systems that want to adjust when the remaining time alarm warning is sent. The remaining time value can be read to verify the value in use by the Smart Battery's RemainingTimeAlarm().

SMBus Protocol: Read or Write Word

Input/Output:

Unsigned integer—the point below which remaining time messages are sent.

Units: minutes

Range: 0 to 65,535 minutes

Granularity: Not applicable

Accuracy: see AverageTimeToEmpty()

BatteryMode() (0x03); [0x03]

Description:
This function selects the various battery operational modes and reports the battery's mode and requests.

Defined modes include:

- Whether the battery's capacity information is specified in mAh or 10mWh (CAPACITY_MODE bit)
- Whether the ChargingCurrent() and ChargingVoltage() values are broadcast to the Smart Battery Charger when the Smart Battery requires charging (CHARGER_MODE bit)
- Whether all broadcasts to the Smart Battery Charger and Host are disabled

The defined request condition is the battery requesting a conditioning cycle (CONDITION_FLAG).

Purpose:
The CAPACITY_MODE bit allows power management systems to best match their electrical characteristics with those reported by the battery. For example, a switching power supply represents a constant power load, whereas a linear supply is better represented by a constant current model. The CHARGER_MODE bit allows a SMBus Host or Smart Battery Charger to override the Smart Battery's desired charging parameters by disabling the bq2060's broadcasts. The CONDITION_FLAG bit allows the battery to request a conditioning cycle.

SMBus Protocol: Read or Write Word

Input/Output:

Unsigned integer —bit mapped— see below.

Units: not applicable

Range: 0–1

Granularity: not applicable

Accuracy: Not applicable

The BatteryMode() word is divided into two halves, the MSB (bits 8–15) which is read/write and the LSB (bits 0–7) which is read only. Attempts to set (write 1's) to the reserved bits in the LSB are prohibited.

Table 7 summarizes the meanings of the individual bits in the BatteryMode() word and specifies the default values if any. Power-on default values, where applicable, are noted.

Table 7. Battery Mode Bits and Values

Battery Mode() Bits	Bits Used	Format	Allowable Values
INTERNAL_CHARGE_CONTROLLER	0	Read only bit flag	
PRIMARY_BATTERY_SUPPORT	1	Read only bit flag	
Reserved	2–6		
CONDITION_FLAG	7	Read only bit flag	0—Battery OK 1—Conditioning cycle requested
CHARGE_CONTROLLER_ENABLED	8	R/W bit flag	
PRIMARY_BATTERY	9	R/W bit flag	
Reserved	10–12		
ALARM_MODE	13	R/W bit flag	0—Enable alarm broadcast (default) 1—Disable alarm broadcast (default)
CHARGER_MODE	14	R/W bit flag	0—Enable broadcast to charger (default) 1—Disable broadcast to charger
CAPACITY_MODE	15	R/W bit flag	0—Report in ma or maH (default) 1—Report in 10mw or 10mWh

INTERNAL_CHARGE_CONTROLLER bit is not used by the bq2060.

PRIMARY_BATTERY_SUPPORT bit is not used by the bq2060.

CONDITION_FLAG bit set indicates that the bq2060 is requesting a conditioning cycle for the battery. A conditioning cycle may be requested because of the characteristics of the battery chemistry and/or the electronics in combination with the usage pattern. The conditioning cycle is pack specific, but typically consists of a full-charge to full-discharge back to full-charge of the pack. The bq2060 clears this flag after it detects that a conditioning cycle has been completed.

CHARGE_CONTROLLER_ENABLED bit is not used by the bq2060. Set to 0 on "On-State."

PRIMARY_BATTERY bit is not used by the bq2060. Set to 0 on "On-State."

ALARM_MODE bit is set to disable the bq2060's ability to master the SMBus and send AlarmWarning() messages to the SMBus Host and the Smart Battery Charger. When set, the bq2060 does NOT master the SMBus, and AlarmWarning() messages are NOT sent to the SMBus Host and the Smart Battery Charger **for a period of no more than 65s and no less than 45s.** When cleared (default), the Smart Battery sends the AlarmWarning() messages to the SMBus Host and the Smart Battery Charger any time an alarm condition is detected.

- The bq2060 polls the ALARM_MODE bit every 125ms. Sixty seconds from the time the bit was last set, the bq2060 automatically enables alarm broadcasts to insure that the accidental deactivation of broadcasts does not persist. An SMBus host that does not want the bq2060 to be a master on the SMBus must therefore continually set this bit at least once per 45s to keep the bq2060 from broadcasting alarms.
- The ALARM_MODE bit defaults to a cleared state when the bq2060 detects the SMBus "On-State."
- The condition of the ALARM-MODE bit does NOT affect the operation or state of the CHARGER_MODE bit which is used to prevent broadcasts of ChargingCurrent() and ChargingVoltage() to the Smart Battery Charger.

CHARGER_MODE bit enables or disables the bq2060's transmission of ChargingCurrent() and ChargingVoltage() messages to the Smart Battery Charger. When set, the bq2060 does NOT transmit ChargingCurrent() and ChargingVoltage() values to the Smart Battery Charger. When cleared, the bq2060 transmits the ChargingCurrent() and ChargingVoltage() values to the Smart Battery Charger when charging is desired. The CHARGER_MODE bit defaults to a cleared state when the bq2060 detects the SMBus "On-State."

CAPACITY_MODE bit indicates if capacity information is reported in mA/mAh or 10mW/10mWh. When set, the bq2060 reports capacity information in 10mW/10mWh as appropriate. When cleared, the bq2060 reports capacity information in mA/mAh as appropriate. Set to 0 on "On-State."

Note 1: The following functions are changed to accept or return values in mA/mAh or 10mW/10mWh depending on the CAPACITY_MODE bit:

- RemainingCapacityAlarm()
- AtRate()
- RemainingCapacity()
- FullChargeCapacity()
- DesignCapacity()

Note 2: The following functions are calculated on the basis of capacity and may be calculated differently depending on the CAPACITY_MODE bit:

- AtRateOK()
- AtRateTimeToEmpty()
- RunTimeToEmpty()
- AverageTimeToEmpty()
- Remaining Time Alarm()
- BatteryStatus()

AtRate() (0x04); [0x04]

Description:
The AtRate() function is the first half of a two-function call-set used to set the AtRate value used in calculations made by the AtRateTimeToFull(), AtRateTimeToEmpty(), and AtRateOK() functions. The AtRate value may be expressed in either current (mA) or power (10mW) depending on the setting of the BatteryMode()'s CAPACITY_MODE bit.

Purpose:
Since the AtRate() function is the first half of a two-function call-set, it is followed by the second function of the call-set that calculates and returns a value based on the AtRate value and the battery's present state. A delay of 300ms is required after writing AtRate() and before reading the second function.

- When the AtRate value is positive, the AtRateTimeToFull() function returns the predicted time to full-charge at the AtRate value of charge.

- When the AtRate value is negative, the AtRateTimeToEmpty() function returns the predicted operating time at the AtRate value of discharge.
- When the AtRate value is negative, the AtRateOK() function returns a Boolean value that predicts the battery's ability to supply the AtRate value of *additional* discharge energy (current or power) for 10 seconds.

The default value for AtRate() is zero. Writing AtRate() values over the HDQ16 serial port does NOT trigger a re-calculation of AtRateTimeToFull(), AtRateTimeToEmpty(), and AtRateOK() functions.

SMBus Protocol: Read or Write Word

Input/Output: Signed integer — charge or discharge; the AtRate value is positive for charge, negative for discharge, and zero for neither (default).

Battery Mode		
	CAPACITY_MODE bit = 0	CAPACITY_MODE bit = 1
Units	mA	10mW
Charge Range	1–32,767mA	1–32,768 10mW
Discharge Range	-1– -32,768mA	-1– -32,768 10mW
Granularity	1 Unit	
Accuracy	NA	

AtRateTimeToFull() (0x05);[0x05]

Description:
Returns the predicted remaining time to fully charge the battery at the AtRate value (mA).

Purpose:
The AtRateTimeToFull() function is part of a two-function call-set used to determine the predicted remaining charge time at the AtRate value in mA. It may be read 300ms after the SMBus Host sets the AtRate value. If read before this delay, the command is No Acknowledged and the error code in BatteryStatus is set to "not ready." Refer to AtRate().

SMBus Protocol: Read Word

Output:

Unsigned integer—predicted time in minutes to fully charge the battery.

Units: minutes

Range: 0 to 65,534 min

Granularity: 2 min or better

Accuracy: ±MaxError() * FullChargeCapacity()/|AtRate()|

Invalid Data Indication: 65,535 indicates the battery is not being charged.

AtRateTimeToEmpty() (0x06); [0x06]

Description:
Returns the predicted remaining operating time if the battery is discharged at the AtRate value.

Purpose:
The AtRateTimeToEmpty() function is part of a two-function call-set used to determine the remaining operating time at the AtRate value. It may be read 300ms after the SMBus Host sets the AtRate value. If read before this delay, the command is No Acknowledged and the error code in BatteryStatus is set to "not ready." Refer to AtRate().

SMBus Protocol: Read Word

Output:

Unsigned integer — estimated operating time left.

Units: minutes

Range: 0 to 65,534 min

Granularity: 2 min or better

Accuracy: -0,+MaxError() * FullChargeCapacity/|AtRate()|

Invalid Data Indication: 65,535 indicates the battery is not being discharged.

AtRateOK() (0x07); [0x07]

Description:
Returns a Boolean value that indicates whether or not the battery can deliver the AtRate value of *additional* energy for 10 seconds (Boolean). If the AtRate value is zero or positive, the AtRateOK() function ALWAYS returns true.

Purpose:
The AtRateOK() function is part of a two-function call-set used by power management systems to determine if the battery can safely supply enough energy for an additional load. It may be read 300ms after the SMBus Host sets the AtRate value. If read before this delay, the command is No Acknowledged and the error code in BatteryStatus is set to "not ready." Refer to AtRate().

SMBus Protocol: Read Word

Output:

Boolean—indicates if the battery can supply the *additional* energy requested.

16/38

Units: Boolean

Range: TRUE, FALSE

Granularity: not applicable

Accuracy: not applicable

Temperature() (0x08); [0x08]

Description:
Returns the temperature (K) measured by the bq2060.

Purpose:
The Temperature() function provides accurate cell temperatures for use by battery chargers and thermal management systems. A battery charger can use the temperature as a safety check. Thermal management systems may use the temperature because the battery is one of the largest thermal sources in a system.

SMBus Protocol: Read Word

Output:

Unsigned integer—cell temperature in tenth degree Kelvin increments.

Units: 0.1°K

Range: 0 to +6553.5°K {real range}

Granularity: 0.1°K

Accuracy: ±2°K

Voltage() (0x09); [0x09]

Description:
Returns the cell-pack voltage (mV).

Purpose:
The Voltage() function provides power management systems with an accurate battery terminal voltage. Power management systems can use this voltage, along with battery current information, to characterize devices they control. This ability helps enable intelligent, adaptive power management systems.

SMBus Protocol: Read Word

Output:

Unsigned integer—battery terminal voltage in mv.

Units: mV

Range: 0 to 20,000 mV

Granularity: 1mV

Accuracy: 10mV

Current() (0x0a); [0x0a]

Description:
Returns the current being supplied (or accepted) through the battery's terminals (mA).

Purpose:
The Current() function provides a snapshot for the power management system of the current flowing into or out of the battery. This information is of particular use in power management systems because they can characterize individual devices and "tune" their operation to actual system power behavior.

SMBus Protocol: Read Word

Output:

Signed integer—charge/discharge rate in mA increments—positive for charge, negative for discharge.

Units: mA

Range: (±300mV/Rs) mA

Granularity: 1mA

Accuracy: ±610μV/Rs

AverageCurrent() (0x0b); [0x0b]

Description:
Returns an value that approximates a one-minute rolling average of the current being supplied (or accepted) through the battery's terminals (mA). The AverageCurrent() function returns meaningful values during the battery's first minute of operation.

Purpose:
The AverageCurrent() function provides the average current flowing into or out of the battery for the power management system.

SMBus Protocol: Read Word

Output:

Signed integer—charge/discharge rate in ma increments—positive for charge, negative for discharge.

Units: mA

Range: 0 to 32,767 ma for charge or 0 to -32,768 mA for discharge

Granularity: 1mA

Accuracy: ±610μV/Rs

MaxError() (0x0c); [0x0c]

Description:
Returns the expected margin of error (%) in the state of charge calculation. For example, when MaxError() re-

turns 10% and RelativeStateOfCharge() returns 50%, the Relative StateOfCharge() is more likely between 50 and 60%. The MaxError() of bq2060 increases between "learn" cycles. When a "learn" cycle is performed, MaxError() is set to 2%.

If voltage-based corrections are applied to the coulomb counter, MaxError() is set to 15%.

Purpose:
The MaxError() function has real value in two ways: first, to give the user a confidence level about the state of charge and second, to give the power management system information about how aggressive it should be, particularly as the battery nears the end of its life.

SMBus Protocol: Read Word

Output:

Unsigned integer—percent uncertainty for selected information.

Units: %

Range: 2 to 100%

Granularity: 1%

Accuracy: not applicable

RelativeStateOfCharge() (0x0d); [0x0d]

Description:
Returns the predicted remaining battery capacity expressed as a percentage of FullChargeCapacity() (%).

Purpose:
The RelativeStateOfCharge() function is used to estimate the amount of charge remaining in the battery relative to the last "learned" capacity.

SMBus Protocol: Read Word

Output:

Unsigned integer—percent of remaining capacity.

Units: %

Range: 0 to 100%

Granularity: 1%

Accuracy: -0, +MaxError()

AbsoluteStateOfCharge()(0x0e); [0x0e]

Description:
Returns the predicted remaining battery capacity expressed as a percentage of DesignCapacity() (%). Note that AbsoluteStateOfCharge() can return values greater than 100%.

Purpose:
The AbsoluteStateOfCharge() function is used to estimate the amount of charge remaining in the battery relative to the nominal or DesignCapacity().

SMBus Protocol: Read Word

Output:

Unsigned integer—percent of remaining capacity.

Units: %

Range: 0 to 100+%

Granularity: 1%

Accuracy: -0, +MaxError()

RemainingCapacity() (0x0f); [0x0f]

Description:
Returns the predicted charge or energy remaining in the battery. The RemainingCapacity() value is expressed in either charge (mAh at a C/5 discharge rate) or energy (10mWh at a P/5 discharge rate) depending on the setting of the BatteryMode()'s CAPACITY_MODE bit.

Purpose:
The RemainingCapacity() function returns the battery's remaining capacity. This information is a numeric indication of remaining charge or energy given by the Absolute or Relative StateOfCharge() functions and may be in a better form for use by power management systems.

SMBus Protocol: Read Word

Output:

Unsigned integer—remaining charge in mAh or 10mWh.

Battery Mode		
	CAPACITY_MODE bit = 0	CAPACITY_MODE bit = 1
Units	mAh	10m
Range	0–65,535mAh	0–65,535 10mWh
Granularity	mAh	10mWh
Accuracy	-0, +MaxError() * FullChargeCapacity()	

FullChargeCapacity() (0x10); [0x10]

Description:
Returns the predicted pack capacity when it is fully charged. The FullChargeCapacity() value is expressed in either current (mAh at a C/5 discharge rate) or power (10mWh at a P/5 discharge rate) depending on the setting of the BatteryMode()'s CAPACITY_MODE bit.

Purpose:
The FullChargeCapacity() function provides the user with a means of understanding the "tank size" of their battery. This information, along with information about the original capacity of the battery, can be presented to the user as an indication of battery wear.

SMBus Protocol: Read Word

Output:

Unsigned integer—estimated full charge capacity in mAh or 10mWh.

Battery Mode		
	CAPACITY_MODE bit = 0	CAPACITY_MODE bit = 1
Units	mAh	10mWh
Range	0–65,535mAh	0–65,535 10mWh
Granularity	mAh	10mWh
Accuracy	-0, +MaxError() * FullChargeCapacity()	

RunTimeToEmpty() (0x11); [0x11]

Description:
Returns the predicted remaining battery life at the present rate of discharge (minutes). The RunTimeToEmpty() value is calculated based on either current or power depending on the setting of the BatteryMode()'s CAPACITY_MODE bit. This is an important distinction because use of the wrong calculation mode may result in inaccurate return values.

Purpose:
The RunTimeToEmpty() can be used by the power management system to get information about the relative gain or loss in remaining battery life in response to a change in power policy. This information is NOT the same as the AverageTimeToEmpty(), which is not suitable to determine the effects that result from a change in power policy.

SMBus Protocol: Read Word

Output:

Unsigned integer—minutes of operation left.

Units: minutes

Range: 0 to 65,534 min

Granularity: 2 min or better

Accuracy: -0, +MaxError() * FullChargeCapacity() / Current()

Invalid Data Indication: 65,535 indicates battery is not being discharged.

AverageTimeToEmpty() (0x12); [0x12]

Description: Returns a one-minute rolling average of the predicted remaining battery life (minutes). The AverageTimeToEmpty() value is calculated based on either current or power depending on the setting of the BatteryMode()'s CAPACITY_MODE bit. This is an important distinction because use of the wrong calculation mode may result in inaccurate return values.

Purpose:
The AverageTimeToEmpty() displays state-of-charge information in a more useful way. By averaging the instantaneous estimations, the remaining time does not appear to "jump" around.

SMBus Protocol: Read Word

Output:

Unsigned integer — minutes of operation left.

Units: minutes

Range: 0 to 65,534 min

Granularity: 2 min or better

Accuracy: -0, +MaxError() * FullChargeCapacity() / AverageCurrent()

Invalid Data Indication: 65,535 indicates battery is not being discharged.

AverageTimeToFull() (0x13); [0x13]

Description: Returns a one minute rolling average of the predicted remaining time until the Smart Battery reaches full charge (minutes).

Purpose: The AverageTimeToFull() function can be used by the SMBus Host's power management system to aid in its policy. It may also be used to find out how long the system must be left on to achieve full charge.

SMBus Protocol: Read Word

Output:

Unsigned integer —remaining time in minutes.

Units: minutes

Range: 0 to 65,534 minutes

Granularity: 2 minutes or better

Accuracy: MaxError() * FullChargeCapacity() / AverageCurrent()

Invalid Data Indication: 65,535 indicates the battery is not being charged.

ChargingCurrent() (0x14); [0x14]

Description: Returns the desired charging rate in mA.

Purpose: The ChargingCurrent() function sets the maximum charge current of the battery. The ChargingCurrent() value should be used in combination with the ChargingVoltage() value to set the charger's operating point. Together, these functions permit the bq2060 to dynamically control the charging profile (current/voltage) of the battery. The bq2060 can effectively turn off a charger by returning a value of 0 for this function. The charger may be operated as a constant voltage source above its maximum regulated current range by returning a ChargingCurrent() value of 65,535.

SMBus Protocol: Read Word

Output:

Unsigned integer—maximum charger output current in ma.

Units: ma

Range: 0 to 61,456 ma

Granularity: 1mA

Accuracy: not applicable

Invalid Data Indication: 65,535 indicates that a charger should operate as a voltage source outside its maximum regulated current range.

ChargingVoltage() (0x15); [0x15]

Description: Returns the desired charging voltage in mV.

Purpose: The ChargingVoltage() function sets the maximum charge voltage of the battery. The ChargingVoltage() value should be used in combination with the ChargingCurrent() value to set the charger's operating point. Together, these functions permit the bq2060 to dynamically control the charging profile (current/voltage) of the battery. The charger may be operated as a constant current source above their maximum regulated voltage range by returning a ChargingVoltage() value of 65,535.

SMBus Protocol: Write Word

Output:

Unsigned integer—charger output voltage in mV.

Units: mV

Range: 0 to 61,456 mV

Granularity: 1mV

Accuracy: not applicable

Invalid Data Indication: 65,535 indicates the charger should operate as a current source outside its maximum regulated voltage range.

BatteryStatus()(0x16); [0x16]

Description: Returns the Smart Battery's status word (flags). Some of the BatteryStatus() flags (REMAINING_CAPACITY_ALARM and REMAINING_TIME_ALARM) are calculated based on either current or power depending on the setting of the BatteryMode()'s CAPACITY_MODE bit. This is important because use of the wrong calculation mode may result in an inaccurate alarm.

Purpose: The BatteryStatus() function is used by the power management system to get alarm and status bits, as well as error codes from the bq2060. This is basically the same information broadcast to both the SMBus Host and the Smart Battery Charger by the AlarmWarning() function except that the AlarmWarning() function sets the Error Code bits all high before sending the data.

SMBus Protocol: Read Word

Output:

Unsigned integer—Status Register with alarm conditions bit mapped as follows:

Alarm Bits	
0x8000	OVER_CHARGED_ALARM
0x4000	TERMINATE_CHARGE_ALARM
0x2000	reserved
0x1000	OVER_TEMP_ALARM
0x0800	TERMINATE_DISCHARGE_ALARM
0x0400	reserved
0x0200	REMAINING_CAPACITY_ALARM
0x0100	REMAINING_TIME_ALARM
Status Bits	
0x0080	INITIALIZED
0x0040	DISCHARGING
0x0020	FULLY_CHARGED
0x0010	FULLY_DISCHARGED
Error Codes	
0x0007	Unknown Error
0x0006	BadSize
0x0005	Overflow/Underflow
0x0004	AccessDenied
0x0003	UnsupportedCommand
0x0002	ReservedCommand
0x0001	Busy
0x0000	OK

Alarm Bits

OVER_CHARGED_ALARM bit is set whenever the bq2060 detects that the battery is being charged beyond an end-of-charge indication. This bit will be cleared

when the bq2060 detects that the battery is no longer being charged.

TERMINATE_CHARGE_ALARM bit is set when the bq2060 detects that one or more of the battery's charging parameters are out of range (e.g. its voltage or current are too high). This bit will be cleared when the parameter falls back in into the allowable range. Failure to correct the problem may result in permanent damage to the battery.

OVER_TEMP_ALARM bit will be set when the bq2060 detects that the internal battery temperature is greater than allowed. This bit will be cleared when the internal temperature falls back into the acceptable range.

TERMINATE_DISCHARGE_ALARM bit is set when the bq2060 determines that the battery has supplied all the charge it can without being damaged (i.e., continued use will result in permanent capacity loss to the battery). This bit will be cleared when the battery reaches a state-of-charge sufficient for it to once again safely supply power.

REMAINING_CAPACITY_ALARM bit is set when the bq2060 detects that RemainingCapacity() is less than that set by the RemainingCapacityAlarm() function. This bit will be cleared when either the value set by the RemainingCapacityAlarm() function is lower than the RemainingCapacity() or when the RemainingCapacity() is increased by charging.

REMAINING_TIME_ALARM bit is set when the bq2060 detects that the estimated remaining time at the present discharge rate is less than that set by the RemainingTimeAlarm() function. This bit will be cleared when either the value set by the RemainingTimeAlarm() function is lower than the AverageTimeToEmpty() or when the AverageTimeToEmpty() is increased by charging.

Status Bits

INITIALIZED bit is set when the bq2060 is calibrated at time of manufacture. It will be cleared when the bq2060 detects that its calibration data has been lost or altered due to unknown causes.

DISCHARGING bit is set when the bq2060 determines that the battery is not being charged. This bit will be cleared when the bq2060 detects that the battery is being charged.

FULLY_CHARGED bit is set when the bq2060 determines that the battery has reached a charge termination point. This bit will be cleared when the battery may be charged again.

FULLY_DISCHARGED bit is set when the bq2060 determines that the battery has supplied all the charge it can without being damaged (that is, continued use will result in permanent capacity loss to the battery). This bit will be cleared when the RelativeStateOfCharge() is greater than or equal to 20%.

Error	Description
OK	The bq2060 processed the function code without detecting any errors.
Busy	The bq2060 is unable to process the function code at this time.
Reserved	The bq2060 detected an attempt to read or write to a function code reserved by this version of the specification. The 2060 detected an attempt to access an unsupported optional manufacturer function code.
Unsupported	The bq2060 does not support this function code which is defined in this version of the specification.
AccessDenied	The bq2060 detected an attempt to write to a read only function code.
Over/Underflow	The bq2060 detected a data overflow or underflow.
BadSize	The bq2060 detected an attempt to write to a function code with an incorrect data block.
UnknownError	The bq2060 detected an unidentifiable error.

CycleCount()(0x17); [0x17]

Description: Returns a number which represents the total charge removed from the pack. The mAh value of each count is determined by programming the *Cycle Count Threshold* value in EE 0x66–0x67. The bq2060 saves the cycle count value to EEPROM after an update to CycleCount().

Purpose: The CycleCount() function provides a means to determine their battery's wear. It may be used to give advanced warning that the battery is nearing its end of life.

SMBus Protocol: Read Word

Output:

Unsigned integer—count of total charge removed from the battery over its life.

Units: cycle

Range: 0 to 65,534 cycles 65,535 indicates battery has experienced 65,535 or more cycles.

Granularity: 1 cycle

Accuracy: absolute count

DesignCapacity() (0x18); [0x18]

Description: Returns the theoretical or nominal capacity of a new pack. The DesignCapacity() value is expressed in either current (mAh at a C/5 discharge rate) or power (10mWh at a P/5 discharge rate) depending on the setting of the BatteryMode()'s CAPACITY_MODE bit.

Purpose: The DesignCapacity() function is used by the SMBus Host's power management in conjunction with FullChargeCapacity() to determine battery wear. The power management system may present this information to the user and also adjust its power policy as a result.

SMBus Protocol: Read Word

Output:

Unsigned integer—battery capacity in mAh or 10mWh.

	Battery Mode	
	CAPACITY_MODE bit = 0	CAPACITY_MODE bit = 1
Units	mAh	10mWh
Range	0–65,535mAh	0–65,535 10mWh
Granularity	Not applicable	
Accuracy	Not applicable	

DesignVoltage() (0x19); [0x19]

Description: Returns the theoretical voltage of a new pack (mV).

Purpose: The DesignVoltage() function can be used to give additional information about a particular Smart Battery's expected terminal voltage.

SMBus Protocol: Read Word

Output:

Unsigned integer—the battery's designed terminal voltage in mV

Units: mV

Range: 0 to 65,535 mV

Granularity: not applicable

Accuracy: not applicable

SpecificationInfo() (0x1a); [0x1a]

Description: Returns the version number of the Smart Battery specification the battery pack supports, as well as voltage and current scaling information in a packed unsigned integer. Power scaling is the product of the voltage scaling times the current scaling. The SpecificationInfo is packed in the following fashion: (major version number * 0x10 + minor revision number) + (voltage scaling + current scaling * 0x10) * 0x100.

The bq2060 VScale (voltage scaling) and IPScale (current scaling) should always be set to zero.

Purpose: The SpecificationInfo() function is used by the SMBus Host's power management system to determine what information the Smart Battery can provide.

SMBus Protocol: Read Word

Output:

Unsigned integer—packed specification number and scaling information.

Field	Bits Used	Format	Allowable Values
Revision	0...3	4-bit binary value	0–15
Version	4...7	4-bit binary value	1–15
VScale	8...11	4-bit binary value	0 (multiplies voltage by 10^ VScale)
IPScale	12...15	4-bit binary value	0 (multiplies current by 10 ^ IPScale)

ManufactureDate() (0x1b); [0x1b]

Description: This function returns the date the cell pack was manufactured in a packed integer. The date is packed in the following fashion: (year-1980) * 512 + month * 32 + day.

Purpose: The ManufactureDate() provides the system with information that can be used to uniquely identify a particular battery pack when used in conjunction with SerialNumber().

SMBus Protocol: Read Word

Output:

Unsigned integer—packed date of manufacture.

Field	Bits Used	Format	Allowable Values
Day	0...4	5-bit binary value	0–31 (corresponds to date)
Month	5...8	4-bit binary value	1–12 (corresponds to month number)
Year	9...15	7-bit binary value	0–127 (corresponds to year biased by 1980)

SerialNumber() (0x1c); [0x1c]

Description: This function is used to return a serial number. This number, when combined with the ManufacturerName(), the DeviceName(), and the ManufactureDate(), uniquely identifies the battery (unsigned int).

Purpose: The SerialNumber() function is used to identify a particular battery. This may be important in systems that are powered by multiple batteries where the system can log information about each battery that it encounters.

SMBus Protocol: Read Word

Output:

Unsigned integer

ManufacturerName() (0x20); [0x20-0x25]

Description: This function returns a character array containing the battery's manufacturer's name. For example, "MyBattCo" would identify the Smart Battery's manufacturer as MyBattCo.

Purpose: The ManufacturerName() function returns the name of the Smart Battery's manufacturer. The manufacturer's name can be displayed by the SMBus Host's power management system display as both an identifier and as an advertisement for the manufacturer. The name is also useful as part of the information required to uniquely identify a battery.

SMBus Protocol: Read Block

Output:

String—character string with maximum length of 11 characters (11+length byte).

DeviceName() (0x21); [0x28-0x2b]

Description: This function returns a character string that contains the battery's name. For example, a DeviceName() of "BQ2060A" would indicate that the battery is a model BQ2060A.

Purpose: The DeviceName() function returns the battery's name for identification purposes.

SMBus Protocol: Read Block

Output:

String—character string with maximum length of 7 characters (7+length byte).

DeviceChemistry() (0x22); [0x30-0x32]

Description: This function returns a character string that contains the battery's chemistry. For example, if the DeviceChemistry() function returns "NiMH," the battery pack would contain nickel metal hydride cells.

Purpose: The DeviceChemistry() function gives cell chemistry information for use by charging systems. The bq2060 does not use DeviceChemisty() values for internal charge control or fuel gauging.

SMBus Protocol: Read Block

Output:

String—character string with maximum length of 5 characters (5+length byte).

Note: The following is a partial list of chemistries and their expected abbreviations. These abbreviations are NOT case sensitive.

Lead Acid	PbAc
Lithium Ion	LION
Nickel Cadmium	NiCd
Nickel Metal Hydride	NiMH
Nickel Zinc	NiZn
Rechargeable Alkaline-Manganese	RAM
Zinc Air	ZnAr

ManufacturerData() (0x23); [0x38–0x3a]

Description: This function allows access to the manufacturer data contained in the battery (data).

Purpose: The ManufacturerData() function may be used to access the manufacturer's data area. The data fields of this command are free locations and may include items such as: lot codes, number of deep cycles, discharge patterns, deepest discharge, etc.

SMBus Protocol: Read Block

Output:

Block data—data whose meaning is assigned by the manufacturer with maximum length of 5 characters (5+length byte).

Pack Status and Pack Configuration (0x2f); [0x2f]

This function returns the Pack Status and Pack Configuration registers. The Pack Status register contains a number of status bits relating to the bq2060 secondary protection of Li-Ion cells. The Pack Status register is the least significant byte of the word.

COK

b7	b6	b5	b4	b3	b2	b1	b0
-	-	-	-	COK	DOK	CVOV	CVUV

The COK bit indicates the status of the CFC pin of the bq2060.

0 CFC pin is low

1 CFC pin is high

DOK

The DOK bit indicates the status of the DFC pin of the bq2060

0 DFC pin is low

1 DFC pin is high

CVOV

The CVOV bit indicates if any individual cell exceeded the programmed high voltage limit. The bit applies to batteries of lithium chemistry only. The bit is not latched and merely reflects the present over voltage status.

0 All series cells are below the high voltage limit

1 A series cell is above the high voltage limit

CVUV

The CVUV bit indicates if any individual cell falls below the programmed low-voltage limit. The bit applies to batteries of lithium chemistry only. The bit is not latched and merely reflects the present over voltage status.

0 All series cells are above the low-voltage limit

1 A series cell is below the low voltage limit

The Pack Configuration register reflects how the bq2060 is configured as defined by the value programmed in *Pack Configuration* in EE 0x3f.

VCELL4–VCELL1 (0x3c–0x3f); [0x3c–0x3f]

These functions return the calculated voltages in mV at the $VCELL_4$ through $VCELL_1$ inputs.

EEPROM

General

The bq2060 accesses the external EEPROM during a full reset and when storing historical data. During an EEPROM access, the VOUT pin becomes active and the bq2060 uses the ESCL and ESDA pins to communicate with the EEPROM. The EEPROM stores basic configuration information for use by the bq2060. The EEPROM must be programmed correctly for proper bq2060 operation.

Memory Map

Table 8 shows the memory map for the EEPROM. It also contains example data for a 10 series NiMH battery pack with a 0.05Ω sense resistor.

EEPROM Programming

The following sections describes the function of each EEPROM location and how the data is to be stored.

Fundamental Parameters

Sense Resistor Value

Two factors are used to scale the current related measurements. The 16-bit *ADC Sense Resistor* value in EE 0x6c-0x6d scales Current() to mA. Adjusting *ADC Sense Resistor* from its nominal value provides a method to calibrate the current readings for system errors and the sense resistor value (Rs) . The nominal value is set by

$$ADC\ Sense\ Resistor = \frac{625}{(Rs)} \quad (3)$$

The 16-bit *VFC Sense Resistor* in EE 0x6e-0x6f scales each VFC interrupt to mAh. *VFC Sense Resistor* is based on the resistance of the series sense resistor. The following formula computes a nominal or starting value for *VFC Sense Resistor* from the sense resistor value.

$$VFC\ Sense\ Resistor = \frac{409.6}{Rs} \quad (4)$$

Sense resistor values are limited to the range of 0.00916 to 0.100Ω.

Digital Filter

The desired digital filter threshold, VDF (µV), is set by calculating the value stored in *Digital Filter* EE 0x63.

$$Digital\ Filter = \mathrm{Int}\left[\left\{\frac{1.125E\ -\ 02}{(VDF*5)}\right\} + 0.5\right] \quad (5)$$

Cell Characteristics

Battery Pack Capacity

Pack capacity is programmed in mAh units to *Design Capacity* in EE 0x10–0x11, *FCC* in EE 0x52–0x53, and *Pack Capacity* in EE 0x6a–0x6b. In mAh mode, the bq2060 copies *Design Capacity* to DesignCapacity(). In mWh mode, the bq2060 multiplies *Design Capacity* by *Design Voltage* EE 0x12–0x13 to calculate DesignCapacity() scaled to 10*mWh. *Design Capacity* is a static value that represents the nominal pack capacity.

The initial pack capacity is programmed in *FCC. FCC* is modified over the course of pack usage to reflect cell aging under the particular use conditions. The bq2060 updates *FCC* after a capacity learning cycle.

Table 8. EEPROM Memory Map

EEPROM Address		Name	Chemistry	NiMH Example	Data		Li-Ion Example	Data	
					MSB	LSB		MSB	LSB
0x00		*Block Length*	Li-Ion, Nickel	127	-	7f	127	-	7f
0x01		Reserved	-	0	-	00	0	-	00
0x02	0x03	*Remaining Time Alarm*	Li-Ion, Nickel	10 minutes	00	0a	10 minutes	00	0a
0x04	0x05	*Remaining Capacity Alarm*	Li-Ion, Nickel	350mAh	01	5e	400mAh	01	90
0x06		*Slave Mode*	Li-Ion, Nickel	0	-	00	0	-	00
0x07		Reserved	-	255	-	ff	255	-	ff
0x08		Reserved	-	0	-	00	0	-	00
0x09		Reserved	-	0	-	00	0	-	00
0x0a	0x0b	*Charging Voltage*	Li-Ion, Nickel	65535mV	ff	ff	12600mV	31	38
0x0c	0x0d	*Battery Status*	Li-Ion, Nickel	128	00	80	128	00	80
0x0e	0x0f	*Cycle Count*	Li-Ion, Nickel	0	00	00	0	00	00
0x10	0x11	*Design Capacity*	Li-Ion, Nickel	4000mAh	0f	a0	4050mAh	0f	d2
0x12	0x13	*Design Voltage*	Li-Ion, Nickel	12000mV	2e	e0	10800mV	2a	30
0x14	0x15	*Specification Information*	Li-Ion, Nickel	v1.1 = 33	00	21	v1.1 = 33	00	21
0x16	0x17	*Manufacture Date*	Li-Ion, Nickel	2/25/99=9817	26	59	2/25/99=9817	26	59
0x18	0x19	*Serial Number*	Li-Ion, Nickel	1	00	01	1	00	01
0x1a	0x1b	*Fast-Charging Current*	Li-Ion, Nickel	4000mA	0f	a0	3000mA	0b	b8
0x1c	0x1d	*Maintenance Charging Current*	Li-Ion, Nickel	200mA	00	c8	0mA	00	00
0x1e	0x1f	*Pre-Charge Current*	Li-Ion, Nickel	800mA	03	20	100mA	00	64
0x20		*Manufacturer Name Length*	Li-Ion, Nickel	9	-	09	9	-	09
0x21		*Character 1*	Li-Ion, Nickel	B	-	42	B	-	42
0x22		*Character 2*	Li-Ion, Nickel	E	-	45	E	-	45
0x23		*Character 3*	Li-Ion, Nickel	N	-	4e	N	-	4e
0x24		*Character 4*	Li-Ion, Nickel	C	-	43	C	-	43
0x25		*Character 5*	Li-Ion, Nickel	H	-	48	H	-	48
0x26		*Character 6*	Li-Ion, Nickel	M	-	4d	M	-	4d
0x27		*Character 7*	Li-Ion, Nickel	A	-	41	A	-	41
0x28		*Character 8*	Li-Ion, Nickel	R	-	52	R	-	52
0x29		*Character 9*	Li-Ion, Nickel	Q	-	51	Q	-	51
0x2a		*Character 10*	Li-Ion, Nickel	0	-	00	0	-	00
0x2b		*Character 11*	Li-Ion, Nickel	0	-	00	0	-	00
0x2c		*Current Taper Threshold*	Li-Ion	0	-	00	200mA	-	08
0x2d		*EDV0F*	Li-Ion	0	-	00	51	-	33
0x2e	0x2f	*Maximum Overcharge*	Li-Ion, Nickel	200mAh	ff	38	256mAh	ff	00
0x30		*Device Name Length*	Li-Ion, Nickel	7	-	07	7	-	07
0x31		*Character 1*	Li-Ion, Nickel	B	-	42	B	-	42

Note: Reserved locations must be set as shown. Locations marked with an * are calibration values that can be adjusted for maximum accuracy. For these locations the table shows the appropriate default or initial setting.

Table 8. EEPROM Memory Map (Continued)

EEPROM Address		Name	Chemistry	NiMH Example	Data		Li-Ion Example	Data	
					MSB	LSB		MSB	LSB
0x32		*Character 2*	Li-Ion, Nickel	Q	-	51	Q	-	51
0x33		*Character 3*	Li-Ion, Nickel	2	-	32	2	-	32
0x34		*Character 4*	Li-Ion, Nickel	0	-	30	0	-	30
0x35		*Character 5*	Li-Ion, Nickel	6	-	36	6	-	36
0x36		*Character 6*	Li-Ion, Nickel	0	-	30	0	-	30
0x37		*Character 7*	Li-Ion, Nickel	A	-	41	A	-	41
0x38	0x39	*Overload Current*	Li-Ion, Nickel	6000mA	e8	90	6000mA	e8	90
0x3a		*Current Taper Cell Voltage*	Li-Ion	0	-	00	4150mV	-	89
0x3b		*Overvoltage Margin*	Li-Ion, Nickel	0	-	00	800mV	-	80
0x3c		*Overcurrent Margin*	Li-Ion, Nickel	200mA	-	0c	512mA	-	20
0x3d		*Fast Charge Termination %*	Li-Ion, Nickel	96%	-	a0	100%	-	64
0x3e		Reserved	-	0	-	00	0	-	00
0x3f		*Pack Configuration*	Li-Ion, Nickel	235	-	eb	230	-	e6
0x40		*Device Chemistry Length*	Li-Ion, Nickel	4	-	04	4	-	04
0x41		*Character 1*	Li-Ion, Nickel	N	-	4e	L	-	4c
0x42		*Character 2*	Li-Ion, Nickel	I	-	49	I	-	49
0x43		*Character 3*	Li-Ion, Nickel	M	-	4d	O	-	4f
0x44		*Character 4*	Li-Ion, Nickel	H	-	48	N	-	4e
0x45		*Character 5*	Li-Ion, Nickel	0	-	00	0	-	00
0x46		*Near Full %*	Li-Ion, Nickel	96%	-	f6	99.6%	-	ff
0x47		*Temperature Offset**	Li-Ion, Nickel	0	-	00	0	-	00
0x48	0x49	*ADC Full Scale Voltage**	Li-Ion, Nickel	20000	4e	20	20000	4e	20
0x4a	0x4b	*EDV0*	Li-Ion, Nickel	9500mV	da	e4	2850mV	f4	de
0x4c	0x4d	*EDV1*	Li-Ion, Nickel	10500mV	d6	fc	3250mV	f3	4e
0x4e	0x4f	*EDV2*	Li-Ion, Nickel	11000mV	d5	08	3375mV	f2	d1
0x50		Reserved	-	0	-	00	0	-	00
0x51		*Cell 4 Calibration Factor**	Li-Ion	0	-	00	0	-	00
		Efficiency Reduction Rate	Nickel	1%	-	50	0	-	00
0x52	0x53	*FCC*	Li-Ion, Nickel	4000mAh	0f	a0	4050mAh	0f	d2
0x54		*EDV1F*	Li-Ion	0	-	00	18	-	12
0x55		*FET Control*	Li-Ion	0	-	00	255	-	ff
0x56		*Cell 2 Calibration Factor**	Li-Ion	0	-	00	0	-	00
		Efficiency Temperature Compensation	Nickel	1%	-	80	0	-	00
0x57		*Cell 3 Calibration Factor **	Li-Ion	0	-	00	0	-	00
		Efficiency Drop Off Percentage	Nickel	96%	-	a0	0	-	00
0x58		Reserved	-	0	-	00	0	-	00
0x59		Reserved	-	0	-	00	0	-	00

Note: Reserved locations must be set as shown. Locations marked with an * are calibration values that can be adjusted for maximum accuracy. For these locations the table shows the appropriate default or initial setting.

26/38

Table 8. EEPROM Memory Map (Continued)

EEPROM Address		Description	Chemistry	NiMH Example	Data		Li-Ion Example	Data	
					MSB	LSB		MSB	LSB
0x5a		*Internal Temperature Gain Factor**	Li-Ion, Nickel	0	-	00	0	-	00
0x5b		Reserved	-	0	-	00	0	-	00
0x5c	0x5d	*VFC Offset**	Li-Ion, Nickel	0	00	00	0	00	00
0x5e		*VFC Offset**	Li-Ion, Nickel	0	-	00	0	-	00
0x5f		Reserved	-	0	-	00	0	-	00
0x60		*MaxT DeltaT*	Li-Ion, Nickel	50C, 3.0	-	c7	50C, 4.6	-	cf
0x61		EDV2F	Li-Ion	0	-	00	128	-	80
		DeltaT Time	Nickel	180s	-	f7	0	-	00
0x62		*DeltaT Holdoff Time*	Nickel	240s	-	f4	0	-	ff
0x63		*Digital Filter*	Li-Ion, Nickel	100µV	-	17	100µV	-	17
0x64		*Self-Discharge Rate*	Li-Ion, Nickel	1%	-	cb	0.21%	-	04
0x65		*High Charge Efficiency*	Li-Ion, Nickel	95%	-	cd	100%	-	ff
0x66	0x67	*Cycle Count Threshold*	Li-Ion, Nickel	500mAh	fe	0c	3240mAh	f3	58
0x68		*Battery Low %*	Li-Ion, Nickel	12%	-	1e	7%	-	12
0x69		*Fully Charged Clear %*	Li-Ion, Nickel	90%	-	a6	95%	-	5f
0x6a	0x6b	*Pack Capacity*	Li-Ion, Nickel	4000mAh	0f	a0	4050mAh	0f	d2
0x6c	0x6d	*ADC Sense Resistor**	Li-Ion, Nickel	0.05Ω	30	d4	0.05Ω	30	d4
0x6e	0x6f	*VFC Sense Resistor**	Li-Ion, Nickel	0.05Ω	20	00	0.05Ω	20	00
0x70	0x71	*VOC 25%*	Li-Ion, Nickel	11500mV	d3	14	10550mV	d6	ca
0x72	0x73	*VOC 50%*	Li-Ion, Nickel	12500mV	cf	2c	10750mV	d6	02
0x74	0x75	*VOC 75%*	Li-Ion, Nickel	13500mV	cb	44	11200mV	d4	40
0x76		Reserved	-	0	-	00	0	-	00
0x77		Reserved	-	0	-	00	0	-	00
0x78		Reserved	-	0	-	00	0	-	00
0x79		Reserved	-	0	-	00	0	-	00
0x7a		Reserved	-	0	-	00	0	-	00
0x7b		Reserved	-	0	-	00	0	-	00
0x7c		Reserved	-	0	-	00	0	-	00
0x7d		Reserved	-	0	-	00	0	-	00
0x7e		*ADC Current Offset**	Li-Ion, Nickel	0	-	00	0	-	00
0x7f		*Check Byte 1*	Li-Ion, Nickel	165	-	a5	165	-	a5

Note: Reserved locations must be set as shown. Locations marked with an * are calibration values that can be adjusted for maximum accuracy. For these locations the table shows the appropriate default or initial setting.

EDV Thresholds and Near Full Percentage

The bq2060 uses three pack voltage thresholds to apply voltage based corrections to RM, and to provide voltage based warnings of low battery capacity. EDV0, EDV1, and EDV2, are stored in 2's complement of the desired voltage (mV) in the locations *EDV0* in EE 0x4a-0x4b, *EDV1* in EE 0x4c-0x4d, and *EDV2* in EE 0x4e-0x4f, respectively. For capacity correction at EDV2, *Battery Low %* EE 0x68 can be set at a desired state-of-charge, STATEOFCHARGE%, in the range of 5 to 20%. Typical values for STATEOFCHARGE% are 7–12% representing 7 –12% capacity.

$$\textit{Battery Low \%} = \text{STATEOFCHARGE\%} * 2.56 \quad (6)$$

The bq2060 updates FCC if a qualified discharge occurs from a near full threshold to EDV2. The near full threshold is programmed in *Near Full %* in EE 0x46.

$$\textit{Near Full \%} = \text{STATEOFCHARGE\%} * 2.56 \quad (7)$$

EDV Discharge Rate and Temperature Compenstaion

The bq2060 uses configuration parameters *EDV0F* in EE 0x2d, *EDV1F* in EE 0x54, and *EDV2F* in EE 0x61 to set the compensations for the three thresholds according to the following equations.

ΔEDV represents the shift in the end-of-discharge threshold levels for a change in temperature or rate. Setting *EDV0F*, *EDV1F*, and *EDV2F* to 0 disables compensation to the thresholds.

$$\textit{EDV0F} = \text{Int}[1000 * X_1 * 25.6] \quad (8)$$

where

$$0 \le X_1 \le 0.099$$

$$X_1 = \frac{\Delta EDV}{\Delta T} \text{ for } T \ge 15°C$$

and

$$\textit{EDV1F} = \text{Int}\left[\frac{1000 * X_2 * 256}{DC}\right] \quad (9)$$

where

$$0 \le \frac{X_2}{DC} \le 0.996$$

$$X_2 = \frac{\Delta EDV}{\Delta R} \text{ for } R \ge 0.5C \text{ and } DC = \text{DesignCapacity()}$$

and

$$\textit{EDV2F} = \text{Int}[12800 * X_3] \quad (10)$$

where

$$0 \le X_3 \le 0.199$$

$$X_3 = \frac{\Delta EDV}{\Delta T} \text{ for } T < 15°C$$

The bq2060 applies the EDV compensation only when the CHEM bit is set in Pack Configuration denoting a Li-Ion pack.

Overload Current Threshold

The *Overload Current* threshold is a 16-bit value stored in EE 0x38-0x39. It is stored in 2's complement form using mA units.

Mid Range Capacity Corrections

Three voltage-based thresholds, *VOC25* EE 0x70-0x71, *VOC50* EE 0x72-0x73, and *VOC75* EE 0x74-0x75, are used to test the accuracy of the RM based on open-circuit pack voltages. These thresholds are stored in the EEPROM in 2's complement of voltage in mV. The values represent the open-circuit battery voltage at which the battery capacity should correspond to the associated state of charge for each threshold.

Threshold	Associated State of Charge
VOC25	25%
VOC50	50%
VOC75	75%

Self-Discharge Rate

The nominal self-discharge rate, %PERDAY, is programmed in an 8-bit value *Self-Discharge Rate* EE0x64 by the following relation:

$$\textit{Self - Discharge Rate} = 2\text{'s}\left[\text{Int}\left\{\left(\frac{53}{\%\text{PERDAY}}\right) + 0.5\right\}\right] \quad (11)$$

Charge Efficiency

The bq2060 uses four charge efficiency factors to compensate for charge acceptance. These factors are coded in *High-Charge Efficiency*, *Efficiency Reduction Rate*, *Efficiency Drop Off Percentage*, and *Efficiency Temperature Compensation*.

The bq2060 applies the efficiency factor, EFF%, when RelativeStateofCharge() is less than the value coded in *Efficiency Drop Off Percentage* EE 0x57. When RelativeStateOfCharge() is greater than or equal to the value coded in *Efficiency Drop Off Percentage*, EFF% and ERR% determine the charge efficiency rate. ERR% defines the percent efficiency reduction per percentage point of RelativeStateOfCharge() over *Efficiency Drop Off Percentage*. EFF% is encoded in *High Charge Efficiency* EE 0x65 according to the following equation

$$\textit{High Charge Efficiency} = 10 * (\text{EFF\%} - 74.5) \quad (12)$$

where

$$74.5 \le \text{EFF\%} \le 100.$$

ERR% is encoded in *Efficiency Reduction Rate* EE 0x51 according to the following equation

$$\textit{Efficiency Reduction Rate} = \frac{\text{ERR\%}}{0.0125} \quad (13)$$

where

$$0 \le \text{ERR\%} \le 3.19.$$

The *Efficiency Drop Off* Percentage is stored in 2's complement of percent.

The bq2060 also adjusts the efficiency factors for temperature. TEFF% defines the percent efficiency reduction per degree C over 25°C. TEFF% is encoded in *Efficiency Temperature Compensation* EE 0x56 according to the following equation

$$\textit{Efficiency Temperature Compensation} = \frac{\text{TEFF\%} * 1.6}{0.0125} \quad (14)$$

where

$$0 \le \text{TEFF\%} \le 1.99.$$

The bq2060 applies all four charge-compensation factors when the CHEM bit in Pack Configuration is not set denoting a nickel pack. If CHEM is set denoting a Li-Ion pack, the bq2060 applies only the value coded in *High Charge Efficiency* and makes no other adjustments for charge acceptance.

Charge Limits and Termination Techniques

Charging Voltage

The 16-bit value, *Charging Voltage* EE 0x0a-0x0b, programs the ChargingVoltage() value broadcast to a Smart Charger. It is also sets the base value for determining overvoltage conditions during charging and voltage compliance during a constant-voltage charging methodology. It is stored in mV.

Overvoltage

The 8-bit value, *Overvoltage Margin* EE 0x3b, sets the limit over ChargingVoltage() that is to be considered as an overvoltage charge suspension condition. The voltage in mV above the ChargingVoltage(), VOVM, that should trigger a charge suspend is encoded in *Overvoltage Margin* as follows

$$\textit{Overvoltage Margin} = \frac{[\text{VOVM}]}{16} \quad (15)$$

VOVM is between 0 and 4080mV.

Charging Current

ChargingCurrent() values are either broadcast to a Level 2 Smart Battery Charger or read from the bq2060 by a Level 3 Smart Battery Charger. The bq2060 sets the value of ChargingCurrent(), depending on the charge requirements and charge conditions of the pack.

When fast charge is allowed, the bq2060 sets ChargingCurrent() to the rate programmed in *Fast Charging Current* EE 0x1a-0x1b.

When fast charge terminates, the bq2060 sets ChargingCurrent() to zero and then to the *Maintenance Charging Current* EE0x1c-0x1d when the termination condition ceases.

When Voltage() is less than EDV0, the bq2060 sets ChargingCurrent() to *Pre-charge Current* EE 0x1e-0x1f. Typically this rate is larger than the maintenance rate to charge a deeply depleted pack up to the point where it may be fast charged.

Fast Charging Current, *Maintenance Charging Current*, and *Pre-Charge Current* are stored in mA.

Charge Suspension

During charge, the bq2060 compares the current to the ChargingCurrent() plus the value IOIM. If the pack is charged at a current above the ChargingCurrent() plus IOIM, the bq2060 sets ChargingCurrent() set to zero to stop charging. IOIM is programmed in the EEPROM value, *Overcurrent Margin*, encoded as:

$$\textit{Overcurrent Margin} = \frac{\text{IOIM}}{16} \quad (16)$$

Overcurrent Margin EE 0x3c may be used to program IOIM values of 0 to 4080mA in 16mA steps.

The desired temperature threshold for charge suspension, MAXTEMP, may be programmed between 45°C and 69°C in 1.6°C steps. *MaxT* EE 0x60 is stored in a 4-bit value as shown:

$$\textit{MaxT} = \text{Int}\left[\frac{69 - \text{MAXTEMP}}{1.6} + 0.5\right] \quad (17)$$

The bq2060 suspends fast charge when fast charge continues past full by the amount programmed in *Maximum Overcharge* EE 0x2e-0x2f. *Maximum Overcharge* is programmed in 2's complement form of charge in mAh.

FULLY_CHARGED Bit Clear Threshold

The bq2060 clears the FULLY_CHARGED bit in BatteryStatus() when RelativeStateOfCharge() reaches the value, *Fully Charged Clear %* EE 0x69. *Fully Charged Clear %* is an 8-bit value and is stored as a 2's complement of percent.

Fast Charge Termination Percentage

The bq2060 sets RM to a percentage of FCC upon charge termination if the CSYNC bit is set in the Pack Configuration register. The percentage of FCC is stored in *Fast Charge Termination %* in EE 0x3d. The value is stored in 2's complement of percent.

Cycle Count Threshold

Cycle Count Threshold 0x66–0x67 sets the number of mAh that must be removed from the battery to increment CycleCount(). Cycle Count Threshold is a 16-bit value stored in 2's complement of charge in mAh.

ΔT/Δt Rate and Hold-off Programming

The ΔT portion of the ΔT/Δt rate is programmed in *DeltaT*, the low nibble of *MaxT DeltaT* EE 0x60. The Δt portion is programmed in *DeltaT Time* EE 0x61.

$$\Delta T/\Delta t = \frac{[DeltaT * 2 + 16]}{[2s(DeltaT\ Time) * 3.33]} \quad (18)$$

DeltaT	ΔT (°C)	*DeltaT Time*	Δt (s)
0	1.6	10	320
1	1.8	f1	300
2	2.0	f2	280
3	2.2	f3	260
4	2.4	f4	240
5	2.6	f5	220
6	2.8	f6	200
7	3.0	f7	180
8	3.2	f8	160
9	3.4	f9	140
a	3.6	fa	120
b	3.8	fb	100
c	4.0	fc	80
d	4.2	fd	60
e	4.4	fe	40
f	4.6	ff	20

ΔT/Δt Hold-off Timer Programming

The hold-off timer is programmed in the lower nibble of *DeltaT Holdoff Time* EE 0x62. The hold-off time is 20sec times the 2's complement of the *DeltaT Holdoff Time* value.

DeltaT Hold-off Time	Hold-off Time (s)	*DeltaT Hold-off Time*	Hold-off Time (s)
f0	320	f8	160
f1	300	f9	140
f2	280	fa	120
f3	260	fb	100
f4	240	fc	80
f5	220	fd	60
f6	200	fe	40
f7	180	ff	20

Current Taper Termination Characteristics

Two factors in the EEPROM set the current taper termination for Li-Ion battery packs. The two coded locations are *Current Taper Cell Voltage* EE 0x3a. Current taper termination occurs during charging when the highest cell voltage in the pack is greater than the voltage CELLV (mV) and the charging current is below the threshold coded in *Current Taper Threshold* EE 0x2c for at least 40s.

$$Current\ Taper\ Cell\ Voltage = \frac{CELLV\ -\ 3600}{4} \quad (19)$$

where

$$3600 \le CELLV \le 4620mV$$

$$Current\ Taper\ Threshold = Int\left[\left(\frac{Rs * i}{22.50}\right) * 20\right]$$

where i = the desired current termination threshold in mA and R_S = VFC sense resistor in ohms.

Pack Options

Pack Configuration

Pack Configuration EE 0x3f contains bit-programmable features.

b7	b6	b5	b4	b3	b2	b1	b0
DMODE	SEAL	CSYNC	INTEMP	VCOR	CHEM	LCC 1	LCC 0

DMODE

The DMODE bit determines whether the LED outputs will indicate AbsoluteStateOfCharge() or RelativeStateOfCharge()

0 LEDs reflect AbsoluteStateOfCharge()

1 LEDs reflect RelativeStateOfCharge()

SEAL

The SEAL bit determines the SMBus access state of the bq2060 on reset

0 SMBus commands (0x00–0xff) are accessible for both read and write.

1 SMBus read access is limited to commands (0x00–0x1c), (0x20–0x23), (0x2f), (0x3c–0x3f) and SMBus write access is limited to commands (0x00–0x04).

CSYNC

In usual operation of the bq2060, the CSYNC bit is set so that the coulomb counter is adjusted when a fast charge is detected. In some applications, especially those where an externally controlled charger is used, it may be desirable NOT to adjust the coulomb counter. In these cases the CSYNC bit should be cleared.

0 The bq2060 does not alter RM at the time of a valid charge termination

1 The bq2060 sets update RM with a programmed percentage of FCC.

INTEMP

The INTEMP bit determines whether the bq2060 uses its internal temperature sensor or an external temperature sensor connected to TS.

0 The bq2060 uses the external thermistor

1 The bq2060 uses its internal temperature sensor

The recommended mode of operation is to use a thermistor and set INTEMP = 0.

VCOR

The VCOR bit enables the mid range voltage correction algorithm. When set, the bq2060 compares the pack voltage to RM and may adjust RM according to the values programmed in *VOC25*, *VOC50*, and *VOC75*.

0 Mid-range corrections disabled

1 Mid-range corrections enabled

CHEM

The CHEM bit configures the bq2060 for nickel packs (NiCD or NiMH) or Li-Ion packs. When set the bq2060 employs the configuration parameters in EEPROM designated for Li-Ion. When not set, the bq2060 employs the configuration parameters designated for Nickel.

0 The bq2060 uses Nickel configuration parameters

1 The bq2060 uses Li-Ion configuration parameters

LCC0 and LCC1

The LCC0 and LCC1 bits configure the cell voltage inputs ($VCELL_{1-4}$).

No. of Series Cells	LCC1 LCC0	Cell Voltage Inputs
1	00	VCELL1 = Cell 1
2	01	VCELL1 = Cell 1 VCELL2 = Cell 2
3	10	VCELL1 = Cell 1 VCELL2 = Cell 2 VCELL3 = Cell 3
4	11	VCELL1 = Cell 1 VCELL2 = Cell 2 VCELL3 = Cell 3 VCELL4 = Cell 4

For Li-Ion packs, LCC0 and LCC1 define the number of series elements and their voltage measurement inputs. In each case, the bq2060 uses the highest numbered cell voltage input to measure the pack voltage measurement as returned with Voltage(). For nickel chemistries, LCC0 and LCC1 define the pack voltage input. For nickel, the recommended setting is 11 to designate VCELL4 as the pack voltage input.

Remaining Time and Capacity Alarms

Remaining Time Alarm in EE 0x02–0x03 and *Remaining Capacity Alarm* in 0x04–0x05set the alarm thresholds used in the SMBus command codes 0x01 and 0x02, respectively. *Remaining Time Alarm* is stored in minutes and *Remaining Capacity Alarm* in mAh.

Secondary Protection Limits for Li-Ion

Undervoltage and overvoltage thresholds may be programmed in the byte value *FET Control* EE 0x55 to set a secondary level of protection for Li-Ion cells. The bq2060 checks individual cell voltages for undervoltage and overvoltage conditions. The bq2060 displays the results in the Pack Status register and controls the state of the FET control outputs CFC and DFC. If any cell voltage is less than the VUV threshold, the bq2060 sets the CVUV bit in Pack Status and pulls the DFC pin to a logic low. If any cell voltage is greater than the VOV

threshold, the bq2060 sets the CVOV bit in Pack Status and pulls the CFC pin to a logic low.

VUV = 2048 + (*FET Control* AND 0xf0) * 4 (20)

VOV = 4096 + (*FET Control* AND 0x0f) * 32

FET Control (lower nibble)	VUV (mV)	*FET Control* (upper nibble)	VOV (mV)
0	2048	0	4096
1	2112	1	4128
2	2176	2	4160
3	2240	3	4192
4	2304	4	4224
5	2368	5	4256
6	2432	6	4288
7	2496	7	4320
8	2560	8	4352
9	2624	9	4384
a	2688	a	4416
b	2752	b	4448
c	2816	c	4480
d	2880	d	4512
e	2944	e	4544
f	3008	f	4576

Battery Status and Cycle Count Initialization

Battery Status EE 0x0c–0x0d stores the default value for the BatteryStatus() function. It should be programmed to 0x0080. *Cycle Count* EE 0x0e–0x0d stores the initial value for the CycleCount() function. It should be programmed to 0x0000.

Measurement Calibration

ADC

The reported voltage measurements, Voltage() and $VCELL_{1-4}$, may be calibrated by adjusting the 16-bit factor in EEPROM. The bq2060 uses these parameters to correct for variances in the ADC gain and the internal voltage reference. For nickel chemistries or Li-Ion without individual cell measurements, the bq2060 calibrates $VCELL_4$ with the 16-bit ADC Full Scale Voltage parameter in EE 0x48–0x49.

The nominal setting for *ADC Full Scale Voltage* is 20,000 for a 16:1 divider on $VCELL_4$. A two or three point curve fit should be used to find the optimum value for *ADC Full Scale Voltage* using the relation.

$$VCELL_4 = \frac{[\text{ADC Reading} * \textit{ADC Full Scale Voltage} * 2]}{65535} \quad (21)$$

For Li-Ion with individual cell measurements, the bq2060 uses three additional factors to calibrate the $VCELL_{1-4}$ inputs: *Cell 2 Calibration Factor* in EE 0x56, *Cell 3 Calibration Factor* in EE 0x57, and Cell 4 Calibration Factor in EE 0x51. To calibrate $VCELL_1$, the bq2060 uses the factor stored in *ADC Full Scale Voltage* according to the equation

$$VCELL_1 = \frac{[\text{ADC Reading} * \textit{ADC Full Scale Voltage}]}{65535} \quad (22)$$

To calibrate $VCELL_2$, $VCELL_3$, and $VCELL_4$, the bq2060 uses the additional factors *Cell 2 Calibration Factor*, *Cell 3 Calibration Factor*, and *Cell 4 Calibration Factor* respectively according to the equations

$$VCELL_{3-4} = \text{ADC Reading} * (\textit{ADC Full Scale Voltage} + \textit{Cell 3–4 Calibration Factor} * 8) * 2/65536 \quad (23)$$

$$VCELL_2 = \text{ADC Reading} * (\textit{ADC Full Scale Voltage} + \textit{Cell 2 Calibration Factor} * 8) /65536$$

ADC Reading is the converted voltage at the $VCELL_{1-4}$ inputs with a range of 0–32,767.

The bq2060 subtracts the sense resistor voltage from the $VCELL_4$ calculation to calculate Voltage().

Current

The bq2060 scales Current() to mA units by the 16-bit value *ADC Sense Resistor* in EE 0x6c-0x6d. Adjusting *ADC Sense Resistor* from its nominal value provides a method to calibrate the current readings for variances in the ADC gain, internal voltage reference, and sense resistor value. An additional factor *ADC Current Offset* in EE 0x7e adjusts the current offset. *ADC Current Offset* is a signed 8-bit value that cancels offset present in the circuit with no current flow. *ADC Current Offset* is typically set between -10 and 10. The bq2060 calculates Current() by

(24)

$$\text{Current}() = \frac{[(\text{ADC Reading} + \textit{ADC Current Offset}) * \textit{ADC Sense Resistor}]}{16{,}384}$$

VFC

To calibrate the coulomb counting measurement for system errors and sense resistor error, the value of *VFC Sense Resistor* EE 0x6e-0x6f may be adjusted.

The bq2060 VFC circuit has the ability to introduce a signal opposite in sign as the inherent device and circuit offset to cancel this error. The offset calibration routine is initiated with commands to ManufacturerAccess().

The bq2060 calculates the offset with the calibration routine and stores the calibration value in *VFC Offset* in EE 0x5c–0x5d and 0x5e.

Temperature

With an external thermistor (INTEMP bit = 0 in Pack Configuration), the bq2060 uses *Temperature Offset* in EE 0x47 to calibrate the Temperature() function for offset. The required offset adjustment, TOFF, sets *Temperature Offset* according to the equation

$$\textit{Temperature Offset} = \text{TOFF} * 10 \qquad (25)$$

where

$$-12.8 \le \text{TOFF} \le 12.7$$

Using the internal (INTEMP bit = 1 in Pack Configuration), the bq2060 uses *Temperature Offset* and *Internal Temperature Gain* in EE 0x5a for offset and gain adjustment, respectively. The nominal value of *Temperature Offset* and *Internal Temperature Gain* is zero.

Constants and String Data

EEPROM Constants

Block Length EE 0x00 and *Check Byte 1* EE 0x7d must be programmed to 0x7f and 0xa5, respectively.

Specification Information

Specification Information EE 0x14–0x15 stores the default value for the SpecificationInfo() function. It is stored in EEPROM in the same format as the data returned by the SepcificationInfo().

Manufacture Date

Manufacture Date EE 0x16–0x17 stores the default value for the ManufactureDate() function. It is stored in EEPROM in the same format as the data returned by the ManufactureDate().

Serial Number

Serial Number EE 0x18–0x19 stores the default value for the SerialNumber() function. It is stored in EEPROM in the same format as the data returned by the SerialNumber().

Manufacturer Name Data

Manufacturer Name Length EE 0x20 stores the length of the desired string that is returned by the ManufacturerName() function. Locations EE 0x21–0x2b store the characters for ManufacturerName() in ASCII code.

Device Name Data

Device Name Length EE 0x30 stores the length of the desired string that is returned by the DeviceName() function. Locations EE 0x31–0x37 store the characters for DeviceName() in ASCII code.

Device Chemistry Data

Device Chemistry Length EE 0x40 stores the length of the desired string that is returned by the DeviceChemistry() function. Locations EE 0x41–0x45 store the characters for DeviceChemistry() in ASCII code.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}—Supply voltage	Relative to V_{SS}	-0.3	+6.0	V	
V_{IN}–All other pins	Relative to V_{SS}	-0.3	+6.0	V	
T_{OPR}	Operating temperature	-20	+70	°C	Commercial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

4

DC Electrical Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CC}	Supply voltage		2.9	3.1	3.7	V
I_{CC}	Operating current	V_{OUT} inactive		135	TBD	µA
I_{SLP}	Sleep current	1.5V < V_{CC} < 3.7V		5	10	µA
I_{LVOUT}	V_{OUT} leakage current	V_{OUT} inactive	-0.2		0.2	µA
I_{VOUT}	V_{OUT} source current	V_{OUT} active, V_{OUT} = V_{CC} - 0.6V	-5.0			mA
I_{REG}	REG output current		1.0			µA
I_{OLS}	Sink current: LED_1–LED_5, CFC, DFC, THON, CVON	V_{OLS} = 0.4V			10	mA
V_{IL}	Input voltage low $\overline{DISP}$		-0.3		0.8	V
V_{IH}	Input voltage high $\overline{DISP}$		2.0		V_{CC} + 0.3	V
V_{OL}	Output voltage low SMBC, SMBD	I_{OL} = 1.0mA			0.4	V
V_{ILS}	Input voltage low SMBC, SMBD		-0.3		0.8	V
V_{IHS}	Input voltage high SMBC, SMBD		1.4		V_{CC} + 0.3	V
V_{SR}	Input voltage range, V_{SR2} and V_{SR1}	V_{SR} = V_{SR2} - V_{SR1}	-0.3		+0.3	V
V_{SROS}	V_{SR} input offset	V_{SR2} = V_{SR1}, auto-correction disabled	-500	-50	500	µV
V_{AI}	Input voltage range $VCELL_{1-4}$, VTH		V_{SS} - 0.3		V_{CC} + 0.3	V
I_{RB}	RBI data-retention input current	V_{RBI} > 3.0V, V_{CC} < 2.0V		10	50	nA

SMBus AC Specifications ($T_A = T_{OPR}$, 2.9V < V_{CC} < 3.7V unless otherwise noted)

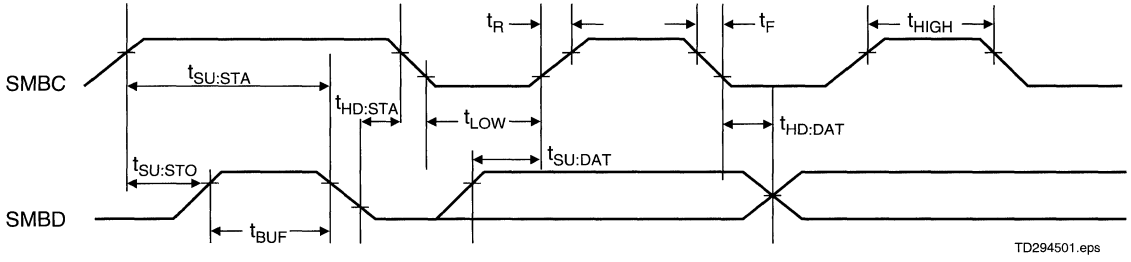
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F_{SMB}	SMBus operating frequency	Slave mode, SMBC 50% duty cycle	10		100	kHz
F_{MAS}	SMBus master clock frequency	Master mode, no clock low slave extend		51.2		kHz
T_{BUF}	Bus free time between start and stop		4.7			µs
$T_{HD:STA}$	Hold time after (repeated) start		4.0			µs
$T_{SU:STA}$	Repeated start setup time		4.7			µs
$T_{SU:STO}$	Stop setup time		4.0			µs
$T_{HD:DAT}$	Data hold time	Receive mode	0			ns
		Transmit mode	300			ns
$T_{SU:DAT}$	Data setup time		250			ns
$T_{TIMEOUT}$	Error signal/detect	See Note 1	28.1		32.8	ms
T_{LOW}	Clock low period		4.7			µs
T_{HIGH}	Clock high period	See Note 2	4.0		80	µs
$T_{LOW:SEXT}$	Cumulative clock low slave extend time	See Note 3			25	ms
$T_{LOW:MEXT}$	Cumulative clock low master extend time	See Note 4			10	ms

Notes:
1. The bq2060 will time-out when any clock low exceeds $T_{TIMEOUT}$.
2. T_{HIGH} Max. is minimum bus idle time. SMBC = SMBD = "1" for t > 80µs will cause reset of any transaction involving bq2060 that is in progress.
3. $T_{LOW:SEXT}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop. The bq2060 typically extends the clock only 20µs as a slave in the read byte or write byte protocol.
4. $T_{LOW:MEXT}$ is the cumulative time a master device is allowed to extend the clock cycles in one message from initial start to the stop. The bq2060 typically extends the clock only 20µs as a master in the read byte or write byte protocol.

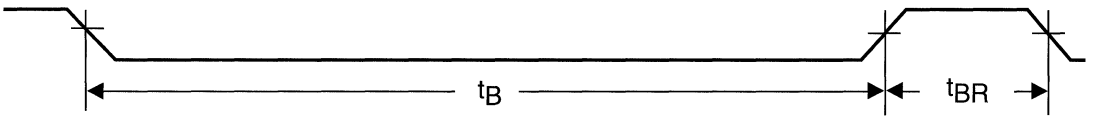
HDQ16 AC Specifications ($T_A = T_{OPR}$, 2.9V < V_{CC} < 3.7V unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{CYCH}	Cycle time, host to bq2060 (write)		190	-	-	µs
t_{CYCB}	Cycle time, bq2060 to host (read)		190	205	250	µs
t_{STRH}	Start hold time, host to bq2060 (write)		5	-	-	ns
t_{STRB}	Start hold time, host to bq2060 (read)		32	-	-	µs
t_{DSU}	Data setup time		-	-	50	µs
t_{DSUB}	Data setup time		-	-	50	µs
t_{DH}	Data hold time		90	-	-	µs
t_{DV}	Data valid time		-	-	80	µs
t_{SSU}	Stop setup time		-	-	145	µs
t_{SSUB}	Stop setup time		-	-	95	µs
t_{RSPS}	Response time, bq2060 to host		190	-	-	µs
t_B	Break time		190	-	-	µs
t_{BR}	Break recovery time		40	-	-	µs

SMBus Timing Data

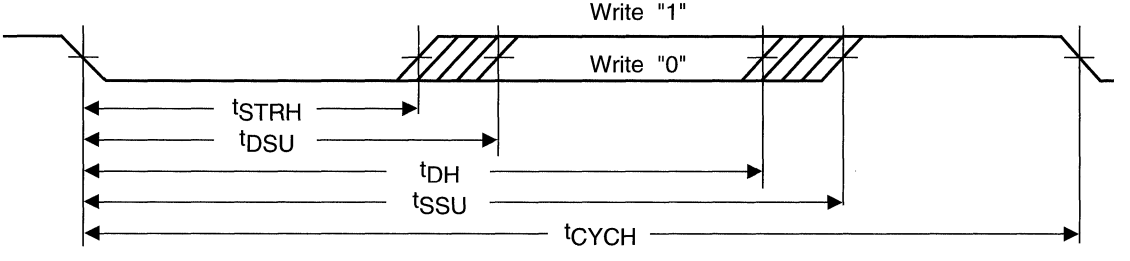


HDQ16 Break Timing

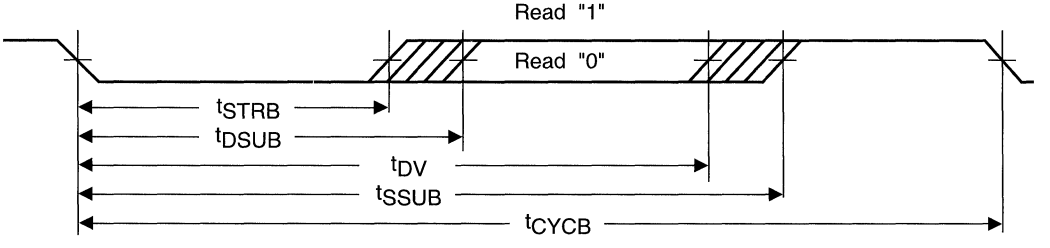


TD201803.eps

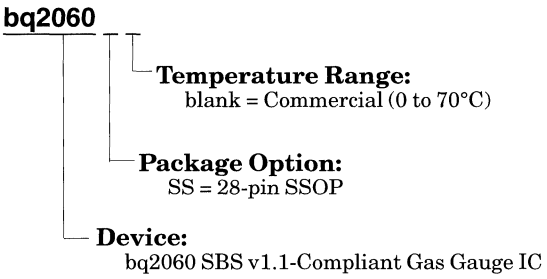
HDQ16 Host to bq2060



HDQ16 bq2060 to Host



Ordering Information



UNITRODE

bq2092

Gas Gauge IC with SMBus-Like Interface

Features

- Provides accurate measurement of available charge in NiCd, NiMH, and Li-Ion rechargeable batteries
- Supports SBData charge control commands for Li-Ion, NiMH, and NiCd chemistries
- Designed for battery pack integration
  - 120µA typical operating current
  - Small size enables implementations in as little as ¾ square inch of PCB
- Two-wire SMBus-like interface
- Measurements compensated for current and temperature
- Programmable self-discharge and charge compensation
- 16-pin narrow SOIC

General Description

The bq2092 Gas Gauge IC With SMBus-Like Interface is intended for battery-pack or in-system installation to maintain an accurate record of available battery charge. The bq2092 directly supports capacity monitoring for NiCd, NiMH, and Li-Ion battery chemistries.

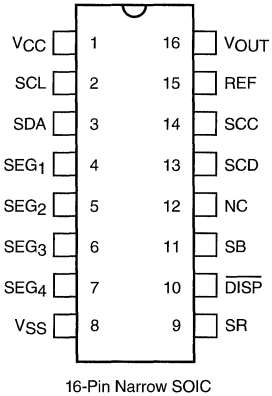
The bq2092 uses the SMBus protocol that supports many of the Smart Battery Data (SBData) commands. The bq2092 also supports SBData charge control. Battery state-of-charge, capacity remaining, remaining time and chemistry are available over the serial link. Battery-charge state can be directly indicated using a four-segment LED display to graphically depict battery full-to-empty in 25% increments.

The bq2092 estimates battery self-discharge based on an internal timer and temperature sensor and user-programmable rate information stored in external EEPROM. The bq2092 also automatically recalibrates or "learns" battery capacity in the full course of a discharge cycle from full to empty.

The bq2092 may operate directly from three nickel chemistry cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide V_{CC} for other battery cell configurations.

An external EEPROM is used to program initial values into the bq2092 and is necessary for proper operation.

Pin Connections



16-Pin Narrow SOIC

PN209101.eps

Pin Names

V_{CC}	3.0–5.5V
SCL	Serial memory clock
SDA	Serial memory data
SEG_1	LED segment 1
SEG_2	LED segment 2
SEG_3	LED segment 3
SEG_4	LED segment 4
V_{SS}	System ground
SR	Sense resistor input
$\overline{DISP}$	Display control input
SB	Battery sense input
SCD	Serial communication data input/output
SCC	Serial communication clock
REF	Voltage reference output
V_{OUT}	EEPROM supply output

Pin Descriptions

V_{CC} **Supply voltage input**

SCL **Serial memory clock**

This output is used to clock the data transfer between the bq2092 and the external nonvolatile configuration memory.

SDA **Serial memory data and address**

This bi-directional pin is used to transfer address and data to and from the bq2092 and the external configuration memory.

SEG_1–SEG_4 **LED display segment outputs**

Each output may activate an external LED to sink the current sourced from V_{CC}.

V_{SS} **Ground**

SR **Sense resistor input**

The voltage drop (V_{SR}) across pins SR and V_{SS} is monitored and integrated over time to interpret charge and discharge activity. The SR input is connected to the sense resistor and the negative terminal of the battery. $V_{SR} < V_{SS}$ indicates discharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2092 is $V_{SR} + V_{OS}$ (see Table 3).

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ floating allows the LED display to be active during charge if the rate is greater than 100mA. $\overline{DISP}$ low activates the display for 4 seconds.

SB **Secondary battery input**

This input monitors the cell pack voltage as a single-cell potential through a high-impedance resistor divider network. The cell pack voltage is reported in the SBD register function Voltage (0x09) and is compared to end-of-discharge voltage and charging voltage parameters.

NC **No connect**

SCD **Serial communication data**

This open-drain bidirectional pin is used to transfer address and data to and from the bq2092.

SCC **Serial communication clock**

This open-drain bidirectional pin is used to clock the data transfer to and from the bq2092.

REF **Reference output for regulator**

REF provides a reference output for an optional micro-regulator.

V_{OUT} **Supply output**

This output supplies power to the external EEPROM configuration memory.

Functional Description

General Operation

The bq2092 determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2092 measures discharge and charge currents, estimates self-discharge, and monitors the battery for low-battery voltage thresholds. The charge measurement is made by monitoring the voltage across a small-value series sense resistor between the battery's negative terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2092 using the LED capacity display, the serial port, and an external EEPROM for battery pack programming information. The bq2092 must be configured and calibrated for the battery-specific information to ensure proper operation. Table 1 outlines the externally programmable functions available in the bq2092. Refer to the Programming the bq2092 section for further details.

An internal temperature sensor eliminates the need for an external thermistor—reducing cost and components. An internal, temperature-compensated timebase eliminates the need for an external resonator, further reducing cost and components. The entire circuit in Figure 1 can occupy less than ¾ square inch of board space.

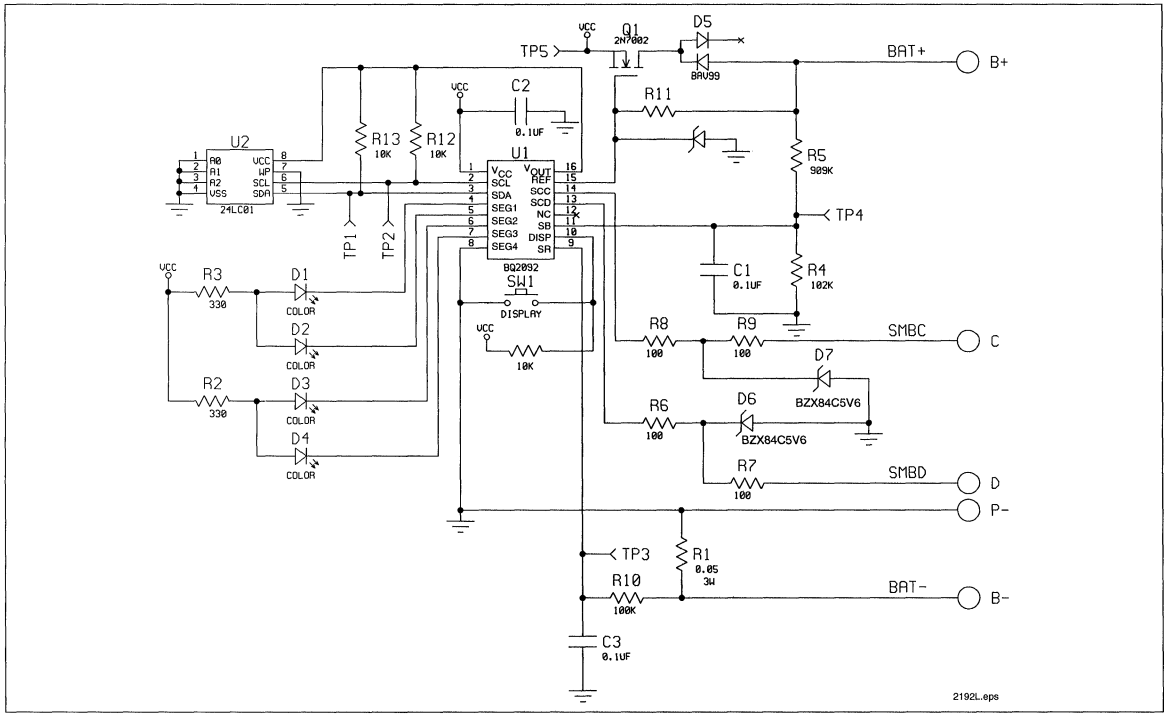


Figure 1. Battery Pack Application Diagram—LED Display

Table 1. Configuration Memory Programming Values

Parameter Name	Address	Length	Units
Design capacity	0x00/0x01	16 bits: low byte, high byte	mAh
Initial battery voltage	0x02/0x03	16 bits: low byte, high byte	mV
Fast charging current	0x04/0x05	16 bits: low byte, high byte	mA
Charging voltage	0x06/0x07	16 bit: low byte, high byte	mV
Remaining capacity alarm	0x08/0x09	16 bits: low byte, high byte	mAh
FLAGS1	0x0a	8 bits	N/A
FLAGS2	0x0b	8 bits	N/A
Current measurement gain	0x0c/0x0d	16 bits: low byte, high byte	N/A
EDV_1	0x0e/0x0f	16 bits: low byte, high byte	mV
EDV_F	0x10/0x11	16 bits: low byte, high byte	mV
Temperature offset	0x12	8 bits	0.1°K
Maximum charge temperature/$\Delta T/\Delta t$	0x13	8 bits	N/A
Self-discharge rate	0x14	8 bits	N/A
Digital filter	0x15	8 bits	N/A
Current integration gain	0x16/0x17	16 bits: low byte, high byte	N/A
Full charge percentage	0x18	8 bits	N/A
Charge compensation	0x19	8 bits	N/A
Battery voltage offset	0x1a	8 bits	mV
Battery voltage gain	0x1b/0x1c	16 bits: high byte, low byte	N/A
Serial number	0x1d/0x1e	16 bits: low byte, high byte	N/A
Hold-off timer	0x1f	8 bits	N/A
Cycle count	0x20/0x21	16 bits: low byte, high byte	N/A
Maintenance charge current	0x22/0x23	16 bits: low byte, high byte	mA
Reserved	0x24/0x31	–	–
Design voltage	0x32/0x33	16 bits: low byte, high byte	mV
Specification information	0x34/0x35	16 bits: low byte, high byte	N/A
Manufacturer date	0x36/0x37	16 bits: low byte, high byte	N/A
Reserved	0x38/0x3f	–	–
Manufacturer name	0x40/0x4f	8 + 120 bits	N/A
Device name	0x50/0x5f	8 + 120 bits	N/A
Chemistry	0x60/0x6f	8 + 120 bits	N/A
Manufacturer data	0x70/0x7f	8 +120 bits	N/A

Note: N/A = Not applicable; data packed or coded. See "Programming the bq2092" for details.

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2092 monitors the battery potential through the SB pin. The voltage potential is determined through a resistor-divider network per the following equation:

$$\frac{R_5}{R_4} = \frac{MBV}{2.25} - 1$$

where MBV is the maximum battery voltage, R_5 is connected to the positive battery terminal, and R_4 is connected to the negative battery terminal. R_5/R_4 should be rounded to the next highest integer. The voltage at the SB pin (V_{SB}) should never exceed 2.4V.

The battery voltage is monitored for the end-of-discharge voltage (EDV), for maximum pack voltage and for alarm warning conditions. EDV threshold levels are used to determine when the battery has reached an "empty" state, and the charging voltage plus 5% threshold is used for fault detection during charging. The battery voltage gain, two EDV thresholds, and charge voltage limit are programmed via EEPROM. See the Programming the bq2092 section for further details.

If V_{SB} is below either of the two EDV thresholds, the associated flag is latched and remains latched, independent of V_{SB}, until the next valid charge.

EDV monitoring may be disabled under certain conditions. If the discharge current is greater than approximately 6A, EDV monitoring is disabled and resumes after the current falls below 6A.

Reset

The bq2092 is reset when first connected to the battery pack. The bq2092 can also be reset with a command over the serial port, as described in the Software Reset section.

Temperature

The bq2092 monitors temperature using an internal sensor. The temperature is used to adapt charge/discharge and self-discharge compensations as well as maximum temperature and $\Delta T/\Delta t$ during bq2092 controlled charge. Temperature may also be accessed over the serial port. See the Programming the bq2092 section for further details.

Layout Considerations

The bq2092 measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally, in reference to Figure 1:

- The capacitors (C1, C2, and C4) should be placed as close as possible to the SB and V_{CC} pins, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor capacitor (C3) should be placed as close as possible to the SR pin.
- The sense resistor (R1) should be as close as possible to the bq2092.
- The IC should be close to the cells for the best temperature measurement.
- An optional zener may be necessary to ensure V_{CC} is not above the maximum rating during operation.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2092. The bq2092 accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge currents are compensated for temperature and state-of-charge. Self-discharge is only temperature-compensated.

The main counter, RemainingCapacity (RM), represents the available battery capacity at any given time. Battery charging increments the RM register, whereas battery discharging and self-discharge decrement the RM register and increment the Discharge Count Register (DCR).

The Discharge Count Register (DCR) is used to update the FullChargeCapacity (FCC) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2092 adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the DesignCapacity (DC). Until FCC is updated, RM counts up to, but not beyond, this threshold during subsequent charges.

1. **FullChargeCapacity or learned-battery capacity:**

   FCC is the last measured discharge capacity of the battery. On initialization (application of V_{CC} or reset), FCC = DC. During subsequent discharges, the FCC is updated with the latest measured capacity in the Discharge Count Register, representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the FCC register. The FCC also serves as the 100% reference threshold used by the relative state-of-charge calculation and display.

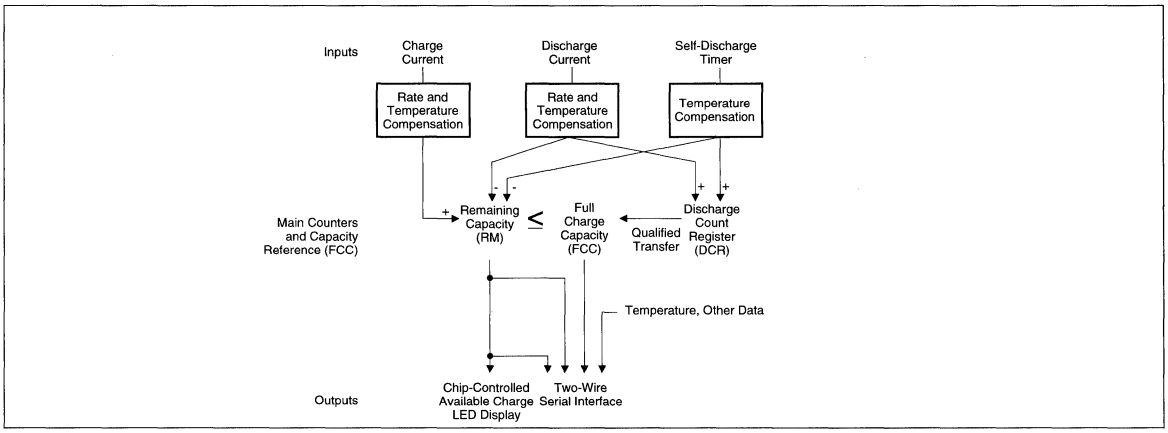


Figure 2. Operational Overview

2. DesignCapacity (DC):

The DC is the user-specified battery capacity and is programmed by using an external EEPROM. The DC also provides the 100% reference for the absolute display mode.

3. Remaining Capacity (RM):

RM counts up during charge to a maximum value of FCC and down during discharge and self-discharge to 0. RM is reset to 0000Ah when EDV1 = 1 and a valid charge is detected. To prevent overstatement of charge during periods of overcharge, RM stops incrementing when RM = FCC. RM may optionally be written to a user-defined value when fully charged when the battery pack is under bq2092 charge control. See the Charge Control section for further details.

4. Discharge Count Register (DCR):

The DCR counts up during discharge independent of RM and can continue increasing after RM has decremented to 0. Before RM = 0 (empty battery), both discharge and self-discharge increment the DCR. After RM = 0, only discharge increments the DCR. The DCR resets to 0 when RM = FCC. The DCR does not roll over but stops counting when it reaches FFFFh.

The DCR value becomes the new FCC value on the first charge after a valid discharge to V_{EDV1} if:

- No valid charge initiations (charges greater than 10mAh, where $V_{SRO} > |V_{SRD}|$) occurred during the period between RM = FCC and EDV1 detected.
- The self-discharge count is not more than 256mAh.
- The temperature is ≥ 273°K (0°C) when the EDV1 level is reached during discharge.

The valid discharge flag (VDQ) indicates whether the present discharge is valid for FCC update. FCC cannot be reduced by more than 256mAh during any single cycle.

Charge Counting

Charge activity is detected based on a positive voltage on the V_{SR} input. If charge activity is detected, the bq2092 increments RM at a rate proportional to V_{SRO} and, if enabled, activates an LED display. Charge actions increment the RM after compensation for charge rate and temperature.

The bq2092 determines charge activity sustained at a continuous rate equivalent to $V_{SRO} > |V_{SRD}|$. **A valid charge equates to sustained charge activity greater than 10 mAh**. Once a valid charge is detected, charge counting continues until V_{SRO} falls below $|V_{SRD}|$. V_{SRD} is a programmable threshold as described in the Digital Magnitude Filter section.

Discharge Counting

All discharge counts where $V_{SRO} < |V_{SRD}|$ cause the RM register to decrement and the DCR to increment. V_{SRD} is a programmable threshold as described in the Digital Magnitude Filter section.

Self-Discharge Estimation

The bq2092 continuously decrements RM and increments DCR for self-discharge based on time and temperature. The self-discharge rate is dependent on the battery chemistry. The bq2092 self-discharge estimation rate is externally programmed in EEPROM

6/26

and can be programmed from 0 to 25% per day at 20-30°C. This rate doubles every 10°C increase until T > 70°C or is halved every 10° decrease until T < 10°C.

The self-discharge estimate reduces RM by 0.39% of its current value at time intervals spaced so that the average reduction equals the programmed value adjusted for temperature. The EEPROM program constant is the 2's complement of $52.73/X$, where $X = \%/day$ self-discharge rate desired at 25°C.

Charge Control

The bq2092 supports SBD charge control by broadcasting ChargingCurrent() and ChargingVoltage() to the Smart Charger address. Smart Charger broadcasts can be disabled by writing bit 14 of Battery Mode() to 1. The bq2092-based charge control can be enabled by setting bit 4 in FLAGS2 (MSB of 0x2f) to 1. See Programming the bq2092 for further details. If the Fully_Charged bit is not set in BatteryStatus, the bq2092 broadcasts the fast charge current and voltage to the Smart Charger. The bq2092 broadcasts the maintenance current values (trickle rate) if the Fully_Charged bit is set or Voltage is below EDVF.

The bq2092 internal charge control is compatible with nickel-based and Li-Ion chemistries.

For Li-Ion, the bq2092 broadcasts the required ChargingCurrent and ChargingVoltage according to the values programmed in the external EEPROM. During a valid charge (VQ = 1), the bq2092 signals a valid charge termination when the Terminate_Charge_Alarm and Fully_Charged bits are set in BatteryStatus. These bits are set when the battery is charged more than 256mAh above FCC.

For nickel-based chemistries, the bq2092 broadcasts the required charge current and voltage according to the programmed values in the external EEPROM. Maximum temperature and ΔT/Δt are used as valid charge termination methods. **Note:** Nickel-based chemistries require a charge voltage higher than the maximum cell voltage during charge to ensure constant-current charging. During a valid charge (VQ = 1), if the bq2092 determines a maximum temperature condition, a ΔT/Δt rate greater than the programmed value, or a charge state greater than 256mAh above FCC, then the Terminate_Charge_Alarm, Over_Charge_Alarm, and Fully_Charged bits are set in BatteryStatus.

Once the bq2092 detects a valid charge termination, the Fully_Charged bit, Terminate_Charge_Alarm, and Over_Charge_Alarm bits are set and the ChargingCurrent is set to zero. Once the terminating condition ceases, the Terminate_Charge_Alarm and OverCharge Alarm bits are cleared and the ChargingCurrent is set to the maintenance rate. The bq2092 requests the maintenance current and charging voltage until RM falls below the full charge percentage. Once this occurs, the Fully_Charged bit is cleared, and the bq2092 requests the fast charging current and charging voltage.

During fast charge, the bq2092 suspends charge by requesting zero current and setting the Terminate_Charge_Alarm bit in BatteryStatus. Charge is suspended if the actual charge current is 25% greater than the programmed charged current. If the programmed charge current is less than 1024mA, overcurrent suspend occurs if the actual charge current is 256mA greater than the programmed value. Charge is also suspended if the actual battery voltage is 5% greater than the programmed charge voltage. If the battery temperature is greater than the programmed maximum temperature before charge, then the bq2092 suspends charge requests until the temperature falls below 50°C.

If the battery temperature is less than 0°C, the charging current sets to maintenance (trickle) charge current. The fast charging current is requested when the temperature is above 5°C.

ΔT/Δt

The ΔT/Δt used by the bq2092 is programmable in both the temperature step (1.6°C–4.6°C) and time step (20 seconds–320seconds). Typical settings for 1°C/min include 2°C over 120 seconds and 3°C over 180 seconds. Longer times are required for increased slope resolution.

$\frac{\Delta T}{\Delta t}$ is set by the formula: $\frac{\Delta T}{\Delta t} =$

$$\frac{[(\text{lower nibble of } 0*13 \text{ in } E^2PROM)*2+16]}{[2^s(\text{lower nibble of } 0*1f \text{ in } E^2PROM)*3.33]}\left[\frac{°C}{\text{minute}}\right]$$

In addition to the ΔT/Δt timer, there is a hold-off timer, which starts when the battery is being charged at more than 256mA and the temperature is above 25°C. (This is valid only for NiMH chemistry, bit 5 in FLAGS2 set to 0.) Until this timer expires, ΔT/Δt is suspended. If the temperature falls below 25°C, or if charging current fallls below 255mA, the timer is reset and restarts only if the above conditions are once again met.

Safety Termination

If charging continues for more than 256mAh beyond RM = FCC, the Terminate_Charge_Alarm and Fully_Charged bits are set, and the charging current is modified to request maintenance current. If the battery is discharged from full by less than 256mAh, then the safety overcharge termination, for NiMH only, is allowed to extend to 512 mAh.

Updating RM after a valid charge termination, RM may optionally be set to a value from 0 to 100% of the FullChargeCapacity. If RM is below the value programmed

in full charge percentage, RM is set to full charge percentage of FCC on valid charge termination. If RM is above the full charge percentage, RM is not modified.

Count Compensations

Charge activity is compensated for temperature and state-of-charge before updating the RM and/or DCR. RM is compensated for temperature before updating the RM register. Self-discharge estimation is compensated for temperature before updating RM or DCR.

Charge Compensation

Charge efficiency is compensated for state-of-charge, temperature, and battery chemistry. For Li-Ion chemistry cells, the charge efficiency is unity for all cases. The charge efficiency for nickel chemistry cells, however, is adjusted using the following equation:

$$RM = RM * (Q_{EFC} - Q_{ET})$$

where RelativeStateofCharge $\leq$ FullChargePercentage

and Q_{EFC} is the programmed fast charge efficiency varying from .75 to .99.

$$RM = RM * (Q_{ETC} - Q_{ET})$$

where RelativeStateofCharge $\geq$ FullChargePercentage

and Q_{ETC} is the programmed maintenance (trickle) charge efficiency varying from 0.50 to 0.97.

Q_{ET} is used to adjust the charge efficiency as the battery temperature increases according to the following:

$Q_{ET} = 0$ if $T < 30°C$

$Q_{ET} = 0.02$ if $30°C \leq T < 40°C$

$Q_{ET} = 0.05$ if $T \geq 40°C$

Remaining Capacity Compensation

The bq2092 adjusts the RM as a function of temperature. This adjustment accounts for the reduced capacity of the battery at colder temperatures. The following equation is used to adjust RM:

If $T \geq 5°C$

RemainingCapacity =
Nominal Available Capacity (NAC)

If $T < 5°C$

$RM() = NAC() (1 + TCC * (T - 5°C))$

Where T = temperature °C

TCC = 0.004

Table 2. Typical Digital Filter Settings

DMF	DMF Hex.	$\lvert V_{SRD}$ (mV)$\rvert$
75	4B	±0.60
100	64	±0.45
150 (default)	96	±0.30
175	AF	±0.26
200	C8	±0.23

RM adjusts upward to Nominal Available Capacity as the temperature increases.

Digital Magnitude Filter

The bq2092 has a programmable digital filter to eliminate charge and discharge counting below a set threshold. Table 2 shows typical digital filter settings. The proper digital filter setting can be calculated using the following equation.

$$|V_{SRD} (mV)| = 45 / DMF$$

Error Summary

Capacity Inaccurate

The FCC is susceptible to error on initialization or if no updates occur. On initialization, the FCC value includes the error between the design capacity and the actual capacity. This error is present until a valid discharge occurs and FCC is updated (see the DCR description on page 6). The other cause of FCC error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity. Periodic discharges from full to empty will minimize errors in FCC.

Current-Sensing Error

Table 3 illustrates the current-sensing error as a function of V_{SR}. A digital filter eliminates charge and discharge counts to the RM register when V_{SRO} is between V_{SRQ} and V_{SRD}.

Display

The bq2092 can directly display capacity information using low-power LEDs. The bq2092 displays the battery charge state in either absolute or relative mode. In relative mode, the battery charge is represented as a percentage of the FCC. Each LED segment represents 25% of the FCC.

8/26

Table 3. bq2092 Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
V_{OS}	Offset referred to V_{SR}	± 50	± 150	µV	$\overline{DISP}$ = V_{CC}.
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

In absolute mode, each segment represents a fixed amount of charge, 25% of the design capacity. As the battery wears out over time, it is possible for the FCC to be below the design capacity. In this case, all of the LEDs may not turn on in absolute mode, representing the reduction in the actual battery capacity.

The displayed capacity is compensated for the present battery temperature. The displayed capacity varies as temperature varies, indicating the available charge at the present conditions.

When $\overline{DISP}$ is tied to V_{CC}, the SEG_{1-4} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active whenever the bq2092 detects a charge rate of 100mA or more. When pulled low, the segment outputs become active immediately for a period of approximately 4 seconds. The $\overline{DISP}$ pin must be returned to float or V_{CC} to reactivate the display.

The segment outputs are modulated as two banks of two, with segments 1 and 3 alternating with segments 2 and 4. The segment outputs are modulated at approximately 100Hz with each segment bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV1} (EDV_1 = 1), indicating a low-battery condition. V_{SB} below V_{EDVF} (EDV_F = 1) disables the display output.

Microregulator

The bq2092 can operate directly from three nickel chemistry cells. To facilitate the power supply requirements of the bq2092, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2092 can be inexpensively built using the FET and an external resistor; see Figure 1. Note that an optional zener diode may be necessary to limit V_{CC} during charge.

Communicating With the bq2092

The bq2092 includes a simple two-pin (SCC and SCD) bidirectional serial data interface. A host processor uses the interface to access various bq2092 registers; see Table 4. This allows battery characteristics to be easily monitored. The open-drain SCD and SCC pins on the bq2092 are pulled up by the host system, or may be connected to V_{SS}, if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends the battery address and an eight-bit command byte to the bq2092. The command directs the bq2092 to either store the next data received to a register specified by the command byte or output the data specified by the command byte.

bq2092 Data Protocols

The host system, acting in the role of a Bus master, uses the read word and write word protocols to communicate integer data with the bq2092. (See Figure 3.)

Host-to-bq2092 Message Protocol

The Bus Host communicates with the bq2092 using one of three protocols:

- Read word
- Write word
- Read block

The particular protocol used is a function of the command. The protocols used are shown in Figure 3.

Host-to-bq2092 Messages (see Table 4)

ManufacturerAccess() (0x00)

This optional function is not operational for the bq2092.

RemainingCapacityAlarm() (0x01)

This function sets or returns the low-capacity alarm value. When RM falls below the RemainingCapacityAlarm value, the Remaining_Capacity_Alarm bit is set in BatteryStatus (0x16). The system may alter this alarm value during operation.

Table 4. bq2092 Register Functions

Function	Code	Access	Units	Defaults[1]
ManufacturerAccess	0x00	read/write	-	-
RemaningCapacityAlarm	0x01	read/write	unsigned int.	E^2
RemainingTimeAlarm	0x02	read/write	unsigned int.	10
BatteryMode	0x03	read/write	bit flag	-
Temperature	0x08	read	0.1°K	-
Voltage	0x09	read	mV	-
Current	0x0a	read	mA	0000h
AverageCurrent	0x0b	read	mA	0000h
MaxError	0x0c	read	percent	100
RelativeStateOfCharge	0x0d	read	percent	0000h
AbsoluteStateOfCharge	0x0e	read	percent	0000h
RemainingCapacity	0x0f	read	mAh	0000h
FullChargeCapacity	0x10	read	mAh	E^2
RunTimeToEmpty	0x11	read	minutes	-
AverageTimeToEmpty	0x12	read	minutes	-
Reserved	0x13	-	-	-
ChargingCurrent	0x14	read	mA	E^2
ChargingVoltage	0x15	read	mV	E^2
BatteryStatus	0x16	read	number	0000h
CycleCount	0x17	read	count	E^2
DesignCapacity	0x18	read	mAh	E^2
DesignVoltage	0x19	read	mV	E^2
SpecificationInfo	0x1a	read	number	E^2
ManufactureDate	0x1b	read	unsigned int	E^2
SerialNumber	0x1c	read	number	E^2
Reserved	0x1d - 0x1f	-	-	-
ManufacturerName	0x20	read	string	E^2
DeviceName	0x21	read	string	E^2
DeviceChemistry	0x22	read	string	E^2
ManufacturerData	0x23	read	string	E^2
FLAGS1 and FLAGS2	0x2f	read	bit flag	E^2
Endof DischargeVoltage1	0x3e	read	mV	E^2
EndofDischargeVoltageFinal	0x3f	read	mV	E^2

Note: 1. Defaults after reset or power-up.

10/26

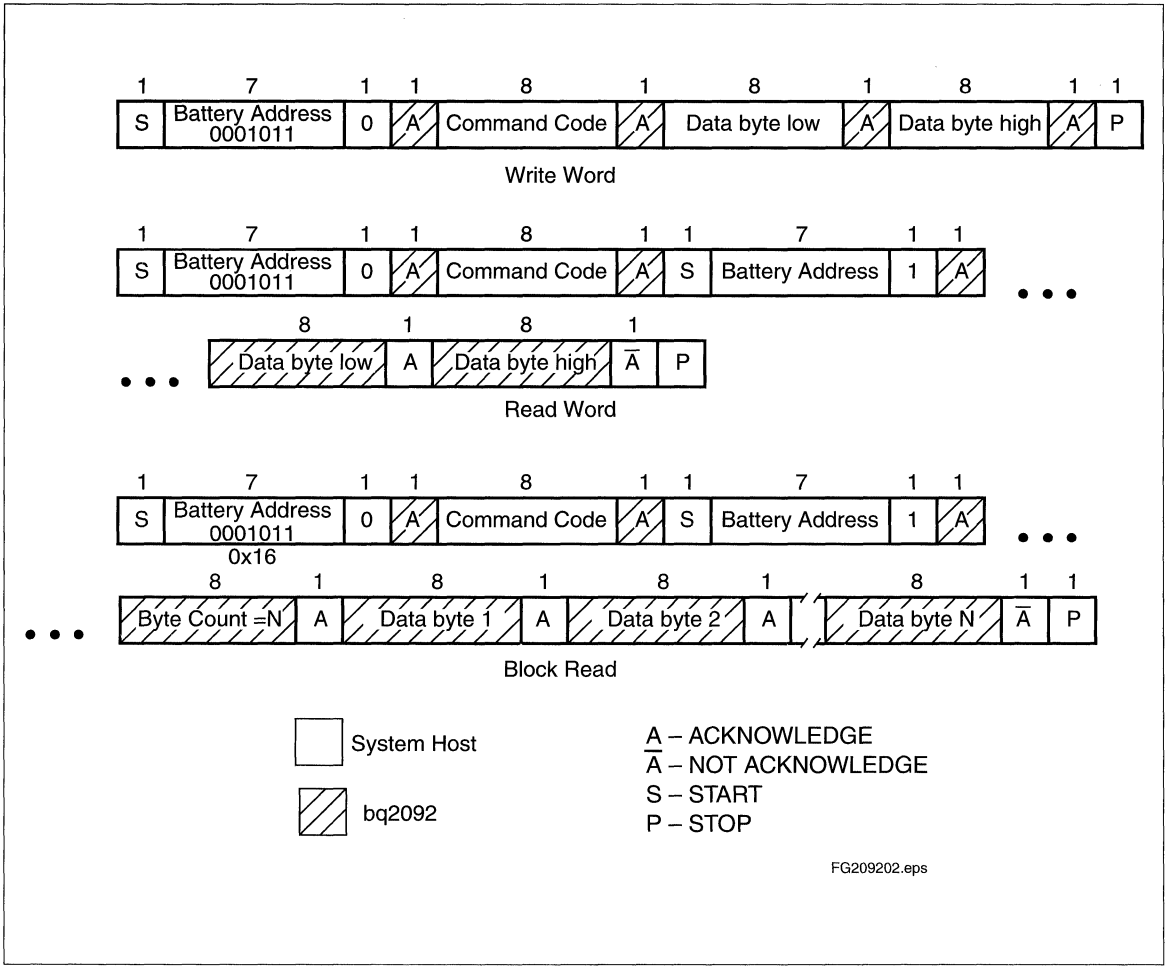


Figure 3. Host Communication Protocols

Input/Output: unsigned integer. This sets/returns the value where the Remaining Capacity Alarm bit is set in BatteryStatus.

RemainingTimeAlarm() (0x02)

This function sets or returns the low remaining time alarm value. When the AverageTimeToEmpty (0x12) falls below this value, the Remaining_Time_Alarm bit in BatteryStatus is set. The default value for this register is set in EEPROM. The system may alter this alarm value during operation.

Input/Output: unsigned integer. This sets/returns the value where the Remaining_Time_Alarm bit is set in BatteryStatus.

BatteryMode() (0x03)

This read/write word selects the various battery operational modes. The bq2092 supports the battery capacity information specified in mAh. This function also determines whether the bq2092 charging values are broadcasted to the Smart Battery Charger address.

Writing bit 14 to 1 disables voltage and current Smart Battery Charger messages. Bit 14 is reset to 0 once the pack is removed from the system (SCC and SCD = 0 for greater than 2 seconds.)

Writing bit 13 to 1 disables all Smart Battery Charger messages including alarm messages. This bit remains set until overwritten. Programming bit 3 of FLAGS2 in EEPROM (EE 0x0b) initializes bit 13 of BatteryMode to 1.

Temperature() (0x08)

This read-only word returns the cell-pack's internal temperature (0.1°K).

Output: unsigned integer. Returns cell temperature in tenths of degrees Kelvin increments

Units: 0.1°K

Range: 0 to +500.0°K

Granularity: 0.5°K or better

Accuracy: ±3°K after calibration

Voltage() (0x09)

This read-only word returns the cell-pack voltage (mV).

Output: unsigned integer. Returns battery terminal voltage in mV

Units: mV

Range: 0 to 65,535 mV

Granularity: 0.2% of DesignVoltage

Accuracy: ±1% of DesignVoltage after calibration

Current() (0x0a)

This read-only word returns the current through the battery's terminals (mA).

Output: signed integer. Returns the charge/discharge rate in mA, where positive is for charge and negative is for discharge

Units: mA

Range: 0 to 32,767 mA for charge or 0 to –32,768 mA for discharge

Granularity: 0.2% of the DesignCapacity or better

Accuracy: ±1% of the DesignCapacity after calibration

AverageCurrent() (0x0b)

This read-only word returns a rolling average of the current through the battery's terminals. For the bq2092 Current = AverageCurrent. The AverageCurrent function returns meaningful values after the battery's first minute of operation.

Output: signed integer. Returns the charge/discharge rate in mA, where positive is for charge and negative is for discharge

Units: mA

Range: 0 to 32,767 mA for charge or 0 to –32,768 mA for discharge

Granularity: 0.2% of the DesignCapacity or better

Accuracy: ±1% of the DesignCapacity after calibration

MaxError() (0x0c)

This read-only word returns the expected margin of error (%).

Output: unsigned integer. Returns percent uncertainty

Units: %

Range: 0 to 100%

RelativeStateOfCharge() (0x0d)

This read-only word returns the predicted remaining battery capacity expressed as a percentage of FullChargeCapacity (%). **RelativeStateOfCharge is only valid for battery capacities less than 10,400mAh.**

Output: unsigned integer. Returns the percent of remaining capacity

Units: %

Range: 0 to 100%

Granularity: 1%

AbsoluteStateOfCharge() (0x0e)

This read-only word returns the predicted remaining battery capacity expressed as a percentage of DesignCapacity (%). Note that AbsoluteStateOfCharge can return values greater than 100%. **Absolute StateOfCharge is only valid for battery capacities less than 10,400mAh**.

Output: unsigned integer. Returns the percent of remaining capacity.

Units: %

Range: 0 to 65,535 %

Granularity: 1% or better

Accuracy: ±MaxError

RemainingCapacity() (0x0f)

This read-only word returns the predicted remaining battery capacity. The RemainingCapacity value is expressed in mAh.

Output: unsigned integer. Returns the estimated remaining capacity in mAh.

Units: mAh

Range: 0 to 65,535 mAh

Granularity: 0.2% of DesignCapacity or better

FullChargeCapacity() (0x10)

This read-only word returns the predicted pack capacity when it is fully charged. FullChargeCapacity defaults to the value programmed in the external EEPROM until a new pack capacity is learned.

Output: unsigned integer. Returns the estimated full charge capacity in mAh.

Units: mAh

Range: 0 to 65,535 mAh

Granularity: 0.2% of DesignCapacity or better

RunTimeToEmpty() (0x11)

This read-only word returns the predicted remaining battery life at the present rate of discharge (minutes). The RunTimeToEmpty() value is calculated based on Current().

Output: unsigned integer. Returns the minutes of operation left.

Units: minutes

Range: 0 to 65,534 minutes

Granularity: 2 minutes or better

Invalid data indication: 65,535 indicates battery is not being discharged

AverageTimeToEmpty() (0x12)

This read-only word returns the predicted remaining battery life at the present average discharge rate (minutes). The AverageTimeToEmpty is calculated based on AverageCurrent.

Output: unsigned integer. Returns the minutes of operation left.

Units: minutes

Range: 0 to 65,534 minutes

Granularity: 2 minutes or better

Invalid data indication: 65,535 indicates battery is not being charged

ChargingCurrent() (0x14)

If enabled, the bq2092 sends the desired charging rate in mA to the Smart Battery Charger.

Output: unsigned integer. Transmits/returns the maximum charger output current in mA.

Units: mA

Range: 0 to 65,534 mA

Granularity: 0.2% of the design capacity or better

Invalid data indication: 65,535 indicates that the Smart Charger should operate as a voltage source outside its maximum regulated current range.

ChargingVoltage() (0x15)

If enabled, the bq2092 sends the desired voltage in mV to the Smart Battery Charger.

Output: unsigned integer. Transmits/returns the charger voltage output in mV.

Units: mV

Range: 0 to 65,534mV

Granularity: 0.2% of the DesignVoltage or better

Invalid data indication: 65,535 indicates that the Smart Battery Charger should operate as a cur-

rent source outside its maximum regulated voltage range.

BatteryStatus() (0x16)

This read-only word returns the BatteryStatus word.

Output: unsigned integer. Returns the status register with alarm conditions bitmapped as shown in Table 5.

Some of the BatteryStatus flags (Remaining_Capacity_Alarm and Remaining_Time_Alarm) are calculated based on current. See Table 8 for definitions.

CycleCount() (0x17)

This read-only word returns the number of charge/discharge cycles the battery has experienced. A charge/discharge cycle starts from a base value equivalent to the battery's state-of-charge, on completion of a charge cycle. The bq2092 increments the cycle counter during the current charge cycle, if the battery has been discharged 15% below the state-of-charge at the end of the last charge cycle. This prevents false reporting of small charge/discharge cycles.

Output: unsigned integer. Returns the count of charge/discharge cycles the battery has experienced.

Units: cycles

Range: 0 to 65,535 cycles; 65,535 indicates battery has experienced 65,535 or more cycles

Granularity: 1 cycle

DesignCapacity() (0x18)

This read-only word returns the theoretical capacity of a new pack. The DesignCapacity() value is expressed in mAh at the nominal discharge rate.

Output: unsigned integer. Returns the battery capacity in mAh.

Units: mAh

Range: 0 to 65,535 mAh

DesignVoltage() (0x19)

This read-only word returns the theoretical voltage of a new pack in mV.

Output: unsigned integer. Returns the battery's normal terminal voltage in mV.

Units: mV

Range: 0 to 65,535 mV

SpecificationInfo() (0x1a)

This read-only word returns the specification revision the bq2092 supports. It is typically set to all zeros to represent non-Rev 1.0 compliance to the SMBus specification output: unsigned integer.

ManufactureDate() (0x1b)

This read-only word returns the date the cell was manufactured in a packed integer word. The date is packed as follows: (year - 1980) * 512 + month * 32 + day.

Field	Bits Used	Format	Allowable Value
Day	0–4	5-bit binary value	1–31 (corresponds to date)
Month	5–8	4-bit binary value	1–12 (corresponds to month number)
Year	9–15	7-bit binary value	0–127 (corresponds to year biased by 1980)

Table 5. Status Register

Alarm Bits	
0x8000	Overcharge_Alarm
0x4000	Terminate_Charge_Alarm
0x2000	Reserved
0x1000	Over_Temp_Alarm
0x0800	Terminate_Discharge_Alarm
0x0400	Reserved
0x0200	Remaining_Capacity_Alarm
0x0100	Remaining_Time_Alarm
Status Bits	
0x0080	Initialized
0x0040	Discharging
0x0020	Fully_Charged
0x0010	Fully_Discharged
Error Code	
0x0000-0x000f	Reserved for error codes

SerialNumber() (0x1c)

This read-only word returns a serial number. This number, when combined with the ManufacturerName, the DeviceName, and the ManufactureDate, uniquely identifies the battery.

Output: unsigned integer

14/26

ManufacturerName() (0x20)

This read-only string returns a character string where the first byte is the number of characters available. The maximum number of characters is 15. The character string contains the battery manufacturer's name. For example, "Unitrode" identifies the battery pack manufacturer as Unitrode.

Output: string or ASCII character string

DeviceName() (0x21)

This read-only string returns a character string where the first byte is the number of characters available. The maximum number of characters is 15. The 15-byte character string contains the battery's name. For example, a DeviceName of "bq2092" indicates that the battery is a model bq2092.

Output: string or ASCII character string

DeviceChemistry() (0x22)

This read-only string returns a character string where the first byte is the number of characters available. The maximum number of characters is 15. The 15-byte character string contains the battery's chemistry. For example, if the DeviceChemistry function returns "NiMH," the battery pack contains nickel-metal hydride cells.

Output: string or ASCII character string

ManufacturerData() (0x23)

This read-only string allows access to an up to 15-byte manufacturer data string.

Output: block data—data whose meaning is assigned by the Smart Battery's manufacturer.

EndofDischargeVoltage1() (0x3e)

This read-only word returns the first end-of-discharge voltage programmed for the pack.

Output: two's complemented unsigned integer. Returns battery end-of-discharge voltage programmed in EEPROM in mV.

EndofDischargeVoltageF() (0x3f)

This read-only word returns the final end-of-discharge voltage programmed for the pack.

Output: two's complemented unsigned integer. Returns battery final end-of-discharge voltage programmed in EEPROM in mV.

FLAGS1&2() (0x2f)

This read-only register returns an unsigned integer representing the internal status registers of the bq2092. The MSB represents FLAGS2, and the LSB represents FLAGS1. See Table 6 for the bit description for FLAGS1 and FLAGS2.

FLAGS2

The *Display Mode* flag (DMODE), bit 7, determines whether the bq2092 displays Relative or Absolute capacity.

The DMODE values are:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
DMODE	-	-	-	-	-	-	-

Where DMODE is:

0 Selects Absolute display

1 Selects Relative display

Bit 6 is reserved.

The *Chemistry* flag (CHM), bit 5, selects Li-Ion or nickel compensation factors.

The CHM values are:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
-	-	CHM	-	-	-	-	-

Table 6. Bit Descriptions for FLAGS1 and FLAGS2

	(MSB) 7	6	5	4	3	2	1	0 (LSB)
FLAGS2	DMODE	-	CHM	CC	-	OV	LTF	OC
FLAGS1	-	-	VQ	WRINH	VDQ	SEDV	EDV1	EDVF

Note: - = Reserved

15/26

Where CHM is:

0 Selects Nickel

1 Selects Li-Ion

Bit 4, the *Charge Control* flag (CC), determines whether a bq2092-based charge termination will set RM to a user-defined programmable full charge capacity.

The CC values are:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	CC	-	-	-	-

Where CC is:

0 RM is not modified on valid bq2092 charge termination

1 RM is set to a programmable percentage of the FCC when a valid bq2092 charge termination occurs

Bit 3 is reserved.

Bit 2, the *Overvoltage* flag (OV), is set when the bq2092 detects a pack voltage 5% greater than the programmed charging voltage. This bit is cleared when the pack voltage falls 5% below the programmed charging voltage.

The OV values are:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	OV	-	-

Where OV is:

0 BatteryVoltage() < 1.05 * ChargingVoltage

1 BatteryVoltage() ≥ 1.05 * ChargingVoltage

Bit 1, the *Low Temperature Fault* flag (LTF), is set when temperature < 0°C and cleared when temperature > 5°C.

The LTF values are:

Where LTF is:

0 Temperature > 5°C

1 Temperature < 0°C

Bit 0, the *Overcurrent* flag (OC), is set when the average current is 25% greater than the programmed charging current. If the charging current is programmed less than 1024mA, overcurrent is set if the average current is 256mA greater than the programmed charging current. This flag is cleared when the average current falls below 256mA.

The OC values are:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OC

Where OC is:

0 Average current is less than 1.25 * charging current or less than 256mA if charging current is programmed less than 1024mA

1 Average current exceeds 1.25 * charging current or 256mA if the charging current is programmed less than 1024mA. This bit is cleared if average current < 256mA

FLAGS1

Bits 7 and 6 are reserved. The *Valid Charge* flag (VQ), bit 5, is set when $V_{SRO} \geq |V_{SRD}|$ and 10mAh of charge has accumulated. This bit is cleared during a discharge and when $V_{SRO} \leq |V_{SRD}|$.

The VQ values are:

FLAGS1 Bits							
7	6	5	4	3	2	1	0
-	-	VQ	-	-	-	-	-

Where VQ is:

0 $V_{SRO} \leq |V_{SRD}|$

1 $V_{SRO} \geq |V_{SRD}|$ and 10mAh of charge has accumulated

The *Write Inhibit* flag (WRINH), bit 4, allows or inhibits writes to all registers.

The WRINH values are:

FLAGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	WRINH	-	-	-	-

Where WRINH is:

0 Allows writes to all registers

1 Inhibits all writes and secures the bq2092 from invalid/undesired writes.

WRINH should be set at the time of pack assembly and tested to prevent special read-write registers from accidental over-writing.

The *Valid Discharge* flag (VDQ), bit 3, is set when a valid discharge is occurring (discharge cycle valid for learning new full charge capacity) and cleared if a partial charge is detected, EDV1 is asserted when T < 0°C, or self-discharge accounts for more than 256mAh of the discharge.

The VDQ values are:

FLAGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

Where VDQ is:

0 Self-discharge is greater than 256mAh, EDV1 = 1 when T < 0°C or VQ = 1

1 On first discharge after RM=FCC

The *Stop EDV* flag (SEDV), bit 2, is set when the discharge current > 6.15A and cleared when the discharge current falls below 6.15A.

The SEDV values are:

FLAGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	SEDV	-	-

Where SEDV is:

0 Current < 6.15A

1 Current > 6.15A

The *First End-of-Discharge Voltage* flag (EDV1), bit 1, is set when Voltage < EDV1 = 1 if SEDV = 0 and cleared when VQ = 1 and Voltage > EDV1.

The EDV1 values are:

FLAGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV1	-

Where EDV1 is:

0 VQ = 1 and Voltage > EDV1

1 Voltage < EDV1 and SEDV = 0

The *Final End-of-Discharge Voltage* flag (EDVF), bit 0, is set when Voltage < EDVF = 1 if SEDV = 0 and cleared when VQ = 1 and Voltage() > EDVF.

The EDVF values are:

FLAGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	EDVF

Where EDVF is:

0 VQ = 1 and Voltage > EDVF

1 Voltage < EDVF and SEDV = 0

Software Reset

The bq2092 can be reset over the serial port by confirming that the WRINH bit is set to zero in FLAGS1, writing MaxError (0x0c) to any value other than 2, and writing the reset register (0x44) to 8009, causing the bq2092 to reinitialize and read the default values from the external EEPROM.

Error Codes and Status Bits

Error codes and status bits are listed in Table 7 and Table 8, respectively.

Programming the bq2092

The bq2092 requires the proper programming of an external EEPROM for proper device operation. Each module can be calibrated for the greatest accuracy, or general "default" values can be used. A programming kit (interface board, software, and cable) for an IBM-compatible PC is available from Unitrode. Please contact Unitrode for further details

The bq2092 uses a 24LC01 or equivalent serial EEPROM for storing the various initial values, calibration data, and string information. Table 1 outlines the parameters and addresses for this information. Tables 9 and 10 detail the various register contents and show an example program value for an 1800mAh NiMH battery pack, using a 50mΩ sense resistor.

Table 7. Error Codes (BatteryStatus() (0x16))

Error	Code	Access	Description
OK	0x0000	read/write	bq2092 processed the function code without detecting any errors
Busy	0x0001	read/write	bq2092 is unable to process the function code at this time
NotReady	0x0002	read/write	bq2092 cannot read or write the data at this time—try again later
UnsupportedCommand	0x0003	read/write	bq2092 does not support the requested function code
AccessDenied	0x0004	write	bq2092 detected an attempt to write to a read-only function code
Overflow/Underflow	0x0005	read/write	bq2092 detected a data overflow or underflow
BadSize	0x0006	write	bq2092 detected an attempt to write to a function code with an incorrect size data block
UnknownError	0x0007	read/write	bq2092 detected an unidentifiable error

Note: Reading the bq2092 after an error clears the error code.

Table 8. Status Bits

Alarm Bits		
Bit Name	**Set When:**	**Reset When:**
OVER_CHARGE_ALARM	bq2092 detects over-temperature or ΔT/Δt. (**Note: valid charge termination**).	A discharge occurs or when ΔT/Δt, or over-temperature, ceases during charge.
TERMINATE_CHARGE_ALARM	bq2092 detects over-current, over-voltage, over-temperature, or ΔT/Δt conditions exist during charge. Charging current is set to zero, indicating a charge suspend.	A discharge occurs or when all conditions causing the event cease.
ΔT/Δt_ALARM	bq2092 detects the rate-of-temperature increase is above the programmed value (valid termination)	The temperature rise falls below the programmed rate.
OVER_TEMP_ALARM	bq2092 detects that its internal temperature is greater than the programmed value (valid termination).	Internal temperature falls below 50°C.
TERMINATE_DISCHARGE_ALARM	bq2092 determines that it has supplied all the charge that it can without being damaged (EDVF).	$V_{BAT} > V_{EDVF}$ signifying that the battery has reached a state of charge sufficient for it to once again safely supply power.
REMAINING_CAPACITY_ALARM	bq2092 detects that the RemainingCapacity() is less than that set by the RemainingCapacity() function.	Either the value set by the RemainingCapacityAlarm() function is lower than the Remaining Capacity() or the RemainingCapacity() is increased by charging.
REMAINING_TIME_ALARM	bq2092 detects that the estimated remaining time at the present discharge rate is less than that set by the RemainingTimeAlarm() function.	Either the value set by the RemainingTimeAlarm() function is lower than the AverageTimeToEmpty() or a valid charge is detected.
Status Bits		
Bit Name	**Set When:**	**Reset When:**
INITIALIZED	bq2092 is set when the bq2092 has reached a full or empty state.	Battery detects that power-on or user-initiated reset has occurred.
DISCHARGING	bq2092 determines that it is not being charged.	Battery detects that it is being charged.
FULLY_CHARGED	bq2092 determines a valid charge termination. RM will then be set to full charge percentage if necessary.	RM discharges below the full charge percentage
FULLY_DISCHARGED	bq2092 determines that it has supplied all the charge that it can without being damaged (that is, continued use will result in permanent capacity loss to the battery)	RelativeStateOfCharge is greater than or equal to 20%

Table 9. Example Register Contents

Description	EEPROM Address		EEPROM Hex Contents		Example Values	Notes
	Low Byte	High Byte	Low Byte	High Byte		
Design Capacity	0x00	0x01	08	07	1800mAh	This sets the initial full charge battery capacity stored in FCC. FCC is updated with the actual full to empty discharge capacity after a valid discharge from RM = FCC to Voltage() = EDV1.
Initial Battery Voltage	0x02	0x03	30	2a	10800mV	This register is used to set the battery voltage on reset.
Fast charging current	0x04	0x05	08	07	1800mA	This register is used to set the fast charge current for the Smart Charger.
Fast charging voltage	0x06	0x07	c4	3b	15300mV	This register is used to set the fast charge voltage for the Smart Charger.
Remaining Capacity Alarm	0x08	0x09	b4	00	180mAh	This value represents the low capacity alarm value.
FLAGS1	0x0a		10			FLAGS1 should be set to 10h before pack shipment to inhibit undesirable writes to the bq2092. (WRINH = 1.)
FLAGS2	0x0b		90		Li-Ion = b0h NiMH = 90h	See FLAGS2 register for the bit description and the proper value for programming FLAGS2. Selects relative display mode, selects NiMH compensation factors, and enables bq2092 Smart Charger control.
Current Measurement Gain[1]	0x0c	0x0d	ee	02	37.5/.05	The current gain measurement and current integration gain are related and defined for the bq2092 current measurement. 0x0c = 37.5/sense resistor value in ohms.
EDV1	0x0e	0x0f	16	db	9450mV (1.05V/cell)	The value programmed is the two's complement of the threshold voltage in mV.
EDVF	0x10	0x11	d8	dc	9000mV (1.0V/cell)	The value programmed is the two's complement of the threshold voltage in mV.

Note: 1. Can be adjusted to calibrate the battery pack.

Table 9. Example Register Contents (Continued)

Description	EEPROM Address		EEPROM Hex Contents		Example Values	Notes
	Low Byte	High Byte	Low Byte	High Byte		
Temperature Offset[1]	0x12		32		5.0°C	The default value is 0x80 (12.8° + nominal value). Actual temp (20°C) = Nominal temp. (15°C) - temp. offset (5°C) where temperature determined by the bq2092 can be adjusted from 0° to 25.5° (Temperature offset (0-255) * 0 .1) + nominal value temp.
Maximum Charge Temperature, ΔTemp.	0x13		87		MaxT = 61.2°C (74 - (8 * 1.6)) ΔT = 3°C ((7*2) + 16)/10	Maximum charge temperature is 74 - (mt x 1.6)°C (mt = upper nibble). The ΔT step is (dT*2+16)/10°C (dT = lower nibble).
Self-Discharge Rate	0x14		dd		1.5%	This packed field is the two's complement of 52.73/x, where x = %/day is the self-discharge rate desired at room temperature.
Digital Filter	0x15		96		0.3mV	This field is used to set the digital magnitude filter as described in Table 2.
Current Integration Gain[1]	0x16	0x17	40	00	3.2/0.05	This field represents the following: 3.2/sense resistor in ohms. It is used by the bq2092 to scale the measured voltage values on the SR pin in mA and mAh. This register also compensates for variations in the reported sense resistor value.
Full Charge Percentage	0x18		a0		96% = 60h 2's (60h) = a0h	This packed field is the two's complement of the desired value in RM when the bq2092 determines a full charge termination. If RM is below this value, RM is set to this value. If RM is above this value, then RM is not adjusted.
Charge Compensation	0x19		bd		85% = maintenance comp. 95% = fast charge comp.	This packed value is used to set the fast charge and maintenance charge efficiency for nickel-based batteries. The upper nibble adjusts the maintenance charge compensation; the lower nibble adjusts the fast charge compensation. Maintenance, upper nibble = (eff% * 256 - 128)/8 Fast charge, lower nibble = (eff% * 256 - 192)/4
Battery Voltage Offset[1] (V_{OFF})	0x1a		0a		10mV	This value is used to adjust the battery voltage offset according to the following: Voltage () = (V_{SB} (mV) + V_{OFF}) * Voltage Gain
Voltage Gain[1]	0x1b	0x1c	09	17	9.09	Voltage gain is packed as two units. For example, (R_4 + R_5)/R_4 = 9.09 would be stored as: whole number stored in 0x1b (=09h) and the decimal component stored in 0x1c as 256 x 0.09 = 23.
Serial Number	0x1d	0x1e	12	27	10002	This contains the optional pack serial number.

Table 9. Example Register Contents (Continued)

Description	EEPROM Address		EEPROM Hex Contents		Example Values	Notes
	Low Byte	High Byte	Low Byte	High Byte		
Hold-off Timer/ ΔTime	0x1f		07		320 s hold-off 180 s Δtime	Hold-off time is 20 s * the two's complement of the upper nibble value. ΔT is 20 s * the two's complement of the lower nibble value.
Charge Cycle Count	0x20	0x21	00	00	0	This field contains the charge cycle count and should be set to zero for a new battery.
Maintenance Charge Current	0x22	0x23	64	00	100mA	This field contains the desired maintenance current after fast charge termination by the bq2092.
Reserved	0x24	0x31				
Design Voltage	0x32	0x33	30	2a	10800mV	This is nominal battery pack voltage.
Specification Information	0x34	0x35	00	00		This is the default value for this register.
Manufacturer Date	0x36	0x37	a1	20	May 1, 1996 = 8353	Packed per the ManufactureDate description, which represents May 1, 1996 in this example.

Table 10. Example Register Contents (String Data)

String Description	Address	0x X0	0x X1	0x X2	0x X3	0x X4	0x X5	0x X6	0x X7	0x X8	0x X9	0x Xa	0x Xb-Xf
Reserved	0x38-0x3f	00	00	00	00	00	00	00	00	00	00	00	00-00
Manufacturer's Name	0x40-0x4f	09	42 B	45 E	4e N	43 C	48 H	4d M	41 A	52 R	51 Q	00	00-00
Device Name	0x50-0x5f	08	42 B	51 Q	32 2	30 0	39 9	32 2	41 A	33 3	31 1	31 1	00-00
Chemistry	0x60-0x6f	04	4e N	69 I	4d M	48 H	00	00	00	00	00	00	00-00
Manufacturer's Data	0x70-0x7f	04	44 D	52 R	31 1	35 5	00	00	00	00	00	00	00-00

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
REF	Relative to V_{SS}	-0.3	+8.5	V	Current limited by R1 (see Figure 1)
V_{SR}	Relative to V_{SS}	-0.3	+7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2092 application note for details).
T_{OPR}	Operating temperature	0	+70	°C	Commercial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 5.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
E_{VSB}	Battery voltage error relative to SB	-50mV	-	50mV	V	See note

Note: The accuracy of the voltage measurement may be improved by adjusting the battery voltage offset and gain, stored in external EEPROM. For proper operation, V_{CC} should be 1.5V greater than V_{SB}.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	5.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V
		-	120	180	µA	V_{CC} = 4.25V
		-	170	250	µA	V_{CC} = 5.5V
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	$0 < V_{SB} < V_{CC}$
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	$V_{DISP} = V_{SS}$
I_{LVOUT}	V_{OUT} output leakage	-0.2	-	0.2	µA	EEPROM off
V_{SR}	Sense resistor input	-0.3	-	2.0	V	$V_{SR} < V_{SS}$ = discharge; $V_{SR} > V_{SS}$ = charge
R_{SR}	SR input impedance	10	-	-	MΩ	$-200mV < V_{SR} < V_{CC}$
V_{IH}	Logic input high	0.5 * V_{CC}	-	V_{CC}	V	SCL, SDA
		1.4	-	5.5	V	SCC, SCD
V_{IL}	Logic input low	0	-	0.3 * V_{CC}	V	SCL, SDA
		-0.5		0.6	V	SCC, SCD
V_{OL}	Data, clock output low	-	-	0.4	V	I_{OL}=350µA, SDA, SCD
I_{OL}	Sink current	100	-	350	µA	V_{OL}≤0.4V, SDA, SCD
V_{OLSL}	SEG_X output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, I_{OLS} ≤ 1.75mA SEG_1–SEG_4
V_{OLSH}	SEG_X output low, high V_{CC}	-	0.4	-	V	V_{CC} = 5.5V, I_{OLS} ≤ 11.0mA SEG_1–SEG_4
V_{OHVL}	V_{OUT} output, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{VOUT} = -5.25mA
V_{OHVH}	V_{OUT} output, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} = 5.5V, I_{VOUT} = -33.0mA
I_{VOUT}	V_{OUT} source current	-33	-	-	mA	At $V_{OHVH} = V_{CC}$ - 0.6V
I_{OLS}	SEG_X sink current	-	-	11.0	mA	At V_{OLSH} = 0.4V

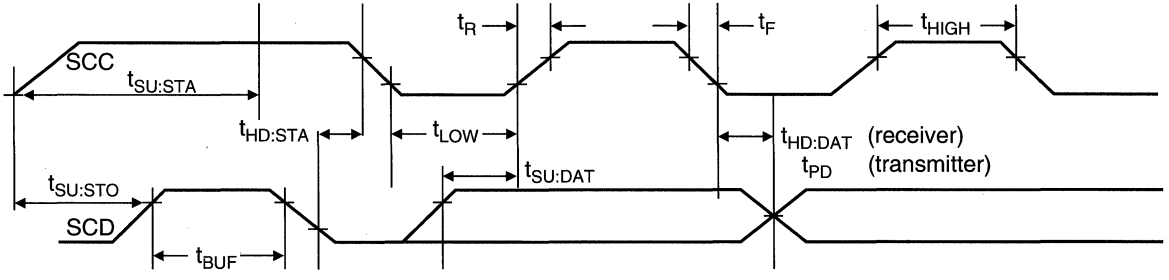
Note: All voltages relative to V_{SS}.

AC Specifications

Symbol	Parameter	Min	Max	Units	Notes
F_{SMB}	SMBus operating frequency	10	100	KHz	
T_{BUF}	Bus free time between stop and start condition	4.7		µs	
$T_{HD:STA}$	Hold time after (repeated) start condition	4.0		µs	
$T_{SU:STA}$	Repeated start condition setup time	250		ns	SCD
		4.7		µs	External Memory
$T_{SU:STO}$	Stop condition setup time	4.0		µs	
$T_{HD:DAT}$	Data hold time	1		µs	
$T_{SU:DAT}$	Data setup time	250		ns	
T_{EXT1}	Data buffering time addresses		40	ms	0x19, 0x1a, 0x1b
T_{EXT2}	String buffering time addresses 0x20-0x23 per character		15	ms	40ms for first character
T_{PD}	Data output delay time	300	3500	ns	External memory only. See Note.
T_{LOW}	Clock low period	4.7		µs	
T_{HIGH}	Clock high period	4.0		µs	
T_F	Clock/Data fall time		300	ns	
T_R	Clock/data rise time		1000	ns	

Note: The external memory must provide this internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Bus Timing Data



TD209201.eps

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	21	Correction in the Self-Discharge Rate EEPROM Hex contents	Was: f0 Is: df
1	21	Correction in the Self-Discharge Rate example values	Was: 0.15C Is: 1.5%
2	3	Updated application diagram	
2	5	Added VSB should not exceed 2.4V	
2	12	Clarified operation of bits 13 and 14 in BatteryMode()	
2	13	Clarified invalid data indication in RunTimeToEmpty()	
2	13	Clarified invalid data indication in AverageTimeToEmpty()	
2	21	Update formula for voltage divider in Voltage Gain.	

Note: Change 1 = Nov. 1997 B changes from April 1997.
Change 2 = June 1999 C changes from Nov. 1997 B.

Ordering Information

bq2092

Temperature Range:
blank = Commercial (-20 to +70°C)

Package Option:
SN = 16-pin narrow SOIC

Device:
bq2092 Gas Gauge IC With SMBus-Like Interface

UNITRODE

bq2945

Gas Gauge IC with SMBus Interface

Features

- Provides accurate measurement of available charge in NiCd, NiMH, and Li-Ion batteries
- Supports SBS v1.0 data set and two-wire interface
- Two programmable general purpose output ports for added flexibility
- Designed for battery pack integration
  - Low operating current
  - Complete circuit can fit on less than ¾ square inch of PCB space
- Supports SBS charge control commands for NiCd, NiMH, and Li-Ion
- Drives a five-segment LED display for remaining capacity indication
- 16-pin narrow SOIC

General Description

The bq2945 Gas Gauge IC With SMBus Interface is intended for battery-pack or in-system installation to maintain an accurate record of available battery charge. The bq2945 directly supports capacity monitoring for NiCd, NiMH, and Li-Ion battery chemistries.

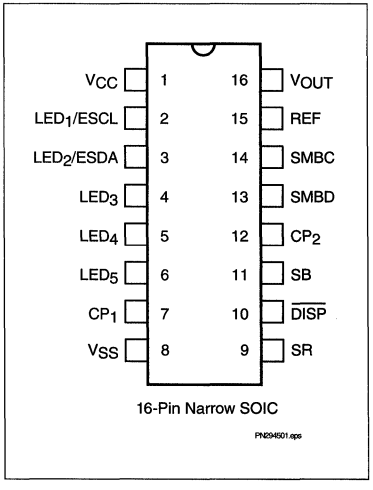
The bq2945 uses the System Management Bus v1.0 (SMBus) protocol and supports the Smart Battery Data (SBData) commands. The bq2945 also supports the SBData charge control functions. Battery state-of-charge, remaining capacity, remaining time, and chemistry are available over the serial link. Battery-charge state can be directly indicated using a five-segment LED display to graphically depict battery full-to-empty in 20% increments.

The bq2945 estimates battery self-discharge based on an internal timer and temperature sensor and user-programmable rate information stored in external EEPROM. The bq2945 also automatically recalibrates or "learns" battery capacity in the full course of a discharge cycle from full to empty.

The bq2945 may operate directly from three nickel chemistry cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide V_{CC} for other battery cell configurations.

An external EEPROM programs initial values into the bq2945 and is necessary for proper operation.

Pin Connections



16-Pin Narrow SOIC

Pin Names

V_{CC}	3.0–6.5V
LED_1	LED segment 1/ EEPROM clock
LED_2	LED segment 2/ EEPROM data
LED_3	LED segment 3
LED_4	LED segment 4
LED_5	LED segment 5
CP_1	Control pin 1
V_{SS}	System ground
SR	Sense resistor input
$\overline{DISP}$	Display control input
SB	Battery sense input
CP_2	Control pin 2
SMBD	SMBus data input/output
SMBC	SMBus clock
REF	Voltage reference output
V_{OUT}	EEPROM supply output

Pin Descriptions

V_{CC} **Supply voltage input**

LED_1–LED_5 **LED display segment outputs**

Each output may drive an external LED.

ESCL **Serial memory clock**

Output used to clock the data transfer between the bq2945 and the external nonvolatile configuration memory.

ESDA **Serial memory data and address**

Bidirectional pin used to transfer address and data to and from the bq2945 and the external nonvolitile configuration memory.

CP_1–CP_2 **Control pins 1 and 2**

These open-drain outputs can be controlled by an SMBus command from the host. CP_2 can also act as a digital input.

V_{SS} **Ground**

SR **Sense resistor input**

The voltage drop (V_{SR}) across pins SR and V_{SS} is monitored and integrated over time to interpret charge and discharge activity. The SR input is connected to the sense resistor and the negative terminal of the battery. $V_{SR} < V_{SS}$ indicates discharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2945 is $V_{SR} + V_{OS}$. (See Table 3.)

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ floating allows the LED display to be active during charge if the rate is greater than 100mA. $\overline{DISP}$ low activates the display for 4 seconds.

SB **Secondary battery input**

Monitors the pack voltage through a high-impedance resistor divider network. The pack voltage is reported in the SBD register function Voltage (0x09) and is monitored for end-of-discharge voltage and charging voltage parameters.

SMBD **SMBus data**

Open-drain bidirectional pin used to transfer address and data to and from the bq2945.

SMBC **SMBus clock**

Open-drain bidirectional pin used to clock the data transfer to and from the bq2945.

REF **Reference output for regulator**

REF provides a reference output for an optional FET-based micro-regulator.

V_{OUT} **Supply output**

Supplies power to the external EEPROM configuration memory.

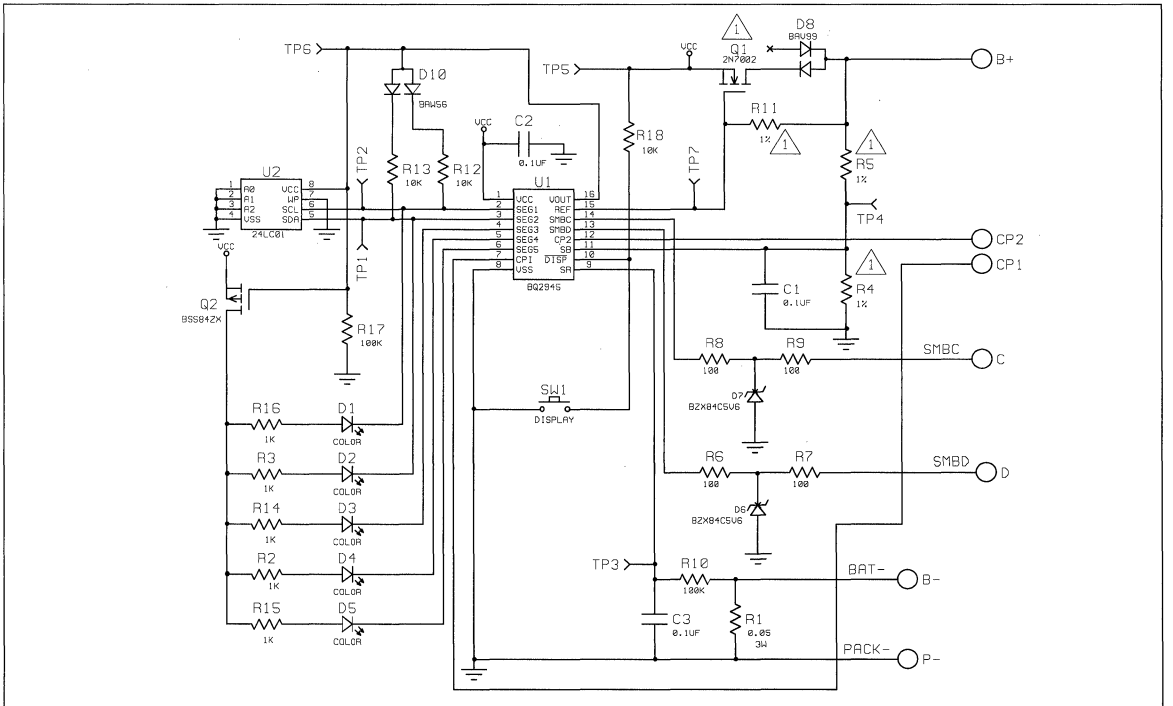
Functional Description

General Operation

The bq2945 determines battery capacity by monitoring the amount of charge put into or removed from a rechargeable battery. The bq2945 measures discharge and charge currents, estimates self-discharge, and monitors the battery for low-battery voltage thresholds. The charge is measured by monitoring the voltage across a small-value series sense resistor between the battery's negative terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2945 using the LED capacity display, the serial port, and an external EEPROM for battery pack programming information. The bq2945 must be configured and calibrated for the battery-specific information to ensure proper operation. Table 1 outlines the configuration information that must be programmed in the EEROM.

An internal temperature sensor eliminates the need for an external thermistor—reducing cost and components. An internal, temperature-compensated timebase eliminates the need for an external resonator, further reducing cost and components. The entire circuit in Figure 1 can occupy less than ¾ square inch of board space.



See Chart 1 for resistor values and Q1 FET selection

Chart 1

	No. of Cells	Q1	R4	R5	R11
Li-Ion	2	BSS138	100K	301K	604K
	3	BSS138	100K	499K	806K
	4	2N7002	100K	698K	604K
NiMH	6	BSS138	100K	499K	499K
	8	BSS138	100K	698K	806K
	9	2N7002	100K	806K	499K
	10	2N7002	100K	909K	604K
	12	2N7002	86.5K	909K	909K

Notes: R4, R5, and R11 values depend on the battery voltage. R12 and R13 nominal values must be 10k

Figure 1. Battery Pack Application Diagram—LED Display

3/30

Table 1. Configuration Memory Map

Parameter Name	Address	Description	Length	Units
EEPROM length	0x00	Number of EEPROM data locations must = 0x64	8 bits	NA
EEPROM check1	0x01	EEPROM data integrity check byte must = 0x5b	8 bits	NA
Remaining time alarm	0x02/0x03	Sets RemainingTimeAlarm (0x02)	16 bits	minutes
Remaining capacity alarm	0x04/0x05	Sets RemainingCapacityAlarm (0x01)	16 bits	mAh
Reserved	0x06/0x07	Reserved for future use	16 bits	NA
Initial charging current	0x08/0x09	Sets the initial charging current	16 bits	mA
Charging voltage	0x0a/0x0b	Sets ChargingVoltage (0x15)	16 bits	mV
Battery status	0x0c/0x0d	Initializes BatteryStatus (0x16)	16 bits	NA
Cycle count	0x0e/0x0f	Initializes and stores CycleCount (0x17)	16 bits	cycles
Design capacity	0x10/0x11	Sets DesignCapacity (0x18)	16 bits	mAh
Design voltage	0x12/0x13	Sets DesignVoltage (0x19)	16 bits	mV
Specification information	0x14/0x15	Programs SpecificationInfo (0x1a)	16 bits	NA
Manufacturer date	0x16/0x17	Programs ManufactureDate (0x1b)	16 bits	NA
Serial number	0x18/0x19	Programs SerialNumber (0x1c)	16 bits	NA
Fast-charging current	0x1a/0x1b	Sets ChargingCurrent (0x14)	16 bits	mA
Maintenance-charge current	0x1c/0x1d	Sets the trickle current request	16 bits	mA
Reserved	0x1e/0x1f	Reserved must = 0x0000	16 bits	mAh
Manufacturer name	0x20-0x2b	Programs ManufacturerName (0x20)	96 bits	NA
Current integration gain	0x2c/0x2d	Programs the sense resistor scale	16 bits	NA
Reserved	0x2e/0x2f	Reserved for future use	16 bits	NA
Device name	0x30-0x37	Programs DeviceName (0x21)	64 bits	NA
Li-Ion taper current	0x38/0x39	Sets the upper limit of the taper current for charge termination	16 bits	mA
Maximum overcharge limit	0x3a/0x3b	Sets the maximum amount of overcharge	16 bits	NA
Reserved	0x3c	Reserved must = 0x00	8 bits	NA
Access protect	0x3d	Locks commands outside of the SBS data set	8 bits	NA
FLAGS1	0x3e	Initializes FLAGS1	8 bits	NA
FLAGS2	0x3f	Initializes FLAGS2	8 bits	NA
Device chemistry	0x40-0x47	Programs DeviceChemistry (0x22)	64 bits	NA
Battery voltage offset	0x48	Voltage calibration value	8 bits	NA
Temperature offset	0x49	Temperature calibration value	8 bits	NA
Maximum temperature and ΔT step	0x4a	Sets the maximum charge temperature and the ΔT step for $\Delta T/\Delta t$ termination	8 bits	NA

Table 1. Configuration Memory Map (Continued)

Parameter Name	Address	Description	Length	Units
Charge efficiency	0x4b	Sets the high/low charge rate efficiencies	8 bits	NA
Full-charge percentage	0x4c	Sets the percent at which the battery is considered fully charged	8 bits	NA
Digitial filter	0x4d	Sets the minimum charge/discharge threshold	8 bits	NA
Reserved	0x4e	Reserved for future use	8 bits	NA
Self-discharge rate	0x4f	Sets the battery's self-discharge rate	8 bits	NA
Manufacturer data	0x50-0x55	Programs ManufacturerData (0x23)	48 bits	NA
Voltage gain1	0x56/0x57	Battery divider calibration value	16 bits	NA
Reserved	0x58-0x59	Reserved	16 bits	NA
Current measurement gain	0x5a/0x5b	Sense resistor calibration value	16 bits	NA
End of discharge voltage1	0x5c/0x5d	Sets EDV1	16 bits	NA
End of discharge voltage final	0x5e/0x5f	Sets EDVF	16 bits	NA
Full-charge capacity	0x60/0x61	Initializes and stores FullChargeCapacity (0x10)	16 bits	mAh
Δt step	0x62	Sets the Δt step for $\Delta T/\Delta t$ termination	8 bits	NA
Hold-off time	0x63	Sets $\Delta T/\Delta t$ hold-off timer	8 bits	NA
EEPROM check 2	0x64	EEPROM data integrity check byte must = 0xb5	8 bits	NA
Reserved	0x65-0x7f	Reserved for future use		NA

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2945 monitors the battery potential through the SB pin. The voltage potential is determined through a resistor-divider network per the following equation:

$$\frac{R_5}{R_4} = \frac{MBV}{2.25} - 1$$

where MBV is the maximum battery voltage, R_5 is connected to the positive battery terminal, and R_4 is connected to the negative battery terminal. R_5/R_4 should be rounded to the next higher integer. R_5 and R_4 should be sized so that the voltage at the SB pin (V_{SB}) should never exceed 2.4V.

The battery voltage is monitored for the end-of-discharge voltages (EDV1 and EDVF) and for alarm warning conditions. EDV threshold levels are used to determine when the battery has reached an "empty" state. The bq2945 generates an alarm warning when the battery voltage exceeds the maximum charging voltage by 5% or if the voltage is below EDVF. The battery voltage gain, the two EDV thresholds, and the charging voltage are programmable in the EEPROM.

If V_{SB} is below either of the two EDV thresholds, the associated flag is latched and remains latched, independent of V_{SB}, until the next valid charge.

EDV monitoring may be disabled under certain conditions. If the discharge current is greater than approximately 6A, EDV monitoring is disabled and resumes after the current falls below 6A.

Reset

The bq2945 is reset when first connected to the battery pack. On power-up, the bq2945 initializes and reads the EEPROM configuration memory. The bq2945 can also be reset with a command over the SMBus. The software reset sequence is the following: (1) write MaxError (0x0c) to 0x0000; (2) write the reset register (0x64) to 0x8009. A software reset can only be performed if the bq2945 is in an unlocked state as defined by the value in location 0x3d of the EEPROM (EE 0x3d) on power-up.

Temperature

The bq2945 monitors temperature sensing using an internal sensor. The temperature is used to adapt charge and self-discharge compensations as well as to monitor for maximum temperature and $\Delta T/\Delta t$ during a bq2945 controlled charge. Temperature may also be accessed over the SMBus with command 0x08.

Layout Considerations

The bq2945 measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally, in reference to Figure 1:

- The capacitors (C1 and C2) should be placed as close as possible to the SB and V_{CC} pins, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor capacitor (C3) should be placed as close as possible to the SR pin.
- The bq2945 should be in thermal contact with the cells for optimum temperature measurement.
- An optional zener (D9) may be necessary to ensure that V_{CC} is not above the maximum rating during operation.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2945. The bq2945 accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge currents are compensated for temperature and state-of-charge of the battery. Self-discharge is temperature-compensated.

The main counter, RemainingCapacity (RM), represents the available battery capacity at any given time. Battery charging increments the RM register, whereas battery discharging and self-discharge decrement the RM register and increment the internal Discharge Count Register (DCR).

The Discharge Count Register is used to update the FullChargeCapacity (FCC) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2945 adapts its capacity determination based on the actual conditions of discharge.

The battery's initial full capacity is set to the value stored in EE 0x60-0x61. Until FCC is updated, RM counts up to, but not beyond, this threshold during subsequent charges.

1. **FullChargeCapacity or learned-battery capacity:**

   FCC is the last measured discharge capacity of the battery. On initialization (application of V_{CC} or reset), FCC is set to the value stored in the EEPROM. During subsequent discharges, FCC is updated with the

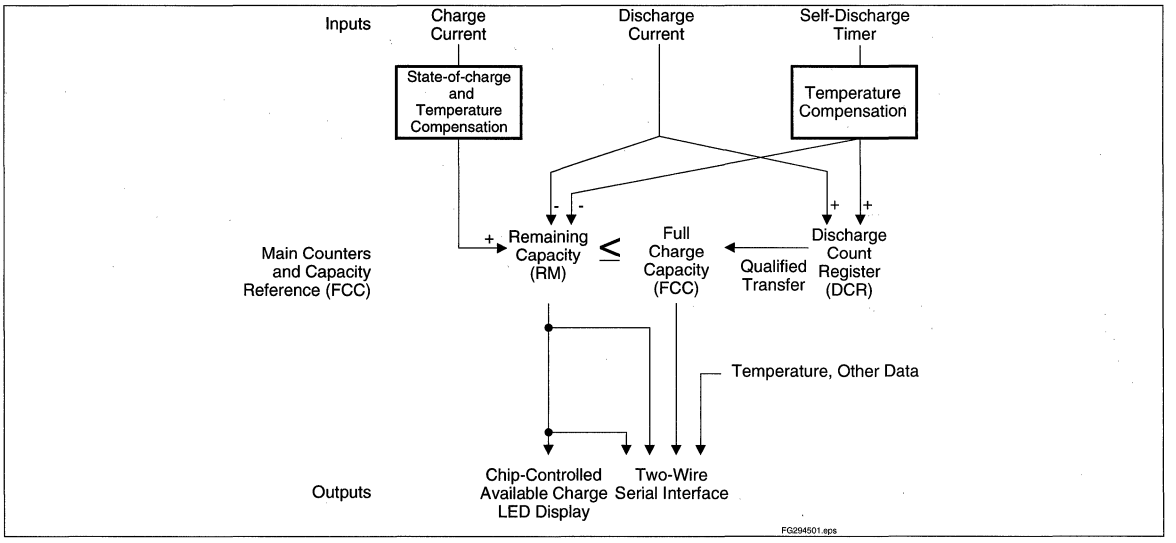


Figure 2. Operational Overview

latest measured capacity in the Discharge Count Register, representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the FCC register. Once updated, the bq2945 writes the new FCC to the EEPROM. The FCC also serves as the 100% reference threshold used by the relative state-of-charge calculation and display.

2. **DesignCapacity (DC):**

   The DC is the user-specified battery capacity and is programmed from external EEPROM. The DC also provides the 100% reference for the absolute display mode.

3. **RemainingCapacity (RM):**

   RM counts up during charge to a maximum value of FCC and down during discharge and self-discharge to 0. RM is set to 000Ah after the EDV1 threshold has been reached and a valid charge has been detected. To prevent overstatement of charge during periods of overcharge, RM stops incrementing when RM = FCC. RM may optionally be written to a user-defined value when fully charged if the battery pack is under bq2945 charge control. On initialization, RM is set to the value stored in EE 0x1e—0x1f.

4. **Discharge Count Register (DCR):**

   The DCR counts up during discharge independent of RM and can continue increasing after RM has decremented to 0. Prior to RM = 0 (empty battery), both discharge and self-discharge increment the DCR. After RM = 0, only discharge increments the DCR. The DCR resets to 0 when RM = FCC. The DCR does not roll over but stops counting when it reaches FFFFh.

   The DCR value becomes the new FCC value on the first charge after a qualified discharge to EDV1. A qualified discharge to EDV1 occurs if all of the following conditions exist:

   - No valid charge initiations (charges greater than 10mAh), where $V_{SRO} > +V_{SRD}$ occurred during the period between RM = FCC and EDV1 detected.
   - The self-discharge count is not more than 256mAh.
   - The temperature is ≥ 273°K (0°C) when the EDV1 level is reached during discharge.

   The valid discharge flag (VDQ) in FLAGS1 indicates whether the present discharge is valid for an FCC update. FCC cannot be reduced by more than 256mAh during any single cycle.

Charge Counting

Charge activity is detected based on a positive voltage on the SR input. If charge activity is detected, the bq2945 increments RM at a rate proportional to V_{SRO} and, if enabled, activates an LED display. Charge actions increment the RM after compensation for charge state and temperature.

The bq2945 determines charge activity sustained at a continuous rate equivalent to $V_{SRO} > +V_{SRD}$. **A valid charge equates to sustained charge activity greater than 10 mAh**. Once a valid charge is detected, charge threshold counting continues until V_{SRO} falls below V_{SRD}. V_{SRD} is a programmable threshold as described in the Digital Magnitude Filter section.

Discharge Counting

All discharge counts where $V_{SRO} < -V_{SRD}$ cause the RM register to decrement and the DCR to increment. V_{SRD} is a programmable threshold as described in the Digital Magnitude Filter section.

Self-Discharge Estimation

The bq2945 continuously decrements RM and increments DCR for self-discharge based on time and temperature. The bq2945 self-discharge estimation rate is programmed in EE 0x4f and can be set from 0 to 25% per day for 20–30°C. This rate doubles every 10°C from 30°C to 70°C and halves every 10°C from 20°C to 0°C.

Charge Control

The bq2945 supports SBS charge control by broadcasting the ChargingCurrent and the ChargingVoltage to the Smart Charger address. The bq2945 broadcasts charging commands every 10 seconds; the broadcasts can be disabled by writing bit 14 of BatteryMode to 1. On reset, the initial charging current broadcast to the charger is set to the value programmed in EE 0x08-0x09. The bq2945 updates the value used in the charging current broadcasts based on the battery's state of charge, voltage, and temperature.

The bq2945 internal charge control is compatible with nickel-based and Li-Ion chemistries. The bq2945 uses current taper detection for Li-Ion primary charge termination and $\Delta T/\Delta t$ for nickel based primary charge termination. The bq2945 also provides a number of safety terminations based on battery capacity, voltage, and temperature.

Current Taper

For Li-Ion charge control, the ChargingVoltage must be set to the desired pack voltage during the constant voltage charge phase. The bq2945 detects a current taper termination when it measures the pack voltage to be within 128mV of the requested charging voltage and when the AverageCurrent is between the programmed threshold in EE 0x38—0x39 and 100 mA for at least 40s.

$\Delta T/\Delta t$

The $\Delta T/\Delta t$ used by the bq2945 is programmable in both the temperature step (1.6°C–4.6°C) and time step (20 seconds–320seconds). Typical settings for 1°C/min include 2°C over 120 seconds and 3°C over 180 seconds. Longer times are required for increased slope resolution.

$\frac{\Delta T}{\Delta t}$ is set by the formula: $\frac{\Delta T}{\Delta t} =$

$$\frac{[(\text{lower nibble of EE 0x4a}) * 2 + 16] / 10}{[2^{s}(\text{EE 0x62}) * 20]} \left[\frac{^{\circ}C}{s}\right]$$

In addition to the $\Delta T/\Delta t$ timer, there is a hold-off timer, which starts when the battery is being charged at more than 255mA and the temperature is above 25°C. Until this timer expires, $\Delta T/\Delta t$ is suspended. If the temperature falls below 25°C, or if charging current falls below 255mA, the timer is reset and restarts only if these conditions are once again within range. The hold-off time is programmed in EE 0x63.

Charge Termination

Once the bq2945 detects a valid charge termination, the Fully_Charged, Terminate_Charge_Alarm, and the Over_Charged_Alarm bits are set in BatteryStatus, and the requested charge current is set to zero. Once the terminating conditions cease, the Terminate_Charge_Alarm and the Over_Charged_Alarm are cleared, and the requested charging current is set to the maintenance rate. The bq2945 requests the maintenance rate until RM falls below 95% of full-charge percentage. Once this occurs, the Fully_Charged bit is cleared, and the requested charge current and voltage are set to the fast-charge rate.

Bit 4 (CC) in FLAGS2 determines whether RM is modified after a $\Delta T/\Delta t$ or current taper termination occurs. If CC = 1, RM may be set from 0 to 100% of the FullChargeCapacity as defined in EE 0x4c. If RM is below the full-charge percentage, RM is set to the full-charge percentage of FCC. If RM is above the full-charge percentage, RM is not modified.

Charge Suspension

The bq2945 may temporarily suspend charge if it detects a charging fault. The charging faults include the following conditions:

- **Maximum Overcharge:** If charging continues for more than the programmed maximum overcharge limit as defined in EE 0x3a—0x36 beyond RM=FCC, the Fully_Charged bit is set, and the requested charging current is set to the maintenance rate.
- **Overvoltage:** An over-voltage fault exists when the bq2945 measures a voltage more than 5% above the ChargingVoltage. When the bq2945 detects an overvoltage condition, the requested charge current is set to 0 and the Terminate_Charge_Alarm bit is set in Battery Status. The alarm bit is cleared when

the current drops below 256mA and the voltage is less than 105% of ChargingVoltage.

- **Overcurrent:** An overcurrent fault exists when the bq2945 measures a charge current more than 25% above the ChargingCurrent. If the ChargingCurrent is less than 1024mA, an overcurrent fault exists if the charge current is more than 256mA above the ChargingCurrent. When the bq2945 detects an overcurrent condition, the requested charge current is set to 0 and the Terminate_Charge_Alarm bit is set in Battery Status. The alarm bit is cleared when the current drops below 256mA.
- **Maximum Temperature**: When the battery temperature exceeds the programmed maximum temperature, the requested charge current is set to zero and the Over_Temp_Alarm and the Terminate_Charge_Alarm bits are set in Battery Status. The alarm bits are cleared when the temperature drops below 50°C.
- **Low Temperature:** When the battery temperature is less than 0°C, the requested charge current is set to the maintenance rate. Once the temperature is above 5°C, the requested charge current is set to the fast rate.
- **Undervoltage:** When the battery voltage is below the EDVF threshold, the requested charge current is set to the maintenance rate. Once the voltage is above EDVF, the requested charge current is set to the fast rate.

Count Compensations

Charge activity is compensated for temperature and state-of-charge before updating the RM and/or DCR. Self-discharge estimation is compensated for temperature before updating RM or DCR.

Charge Compensation

Charge efficiency is compensated for state-of-charge, temperature, and battery chemistry. The charge efficiency is adjusted using the following equations:

$$1.)\,RM = RM * (Q_{EFC} - Q_{ET})$$

where RelativeStateOfCharge < FullChargePercentage, and Q_{EFC} is the programmed fast-charge efficiency varying from 0.75 to 1.0.

$$2.)\,RM = RM * (Q_{ETC} - Q_{ET})$$

where RelativeStateOfCharge ≥ FullChargePercentage and Q_{ETC} is the programmed maintenance (trickle) charge efficiency varying from 0.75 to 1.0.

Q_{ET} is used to adjust the charge efficiency as the battery temperature increases according to the following:

$Q_{ET} = 0$ if $T < 30°C$

$Q_{ET} = 0.02$ if $30°C \le T < 40°C$

$Q_{ET} = 0.05$ if $T \ge 40°C$

Q_{ET} is 0 over the entire temperature range for Li-Ion.

Digital Magnitude Filter

The bq2945 has a programmable digital filter to eliminate charge and discharge counting below a set threshold, V_{SRD}. Table 2 shows typical digital filter settings. The proper digital filter setting can be calculated using the following equation.

$$DMF = \frac{45}{V_{SRD}}$$

Table 2. Typical Digital Filter Settings

DMF	DMF Hex.	V_{SRD} (mV)
75	4B	0.60
100	64	0.45
150	96	0.30
175	AF	0.26
200	C8	0.23

Error Summary

Capacity Inaccurate

The FCC is susceptible to error on initialization or if no updates occur. On initialization, the FCC value includes the error between the design capacity and the actual capacity. This error is present until a qualified discharge occurs and FCC is updated (see the DCR description). The other cause of FCC error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity. Periodic qualified discharges from full to empty will minimize errors in FCC.

Current-Sensing Error

Table 3 illustrates the current-sensing error as a function of V_{SR}. A digital filter eliminates charge and discharge counts to the RM register when $-V_{SRD} < V_{SRO} < +V_{SRD}$.

Display

The bq2945 can directly display capacity information using low-power LEDs. The bq2945 displays the battery charge state in either absolute or relative mode. In relative mode, the battery charge is represented as a percentage of the FCC. Each LED segment represents 20% of the FCC.

Table 3. bq2945 Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
V_{OS}	Offset referred to V_{SR}	± 75	± 150	µV	$\overline{DISP}$ = V_{CC}.
INL	Integrated non-linearity error	± 1	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 0.5	± 1	%	Measurement repeatability given similar operating conditions.

In absolute mode, each segment represents a fixed amount of charge, 20% of the DesignCapacity. As the battery wears out over time, it is possible for the FCC to be below the design capacity. In this case, all of the LEDs may not turn on in absolute mode, representing the reduction in the actual battery capacity.

When $\overline{DISP}$ is tied to V_{CC}, the LED_{1-5} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active whenever the bq2945 detects a charge rate of 100mA or more. When pulled low, the segment outputs become active immediately for a period of approximately 4 seconds. The $\overline{DISP}$ pin must be returned to float or V_{CC} to reactivate the display.

LED_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below EDV1 (EDV1 = 1), indicating a low-battery condition. V_{SB} below EDVF (EDVF = 1) disables the display output.

Microregulator

The bq2945 can operate directly from three nickel chemistry cells. To facilitate the power supply requirements of the bq2945, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2945 can be inexpensively built using a 2N7002 or BSS138 FET and an external resistor. (See Figure 1.) The value of R11 depends on the battery pack's nominal voltage.

Communicating with the bq2945

The bq2945 includes a simple two-pin (SMBC and SMBD) bi-directional serial data interface. A host processor uses the interface to access various bq2945 registers; see Table 4. This method allows battery characteristics to be monitored easily. The open-drain SMBD and SMBC pins on the bq2945 are pulled up by the host system, or may be connected to V_{SS}, if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends the battery address and an eight-bit command byte to the bq2945. The command directs the bq2945 to either store the next data received to a register specified by the command byte or output the data specified by the command byte.

bq2945 Data Protocols

The host system, acting in the role of a Bus master, uses the read word and write word protocols to communicate integer data with the bq2945. (See Figure 3.)

Host-to-bq2945 Message Protocol

The Bus Host communicates with the bq2945 using one of three protocols:

- Read word
- Write word
- Read block

The particular protocol used is a function of the command. The protocols used are shown in Figure 3.

Host-to-bq2945 Messages (see Table 4)

ManufacturerAccess() (0x00)

This function is used to control CP_1 and CP_2. (See Table 7.)

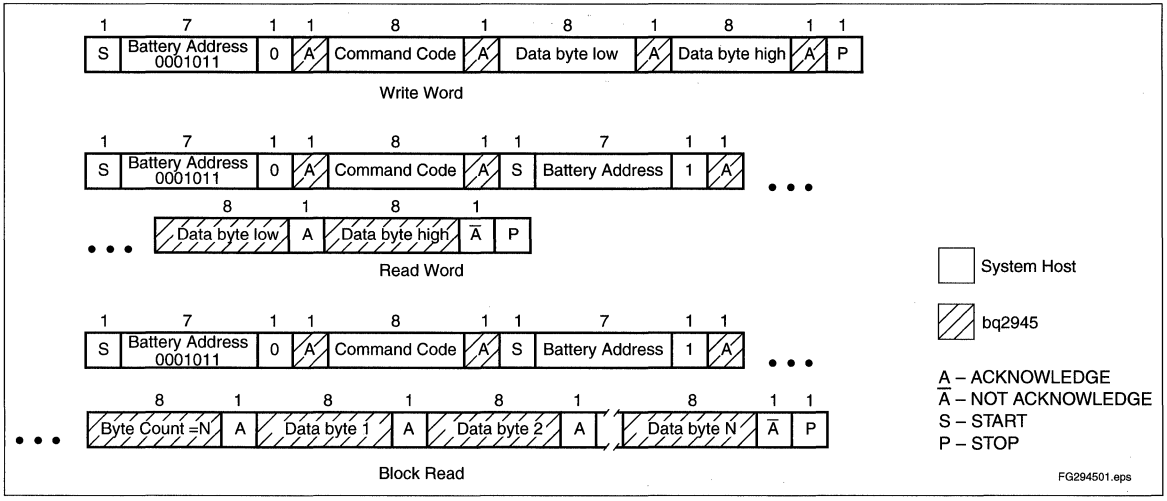


Figure 3. Host Communication Protocols

RemainingCapacityAlarm() (0x01)

This function sets or returns the low-capacity alarm value. When RM falls below the RemainingCapacityAlarm value initialized from the external EEPROM, the Remaining_Capacity_Alarm bit is set in BatteryStatus. The system may alter this alarm during operation.

Input/Output: unsigned integer. This sets/returns the value where the Remaining_Capacity_Alarm bit is set in Battery Status.

Units: mAh

Range: 0 to 65,535mAh

RemainingTimeAlarm() (0x02)

This function sets or returns the low remaining time alarm value. When the AverageTimeToEmpty falls below this value, the Remaining_Time_Alarm bit in BatteryStatus is set. The default value for this register is programmed in EE 0x02-0x03. The system may alter this alarm during operation.

Input/Output: unsigned integer. This sets/returns the value where the Remaining_Time_Alarm bit is set in Battery Status.

Units: minutes

Range: 0 to 65,535 minutes

BatteryMode() (0x03)

This read/write word selects the various battery operational modes. The bq2945 supports the battery capacity information specified in mAh. This function also determines whether the bq2945 charging values are broadcasted to the Smart Battery Charger address.

Writing bit 14 to 1 disables voltage and current Master Mode broadcasts to the Smart Battery Charger. Bit 14 is automatically reset to 0 if SMBC and SMBD = 0 for greater than 2 seconds (i.e. pack removal).

Writing bit 13 to 1 disables all Master Mode broadcasts including alarm messages to the Smart Battery Charger and Host. The bit remains set until overwritten. Programming bit 3 of FLAGS2 in the EEPROM (EE0x3f) initializes this bit to a 1.

Bit 7 is the condition request flag. It is set when the bq2945 is initialized from the EEPROM and reset when a learning cycle has been completed. It is also set to a 1 if CycleCount increases by 32 without a new learning cycle.

AtRate() (0x04)

This read/write word is the first half of a two-function set used to set the AtRate value used in calculations made by the AtRateTimeToFull and AtRateTimeToEmpty.

- When the AtRate value is positive, the AtRateTimeToFull function returns the predicted time to full-charge at the AtRate value of charge.

Table 4. bq2945 Register Functions

Function	Code	Access	Units	Defaults[1]
ManufacturerAccess	0x00	read/write	-	-
Remaning_Capacity_Alarm	0x01	read/write	mAh	E^2
Remaining_Time_Alarm	0x02	read/write	minutes	E^2
BatteryMode	0x03	read/write	bit flag	-
AtRate	0x04	read/write	mA	-
AtRateTimeToFull	0x05	read	minutes	-
AtRateTimeToEmpty	0x06	read	minutes	-
AtRateOK	0x07	read	Boolean	-
Temperature	0x08	read	0.1°K	2930
Voltage	0x09	read	mV	E^2
Current	0x0a	read	mA	0
AverageCurrent	0x0b	read	mA	0
MaxError	0x0c	read	percent	100
RelativeStateOfCharge	0x0d	read	percent	-
AbsoluteStateOfCharge	0x0e	read	percent	-
RemainingCapacity	0x0f	read	mAh	E^2
FullChargeCapacity	0x10	read	mAh	E^2
RunTimeToEmpty	0x11	read	minutes	-
AverageTimeToEmpty	0x12	read	minutes	-
AverageTimeToFull	0x13	read	minutes	-
ChargingCurrent	0x14	read	mA	E^2
ChargingVoltage	0x15	read	mV	E^2
Battery Status	0x16	read	bit flags	E^2
CycleCount	0x17	read	cycle	E^2
DesignCapacity	0x18	read	mAh	E^2
DesignVoltage	0x19	read	mV	E^2
Specification Info	0x1a	read	-	E^2
ManufactureDate	0x1b	read	-	E^2
SerialNumber	0x1c	read	integer	E^2
Reserved	0x1d - 0x1f	-	-	-
ManufacturerName	0x20	read	string	E^2
DeviceName	0x21	read	string	E^2

Note: 1. Defaults after reset or power-up.

Table 4. bq2945 Register Functions (Continued)

Function	Code	Access	Units	Defaults[1]
DeviceChemistry	0x22	read	string	E^2
ManufacturerData	0x23	read	string	E^2
FLAG1 and FLAG2	0x2f	read	bit flags	E^2
End of Discharge Voltage 1 (EDV1)	0x3e	read	-	E^2
End of Discharge Voltage Final (EDVF)	0x3f	read	-	E^2

Note: 1. Defaults after reset or power-up.

- When the AtRate value is negative, the AtRateTimeToEmpty function returns the predicted operating time at the AtRate value of discharge.

  Input/Output: signed integer. AtRate is positive for charge and negative for discharge.

  Units: mA

  Range: -32,768mA to 32,767mA

AtRateTimeToFull() (0x05)

This read-only word returns the predicted remaining time to fully charge the battery at the AtRate value (mA) and is valid only if read immediately after an AtRate command.

Output: unsigned integer. Returns the predicted time to full charge.

Units: minutes

Range: 0 to 65,534min

Granularity: 2 min or better

Invalid Data Indication: 65,535 indicates that the AtRate value is negative.

AtRateTimeToEmpty() (0x06)

This read-only word returns the predicted remaining operating time if the battery is discharged at the AtRate value and is valid only if read immediately after an AtRate command.

Output: unsigned integer. Returns the predicted time to empty.

Units: minutes

Range: 0 to 65,534min

Granularity: 2min or better

Invalid Data Indication: 65,535 indicates that the AtRate value is not negative.

AtRateOK() (0x07)

This read-only word returns a Boolean value that indicates whether or not the EDVF flag has been set.

Boolean: Indicates if the battery can supply additional energy.

Units: Boolean

Range: TRUE ≠ 0, FALSE = 0

Temperature() (0x08)

This read-only word returns the cell-pack's internal temperature.

Output: unsigned integer. Returns the cell temperature in tenths of degrees Kelvin increments.

Units: 0.1°K

Range: 0 to +500.0°K

Granularity: 0.5°K or better

Accuracy: ±3°K after calibration

Voltage() (0x09)

This read-only word returns the cell-pack voltage (mV).

Output: unsigned integer. Returns the battery terminal voltage in mV.

Units: mV

Range: 0 to 65,535mV

Granularity: 0.2% of DesignVoltage

Accuracy: ±1% of DesignVoltage after calibration

Current() (0x0a)

This read-only word returns the current through the battery's terminals (mA).

Output: signed integer. Returns the charge/discharge rate in mA, where positive is for charge and negative is for discharge

Units: mA

Range: 0 to 32,767mA for charge or 0 to –32,768mA for discharge

Granularity: 0.2% of the DesignCapacity or better

Accuracy: ±1% of the DesignCapacity after calibration

AverageCurrent() (0x0b)

This read-only word returns a rolling average of the current through the battery's terminals. The AverageCurrent function returns meaningful values after the battery's first minute of operation.

Output: signed integer. Returns the charge/discharge rate in mA, where positive is for charge and negative is for discharge

Units: mA

Range: 0 to 32,767mA for charge or 0 to –32,768mA for discharge

Granularity: 0.2% of the DesignCapacity or better

Accuracy: ±1% of the DesignCapacity after calibration

MaxError() (0x0c)

Returns the expected margin of error (%) in the state of charge calculation.

Output: unsigned integer. Returns the percent uncertainty for selected information.

Units: %

Range: 0 to 100%

RelativeStateOfCharge() (0x0d)

This read-only word returns the predicted remaining battery capacity expressed as a percentage of FullChargeCapacity (%). **RelativeStateOfCharge is only valid for battery capacities more than 1504mAh and less than 10,400mAh.**

Output: unsigned integer. Returns the percent of remaining capacity.

Units: %

Range: 0 to 100%

Granularity: 1%

Accuracy: ±MaxError after circuit and capacity calibration

AbsoluteStateOfCharge() (0x0e)

This read-only word returns the predicted remaining battery capacity expressed as a percentage of DesignCapacity (%). Note that AbsoluteStateOfCharge can return values greater than 100%. **Absolute StateOfCharge is only valid for battery capacities more than 1504mAh and less than 10,400mAh.**

Output: unsigned integer. Returns the percent of remaining capacity.

Units: %

Range: 0 to 65,535%

Granularity: 1%

Accuracy: ±MaxError after circuit and capacity calibration

RemainingCapacity() (0x0f)

This read-only word returns the predicted remaining battery capacity. The RemainingCapacity value is expressed in mAh.

Output: unsigned integer. Returns the estimated remaining capacity in mAh.

Units: mAh

Range: 0 to 65,535mAh

Granularity: 0.2% of DesignCapacity or better

Accuracy: ±MaxError * FCC after circuit and capacity calibration

FullChargeCapacity() (0x10)

This read-only word returns the predicted pack capacity when it is fully charged. FullChargeCapacity defaults to the value programmed in the external EEPROM until a new pack capacity is learned. The new FCC is stored to EEPROM within 400ms of a valid charge after a qualified discharge.

Output: unsigned integer. Returns the estimated full charge capacity in mAh.

Units: mAh

Range: 0 to 65,535mAh

Granularity: 0.2% of DesignCapacity or better

Accuracy: ±MaxError * FCC after circuit and capacity calibration

RunTimeToEmpty() (0x11)

This read-only word returns the predicted remaining battery life at the present rate of discharge (minutes). The RunTimeToEmpty value is calculated based on Current.

Output: unsigned integer. Returns the minutes of operation left.

Units: minutes

Range: 0 to 65,534min

Granularity: 2min or better

Invalid data indication: 65,535 indicates battery is not being discharged.

AverageTimeToEmpty() (0x12)

This read-only word returns the predicted remaining battery life at the present average discharge rate (minutes). The AverageTimeToEmpty is calculated based on AverageCurrent.

Output: unsigned integer. Returns the minutes of operation left.

Units: minutes

Range: 0 to 65,534min

Granularity: 2min or better

Invalid data indication: 65,535 indicates battery is not being discharged.

AverageTimeToFull() (0x13)

This read-only word returns the predicted time until the Smart Battery reaches full charge at the present average charge rate (minutes).

Output: unsigned integer. Returns the remaining time in minutes to full.

Units: minutes

Range: 0 to 65,534min

Granularity: 2min or better

Invalid data indication: 65,535 indicates battery is not being charged.

ChargingCurrent() (0x14)

If enabled, the bq2945 sends the desired charging rate in mA to the Smart Battery Charger.

Output: unsigned integer. Transmits/returns the maximum charger output current in mA.

Units: mA

Range: 0 to 65,534mA

Granularity: 0.2% of the design capacity or better

Invalid data indication: 65,535 indicates that the Smart Charger should operate as a voltage source outside its maximum regulated current range.

ChargingVoltage() (0x15)

If enabled, the bq2945 sends the desired voltage in mV to the Smart Battery Charger.

Output: unsigned integer. Transmits/returns the charger voltage output in mV.

Units: mV

Range: 0 to 65,534mV

Granularity: 0.2% of the DesignVoltage or better

Invalid data indication: 65,535 indicates that the Smart Battery Charger should operate as a current source outside its maximum regulated voltage range.

BatteryStatus() (0x16)

This read-only word returns the battery status word.

Output: unsigned integer. Returns the status register with alarm conditions bitmapped as shown in Table 5.

Some of the BatteryStatus flags (Remaining_Capacity_Alarm and Remaining_Time_Alarm) are calculated based on current. See Table 8 and 9 for definitions.

Table 5. Status Register

Alarm Bits	
0x8000	Over_Charged_Alarm
0x4000	Terminate_Charge_Alarm
0x2000	Reserved
0x1000	Over_Temp_Alarm
0x0800	Terminate_Discharge_Alarm
0x0400	Reserved
0x0200	Remaining_Capacity_Alarm
0x0100	Remaining_Time_Alarm
Status Bits	
0x0080	Initialized
0x0040	Discharging
0x0020	Fully_Charged
0x0010	Fully_Discharged
Error Code	
0x0000-0x000f	Reserved for error codes

CycleCount() (0x17)

This read-only word returns the number of charge/discharge cycles the battery has experienced. A charge/discharge cycle starts from a base value equivalent to the battery's state-of-charge on completion of a charge cycle. The bq2945 increments the cycle counter during the current charge cycle if the battery has been discharged 15% below the state-of-charge at the end of the last charge cycle. This prevents false reporting of small charge/discharge cycles. The cycle count is stored in EEPROM within 400ms of an update.

Output: unsigned integer. Returns the count of charge/discharge cycles the battery has experienced.

Units: cycles

Range: 0 to 65,535 cycles; 65,535 indicates battery has experienced 65,535 or more cycles.

Granularity: 1 cycle

DesignCapacity() (0x18)

This read-only word returns the theoretical capacity of a new pack. The DesignCapacity value is expressed in mAh at the nominal discharge rate.

16/30

Table 6. Bit Descriptions for FLAGS1 and FLAGS2

	(MSB) 7	6	5	4	3	2	1	0 (LSB)
FLAGS2	DMODE	CP2 DI	CHM	CC	-	OV	LTF	OC
FLAGS1	-	-	VQ	-	VDQ	SEDV	EDV1	EDVF

Note: - = Reserved

Output: unsigned integer. Returns the battery capacity in mAh.

Units: mAh

Range: 0 to 65,535mAh

DesignVoltage() (0x19)

This read-only word returns the theoretical voltage of a new pack in mV.

Output: unsigned integer. Returns the battery's normal terminal voltage in mV.

Units: mV

Range: 0 to 65,535mV

Specification Info() (0x1a)

This read-only word returns the specification revision the bq2945 supports.

ManufactureDate() (0x1b)

This read-only word returns the date the cell was manufactured in a packed integer word. The date is packed as follows: (year - 1980) * 512 + month * 32 + day.

Field	Bits Used	Format	Allowable Value
Day	0–4	5-bit binary value	1–31 (corresponds to date)
Month	5–8	4-bit binary value	1–12 (corresponds to month number)
Year	9–15	7-bit binary value	0 * 127 (corresponds to year biased by 1980)

SerialNumber() (0x1c)

This read-only word returns a serial number. This number, when combined with the ManufacturerName, the DeviceName, and the ManufactureDate, uniquely identifies the battery.

Output: unsigned integer

ManufacturerName() (0x20)

This read-only string returns a character string where the first byte is the number of characters available. The maximum number of characters is 11. The character string contains the battery manufacturer's name. For example, "Unitrode" identifies the battery pack manufacturer as Unitrode.

Output: string or ASCII character string

DeviceName() (0x21)

This read-only string returns a character string where the first byte is the number of characters available. The maximum number of characters is 7. The 7-byte character string contains the battery's name. For example, a DeviceName of "bq2945" indicates that the battery is a model bq2945.

Output: string or ASCII character string

DeviceChemistry() (0x22)

This read-only string returns a character string where the first byte is the number of characters available. The maximum number of characters is 5. The 5-byte character string contains the battery's chemistry. For example, if the DeviceChemistry function returns "NiMH," the battery pack contains nickel-metal hydride cells.

Output: string or ASCII character string

ManufacturerData() (0x23)

This read-only string allows access to an up to 5-byte manufacturer data string.

Output: block data—data whose meaning is assigned by the Smart Battery's manufacturer.

End of Discharge Voltage1 (0x3e)

This read-only word returns the first end-of-discharge voltage programmed for the pack.

Output: two's complemented unsigned integer. Returns battery end-of-discharge voltage programmed in EEPROM in mV.

End of Discharge VoltageF (0x3f)

This read-only word returns the final end-of-discharge voltage programmed for the pack.

Output: two's complemented unsigned integer. Returns battery final end-of-discharge voltage programmed in EEPROM in mV.

FLAGS1&2() (0x2f)

This read-only register returns an unsigned integer representing the internal status registers of the bq2945. The MSB represents FLAGS2, and the LSB represents FLAGS1. See Table 6 for the bit description for FLAGS1 and FLAGS2.

FLAGS2

The *Display Mode* flag (DMODE), bit 7 determines whether the bq2945 displays Relative or Absolute capacity.

The DMODE values are:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
DMODE	-	-	-	-	-	-	-

Where DMODE is:

0 Selects Absolute display

1 Selects Relative display

Bit 6 reflects the high/low state of CP2.

FLAGS2 Bits							
7	6	5	4	3	2	1	0
-	CP2DI	-	-	-	-	-	-

The *Chemistry* flag (CHM), bit 5, selects Li-Ion or nickel compensation factors.

The CHM values are:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
-	-	CHM	-	-	-	-	-

Where CHM is:

0 Selects Nickel

1 Selects Li-Ion

Bit 4, the *Charge Control* flag (CC), determines whether a bq2945-based charge termination will set RM to a user-defined programmable full charge capacity.

The CC values are:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	CC	-	-	-	-

Where CC is:

0 RM is not modified on valid bq2945 charge termination

1 RM is set to a programmable percentage of the FCC when a valid bq2945 charge termination occurs

Bit 3 is reserved.

Bit 2, the *Overvoltage* flag (OV), is set when the bq2945 detects a pack voltage 5% greater than the programmed charging voltage. This bit is cleared when the pack voltage falls 5% below the programmed charging voltage.

The OV values are:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	OV	-	-

Where OV is:

0 Voltage < 1.05 * ChargingVoltage

1 Voltage ≥ 1.05 * ChargingVoltage

Bit 1, the *Low Temperature Fault* flag (LTF), is set when temperature < 0°C and cleared when temperature > 5°C.

The LTF values are:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	LTF	-

Where LTF is:

0 Temperature > 5°C

1 Temperature < 0°C

Bit 0, the *Overcurrent* flag (OC), is set when the average current is 25% greater than the programmed charging current. If the charging current is programmed less than 1024mA, overcurrent is set if the average current is 256mA greater than the programmed charging current.

This flag is cleared when the average current falls below 256mA.

The OC values are:

FLAGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OC

Where OC is:

0 AverageCurrent is less than 1.25 * ChargingCurrent or less than 256mA if charging current is programmed less than 1024mA

1 AverageCurrent exceeds 1.25 * ChargingCurrent or 256mA if the charging current is programmed less than 1024mA. This bit is cleared if average current < 256mA.

FLAGS1

Bits 7 and 6 are reserved.

The *Valid Charge* flag (VQ), bit 5, is set when $V_{SRO} \geq |V_{SRD}|$ and 10mAh of charge has accumulated. This bit is cleared during a discharge and when $V_{SRO} \leq |V_{SRD}|$.

The VQ values are:

FLAGS1 Bits							
7	6	5	4	3	2	1	0
-	-	VQ	-	-	-	-	-

Where VQ is:

0 $V_{SRO} \leq |V_{SRD}|$

1 $V_{SRO} \geq |V_{SRD}|$ and 10mAh of charge has accumulated

Bit 4 is reserved.

The *Valid Discharge* flag (VDQ), bit 3, is set when a valid discharge is occurring (discharge cycle valid for learning new full charge capacity) and cleared if a partial charge is detected, EDV1 is asserted when T < 0°C, or self-discharge accounts for more than 256mAh of the discharge.

The VDQ values are:

FLAGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

Where VDQ is:

0 Self-discharge is greater than 256mAh, EDV1 = 1 when T < 0°C or VQ = 1

1 On first discharge after RM=FCC

The *Stop EDV* flag (SEDV), bit 2, is set when the discharge current > 6.15A and cleared when the discharge current falls below 6.15A.

The SEDV values are:

FLAGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	SEDV	-	-

Where SEDV is:

0 Current < 6.15A

1 Current > 6.15A

The *First End-of-Discharge Voltage* flag (EDV1), bit 1, is set when Voltage < EDV1 and SEDV = 0 and cleared when VQ = 1 and Voltage > EDV1.

The EDV1 values are:

FLAGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV1	-

Where EDV1 is:

0 VQ = 1 and Voltage > EDV1

1 Voltage < EDV1 and SEDV = 0

The *Final End-of-Discharge Voltage* flag (EDVF), bit 0, is set when Voltage < EDVF and SEDV = 0 and cleared when VQ = 1 and Voltage > EDVF.

The EDVF values are:

FLAGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	EDVF

Where EDVF is:

0 VQ = 1 and Voltage > EDVF

1 Voltage < EDVF and SEDV = 0

Error Codes and Status Bits

Error codes and status bits are listed in Table 8 and Table 9, respectively.

Control Pins 1 and 2 (CP_1, CP_2)

CP_1 and CP_2 are open drain outputs that are controlled by host command. Since they are under the control of the host, their use can be defined by the pack designer. Some uses for these pins are charger control, control of current path (charge FET, discharge FET, or fuse), or special LED function. CP_1 and CP_2 are controlled by the host writing a command to the battery's ManufacturerAccess slave function. Table 7 describes the commands that are available to control CP_1 and CP_2.

The CP_2 can also act as a digital input. The logical status can be monitored in bit 6 of the FLAGS2 register.

Table 7. ManufactureAccess Commands

CMD (0x00) =	Action
0x0505	CP_1 set to hi-Z
0x051b	CP_1 set low
0x0536	CP_2 set to hi-Z
0x054e	CP_2 set low
0x0563	CP_1 and CP_2 set to hi-Z
0x057d	CP_1 and CP_2 set low

SBD Seal

The bq2945 address space can be "locked" to enforce the SBS specified access to each command code. To lock the address space, the bq2945 must be initialized with EE 0x3d set to 00h. Once this is done, only commands 0x00-0x04 may be written. Attempting to write to any other address will cause a "no acknowledge" of the data. Reading will only be permitted from the command codes listed in the SBD specification plus the five locations designated as optional manufacturing functions 1—5 (0x2f, 0x3c—0x3f).

Programming the bq2945

The bq2945 requires the proper programming of an external EEPROM for proper device operation. Each module can be calibrated for the greatest accuracy, or general "default" values can be used. An EV2200-45 programming kit (interface board, software, and cable) for an IBM-compatible PC is available from Unitrode.

The bq2945 uses a 24LC01 or equivalent serial EEPROM (capable of read operation to 2.0V) for storing the various initial values, calibration data, and string information. Table 1 outlines the parameters and addresses for this information. Tables 10 and 11 detail the various register contents and show an example program value for an 2400mAh 4-series Li-Ion battery pack, using a 50mΩ sense resistor.

Table 8. Error Codes (BatteryStatus() (0x16))

Error	Code	Access	Description
OK	0x0000	read/write	bq2945 processed the function code without detecting any errors.
Busy	0x0001	read/write	bq2945 is unable to process the function code at this time.
ReservedCommand	0x0002	read/write	bq2945 cannot read or write the data at this time—try again later.
UnsupportedCommand	0x0003	read/write	bq2945 does not support the requested function code.
AccessDenied	0x0004	write	bq2945 detected an attempt to write to a read-only function code.
Overflow/Underflow	0x0005	read/write	bq2945 detected a data overflow or underflow.
BadSize	0x0006	write	bq2945 detected an attempt to write to a function code with an incorrect size data block.
UnknownError	0x0007	read/write	bq2945 detected an unidentifiable error.

Note: Reading the bq2945 after an error clears the error code.

Table 9. BatteryStatus Bits

Alarm Bits		
Bit Name	**Set When:**	**Reset When:**
OVER_CHARGED_ALARM	The bq2945 detects a ΔT/Δt or current taper termination. (**Note: ΔT/Δt and current taper are valid charge terminations**.)	A discharge occurs or when the ΔT/Δt or current taper termination condition ceases during charge.
TERMINATE_CHARGE_ALARM	The bq2945 detects an over-current, over-voltage, over-temperature, ΔT/Δt, or current taper condition during charge.	A discharge occurs or when all conditions causing the event cease.
OVER_TEMP_ALARM	The bq2945 detects that its internal temperature is greater than the programmed value.	Internal temperature falls below 50°C.
TERMINATE_DISCHARGE_ALARM	The bq2945 determines that it has supplied all the charge that it can without being damaged (Voltage < EDVF).	Voltage > EDVF signifies that the battery has reached a state of charge sufficient for it to once again safely supply power.
REMAINING_CAPACITY_ALARM	The bq2945 detects that the RemainingCapacity is less than that set by the RemainingCapacityAlarm function.	Either the value set by the RemainingCapacityAlarm function is lower than the Remaining Capacity or the RemainingCapacity is increased by charging.
REMAINING_TIME_ALARM	The bq2945 detects that the estimated remaining time at the present discharge rate is less than that set by the RemainingTimeAlarm function.	Either the value set by the RemainingTimeAlarm function is lower than the AverageTimeToEmpty or a valid charge is detected.
Status Bits		
Bit Name	**Set When:**	**Reset When:**
INITIALIZED	The bq2945 has completed a "learn" cycle.	Battery detects that power-on or user-initiated reset has occurred.
DISCHARGING	The bq2945 determines that it is not being charged.	Battery detects that it is being charged.
FULLY_CHARGED	The bq2945 determines a valid charge termination or a maximum overcharge state.	RM discharges below 95% of the full charge percentage.
FULLY_DISCHARGED	bq2945 determines that it has supplied all the charge that it can without being damaged.	RelativeStateOfCharge is greater than or equal to 20%

Table 10. Example Register Contents

Description	EEPROM Address		EEPROM Hex Contents		Example Values	Notes
	Low Byte	High Byte	Low Byte	High Byte		
EEPROM length	0x00		64		100	Must be equal to 0x64.
EEPROM check 1	0x01		5b		91	Must be equal to 0x5b.
Remaining time alarm	0x02	0x03	0a	00	10 minutes	Sets the low time alarm level.
Remaining capacity alarm	0x04	0x05	f0	00	240mAh	Sets the low capacity alarm level.
Reserved	0x06	0x07	00	00	0	Not currently used by the bq2945.
Initial charging current	0x08	0x09	60	09	2400mA	Sets the initial charge request.
Charging voltage	0x0a	0x0b	d8	40	16600mV	Used to set the fast-charge voltage for the Smart Charger.
Battery status	0x0c	0x0d	80	00	128	Initializes BatteryStatus.
Cycle count	0x0e	0x0f	00	00	0	Contains the charge cycle count and can be set to zero for a new battery.
Design capacity	0x10	0x11	60	09	2400mAh	Nominal battery pack capacity.
Design voltage	0x12	0x13	40	38	14400mV	Nominal battery pack voltage.
Specification information	0x14	0x15	10	00	1.0	Default value for this register in a 1.0 part.
Manufacturer date	0x16	0x17	a1	20	May 1, 1996 = 8353	Packed per the ManufactureDate description.
Serial number	0x18	0x19	12	27	10002	Contains the optional pack serial number.
Fast-charging current	0x1a	0x1b	60	09	2400mA	Used to set the fast-charge current for the Smart Charger.
Maintenance charge current	0x1c	0x1d	00	00	0mA	Contains the desired maintenance current after fast-charge termination by the bq2945.
Reserved	0x1e	0x1f	00	00	0	Must be programmed to 0x00.
Current integration gain[1]	0x2c	0x2d	40	00	3.2/0.05	Represents the following: 3.2/sense resistor in ohms. It is used by the bq2945 to scale the measured voltage values on the SR pin in mA and mAh. This register also compensates for variations in the reported sense resistor value.

Note: 1. Can be adjusted to calibrate the battery pack.

Table 10. Example Register Contents (Continued)

Description	EEPROM Address		EEPROM Hex Contents		Example Values	Notes
	Low Byte	High Byte	Low Byte	High Byte		
Reserved	0x2e	0x2f	00	00	0	Not currently used by the bq2945.
Li-Ion taper current	0x38	0x39	10	ff	240mA	Sets the upper taper limit for Li-Ion charge termination. Stored in 2's complement.
Maximum overcharge limit	0x3a	0x3b	9c	ff	100mAh	Sets the maximum amount of overcharge before a maximum overcharge charge suspend occurs. Stored in 2's complement.
Reserved	0x3c		00		0	Should be programmed to 0.
Access protect	0x3d		00		SBD access only	If the bq2945 is reset and this location is 0, the bq2945 locks access to any command outside of the SBD data set. Program to 0x08 for full R/W access.
FLAGS1	0x3e		00		0	Initializes FLAGS1
FLAGS2	0x3f		b0		Relative display Li-Ion chemistry bq2945 charge control	Initializes FLAGS2.
Battery voltage offset[1]	0x48		fe		-2mV	Used to adjust the battery voltage offset according to the following: Voltage = (V_{SB}(mV) + V_{OFF}) * Voltage gain
Temperature offset[1]	0x49		8a		13.8°C	The default value (zero adjustment) for the offset is 12.8°C or 0x80. $TOFF_{NEW}$ = $TOFF_{CURRENT}$ + ($TEMP_{ACTUAL}$ - $TEMP_{REPORTED}$)* 10
Maximum temperature and ΔT step	0x4a		8f		Maximum temperature = 61.2°C ΔT step = 4.6°C	Maximum charge temperature is 74 - (mt * 1.6)°C (mt = upper nibble). The ΔT step is (dT * 2 + 16)/10°C (dT = lower nibble)
Charge efficiency	0x4b		ff		Maintenance compensation = 100% Fast compensation = 100%	Sets the fast-charge (high) and maintenance charge (low) efficiencies. The upper nibbles sets the low efficiency and the lower nibble adjusts the high efficiency according to the equation: Nibble = (efficiency% * 256 - 196)/4
Full-charge percentage	0x4c		9c		100%	This packed field is the two's complement of the desired value in RM when the bq2945 determines a full-charge termination. If RM is below this value, RM is set to this value. If RM is above this value, then RM is not adjusted.

Note: 1. Can be adjusted to calibrate the battery pack.

Table 10. Example Register Contents (Continued)

Description	EEPROM Address		EEPROM Hex Contents		Example Values	Notes
	Low Byte	High Byte	Low Byte	High Byte		
Digital filter	0x4d		96		0.30mV	Used to set the digital magnitude filter as described in Table 2.
Reserved	0x4e		00		0	Not currently used by the bq2945.
Self-discharge rate	0x4f		2d		0.25%	This packed field is the two's complement of (52.73/x) where x is the desired self-discharge rate per day (%) at room temperature.
Voltage gain[1]	0x56	0x57	17	07	7.09	Voltage gain is packed as two units. For example, (R4 + R5)/R4 = 7.09 would be stored as: whole number stored in 0x57 as 7 and the decimal component stored in 0x56 as 256 x 0.09 = 23 (= 17h).
Reserved	0x58	0x59	00	00	0	Should be programmed to 0.
Current measurement gain[1]	0x5a	0x5b	ee	02	750	The current gain measurement and current integration gain are related and defined for the bq2945 current measurement. This word equals 37.5/sense resistor value in ohms.
End of discharge voltage1	0x5c	0x5d	20	d1	12000mV	The value programmed is the two's complement of the threshold voltage in mV.
End of discharge voltage final	0x5e	0x5f	40	d4	11200mV	The value programmed is the two's complement of the threshold voltage in mV.
Full charge capacity	0x60	0x61	d0	07	2000mA	This value sets the initial estimated pack capacity.
Δt step	0x62		ff		20s	The Δt step for $\Delta T/\Delta t$ termination equals 20s * the two's complement of the byte value.
Hold-off time	0x63		f0		320s hold-off	The hold-off time is 20s * the two's complement of the byte value.
EEPROM check 2	0x64		b5		181	Must be equal to 0xb5.
Reserved	0x65	0x7f			NA	Not currently used by the bq2945.

Note: 1. Can be adjusted to calibrate the battery pack.

Table 11. Example Register Contents (String Data)

String Description	Address	0x X0	0x X1	0x X2	0x X3	0x X4	0x X5	0x X6	0x X7	0x X8	0x X9-Xf	0x xa	0x xb
Manufacturer name	0x20- 0x2b	09	42 B	45 E	4e N	43 C	48 H	4d M	41 A	52 R	51 Q	-	-
Device name	0x30- 0x37	06	42 B	51 Q	32 2	39 9	34 4	35 5	-				
Device chemistry	0x40- 0x47	04	6c L	69 I	4f O	4e N	-						
Manufacturer data	0x50- 0x55	05	42 B	51 Q	32 2	30 0	32 2						

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
REF	Relative to V_{SS}	-0.3	+8.5	V	Current limited by R1 (See Figure 1.)
V_{SR}	Relative to V_{SS}	-0.3	+7.0	V	Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery.
T_{OPR}	Operating temperature	0	+70	°C	Commercial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 5.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
E_{VSB}	Battery voltage error relative to SB	-50mV	-	50mV	V	See note

Note: The accuracy of the voltage measurement may be improved by adjusting the battery voltage offset and gain, stored in external EEPROM. For best operation, V_{CC} should be 1.5V greater than V_{SB}.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

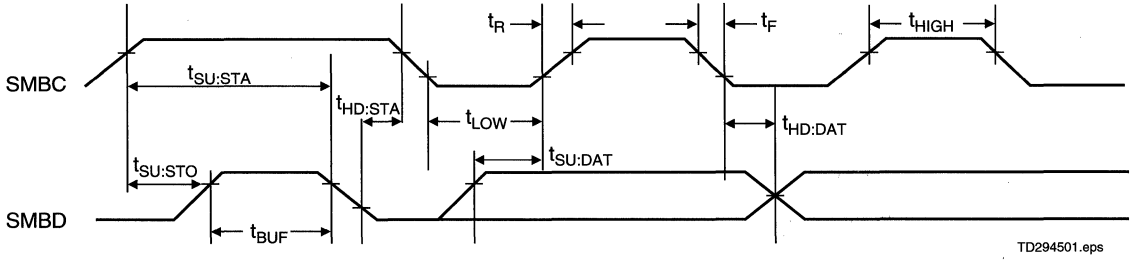
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V
		-	120	180	µA	V_{CC} = 4.25V
		-	170	250	µA	V_{CC} = 5.5V
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	0 < V_{SB} < V_{CC}
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	V_{DISP} = V_{SS}
I_{LVOUT}	V_{OUT} output leakage	-0.2	-	0.2	µA	EEPROM off
V_{SR}	Sense resistor input	-0.3	-	2.0	V	V_{SR} < V_{SS} = discharge; V_{SR} > V_{SS} = charge
R_{SR}	SR input impedance	10	-	-	MΩ	-200mV < V_{SR} < V_{CC}
V_{IH}	Logic input high	0.5 * V_{CC}	-	V_{CC}	V	ESCL, ESDA
		1.4	-	5.5	V	SMBC, SMBD
V_{IL}	Logic input low	0	-	0.3 * V_{CC}	V	ESCL, ESDA
		-0.5		0.6	V	SMBC, SMBD
V_{OL}	Data, clock output low	-	-	0.4	V	I_{OL}=350µA, SMBC, SMBD
I_{OL}	Sink current	100	-	350	µA	V_{OL}≤0.4V, SMBC, SMBD
V_{OLSL}	LED_X , CP_1, CP_2 output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, I_{OLS} ≤ 1.75mA LED_1–LED_5, CP_1, CP_2
V_{OLSH}	LED_X , CP_1, CP_2 output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, I_{OLS} ≤ 11.0mA LED_1–LED_5, CP_1, CP_2
V_{OHVL}	V_{OUT} output, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{VOUT} = -5.25mA
V_{OHVH}	V_{OUT} output, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} = 6.5V, I_{VOUT} = -33.0mA
I_{VOUT}	V_{OUT} source current	-33	-	-	mA	At V_{OHVH} = V_{CC} - 0.6V
I_{OLS}	LED_X , CP_1, CP_2 sink current	11.0	-		mA	At V_{OLSH} = 0.4V

Note: All voltages relative to V_{SS}.

AC Specifications

Symbol	Parameter	Min	Max	Units	Notes
F_{SMB}	SMBus operating frequency	10	100	KHz	
T_{BUF}	Bus free time between stop and start condition	4.7		µs	
$T_{HD:STA}$	Hold time after (repeated) start condition	4.0		µs	
$T_{SU:STA}$	Repeated start condition setup time	4.7		µs	
$T_{SU:STO}$	Stop condition setup time	4.0		µs	
$T_{HD:DAT}$	Data hold time	300		ns	
$T_{SU:DAT}$	Data setup time	250		ns	
T_{LOW}	Clock low period	4.7		µs	
T_{HIGH}	Clock high period	4.0		µs	
T_F	Clock/Data fall time		300	ns	
T_R	Clock/data rise time		1000	ns	
$T_{LOW:SEXT}$	Cumulative clock low extend time (slave)		25	ms	
$T_{TIMEOUT}$		25	35	ms	

Bus Timing Data



Data Sheet Revision History

ChangeNo.	Page No.	Description of Change
1	All	"Final" changes from "Preliminary" version
2	6	Added V_{SB} should not exceed 2.4V
2	11	Changed cycle count increase from 30 to 32 for condition request
2	14	Changed AtRateOK() indication from EDV1 to EDVF
2	25	Changed self discharge programming from 52.75/x to 52.73/x

Notes: Change 1 = June 1998 B changes from Sept. 1997 "Preliminary."
Change 2 = June 1999 C changes from June 1998.

Ordering Information

bq2945

Temperature Range:
blank = Commercial (0 to 70°C)

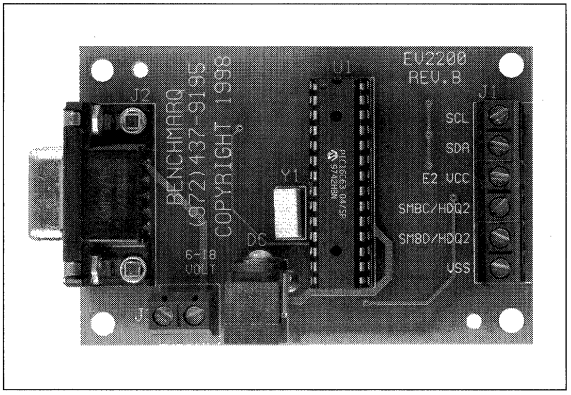
Package Option:
SN = 16-pin narrow SOIC

Device:
bq2945 Gas Gauge IC with SMBus Interface

PC Interface Board for Gas Gauge Evaluation

Features

- Development system for HDQ (bq2013H, bq2018, and bq2050H) and SMBus (bq2040, bq2060, bq2092, bq2945) gas gauge ICs
- Provides interface between intelligent battery and Windows-based PC
- Connects to the serial communications port of a PC
- On screen display and programming of gas gauge register functions
- Programs EEPROM and calibrates current, temperature and voltage in bq2040, bq2092, and bq2945 based packs



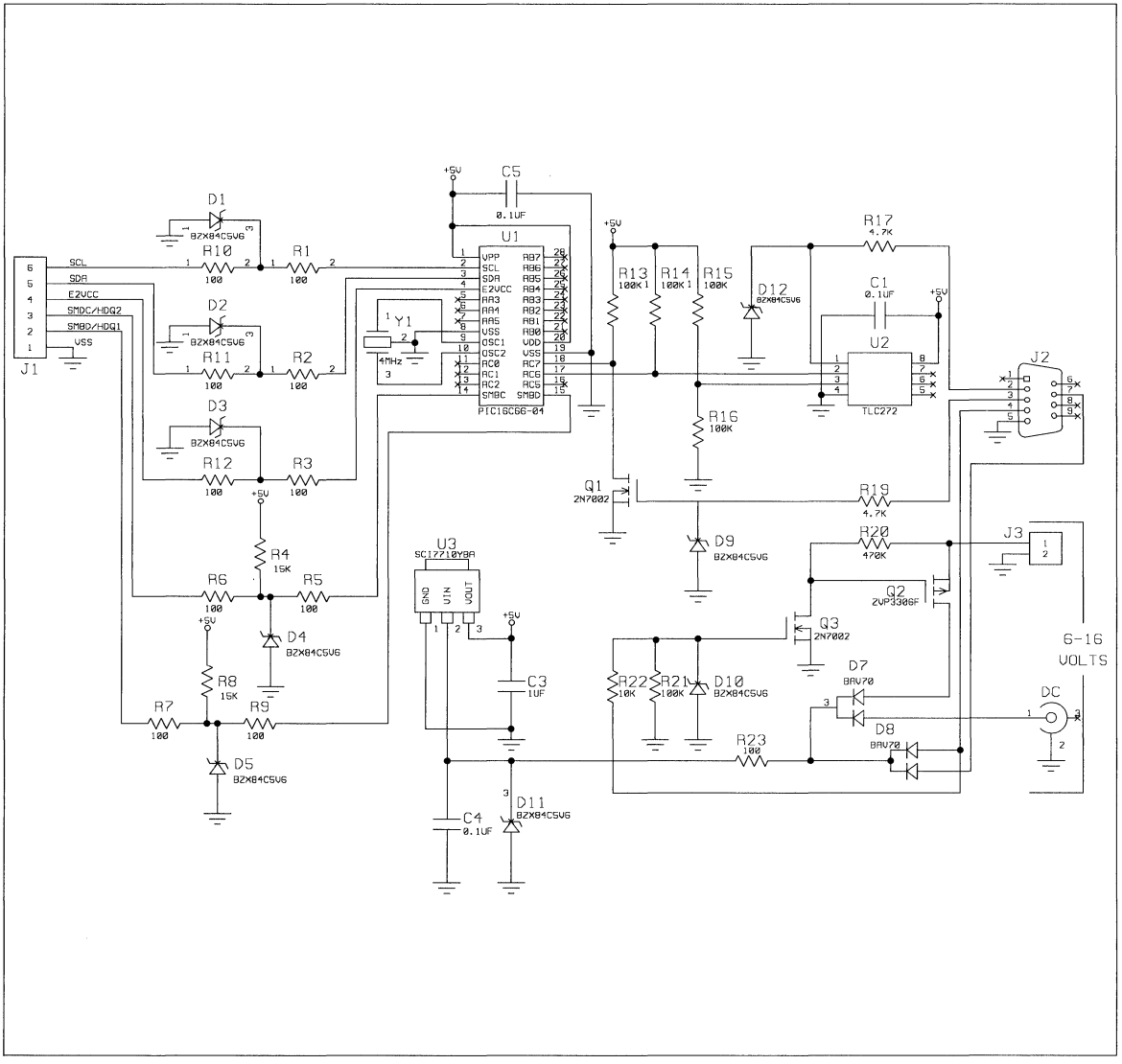
General Description

The EV2200 provides a development and evaluation environment for HDQ based and SMBus based gas gauge ICs. The EV2200 provides connections for the communication lines of an intelligent battery and a serial interface port of a Windows-based PC. With the EV2200, the user can read/write the gas gauge registers of each IC and monitor the battery's status. In the SBS SMBus environment, the interface board and software allow the battery pack designer to evaluate the function of the ICs, calibrate the intelligent battery circuit for current, temperature, and voltage measurements, and program the external EEPROM. The evaluation system includes the interface board, DC power supply, and PC software.

Please specify the desired software to be included with the EV2200 evaluation board as shown below:

Gas Gauge IC	Part Number
bq2013H	EV2200-13H
bq2018	EV2200-18
bq2040	EV2200-40
bq2050H	EV2200-50H
bq2060	EV2200-60
bq2092	EV2200-92
bq2945	EV2200-45

EV2200 Board Schematic



Rev. C Board

Smart Battery System Gas Gauge IC

Introduction

This document supplements the *Smart Battery Systems Specifications* and the bq2040 data sheet.

The bq2040 Gas Gauge IC meets the requirements for systems incorporating the industry standard Smart Battery System bus and data set. It is based on Unitrode's proven technology for accurately monitoring battery capacity.

In this tutorial, "user" is the battery system designer who determines the configuration of a pack, not the end-user of a system. Terms from the SMB/SBD specifications are printed with the first letter of each word capitalized as printed in those specifications, while configuration and status parameters specific to the bq2040 are fully capitalized.

System Components and Operation

SMB Two-Wire Serial Port

The SMB serial port meets all DC and AC parameters in the SMB 1.0 specification.

SBD Data Set

The bq2040 supports the Smart Battery Data Specification 1.0.

Measurement Subsystems

Of primary importance in any battery management solution are the analog measurement components. The parameters that must be measured include battery voltage, battery temperature and battery current. Because current-sensing requires the measurement of low-level signals with a wide dynamic range, while measuring battery voltage and temperature do not, the bq2040 has two measurement units. A successive approximation A/D is used to measure battery voltage and temperature, and a voltage-to-frequency converter is used to measure battery current.

Measuring Voltage and Temperature

Battery voltage is monitored at the SB input. The pack voltage is typically divided down by a resistor divider to represent the average single cell voltage of nickel chemistry cells or half that of the average lithium-ion chemistry cell. These ratios of division are the most common, although not required. The 10-bit A/D at the SB input measures voltages between 0 and 2.4V.

Battery temperature is measured by an internal sensor and the 10-bit A/D. In designing the mechanics of a battery pack, the proximity of the bq2040 to the cells and the thermal characteristics of the packaging must be considered. This consideration is most important for nickel chemistry applications where $\Delta T/\Delta t$ charge termination is desired.

Measuring Current

Battery current is monitored at the SR input by measuring the voltage drop across a series sense resistor. The most common value for the sense resistor is 0.05 ohms; however, the bq2040 can be calibrated to any value down to 0.0125 ohms and to well above a practical limit of about 0.2 ohms. Accurate capacity monitoring requires measuring battery current over a wide dynamic range, and since battery systems operate over long time periods, small errors can accumulate with time and cause the capacity to be reported inaccurately. To provide an accurate, cost-effective solution to this problem, the bq2040 employs a voltage-to-frequency converter (VFC) to monitor the voltage drop across the series current sense resistor. VFCs are less conventional, but they allow the measurement of very small signals without the quantization error associated with more widely used A/D converters. Also, the input offset of the VFC in the bq2040 is typically 50µV, much lower than that achievable with most A/D implementations.

The VFC integrates the voltage at its input and supplies a pulse to an internal counter for each 45mVs that has been integrated. Because the voltage at the SR input represents current, the integral of the voltage represents charge and thus the internal counter increments with each packet of charge detected. Two pulses are available, one for positive inputs on SR and one for negative inputs. The counter is incremented for charge entering the battery or decremented for charge leaving the battery. The relation of current, sense resistance, and the period of pulses to the counter within the VFC is

$$t_i = \frac{0.045}{i_{SR} \cdot R_{SR}} [s]$$

Measurements performed with a VFC are inherently average values rather than instantaneous values. This is an advantage for applications such as capacity monitoring because the input is sampled nearly continuously.

Alternatively, an A/D which typically samples its input briefly at relatively infrequent intervals can miss significant but short duration current drain events, such as spinning up a hard drive or turning on a fan.

The use of a VFC optimizes the accuracy of charge and discharge measurement, the prime objective of the Gas Gauge IC. It is also dynamically balanced to enhance the charge measurement accuracy. Current flow in and out of the battery may be calculated from the rate of charge accumulation, but is typically a noisy measurement since it is a derivative of the charge accumulation measurement. The current calculation is averaged to achieve a more stable reported value. The resulting delay and granularity in reported current do not indicate inaccurate capacity reporting. An implementation optimized for very accurate and smoothed current indication, with correspondingly less capacity-gauging accuracy, may not meet the user's need for accurate capacity gauging.

The current reported in Current (0x0a) is the average of the current over the previous 20 seconds. The current reported in AverageCurrent (0x0b) is the average of the current over the previous 60 seconds. The reported AverageCurrent is updated every 20 seconds. The granularity in current reporting may be determined by use of the above formula for both the 20-second and 60-second average current values. Current is reported as zero if it is less than this minimum granularity value (15mA average current with a .05 ohm sense resistor).

Even with reported currents of zero, the capacity gauge continues to measure charge and discharge of the battery accurately as long as the current develops more voltage across the sense resistor than the digital filter threshold (5mA minimum with .05 ohm sense resistor and 250µV digital filter threshold). The current reported by Current (0x0a) and AverageCurrent (0x0b) may be calibrated by adjustment of the IRES60 current-measurement gain factor to account for variations in the effective sense resistor value from unit to unit. The maximum reported current flow is limited to the value that drops 285mV across the sense resistor.

Capacity Monitoring

Minimum Measurable Current Flow

Systems expected to measure very small signals must establish a minimum signal level. The minimum signal level should be larger than the errors due to circuit offsets or noise. In the case of capacity monitoring this insures that the capacity counter does not increment or decrement while there is no current flowing. In the bq2040 a user-settable filter sets this minimum level and disallows changes to capacity from signal levels below the digital filter. Every bq2040 is tested to 150µV input offset of the SR pin, although typically the offset is 50µV. SR input offset is greatly affected by the printed circuit board layout and bypass capacitor selection. A digital filter cutoff value of 250µV is usually recommended but may be adjusted for individual designs. A bq2040 and PCB layout with an offset of 100µV and a digital filter of 250µV with a 0.1 ohm sense resistor translates to minimum measurable current of 3.5mA with 1mA of absolute error.

Coulomb Counting

The internal counter mentioned earlier is a 24-bit counter whose unit count value is (1/256)mAh. The upper 16-bits of the counter are displayed as the SBD Function RemainingCapacity(0x0f) (RM). Each charge packet detected increments or decrements the 24-bit coulomb counter by an amount calculated from the current polarity, sense-resistor value, battery charge efficiency and the measured battery temperature. The base mAh value of the packets are programmed in the parameter called current integration gain, or DELCAP, which has the units of (1/256)mAh. This configuration parameter scales the charge packets to the sense-resistor. The base value for a 0.05 ohm sense-resistor is 0.25mAh.

Charge Compensation

The value of charge accumulated during battery charging is adjusted for battery charge efficiency. Charge compensation is determined using a two-segment piece-wise linear model. The two segments are divided at the point where the cells are considered full for fast-charge purposes, such as the point that a $\Delta T/\Delta t$ termination occurs. This point is user selected, and referred to as full-charge percentage or FULPCT. If RelativeStateofCharge (0x0d) is below FULPCT, charging occurs at the high efficiency rate (HEFF), and above this point charging is counted at the low efficiency rate (LEFF). The LEFF and HEFF charge efficiency factors are used whether CHM is a 1 or 0. The charge efficiencies are generally programmed for 100% charge efficiency for lithium-ion batteries. The charge efficiency is also modified by temperature, but only if CHM=0. If CHM=0, both LEFF and HEFF are decreased by 2 percentage points for temperatures between 30°C and 40°C, and by 5 percentage points for temperatures above 40°C.

Discharge Compensation

There is no compensation during discharge. The coulomb counter is decremented by the value of DELCAP for each charge packet detected with a negative signal on SR. DELCAP is a programmable value and is normally calibrated to account for variation in effective sense-resistor values from unit to unit to achieve optimal accuracy.

Self-Discharge

The bq2040 also estimates self-discharge of the cells. The user selects the estimated rate for the range 20-30°C and the capacity is decreased by that rate each

day. For each ten degrees above the 20–30°C range the rate doubles (up to a maximum 70–80°C range) and for each 10 degrees below the 20–30°C range, the rate halves (down to a minimum 0–10°C range). Self-discharge estimation is made by reducing Nominal Available Capacity (NAC), and consequently Remaining-Capacity (0x0f), by 1/256th of its present value.

The self-discharge estimation is varied by adjusting the time interval between self-discharge estimation adjustments. At 25°C, the self-discharge estimation is made every Sdtime with a corresponding Sdest per day. These values are related to the programmed SDRATE at 25°C as follows:

$$Sdtime = 640 \times 2's[SDRATE][s]$$

$$Sdest = \frac{13500}{256x2's[SDRATE]}[\%day]$$

Self-discharge estimation is not done unless Discharging flag in BatteryStatus is set. No self-discharge estimation is done while charging.

Calibration Cycles

To keep the capacity counter accurate and adjust the full capacity register to changes in capacity over the life of the battery, calibration or learning cycles are required from time to time. A calibration cycle consists of a valid discharge from full to empty. The full condition is defined as RemainingCapacity (0x0f) (RM) equal to Full-ChargeCapacity (0x10) (FCC). The empty condition is defined as reaching a programmable First End of Discharge Voltage (EDV1) threshold. The RelativeS-tateofCharge(0x0d) value associated with this voltage is also a programmable value.

If the battery is used in an application where it very seldom is empty, the use of a higher EDV1 threshold associated with a non-zero remaining capacity allows the battery to go through a calibration cycle more often during normal use. If the battery is discharged until the battery voltage drops below the EDV1 threshold, RM is written down to the programmed EDV1 Battery Low Percentage (BLPCT) times FCC unless RM is already equal to or less than this value.

If RM reaches the appropriate capacity threshold value before the battery voltage falls below the EDV1 threshold on a discharge, further decrementing of RM does not occur until the EDV1 voltage threshold is reached. Further discharge below EDV1 causes RM to continue decrementing.

The various thresholds for EDV1, EDVF, and BLPCT should be programmed such that RM decreases to zero before the battery voltage falls below the Final End of Discharge Voltage (EDVF) threshold. If not already zero, RM is set to zero when the EDVF threshold is reached.

If a calibration cycle is completed, FCC is updated with a new learned capacity. The Valid Discharge Flag (VDQ) in FLAGS1 indicates that a valid discharge is in progress. VDQ is set whenever RM equals FCC on a charge. It is reset if there is a charge cycle large enough to set VQ (at least 10 mAh) or if the battery sits unused long enough to accumulate a total self-discharge estimation of at least 256mAh. VDQ is also reset if the Low Temperature Fault flag is set or if battery voltage is dropping so fast that Voltage is 256mV or more below the EDV1 threshold at the time that EDV1 flag in FLAGS1 is set.

A new FCC value is computed as the old FCC times BLPCT plus the discharge capacity measured by the Discharge Count Register (DCR) during the valid discharge cycle. This capacity reflects the available capacity that the battery is able to deliver under use conditions. If the new learned capacity is lower than the previous capacity, the new FCC value is limited to a maximum decrease of 256mAh from the prior FCC value. The update to FCC is made after detection of a valid charge (10mAh) following completion of a valid calibration cycle. MaxError (0x0c) is changed to 0x0002 (2%) and the updated FCC value is stored in EEPROM if the FCC value before update was more than 256mAh and was not more than 256mAh greater than the new updated FCC value.

Repeated Accuracy

The bq2040 measurement circuits and basic capacity monitoring methodology were accurate to less than 10% error in tests where a battery was cycled 30 times between 70% and 30%; i.e., without reaching full or empty.

Charge Control

The bq2040 can be used to control a Smart Battery Charger that complies with the Smart Battery System Smart Battery Charger Specification 1.0. To enable the bq2040 to manage the charging, the CC bit *must* be set. The effects of this are explained in the following sections.

The bq2040 controls the Smart Charger by broadcasting the ChargingCurrent and ChargingVoltage to the charger every 10 seconds. If a charger alarm bit is set in BatteryStatus, the broadcast includes the AlarmWarning message and the charging current is set to zero.

Charge Suspension

The charge may be suspended temporarily by the bq2040 if fault conditions are detected. The fault conditions are explained below.

Overcurrent

An overcurrent condition exists when the current measured by the bq2040 exceeds the ChargingCurrent broadcast to the charger by 25%. If the charging current is less than 1024mA, an overcurrent condition is determined as 256mA more than the ChargingCurrent. Once an overcurrent condition is detected the ChargingCurrent is zeroed and the AlarmWarning Terminate_Charge_ Alarm bit is set. The Smart Charger receives a broadcast of AlarmWarning, ChargingVoltage and ChargingCurrent, with ChargingCurrent = 0. Charging is suspended until the bq2040 measures current below 256mA.

Overvoltage

An overvoltage condition exists when the voltage measured by the bq2040 exceeds ChargingVoltage by 5%. When an overvoltage condition is detected, the ChargingCurrent is set to zero, and the AlarmWarning Terminate_Charge_Alarm bit is set. The Smart Charger receives a broadcast of AlarmWarning, ChargingVoltage and ChargingCurrent, with ChargingCurrent = 0. Charging is suspended until the bq2040 measures current below 256mA and voltage less than 105% of ChargingVoltage.

Low Temperature

If the temperature is measured to be less than 12°C then ChargingCurrent is set to the trickle rate. Once the temperature is at or above 15°C, the charging rate is restored to the appropriate rate.

Maximum Temperature

The maximum temperature, safety termination is programmable from 45°C to 69°C in 1.6°C increments. When the battery temperature equals or exceeds the user-programmed maximum temperature, the Over_Temp_ Alarm and Terminate_Charge_Alarm bits are set and ChargingCurrent is zeroed. These Alarm bits are not cleared until the temperature falls to 43°C or below the maximum temperature minus 5°C. A maximum temperature termination is not a valid charge termination but only a charge suspension and as such, the Over_Charged_Alarm bit is not set.

Undervoltage

When the battery voltage is below the EDVF threshold, the Terminate_Discharge_Alarm is set and ChargingCurrent is set to the EDVF rate. Once the voltage is above EDVF, the charging rate is restored to the fast rate unless LTF flag is set (sets trickle rate) and the Terminate_Discharge_Alarm is reset.

PSTAT

When the PSTAT input is greater than or equal to 1.5V, a suspend charge condition is gererated. The ChargingCurrent is set to zero and the Terminate_Charge_Alarm is set if the Discharging flag in BatteryStatus is not set. The Terminate_Charge_Alarm clears when the PSTAT input is less than 1.0V.

Charge Termination

The bq2040 terminates a charge in three ways. The primary charge terminations are ΔT/Δt and current taper, while the secondary safety termination is a capacity based overcharge termination.

Δ**T**/Δ **t**

The ΔT/Δt algorithm detects a preset temperature step over a specified time rather than an instantaneous slope in the temperature. The ΔT/Δt rate is programmable in both the temperature step (1.6°C–4.6°C) and the time (20s-300s) over which the step is allowed to occur. Typical settings for 1C/minute include 2C/120s and 3C/180s. Longer times are required for increased slope resolution. Note that the ΔT/Δt calculation is not made continuously, but only at the end of each Δt interval.

In addition to the ΔT/Δt timer, there is a hold-off timer which starts when the battery is being charged at more than 255mA and is hotter than 25C. The hold-off timer is programmable from 20s to 300s. Until it times out, the ΔT/Δt detection is suspended. If any of the conditions cease, the timer resets and will restart only when all conditions are met again. The ΔT/Δt termination conditions are checked regardless of the state of the chemistry bit; therefore, the various ΔT/Δt constants must be programmed to values that prevent an unwanted ΔT/Δt termination with a lithium chemistry battery.

When a ΔT/Δt detection occurs, the Over_Charged_Alarm, Terminate_Charge_Alarm, and Fully_Charged bits are set and ChargingCurrent is zeroed. When the charger turns off and Current < 256mA, the alarm bits are cleared.

Current Taper

The current taper method is intended for lithium-ion batteries. ChargingVoltage (0x15) must be set to the pack voltage desired during the constant-voltage phase of charging. The bq2040 detects a current taper termination when the AverageCurrent (0x0b) decreases to less than the user programmable TAPER current and still remains non-zero for at least 100 seconds while also meeting the criterion of a pack voltage measurement greater than the ChargingVoltage (0x15) less 128mV. As with ΔT/Δt, the Over_Charged_Alarm, Terminate_Charge_Alarm, and Fully_Charged bits are

set and ChargingCurrent is zeroed. The alarm bits is cleared when AverageCurrent falls below 256mA.

Capacity-Based Overcharge Termination

The capacity based overcharge termination is a safety termination. It occurs if the battery continues to be charged more than a user selected maximum overcharge limit (MAXOVQ) after RM = FCC. When this point is reached, the Fully_Charged bit is set and current is requested at the trickle rate. Note that the LEFF efficiency is applied to the overcharge before it is counted and compared with MAXOVQ. This is not a valid charge termination and the Over_Charged_Alarm is not set.

Writing RM to FULPCT on Charge Termination

When a $\Delta T/\Delta t$ or Current Taper charge termination occurs, the RM register is set by the internal controller to a programmed full-charge percentage (FULPCT) of FCC if the CC bit is set This does not occur, however, if RM is already above this value or if the CC bit is not set. The Fully_Charged bit is also set when a valid charge termination occurs, but is immediately cleared if CC=0 and RM < FULPCT.

LED Display

A four-segment LED display is available to indicate either RelativeStateOfCharge or AbsoluteStateOfCharge in 25% increments. This selection depends on the state of the msb in FLAGS2&1(0x2f). RelativeStateOfCharge is selected if the msb is set. The display is controlled by the state of the $\overline{\text{DISP}}$ pin. With $\overline{\text{DISP}}$ pulled to Vcc, the display is off. With $\overline{\text{DISP}}$ floating, the display turns on when AverageCurrent(0x0b) is at least +100mA. $\overline{\text{DISP}}$ can also be switched to Vss, in which case the display is active for four seconds. Reactivation of the display requires that it return to the float or Vcc level before switching to Vss. A battery low condition is signaled by blinking LED1 at a 4 Hz rate instead of the normal steady display when the LED display is enabled. LED1 blinks if EDVF is not set, AverageCurrent(0x0b) is at least +100ma (charging), and Remainin_Capacity_Alarm in BatteryStatus(0x16) is set (RemainingCapacity(0x0f) < RemainingCapacityAlarm(0x01)). If EDVF is set, the display is blanked regardless of the state of /$\overline{\text{DISP}}$.

Master Mode Messages

The bq2040 supports the SBData charge-control functions. Master Modes messages are periodically broadcast to a Smart Charger or Host unless disabled. ChargingCurrent and ChargingVoltage are broadcast to the Smart Charger (slave address = 0x12) approximately every 10 seconds. If any alarm bits are set in BatteryStatus (upper byte), the BatteryStatus word is also broadcast. It is broadcast to the Smart Charger in addition to the ChargingCurrent and ChargingVoltage messages if any of the 6 msbs are set (any alarms except Remaining_Time_Alarm and Remaining_Capacity_Alarm). It is also broadcast to the Host (slave address = 0x10) if any alarm bits are set (including Remaining_Time_Alarm and Remaining_Capacity_Alarm).

Configuration and Calibration of the bq2040

The bq2040 reads configuration data from an external EEPROM on power-up or when a software reset is issued. Although it is possible to write to the EEPROM through the SMBus port of the bq2040, not all the locations are accessible, so the EEPROM should be preprogrammed with initial values by an external programmer either before pack assembly or before the devices are soldered to the PC board. After PCB or pack assembly, a few parameters may be adjusted for better accuracy in measuring voltage, temperature, and current.

EEPROM Initialization Parameters

SBD Data Registers Initialized from the EEPROM

RemainingCapacityAlarm (0x01)

RemainingTimeAlarm (0x02)

FullyChargedCapacity (0x10)

ChargingCurrent (0x14)

ChargingVoltage (0x15)

BatteryStatus (0x16)

CycleCount (0x17)

DesignCapacity (0x18)

DesignVoltage (0x19)

SpecificationInfo (0x1a)

ManufactureDate (0x1b)

SerialNumber (0x1c)

ManufacturerName (0x20) text string =11 bytes

DeviceName (0x21) text string = 7 bytes

DeviceChemistry (0x22)text string = 5 bytes

ManufacturerData (0x23)text string = 5 bytes

Gas Gauging Parameters Initialized from EEPROM

FLAGS1 This is the startup value for FLAGS1 and should be set to 0x00.

FLAGS2 This is the startup value for flags2. User should determine display mode, chemistry, and CC mode, and should set the other bits to 0.

SDRATE The self-discharge-rate byte register, calculated according to

$$SRATE = 2's\left[\frac{52.73}{X}\right]$$

where X is the desired self-discharge percentage per day at 25C.

EDV1 (edv1l and edv1h) This 16-bit word register holds the 2's complement of the first end of discharge threshold. [mV]

EDVF (edvfl and edvfh) This 16-bit word register holds the 2's complement of the final end of discharge threshold. [mV]

IOVLD (iovldl and iovldh) This 16-bit word register holds the absolute value of the overload current. AverageCurrent greater than or equal to this value prevents EDV flags from setting.

DELCAP The current integration gain, an 8-bit word register, holds the incremental change in capacity for each tick of the voltage-to-frequency converter assuming 100% efficiency. It is programmed in the EEPROM according to the following formula:

$$DELCAP = \frac{3.2}{R_{SR}}[mAh / 256]$$

BLPCT This 8-bit word register holds the percentage of FCC that represents the capacity of the battery when the battery voltage falls to EDV1. It is programmed in the EEPROM according to the following formula:

BLPCT = 2.56 * (%RM at EDV1)

Programmable Charge Compensations

Charge compensations are programmable in the CEFF variable stored in RAM and EEPROM. One compensation factor (HEFF) is applied while the RelativeStateofCharge is less than FULPCT. A second factor (LEFF) is applied when the RelativeStateofCharge is greater than or equal to FULPCT. These factors are programmable from 76% to 100%. Both factors are varied across temperature in three ranges. Below 30°C the factors are as programmed, for 30°C to 40°C the factors are decreased by 2%, and when Temperature is above 40°C the factors are decreased by 5%.

CEFF Charge efficiency is a packed byte containing the two charge compensations. Bits b7-4 encode LEFF, the low efficiency factor used at or above FULPCT. Bits b3-0 encode HEFF, the high efficiency factor used below FULPCT. The nibble values are each calculated from percent efficiency by the following formula:

$$CEFF\_nibble = \frac{(eff\% \cdot 256 - 196)}{4}$$

The user should note the effect of rounding the result of first calculation by calculating the effective efficiency factor using the following:

$$CEFF\_value = \frac{\{CEFF\_nibble\} \cdot 4 + 196}{256}\%$$

For example: If LEFF=85% and HEFF=95%, choose CEFF=0x5c. This results in LEFF=84.3%, HEFF=95.3%.

FULPCT Percentage of FullChargeCapacity at which the battery is to be considered fully charged. RemainingCapacity may be written to this percentage of fccp on a valid charge termination. Charging current requests are at the slow rate when RemainingCapacity is more than this percentage of FCC. FULPCT is stored in RAM and EEPROM in 2's complement form.

Programmable Minimum Current Signal filter

DIGFIL

The digital filter byte register holds the threshold for filtering false counting due to Vos. The value represents the number of seconds to wait for VFC interrupts before ignoring them.

$$DIGFIL = \frac{0.045}{V_{SRD}}[s]$$

where V_{SRD} is the smallest voltage on SR that allows NAC to count.

Capacity-Based Maximum Overcharge

MAXOVQ

Maximum overcharge that is measured after RM = FCC. The measurement is compensated for efficiency and temperature where applicable. MAXOVQ is a 16-bit word register that holds the 2's complement of the amount of overcharge in mAh.

Programmable Current Taper Detection

TAPER

Upper limit of current taper detection for terminating charging. TAPER is a 16-bit word register that holds the 2's complement of the taper current.

Programmable ΔT/Δt Threshold

The delta-T portion of the ΔT/Δt rate is programmed into the lower nibble of EEPROM address 0x4a. The Δτ portion is programmed in EEPROM address 0x62.

$$\Delta T = \frac{(\Delta T\_value\_in\_EEPROMx2 + 16)}{10}[^{\circ}C]$$

$$\Delta t = 320 - \Delta t\_value\_in\_EEPROMx20[\text{sec}]$$

ΔT Value in EEPROM	ΔT (°C)	Δ t Value in EEPROM	Δ t Timer Period (s)
0	1.6	**00**	320
1	1.8	**01**	300
2	2.0	**02**	280
3	2.2	**03**	260
4	2.4	**04**	240
5	2.6	**05**	220
6	2.8	**06**	200
7	3.0	**07**	180
8	3.2	**08**	160
9	3.4	**09**	140
a	3.6	**0a**	120
b	3.8	**0b**	100
c	4.0	**0c**	80
d	4.2	**0d**	60
e	4.4	**0e**	40
f	4.6	**0f**	20

ΔT/Δt Hold-off Timer

The hold-off timer is programmed in EEPROM address 0x63. No ΔT/Δt termination is allowed until the hold-off time expires after a valid charge is detected. The hold-off time is 320s minus 20 times the EEPROM value.

Value in EEPROM	Hold-Off Time [s]	HO Value in EEPROM	Hold-Off Time [s])
00	320	**08**	160
01	300	**09**	140
02	280	**0a**	120
03	260	**0b**	100
04	240	**0c**	80
05	220	**0d**	60
06	200	**0e**	40
07	180	**0f**	20

Programmable Maximum Temperature Fault

The maximum temperature is programmable in EEPROM over a range of 45°C to 69°C. The value is programmed in to the upper-nibble of EEPROM address 0x4a.

$$Maximum\ Temperature = 69 - (mt\_value\_in\_EEPROM \cdot 1.6)[^\circ C]$$

mt_value_in_ EEPROM	Maximum Temperature	mt_value_in_ EEPROM	Maximum Temperature
0	69.0	**8**	56.2
1	67.4	**9**	54.6
2	65.8	**a**	53.0
3	64.2	**b**	51.4
4	62.6	**c**	49.8
5	61.0	**d**	48.2
6	59.4	**e**	46.6
7	57.8	**f**	45.0

Measurement Parameters and Calibration

A few more parameters are required to configure the bq2040's measurement subsystems. Additionally, measurement accuracy can be improved by calibrating these factors for variations in the battery voltage divider resistors, sense-resistor, PC board conductor resistance in high current paths and for variations in the bq2040 devices themselves. The calibration can be done on PC board assemblies or on assembled and sealed packs by using a feature of the bq2040 which writes data to the EEPROM from an SMBus command.

SMBus Write-through to EEPROM

The SMBus write through function writes two bytes at a time. The correct data word to be changed in the EEPROM may be determined from the E2 Map in the reference section. To modify an EEPROM location from an SMBus command, the WRALL bit must be set and the following sequence must be executed:

1. Write the new information to be updated into the appropriate RAM location using a normal SMB write command.
2. Execute a SMB write command to address 0x3c with the EEPROM location to modify as the LSB data and the access key 0xb3 as the MSB data written with CMD (0x3c). The EEPROM location should always be an even address. A full 16-bit word consisting of both the LSB byte in the even address and MSB byte in the next higher address are written at the same time into the EEPROM. The RAM address is not needed by the processor, as the map relating the two sets of addresses is internal to the processor. The write operation occurs within 0.5 seconds. The processor clears the 0xb3 access key from the msb of CMD (0x3c) when the operation is completed.
3. Confirmation of a successful EEPROM write is only possible by checking the RAM locations initialized from the EEPROM after a full device reset. The calibration factors in the EEPROM cannot be read directly from the SMBus.

WRALL: The WRALL bit controls read and write access to a number of register locations. CMD (0x3c) is read only unless WRALL is set, thus preventing an EEPROM write-through. CMD (0x64) is not accessible unless WRALL is set, preventing a software reset command. WRALL comes up set if EEPROM location 0x3d (BUSYFLG) has bit b3 = 1.

RESET: A software reset reinitializes all register values from the EEPROM. It is the only way to verify that EEPROM values have indeed been updated. A software reset is performed by the following sequence:

1. Check the value of MaxError (0x0c). If this value is 0x0002 (2%), it must be first written to any different value.
2. Write 0x8009 into CMD (0x64).
3. Confirmation of a successful reset may be accomplished by verifying that MaxError (0x0c) is now 0x0064 (100%) and that Temperature (0x08) is 0x0b72 (293.0°K). Temperature is updated to the actual reading 20 seconds after the reset.

Voltage Parameters

NCCAL Byte register to calibrate the Voltage (0x09) function. NCCAL/256 is the fractional multiplier of the voltage on the SB pin.

NCELLS Byte register to calibrate the Voltage (0x09) function. NCELLS is the integer multiplier of the voltage on the SB pin.

VOFF

Byte register to calibrate the Voltage (0x09) function. VOFF is a signed integer which is represents the number of millivolts used to correct for voltage offset in the conversion of the signal on the SB input. Voltage is calculated according to the following formula which uses the preceding byte registers and A/D conversion of the SB input:

$$Voltage = [(Vsb \cdot 1000) + VOFF] \cdot [NCELLS + NCCAL / 256][mV]$$

the offset correction is applied before the gain (ncells.nccal) is applied.

Temperature Calibration

TTRIM

Temperature offset trim is a byte value used to calibrate the internal temperature sensor. The nominal value is 0x80, and represents 12.8°C added to a raw result of temperature. To calibrate the Temperature function TTRIM can be increased to 0xff, 25.5C, or decreased to 0x00, 0C. Thus the calibration range is +12.7K,-12.8K.

Current Calibration

IRES60

Current-measurement gain factor word is used to calibrate the Current and AverageCurrent functions.

$$IRES60 = 192/R_{SR}$$

where R_{SR} is the value of the sense resistor in ohms.

Coulomb Counting Calibration

DELCAP

Based on the accuracy of the current sense, DELCAP may have to be adjusted for more accurate gas gauging. Remember that DELCAP is the sense resistor gain factor word used to calibrate the RemainingCapacity function.

$$DELCAP = 3.2/R_{SR}$$

where R_{SR} is the value of the sense resistor in ohms.

Reference Section

Smart Battery Slave Functions: Details of how they work in the bq2040

ManufacturerAccess (0x00)

ManufacterAccess is currently unused. It is available for read/write access by the user.

RemainingCapacityAlarm (0x01)

This value is initialized from the EEPROM, but can be written by the user at any time. When RemainingCapacity(0x0f) falls below this value, the Remaining_Capacity_Alarm bit is set in BatteryStatus(0x16).

RemainingTimeAlarm (0x02)

This value is initialized from the EEPROM, but can be written by the user at any time. When the AverageTimeToEmpty(0x12) falls below this value, the Remaining_Time_Alarm bit is set in BatteryStatus(0x16).

BatteryMode (0x03)

This read/write word is used to control Smart Charger and Host broadcast messages from the bq2040. Writing bit 14 to a 1 disables these Master Mode broadcast messages to the charger and host. Bit 14 is automatically reset if the SMBC and SMBD communication lines are held low for greater than 2 seconds. If resetting bit 14 is required when the battery pack is removed from the system, 1M pull-down resistors should be added within the battery pack from SMBC and SMBD to Vss to force a logic low on the communication lines. If bit 13 is written to a 1, the Master Mode broadcast messages are also disabled, but this disable is not automatically reset like bit 14. The EEPROM can be configured to initialize bit 13 to a 1 by programming bit b3 in address 0x3f (location that initializes FLAGS2) to a 1.

AtRate(0x04)-(0x07)

The AtRate functions (0x05)-(0x07) are updated every twenty seconds and immediately after AtRate(0x04) is written. Reading commands (0x05)-(0x07) while they are being recalculated results in a no-acknowledge of the command and the error code not ready is reported in BatteryStatus(0x16).

Temperature (0x08)

The temperature measurement is updated every 20 seconds.

Voltage (0x09)

The voltage measurement is updated approximately every 2 seconds.

Current (0x0a)

The current measurement is a 20 second average of ticks from the voltage-to-frequency converter.

AverageCurrent (0x0b)

The value reported for the AverageCurrent function is a 60 second rolling average of the Current function. It is updated every 20 seconds.

MaxError (0x0c)

MaxError is set to 100% upon initial power up or full device reset. It is set to 2% when FULCAP is calibrated and to 5% when the request condition cycle bit (b7) is set in BatteryMode.

RelativeStateOfCharge(0x0d)

The value reported for RelativeStateOfCharge is calculated from RemainingCapacity/FullChargeCapacity at least every 500ms.

AbsoluteStateOfCharge(0x0e)

The value reported for AbsoluteStateOfCharge is calculated from RemainingCapacity/DesignCapacity at least every 500ms.

RemainingCapacity (0x0f)

The value reported from RemainingCapacity is the current battery capacity in mAh and ranges from 0 to a maximum of FullChargeCapacity.

FullChargeCapacity (0x10)

This value is the latest measurement of the battery capacity in mAh.

RunTimeToEmpty(0x11)

The value for RunTimeToEmpty is calculated from Current and RemainingCapacity at least every 500ms.

AverageTimeToEmpty(0x12)

The value for AverageTimeToEmpty is calculated from AverageCurrent and RemainingCapacity every 20s.

AverageTimeToFull(0x13)

The value for AverageTimeToFull is calculated from AverageCurrent and RemainingCapacity every 20s.

ChargingCurrent (0x14)

The value stored in this register changes according to various battery conditions. The value in this register is broadcast to the Smart Charger every 10 seconds if Master Mode messages are enabled. The value in this register is initially loaded with the value programmed into the EEPROM locations 0x08 and 0x09. This value is updated as soon as the gauge determines the charge state of the battery. The value programmed into the EEPROM fast-charging current (FCHGI) location is the value normally loaded in ChargingCurrent. If The Terminate_Charge_Alarm in BatteryStatus is set, ChargingCurrent is set to zero. When the Fully_Charged bit in BatteryStatus or the Low Temperature Fault bit in FLAGS2 is set, ChargingCurrent is set to the maintenance charging current (TCHGI) rate programmed in the EEPROM. If the Terminate_Discharge_Alarm in BatteryStatus is set, ChargingCurrent is set to the EDVF charging current (MCHGI) rate programmed in the EEPROM.

ChargingVoltage (0x15):

The value programmed into the EEPROM for ChargingVoltage (CHGV) determines the contents of this register. This register value is broadcast to the Smart Charger every 10 seconds if Master Mode messages are enabled.

BatteryStatus (0x16)

This 16-bit register reports the system status including alarms, charge state, and communication errors. If any of the alarm bits (b10-b15) in this word are set, this word is broadcast to the Smart Charger. If any bits b8-b15 in this word are set, this word is broadcast to the System Host. These broadcasts occur every 10 seconds unless Master Mode messages are disabled.

b15 **Over_Charged_Alarm:** Set when a current taper or ΔT/Δt condition occurs during a charge. Cleared during discharge or when current taper and ΔT/Δt conditions cease during a charge. This bit indicates a *valid charge termination* and causes RemainingCapacity to be written to FULPCT of FCC if the CC bit in FLAGS2 is set.

b14 **Terminate_Charge_Alarm:** Set when overcurrent, overvoltage, current taper, over-temperature or ΔT/Δt conditions occur during a charge. Cleared during discharge or when all of the setting conditions cease during a charge. Charging current is set to zero when this bit is set. This bit indicates a *charge suspend.*

b13 **Reserved**

b12 **Over_Temp_Alarm:** Set when the temperature is above the programmed maximum temperature. Cleared when the temperature is at or below 43°C or below the maximum temperature minus 5°C. This bit indicates a *charge suspend.*

b11	**Terminate_Discharge_Alarm:** Set when the battery voltage is below the EDVF threshold. Cleared otherwise. While this bit is set, charging current is requested at the EDVF (MCHGI) rate.
b10	**Reserved**
b9	**Remaining_Capacity_Alarm:** Set when RemainingCapacity (0x0f) is less than RemainingCapacityAlarm (0x01). Cleared otherwise.
b8	**Remaining_Time_Alarm:** Set when AverageTimeToEmpty (0x12) is less than the value in RemainingTimeAlarm (0x02). Cleared otherwise.
b7	**Initialized:** Set or cleared according to the default register data loaded from the EEPROM on a full reset of bq2040.
b6	**Discharging:** Set when not charging. Cleared when charging.
b5	**Fully_Charged:** Set when a *valid charge termination* or capacity based overcharge termination occurs. Cleared when the RelativeStateOfCharge (0x0d) is less than FULPCT.
b4	**Fully_Discharged:** Set when set when pack voltage is less than EDVF. Cleared when RelativeStateOfCharge 20%.
b3-0	**Communication Error Codes:** As described in the SBD specification.

CycleCount (0x17)

The cycle count algorithm matches the method described in the SBD specification. When a valid charge is detected, the value of AbsoluteStateOfCharge at the beginning of the previous discharge is used to determine if the battery has been discharged 15 percentage points. Cycle count is saved in EEPROM each time the value is incremented.

DesignCapacity (0x18)

This word returns the programmed value for the design capacity of the battery in mAh. It is used as the 100% reference charge value for the AbsoluteStateOfCharge(0x0e) calculation.

DesignVoltage (0x19)

This word contains the nominal output voltage of the battery pack in mV. It is output as the initial value for the Voltage(0x09) until the first calculation update is made after a reset.

SpecificationInfo (0x1a)

This word should be programmed to the SMB specification revision that the bq2040 supports plus scale factors on reported voltage and current. It should be programmed to 0x1000 for the bq2040, representing SMB specification version 1.0 and scale factors of unity on reported voltage and current.

ManufactureDate (0x1b)

This word is for the battery manufacturer to use to program the date of manufacture of the battery pack. The packed word is determined as follows:

(year–1980) * 512 + month * 32 + day

SerialNumber (0x1c)

This word is for the battery manufacturer to use to program the serial number of the battery pack.

ManufacturerName (0x20)

This word contains an ASCII character string containing the manufacturer's name. The first byte contains the number of characters in the name and following bytes contain the appropriate ASCII character codes. The maximum number of characters is 11.

DeviceIName (0x21)

This word contains an ASCII character string containing the battery name. The first byte contains the number of characters in the name and following bytes contain the appropriate ASCII character codes. The maximum number of characters is 7.

DeviceChemistry (0x22)

This word contains an ASCII character string containing the battery chemistry. The first byte contains the number of characters in the name, and following bytes contain the appropriate ASCII character codes. The maximum number of characters is 5.

ManufacturerData (0x23)

This word contains an ASCII character string containing the manufacturer's data. The first byte contains the number of characters in the name and following bytes contain the appropriate ASCII character codes. The maximum number of characters is 5.

Description of bq2040 Specific Flag Bits

The bq2040 has additional bit-registers to manage internal status. The most useful is Flags2&1 (0x2f).

b15 **DMODE:** User-selectable mode to display capacity. When set the bq2040 is in relative mode and the FullChargeCapacity is used as the 100% reference. In absolute mode the DesignCapacity is used as the 100% reference.

b14 **PSTAT:** This bit reflects the state of the PSTAT input pin to the part. It is a 1 if the input voltage is ≥1.5V and is a 0 if the input voltage is less than 1.0V. This flag could be used to monitor an external function, such as the on/off state of a charge FET in a protector.

b13 **CHM:** User-selected chemistry mode. When set the charge efficiency factors (HEFF and LEFF) are not adjusted for temperature. When not set, HEFF and LEFF charge efficiencies are adjusted with appropriate reductions for temperatures above 30C.

b12 **CC:** When the Charge Control bit is set, the RemainingCapacity is set to FULPCT times FullChargeCapacity when a ***valid charge termination*** occurs unless the capacity is already above this value.

b11 **EINT:** The Enable Interrupt flag is set when the voltage on SR is greater than the digital filter cutoff. When the flag is set, the bq2040 counts charge or discharge interrupts from the voltage-to-frequency converter.

b10 **OV:** overvoltage flag set indicates that the bq2040 detected a pack voltage that is 5% over the value of ChargingVoltage. This flag is cleared when the Voltage is not more than 5% above ChargingVoltage. Overvoltage checking is bypassed if the value in ChargingVoltage (0x15) is greater than 0xf2ff.

b9 **LTF:** The Low Temperature Fault is set when the internal temperature sensor detects a temperature of less than 12°C and reset when the temperature is 15°C or greater.

b8 **OC:** The overcurrent flag denotes that the current measured by the bq2040 is 25% more than the ChargingCurrent (0x14), if Charging Current is at least 1024mA. If ChargingCurrent is less than 1024mA, then OC is set if Current is 256mA more than ChargingCurrent. OC is cleared when Current is less than 256mA. Overcurrent checking is bypassed when the value in ChargingCurrent (0x14) is greater than 0xcbff.

b7 **ΔT/Δt:** The ΔT/Δt flag is set when the rate of increase in temperature exceeds the programmed rate. The flag is cleared with the temperature rise slows below the programmed rate, temperature falls below 25C, or AverageCurrent falls below 256mA.

b6 **IMIN:** The IMIN flag is set when a valid current taper charge termination is detected. This occurs when Voltage (0x09) is above ChargingVoltage (0x15) minus 128mV and AverageCurrent (0x0b) is less than the programmed TAPER limit but greater than 0 for at least 100 seconds. When set, the Fully_Charged, Over_Charged, and Terminate_Charge bits are set and ChargingCurrent (0x14) is set to 0.

b5 **VQ:** The Valid Charge flag is set during a charge cycle which has incremented RemainingCapacity by at least 10mAh. It is reset whenever discharge current above the digital filer threshold is detected.

b4 **Reserved**

b3 **VDQ:** The Valid Discharge flag is set when the pack is discharged from full. VDQ is reset if a valid charge occurs or the temperature goes out of range. If discharged to EDV with VDQ set, the FullChargeCapacity is updated on the next valid charge with the amount of charge removed while VDQ was set.

b2 **OVLD:** The Overload flag is set when discharge current is at or above programmed IOVLD value. Reset when discharge current is less than IOVLD value. EDV1 and EDVF are not set if OVLD is set.

b1 **EDV1**: The First End of Discharge Voltage threshold flag is set when the pack voltage is below the threshold programmed in the EEPROM, OVLD not set, and Current is not positive (charging). EDV1 is reset when VQ is set. LED1 flashes when EDV1 is set, EDVF is not set, and the display is enabled.

b0 **EDVF:** The Final End of Discharge Voltage threshold flag is set when the pack voltage is below the threshold programmed in the EEPROM, OVLD not set, and Current is not positive (charging). EDVF is reset when VQ is set. The LED display is blanked when EDVF is set.

RAM, EEPROM, and Bit-Register Maps

RAM Locations for Test/Calibration/Programming

Name	Description	CMD		RAM Address
NACL	NAC low byte, mAh	(0x1f)	lsb	0x3e
NACH	NAC hi byte, mAh*256		msb	0x3f
MANFNAM	ManufacturerName string data, max length = 11	(0x20)		0x40 - 0x4b
DEVNAME	DeviceName string data, max length = 7	(0x21)		0x50 - 0x57
DEVCHM	DeviceChemistry string data, max length = 5	(0x22)		0x60 - 0x65
MANDT	ManufacturerData string data, max length = 5	(0x23)		0x70 - 0x75
IOVLDL	Current overload, absolute value low	(0x26)	lsb	0x4c
IOVLDH	Current overload, absolute value high		msb	0x4d
BLPCT	Battery low %, relative capacity at EDV1 BLPCT = 2.56 * (%RM at EDV1)	(0x27)	lsb	0x4e
UNUSED			msb	0x4f
TAPERL	Li-Ion taper current low, 2's	(0x2c)	lsb	0x58
TAPERH	Li-Ion taper current high, 2's		msb	0x59
MAXOVQL	Maximum overcharge limit low, 2's	(0x2d)	lsb	0x5a
MAXOVQH	Maximum overcharge limit high, 2's		msb	0x5b
MFLAG	Master mode flag register	(0x2e)	lsb	0x5c
BUSYFLG	Access protect register		msb	0x5d
FLGS1	FLAGS1 register	(0x2f)	lsb	0x5e
FLGS2	FLAGS2 register		msb	0x5f
IRES60L	Current-measurement gain factor low	(0x33)	lsb	0x66
IRES60H	Current-measurement gain factor high IRES60 = $192/R_{SR}$		msb	0X67
VOFF	Battery voltage offset trim, signed integer in mV bvolt = (Vsb*1000+VOFF)*(NCELLS + NCCAL/256) (mV)	(0x34)	lsb	0x68
TTRIM	Temperature trim, [0.1K] btemp = TTRIM + raw temp calc (.1°K), nominal value = 80°		msb	0x69
MT_DT	Max Temp fault/ Delta Temp step value (°C) MT=b7-4, maxT = 69 - (MT*1.6) (°C) DT=b3-0, ΔT step = 16+DT*2 (0.1°C)	(0x35)	lsb	0x6a
CEFF	Charge efficiency, LEFF=b7-4, HEFF=b3-0 LEFF, HEFF = [eff(%)*256 - 196]/4		msb	0x6b
FULPCT	Full-charge percentage, 2's complement	(0x36)	lsb	0x6c
DIGFIL	Digital filter value = 0.045/Vsrd (s)		msb	0x6d
DELCAP	Current integration gain factor = 3.2/Rrsr (mAh/256)	(0x37)	lsb	0x6e

RAM Locations for Test/Calibration/Programming (Continued)

Name	Description	CMD		RAM Address
SDRATE	Self-discharge rate, SDRATE = 2's[52.73/X], X = % discharge rate per day		msb	0x6f
NCCAL	Number of cells fraction	(0x3b)	lsb	0x76
NCELLS	Number of cells integer, Voltage gain = NCELLS + NCCAL/256		msb	0x77
I2CWAA	I^2C write EEPROM address to update (MUST BE EVEN)	(0x3c)	lsb	0x78
I2CWAK	I^2C write access key {0xb3}		msb	0x79
MCHGIL	EDVF charging current low (used below EDVF)	(0x3d)	lsb	0x7a
MCHGIH	EDVF charging current high (used below EDVF)		msb	0x7b
EDV1L	EDV1 threshold low, 2's complement	(0x3e)	lsb	0x7c
EDV1H	EDV1 threshold high, 2's complement		msb	0x7d
EDVFL	EDVF threshold low, 2's complement	(0x3f)	lsb	0x7e
EDVFH	EDVF threshold high, 2's complement		msb	0x7f
DTTIM	Δ t step = 320 - DTTIM * 20 [s], ΔT timer = b4-7	(0x41)	lsb	0x82
HLDTIM	Hold-off time = 320 - HLDTIM * 20 [s]		msb	0x83

Bit Registers

Name	b15	b14	b13	b12	b11	b10	b9	b8
Bat-Modeh (0x03)	**mWh**	**ChgrMod**	**DIS-MAST**	-	-	-	-	-
	b7	b6	b5	b4	b3	b2	b1	b0
BatModel (0x03)	**Req Cond. Cycle**	-	-	-	-	-	-	-
	b15	b14	b13	b12	b11	b10	b9	b8
Batsth (0x16)	**OvrChg Alarm**	**TermChg Alarm**	**Reserved**	**OvrTemp Alarm**	**TermDsg Alarm**	-	**RemCap Alarm**	**RemTime Alarm**
	b7	b6	b5	b4	b3	b2	b1	b0
Batstl (0x16)	**Initialized**	**Dsg**	**FullyChg**	**FullyDsg**	**smb error**	**smb error**	**smb error**	**smb error**
	b15	b14	b13	b12	b11	b10	b9	b8
FLAGS2 (0x2f)	**DMODE**	**PSTAT**	**CHM**	**CC**	**ENINT (DISMM)**	**OV**	**LTF**	**OC**
	b7	b6	b5	b4	b3	b2	b1	b0
FLAGS1 (0x2f)	ΔT/Δt	**IMIN**	**VQ**	-	**VDQ**	**OVLD**	**EDV1**	**EDVF**

E^2 Map

Name	Description	CMD		E^2addr (bq2040)
EELENGTH	EEPROM length Number of bytes to read from EEPROM = 0x64			0x00 *
CHKBYTE1	EEPROM check 1 MUST equal 0x5b			0x01 *
RTMALML	Remaining time alarm low	(0x02)	lsb	0x02 *
RTMALMH	Remaining time alarm hi	(0x02)	msb	0x03 *
RCPALML	Remaining capacity alarm low	(0x01)	lsb	0x04 *
RCPALMH	Remaining capacity alarm hi	(0x01)	msb	0x05 *
UNUSED	Reserved		lsb	0x06
UNUSED	Reserved		msb	0x07
CHGIL	Initial charging current after reset low	(0x14)	lsb	0x08
CHGIH	Initial charging current after reset hi	(0x14)	msb	0x09
CHGVL	Charging voltage low	(0x15)	lsb	0x0a
CHGVH	Charging voltage hi	(0x15)	msb	0x0b
BATSTL	Initial BatteryStatus low	(0x16)	lsb	0x0c
BATSTH	Initial BatteryStatus hi	(0x16)	msb	0x0d
CYCLEL	Cycle count low byte	(0x17)	lsb	0x0e
CYCLEH	Cycle count hi byte	(0x17)	msb	0x0f
DESCAPL	Design capacity low byte	(0x18)	lsb	0x10
DESCAPH	Design capacity hi byte	(0x18)	msb	0x11
DESVL	Design voltage low	(0x19)	lsb	0x12
DESVH	Design voltage hi	(0x19)	msb	0x13
SPECL	Specification information low	(0x1a)	lsb	0x14
SPECH	Specification information hi	(0x1a)	msb	0x15
MDATEL	Manufactures date low	(0x1b)	lsb	0x16
MDATEH	Manufactures date hi	(0x1b)	msb	0x17
SERNUML	Serial number low byte	(0x1c)	lsb	0x18
SERNUMH	Serial number hi byte	(0x1c)	msb	0x19
FCHGIL	Fast-charging current low	(0x1d)	lsb	0x1a
FCHGIH	Fast-charging current hi	(0x1d)	msb	0x1b
TCHGIL	Maintenance charging current low	(0x1e)	lsb	0x1c
TCHGIH	Maintenance charging current hi	(0x1e)	msb	0x1d
NACL	Initial NAC value low	(0x1f)	lsb	0x1e
NACH	Initial NAC value hi	(0x1f)	msb	0x1f

E^2 Map (Continued)

Name	Description	CMD		E^2addr (bq2040)
	Manufacturer name string data	(0x20)		0x20 - 0x2b
MANFNAM	String length, max = 11			0x20 *
	ASCII character #1			0x21 *
	ASCII character #2			0x22 *
	ASCII character #3			0x23 *
	ASCII character #4			0x24 *
	ASCII character #5			0x25 *
	ASCII character #6			0x26 *
	ASCII character #7			0x27 *
	ASCII character #8	(0x24)	lsb	0x28
	ASCII character #9	(0x24)	msb	0x29
	ASCII character #10	(0x25)	lsb	0x2a
	ASCII character #11	(0x25)	msb	0x2b
IOVLDL	Current overload, absolute value low	(0x26)	lsb	0x2c
IOVLDH	Current overload, abolute value high	(0x26)	msb	0x2d
BLPCT	Battery low %, relative capacity at EDV1 BLPCT = 2.56 *(%RM at EDV1)	(0x27)	lsb	0x2e
UNUSED		(0x27)	msb	0x2f
	Device name string data	(0x21)		0x30 - 0x37
DEVNAME	String length, max = 7	(0x28)	lsb	0x30 *
	ASCII character #1	(0x28)	msb	0x31 *
	ASCII character #2	(0x29)	lsb	0x32
	ASCII character #3	(0x29)	msb	0x33
	ASCII character #4	(0x2a)	lsb	0x34
	ASCII character #5	(0x2a)	msb	0x35
	ASCII character #6	(0x2b)	lsb	0x36
	ASCII character #7	(0x2b)	msb	0x37
TAPERL	Li-Ion taper current low, 2's	(0x2c)	lsb	0x38
TAPERH	Li-Ion taper current high, 2's	(0x2c)	msb	0x39
MAXOVQL	Maximum overcharge limit low, 2's	(0x2d)	lsb	0x3a
MAXOVQH	Maximum overcharge limit high, 2's	(0x2d)	msb	0x3b
MFLAG	Master mode flags initial value (Program to 0)	(0x2e)	lsb	0x3c
BUSYFLG	Access protect (Program to 0xb0 for pack access protect, 0xb8 for unprotected pack access)	(0x2e)	msb	0x3d
FLGS1	FLAGS1 register initial value	(0x2f)	lsb	0x3e
FLGS2	FLAGS2 register initial value	(0x2f)	msb	0x3f
	Device chemistry string data	(0x22)		0x40 - 0x45
DEVCHM	String length, max = 5	(0X30)	lsb	0X40 *
	ASCII character #1	(0x30)	msb	0X41 *
	ASCII character #2	(0X31)	lsb	0X42
	ASCII character #3	(0x31)	msb	0X43
	ASCII character #4	(0X32)	lsb	0X44
	ASCII character #5	(0x32)	msb	0X45

16/18

E^2 Map (Continued)

Name	Description	CMD		E^2addr (bq2040)
IRES60L	Current-measurement gain factor low	(0x33)	lsb	0x46
IRES60H	Current-measurement gain factor high IRES60 = 192/R_{SR}	(0x33)	msb	0X47
VOFF	Battery voltage offset trim, signed integer in mV bvolt = (Vsb*1000+VOFF)*(NCELLS + NCCAL/256) (mV)	(0x34)	lsb	0x48
TTRIM	Temperature offset trim, [0.1°K] btemp = TTRIM + raw temp calc (.1°K), nom val = 80°	(0x34)	msb	0x49
MT_DT	Max Temp fault/ Delta Temp step value (°C) MT=b7-4, maxT = 69 - (MT*1.6) (°C) DT=b3-0, ΔT step = 16+DT*2 (0.1°C)	(0x35)	lsb	0x4a
CEFF	Charge efficiency, LEFF=b7-4, HEFF=b3-0 LEFF, HEFF = [eff(%)*256 - 196]/4	(0x35)	msb	0x4b
FULPCT	Full-charge percentage, 2's complement	(0x36)	lsb	0x4c
DIGFIL	Digital filter value = 0.045/Vsrd (s)	(0x36)	msb	0x4d
DELCAP	Current integration gain factor = 3.2/Rrsr (mAh/256)	(0x37)	lsb	0x4e
SDRATE	Self-discharge rate SDRATE = 2's[52.73/X], X = % discharge rate per day	(0x37)	msb	0x4f
MANDT	Manufacture data string data	(0x23)		0x50 - 0x55
	String length, max = 5	(0x38)	lsb	0x50 *
	ASCII character #1	(0x38)	msb	0x51 *
	ASCII character #2	(0x39)	lsb	0x52
	ASCII character #3	(0x39)	msb	0x53
	ASCII character #4	(0x3a)	lsb	ox54
	ASCII character #5	(0x3a)	msb	ox55
NCCAL	Number of cells fraction	(0x3b)	lsb	0x56
NCELLS	Number of cells integer, Voltage gain1 = NCELLS + NCCAL/256	(0x3b)	msb	0x57
I2CWAA	I^2C write EEPROM address, Program to 0x00	(0x3c)	lsb	0x58
I2CWAK	I^2C write access key, Program to 0x00	(0x3c)	msb	0x59
MCHGIL	EDVF charging current low (used below EDVF)	(0x3d)	lsb	0x5a
MCHGIH	EDVF charging current high (used below EDVF)	(0x3d)	msb	0x5b
EDV1L	EDV1 threshold low, 2's complement	(0x3e)	lsb	0x5c
EDV1H	EDV1 threshold high, 2's complement	(0x3e)	msb	0x5d
EDVFL	EDVF threshold low, 2's complement	(0x3f)	lsb	0x5e
EDVFH	EDVF threshold high, 2's complement	(0x3f)	msb	0x5f

E^2 Map (Continued)

Name	Description	CMD		E^2addr (bq2040)
FULCAPL	Full-charge capacity low	(0x10)	lsb	0x60 *
FULCAPH	Full-charge capacity high	(0x10)	msb	0x61 *
DTTIM	Δ t step (b0-3) = 320 - DTTIM * 20 [s]	(0x41)	lsb	0x62
HLDTIM	Hold-off time (b0-3) = 320 - HLDTIM * 20 [s]	(0x41)	msb	0x63
CHKBYTE2	Check byte 2 MUST equal 0xb5			0x64 *
RESERVED				0x65 - 0x7f

* Difficult or impossible to update with SMB write-through function

UNITRODE

U-514 Using the bq2010

A Tutorial for Gas Gauging

Introduction

This tutorial introduces the bq2010 Gas Gauge IC (secondary battery available charge monitor). The tutorial should be used with the bq2010 data sheet when designing with or evaluating the bq2010.

The bq2010 Gas Gauge IC is a complete battery monitoring product for NiMH and NiCd batteries. The bq2010 16-pin SOIC provides significant advantages:

- A complete single-chip system solution for in-the-pack monitoring of a battery's available charge
- No battery technology expertise required
- Minimal engineering required, typically a single PCB layout specific to the application
- No software required for stand-alone battery-pack applications
- Single-wire serial interface for communication with an external processor to implement a customized display
- Direct LED display drive

This tutorial describes capacity monitoring, compares Unitrode's gas gauge solutions to microprocessor-based implementations, describes device operation in general terms, and addresses implementation issues.

Available Charge Monitoring

Rechargeable batteries are used in many different applications, from cellular phones, portable computers, and medical equipment to power tools. The operating environment of these batteries covers a wide range of temperatures; therefore, battery efficiency changes due to battery temperature and rate of charge or discharge. The bq2010 compensates for both temperature and charge/discharge rate continuously.

The battery available charge can be displayed on LEDs and can be accessed via the serial port. The calculated available charge of the battery is also compensated according to battery temperature because the actual available charge is reduced at lower temperatures. For example, if the bq2010 indicates that the battery is 60% full at a temperature of 25°C, then the bq2010 indicates 40% full when cooled to 0°C, which is the predicted available charge at that temperature. When the temperature returns to 25°C, the displayed capacity returns to 60%. This ensures that the indicated capacity is always conservatively representative of the charge available for use under the given conditions.

The bq2010 also adjusts the available charge for the approximate internal self-discharge that occurs in NiCd or NiMH batteries. The self-discharge adjustment is based on the selected rate, elapsed time, battery charge level, and temperature. This adjustment provides a conservative estimate of self-discharge that occurs naturally and that is a significant source of discharge in systems that are not charged often or are stored at elevated temperatures.

Comparing bq2010 Solution with MCU-Based Implementations

Low-power, single-chip microprocessors such as those available from Motorola, Toshiba, NEC, and others have been used to implement gas gauges in battery-powered equipment, notably camcorders and laptop computers. Although adequate, these implementations require extensive development efforts to be suitable for use in a battery pack, and even then, require significant space in the pack because of the high component count.

The bq2010 by comparison offers efficiency, ease of use, simplicity of design, and low component count. With careful PCB layout, the bq2010 system can fit in the space between AA batteries. Table 1 compares the bq2010 and a typical MCU gas gauge implementation.

bq2010 Operation

Gas gauging is accomplished by measuring the charge input to and subsequently removed from a battery. This is done by monitoring the voltage drop across a low-value resistor (typically 20 to 100mΩ) during charge and discharge. This voltage is integrated over time, scaled, and used to drive two 16-bit internal counters:

- Nominal Available Charge (NAC) counter—represents the amount of charge available from the battery.
- Discharge Count Register (DCR)—represents the amount of charge removed from the battery since it was last full.

Also, the Last Measured Discharge (LMD) register is an eight-bit register used to store the most recent count value representing "battery full."

In a typical situation, the Unitrode Gas Gauge ICs are installed in a battery pack containing unconditioned batteries with an unknown charge state.

On application of power to the bq2010, the following assumptions are made:

- The battery is empty; therefore, the NAC is zero.
- The battery's storage capacity is the Programmed Full Count (PFC) as specified by the programming inputs, which are loaded into the LMD.

The actual storage capacity of the battery has yet to be determined. The battery capacity can be learned by charging the battery until NAC = LMD (LMD = PFC on initialization) and then discharging the battery until the cell voltage reaches the End-of-Discharge Voltage (EDV1) threshold (1.05V for the bq2010). As discharge occurs, the bq2010 tracks the amount of charge removed from the battery in the DCR. The new battery capacity (DCR) is transferred to the LMD if no partial charges have occurred, the temperature is above 10°C, and self-discharge accounts for less than 8 to 18% of the DCR when EDV1 was reached. The valid discharge flag (VDQ) in the bq2010 indicates whether the present discharge is valid for LMD update.

Table 1. Comparing bq2010 and MCU Implementations

Feature	MCU Implementation	bq2010 Solution
Small size	>> 1 square inch; requires extra battery pack space	≤ 1 square inch; fits between batteries
Operating current (not including LEDs)	Typically ≥ 1mA awake; as low as 10µA asleep	125µA typical
LED display	Yes	Yes
Serial I/O	Depends on programming	Yes
Programmable capacity	Depends on programming	Yes
Self-discharge	Generally not implemented	Yes, with temperature compensations
Charge, discharge rate compensations	Generally not available but depends on programming	Yes
Charge, discharge temperature compensations	Generally not available but depends on programming; requires a thermistor	Yes, uses internal temperature sensor
Programming requirements	Extensive MCU programming required for gas gauge functions; possible host programming, algorithm development, and software testing	No programming for stand-alone applications; small host code for serial I/O applications
Hardware design requirements	Extensive low-power-design, op amp, analog switch, MCU, resonator, low-power regulator, LEDs, sense resistor; component count = 56 typical	No engineering required; component count = 23 typical: bq2010, nFET, LEDs, sense resistor, programming resistors and capacitors

Discharging Before the First Charge

Most battery pack manufacturers will assemble their packs with the bq2010 and ship the packs without charging. When the customer receives a new pack, the gas gauge indicates EMPTY, and the customer then charges the pack until it indicates full. It is possible that fast-charge terminates before the gas gauge shows full because the available capacity of the battery was not zero.

The battery pack manufacturer may want to instruct the user to discharge the battery to EDV before charging. Once this condition is reached, the battery can be fast-charged until termination—allowing NAC to count up to LMD. Now, the gas gauge is synchronized with the battery and learns the true battery capacity on the next valid discharge cycle.

For applications with LED displays, the complete discharge of the battery pack is indicated by LED_1 blinking. For applications using the serial I/O port, complete discharge is indicated when the final end-of-discharge voltage (EDVF) flag is set.

To ensure that the bq2010 accurately predicts the amount of available charge, battery pack manufacturers should instruct their end-users to completely discharge a new battery pack and then charge it until the charger terminates.

Alternatively, the NAC can be written with an estimated battery capacity during pack assembly or testing. The user may then charge the battery so NAC = LMD. The actual capacity is "learned" on the next valid discharge. The appropriate value must be written into the NAC register for proper operation.

Using the bq2010

The bq2010 IC is simple to use and implement into a system. Figure 1 shows the bq2010 configured for full functionality. Almost all of the external connections and components are *optional*, as indicated by the dotted lines. For example, most stand-alone applications do not need the EMPTY pin connection or the DQ port.

All the external components can be surface-mounted. The sense resistor could fit in the space between most cells, and the populated PCB may fit in that space with the correct layout. A bq2010 Gas Gauge IC could, therefore, be added to existing battery packs with little retooling of plastics.

Monitoring the Battery

To determine and track the charge state of the battery, the bq2010 monitors both the divided battery voltage and the voltage drop across the sense resistor.

The divided battery voltage (V_{SB}) is provided by a resistor-divider that divides the battery pack voltage down to a single-cell voltage. V_{SB} is primarily used to determine when the battery has reached the EDV1 threshold so that the new battery capacity determined during discharge may be saved in the LMD. V_{SB} is also used for EDVF determination, battery-removed indication, and battery-replaced indication.

The battery current is monitored using a low-value sense resistor attached to the negative terminal of the battery. The current through the resistor generates a proportional voltage drop, V_{SR}, which is provided to the SR input of the bq2010.

Picking a Sense Resistor

The sense resistor is used to measure the current flowing into or out of the battery. The sense resistor value depends on the currents being measured. The bq2010 specification for V_{SR} ranges from a maximum of 2.0V for charging to -300mV for discharging. The offset error for the bq2010 relative to V_{SR} is ± 150µV.

In general, a sense resistor should be selected so that: (a) the voltage drop across that resistor exceeds 5 to 7mV for the lowest current representing the majority of the battery drain, and (b) the lowest practical V_{SR} voltage drop is achieved to maximize the useful voltage available from the battery pack.

For example, Table 2 summarizes the approximate current requirements for a laptop computer application. The majority of the battery capacity is used in run (no disks) mode. The next largest amount of battery capacity is used in run (with disks) mode, with suspend mode consuming the least amount of battery capacity, even though it makes up the largest block of time.

If a 0.1Ω sense resistor is used, the voltage input to SR is as shown. This means that for both run modes, the integrator repeatability error is a maximum of 2% because $|V_{SR}|$ is well above 30mV. Although the repeatability error associated with suspend mode is approximately 5%, its total error contribution is only 0.5% because suspend mode is responsible for only 10% of the total consumption.

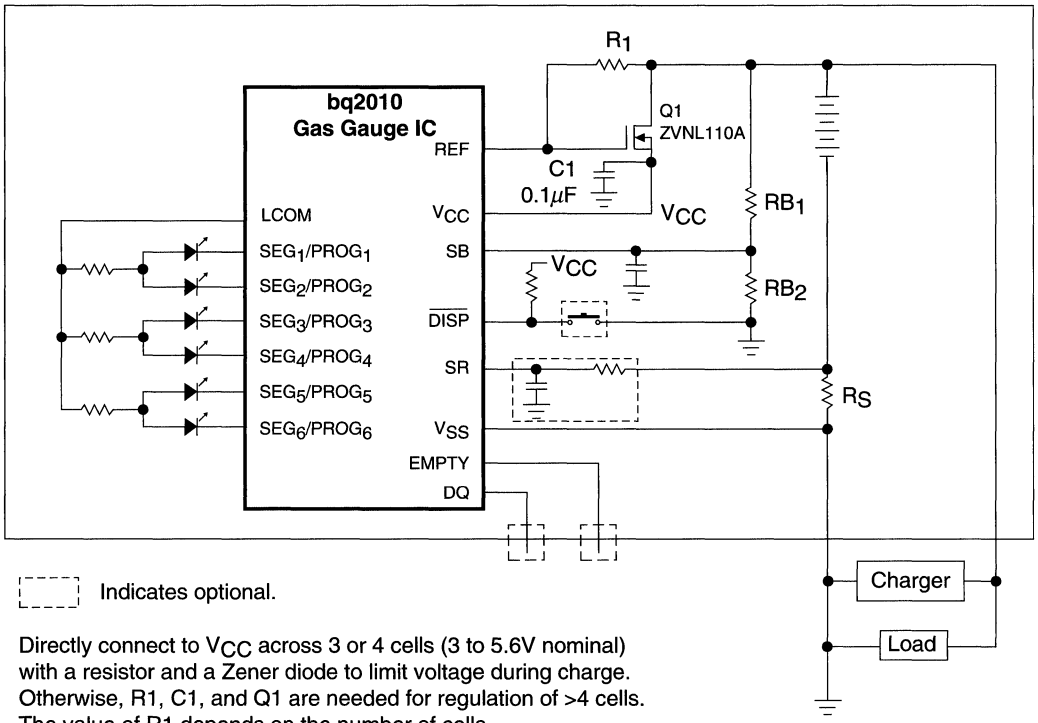


Figure 1. bq2010 Application Diagram—LED Display

Table 2. Approximate Laptop Computer Current Requirements

Mode	Current (A)	0.1Ω Voltage Drop (mV)	Time (min.)	% of Battery Usage
Run (with disks)	1	100.0	20	16.7
Run (no disks)	0.5	50.0	175	72.9
Suspend	0.05	5	250	10.4

Selecting PFCs

When the bq2010 is first connected to the battery pack, a Programmed Full Count (PFC) representing the initial full battery capacity is loaded into the LMD. To select this PFC, determine the initial full battery capacity value in mVh by multiplying the manufacturer's battery capacity rating in mAh by the sense resistor value:

$$mVh = mAh * R_{SNS}$$

Find the nearest corresponding value in Table 3 that is *less than* the calculated mVh value, and then set the programming pin levels to select the Programmed Full Count (PFC), scale, and scale multiplier associated with that value.

Nine PFC settings are available using $PROG_1$ and $PROG_2$, which together with scale ($PROG_3$ and $PROG_4$) settings provide a wide range of initial full battery values. ($PROG_5$ is used to select the self-discharge compensations for either NiMH or NiCd batteries; $PROG_6$ is used to determine the display mode of the bq2010 as described on page 6.)

For example, if a 0.1Ω sense resistor is being used, and the battery is rated at 1100mAh, then the initial full battery value is 110mVh. The nearest available value that is less than 110mVh from Table 3 is 106mVh, which corresponds to $PROG_1$ = Z, $PROG_2$ = Z, $PROG_3$ = L, and $PROG_4$ = L.

Note that some cells in Table 3 have identical initial full battery values. For example, 141mVh can be found two places:

- Example 1: $PROG_1$ = L, $PROG_2$ = L, $PROG_3$ = Z, $PROG_4$ = L = 141mVh
- Example 2: $PROG_1$ = H, $PROG_2$ = Z, $PROG_3$ = L, $PROG_4$ = L = 141mVh

Example 1 corresponds to a PFC of 22528 of 65535 possible counts (34.4%). This means that, in all likelihood, a majority of the counter range will remain unused. Counter resolution could be increased by using the settings in example 2. In this case, the PFC is 45056 of 65535 counts (68.8% of range). In general, when faced with a choice, it is better to pick the finer resolution (that is, a larger PFC).

$PROG_3$ and $PROG_4$ inputs determine the scale to be used by the bq2010. Together these two pins determine the mVh value of a single NAC count. Thus, for any given PFC selected by $PROG_1$ and $PROG_2$, the capacity represented by that PFC (in mVh) is given by:

$$PFC * scale$$

Note that the scale value is given for a $PROG_3$, $PROG_4$ pair at the top of each column in Table 3.

Table 3. bq2010 Programmed Full Count mVh Selections

$PROG_x$		Programmed Full Count (PFC)	$PROG_4$ = L			$PROG_4$ = Z			Units
1	2		$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	
-	-	-	Scale = 1/80	Scale = 1/160	Scale = 1/320	Scale = 1/640	Scale = 1/1280	Scale = 1/2560	mVh/ count
H	H	49152	614	307	154	76.8	38.4	19.2-	mVh
H	Z	45056	563	282	141	70.4	35.2	17.6	mVh
H	L	40960	512	256	128	64.0	32.0	16.0	mVh
Z	H	36864	461	230	115	57.6	28.8	14.4	mVh
Z	Z	33792	422	211	106	53.0	26.4	13.2	mVh
Z	L	30720	384	192	96.0	48.0	24.0	12.0	mVh
L	H	27648	346	173	86.4	43.2	21.6	10.8	mVh
L	Z	25600	320	160	80.0	40.0	20.0	10.0	mVh
L	L	22528	282	141	70.4	35.2	17.6	8.8	mVh
VSR equivalent to 2 counts/sec. (nom.)			90	45	22.5	11.25	5.6	2.8	mV

Using the Programming Pins

The bq2010 is programmed through the LED display pins during a special programming cycle that occurs during power-up or during a device reset.

Programming Without LED Display

In applications where the LED display is not used, programming is very simple. The bq2010 may be programmed by tying each programming pin directly to the appropriate level:

H = V_{CC}

Z = open

L = V_{SS}

LED outputs must be disabled by tying $\overline{DISP}$ to V_{CC}. LCOM may remain open.

Programming With LED Display

When the LED display is used, it is necessary to provide programming information with either a pull-up resistor to V_{CC}, a pull-down resistor to V_{SS} (200KΩ value in either case), or no resistor at all. The logic states are set as follows:

H ≤ 200K to V_{CC}

Z = no resistor

L ≤ 200K to V_{SS}

LCOM must be used to provide power to the LEDs so that they may be disabled during reading of the programming resistors (see Figure 1).

Selecting Battery Chemistry

$PROG_5$ is used during power-up to select self-discharge compensations for either NiMH or NiCd batteries. $PROG_5$ = Z for NiCd and L for NiMH batteries.

Using the LED Display

The bq2010 supports 6 LEDs that display a gauge of available battery charge. LEDs 1 through 5 provide 20% step indication of charge, while the sixth LED indicates "overfull" when the display is operating in absolute mode ($PROG_6$ = Z).

Selecting Display Mode

$PROG_6$ is used during power-up to determine the display mode of the bq2010. The bq2010 uses either absolute or relative battery charge state as described below ($PROG_6$ = Z or L, respectively).

The display indicates available battery charge as a percentage of "battery full." This is based on the current LMD value ("relative" mode) or on the PFC value (the initial battery capacity value programmed, "absolute" mode). Relative mode is for applications where the customer does not want to see on the display the decline in battery capacity following many charge/discharge cycles. Absolute mode is for applications when the customer wants each segment to represent a fixed amount of charge.

Display Activation

The LED display is normally maintained in the OFF state to conserve battery power. It is activated during a high rate of battery charge and discharge if $\overline{DISP}$ is floating, or continuously if the $\overline{DISP}$ pin is pulled to V_{SS}. When the display is not used, the $\overline{DISP}$ pin can be tied to V_{CC} to disable the display and allow the pins to be used strictly as programming pins.

LED Supply

The current source for the LEDs is provided through the LCOM pin in all applications, because the programming inputs and the LED outputs share common pins. When the bq2010 is initially powered-up, the LCOM output is disabled, thus allowing the pins to be sensed for the presence of programming resistors tied to V_{CC} or V_{SS} (see Figure 1).

Standard LEDs such as the Sharp PR series should provide adequate performance at low cost. For better results, customers could use a high-brightness LED (low current) such as the more expensive Sharp LR or UR series. The suitability of any particular LED depends not only on its luminosity at rated current, but also the packaging and lensing technique used (very important in concentrating viewable energy, especially for high-ambient-light conditions).

Using the DQ Serial Port

The bq2010 is also equipped with a bidirectional single-line serial I/O port (DQ) that allows it to conveniently communicate with a host processor.

Data Interface

The DQ serial port allows the implementation of gas gauge functions without the need for the LED display. For example, in cellular telephone and laptop computer applications, the LED display is not needed because an LCD is available. The host processor in these cases can simply obtain the gas gauge display step and the temperature over the serial port and use these to indicate available charge. The gas gauge step data is a 4-bit value that represents 1 of 16 possible steps (6.25% of full per step), giving a greater possible display accuracy than is possible with the LED display.

In a more sophisticated approach, the host may obtain the NAC, LMD, temperature, and operational status flags, and then use these to customize and display functions and features.

Battery Pack Testing

The DQ serial port is also useful for final testing of assembled battery packs. The bq2010 can be exercised from a host processor over the DQ serial port—allowing the host to directly control the state of the LED output pins and the EMPTY pin. The state of the programming pins may also be checked. A battery ID byte (stored in on-chip RAM) allows the manufacturer to identify battery types.

Using the EMPTY Pin

The EMPTY pin provides external control for automatic load disconnection on low battery, preventing deep discharge. It activates when V_{SB} drops below the EDVF threshold.

Supplying Power to the Part

The V_{CC} specification for the bq2010 is:

$$3.0V \leq V_{CC} \leq 6.5V$$

This may be achieved in several ways under various battery configurations.

Direct Battery Power

The bq2010 may be powered directly from the batteries in configurations of 3 or 4 cells. When using unregulated direct battery power, ensure that the battery voltage does not exceed the maximum of 6.5V or fall below the minimum operational value of 3.0V.

Direct unregulated power supply should be limited to situations where varying or pulsed load conditions during discharge or charge do not cause battery voltage spikes. Such spikes typically result when batteries drive switching power supplies that use inductive storage, or when start-up transients in motors produce significant voltage spikes on the battery.

Low-Cost nFET Regulator

Most applications require some kind of voltage regulator to supply V_{CC} within specifications over a broad range of battery voltage conditions. The bq2010 provides support for a low-cost regulator circuit consisting of an nFET and the on-chip reference voltage V_{REF}.

Across temperature, V_{REF} ranges from 4.5V to 7.5V, given an I_{REF} of 5µA, where:

$$V_{CC} = V_{REF} - V_{GS}$$

where V_{GS} is the gate-source voltage of the nFET, Q1. When the battery voltage drops below V_{REF}, the R1/R_{REF} divider determines V_{CC}. A low-threshold nFET exhibiting a maximum V_{GS} of 0.8 to 1.5V may be adequate for this circuit. An example is the BSS138ZX from Zetex. The correct choice for R_1 is a function of the number of cells in the battery pack. Table 4 lists different values for R_1 for various battery packs.

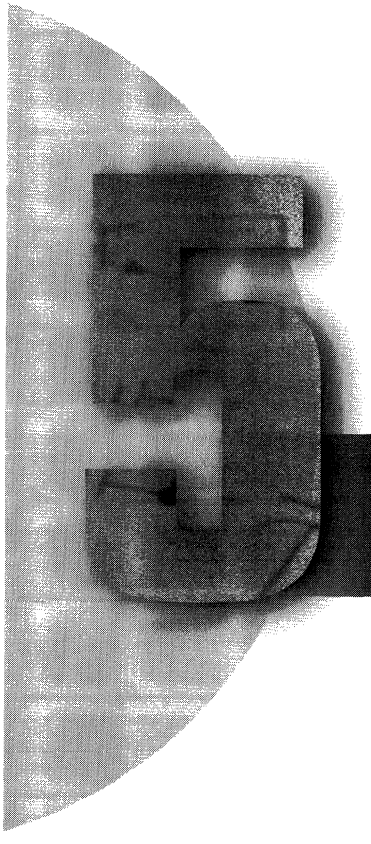
Table 4. Reference Bias Resistor R_1 Selection

Assuming a Nominal Q1 V_{GS} = 1.5V

Number of Cells	R1 (Ω)
5	33K
6	100K
7	180K
8	240K
9	300K
10	390K
11	430K

Split Battery Configurations

When a battery pack contains a large number of cells, the bq2010 may be operated from a small number of cells inside the larger pack. This is possible as long as the current required for LED operation does not significantly reduce the available charge of the small cell cluster relative to the available charge of the other cells in the pack. Generally, it is best not to use the bq2010 display in this configuration.



Battery-Management Modules

Battery-Management Modules Selection Guide

Unitrode's battery management module products provide true turn-key solutions for capacity monitoring and charge control of NiCd, NiMH, Li-Ion, or Rechargeable Alkaline battery packs. Designed for battery pack integration, the small boards contain all necessary components to easily implement intelligent or smart battery packs in a portable system. The wide selection of boards offers battery monitoring, capacity tracking, charge control, and remaining capacity communication to the host system or user. The boards are fully tested and provide direct cell connections for simple battery packs.

- ➤ Turnkey solutions for intelligent or smart batteries for portable equipment
  - – Computers, cellular phones, and camcorders
  - – Handheld terminals
  - – Communication radios
  - – Medical and test equipment
  - – Power tools
- ➤ Capacity monitoring and charge control
- ➤ Pushbutton-activated LED capacity indication
- ➤ Designed for battery pack integration
  - – Small size
  - – Low power
  - – Direct cell connections

5

Battery Technology	Key Features	Part Number	Page Number
NiCd/NiMH	Capacity monitoring, LED indication, serial communications port	bq2110	5-2
	Capacity monitoring, slow-charge control, LED indication, serial communications port	bq2112	5-14
	Capacity monitoring, charge control output, LED indication, serial communications port	bq2114	5-24
	Capacity monitoring and fast charge control	bq2164	5-71
NiCd	Capacity monitoring for high discharge rates, LED indication	bq2111L	5-8
NiCd/NiMH, Lead Acid	Capacity monitoring, LED indication, single-wire serial communications port	bq2113H+	5-20
Li-Ion	Capacity monitoring, Smart Battery data set and interface, LED indication, pack supervision, 4-segment LED indication	bq2148	5-40
	Capacity monitoring, LED indication, serial communications port	bq2150 bq2150H	5-47 5-53
	Pack supervision: overvoltage, undervoltage, and overcurrent control	bq2158 bq2158T	5-57 5-64
	Capacity monitoring, 3- or 4-cell pack supervision, and LED indication	bq2167+ bq2168+	5-77 5-85
NiCd/NiMH/ Lead Acid/ Li-Ion	Capacity monitoring, Smart Battery data set and interface, 5- segment LED indication	bq2145	5-34
	Capacity monitoring, Smart Battery data set and interface, 4-segment LED indication	bq219XL	5-93
Any	Charge and discharge counting, serial communication port, single-wire interface	bq2118	5-30

+ New Product

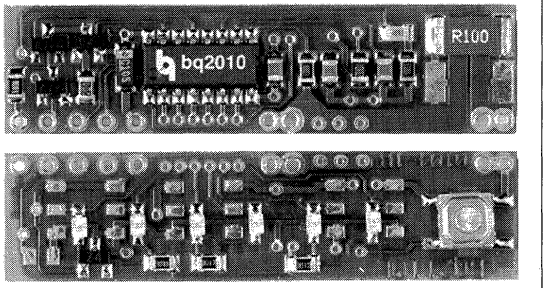
UNITRODE

bq2110

NiCd or NiMH Gas Gauge Module

Features

- Complete bq2010 Gas Gauge solution for NiCd or NiMH battery packs
- Battery information available over a single-wire bidirectional serial port
- Battery state-of-charge monitoring for 4- to 12-cell series applications
- On-board regulator allows direct connection to the battery
- "L" version includes push-button activated LEDs to display state-of-charge information
- Nominal capacity and cell chemistry pre-configured
- Compact size for battery pack integration



General Description

The bq2110 Gas Gauge Module provides a complete and compact solution for capacity monitoring of NiCd and NiMH battery packs. Designed for battery pack integration, the bq2110 incorporates a bq2010 Gas Gauge IC, a current sense resistor, and all other components necessary to accurately monitor and display the capacity of 4 to 12 series cells. The bq2110L includes six surface-mounted LEDs to display remaining capacity in 20% increments of the learned capacity (relative mode) or programmed capacity (absolute mode). The sixth LED is used in absolute mode to represent an overfull condition (charge above the programmed capacity). The LEDs are activated with the onboard push-button switch.

Contacts are provided on the bq2110 for direct connection to the battery stack (BAT+, BAT-), the serial communications port (DQ), and the empty indicator (EMPTY). Please refer to the bq2010 data sheet for the specifics on the operation of the Gas Gauge.

Unitrode configures the bq2110 based on the information requested in Table 1. The configuration defines the number of series cells, the nominal battery pack capacity, the self-discharge rate, and the LED display mode.

A module development kit is also available for the bq2110. The bq2110B-KT or bq2110LB-KT includes one configured module and the following:

1) An interface board that allows connection to the serial port of an AT-compatible computer.
2) Menu-driven software with the bq2110 to display charge/discharge activity and to allow user interface to the bq2010 from any standard DOS PC.
3) Source code for the TSR.

Pin Descriptions

P1	**DQ/Serial communication port**
P2	**BAT+/Battery positive/pack positive**
P3	**No connect**
P4	**EMPTY/Empty indicator output**
P5	**GND/Ground**
P6	**PACK-/Pack negative**
P7	**BAT-/Battery negative**

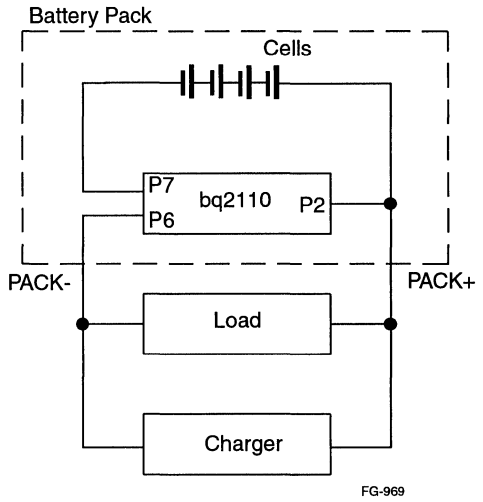


Figure 1. Module Connection Diagram

Table 1. bq2110 Module Configuration

Customer Name: _____

Contact: _____ Phone: _____

Address: _____

_____

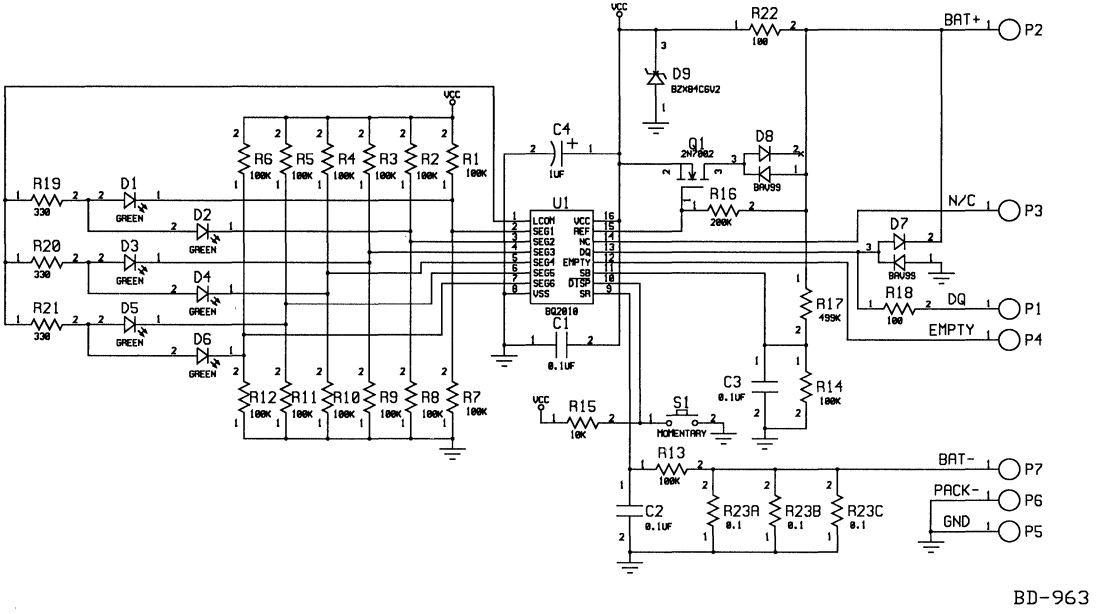
Sales Contact: _____ Phone: _____

Number of series battery cells (4-12)	_____
Battery type (NiCd or NiMH)	_____
Battery pack capacity (mAh)	_____
Discharge rate into load (3.0A max)	Min._____ Avg._____ Max._____
Charge rate (3.0A max)	_____
Display mode (absolute or relative)	_____
LEDs and switch (Y/N)	_____

FAE approval: _____ Date:_____

2/6

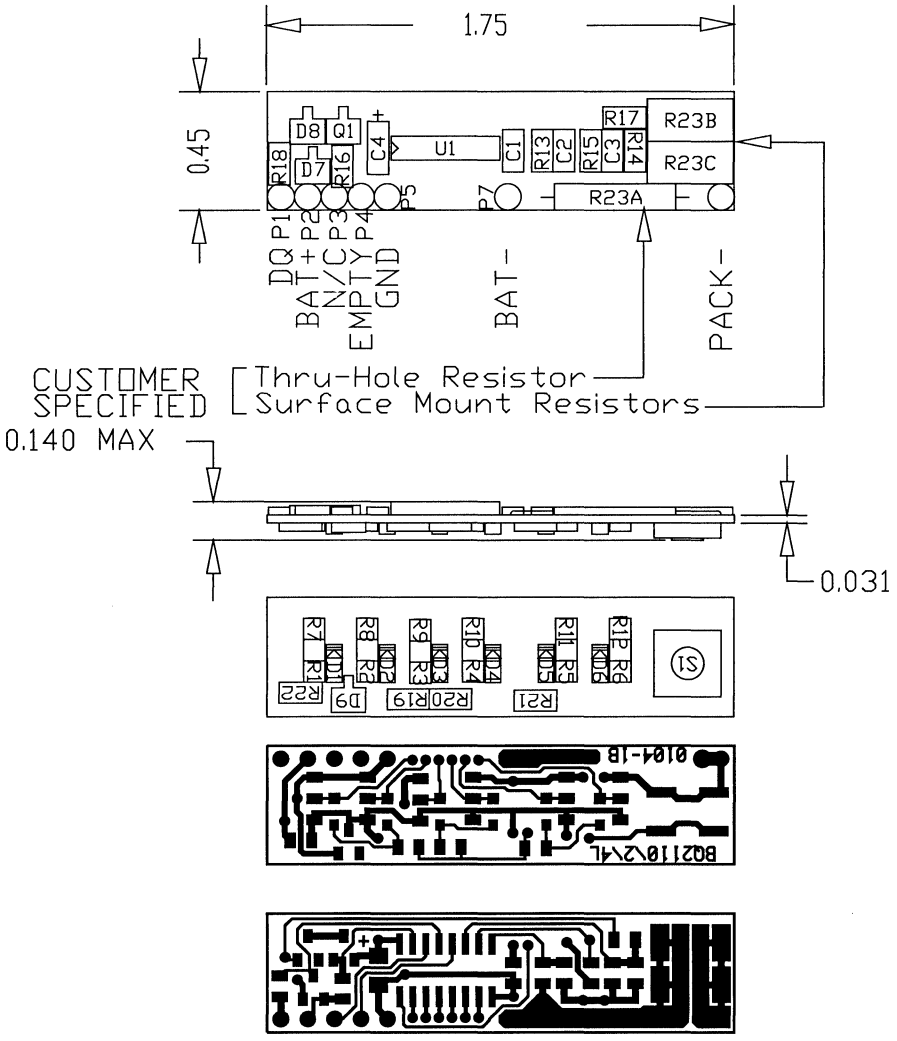
bq2110 Schematic



BD-963

Note: Schematic shows components which may not be placed on the board, depending upon the configuration.

bq2110 Board



Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Conditions
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	bq2010
All other pins	Relative to V_{SS}	-0.3	+7.0	V	bq2010
P_{SR}	Continuous sense resistor power dissipation	-	3	W	Thru-hole sense resistor
		-	1	W	Surface mount sense resistors
I_{CHG}	Continuous charge/ discharge current	-	3.0	A	
T_{OPR}	Operating temperature	0	+70	°C	Commercial
T_{STR}	Storage temperature	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
NumCell	Number of series cells in battery pack	4	-	12	-	
BAT+	Positive terminal of pack	GND	NumCell * 1.2V	NumCell * 1.8V	V	
BAT-	Negative terminal of pack	GND - 0.3	-	GND+2.0	V	
I_{CC}	Supply current at BAT+ terminal (no external loads)	-	200	300	µA	
R_{DQ}	Internal pull-down	500k	-	-	Ω[1]	
I_{OL}	Open-drain sink current DQ, EMPTY	-	-	5.0	mA[1]	
V_{OL}	Open-drain output low, DQ, EMPTY	-	-	0.5	V[1]	I_{OL} < 5mA
V_{IHDQ}	DQ input high	2.5	-	-	V[1]	
V_{ILDQ}	DQ input low	-	-	0.8	V[1]	
V_{OS}	Voltage offset	-	-	150	µV[1]	

Note: 1. Characterized on PCB, IC 100% tested.

DC Voltage Thresholds ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	0.93	0.95	0.97	V	BAT+/NumCell[1]
V_{EDV1}	First empty warning	1.03	1.05	1.07	V	BAT+/NumCell[1]
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	BAT+/NumCell[1]
V_{SRO}	Sense resistor range	-300	-	+2000	mV	$V_{SR} + V_{OS}$[2]
V_{SRQ}	Valid charge	375	-	-	µV	$V_{SR} + V_{OS}$ [2, 3]
V_{SRD}	Valid discharge	-	-	-300	µV	$V_{SR} + V_{OS}$ [2, 3]

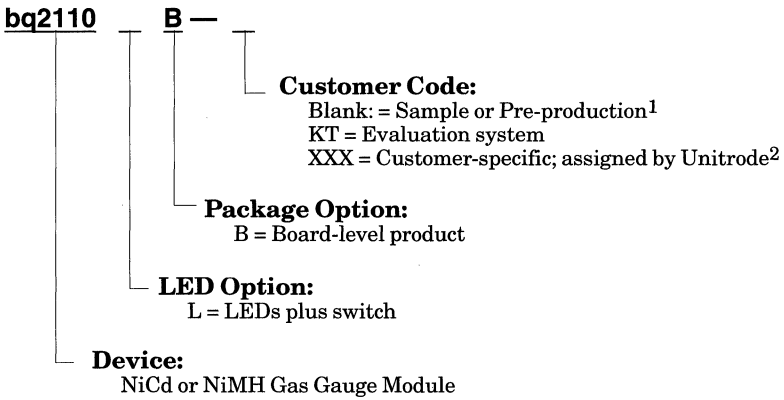
Notes:
1. At SB input of bq2010
2. At SR input of bq2010.
3. Default value; value set in DMF register.

Data Sheet Revision History

Change No.	Page No.	Description
1	2	Updated Table 1 to include 3.0A limit
1	5	Added 3.0A maximum continuous charge/discharge current specification

Note: Change 1 = May 1999 B changes from July 1996.

Ordering Information



Notes:
1. Requires configuration sheet (see Table 1)
2. Example production part number: bq2110LB-001

6/6

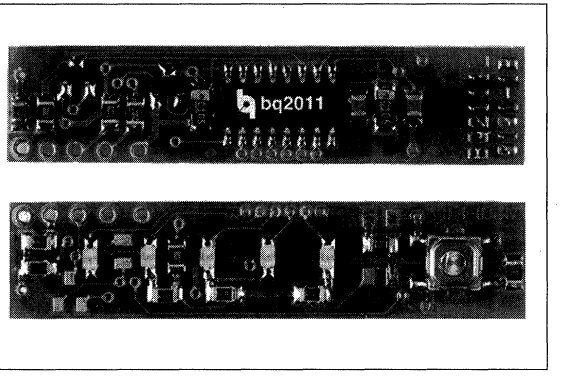
UNITRODE

bq2111L

NiCd Gas Gauge Module with LEDs for High Discharge Rates

Features

- Complete bq2011 Gas Gauge solution for NiCd packs in high discharge rate applications
- Five surface-mounted LEDs to display state-of-charge information
- Battery state-of-charge monitoring for 4- to 12-cell series applications
- On-board regulator allows direct connection to the battery
- Battery information available over a single-wire bidirectional serial port
- Nominal capacity pre-configured
- Compact size for battery pack integration



General Description

The bq2111L Gas Gauge Module provides a complete and compact solution for capacity monitoring of NiCd battery packs in high discharge rate applications such as power tools. Designed for battery pack integration, the bq2111L incorporates a bq2011 Gas Gauge IC, five surface-mounted LEDs, and the other discrete components necessary to monitor and display accurately the capacity of 4 to 12 series cells. The only external component required is a low-value sense resistor connected between GND and PACK-. Contacts are also provided on the bq2111L for direct connection to the battery stack and the serial communications port (DQ). The battery stack should be connected between BAT+ and GND. Please refer to the bq2011 data sheet for the specifics on the operation of the Gas Gauge.

Unitrode configures the bq2111L based on the information requested in Table 1. The configuration defines the number of series cells and the nominal battery pack capacity. The bq211L module uses the absolute LED display to indicate battery capacity. In this mode, the remaining capacity is represented as a percentage of the programmed capacity.

The bq2111L can operate directly from four series cells within the pack using the LBAT+ supply input. For four series cell applications or applications using the on-board regulator, LBAT+ should be connected to BAT+. Please refer to Figure 1 for module connection illustrations.

A module development kit is also available for the bq2111L. The bq2111LB-KT includes one configured module and the following:

1) An interface board that allows connection to the serial port of an AT-compatible computer.
2) Menu-driven software with the bq2111L to display charge/discharge activity and to allow user interface to the bq2011 from any standard DOS PC.
3) Source code for the TSR.

Pin Descriptions

P1	**DQ/Serial communication port**
P2	**BAT+/Battery positive/Pack positive**
P3	**LBAT+/Four--cell power**
P4	**PACK-/Pack negative**
P5	**GND/Ground**

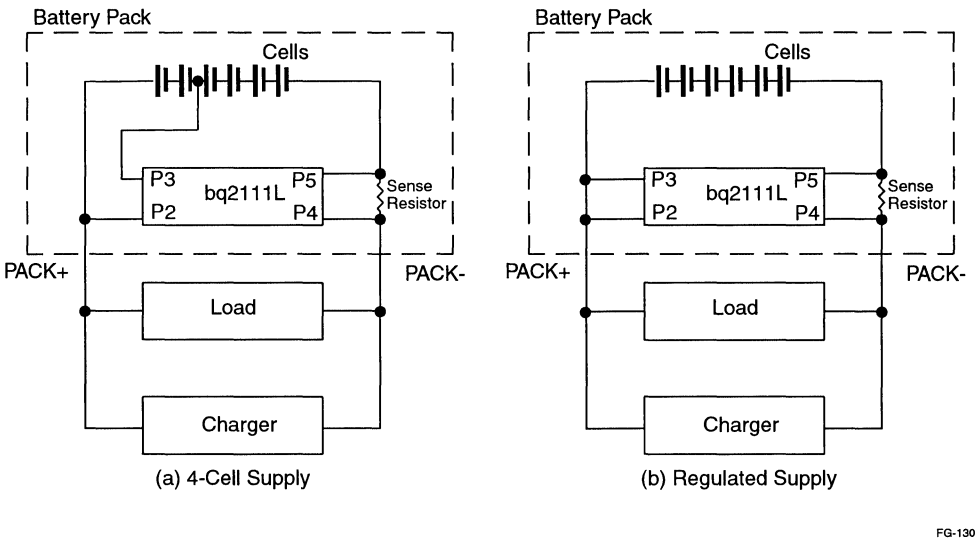


Figure 1. Module Connection Diagram

Table 1. bq2111L Module Configuration

Customer Name: _____

Contact: _____ Phone: _____

Address: _____

_____

Sales Contact: _____ Phone: _____

Number of series battery cells (4–12) _____

Sense resistor size in mΩ[1] _____

Battery pack capacity (mAh) _____

Discharge rate(A) Min._____ Avg._____ Max._____

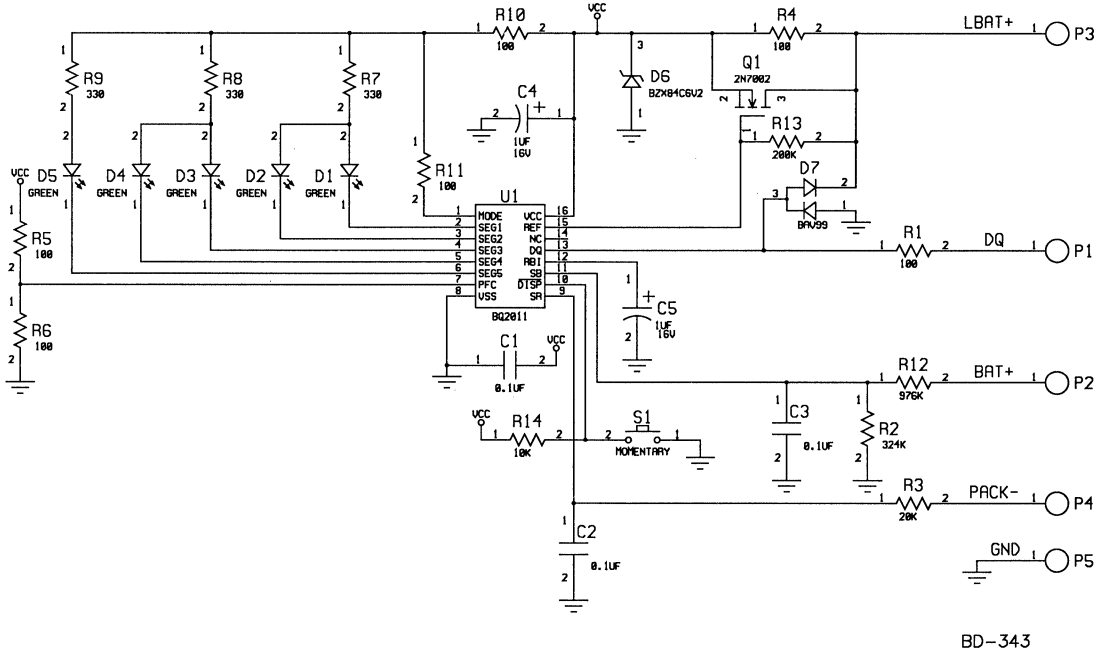
Charge rate (A) _____

FAE approval: _____ Date:_____

Note: 1. Sense resistor is not included with board.

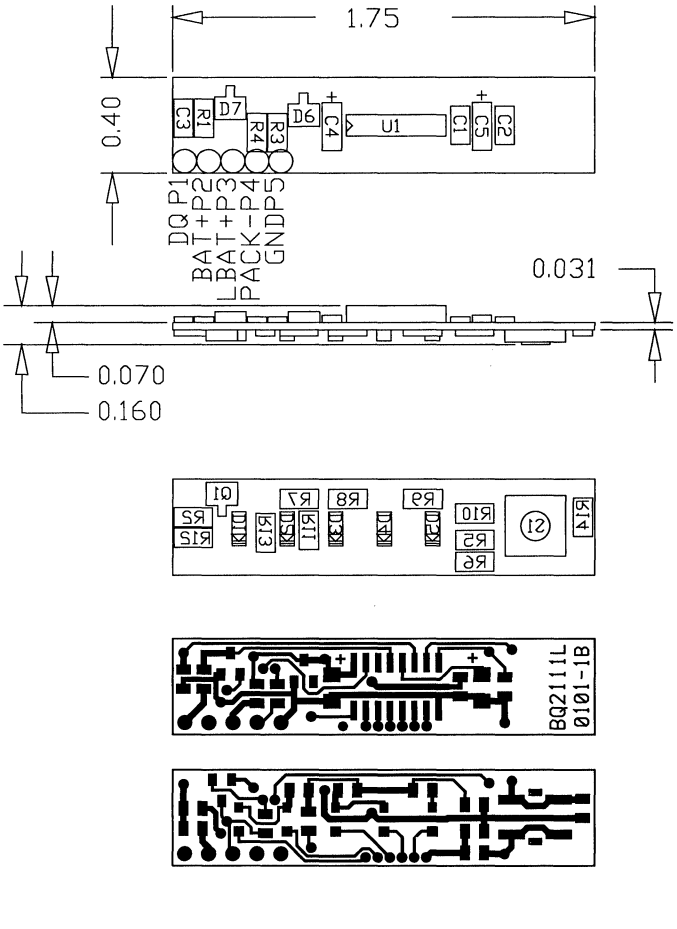
2/6

bq2111L Example Schematic



Note: Schematic shows components which may not be placed on the board, depending upon the configuration.

bq2111L Board



BD-344

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	bq2011
All other pins	Relative to V_{SS}	-0.3	+7.0	V	bq2011
T_{OPR}	Operating temperature	0	+70	°C	Commercial
T_{STR}	Storage temperature	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
NumCell	Number of series cells in battery pack	4	-	12	-	
BAT+	Positive terminal of pack	GND	NumCell * 1.2V	NumCell * 1.8V	V	
V_{SR}	Voltage across the sense resistor, P4 to P5	-0.3	-	2	V	
V_{CC}	Supply voltage (direct cell operation) LBAT+	3.0	4.8	7.2	V	
I_{CC}	Supply current at BAT+ terminal (no external loads)	-	120	250	µA	
R_{DQ}	Internal pull-down	500k	-	-	Ω[1]	
I_{OL}	Open-drain sink current DQ	-	-	5.0	mA[1]	
V_{OL}	Open-drain output low, DQ	-	-	0.5	V[1]	I_{OL} < 5mA
V_{IHDQ}	DQ input high	2.5	-	-	V[1]	
V_{ILDQ}	DQ input low	-	-	0.8	V[1]	
V_{OS}	Voltage offset			150	µV[1]	

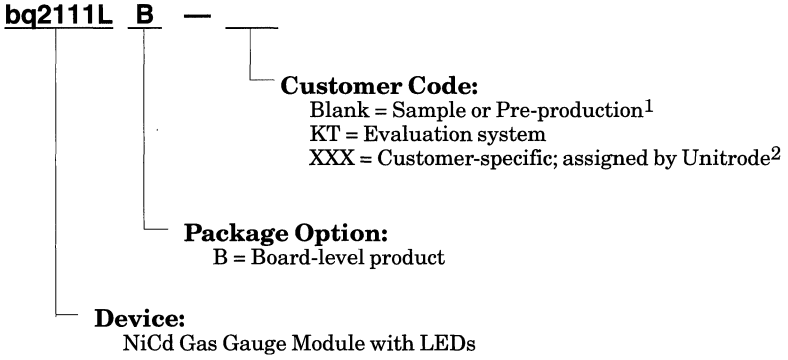
Note: 1. Characterized on PCB, IC 100% tested.

DC Voltage Thresholds ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDV}	Final empty warning	0.87	0.90	0.93	V	BAT+/NumCell[1]
V_{MCV}	Maximum single-cell voltage	1.95	2.0	2.05	V	BAT+/NumCell[1]
V_{SR1}	Discharge compensation threshold	20	50	75	mV	$V_{SR} + V_{OS}$[2]
V_{SR2}	Discharge compensation threshold	70	100	125	mV	$V_{SR} + V_{OS}$[2]
V_{SR3}	Discharge compensation threshold	120	150	175	mV	$V_{SR} + V_{OS}$[2]
V_{SR4}	Discharge compensation threshold	220	253	275	mV	$V_{SR} + V_{OS}$[2]
V_{SRO}	Sense resistor sense range	-300	-	+2000	mV	$V_{SR} + V_{OS}$[2]
V_{SRQ}	Valid charge	-	-	-400	µV	$V_{SR} + V_{OS}$[2]
V_{SRD}	Valid discharge	500	-	-	µV	$V_{SR} + V_{OS}$[2]

Notes: 1. At SB input of bq2011
2. At SR input of bq2011

Ordering Information



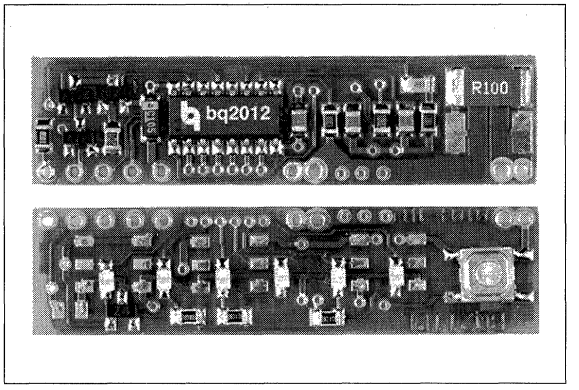
Notes: 1. Requires configuration sheet (see Table 1)
2. Example production part number: bq2111LB-001

6/6

NiCd or NiMH Gas Gauge Module with Slow-Charge Control

Features

- Complete bq2012 Gas Gauge solution for NiCd or NiMH battery packs
- Output for slow-charge control of battery pack
- Battery information available over a single-wire bidirectional serial port
- Battery state-of-charge monitoring for 4- to 12-cell series applications
- On-board regulator allows direct connection to the battery
- "L" version includes push-button activated LEDs to display state-of-charge information
- Nominal capacity and cell chemistry pre-configured
- Compact size for battery pack integration



General Description

The bq2112 Gas Gauge Module provides a complete and compact solution for capacity monitoring of NiCd and NiMH battery packs. Designed for battery pack integration, the bq2112 incorporates a bq2012 Gas Gauge IC, a current sense resistor, and all other components necessary to accurately monitor and display the capacity of 3 to 12 series cells. The bq2112L includes six surface-mounted LEDs to display remaining capacity in 20% increments of the learned capacity (relative mode) or programmed capacity (absolute mode). The sixth LED is used in absolute mode to represent an overfull condition (charge above the programmed capacity). The LEDs are activated with the onboard push--button switch.

Contacts are provided on the bq2112 for direct connection to the battery stack (BAT+, BAT-), the serial communications port (DQ), the empty indicator (EMPTY), and the charge control output ($\overline{\text{CHG}}$). Please refer to the bq2012 data sheet for the specifics on the operation of the Gas Gauge.

Unitrode configures the bq2112 based on the information requested in Table 1. The configuration defines the number of series cells, the nominal battery pack capacity, the self-discharge rate, and the LED display mode.

A module development kit is also available for the bq2112. The bq2112B-KT or bq2112LB-KT includes one configured module and the following:

1) An interface board that allows connection to the serial port of an AT-compatible computer.
2) Menu-driven software with the bq2112 to display charge/discharge activity and to allow user interface to the bq2012 from any standard DOS PC.
3) Source code for the TSR.

Pin Descriptions

P1	**DQ/Serial communication port**
P2	**BAT+/Battery positive/pack positive**
P3	**$\overline{\text{CHG}}$/Charge control output**
P4	**EMPTY/Empty indicator output**
P5	**GND/Ground**
P6	**PACK-/Pack negative**
P7	**BAT-/Battery negative**

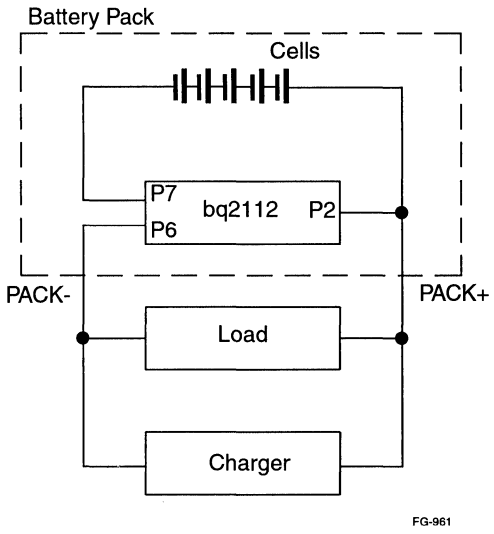


Figure 1. Module Connection Diagram

Table 1. bq2112 Module Configuration

Customer Name: _____

Contact: _____ Phone: _____

Address: _____

_____

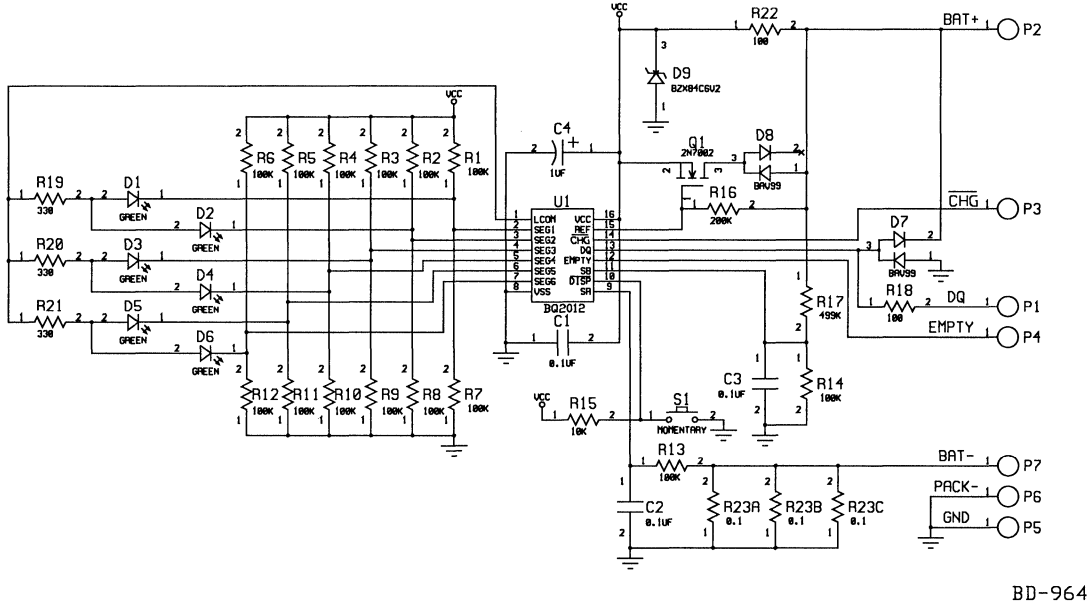
Sales Contact: _____ Phone: _____

Number of series battery cells (4-12)	_____
Battery type (NiCd or NiMH)	_____
Battery pack capacity (mAh)	_____
Discharge rate into load (3.0A max.)	Min._____ Avg._____ Max._____
Charge rate (3.0A max)	_____
Display mode (absolute or relative)	_____
LEDs and switch (Y/N)	_____

FAE approval: _____ Date: _____

2/6

bq2112 Schematic

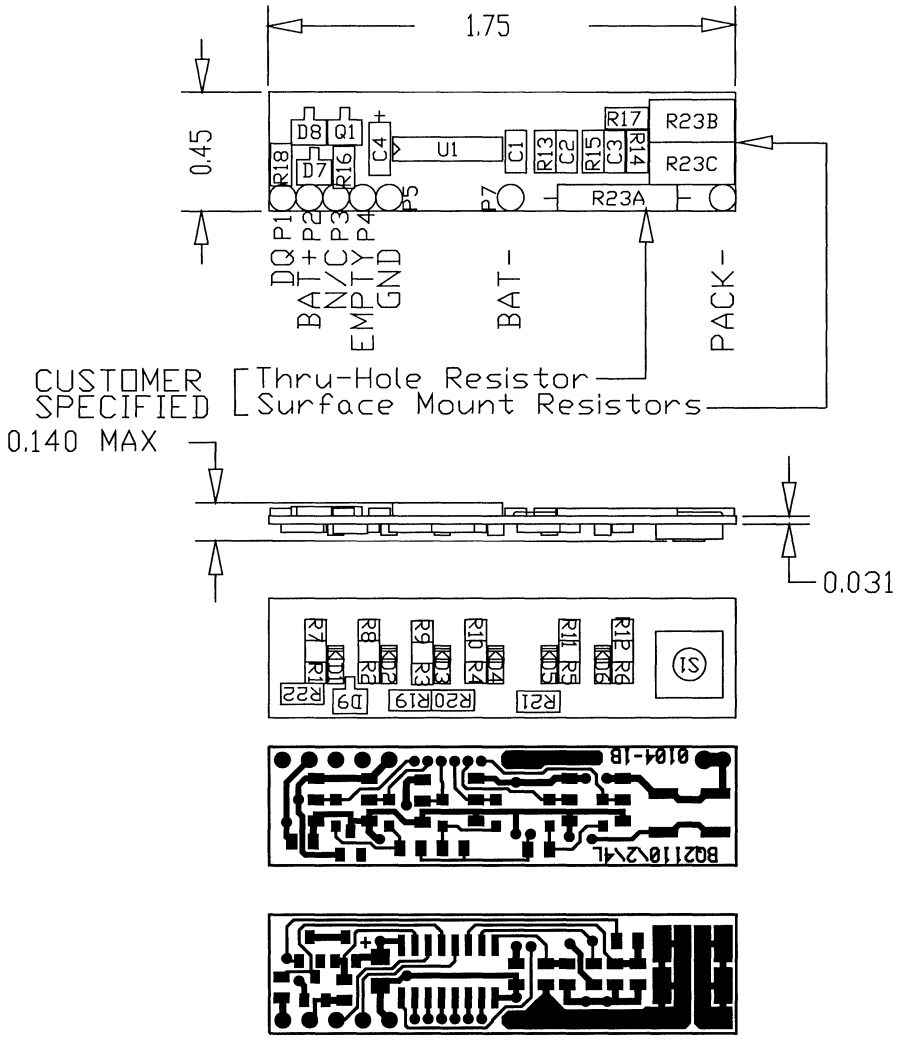


BD-964

Note: Schematic shows components which may not be placed on the board, depending upon the configuration.

3/6

bq2112 Board



4/6

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Conditions
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	bq2012
All other pins	Relative to V_{SS}	-0.3	+7.0	V	bq2012
P_{SR}	Continuous sense resistor power dissipation	-	3	W	Thru-hole sense resistor
		-	1	W	Surface mount sense resistor
I_{CHG}	Continuous charge/ discharge current	-	3.0	A	
T_{OPR}	Operating temperature	0	+70	°C	Commercial
T_{STR}	Storage temperature	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
NumCell	Number of series cells in battery pack	4	-	12	-	
BAT+	Positive terminal of pack	GND	NumCell * 1.2V	NumCell * 1.8V	V	
BAT-	Negative terminal of pack	GND - 0.3	-	GND+2.0	V	
I_{CC}	Supply current at BAT+ terminal (no external loads)	-	200	300	µA	
R_{DQ}	Internal pull-down	500k	-	-	Ω[1]	
I_{OL}	Open-drain sink current DQ, EMPTY, CHG	-	-	5.0	mA[1]	
V_{OL}	Open-drain output low, DQ, EMPTY, CHG	-	-	0.5	V[1]	I_{OL} < 5mA
V_{IHDQ}	DQ input high	2.5	-	-	V[1]	
V_{ILDQ}	DQ input low	-	-	0.8	V[1]	
V_{OS}	Voltage offset	-	-	150	µV[1]	

Note: 1. Characterized on PCB, IC 100% tested.

DC Voltage Thresholds ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	0.93	0.95	0.97	V	BAT+/NumCell[1]
V_{EDV1}	First empty warning	1.03	1.05	1.07	V	BAT+/NumCell[1]
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	BAT+/NumCell[1]
V_{SRO}	Sense resistor range	-300	-	+2000	mV	$V_{SR} + V_{OS}$[2]
V_{SRQ}	Valid charge	375	-	-	µV	$V_{SR} + V_{OS}$ [2, 3]
V_{SRD}	Valid discharge	-	-	-300	µV	$V_{SR} + V_{OS}$ [2, 3]

Notes:
1. At SB input of bq2012.
2. At SR input of bq2012.
3. Default value; value set in DMF register.

5

Data Sheet Revision History

Change No.	Page No.	Description
1	2	Updated Table 1 to include 3.0A limit
1	5	Added 3.0A maximum continuous charge/discharge current specification

Note: Change 1 = May 1999 B changes from Nov. 1997.

Ordering Information

bq2112 _ B — ___

Customer Code:
Blank = Sample or Pre-production[1]
KT = Evaluation system
XXX = Customer specific; assigned by Unitrode[2]

Package Option:
B = Board-level product

LED Option:
L = LEDs plus switch
Blank = No LEDs or switch

Device:
NiCd or NiMH Gas Gauge Module with Slow-Charge Control

Notes:
1. Requires configuration sheet (see Table 1)
2. Example production part number: bq2112LB-002

6/6

Gas Gauge Module for Power-Assist Applications

Features

- Complete bq2013H Gas Gauge solution for nickel or lead acid battery packs
- Battery information available over a single-wire bidirectional serial port
- Battery state-of-charge monitoring for up to 14 nickel or 12 lead acid series applications
- On-board regulator allows direct connection to the battery
- "L" version includes push-button activated LEDs to display state-of-charge information
- Nominal capacity pre-configured
- Compact size for battery pack integration

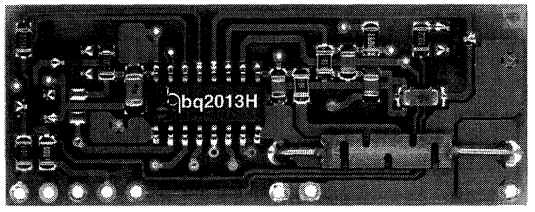
General Description

The bq2113H Gas Gauge Module provides a complete and compact solution for capacity monitoring of nickel or lead acid battery packs. Designed for battery pack integration, the bq2113H incorporates a bq2013H Gas Gauge IC, a current sense resistor, and all other components necessary to accurately monitor and display the capacity of up to 14 nickel or 12 lead acid cells.

The bq2113HL includes five LEDs to display remaining capacity in 20% increments of the learned capacity. The LEDs are activated with the onboard push-button switch.

Contacts are provided on the bq2113H for direct connection to the battery stack (BAT+, BAT-) and the serial communications port (HDQ). The RBI input provides backup power to the bq2013H in the event that the cells are removed or the battery is turned off. The bq2113H has a 1µF capacitor onboard connected to RBI to supply backup power for about an hour. The RBI input can be wired to a single cell to provide prolonged data retention times. The ACC input provides an option to enable the LED display with an external (active low) signal such as from a microcontroller. Please refer to the bq2013H data sheet for the specifics on the operation of the Gas Gauge.

Unitrode configures the bq2113H based on the information requested in Table 1. The configuration defines the number of series cells, the nominal battery pack capacity, and the battery chemistry. Figure 1 shows how the module connects to the cells.



A module development kit is also available for the bq2113H. The bq2113HB-KT or the bq2113HLB-KT includes one configured module and the following:

1) An EV2200-13H interface board that allows connection to the serial port of an AT-compatible computer.
2) Menu-driven software to display charge/discharge activity and to allow user interface to the bq2050 from any standard Windows 3.1x or 95 PC.

Pin Descriptions

P1	**HDQ/Serial Communications port**
P2	**DONE/Done input**
P3	**BAT+/Battery positive/pack positive**
P4	**ACC/Display activation**
P5	**RBI/Register backup input**
P6	**GND/Ground**
P7	**PACK-/Pack negative**
P8	**BAT-/Battery negative**

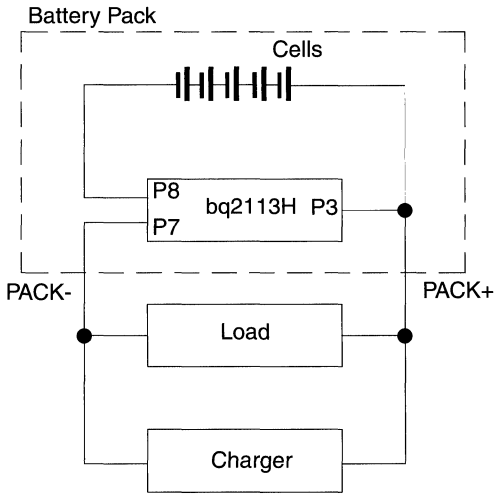


Figure 1. Module Connection Diagram

Table 1. bq2113H Module Configuration

Customer Name: _____

Contact: _____ Phone: _____

Address: _____

_____

Sales Contact: _____ Phone: _____

Number of series battery cells	_____
Battery chemistry	_____
Battery pack capacity (mAh)	_____
Discharge rate into load (A)	min. _____ avg. _____ max. _____
Charge rate (A)	_____
Self-discharge compensation (Y/N)	_____
LEDs and switch (Y/N)	_____
Display Mode(relative or absolute)	_____

FAE Approval: _____ Date: _____

2/4

bq2113H Schematic

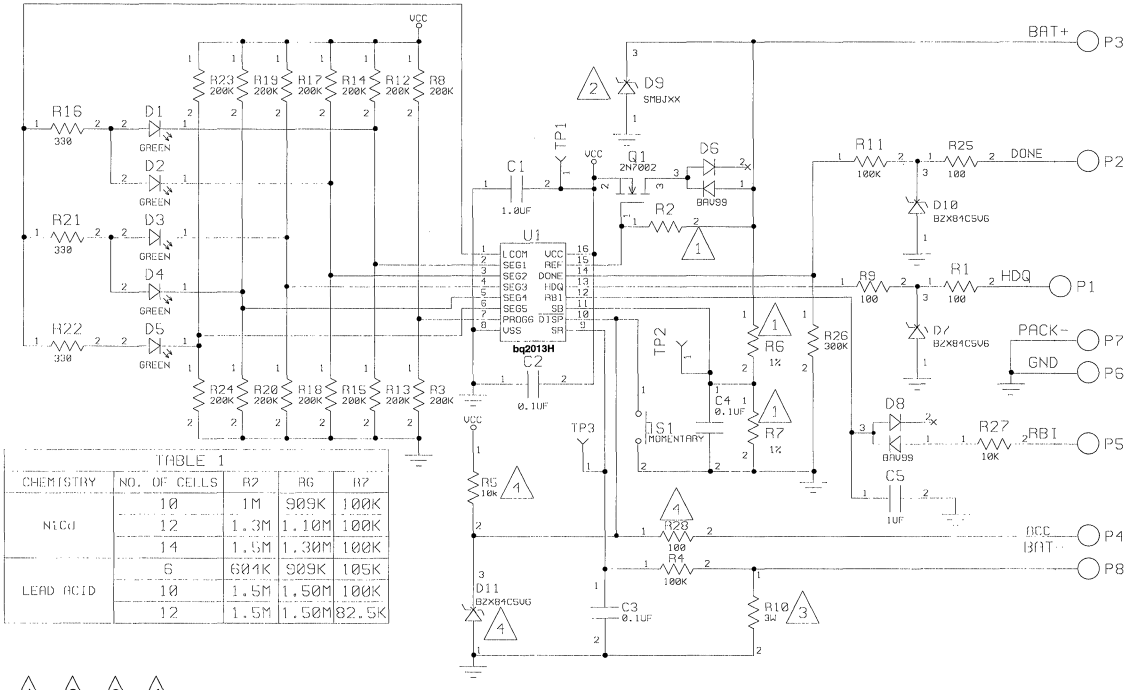


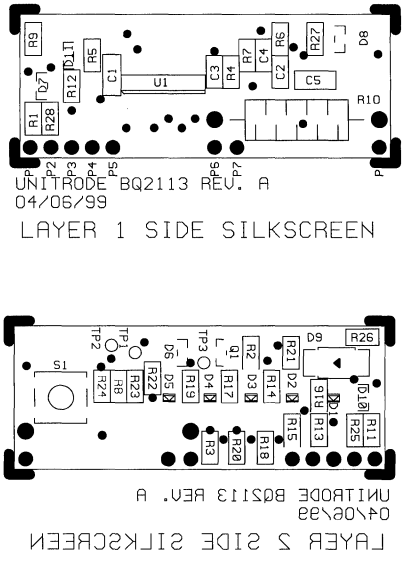
TABLE 1

CHEMISTRY	NO. OF CELLS	R2	R6	R7
NiCd	10	1M	909K	100K
	12	1.3M	1.10M	100K
	14	1.5M	1.30M	100K
LEAD ACID	6	601K	909K	105K
	10	1.5M	1.50M	100K
	12	1.5M	1.50M	82.5K

1 2 3 4 Component values depend on user-provided information in Table 1.

bq2113-a.eps

bq2113H Board



Ordering Information

bq2113H **B** —

Customer Code:
Blank = Sample or Pre-production[1]
KT = Evaluation system
XXX = Customer specific; assigned by Unitrode[2]

Package Option:
B = Board-level product

LED Option:
L = LEDs plus switch
Blank = No LEDs or switch

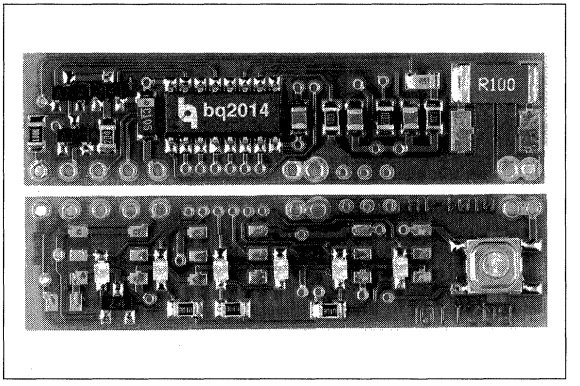
Device:
Gas Gauge Module for Power-Assist Applications

Notes:
1. Requires configuration sheet (see Table 1)
2. Example production part number: bq2113HLB-002

NiCd or NiMH Gas Gauge Module with Charge-Control Output

Features

- Complete bq2014 Gas Gauge solution for NiCd or NiMH battery packs
- Charge-control output allows communication to external charge controller (bq2004)
- Battery information available over a single-wire bidirectional serial port
- Battery state-of-charge monitoring for 4- to 12-cell series applications
- On-board regulator allows direct connection to the battery
- "L" version includes push-button activated LEDs to display state-of-charge information
- Nominal capacity and cell chemistry pre-configured
- Compact size for battery pack integration



General Description

The bq2114 Gas Gauge Module provides a complete and compact solution for capacity monitoring of NiCd and NiMH battery packs. Designed for battery pack integration, the bq2114 incorporates a bq2014 Gas Gauge IC, a current sense resistor, and all other components necessary to accurately monitor and display the capacity of 4 to 12 series cells. The bq2114L includes five surface-mounted LEDs to display remaining capacity in 20% increments of the learned capacity (relative mode). The LEDs are activated with the onboard push-button switch.

Contacts are provided on the bq2114 for direct connection to the battery stack (BAT+, BAT-), the serial communications port (DQ), the empty indicator (EMPTY), and the charge control output (CHG). Please refer to the bq2014 data sheet for the specifics on the operation of the Gas Gauge.

Unitrode configures the bq2114 based on the information requested in Table 1. The configuration defines the number of series cells, the nominal battery pack capacity, and the self-discharge rate.

A module development kit is also available for the bq2114. The bq2114B-KT or bq2114LB-KT includes one configured module and the following:

1) An interface board that allows connection to the serial port of an AT-compatible computer.
2) Menu-driven software with the bq2114 to display charge/discharge activity and to allow user interface to the bq2014 from any standard DOS PC.
3) Source code for the TSR.

Pin Descriptions

P1	**DQ/Serial communication port**
P2	**BAT+/Battery positive/pack positive**
P3	**CHG/Charge control output**
P4	**EMPTY/Empty indicator output**
P5	**GND/Ground**
P6	**PACK-/Pack negative**
P7	**BAT-/Battery negative**

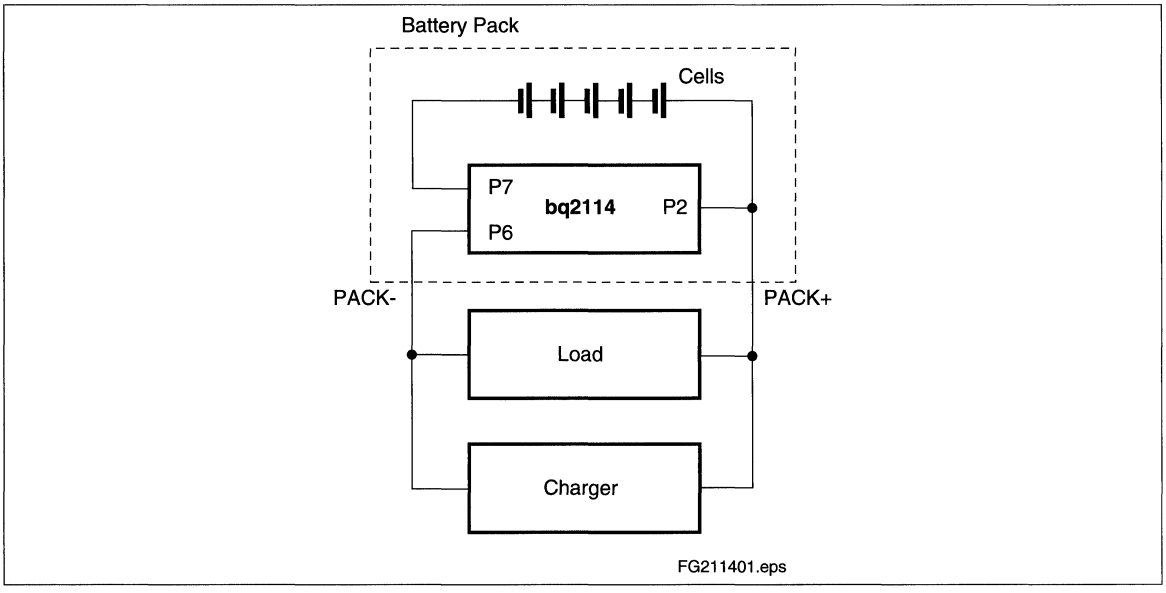


Figure 1. Module Connection Diagram

Table 1. bq2114 Module Configuration

Customer Name: _____

Contact: _____ Phone: _____

Address: _____

_____

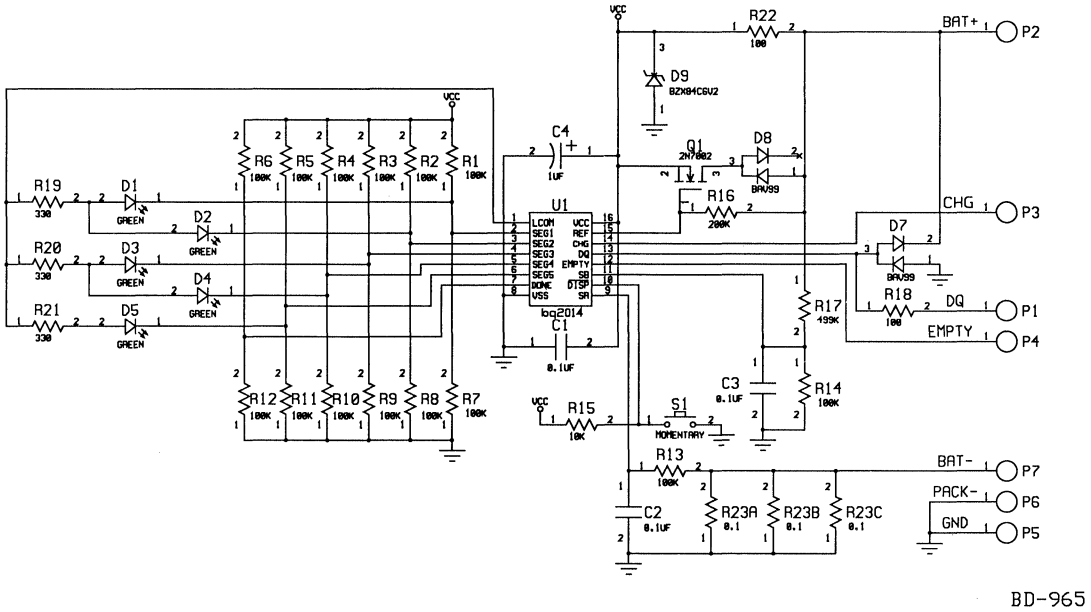
Sales Contact: _____ Phone: _____

Number of series battery cells (4–12)	_____		
Battery type (NiCd or NiMH)	_____		
Battery pack capacity (mAh)	_____		
Discharge rate into load (3.0A max.)	Min._____	Avg._____	Max._____
Charge rate (3.0A max.)	_____		
LEDs and switch (Y/N)	_____		

FAE approval: _____ Date:_____

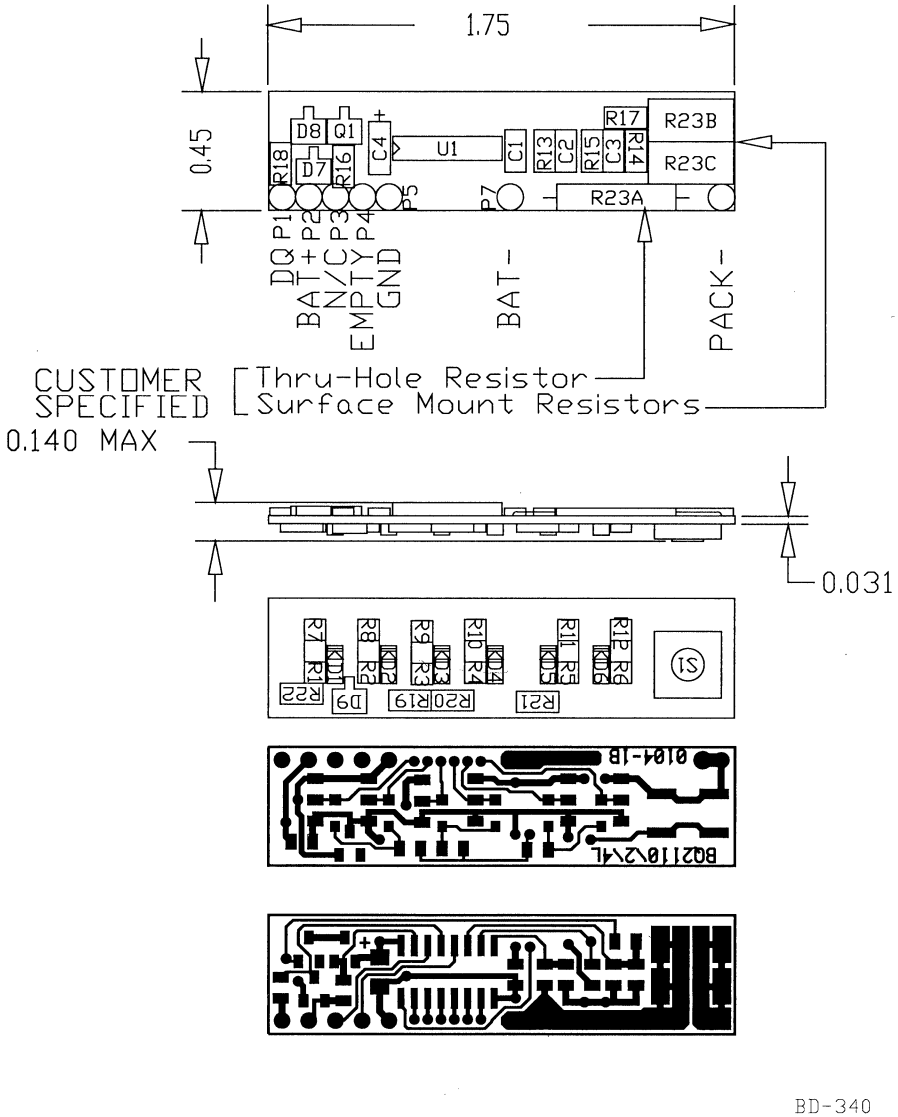
2/6

bq2114 Schematic



Note: Schematic shows components which may not be placed on the board, depending upon the configuration.

bq2114 Board



Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Conditions
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	bq2014
All other pins	Relative to V_{SS}	-0.3	+7.0	V	bq2014
P_{SR}	Continuous sense resistor power dissipation	-	3	W	Thru-hole sense resistor
		-	1	W	Surface-mount sense resistor
I_{CHG}	Continuous charge/ discharge current	-	3.0	A	
T_{OPR}	Operating temperature	0	+70	°C	Commercial
T_{STR}	Storage Temperature	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
NumCell	Number of series cells in battery pack	4	-	12	-	
BAT+	Positive terminal of pack	GND	NumCell * 1.2V	NumCell * 1.8V	V	
BAT-	Negative terminal of pack	GND - 0.3	-	GND+2.0	V	
I_{CC}	Supply current at BAT+ terminal (no external loads)	-	200	300	µA	
R_{DQ}	Internal pull-down	500k	-	-	Ω[1]	
I_{OL}	Open-drain sink current DQ, EMPTY, CHG	-	-	5.0	mA[1]	
V_{OL}	Open-drain output low, DQ, EMPTY, CHG	-	-	0.5	V[1]	I_{OL} < 5mA
V_{IHDQ}	DQ input high	2.5	-	-	V[1]	
V_{ILDQ}	DQ input low	-	-	0.8	V[1]	
V_{OS}	Voltage offset	-	-	150	µV[1]	

Note: 1. Characterized on PCB, IC 100% tested.

DC Voltage Thresholds ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	0.93	0.95	0.97	V	BAT+/NumCell[1]
V_{EDV1}	First empty warning	1.03	1.05	1.07	V	BAT+/NumCell[1]
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	BAT+/NumCell[1]
V_{SRO}	Sense resistor range	-300	-	+2000	mV	$V_{SR} + V_{OS}$[2]
V_{SRQ}	Valid charge	375	-	-	µV	$V_{SR} + V_{OS}$ [2, 3]
V_{SRD}	Valid discharge	-	-	-300	µV	$V_{SR} + V_{OS}$ [2, 3]

Notes:
1. At SB input of bq2014.
2. At SR input of bq2014.
3. Default value; value set in DMF register.

Data Sheet Revision History

Change No.	Page No.	Description
1	2	Updated Table 1 to include 3.0A limit
1	5	Added 3.0A maximum continuous charge/discharge current specification

Note: Change 1 = May 1999 B changes from Sept. 1996.

Ordering Information

bq2114 B –

Customer Code:
Blank = Sample or Pre-production[1]
KT = Evaluation system
XXX = Customer-specific; assigned by Unitrode[2]

Package Option:
B = Board-level product

LED Option:
L = LEDs plus switch
Blank = No LEDs or switch

Device:
NiCd or NiMH Gas Gauge Module with Charge-Control Output

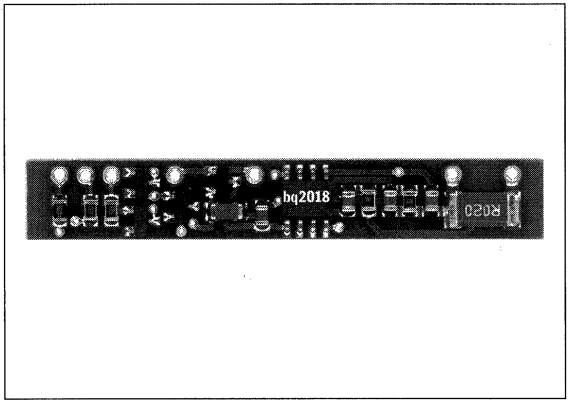
Notes:
1. Requires configuration sheet (see Table 1)
2. Example production part number: bq2114LB-003

6/6

Power Minder™ Mini-Board

Features

- Complete and compact charge/discharge counter
- Combines the bq2018, voltage regulator, sense resistor, and backup capacitor on a single PCB
- Communicates charge/discharge information to a host with a single-wire interface
- Designed for battery pack integration
  - Less than 0.5 square inches
  - Small size allows it to fit in the crevice formed by two adjacent cells
  - Low operating current
- Direct connections for the pack cells and communications port



General Description

The bq2118 Power Minder mini-board provides a complete and compact solution for charge and discharge counting of all types of battery chemistries, including NiCd, NiMH, or Li-Ion batteries. Designed for battery pack integration, the bq2118 incorporates a bq2018 Power Minder IC, supply voltage regulator, sense resistor, and backup capacitor on a small circuit board. The module provides direct connections for the positive and negative terminals of the series cells in the battery pack, and can fit in the crevice formed by two adjacent cells. The bq2118 allows a battery pack to be equipped easily with accurate charge/discharge counting electronics.

Unitrode configures the bq2118 based on the information requested in Table 1. The configuration defines the battery chemistry, the number of series cells, and the charge/discharge current. Figure 1 shows how the module connects to the cells.

A module development kit is also available for the bq2118. The bq2118B-KT includes one configured module and the following:

1. An EV2200-18 interface board that allows connection to the serial port of an AT-compatible computer.
2. Menu-driven software to display charge/discharge activity and to allow user interface to the bq2118 from any standard Windows 3.1 or 95 PC.

Pin Descriptions

BAT+	**Battery positive/pack positive**
BAT-	**Battery negative**
HDQ	**Communications port**
PACK-	**Pack negative**
WAKE	**Wakeup output**
RBI	**Register backup input**
V_{CC}	**bq2018 supply voltage**

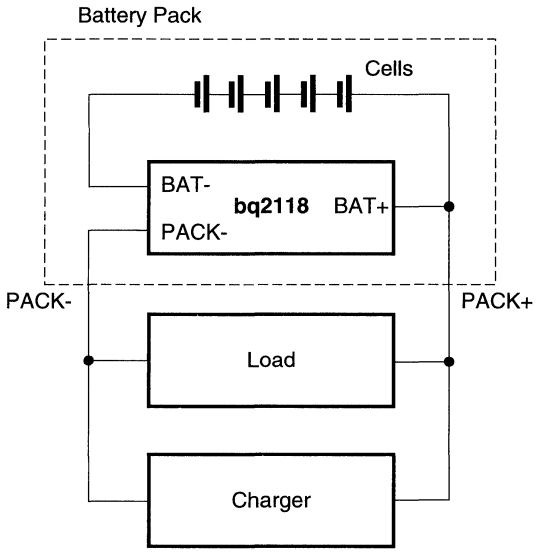


Figure 1. Module Connection Diagram

Table 1. bq2118 Module Configuration

Customer Name: _____

Contact: _____ Phone: _____

Address: _____

_____

Sales Contact: _____ Phone: _____

Number of series battery cells _____

Coke or graphite cell anode _____

Battery pack capacity (mAh) _____

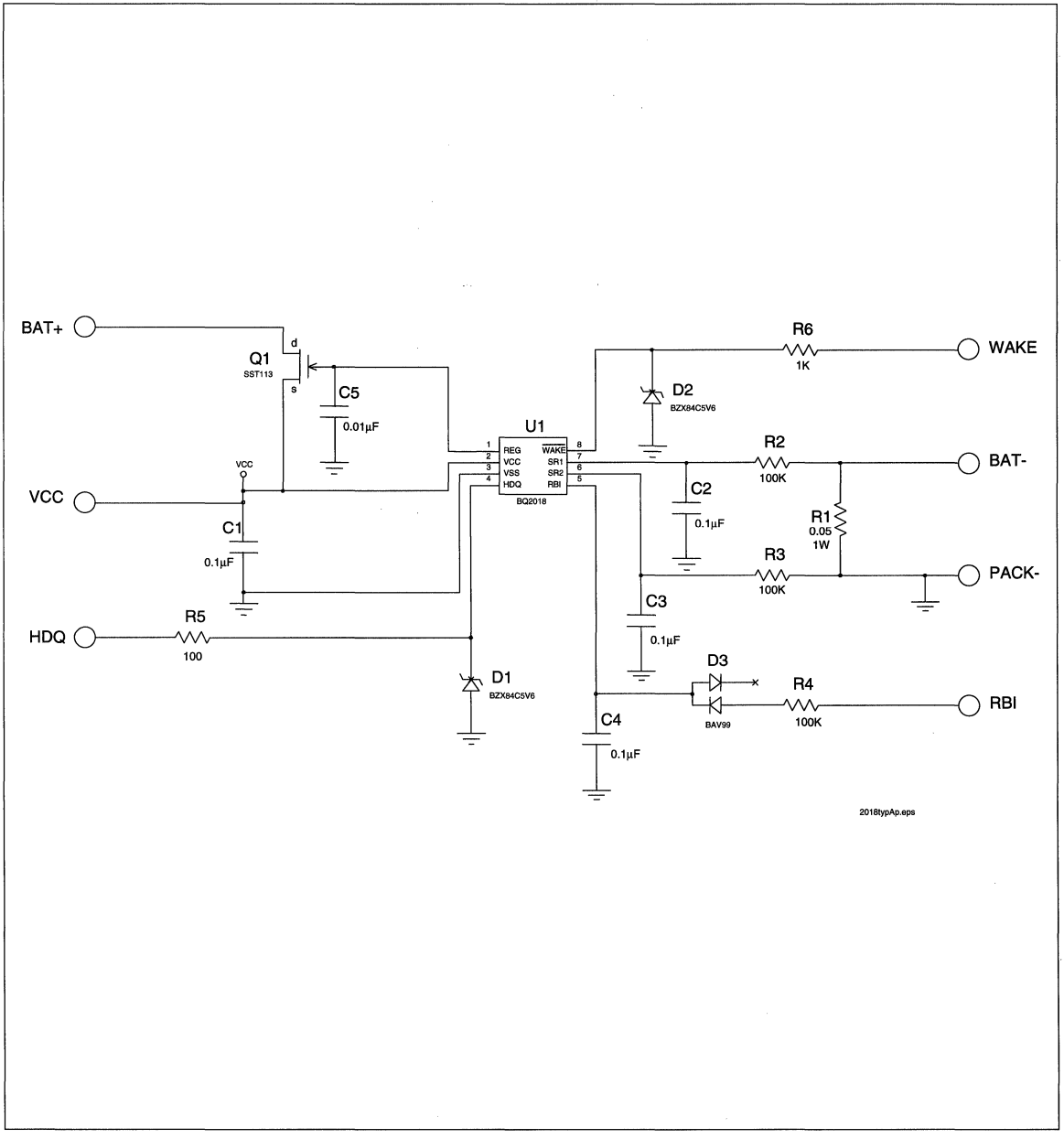
Discharge rate into load (4.0A max) Min. _____ Avg. _____ Max. _____

Charge rate (4.0A max) _____

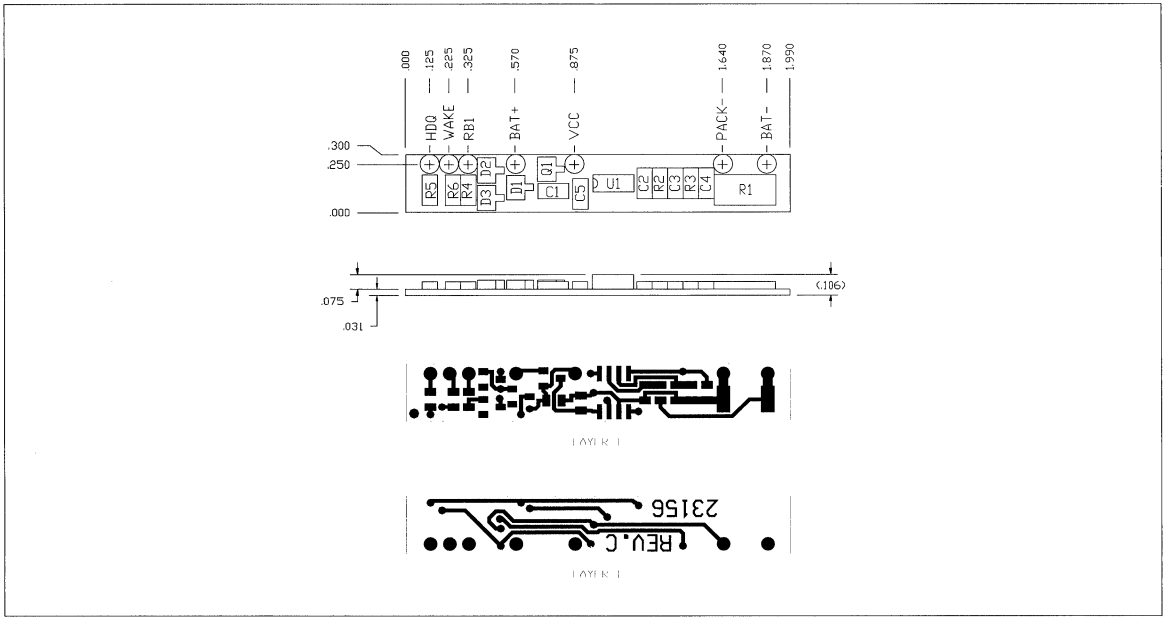
FAE Approval: _____ Date: _____

2/4

bq2118 Schematic



bq2118 Board



Ordering Information

bq2118 B – XXX

Customer Code:
Blank = Sample or Pre-production[1]
KT = Evaluation system
XXX = Customer-specific; assigned by Unitrode[2]

Package Option:
B = Board-level product

Device:
Power Minder Mini-Board

Notes:
1. Requires configuration sheet (see Table 1)
2. Example production part number: bq2118B-001

4/4

Smart Battery Module with LEDs

Features

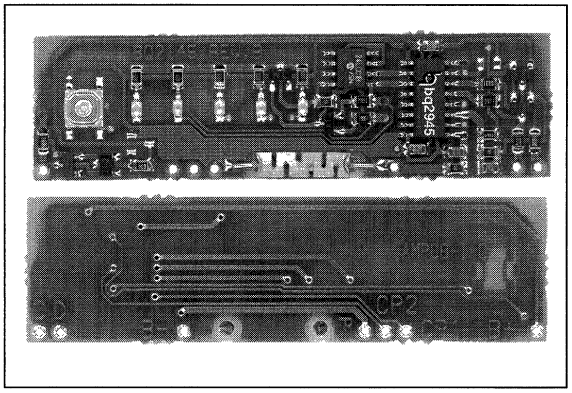
- Complete smart battery solution for NiCd, NiMH, and Li-Ion battery packs
- Based on the bq2945 Gas Gauge IC
- Accurate measurement of available battery capacity
- Designed for battery pack integration:
  - Measures only 2.5 (L) x 0.7 (W) inches
  - Includes Gas Gauge IC, configuration EEPROM, and sense resistor
  - Five onboard state-of-charge LEDs with push-button activation
  - Low operating current for minimal battery drain
- Critical battery information available over two-wire serial port

General Description

The bq2145 Smart Battery Module provides a complete solution for the design of intelligent battery packs. The bq2145 uses the SMBus protocol and supports Smart Battery Data commands in the SMB/SBD specifications. Designed for battery pack integration, the bq2145 combines the bq2945 Gas Gauge IC with a serial EEPROM on a small printed circuit board. The board includes all the necessary components to accurately monitor battery capacity and communicate critical battery parameters to the host system or battery charger. The bq2145 also includes five LEDs. The push-button switch activates the LEDs to show remaining battery capacity in 20% increments.

Contacts are provided on the bq2145 for direct connection to the battery stack (B+, B-) and the two-wire interface (C, D). Please refer to the bq2945 data sheet for specific information on the operation of the Gas Gauge and communication interface.

Unitrode configures the bq2145 based on the information requested in Table 1. The configuration defines the pack voltage, capacity, and chemistry and charge control parameters. The Smart Battery Module uses the onboard sense resistor to track charge and discharge activity of the battery pack. Figure 1 shows how the module connects to the cells.



A module development kit is also available for the bq2145. The bq2145B-KT or the bq2145LB-KT includes one configured module and the following:

1) An EV2200-45 interface board that allows connection to the serial port of any AT-compatible computer.

2) Menu-driven software to display charge/discharge activity and to allow user interface to the Gas Gauge IC and serial E^2PROM from any standard Windows 95 or 3.1x PC.

Pin Descriptions

B+	**BAT+/Battery positive/Pack positive**
P-	**PACK-/Pack negative**
C	**SMBC/Communications clock**
D	**SMBD/Serial data**
B-	**BAT-/Battery negative**
CP2	**Control pin 2**
CP1	**Control pin 1**

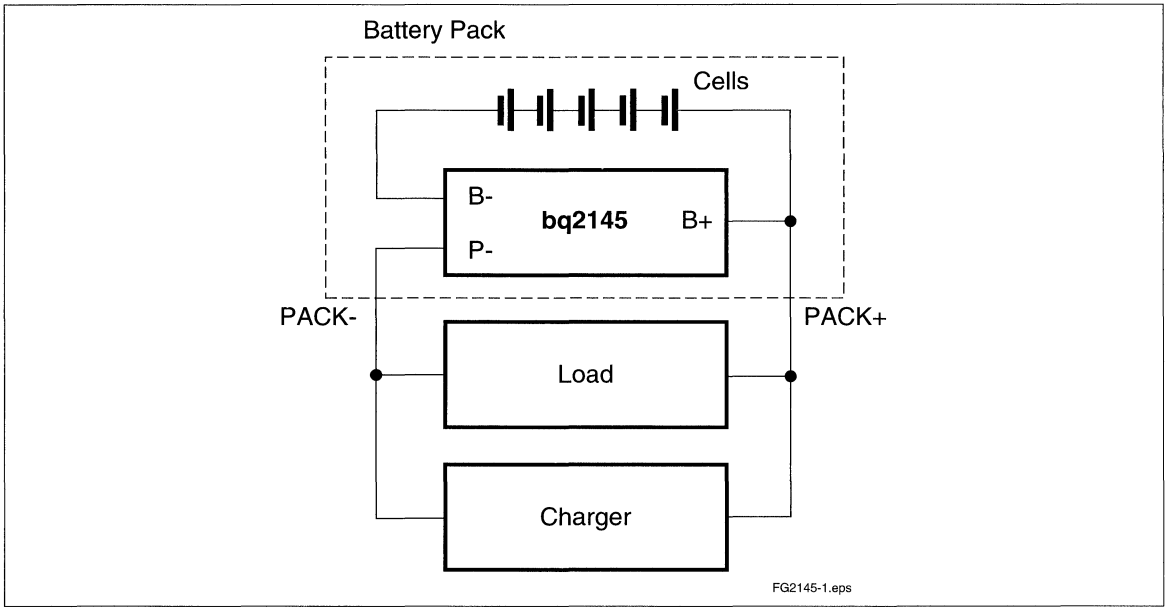


Figure 1. Module Connection Diagram

Table 1. bq2145 Module Configuration

Customer Name: _____

Contact: _____ Phone: _____

Address: _____

Sales Contact: _____ Phone: _____

Board Configuration

LEDs and switch	_____	Yes or No		
Display mode	_____	Relative or Absolute		
Discharge rate (3.0A max.)	Min _____	Avg _____	Max _____	
Duration at max. discharge	_____			
Number of series cells	_____			

EEPROM Configuration			Typical Values NiMH	Typical Values Li-Ion
Remaining time alarm (min)	_____	Sets the low time alarm level	10 min	10 min
Remaining capacity alarm (mAh)	_____	Sets the low capacity alarm level	C/10	C/10
Charging voltage (mV)	_____	Sets the requested charging voltage	65535	4.1V/cell
Design cpaacity (mAh)	_____	Defines the battery pack capacity	3000	3600
Design voltage (mV)	_____	Defines the battery pack voltage	12000	10800
Manufacturer date	_____	Battery pack manufacturer date	mm/dd/yy	mm/dd/yy
Serial number	_____	Battery pack serial number	0-65535	0-65535
Fast-charging current (mA)	_____	Sets the requested charging current	1C	1C
Maintenance charging current (mA)	_____	Sets the requested maintenance charging current	C/20	0
Li-Ion taper current (mA)	_____	Sets the upper limit for charge termination	NA	C/10
Maximum overcharge (mAh)	_____	Sets the maximum amount of overcharge	256mAh	128mAh
Maximum temperature (°C)	_____	Sets the maximum charge temperature	61°C	61°C
$\Delta T/\Delta t$ (°C/min)	_____	Sets the termination rate	3°C/3min	4.6°C/20s
Fast-charge efficiency (%)	_____	Sets the fast-charge efficiency factor	95%	100%
Maintenance charge efficiency (%)	_____	Sets the maintence charge efficiency factor	80%	100%
Self-discharge rate (%/day)	_____	Sets the batterys self-discharge rate	1.5%/day	0.2%/day
EDV1 (mV)	_____	Sets the initial end-of-discharge warning	1.05V/cell	3.0V/cell
EDVF (mV)	_____	Sets the final end-of-discharge warning	1.0V/cell	2.8V/cell
Hold-off timer for $\Delta T/\Delta t$ (sec.)	_____	Sets the hold off period for $\Delta T/\Delta t$ termination	180s	320s
Manufacturer name	_____	Programs manufacturer's name (11 char. max)	bq	bq
Device name	_____	Programs device name (7 char. max)	bq36	bq202
Chemistry	_____	Programs pack's chemistry (7 char. max)	NiMH	LION
Manufacturer data	_____	Open field (5 char. max)	2040	2040
FAE Approval	_____		Date: _____	

3/6

bq2145 Schematic

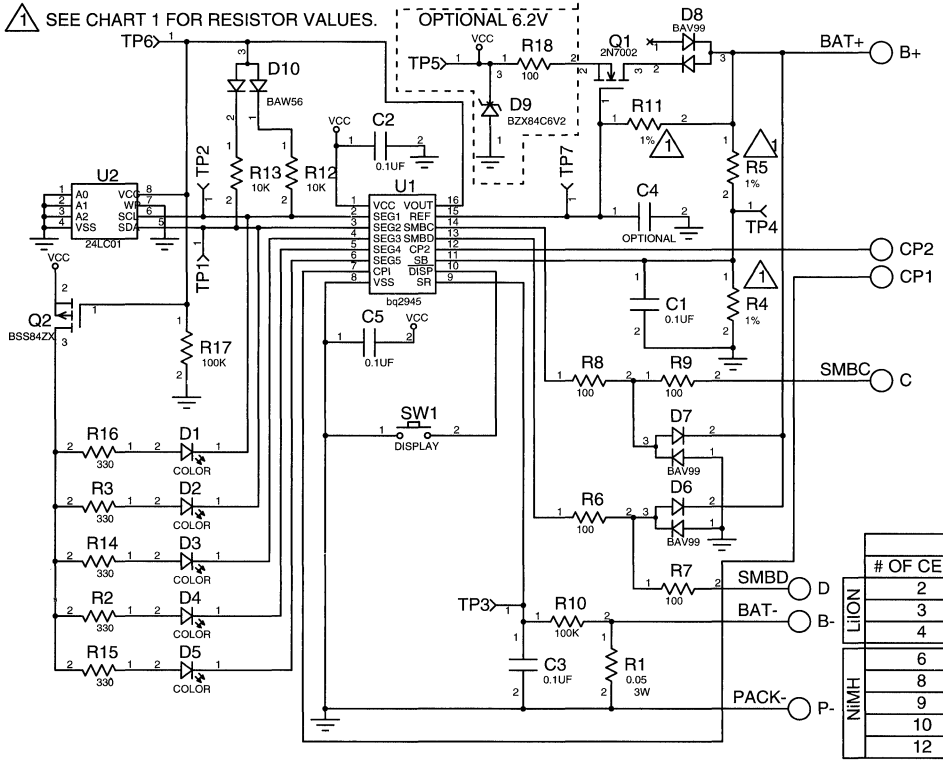
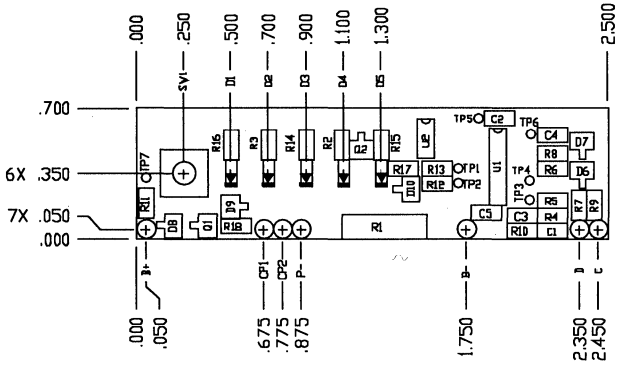


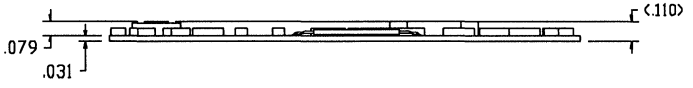
CHART 1

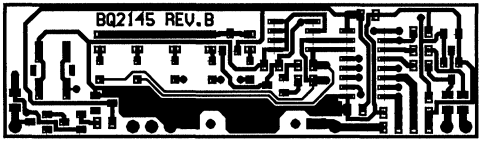
	# OF CELLS	R5	R11	R4
LiION	2	301K	86.5K	100K
	3	499K	909K	100K
	4	698K	909K	100K
NiMH	6	499K	162K	100K
	8	698K	402K	100K
	9	806K	604K	100K
	10	909K	909K	100K
	12	909K	1M	86.5K

4/6

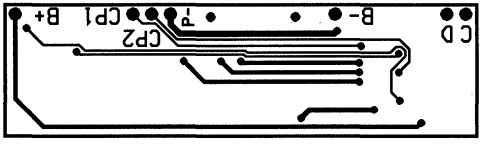
bq2145 Board







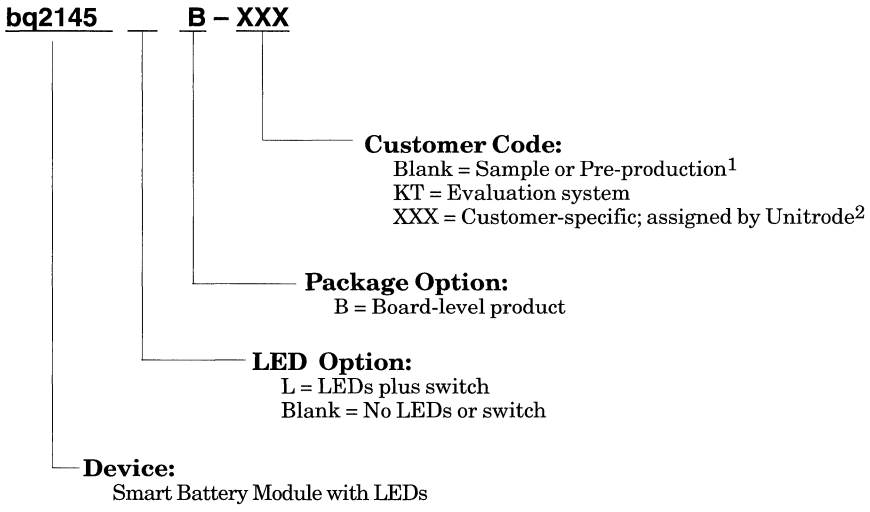
LAYER 1



LAYER 2

5/6

Ordering Information



Notes:
1. Requires configuration sheet (see Table 1)
2. Example production part number: bq2145LB-001

6/6

Smart Battery Module with LEDs and Pack Supervisor

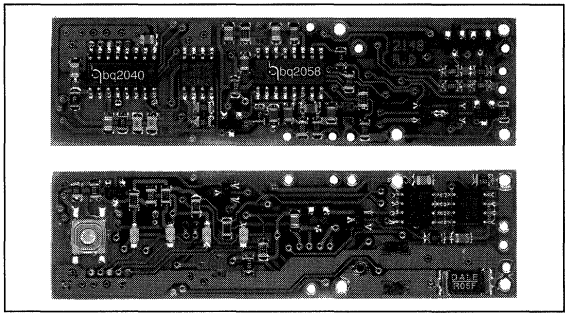
Features

- Complete smart battery management solution for Li-Ion battery packs
- Accurate measurement of available battery capacity
- Provides overvoltage, undervoltage, and overcurrent protection
- Designed for battery pack integration:
  - Small size
  - Includes bq2040 and bq2058 ICs, and configuration EEPROM
  - On-board charge and discharge control FETs
  - Low operating current for minimal battery drain
- Critical battery information available over two-wire serial port
- "L" version includes 4 push-button activated LEDs to display state-of-charge information

General Description

The bq2148 Smaart Battery Module provides a complete and compact battery management solution for Li-Ion battery packs. Designed for battery pack integration, the bq2168 combines the bq2040H Gas Gauge IC with the bq2058 Supervisor IC on a small printed circuit board. The board includes all the necessary components to accurately monitor battery capacity and protect the cells from overvoltage, undervoltage, and overcurrent conditions. The board works with three or four Li-Ion series cells.

The Gas Gauge IC uses the on-board sense resistor to track charge and discharge activity of the battery pack. Critical battery information can be accessed through the serial communications port at SMBC/SMBD. The bq2148 uses the SMBus communications protocol and supports the Smart Battery Data Commands in the SBD specification. The supervisor circuit consists of the bq2058 and two FETs. The bq2058 controls the FETs to protect the batteries during charge/discharge cycles and short circuit conditions. The bq2168 provides contacts for the positive and negative terminals of each battery in the stack. Please refer to the bq2040 and bq2058 data sheets for the specifics on the operation of the power gauge and supervisor ICs.



Unitrode configures the bq2168 based on the information requested in Table 1. The configuration defines all the EEPROM parameters and the protection threshold. Figure 1 shows how the module connects to the cells.

The bq2148L includes four LEDs to display remaining capacity in 25% increments of the learned capacity. The LEDs are activated with the onboard push-button switch.

A module development kit is also available for the bq2148. The bq2148B-KT or the bq2148LB-KT includes one configured module and the following:

1) An EV2200-40 interface board that allows connection to the serial port of any AT-compatible computer.
2) Menu driven software to display charge/discharge activity and to allow user interface to the bq2040 from any standard Windows 3.1x or 95 PC.

Pin Descriptions

POS	**PACK+/Pack positive**
NEG	**PACK-/Pack negative**
SMBC	**Communications clock**
SMBD	**Serial data**
ITEST	**Overcurrent test input**
B1P	**Battery 1 positive input**
B1N	**Battery 1 negative input**
B2N	**Battery 2 negative input**
B3N	**Battery 3 negative input**
B4N	**Battery 4 negative input**

Table 1. bq2148 Module Configuration

Customer Name: _____

Contact: _____ Phone: _____

Address: _____

Sales Contact: _____ Phone: _____

Board Configuration

LEDs and switch _____ Yes or No

Display mode _____ Relative or Absolute

Discharge current (3.9A max.) Min _____ Avg _____ Max _____

Duration at max. discharge _____

Overvoltage threshold (4.25, 4.30, or 4.35V) _____

Number of series cells _____

EEPROM Configuration			Typical Values
Remaining time alarm (min)	_____	Sets the low time alarm level	10 min
Remaining capacity alarm (mAh)	_____	Sets the low capacity alarm level	C/10
Charging voltage (mV)	_____	Sets the requested charging voltage	4.1V/cell
Design cpaacity (mAh)	_____	Defines the battery pack capacity	3600
Design voltage (mV)	_____	Defines the battery pack voltage	10800
Manufacturer date	_____	Battery pack manufacturer date	mm/dd/yy
Serial number	_____	Battery pack serial number	0-65535
Fast-charging current (mA)	_____	Sets the requested charging current	1C
Maintenance charging current (mA)	_____	Sets the requested maintenance charging current	0
Li-Ion taper current (mA)	_____	Sets the upper limit for charge termination	C/10
Maximum overcharge (mAh)	_____	Sets the maximum amount of overcharge	128mAh
Maximum temperature (°C)	_____	Sets the maximum charge temperature	61°C
ΔT/Δt (°C/min)	_____	Sets the termination rate	4.6°C/20s
Fast-charge efficiency (%)	_____	Sets the fast-charge efficiency factor	100%
Maintenance charge efficiency (%)	_____	Sets the maintence charge efficiency factor	100%
Self-discharge rate (%/day)	_____	Sets the batterys self-discharge rate	0.2%/day
EDV1 (mV)	_____	Sets the initial end-of-discharge warning	3.0V/cell
EDVF (mV)	_____	Sets the final end-of-discharge warning	2.8V/cell
Hold-off timer for ΔT/Δt (sec.)	_____	Sets the hold off period for ΔT/Δt termination	320s
Manufacturer name	_____	Programs manufacturer's name (11 char. max)	bq
Device name	_____	Programs device name (7 char. max)	bq202
Chemistry	_____	Programs pack's chemistry (5 char. max)	LION
Manufacturer data	_____	Open field (5 char. max)	2040
FAE approval:	_____	Date: _____	

2/7

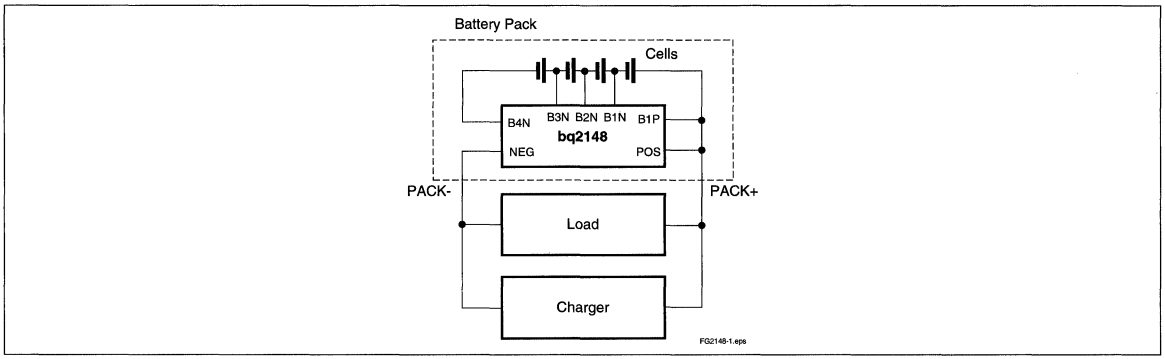


Figure 1. Module Connection Diagram

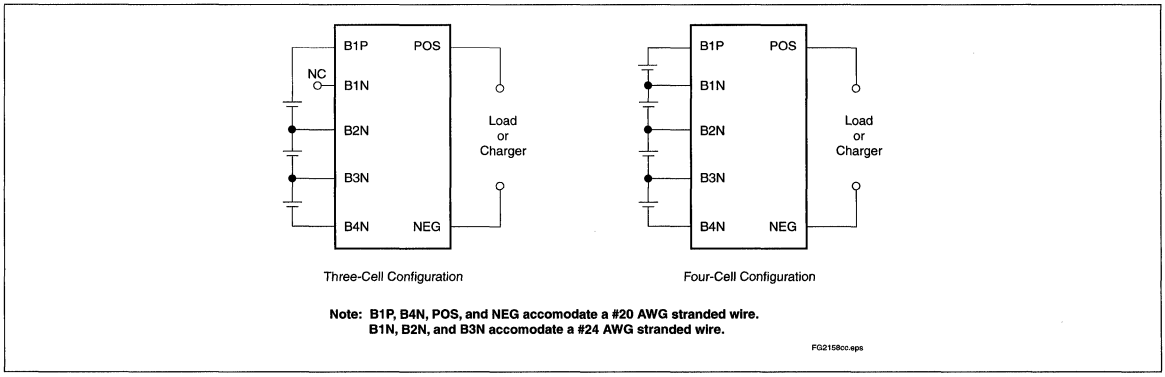


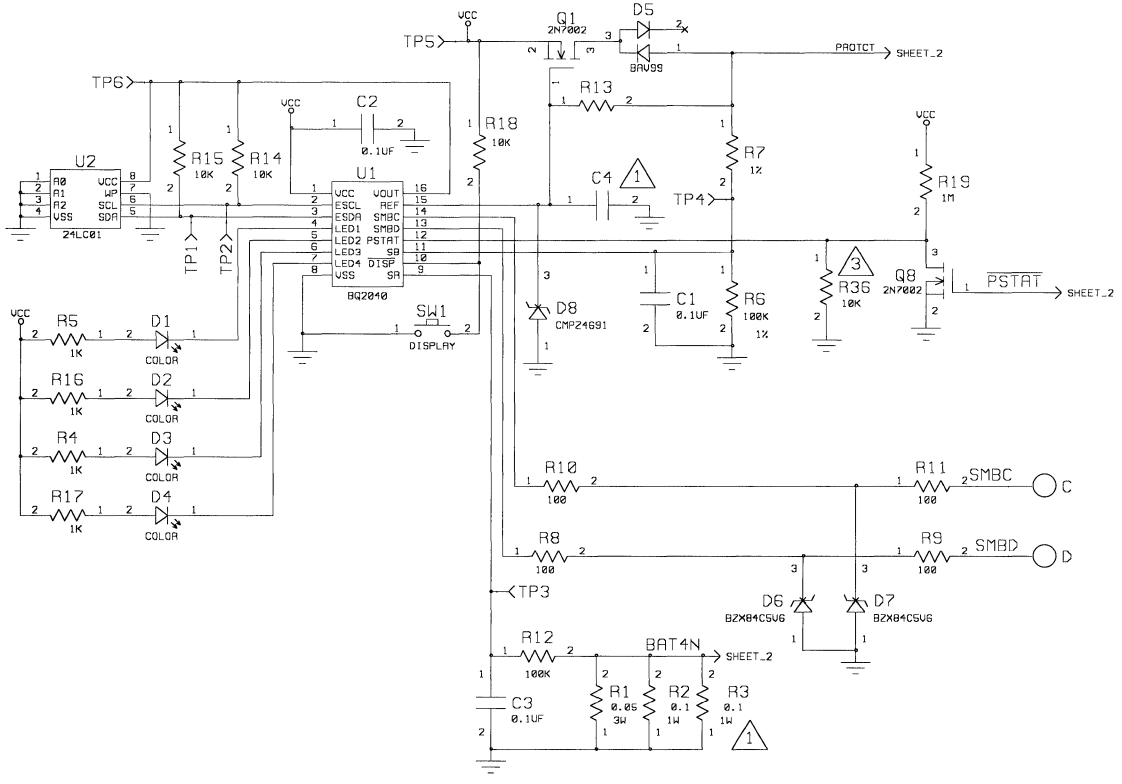
Figure 1. Module Connection Diagram

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{OP}	Supply voltage (B1P to B4N)	18	V	DC
V_{TR}	Maximum transient voltage (B1P to B4N)	32	V	Maximum duration = 1.5µs
V_{CHG}	Charging voltage (POS to NEG)	18	V	
I_{CHG}	Continuous charge/discharge current	3.9	A	V_{OP} > 6V T_A = 25°C
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-55 to +125	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

bq2148 Schematic



1 2 3 Component values depend on user-provided information in Table 1.

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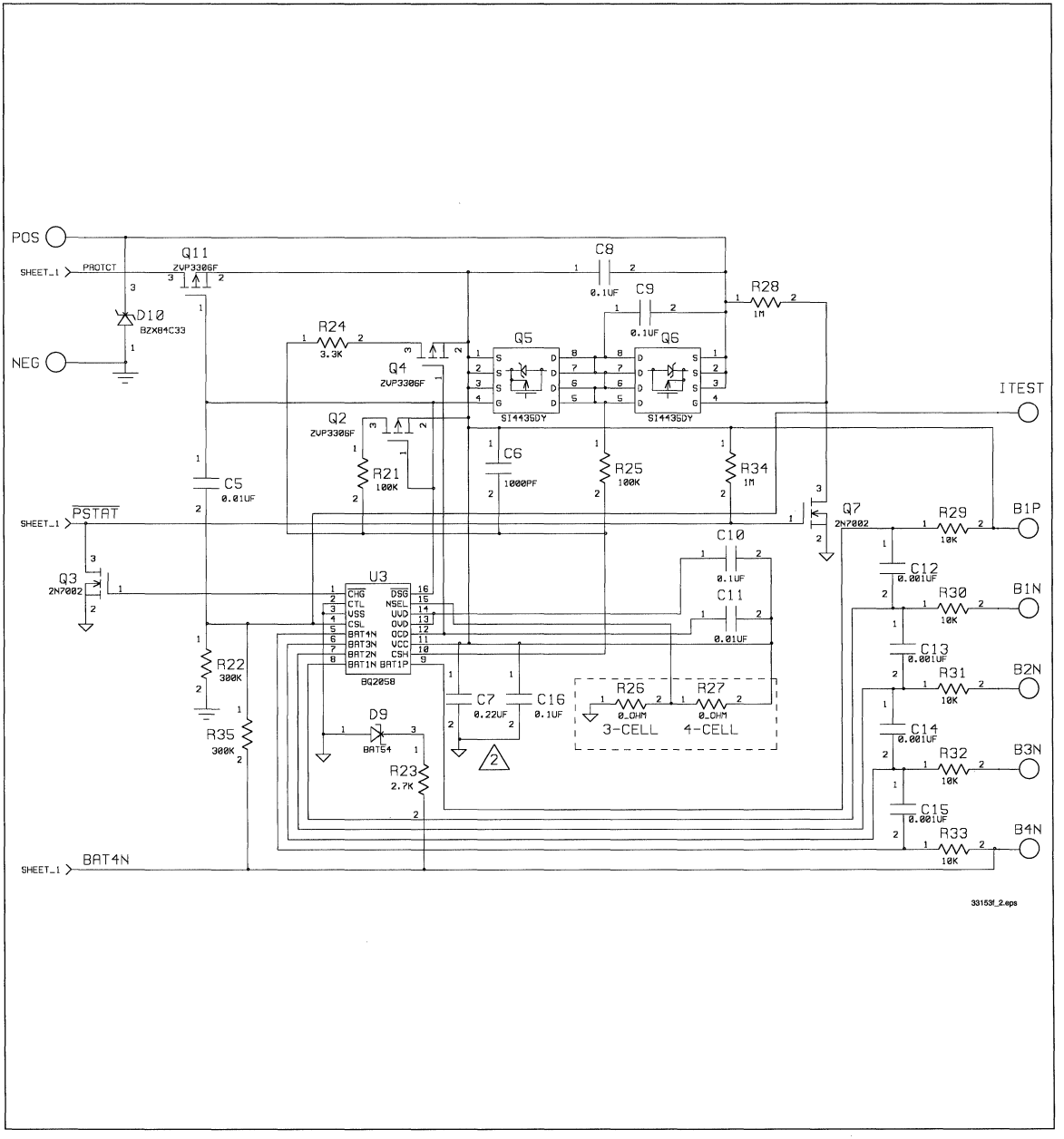
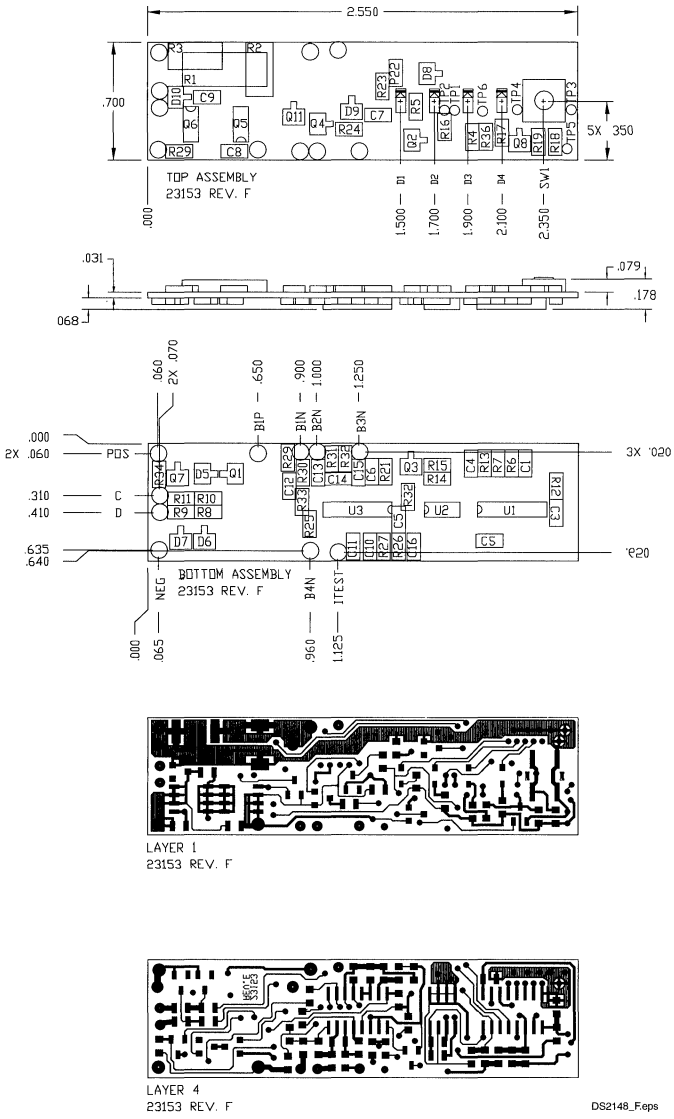
4/7

bq2148 Schematic (Continued)



bq2148 Board



DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
V_{OP}	Operating voltage, B1P to B4N	4.0	-	18	V	
I_{CCA}	Operating current	-	-	350	µA	
R_{ON}	On resistance, B1P to POS	-	-	50	mΩ	T_A = 25°C, V_{OP} = 10V

DC Thresholds ($T_A = T_{OPR}$)

Symbol	Parameter	Value	Tolerance	Unit	Notes
V_{OV}	Overvoltage threshold	4.25	± 50mV	V	
V_{CE}	Charge enable voltage	V_{OV} - 100mV	± 50mV	V	
V_{UV}	Undervoltage limit	2.25	± 100mV	V	
I_{OC}	Overcurrent limit	3.4		A	T_A = 25°C
		3.8		A	T_A = 60°C
t_{UVD}	Undervoltage delay	950	±50%	ms	T_A = 30°C
V_{CD}	Charge detect threshold	70	-60, +80	mV	
t_{OVD}	Overvoltage delay	950	±50%	ms	T_A = 30°C
t_{OCD}	Overcurrent delay	12	±60%	ms	T_A = 30°C

Note: The thresholds above reflect the operation of a bq2148 using the standard bq2058 IC (V_{OV} = 4.25V). Specify other versions of the bq2058 by indicating the appropriate V_{OV} threshold in Table 1.

Ordering Information

bq2148 B — ___

Customer Code:
Blank = Sample or Pre-production[1]
KT = Evaluation system
XXX = Customer-specific; assigned by Unitrode[2]

Package Option:
B = Board-level product

LED Option:
L = LEDs plus switch
Blank = No LEDs or switch

Device:
Smart Battery Module with LEDs and Pack Supervisor

Notes:
1. Requires configuration sheet (Table 1)
2. Example production part number: bq2148LB-001

7/7

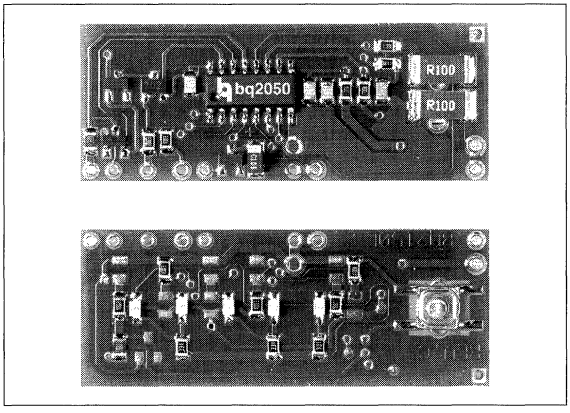
UNITRODE

bq2150

Li-Ion Power Gauge™ Module

Features

- Complete bq2050 Power Gauge solution for Li-Ion battery packs
- Battery information available over a single-wire bidirectional serial port
- Battery state-of-charge monitoring for 2- to 4-cell series applications
- On-board regulator allows direct connection to the battery
- "L" version includes push-button activated LEDs to display state-of-charge information
- Nominal capacity pre-configured
- Compact size for battery pack integration



5

General Description

The bq2150 Power Gauge Module provides a complete and compact solution for capacity monitoring of Li-Ion battery packs. Designed for battery pack integration, the bq2150 incorporates a bq2050 Gas Gauge IC, a current sense resistor, and all other components necessary to accurately monitor and display the capacity of 2 to 4 series cells.

The bq2150L includes five LEDs to display remaining capacity in 20% increments of the learned capacity. The LEDs are activated with the onboard push-button switch.

Contacts are provided on the bq2150 for direct connection to the battery stack (BAT+, BAT-) and the serial communications port (DQ). The RBI input provides backup power to the bq2050 in the event that the cells are removed or the battery is turned off. The bq2150 has a 1µF capacitor onboard connected to RBI to supply backup power for about an hour. In battery packs that use high-side FETs to control the charge/discharge of the Li-Ion cells, the RBI input can be wired to a single cell to provide prolonged data retention times. The SD input allows an external signal (active low) to turn the bq2050 IC off to minimize internal current consumption of the battery pack and maximize storage life of the pack in the system. When turned off, the bq2050 is nonfunctional, and the RBI power source maintains register information. Please refer to the bq2050 data sheet for the specifics on the operation of the gas gauge.

Unitrode configures the bq2150 based on the information requested in Table 1. The configuration defines the number of series cells, the nominal battery pack capacity, and the Li-Ion battery type (coke or graphite anode). Figure 1 shows how the module connects to the cells.

A module development kit is also available for the bq2150. The bq2150B-KT or the bq2150LB-KT includes one configured module and the following:

1) An interface board that allows connection to the serial port of an AT-compatible computer.
2) Menu-driven software to display charge/discharge activity and to allow user interface to the bq2050 from any standard DOS PC.
3) Source code for the TSR.

Pin Descriptions

P1	**DQ/Serial Communications port**
P2	**No connect**
P3	**BAT+/Battery positive/pack positive**
P4	**SD/Shutdown**
P5	**RBI/Register backup input**
P6	**GND/Ground**
P7	**PACK-/Pack negative**
P8	**BAT-/Battery negative**

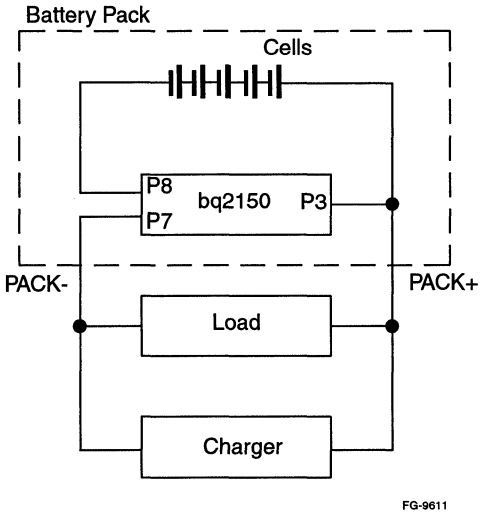


Figure 1. Module Connection Diagram

Table 1. bq2150 Module Configuration

Customer Name: _____

Contact: _____ Phone: _____

Address: _____

_____

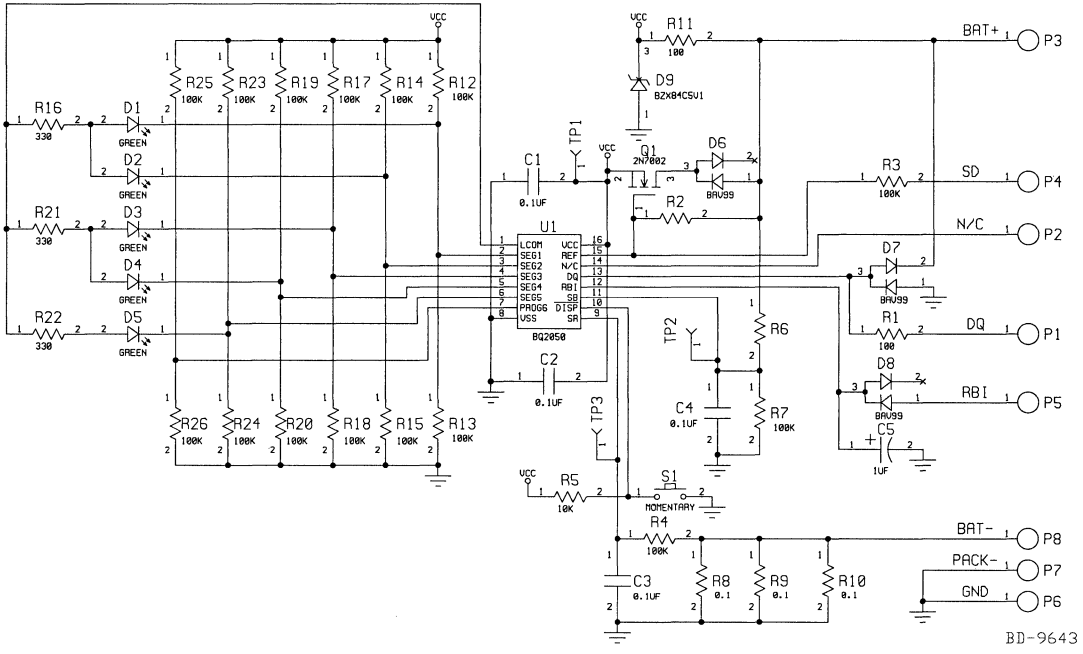
Sales Contact: _____ Phone: _____

Number of series battery cells (2-4)	_____
Coke or graphite cell anode	_____
Battery pack capacity (mAh)	_____
Discharge rate into load (3.0A max)	Min. _____ Avg. _____ Max. _____
Charge rate (3.0A max)	_____
Nominal Available Capacity after reset (Programmed Capacity or Zero)	_____
Self-discharge compensation (Y/N)	_____
LEDs and switch (Y/N)	_____

FAE Approval: _____ Date: _____

2/6

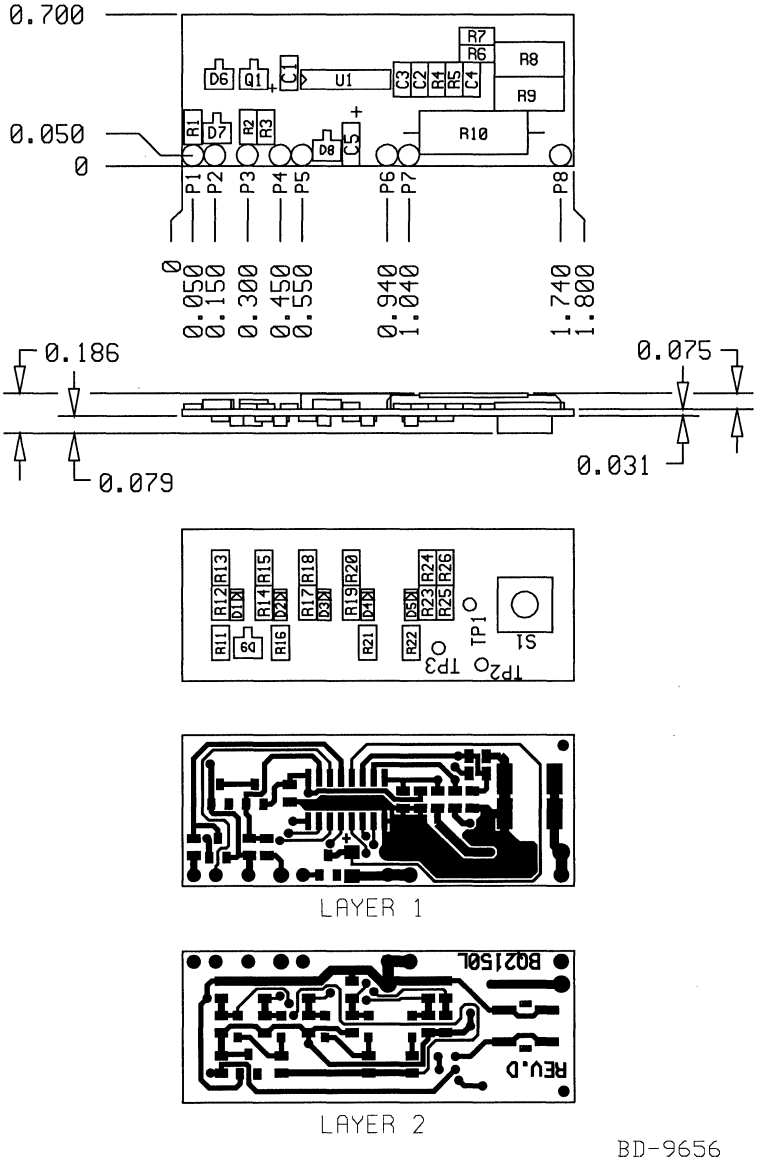
bq2150 Schematic



Note: Schematic shows components that may not be placed on the board, depending on the configuration.

3/6

bq2150 Board



Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Conditions
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	bq2050
All other pins	Relative to V_{SS}	-0.3	+7.0	V	bq2050
P_{SR}	Continuous sense resistor power dissipation	-	3	W	Thru-hole sense resistor
		-	1	W	Surface-mount sense resistor
I_{CHG}	Continuous charge/discharge current	-	3.0	A	
T_{OPR}	Operating temperature	0	+70	°C	Commercial
T_{STR}	Storage temperature	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
NumCell	Number of series cells in battery pack	2	-	4	-	
BAT+	Positive terminal of pack	GND	NumCell * 3.6V	NumCell * 5.4V	V	
BAT-	Negative terminal of pack	GND - 0.3	-	GND+2.0	V	
I_{CC}	Supply current at BAT_{1P} terminal (no external loads)	-	200	300	µA	
R_{DQ}	Internal pull-down	500k	-	-	Ω[1]	
I_{OL}	Open-drain sink current DQ	-	-	5.0	mA[1]	
V_{OL}	Open-drain output low, I_{OL} DQ	-	-	0.5	V[1]	I_{OL} < 5mA
V_{IHDQ}	DQ input high	2.5	-	-	V[1]	
V_{ILDQ}	DQ input low	-	-	0.8	V[1]	
V_{OS}	Voltage offset	-	-	150	µV[1]	

Note: 1. Characterized on PCB, IC 100% tested.

5/6

DC Voltage Thresholds ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	1.45	1.47	1.49	V	BAT+/(2*NumCell)[1]
V_{EDV1}	First empty warning	1.50	1.52	1.55	V	BAT+/(2*NumCell)[1]
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	BAT+/(2*NumCell)[1]
V_{SRO}	Sense range	-300	-	+2000	mV	SR, $V_{SR} + V_{OS}$[2]
V_{SRQ}	Valid charge	210	-	-	µV	$V_{SR} + V_{OS}$ [2, 3]
V_{SRD}	Valid discharge	-	-	-200	µV	$V_{SR} + V_{OS}$ [2, 3]

Notes:
1. At SB input of bq2050
2. At SR input of bq2050.
3. Default value; value set in DMF register.

Data Sheet Revision History

Change No.	Page No.	Description
1	2	Updated Table 1 to include 3.0A limit
1	5	Added 3.0A maximum continuous charge/discharge current specification

Note: Change 1 = May 1999 B changes from April 1999.

Ordering Information

bq2150 B —

Customer Code:
Blank = Sample or Pre-production[1]
KT = Evaluation system
XXX = Customer-specific; assigned by Unitrode[2]

Package Option:
B = Board-level product

LED Option:
L = LEDs plus switch
Blank = No LEDs or switch

Device:
Li-Ion Power Gauge Module

Notes:
1. Requires configuration sheet (Table 1)
2. Example production part number: bq2150LB-001

6/6

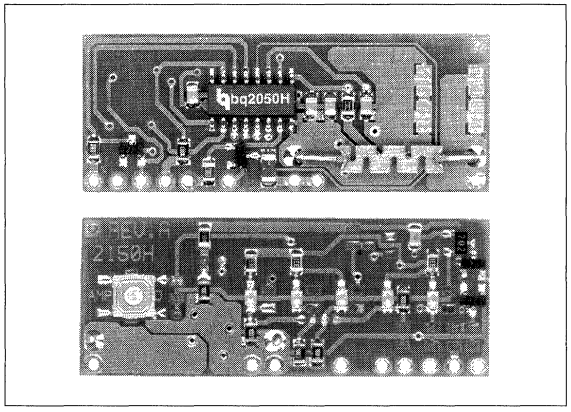
UNITRODE

Preliminary bq2150H

Li-Ion Power Gauge™ Module

Features

- Complete bq2050H Power Gauge solution for Li-Ion battery packs
- Battery information available over a single-wire (HDQ) bidirectional serial port
- Control signals to enhance pack protection
- Battery state-of-charge monitoring for 2- to 5-cell series applications
- On-board regulator allows direct connection to the battery
- "L" version includes push-button activated LEDs to display state-of-charge information
- Nominal capacity pre-configured
- Compact size for battery pack integration



General Description

The bq2150H Power Gauge Module provides a complete and compact solution for capacity monitoring of Li-Ion battery packs. Designed for battery pack integration, the bq2150 incorporates a bq2150H Gas Gauge IC, a current sense resistor, and all other components necessary to accurately monitor and display the capacity of 2 to 5 series cells.

The bq2150L includes five LEDs to display remaining capacity in 20% increments of the learned capacity. The LEDs are activated with the onboard push-button switch.

Contacts are provided on the bq2150H for direct connection to the battery stack (BAT+, BAT-) and the serial communications port (HDQ). The RBI input provides backup power to the bq2150H in the event that the cells are removed or the battery is turned off. The bq2150H has a 1µF capacitor onboard connected to RBI to supply backup power for about an hour. In battery packs that use high-side FETs to control the charge/discharge of the Li-Ion cells, the RBI input can be wired to a single cell to provide prolonged data retention times. The SD input allows an external signal (active low) to turn the bq2050H IC off to minimize internal current consumption of the battery pack and maximize storage life of the pack in the system. When turned off, the bq2150H is non-functional, and the RBI power source maintains register information. Please refer to the bq2050H data sheet for the specifics on the operation of the Gas Gauge.

Unitrode configures the bq2150H based on the information requested in Table 1. The configuration defines the number of series cells, the nominal battery pack capacity, and the Li-Ion battery type (coke or graphite anode). Figure 1 shows how the module connects to the cells.

A module development kit is also available for the bq2150. The bq2150HB-KT or the bq2150HLB-KT includes one configured module and the following:

1) An EV2200-50H interface board that allows connection to the serial port of an AT-compatible computer.
2) Menu-driven software to display charge/discharge activity and to allow user interface to the bq2150H from any standard Windows 3.1x or 95 PC.

Pin Descriptions

P1	**HDQ/Serial Communications port**
P2	**PSTAT/Protector status input**
P3	**BAT+/Battery positive/pack positive**
P4	**SD/Shutdown**
P5	**RBI/Register backup input**
P6	**GND/Ground**
P7	**PACK-/Pack negative**
P8	**BAT-/Battery negative**
P9	**CFC/Charge FET control output**

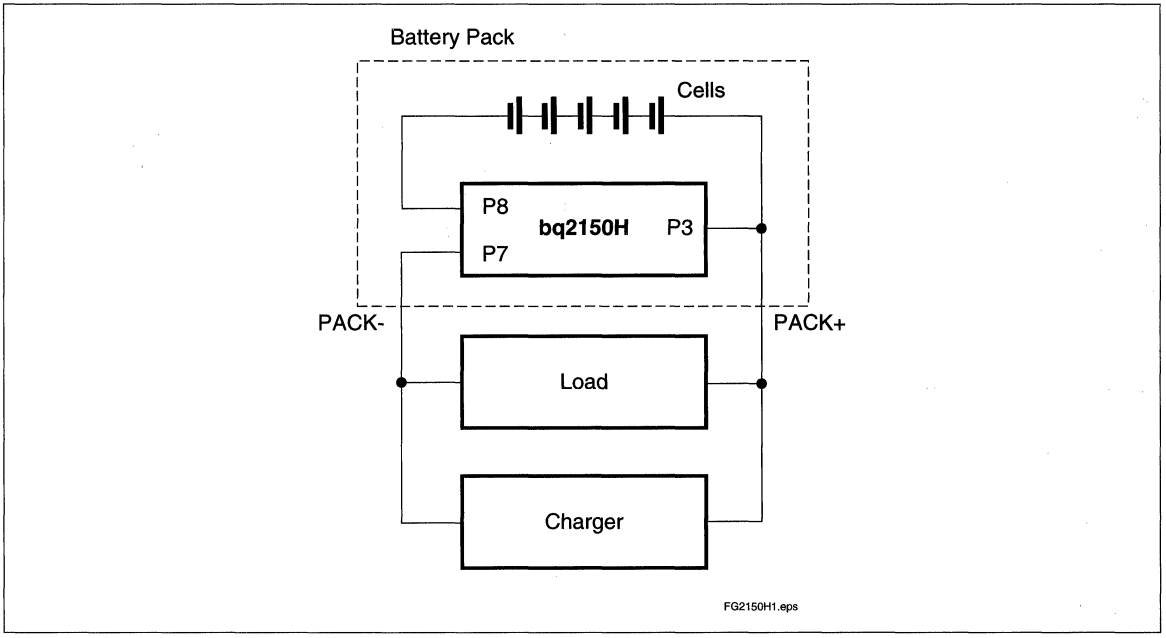


Figure 1. Module Connection Diagram

Table 1. bq2150H Module Configuration

Customer Name: _____

Contact: _____ Phone: _____

Address: _____

_____

Sales Contact: _____ Phone: _____

Number of series battery cells (2-5)	_____
Coke or graphite cell anode	_____
Battery pack capacity (mAh)	_____
Discharge rate into load (A)	min. _____ avg. _____ max. _____
Charge rate	_____
Self-discharge compensation (Y/N)	_____
LEDs and switch (Y/N)	_____

FAE Approval: _____ Date: _____

2/4

bq2150H Schematic

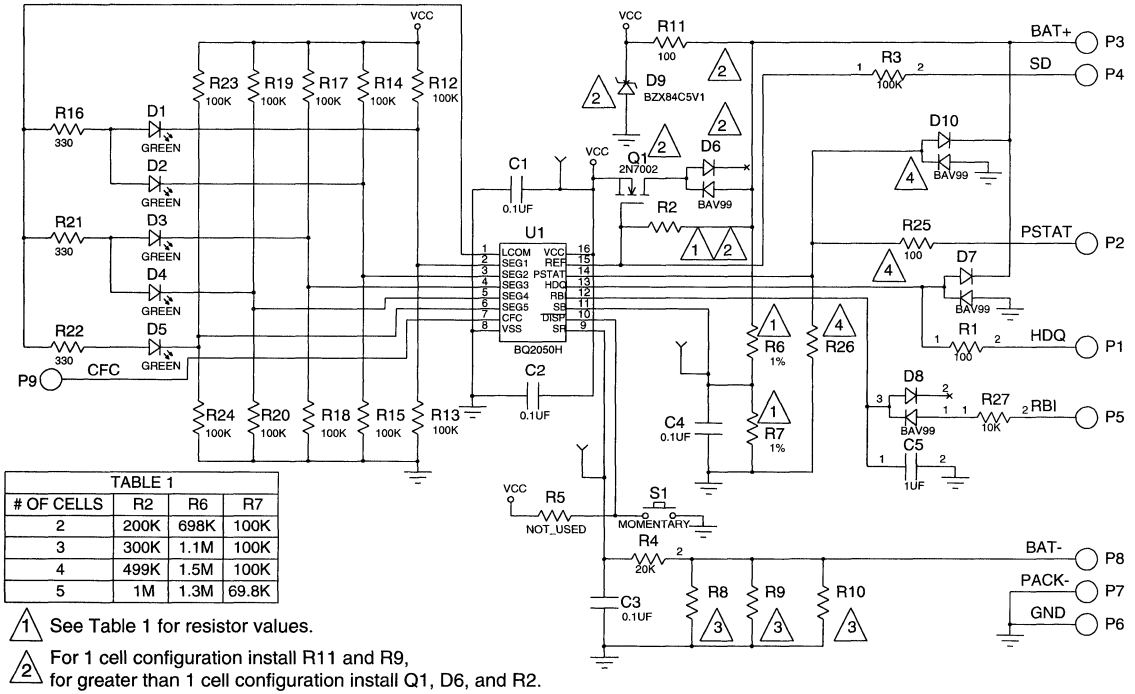


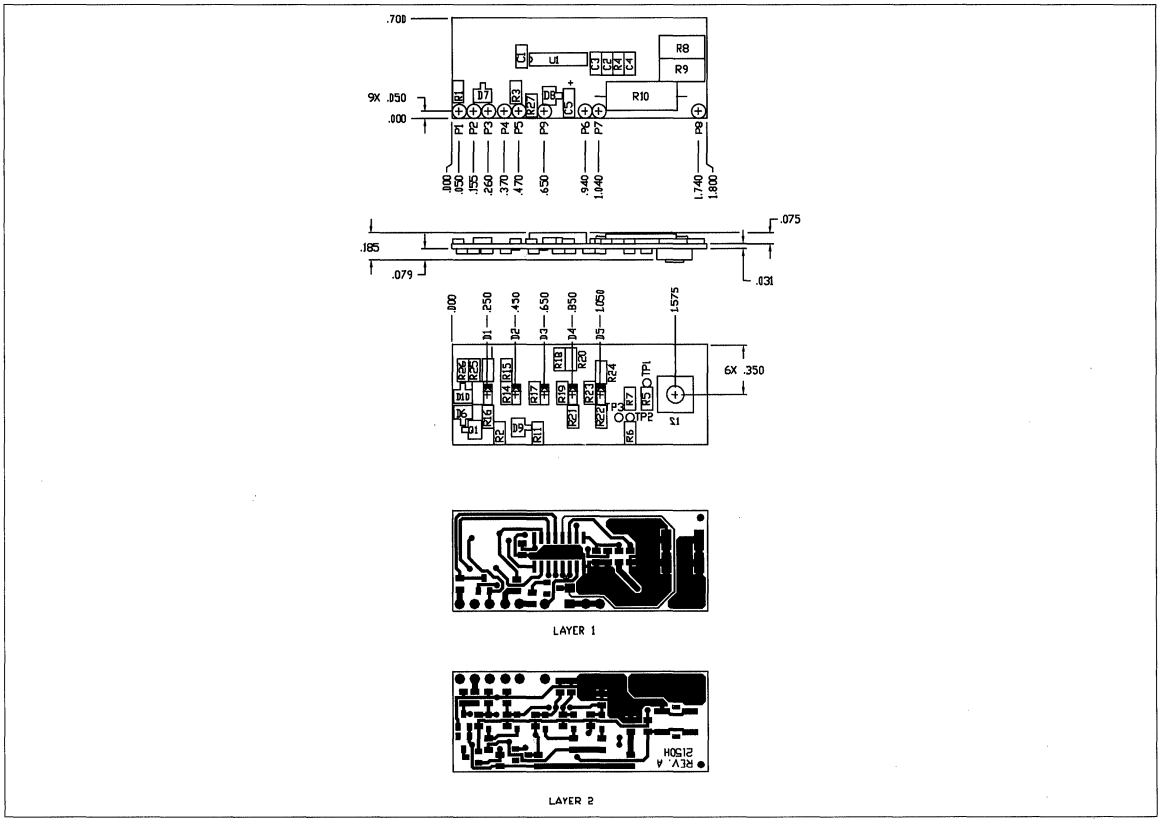
TABLE 1			
# OF CELLS	R2	R6	R7
2	200K	698K	100K
3	300K	1.1M	100K
4	499K	1.5M	100K
5	1M	1.3M	69.8K

1. See Table 1 for resistor values.
2. For 1 cell configuration install R11 and R9, for greater than 1 cell configuration install Q1, D6, and R2.
3. Sense resistor value depends on application.
4. For PSTAT function, install R25 and D10. If not using PSTAT, install 0Ω jumper at R26.

2150H/9-16-97/A

3/4

bq2150H Board



Ordering Information

bq2150H **B** —

Customer Code:
Blank = Sample or Pre-production[1]
KT = Evaluation system
XXX = Customer-specific; assigned by Unitrode[2]

Package Option:
B = Board-level product

LED Option:
L = LEDs plus switch

Device:
Li-Ion Power Gauge Module

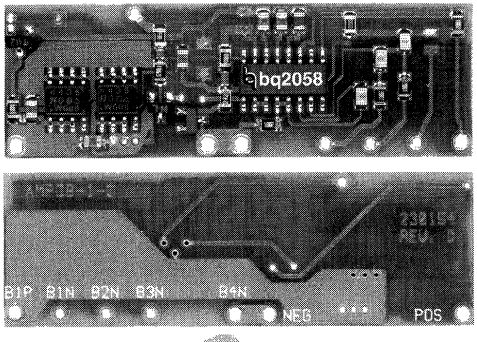
Notes:
1. Requires configuration sheet (Table 1)
2. Example production part number: bq2150HLB-001

bq2158

Three or Four Series Cell Li-Ion Pack Supervisor Module

Features

- Complete and compact lithium-ion pack supervisor
- Provides overvoltage, undervoltage, and overcurrent protection for three or four series Li-Ion cells
- Combines bq2058 with charge/discharge control FETs
- High side low on-resistance FETs
- Designed for battery pack integration
  - Direct connection for series battery terminals
  - Measures 2.10 X 0.70 inches
- Low standby and operating currents



5

General Description

The bq2158 provides a complete solution for the supervision of three or four series Li-Ion cells. Designed for battery pack integration, the bq2158 incorporates a bq2058 Pack Supervisor, two FETs, and all other components required to monitor overvoltage, undervoltage, and overcurrent conditions. The board provides direct connections for the negative and positive terminals of each cell. See Figure 1. Please refer to the bq2058 data sheet for specific information on the operation of the bq2058.

Unitrode configures the bq2158 based on the information in Table 1.

Pin Descriptions

B1P	**Battery 1 positive input/pack positive**
B1N	**Battery 1 negative input**
B2N	**Battery 2 negative input**
B3N	**Battery 3 negative input**
B4N	**Battery 4 negative input**
POS	**Pack positive**
NEG	**Pack negative**

Table 1. bq2158 Module Configuration

Customer Name: _____

Contact: _____ Phone: _____

Address: _____

_____

Sales Contact: _____ Phone: _____

Number of series cells (3 or 4) _____

Overvoltage threshold (4.25, 4.30 or 4.35V) _____

Charge current (3.9A max.) _____

Discharge current (3.9A max.) _____

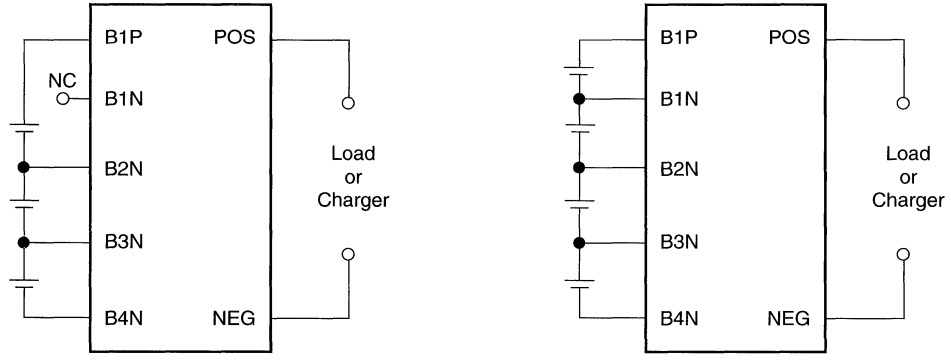
FAE approval: _____ Date: _____

Table 2. Pin Connections

Number of Cells	On-board bq2058 Configuration
3 cells	BAT1N tied to BAT1P NSEL = V_{SS}
4 cells	NSEL = V_{CC}

Operation

The bq2158 monitors each series element for under-voltage, over-voltage, and over-current conditions. If a cell falls below V_{UV} for t_{UVD}, the bq2158 enters into sleep mode. The bq2158 wakes up and enables discharge if a voltage, V_{CD} higher than the battery voltage, is applied across POS and NEG. Charging is disabled if a cell exceeds V_{OV} for t_{OVD}, and can resume when the cell falls below the V_{CE} threshold. The bq2158 turns the discharge FET off if the steady state load current exceeds I_{OC} for t_{OCD} and turns it back on if the load is removed.



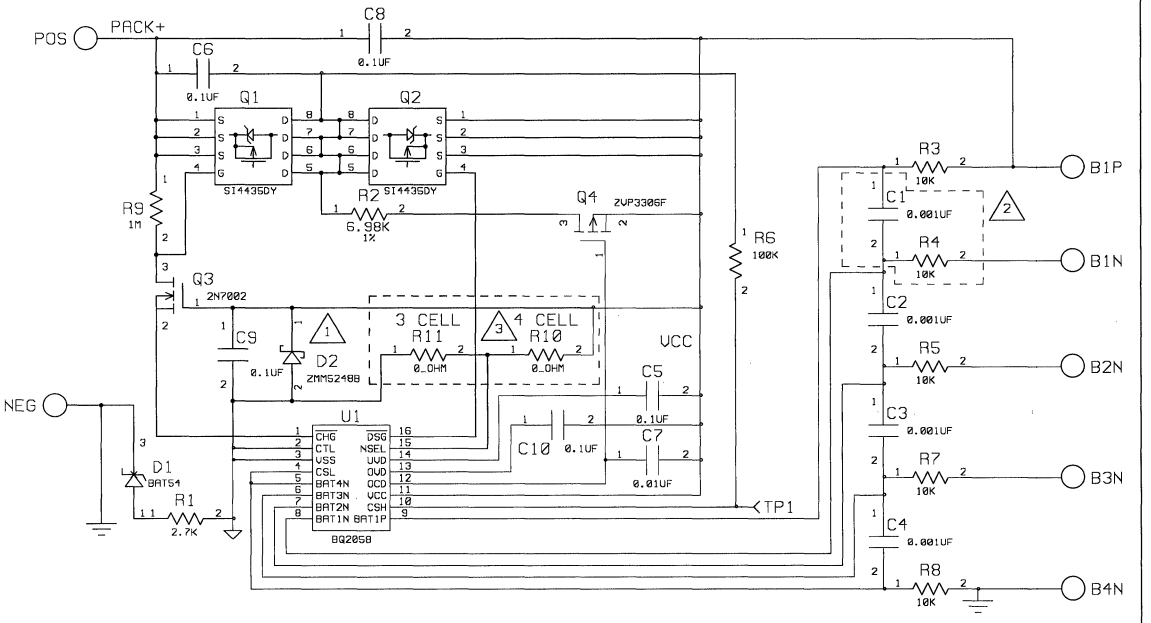
Note: B1P, B4N, POS, and NEG accomodate a #20 AWG stranded wire. B1N, B2N, and B3N accomodate a #24 AWG stranded wire.

FG2158cc.eps

Figure 1. Module Connection Diagram

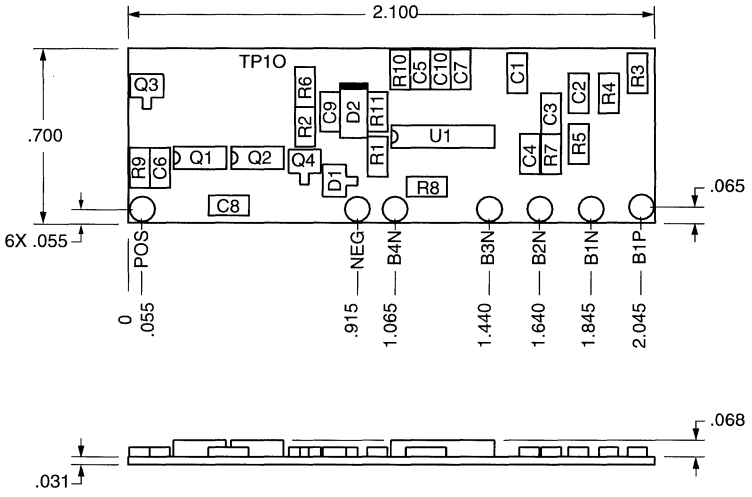
3/7

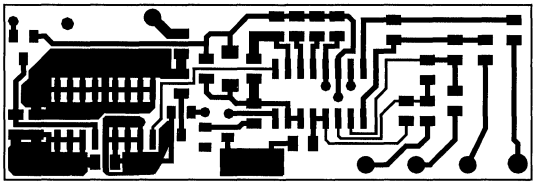
bq2158 Schematic



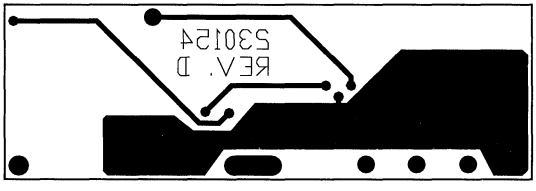
1. NOT USED.
2. FOR 3-CELL APPLICATION REMOVE R4 AND INSTALL 0 OHM RESISTOR IN C1 LOCATION.
3. FOR 3-CELL APPLICATION OMIT R10, FOR 4-CELL APPLICATION OMIT R11.

bq2158 Board





LAYER 1



LAYER 2

5

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{OP}	Supply voltage (B1P to B4N)	18	V	DC
V_{TR}	Maximum transient voltage (B1P to B4N)	32	V	Maximum duration = 1.5µs
V_{CHG}	Charging voltage (POS to NEG)	18	V	
I_{CHG}	Continuous charge/discharge current	3.9	A	V_{OP} > 6V T_A = 25°C
T_{OPR}	Operating temperature	-30 to +70	°C	
T_{STG}	Storage temperature	-55 to +125	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
V_{OP}	Operating voltage, B1P to B4N	4.0	-	18	V	
I_{CCA}	Operating current	-	39	57	µA	
I_{CCS}	Sleep current	-	0.7	1.5	µA	No load across POS and NEG
R_{ON}	On resistance, B1P to POS	-	-	50	mΩ	T_A = 25°C V_{OP} = 10V

DC Thresholds ($T_A = T_{OPR}$)

Symbol	Parameter	Value	Tolerance	Unit	Notes
V_{OV}	Overvoltage threshold	4.25	± 50mV	V	
V_{CE}	Charge enable voltage	V_{OV} - 100mV	± 50mV	V	
V_{UV}	Undervoltage limit	2.25	± 100mV	V	
I_{OC}	Overcurrent limit	3.4		A	T_A = 25°C
		3.8		A	T_A = 60°C
t_{UVD}	Undervoltage delay	950	±50%	ms	T_A = 30°C
V_{CD}	Charge detect threshold	70	-60, +80	mV	
t_{OVD}	Overvoltage delay	950	±50%	ms	T_A = 30°C
t_{OCD}	Overcurrent delay	12	±60%	ms	T_A = 30°C

Note: The thresholds above reflect the operation of a bq2158 using the standard bq2058 IC (V_{OV} = 4.25V). Specify other versions of the bq2058 by indicating the appropriate V_{OV} threshold in Table 1.

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	3	Table 2 pin connections	Clarified onboard bq2058 connection.

Note: Change 1 = May 1999 B changes from July 1996.

Ordering Information

bq2158 B — ____

Customer Code:
Blank = Sample or Pre-production[1]
XXX = Customer-specific; assigned by Unitrode[2]

Package Option:
B = Board-level product

Device:
Three- or Four-Series Cell Li-Ion Supervisor Module

Notes:
1. Requires configuration sheet (Table 1)
2. Example production part number: bq2158B-001

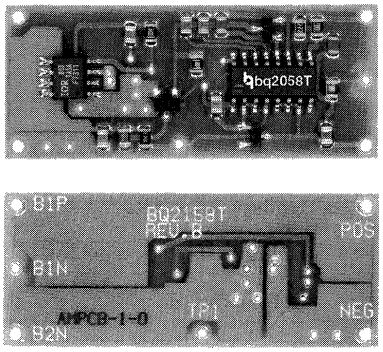
7/7

Preliminary **bq2158T**

Two Series Cell Li-Ion Pack Supervisor Module

Features

- Complete and compact lithium-ion pack supervisor
- Provides overvoltage, undervoltage, and overcurrent protection for two series Li-Ion cells
- Combines bq2058T with charge/discharge control FETs
- Low side low on-resistance FETs
- Designed for battery pack integration
  - Direct connection for series battery terminals
  - Measures 1.70 X 0.70 inches
- Low standby and operating currents



General Description

The bq2158T provides a complete solution for the supervision of two series Li-Ion cells. Designed for battery pack integration, the bq2158T incorporates a bq2058T Pack Supervisor, two FETs, and all other components required to monitor overvoltage, undervoltage, and overcurrent conditions. The board provides direct connections for the negative and positive terminals of each cell. See Figure 1. Please refer to the bq2058T data sheet for specific information on the operation of the bq2058T.

Unitrode configures the bq2158T based on the information in Table 1.

Pin Descriptions

B1P	**Battery 1 positive input**
B1N	**Battery 1 negative input**
B2N	**Battery 2 negative input**
POS	**Pack positive**
NEG	**Pack negative**

Table 1. bq2158T Module Configuration

Customer Name: _____

Contact: _____ Phone: _____

Address: _____

_____

Sales Contact: _____ Phone: _____

Overvoltage threshold (4.25V) _____

Charge current (3.8A max.) _____

Discharge current (3.8A max.) _____

FAE approval: _____ Date: _____

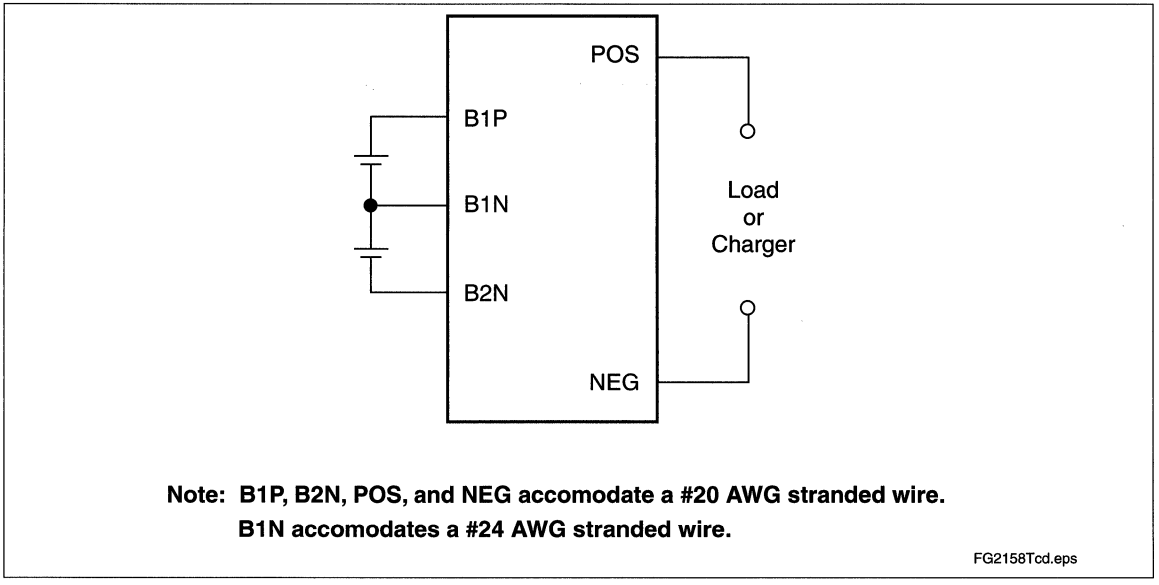
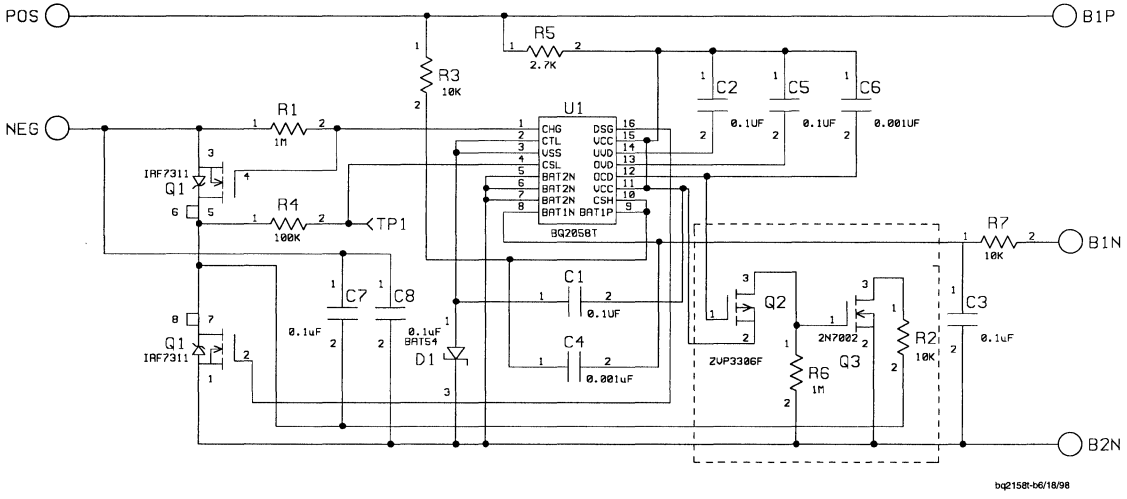


Figure 1. Module Connection Diagram

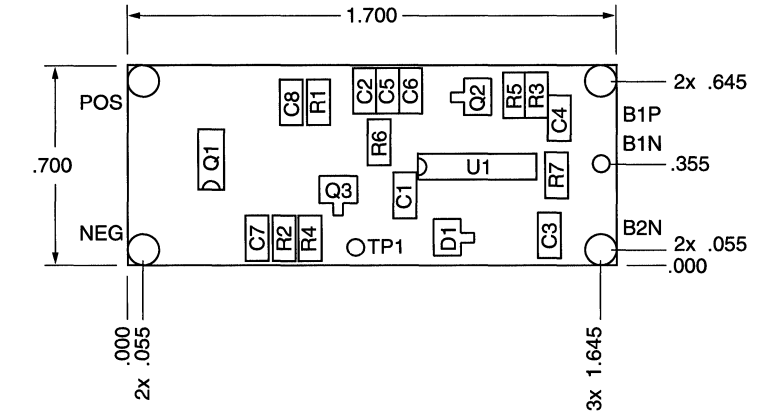
Operation

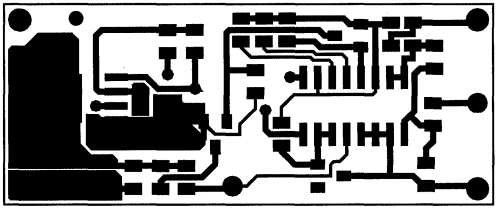
The bq2158T monitors each series element for under-voltage, over-voltage, and over-current conditions. If a cell falls below V_{UV} for t_{UVD}, the bq2158T enters into sleep mode. The bq2158T wakes up and enables discharge if a voltage, V_{CD} higher than the battery voltage, is applied across POS and NEG. Charging is disabled if a cell exceeds V_{OV} for t_{OVD}, and can resume when the cell falls below the V_{CE} threshold. The bq2158T turns the discharge FET off if the steady state load current exceeds I_{OC} for t_{OCD} and turns it back on if the load is removed.

bq2158T Schematic

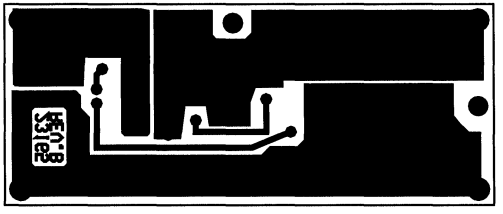


bq2158T Board





LAYER 1



LAYER 2

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{OP}	Supply voltage (B1P to B2N)	12	V	DC
V_{TR}	Maximum transient voltage (B1P to B2N)	32	V	Maximum duration = 1.5µs
V_{CHG}	Charging voltage (POS to NEG)	12	V	
I_{CHG}	Continuous charge/discharge current	3.8	A	V_{OP} > 4V T_A = 25°C
T_{OPR}	Operating temperature	-30 to +70	°C	
T_{STG}	Storage temperature	-55 to +125	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
V_{OP}	Operating voltage, B1P to B2N	4.0	-	12	V	
I_{CCA}	Operating current	-	26	43	µA	
I_{CCS}	Sleep current	-	0.7	1.5	µA	No load across POS and NEG
R_{ON}	On resistance, B2N to NEG	-	-	100	mΩ	T_A = 25°C V_{OP} = 4.5V

6/7

DC Thresholds ($T_A = T_{OPR}$)

Symbol	Parameter	Value	Tolerance	Unit	Notes
V_{OV}	Overvoltage threshold	4.25	± 50mV	V	
V_{CE}	Charge enable voltage	V_{OV} - 100mV	± 50mV	V	
V_{UV}	Undervoltage limit	2.25	± 100mV	V	
I_{OC}	Overcurrent limit	3.3		A	T_A = 25°C
		3		A	T_A = 60°C
t_{UVD}	Undervoltage delay	950	±50%	ms	T_A = 30°C
V_{CD}	Charge detect threshold	70	-60, +80	mV	
t_{OVD}	Overvoltage delay	950	±50%	ms	T_A = 30°C
t_{OCD}	Overcurrent delay	12	±60%	ms	T_A = 30°C

Ordering Information

bq2158T B — ____

Customer Code:
Blank = Sample or Pre-production[1]
XXX = Customer-specific; assigned by Unitrode[2]

Package Option:
B = Board-level product

Device:
Two-Series Cell Li-Ion Supervisor Module

Notes:
1. Requires configuration sheet (Table 1)
2. Example production part number: bq2158TB-001

NiCd or NiMH Gas Gauge Module with Fast-Charge Control

Features

- Complete bq2004/bq2014 battery management solution for NiCd or NiMH pack
- Accurate battery state-of-charge monitoring
- Reliable fast charge termination
- Automatic full capacity calibration
- Battery information available over a single-wire bi-directional serial port
- Nominal capacity, cell chemistry, and charge control parameters pre-configured
- Compact size for battery pack integration

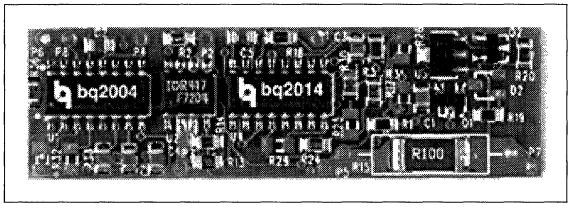
General Description

The bq2164 Gas Gauge Module provides a complete and compact battery management solution for NiCd and NiMH battery packs. Designed for battery pack integration, the bq2164 combines the bq2014 Gas Gauge IC with the bq2004 Fast-Charge IC on a small printed circuit board. The board includes all the necessary components to accurately monitor the capacity and reliably terminate fast charge of 5 to 10 series cells.

The gas gauge IC uses the onboard sense resistor to track charge and discharge activity of the battery pack. The fast charge IC gates a current-limited or constant-current charging supply connected to PACK+. Charging termination is based on $\Delta T/\Delta t$ or $-\Delta V/PVD$, maximum temperature, time, and voltage. The bq2004 signals charge completion to the bq2014 to indicate full capacity. The charge complete signal to the gas gauge eliminates the need to fully cycle the battery pack to initially calibrate full pack capacity.

Contacts are provided on the bq2164 for direct connection to the battery stack (BAT+, BAT-), the gas gauge's communications port (DQ), and the thermistor (THERM+, THERM). The thermistor is required for temperature fast charge termination. Please refer to the bq2004 and bq2014 data sheets for the specifics on the operation of the gas gauge and the fast charge ICs.

Unitrode configures the bq2164 based on the information requested in Table 1. The configuration defines the number of series cells, the nominal battery pack capacity, the self-discharge rate, and the fast charge control parameters. The control parameters depend on the charge rate, cell chemistry and termination technique



specified in the configuration table. They consist of the fast charge hold-off, safety timers, and the pulse trickle rate as shown in the bq2004 data sheet. The bq2164 is optimized for temperature termination with the thermistor provided with the development kit. Figure 1 shows how the module connects to the cells.

The sense resistor value and type should also be specified on the configuration sheet. The two options available are a 3W through-hole type or a 1W surface-mount type. Please refer to the application note entitled "A Tutorial for Gas Gauging" to select the proper value.

A module development kit is also available for the bq2164. The bq2164B-KT includes one configured module and the following:

1) A serial interface board that allows connection to the RS-232 port of an AT-compatible computer.
2) Menu-driven software with the bq2164 to display charge/discharge activity and to allow user interface to the bq2014 from any standard DOS PC.
3) Source code for the TSR.
4) A Philips 10K NTC Thermistor type 2322-640-63103.

Pin Description

P1	**DQ/Serial communication port**
P2	**BAT+/Battery positive**
P3	**PACK+/Pack positive**
P4	**PACK-/Pack negative**
P5	**BAT-/Battery negative**
P6	**THERM+/Thermistor positive**
P7	**THERM-/Thermistor negative**
P8	**MOD/Fast charge control output**

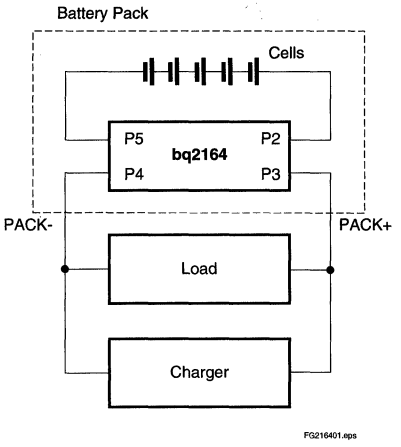


Figure 1. Module Connection Diagram

Table 1. bq2164 Module Configuration

Customer Name: _____

Contact: _____ Phone: _____

Address: _____

_____

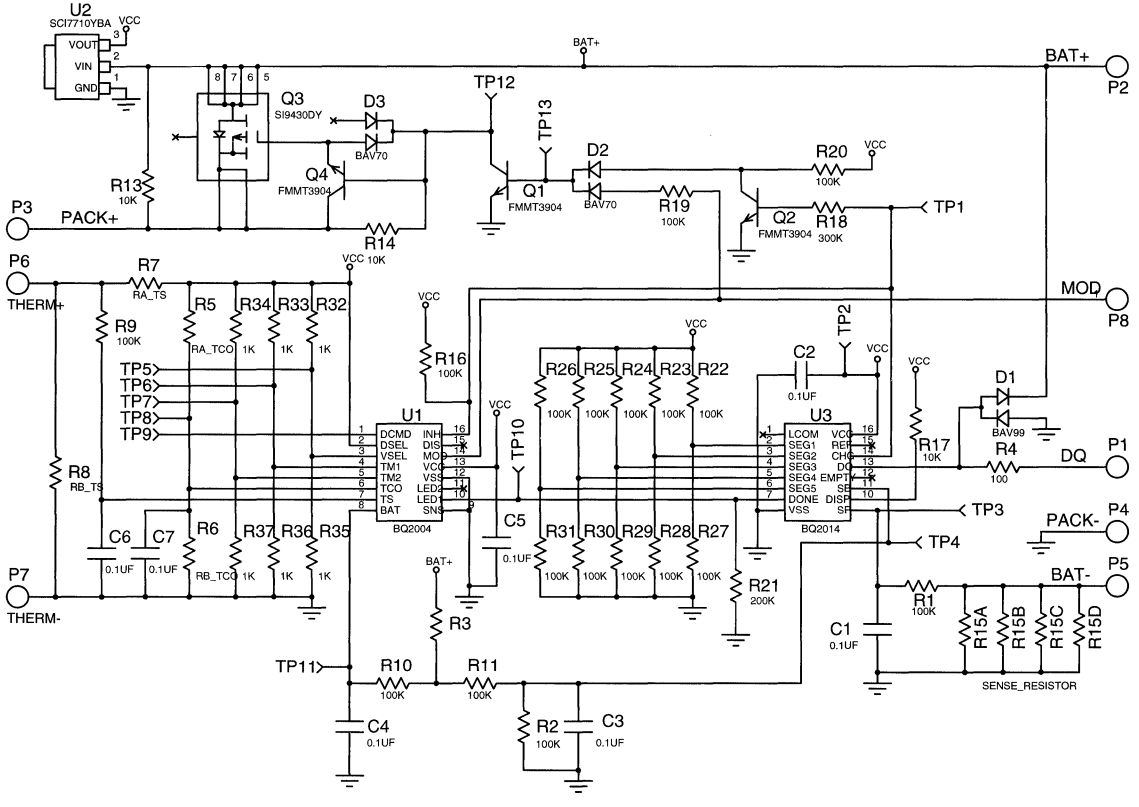
Sales Contact: _____ Phone: _____

Number of series battery cells (5-10)	_____
Battery type (NiCd or NiMH)	_____
Battery pack capacity (mAh)	_____
Discharge rate into load (2.0A max.)	Min. _____ Avg. _____ Max. _____
Sense resistor type: (Thru-hole (3W) or surface-mount (1W))	_____
Sense resistor size in mΩ (0.1Ω standard)	_____
Fast charge current (2.0A max.)	_____
Charge voltage (V)	_____
Temperature termination (enabled/disabled)	_____
PVD or -ΔV termination	_____

FAE Approval _____ Date _____

2/6

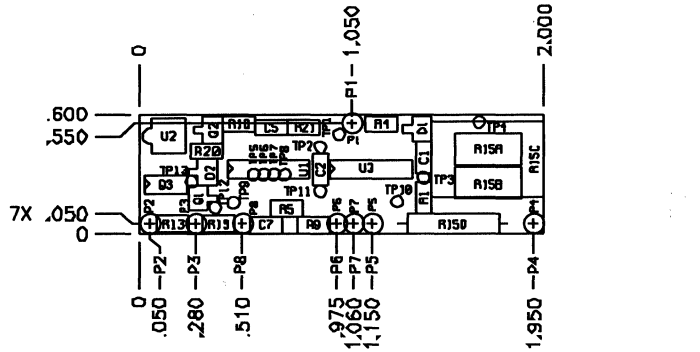
bq2164 Schematic

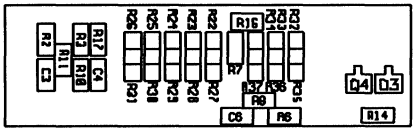


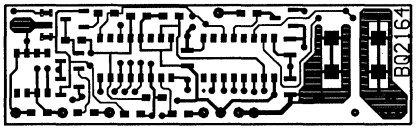
Note: Schematic shows components that may not be placed on the board, depending on the configuration.

3/6

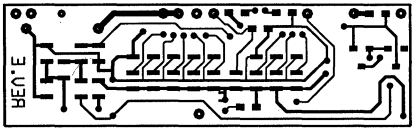
bq2164 Board







LAYER 1



LAYER 2

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
P_{SR}	Continuous sense resistor power dissipation	-	3	W	Thru-hole sense resistor
		-	1	W	Surface-mount sense resistor
V_{CHG}	Charging voltage	-	20	V	
T_{OPR}	Operating temperature	0	+70	°C	Commercial
T_{STR}	Storage temperature	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
NumCell	Number of cells in battery pack	5	-	10	-	
BAT+	Positive terminal of pack	GND	NumCell * 1.2V	NumCell * 1.8V	V	
BAT-	Negative terminal of pack	GND - 0.3	-	GND+2.0	V	
I_{CC}	Supply current at BAT+ terminal (no external loads)	-	200	300	µA	
I_{CHG}	Charge current	-	-	2	A	
I_{DSCHG}	Discharge current	-	-	2	A	
R_{DQ}	Internal pull-down	500k	-	-	Ω[1]	
I_{OL}	Open-drain sink current DQ	-	-	5.0	mA[1]	
V_{OL}	Open-drain output low, DQ	-	-	0.5	V[1]	I_{OL} < 5mA
V_{IHDQ}	DQ input high	2.5	-	-	V[1]	
V_{IHDQ}	DQ input low	-	-	0.8	V[1]	
V_{OS}	Voltage offset			150	µV[1]	

Note: 1. Characterized on PCB, IC 100% tested.

DC Voltage and Temperature Thresholds ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	Final empty warning	0.93	0.95	0.97	V	BAT+/NumCell[1]
V_{EDV1}	First empty warning	1.03	1.05	1.07	V	BAT+/NumCell[1]
V_{MCV}	Maximum single-cell voltage	2.20	2.25	2.30	V	BAT+/NumCell[1]
V_{SRO}	SR sense range	-300	-	+2000	mV	$V_{SR} + V_{OS}$[2]
V_{SRQ}	Valid charge	375	-	-	µV	$V_{SR} + V_{OS}$ [2, 3]
V_{SRD}	Valid discharge	-	-	-300	µV	$V_{SR} + V_{OS}$ [2, 3]
V_{SR1}	Discharge compensation threshold	-120	-150	-180	mV	$V_{SR} + V_{OS}$[2]
T_{LTF}	Low-temperature charging fault	-	10	-	°C	Low-temperature charge inhibit/terminate[4]
T_{HTF}	High-temperature charging fault	-	45	-	°C	High-temperature charge inhibit
V_{EDVC}	Minimum charging cell voltage	-	1	-	V	Minimum cell voltage to initiate charge
V_{MCVC}	Maximum charging cell voltage	-	2	-	V	Maximum cell voltage to initiate or continue charge
$R_{\Delta T/\Delta t}$	$\Delta T/\Delta t$ charge termination rate	-	1	-	°C/ min.	@ 30°C
T_{TCO}	Maximum charging temperature	-	50	-	°C	High-temperature charge termination

Notes:
1. At SB input of bq2014.
2. At SR input of bq2014.
3. Default value; value set in DMF register.
4. PVD termination disables the low-temperature fault charge termination.

Ordering Information

bq2164 B — ____

Customer Code:
Blank = Sample or Pre-production[1]
KT = Evaluation system
XXX = Customer-specific; assigned by Unitrode[2]

Package Option:
B = Board-level product

Device:
NiCd or NiMH Gas Gauge Module with Fast-Charge Control

Notes:
1. Requires configuration sheet (Table 1)
2. Example production part number: bq2164B-001

6/6

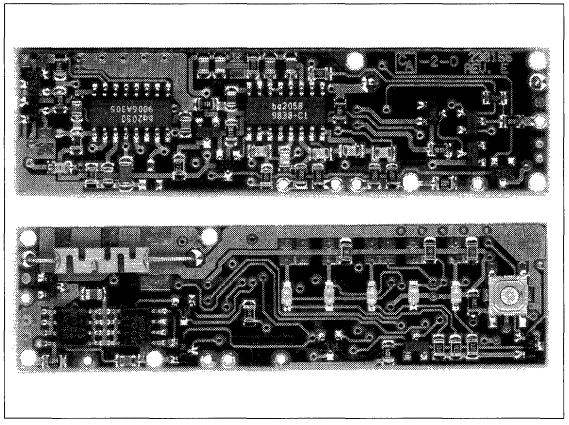
UNITRODE

bq2167

Li-Ion Power Gauge™ Module with Pack Supervisor

Features

- Complete and compact lithium ion gas gauge and protection solution for three or four series cells
- Accurate measurement of available battery capacity
- Provides overvoltage, undervoltage, and overcurrent protection
- Designed for battery pack integration
  - Small size
  - Includes bq2050 and bq2058 ICs
  - On-board charge and discharge control FETs
  - Low operating current for minimal battery drain
- High side FET control
- Battery capacity available through single-wire serial port
- "L" version includes 5 push-button activated LEDs to display state-of-charge information



General Description

The bq2167 Power Gauge Module provides a complete and compact battery management solution for Li-Ion battery packs. Designed for battery pack integration, the bq2167 combines the bq2050 Power Gauge IC with the bq2058 Supervisor IC on a small printed circuit board. The board includes all the necessary components to accurately monitor battery capacity and protect the cells from overvoltage, undervoltage, and overcurrent conditions. The board works with three or four Li-Ion series cells.

The Power Gauge IC uses the on-board sense resistor to track charge and discharge activity of the battery pack. Critical battery information can be accessed through the serial communications port at DQ. The supervisor circuit consists of the bq2058 and two FETs. The bq2058 controls the FETs to protect the batteries during charge/discharge cycles and short circuit conditions. The bq2167 provides contacts for the positive and negative terminals of each battery in the stack. Please refer to the bq2050 and bq2058 data sheets for the specifics on the operation of the power gauge and supervisor ICs.

Unitrode configures the bq2167 based on the information requested in Table 1. The configuration defines the number of series cells, the nominal battery pack capacity, the self-discharge rate, the Li-Ion battery type (coke or graphite anode), and the threshold limits. Figure 1 shows how the module connects to the cells.

The bq2167L includes five LEDs to display remaining capacity in 20% increments of the learned capacity. The LEDs are activated with the onboard push-button switch.

A module development kit is also available for the bq2167. The bq2167B-KT or the bq2167LB-KT includes one configured module and the following:

1) An interface board that allows connection to the serial port of any AT-compatible computer.

2) Menu driven software to display charge/discharge activity and to allow user interface to the bq2050 from any standard DOS PC.

Pin Descriptions

POS	**Pack positive**
B1P	**BAT_{1P}/Battery 1 positive input**
B1N	**BAT_{1N}/Battery 1 negative input**
B2N	**BAT_{2N}/Battery 2 negative input**
B3N	**BAT_{3N}/Battery 3 negative input**
B4N	**BAT_{4N}/Battery 4 negative input**
ITEST	**Overcurrent test input**
DQ	**Serial communications port**
NEG	**Pack negative**

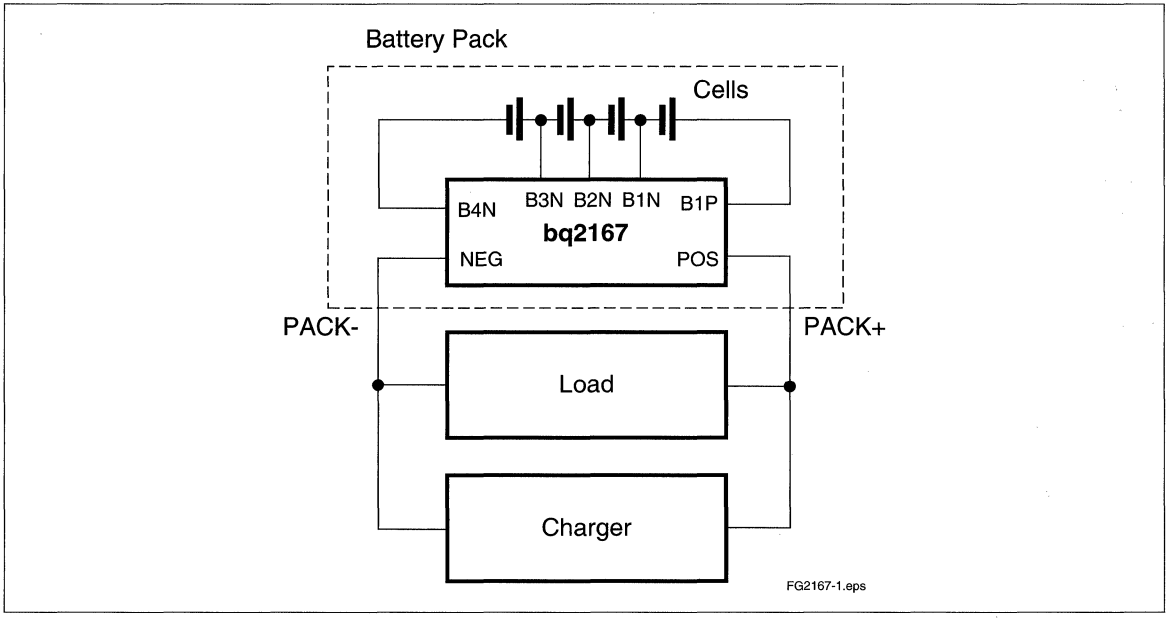


Figure 1. Module Connection Diagram

Table 1. bq2167 Module Configuration

Customer Name: _____

Contact: _____ Phone: _____

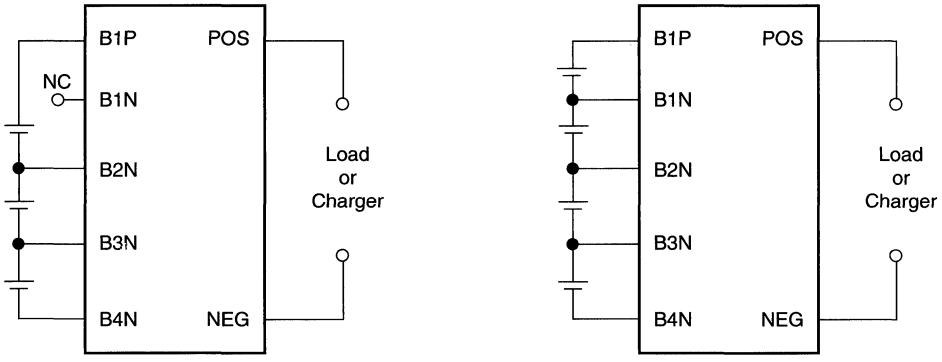
Address: _____

_____

Sales Contact: _____ Phone: _____

Number of series cells (3 or 4)	_____
Coke or graphite cell anode	_____
Battery pack capacity (mAh)	_____
Discharge current into load (3.9A max.)	Min. _____ Avg. _____ Max. _____
Charge current (3.9A max)	_____
Self-discharge compensation (Y/N)	_____
Overvoltage threshold (4.25, 4.30, or 4.35V)	_____
LEDs and switch (Y/N)	_____

FAE approval: _____ Date: _____



Note: B1P, B4N, POS, and NEG accomodate a #20 AWG stranded wire.
B1N, B2N, and B3N accomodate a #24 AWG stranded wire.

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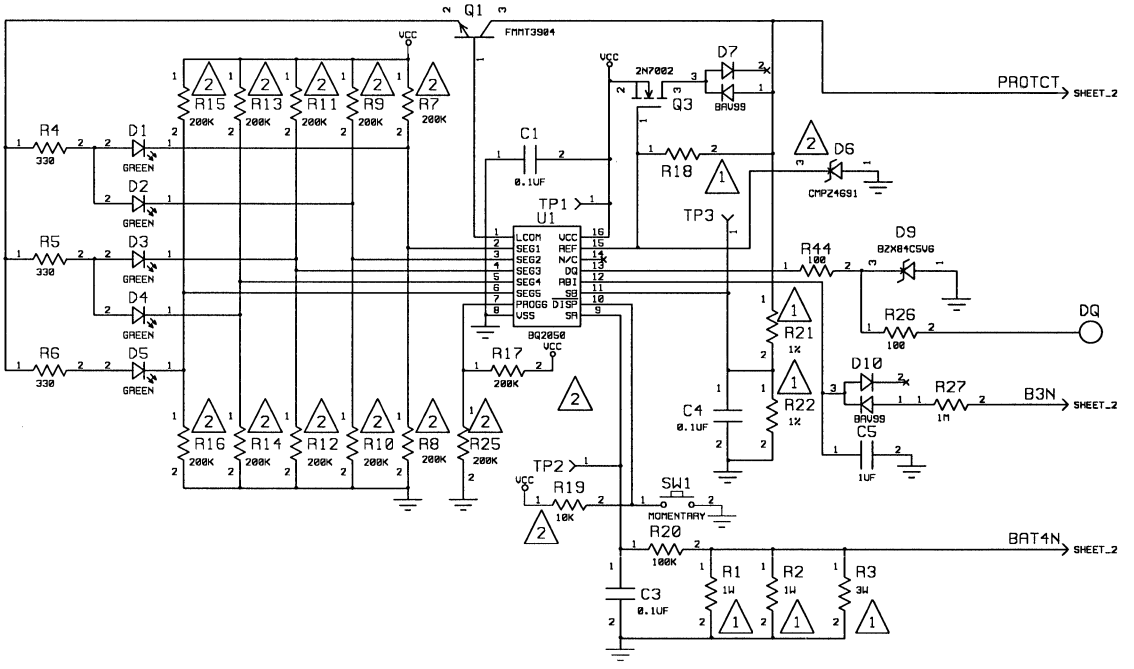
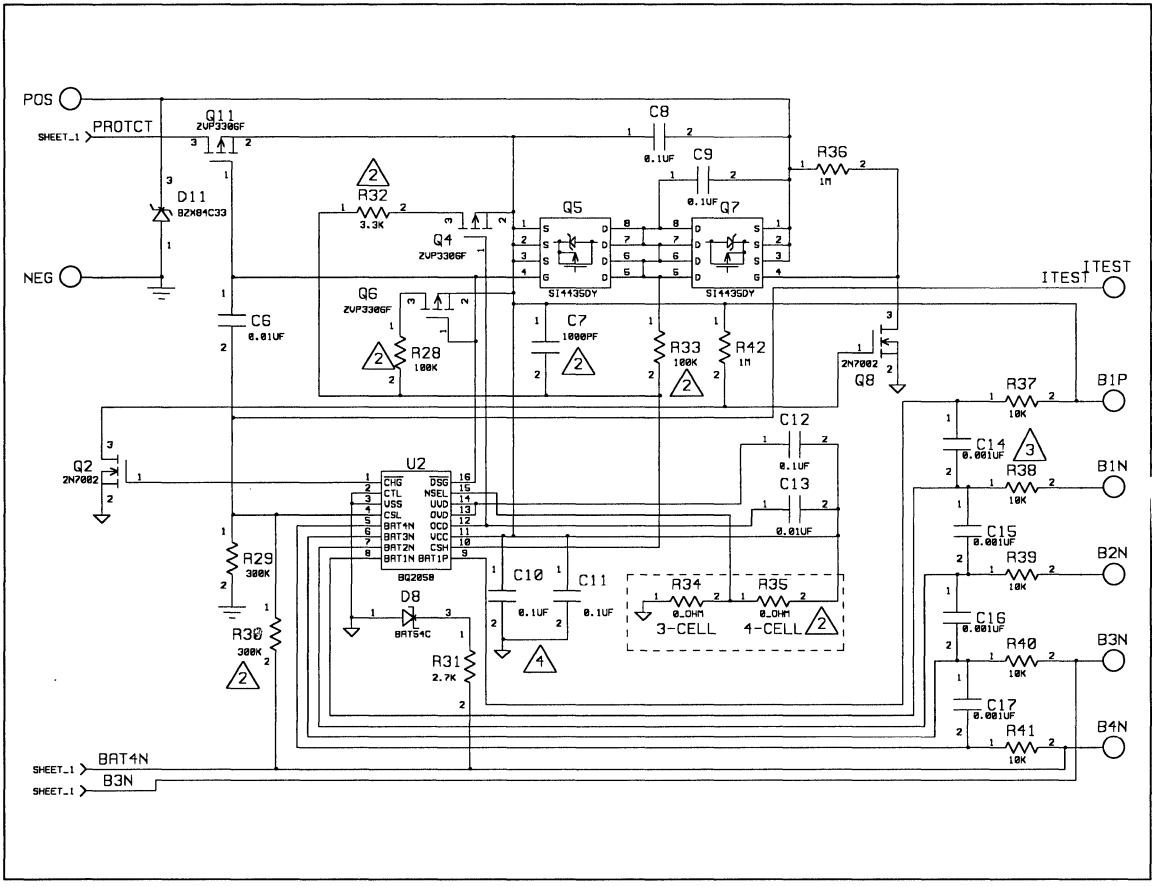
Figure 1. Module Connection Diagram

bq2167 Schematic

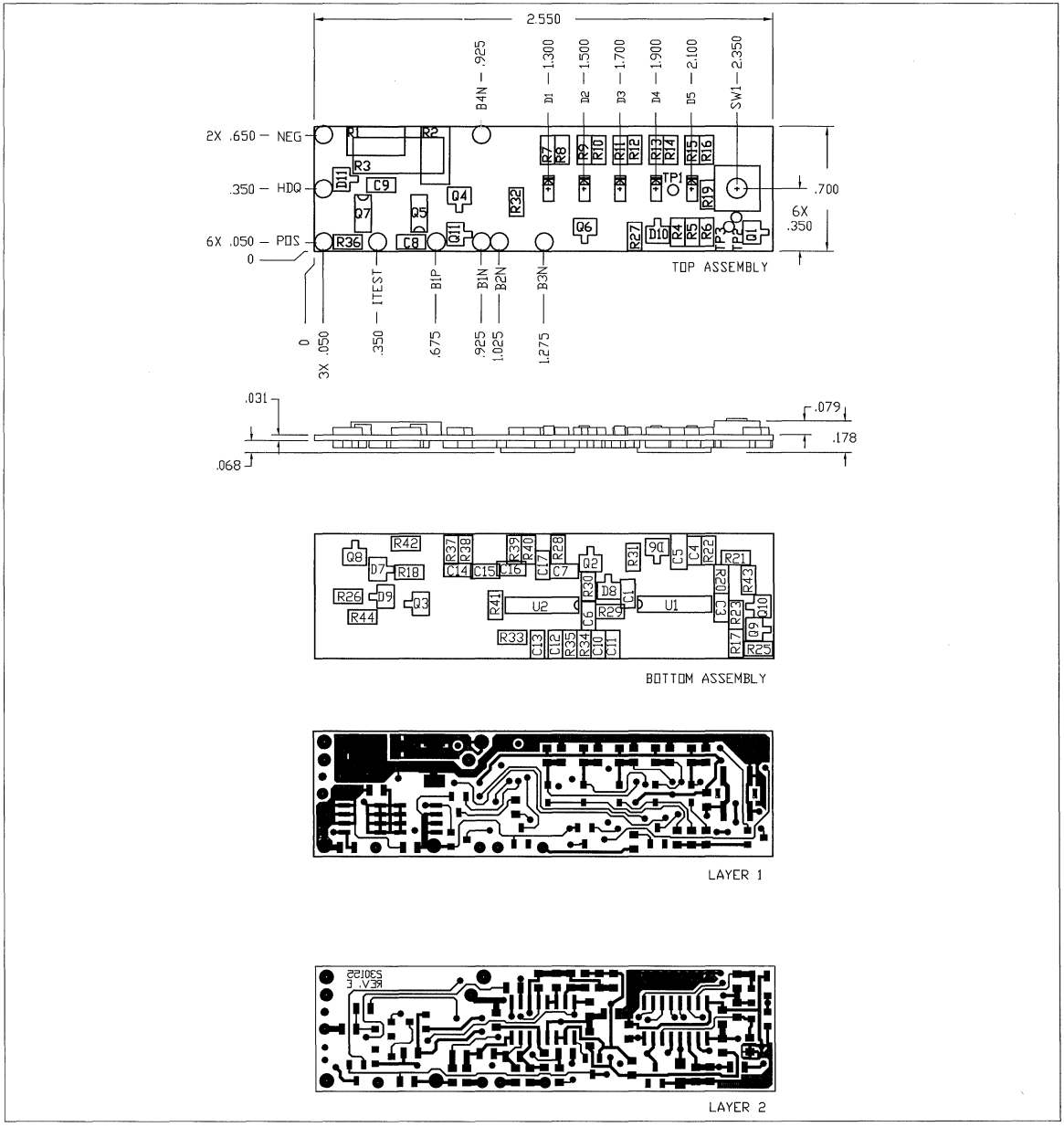


1 2 3 4 Component values depend on user-provided information in Table 1.

bq2167 Schematic (Continued)



bq2167 Board



Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{OP}	Supply voltage (B1P to B4N)	18	V	DC
V_{TR}	Maximum transient voltage (B1P to B4N)	32	V	Maximum duration = 1.5µs
V_{CHG}	Charging voltage (POS to NEG)	18	V	
I_{CHG}	Continuous charge/discharge current	3.9	A	V_{OP} > 6V T_A = 25°C
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-55 to +125	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
V_{OP}	Operating voltage, B1P to B4N	4.0	-	18	V	
I_{CCA}	Operating current	-	-	350	µA	
R_{ON}	On resistance, B1P to POS	-	-	50	mΩ	T_A = 25°C V_{OP} = 10V

DC Thresholds ($T_A = T_{OPR}$)

Symbol	Parameter	Value	Tolerance	Unit	Notes
V_{OV}	Overvoltage threshold	4.25	± 50mV	V	
V_{CE}	Charge enable voltage	V_{OV} - 100mV	± 50mV	V	
V_{UV}	Undervoltage limit	2.25	± 100mV	V	
I_{OC}	Overcurrent limit	3.4		A	T_A = 25°C
		3.8		A	T_A = 60°C
t_{UVD}	Undervoltage delay	950	±50%	ms	T_A = 30°C
V_{CD}	Charge detect threshold	70	-60, +80	mV	
t_{OVD}	Overvoltage delay	950	±50%	ms	T_A = 30°C
t_{OCD}	Overcurrent delay	12	±60%	ms	T_A = 30°C

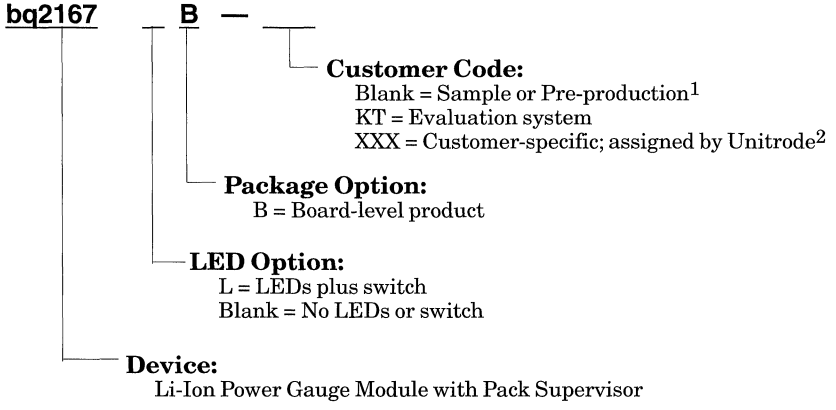
Note: The thresholds above reflect the operation of a bq2158 using the standard bq2058 IC (V_{OV} = 4.25V). Specify other versions of the bq2058 by indicating the appropriate V_{OV} threshold in Table 1.

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	All	From Preliminary to Final	

Note: Change 1 = May 1999 B changes from Apr. 1999.

Ordering Information



Notes: 1. Requires configuration sheet (Table 1)

8/8

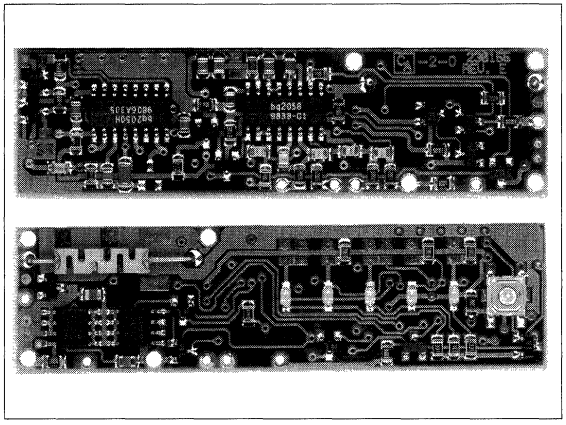
UNITRODE

bq2168

Li-Ion Power Gauge™ Module with Pack Supervisor

Features

- Complete and compact lithium ion gas gauge and protection solution for three or four series cells
- Accurate measurement of available battery capacity
- Provides overvoltage, undervoltage, and overcurrent protection
- Designed for battery pack integration
  - Small size
  - Includes bq2050H and bq2058 ICs
  - On-board charge and discharge control FETs
  - Low operating current for minimal battery drain
- High side FET control
- Battery capacity available through single-wire serial port
- "L" version includes 5 push-button activated LEDs to display state-of-charge information



General Description

The bq2168 Power Gauge Module provides a complete and compact battery management solution for Li-Ion battery packs. Designed for battery pack integration, the bq2168 combines the bq2050H Power Gauge IC with the bq2058 Supervisor IC on a small printed circuit board. The board includes all the necessary components to accurately monitor battery capacity and protect the cells from overvoltage, undervoltage, and overcurrent conditions. The board works with three or four Li-Ion series cells.

The Power Gauge IC uses the on-board sense resistor to track charge and discharge activity of the battery pack. Critical battery information can be accessed through the serial communications port at HDQ. The supervisor circuit consists of the bq2058 and two FETs. The bq2058 controls the FETs to protect the batteries during charge/discharge cycles and short circuit conditions. The bq2168 provides contacts for the positive and negative terminals of each battery in the stack. Please refer to the bq2050H and bq2058 data sheets for the specifics on the operation of the power gauge and supervisor ICs.

Unitrode configures the bq2168 based on the information requested in Table 1. The configuration defines the number of series cells, the nominal battery pack capacity, the self-discharge rate, the Li-Ion battery type (coke or graphite anode), and the threshold limits. Figure 1 shows how the module connects to the cells.

The bq2168L includes five LEDs to display remaining capacity in 20% increments of the learned capacity. The LEDs are activated with the onboard push-button switch.

A module development kit is also available for the bq2168. The bq2168B-KT or the bq2168LB-KT includes one configured module and the following:

1) An EV2200-50H interface board that allows connection to the serial port of any AT-compatible computer.
2) Menu driven software to display charge/discharge activity and to allow user interface to the bq2050H from any standard Windows 3.1x or 95 PC.

Pin Descriptions

POS	**Pack positive**
B1P	**BAT_{1P}/Battery 1 positive input**
B1N	**BAT_{1N}/Battery 1 negative input**
B2N	**BAT_{2N}/Battery 2 negative input**
B3N	**BAT_{3N}/Battery 3 negative input**
B4N	**BAT_{4N}/Battery 4 negative input**
ITEST	**Overcurrent test input**
HDQ	**Serial communications port**
NEG	**Pack negative**

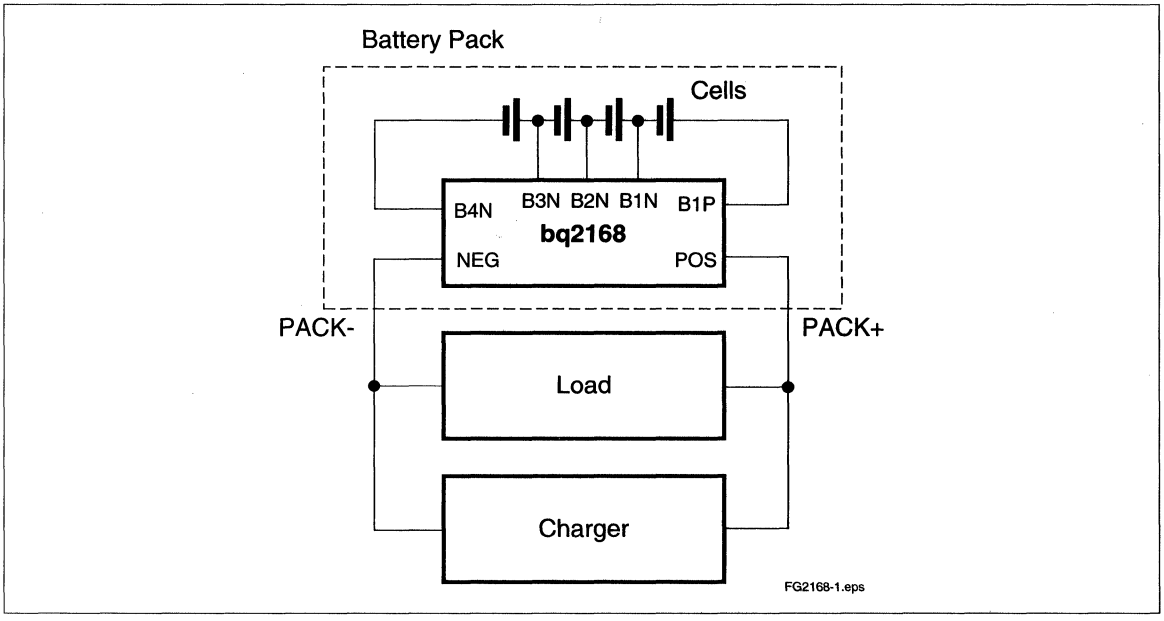


Figure 1. Module Connection Diagram

Table 1. bq2168 Module Configuration

Customer Name: _____

Contact: _____ Phone: _____

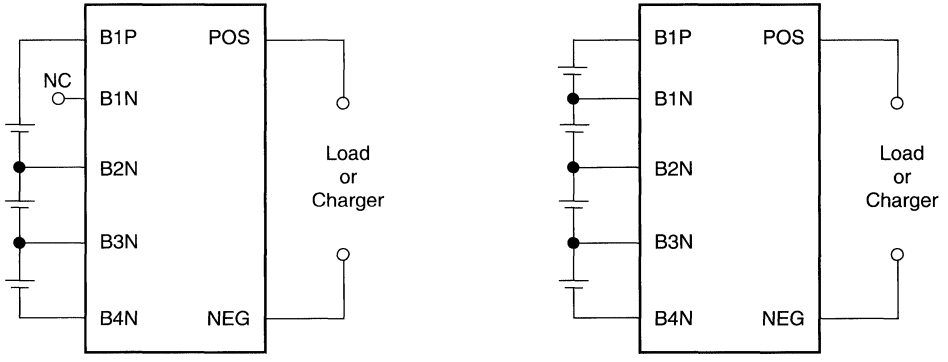
Address: _____

_____

Sales Contact: _____ Phone: _____

Number of series cells (3 or 4)	_____
Coke or graphite cell anode	_____
Battery pack capacity (mAh)	_____
Discharge current into load (3.9A max.)	min. _____ avg. _____ max. _____
Charge current (3.9A max)	_____
Self-discharge compensation (Y/N)	_____
Overvoltage threshold (4.25, 4.30, or 4.35V)	_____
LEDs and switch (Y/N)	_____

FAE approval: _____ Date: _____



Note: B1P, B4N, POS, and NEG accomodate a #20 AWG stranded wire.
B1N, B2N, and B3N accomodate a #24 AWG stranded wire.

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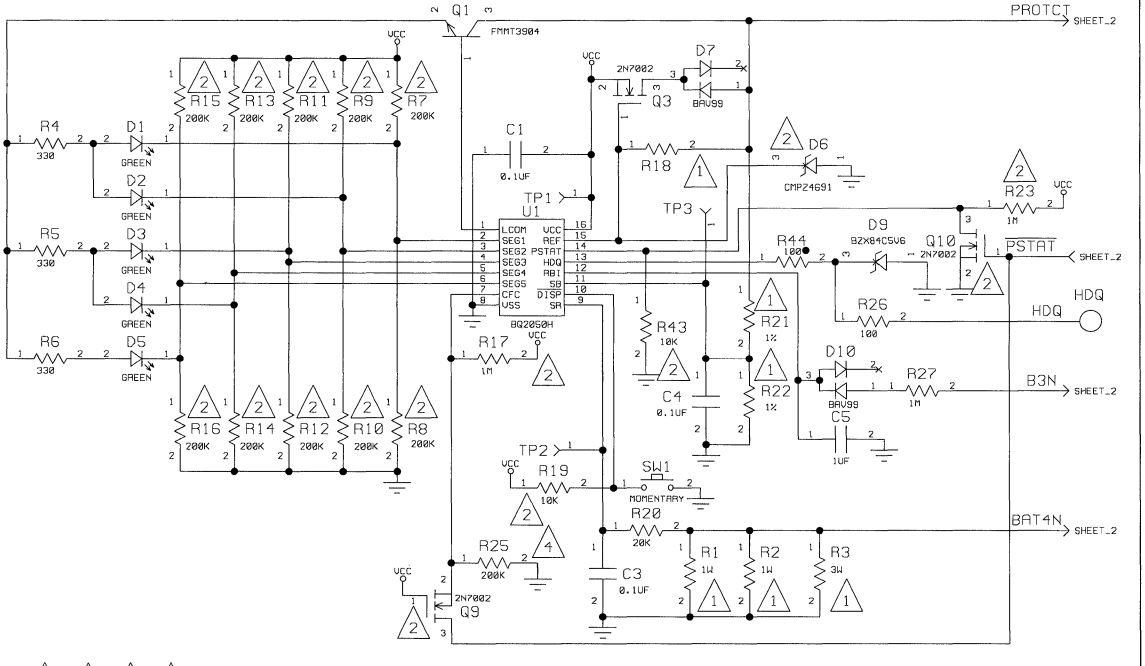
Figure 1. Module Connection Diagram

bq2168 Schematic



1 2 3 4 Component values depend on user-provided information in Table 1.

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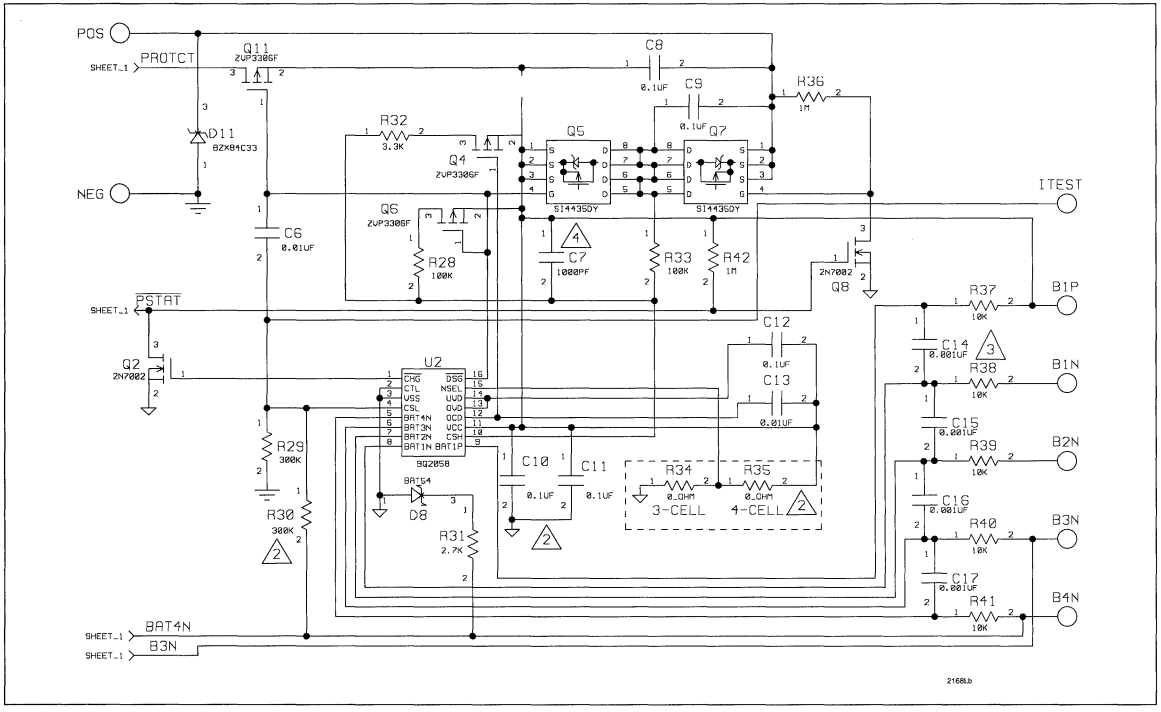
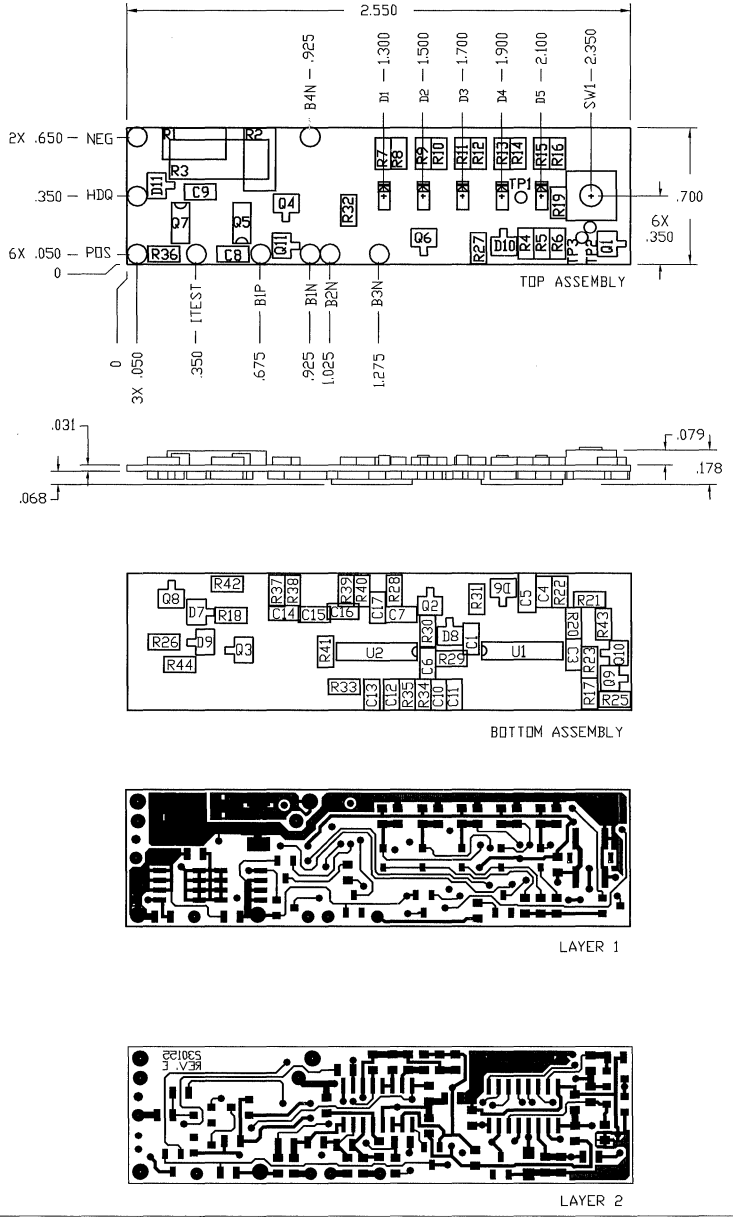
bq2168 Schematic (Continued)



bq2168 Board



Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{OP}	Supply voltage (B1P to B4N)	18	V	DC
V_{TR}	Maximum transient voltage (B1P to B4N)	32	V	Maximum duration = 1.5µs
V_{CHG}	Charging voltage (POS to NEG)	18	V	
I_{CHG}	Continuous charge/discharge current	3.9	A	V_{OP} > 6V T_A = 25°C
T_{OPR}	Operating temperature	0 to +70	°C	
T_{STG}	Storage temperature	-55 to +125	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
V_{OP}	Operating voltage, B1P to B4N	4.0	-	18	V	
I_{CCA}	Operating current	-	-	350	µA	
R_{ON}	On resistance, B1P to POS	-	-	50	mΩ	T_A = 25°C V_{OP} = 10V

DC Thresholds ($T_A = T_{OPR}$)

Symbol	Parameter	Value	Tolerance	Unit	Notes
V_{OV}	Overvoltage threshold	4.25	± 50mV	V	
V_{CE}	Charge enable voltage	V_{OV} - 100mV	± 50mV	V	
V_{UV}	Undervoltage limit	2.25	± 100mV	V	
I_{OC}	Overcurrent limit	3.4		A	T_A = 25°C
		3.8		A	T_A = 60°C
t_{UVD}	Undervoltage delay	950	±50%	ms	T_A = 30°C
V_{CD}	Charge detect threshold	70	-60, +80	mV	
t_{OVD}	Overvoltage delay	950	±50%	ms	T_A = 30°C
t_{OCD}	Overcurrent delay	12	±60%	ms	T_A = 30°C

Note: The thresholds above reflect the operation of a bq2158 using the standard bq2058 IC (V_{OV} = 4.25V). Specify other versions of the bq2058 by indicating the appropriate V_{OV} threshold in Table 1.

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	All	From Preliminary to Final	

Note: Change 1 = May 1999 B changes from Apr. 1999.

Ordering Information

bq2168 **B** — ____

Customer Code:
Blank = Sample or Pre-production[1]
KT = Evaluation system
XXX = Customer-specific; assigned by Unitrode[2]

Package Option:
B = Board-level product

LED Option:
L = LEDs plus switch
Blank = No LEDs or switch

Device:
Li-Ion Power Gauge Module with Pack Supervisor

Notes:
1. Requires configuration sheet (Table 1)
2. Example production part number: bq2168LB-001

8/8

Preliminary bq219XL

Smart Battery Module with LEDs

Features

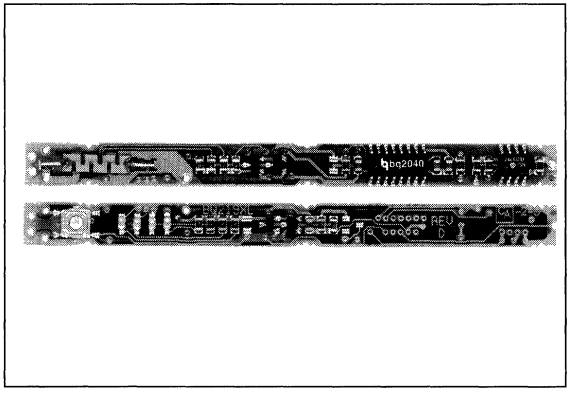
- Complete smart battery solution for NiCd, NiMH, and Li-Ion battery packs
- Based on the bq2092 or bq2040 Gas Gauge IC
- Ideal for DR35 or DR36 type packs
- Narrow board fits in the crevice formed by two adjacent battery packs
- Accurate measurement of available battery capacity
- Designed for battery pack integration:
  - Measures only 3.5 (L) x 0.3 (W) inches
  - Includes Gas Gauge IC, configuration EEPROM, and sense resistor
  - Four onboard state-of-charge LEDs with push-button activation
  - Low operating current for minimal battery drain
- Critical battery information available over two-wire serial port

General Description

The bq219XL Smart Battery Module provides a complete solution for the design of intelligent battery packs. The bq219XL uses the SMBus protocol and supports the Smart Battery Data commands in the SMB/SBD specifications. Designed for battery pack integration, the bq219XL combines the bq2092 or bq2040 Gas Gauge IC with a serial EEPROM on a small printed circuit board. The board includes all the necessary components to accurately monitor battery capacity and communicate critical battery parameters to the host system or battery charger. The bq219XL also includes four LEDs. The push-button switch activates the LEDs to show remaining battery capacity in 25% increments.

Contacts are provided on the bq219XL for direct connection to the battery stack (B+, B-) and the two-wire interface (C, D). Please refer to the bq2092 or bq2040 data sheet for specific information on the operation of the Gas Gauge and communication interface.

Unitrode configures the bq219XL based on the information requested in Table 1. The configuration defines the pack voltage, capacity, and chemistry and charge control



parameters. The Smart Battery Module uses the onboard sense resistor to track charge and discharge activity of the battery pack. Figure 1 shows how the module connects to the cells.

A module development kit is also available for the bq219XL. The bq219XLB-KT includes one configured module and the following:

1) An EV2200-92 or EV2200-40 interface board that allows connection to the serial port of any AT-compatible computer.
2) Menu-driven software to display charge/discharge activity and to allow user interface to the Gas Gauge IC and serial E^2PROM from any standard Windows 95 or 3.1x PC.

Pin Descriptions

B+	**BAT+/Battery positive/Pack positive**
P-	**PACK-/Pack negative**
C	**SMBC/Communications clock**
D	**SMBD/Serial data**
B-	**BAT-/Battery negative**
STAT	**STAT/No connect**

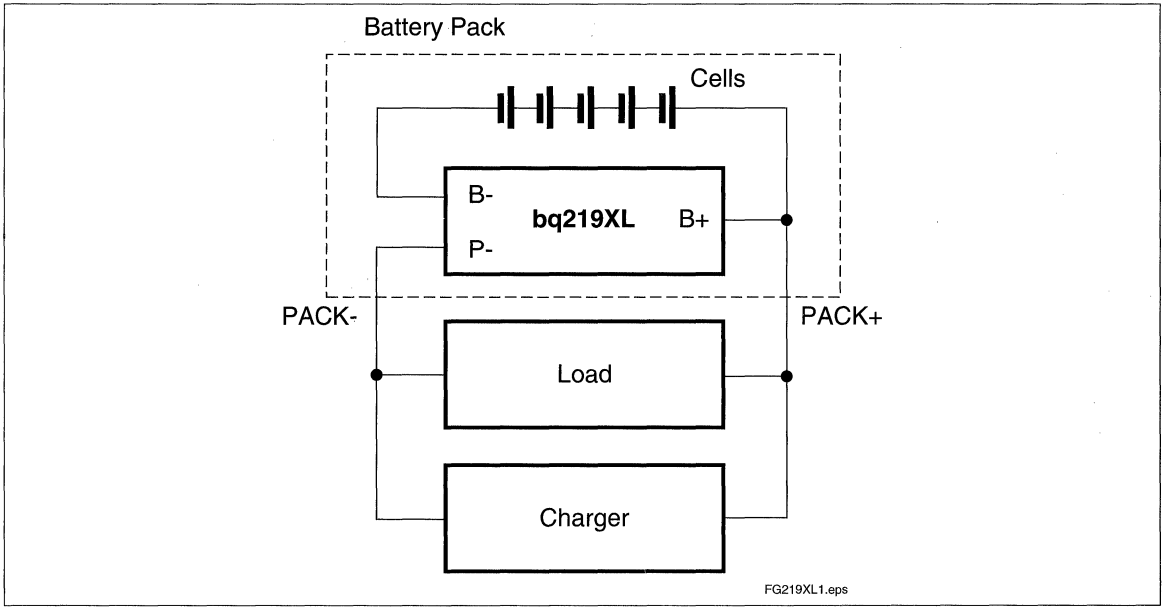


Figure 1. Module Connection Diagram

Table 1. bq219XL Module Configuration

Customer Name: _____

Contact: _____ Phone: _____

Address: _____

Sales Contact: _____ Phone: _____

Board Configuration

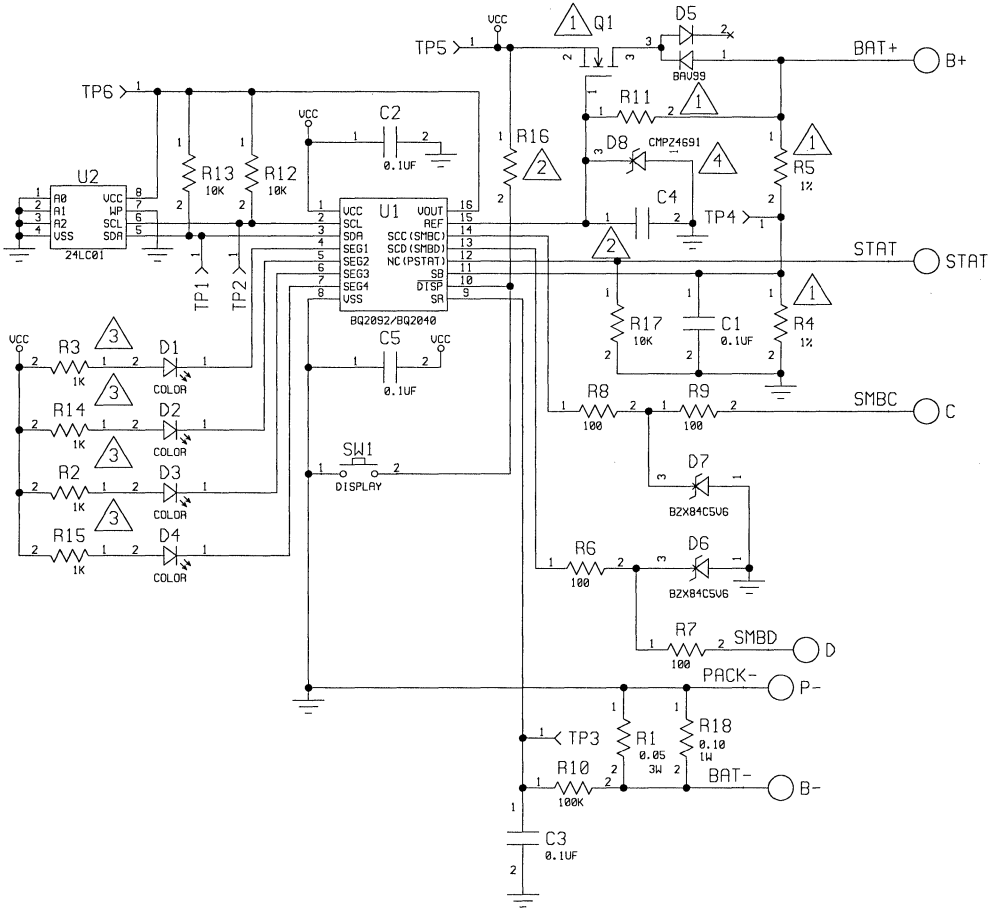
IC type	_____	bq2040 or bq2092
LEDs and switch	_____	Yes or No
Display mode	_____	Relative or Absolute
Discharge rate (3.0A max.)	Min _____	Avg _____ Max _____
Duration at max. discharge	_____	
Number of series cells	_____	

EEPROM Configuration

			Typical Values NiMH	Typical Values Li-Ion
Remaining time alarm (min)	_____	Sets the low time alarm level	10 min	10 min
Remaining capacity alarm (mAh)	_____	Sets the low capacity alarm level	C/10	C/10
Charging voltage (mV)	_____	Sets the requested charging voltage	65535	4.1V/cell
Design cpaacity (mAh)	_____	Defines the battery pack capacity	3000	3600
Design voltage (mV)	_____	Defines the battery pack voltage	12000	10800
Manufacturer date	_____	Battery pack manufacturer date	mm/dd/yy	mm/dd/yy
Serial number	_____	Battery pack serial number	0-65535	0-65535
Fast-charging current (mA)	_____	Sets the requested charging current	1C	1C
Maintenance charging current (mA)	_____	Sets the requested maintenance charging current	C/20	0
Li-Ion taper current (mA)	_____	Sets the upper limit for charge termination	NA	C/10
Maximum overcharge (mAh)	_____	Sets the maximum amount of overcharge	256mAh	128mAh
Maximum temperature (°C)	_____	Sets the maximum charge temperature	61°C	61°C
$\Delta T/\Delta t$ (°C/min)	_____	Sets the termination rate	3°C/3min	4.6°C/20s
Fast-charge efficiency (%)	_____	Sets the fast-charge efficiency factor	95%	100%
Maintenance charge efficiency (%)	_____	Sets the maintence charge efficiency factor	80%	100%
Self-discharge rate (%/day)	_____	Sets the batterys self-discharge rate	1.5%/day	0.2%/day
EDV1 (mV)	_____	Sets the initial end-of-discharge warning	1.05V/cell	3.0V/cell
EDVF (mV)	_____	Sets the final end-of-discharge warning	1.0V/cell	2.8V/cell
Hold-off timer for $\Delta T/\Delta t$ (sec.)	_____	Sets the hold off period for $\Delta T/\Delta t$ termination	180s	320s
Manufacturer name	_____	Programs manufacturer's name (11 char. max)	bq	bq
Device name	_____	Programs device name (7 char. max)	bq36	bq202
Chemistry	_____	Programs pack's chemistry (5 char. max)	NiMH	LION
Manufacturer data	_____	Open field (5 char. max)	2040	2040
FAE Approval:	_____	Date: _____		

3/6

bq219XL Schematic



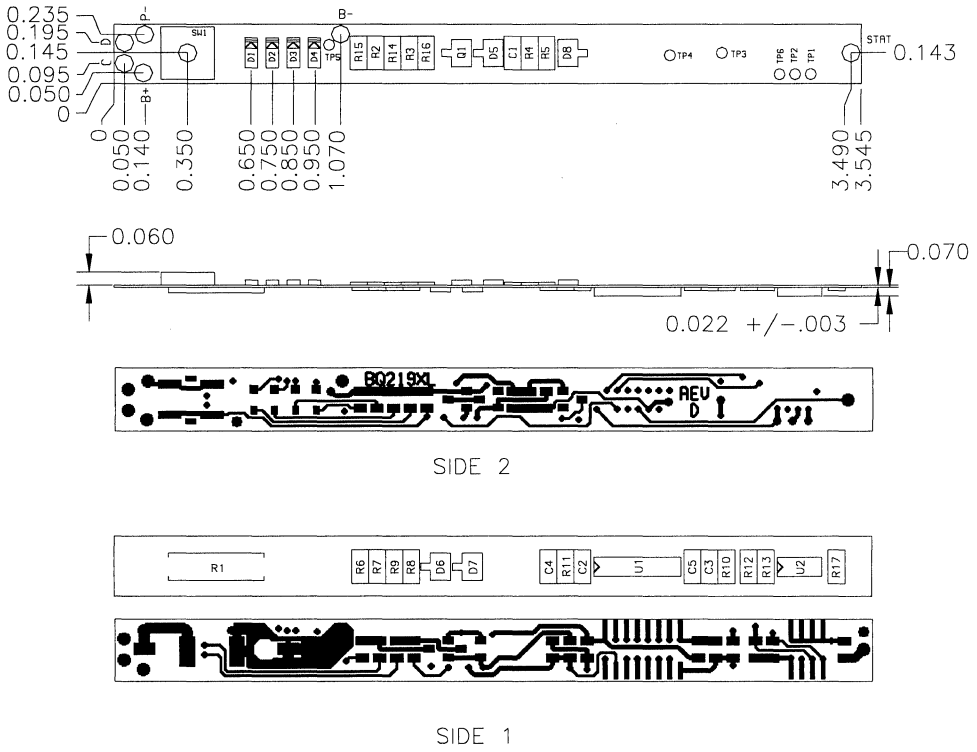
1. SEE CHART 1 FOR BQ2040 DEVICE VALUES. FOR BQ2092 CONSULT APPLICATIONS DEPT.
2. CUSTOMER SPECIFIED OPTION.
3. R2,R3,R14 AND R15 ARE 330 OHM FOR BQ2092
4. D8 IS REQUIRED FOR BQ2092. D8 MAY BE REQUIRED FOR BQ2040 OUTSIDE CELL COUNT RANGE SHOWN IN CHART 1.

CHART 1
FOR BQ2040 WITH NO D8

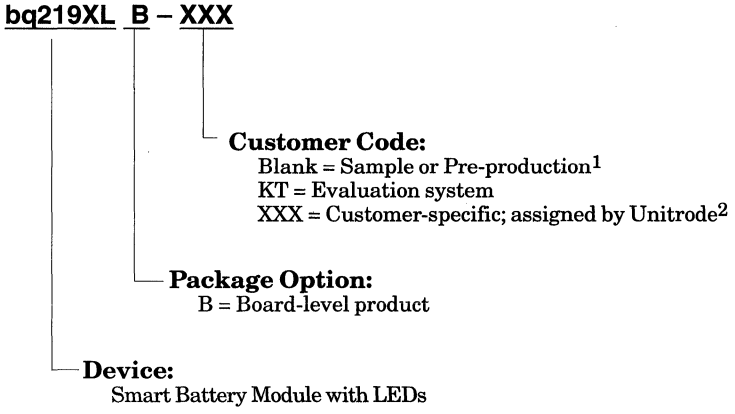
	# OF CELLS	R5	R11	R4	Q1
LiION	2	301K	86.6K	100K	BSS138
	3	499K	909K	100K	2N7002
	4	698K	909K	100K	2N7002
NiMH	6	499K	162K	100K	BSS138
	8	698K	402K	100K	2N7002
	9	806K	604K	100K	2N7002
	10	909K	909K	100K	2N7002
	12	909K	1M	86.6K	2N7002

219xlb

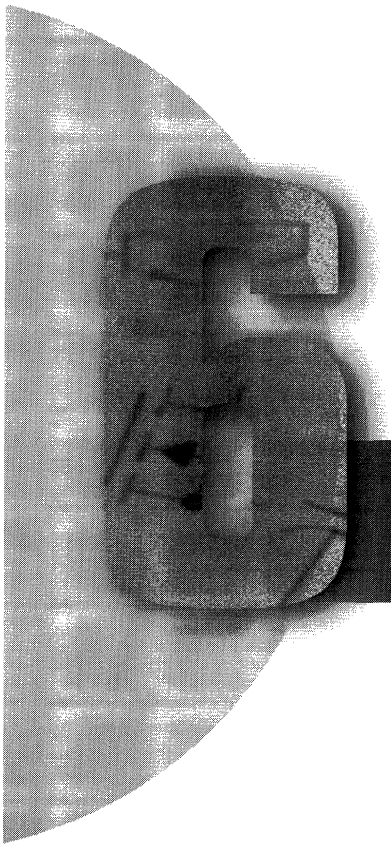
bq219XL Board



Ordering Information



Notes:
1. Requires configuration sheet (see Table 1)
2. Example production part number: bq219XLB-001



Pack-Protection and Supervisory ICs

Pack-Protection and Supervisory ICs Selection Guide

Unitrode Lithium Ion Pack-Protection ICs provide reversible overvoltage, undervoltage, and overcurrent protection for lithium ion battery packs.

- ➤ Protects one to four Lithium Ion series cells from overvoltage, undervoltage, and overcurrent
- ➤ User-selectable thresholds mask-programmable by Unitrode
- ➤ Designed for battery-pack integration
  - – Small outline package, minimal external components and space, and low cost

Battery Technology	Number of Cells Protected	Protection Types	Key Features	Pins / Package	Part Number	Page Number
Lithium Ion	3 or 4	Overvoltage, overcurrent, and undervoltage	Very low power	16/0.150" SOIC	bq2058	6-2
	2				bq2058T	6-14
		Overcharge, overdischarge, overcurrent	Internal MOSFET (80mΩ total)		UCC3911	6-26
	1		Internal MOSFET (50mΩ total)	16/0.150" TSSOP	UCC3952+	6-32
	3 or 4	Overvoltage, undervoltage, overcurrent	Smart-discharge circuitry	16/0.150" SSOP	UCC3957	6-37
	1	Overcharge, overdischarge, overcurrent	Internal MOSFETS (50mΩ total)	16/0.150" SOIC	UCC3958	6-44

+ New Product

UNITRODE

bq2058

Lithium Ion Pack Supervisor for 3- and 4-Cell Packs

Features

- Protects and individually monitors three or four Li-Ion series cells for overvoltage, undervoltage
- Monitors pack for overcurrent
- Designed for battery pack integration
- Minimal external components
- Drives external FET switches
- Selectable overvoltage (V_{OV}) thresholds
  - Mask-programmable by Unitrode
  - Standard version–4.25V
- Supply current: 25µA typical
- Sleep current: 0.7µA typical
- 16-pin 150-mil narrow SOIC

General Description

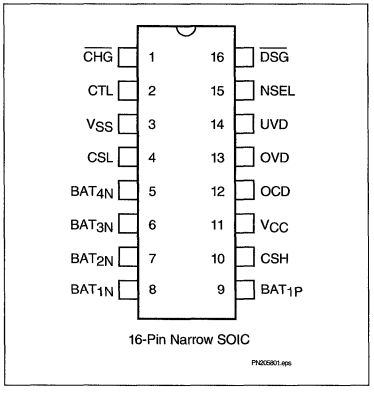
The bq2058 Lithium Ion Pack Supervisor is designed to control the charge and discharge cell voltages for three or four lithium ion (Li-Ion) series cells, accommodating battery packs containing series/parallel configurations. The low operating current does not overdischarge the cells during periods of storage and does not significantly increase the system discharge load. The bq2058 can be part of a low-cost Li-Ion charge control system within the battery pack.

The bq2058 controls two external FETs to limit the charge and discharge potentials. The bq2058 allows charging when each individual cell voltage is below V_{OV} (overvoltage limit). If the voltage on any cell exceeds V_{OV} for a user-configurable delay period (t_{OVD}), the $\overline{CHG}$ pin is driven high, shutting off charge to the battery pack. This safety feature prevents overcharge of any cell within the battery pack. After an overvoltage condition occurs, each cell must fall below V_{CE} (charge enable voltage) for the bq2058 to re-enable charging.

The bq2058 protects batteries from overdischarge. If the voltage on any cell falls below V_{UV} (undervoltage limit) for a user-configurable delay period (t_{UVD}), the $\overline{DSG}$ output is driven high, shutting off the battery discharge. This safety feature prevents overdischarge of any cell within the battery pack.

The bq2058 also stops discharge on detection of an overcurrent condition, such as a short circuit. If an overcurrent condition occurs for a user-configurable delay period (t_{OCD}), the $\overline{DSG}$ output is driven high, disconnecting the load from the pack. $\overline{DSG}$ remains high until removal of the short circuit or overcurrent condition.

Pin Connections



16-Pin Narrow SOIC

PN2058D1.eps

Pin Names

$\overline{CHG}$	Charge control output
CTL	Pack disable input
V_{SS}	Low potential input
CSL	Current sense low-side input
BAT_{4N}	Battery 4 negative input
BAT_{3N}	Battery 3 negative input
BAT_{2N}	Battery 2 negative input
BAT_{1N}	Battery 1 negative input
$\overline{DSG}$	Discharge control output
NSEL	3- or 4-cell selection
UVD	Undervoltage delay input
OVD	Overvoltage delay input
OCD	Overcurrent delay input
V_{CC}	High potential input
CSH	Current sense high-side input
BAT_{1P}	Battery 1 positive input

Pin Descriptions

$\overline{CHG}$ Charge control output

This push-pull output controls the charge path to the battery pack. Charging is allowed when low.

CTL Pack disable input

When high, this input allows an external source to disable the pack by making both $\overline{DSG}$ and $\overline{CHG}$ inactive. For normal operation, the CTL pin is low.

V_{SS} Low potential input

CSL Overcurrent sense low-side input

This input is connected between the low-side discharge FET (or sense resistor) and BAT_{4N} to enable overcurrent sensing in the battery pack's ground path.

BAT_{4N} Battery 4 negative input

This input is connected to the negative terminal of the cell designated BAT4 in Figure 2.

BAT_{3N} Battery 3 negative input

This input is connected to the negative terminal of the cell designated BAT3 in Figure 2.

BAT_{2N} Battery 2 negative input

This input is connected to the negative terminal of the cell designated BAT2 in Figure 2.

BAT_{1N} Battery 1 negative input

This input is connected to the negative terminal of the cell designated BAT1 in Figure 2. This input is connected to BAT_{1P} in a three-cell configuration.

$\overline{DSG}$ Discharge control output

This push-pull output controls the discharge path to the battery pack. Discharge is allowed when low.

NSEL Number of cells input

This input selects the number of series cells in the pack. NSEL should connect to V_{CC} for four cells and to V_{SS} for three cells.

UVD Undervoltage delay input

This input uses an external capacitor to V_{CC} to set the undervoltage delay timing.

OVD Overvoltage delay input

This input uses an external capacitor to V_{CC} to set the overvoltage delay timing.

OCD Overcurrent delay input

This input uses an external capacitor to V_{CC} to set the overcurrent delay timing.

V_{CC} High potential input

CSH Overcurrent sense high-side input

This input is connected between the high-side discharge FET (or sense resistor) and BAT_{1P} to enable overcurrent sense in the battery pack's positive supply path.

BAT_{1P} Battery 1 positive input

This input is connected to the positive terminal of the cell designated BAT1 in Figure 2.

Table 1. Pin Configuration for 3- and 4-Series Cells

Number of Cells	Configuration Pins	Battery Pins
3 cells	BAT_{1N} tied to BAT_{1P} NSEL = V_{SS}	BAT_{1N} – Positive terminal of first cell
		BAT_{2N} – Negative terminal of first cell
		BAT_{3N} – Negative terminal of second cell
		BAT_{4N} – Negative terminal of third cell
4 cells	NSEL = V_{CC}	BAT_{1P} – Positive terminal of first cell
		BAT_{1N} – Negative terminal of first cell
		BAT_{2N} – Negative terminal of second cell
		BAT_{3N} – Negative terminal of third cell
		BAT_{4N} – Negative terminal of fourth cell

2/12

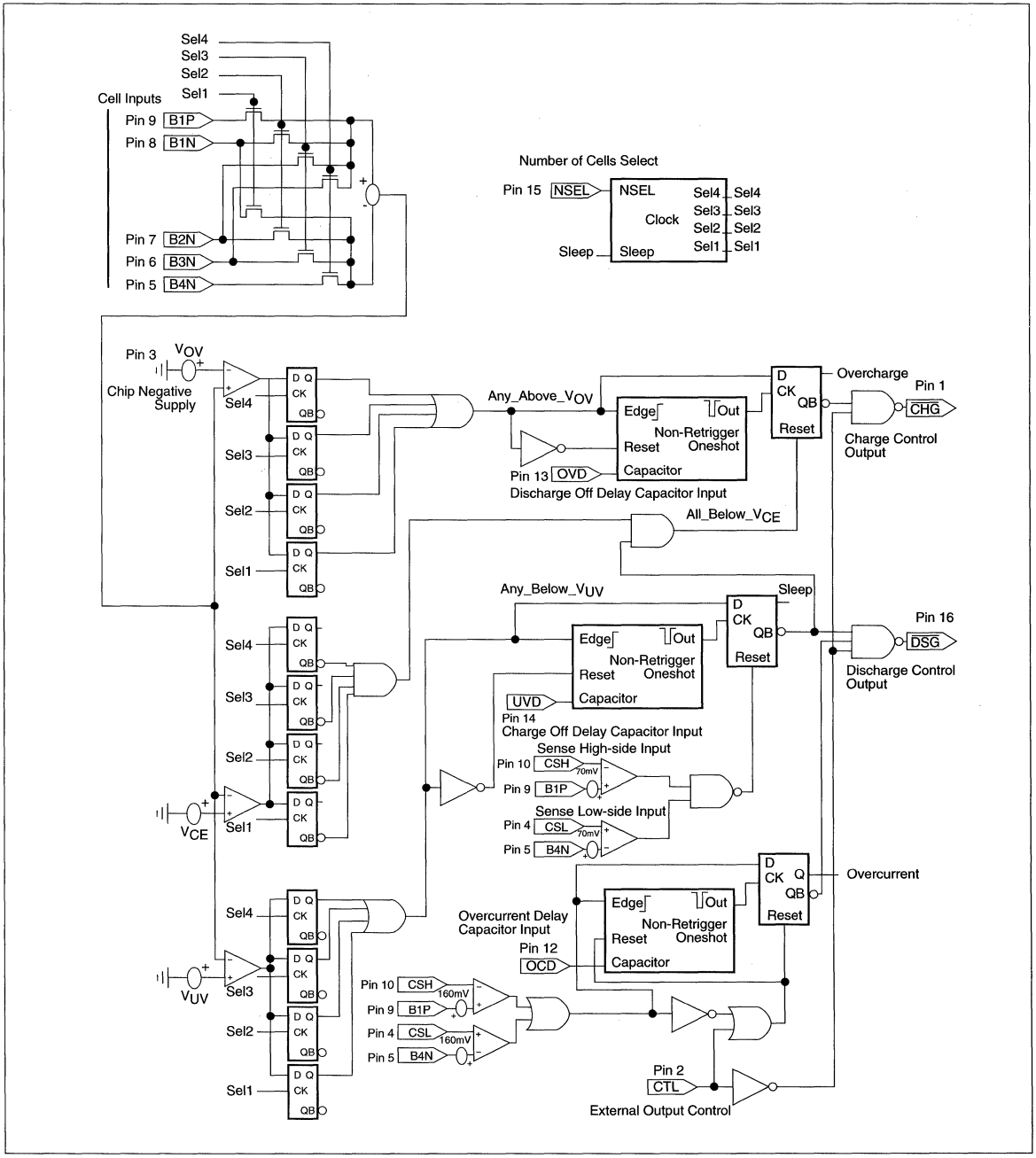


Figure 1. Block Diagram

Functional Description

Figure 1 is a block diagram outlining the major components of the bq2058. Figure 2 shows a 3- or 4-cell pack supervisor circuit. The following sections detail the various functional aspects of the bq2058.

Thresholds

The bq2058 monitors the lithium ion pack for the conditions listed below. Shown with these conditions are the respective thresholds used to determine if that condition exists:

- Overvoltage (V_{OV})
- Undervoltage (V_{UV})
- Overcurrent (V_{OCH}, V_{OCL})
- Charge Enable (V_{CE})
- Charge Detect (V_{CD})

The bq2058 samples a cell every 40ms (typical). Every sample is a fully differential measurement of each cell. During this sample period, the bq2058 compares the measurements with these thresholds to determine if any of the these conditions exist: V_{OV}, V_{UV}, and V_{CE}.

Overcurrent and charge detect are conditions that are not sampled, but are continuously monitored.

Initialization

On initial power-up, such as connecting the battery pack for the first time to the bq2058, the bq2058 enters the low-power sleep mode, disabling the $\overline{DSG}$ output. **It is recommended that a top to bottom cell connection be made at pack assembly for proper initialization.** A charging supply must be applied to the bq2058 circuit to enable the pack. See Low-Power Sleep Mode and Charge Detect sections.

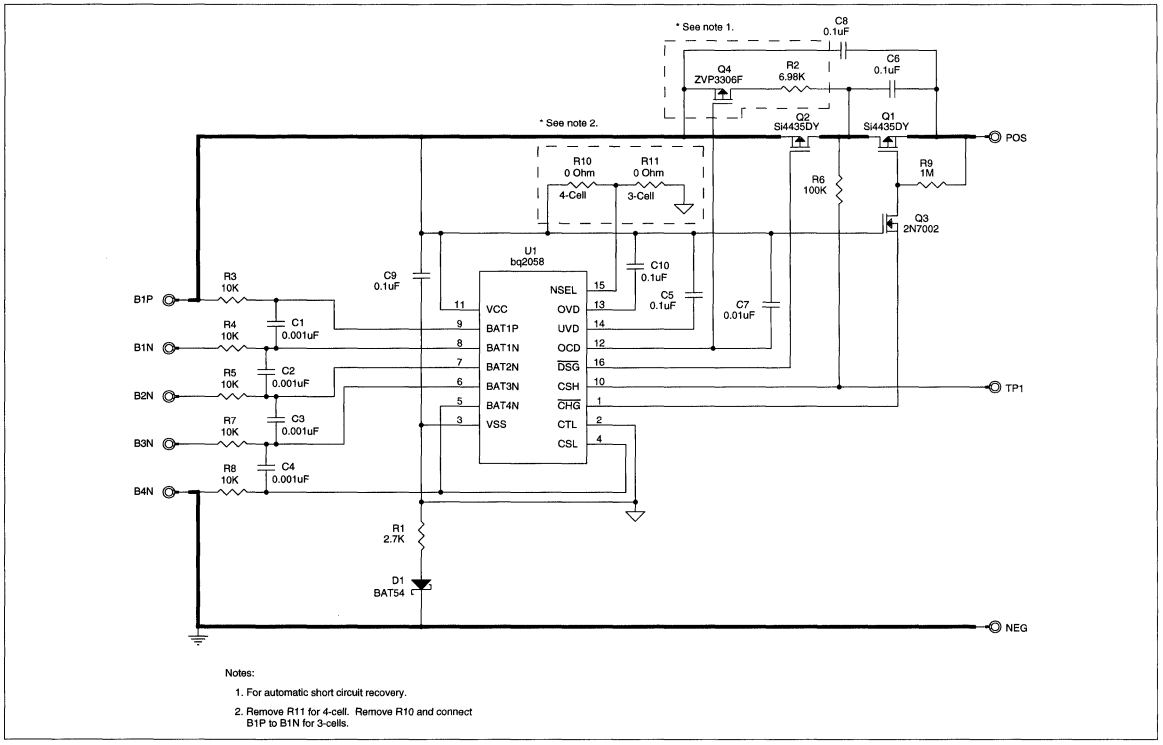


Figure 2. 3- or 4-Cell Li-Ion Battery Pack Supervisor

Low-Power Sleep Mode

The bq2058 enters the low-power sleep mode in two different ways:

1. On initial power-up.
2. After the detection of an undervoltage condition–V_{UV}.

When the bq2058 enters the low-power sleep mode, $\overline{DSG}$ is driven high and the device consumes 0.7µA (typical). The bq2058 only comes out of low-power sleep mode when a valid charge-detect condition exists.

Charge Detect

The bq2058 continuously monitors for a charge-detect condition. A valid charge-detect condition exists when either of the conditions are true:

$$CSL < BAT_{4N} - 70mV\ (V_{CD})$$

$$CSH > BAT_{1P} + 70mV\ (V_{CD})$$

A valid charge-detect enables the $\overline{DSG}$ output, allowing charging of the lithium ion cells. This is accomplished by applying the charging supply to the pack.

Undervoltage

Undervoltage (or overdischarge) protection is asserted when any cell voltage drops below the V_{UV} threshold and remains below the V_{UV} threshold for a time exceeding a user-configurable delay (t_{UVD}). The $\overline{DSG}$ output is driven high disabling the discharge of the pack. The bq2058 then enters the low-power sleep mode.

Overvoltage

Overvoltage (or overcharge) protection is asserted when any cell voltage exceeds the V_{OV} threshold and remains above the V_{OV} threshold for a time exceeding a user-configurable delay (t_{OVD}). The $\overline{CHG}$ pin is driven high, disabling charge into the battery pack. Charging is disabled until a valid charge enable exists. See Charge Enable section.

Important note: If any battery pin floats (BAT_{1P}, BAT_{1N-4N}), the bq2058 assumes an overvoltage has occurred.

Because of different manufacturers specifications for overvoltage thresholds, the bq2058 can be available with different V_{OV} options. Table 2 summarizes these different voltage thresholds.

Table 2. Overvoltage Threshold Options

Part No.	V_{OV} Limit
bq2058	4.25V
bq2058C	4.325
bq2058D	4.30V
bq2058G*	4.375V
bq2058R	4.35V
bq2058W	3.4V

The overvoltage threshold limits are programmed at Unitrode. The bq2058 is the standard option that is more readily available for sampling and prototyping purposes. Please contact Unitrode for other voltage threshold and tolerance options.

Charge Enable

A valid charge enable indicates that an overvoltage (overcharge) condition no longer exists and that the pack is ready to accept further charge. Once overvoltage protection is asserted, charging will not be enabled until all cell voltages fall below V_{CE}. The V_{CE} threshold is a function of V_{OV}, and changes with different V_{OV} limits.

$$V_{CE} = V_{OV} - 150mV$$

Overcurrent

The bq2058 detects an overcurrent (or short circuit) condition only in the discharge direction. Overcurrent protection is asserted when either of the conditions occurs and remain for a time exceeding a user-configurable delay (t_{OCD}):

$$CSL > BAT_{4N} + V_{OCL}$$

$$CSH < BAT_{1P} - V_{OCH}$$

where:

$$V_{OCL} = 160mV\ (\text{low-side detect})$$

$$V_{OCH} = 160mV\ (\text{high-side detect})$$

When either of these conditions occurs, $\overline{DSG}$ is driven high, disconnecting the load from the pack. $\overline{DSG}$ remains high until both of the voltage conditions are false, indicating removal of the short-circuit condition. The user can facilitate clearing these conditions by inserting the battery pack into a charger.

The low-side overcurrent sense can be disabled by connecting CSL to BAT_{4N}. This ensures that CSL is never greater than BAT_{4N}. If low-side detection is disabled, high-side detection must be used with CSH.

The FETs in the charge/discharge path controlled by the $\overline{CHG}$ and $\overline{DSG}$ pins affect the overcurrent level. The on-resistance of these FETs need to be taken into account when determining overcurrent levels.

Condition	$\overline{CHG}$ pin	$\overline{DSG}$ pin
Normal operation	Low	Low
Overvoltage	High	Low
Undervoltage	Low	High
Overcurrent	Low	High
Floating battery input	High	Indeterminate
CTL = high	High	High

$\overline{CHG}$ and $\overline{DSG}$ States

The $\overline{CHG}$ and $\overline{DSG}$ output truth table is shown below.

The polarities of $\overline{CHG}$ and $\overline{DSG}$ are mask programmable at Unitrode. Push-pull vs. open-drain configuration is also mask-configurable at Unitrode. Please contact Unitrode for availability of these variations.

Number of Cells

The user must configure the bq2058 for three- or four-series cell operation. For a three-cell pack, NSEL should be tied directly to V_{SS}. For a four-cell pack, N_{SEL} should be connected directly to V_{CC}.

Number of Series Cells	NSEL
3-cell	Tied to V_{SS}
4-cell	Tied to V_{CC}

Pack Disable Input–CTL

The CTL pin is used to electrically disconnect the battery from the pack terminals through an externally supplied signal. When CTL is taken high, $\overline{CHG}$ and $\overline{DSG}$ are driven high. Any load on the pack terminals will be interpreted as an overcurrent condition by the bq2058 with the overcurrent delay timer held in reset. When the CTL pin is driven low, the overcurrent delay timer is allowed to start. If the programmed delay (t_{OCD}) is too short, the overcurrent recovery circuit, if implemented, will be unable to correct the overcurrent situation prior to the delay time-out. It is recommended that a delay time of greater than 10ms ($C_{OCD} \geq 0.01\mu F$) be used if the CTL pin function is used.

Important note: If CTL floats, it is internally pulled high making both $\overline{DSG}$ and $\overline{CHG}$ inactive, thus disabling the pack. If CTL is not used, it should be tied to V_{SS}.

The polarity of CTL is mask programmable at Unitrode. Please contact Unitrode for other polarity options.

Protection Delay Timers

The delay time between the detection of an overcurrent, overvoltage, or undervoltage condition and the deactivation of the $\overline{CHG}$ and/or $\overline{DSG}$ outputs is user-configurable by the selection of capacitor values between V_{CC} and OCD, OVD, and UVD pins (respectively). See Table 3 below.

The fault condition must persist through the entire delay period, or the bq2058 may not deactivate either FET control output.

Figure 3 shows a step-by-step event cycle for the bq2058.

Table 3. Protection Delay Timers

Protection Feature	Delay Period	Capacitor from V_{CC} to:	Typical		Tolerance
			Capacitor	Time	
Overcurrent	t_{OCD}	OCD	0.010µF	12ms	±40%
Overvoltage	t_{OVD}	OVD	0.100µF	950ms	±40%
Undervoltage	t_{UVD}	UVD	0.100µF	950ms	±40%

Notes:

1. The delay time versus capacitance can be approximated by the following equations:.
   For t_{OCD}: $t_{(s)} \approx 1.2 * C_{(\mu f)}$, where $C \geq 0.001\mu F$
   For t_{OVD}, t_{UVD}: $t_{(s)} \approx 9.5 * C_{(\mu f)}$, where $C \geq 0.01\mu F$
2. Overvoltage and undervoltage conditions are sampled by the bq2058. The delay in Table 2 is in addition to the time required for the bq2058 to detect the violation, which may vary from 0 to 160 ms depending on where in the sampling period the violation occurs. Overcurrent is continuously monitored and is subject to a delay of approximately 1.5ms.

6/12

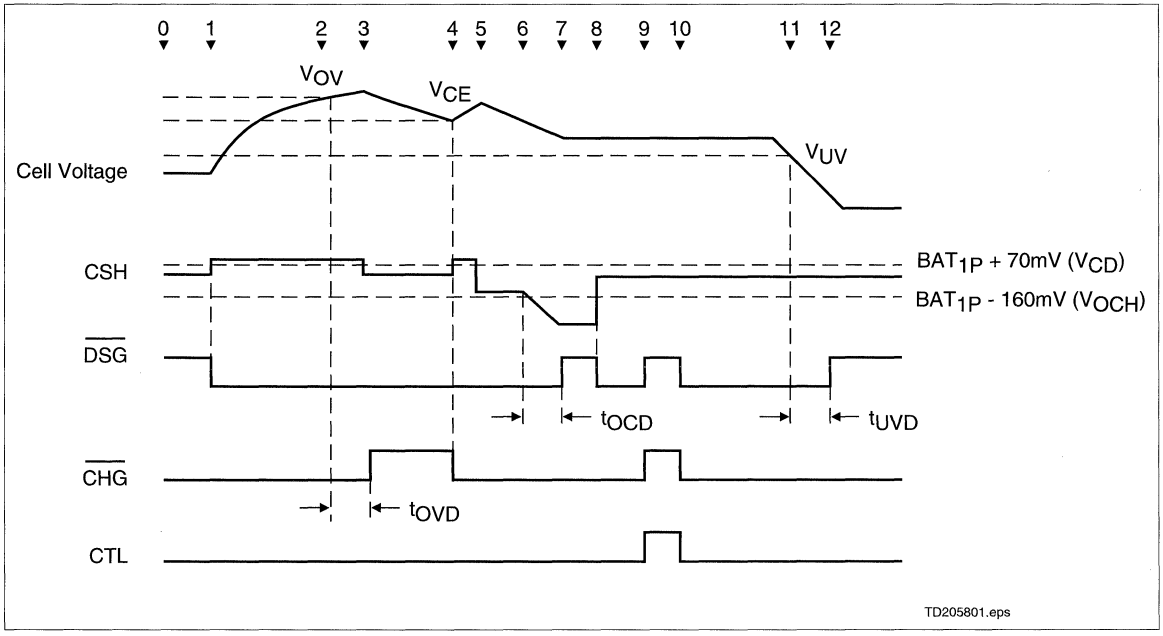


Figure 3. Protector Event Diagram

Event Definition:

0: The bq2058 is in the low-power sleep mode because one or more of the cell voltages are below V_{UV}.

1: A charger is applied to the pack, causing the difference between CSH and BAT_{1P} to become greater than 70mV. This awakens the bq2058, and the discharge pin $\overline{DSG}$ goes low.

2: One or more cells charge to a voltage equal to V_{OV}, initiating the overvoltage delay timer.

3: The overvoltage delay time expires, causing $\overline{CHG}$ to be driven high.

4: All cell voltages fall below V_{CE}, causing $\overline{CHG}$ to be driven low.

5: Stop charging, apply a load.

6: An overcurrent condition is detected, initiating the overcurrent delay timer.

7: The overcurrent delay time expires, causing $\overline{DSG}$ to be driven high.

8: The overcurrent condition is no longer present; $\overline{DSG}$ is driven low.

9: Pin CTL is driven high; both $\overline{DSG}$ and $\overline{CHG}$ are driven high.

10: Pin CTL is driven low; both $\overline{DSG}$ and $\overline{CHG}$ resume their normal function.

11: One or more cells fall below V_{UV}, initiating the overdischarge delay timer.

12: Once the overdischarge delay timer expires, if any of the cells is below V_{UV}, the bq2058 drives $\overline{DSG}$ high and enters the low-power sleep mode.

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	Supply voltage	18	V	Relative to V_{SS}
T_{OPR}	Operating temperature	-30 to +70	°C	
T_{STG}	Storage temperature	-55 to +125	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds
I_{IN}	Maximum input current	±100	µA	All pins except V_{CC}, V_{SS}

Notes:
1 Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

2. Internal protection diodes are in place on every pin relative to V_{CC} and V_{SS}. See Figure 4.

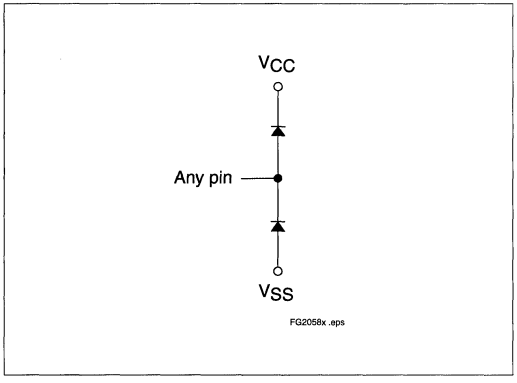


Figure 4. Internal Protection Diodes

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
V_{OH}	Output high voltage	V_{CC} - 0.5	-	-	V	I_{OH} = 10µA, $\overline{CHG}$, $\overline{DSG}$
V_{OL}	Output low voltage	-	-	V_{SS} + 0.5	V	I_{OL} = 10µA, $\overline{CHG}$, $\overline{DSG}$
V_{OP}	Operating voltage	4	-	18.0	V	V_{CC} relative to V_{SS}
V_{IL}	Input low voltage	-	-	V_{SS} + 0.5	V	Pin CTL
V_{IH}	Input high voltage	V_{SS} + 2.0	-	-	V	Pin CTL
V_{IL}	Input low voltage	-	-	V_{SS} + 0.5	V	Pin NSEL
V_{IH}	Input high voltage	V_{CC} - 0.5	-	-	-	Pin NSEL
I_{CCA}	Active current	-	25	40	µA	
I_{CCS}	Sleep current	-	0.7	1.5	µA	

DC Thresholds ($T_A = T_{OPR}$)

Symbol	Parameter	Value	Unit	Tolerance	Conditons
V_{OV}	Overvoltage threshold (See Figure 5)	4.25	V	±50mV	See note 1
		4.375	V	±55mV	For bq2058G only See note 3
		Table 2			Customer option
V_{CE}	Charge enable threshold	V_{OV} - 150mV	V	±50mV	
		V_{OV} - 200mV	V	±50mV	For bq2058W only
V_{UV}	Undervoltage threshold	2.25	V	±100mV	
		2.10	V	±100mV	For bq2058W only
V_{OCH}	Overcurrent detect high-side	160	mV	±35mV	
V_{OCL}	Overcurrent detect low-side	160	mV	±35mV	
V_{CD}	Charge detect threshold	70	mV	-60mV, +80mV	
t_{OVD}	Overvoltage delay threshold	950	ms	±40%	C_{OVD} = 0.100µF, T_A = 30°C See note 2
t_{UVD}	Undervoltage delay threshold	950	ms	±40%	C_{UVD} = 0.100µF, T_A = 30°C See note 2
t_{OCD}	Overcurrent delay threshold	12	ms	±40%	C_{OCD} = 0.01µF, T_A = 30°C

Notes:
1. Standard device. Contact Unitrode for different thresholds and tolerance options.
2. Does not include cell sampling delay, which may add up to 160ms of additional delay until the condition is detected.
3. bq2058G is designed only for 3-cell applications.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
R_{CELL}	Input impedance	-	10	-	MΩ	Pins BAT_{1P}, BAT_{1N-4N}, CSH, CSL

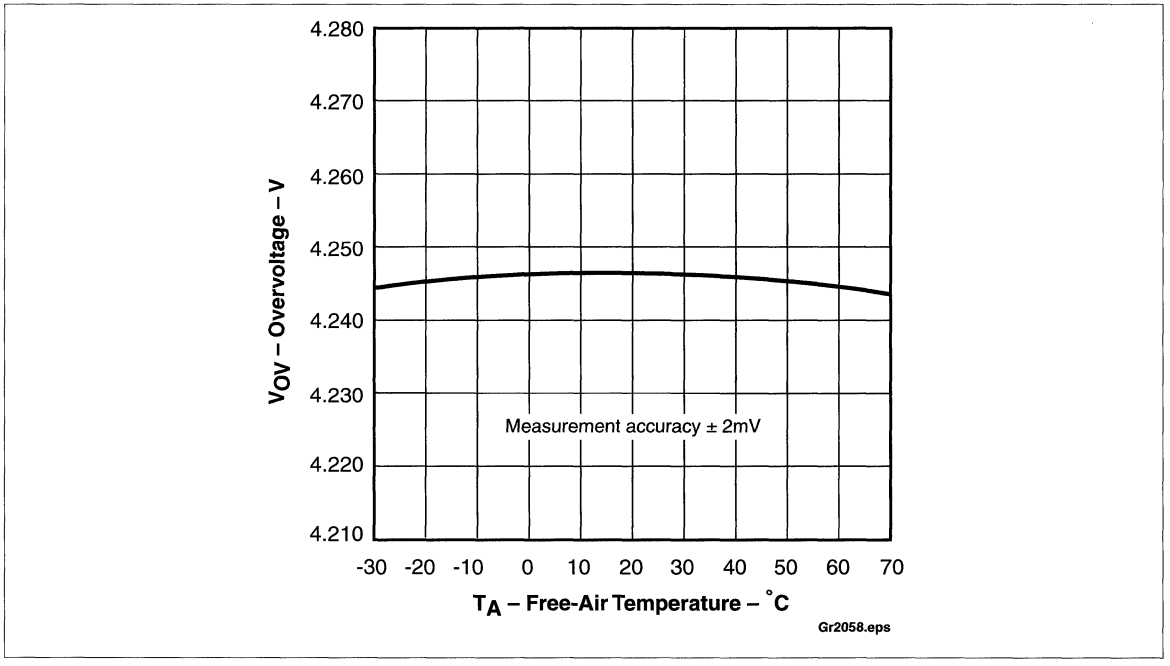


Figure 5. bq2058 4.25V Overvoltage Threshold vs. Free-Air Temperature

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	1, 2, 5	PACK+, PACK-	Pins renamed to CSH and CSL respectively
1	1	Pin description	Added CSH/CSL description
1	3	Block diagram	Update Block diagram
1	4	Figure 2	Update typical application circuit
1	4	Configuration description	Correction to description
1, 2	5	Overcurrent limits	Was: V_{OCH} = 150mV ± 25mV V_{OCL} = 85mV ± 25mV Is: V_{OCH} = 160mV ± 25mV V_{OCL} = 100mV ± 25mV
1	7	Figure 3	Update Event diagram
1, 2	9	DC threshold	Was: V_{OCH} = 150mV ± 25mV V_{OCL} = 100mV ± 80mV V_{CD} = 70mV -60, +50mV Is: V_{OCH} = 160mV ± 25mV V_{OCL} = 100mV ± 25mV V_{CD} = 70mV -60, +80mV
3	1, 3, 5	High-side overcurrent monitored	Was: Between V_{CC} and CSH, Is: Between BAT_{1P} and CSH
3	4	Overvoltage threshold options	Added bq2058R
3	3, 5	Overcurrent limit	Was: V_{OCL} = 100mV, Is: V_{OCL} = 150mV
4	4	Figure 2	Corrected schematic
4	6, 8	Protection Delay Times	Was: t_{OCD} = 10ms ±30% t_{OVD} = 800ms ±30% t_{UVD} = 800ms ±40% Is: t_{OCD} = 12ms ±40% t_{OVD} = 950ms ±40% t_{UVD} = 950ms ±40%
4	10	Overcurrent limits	Was: V_{OCH} = 160mV ±25mV V_{OCL} = 150mV ±25mV Is: V_{OCH} = 160mV ±35mV V_{OCL} = 160mV ±35mV
5	5, 9	Overvoltage threshold Charge enable threshold Undervoltage threshold	Added bq2058W
6	9	DC electrical characteristics	Was: Minimum V_{OP} = 0V, Is: Minimum V_{OP} = 4V
7	5, 9	Overvoltage threshold	Added bq2058C and bq2058G
8	4	Reference circuit amended	Moved D1 to new location

Notes: Change 1 = Feb. 1997 B changes from Jan. 1997 A. Change 2 = April 1997 C changes from Feb. 1997 B.
Change 3 = June 1997 D changes from April 1997 C. Change 4 = July 1997 E changes from June 1997 D.
Change 5 = Feb. 1998 F changes from July 1997 E. Change 6 = May 1998 G changes from Feb. 1998 F.
Change 7 = June 1998 H changes from May 1998 G.
Change 8 = Jan. 1999 I changes from June 1998 H.

11/12

Ordering Information

bq2058 _ _ XXXX

Standard Device:
Blank = Standard device
XXXX = Customer code assigned by Unitrode

Package Option:
SN = 16-pin narrow SOIC

Overvoltage Threshold
Blank = 4.25V (Standard device)
Contact Factory for availability of other thresholds

Device:
bq2058 Lithium Ion Pack Supervisor

Package Devices		
T_A	V_{OV} Threshold	16-pin Narrow SOIC (SN)
-30°C To +70°C	3.4V	bq2058WSN
	4.15V	bq2058MSN
	4.20V	bq2058FSN
	4.225V	bq2058KSN
	4.25V	bq2058SN
	4.325	bq2058CSN
	4.30V	bq2058DSN
	4.35V	bq2058RSN
	4.36V	bq2058JSN
	4.375V	bq2058GSN

Notes: bq2058SN is Standard Device.
Contact factory for availability of other thresholds and tolerances.

12/12

UNITRODE

bq2058T

Lithium Ion Pack Supervisor for 2-Cell Packs

Features

- Protects and individually monitors two Li-Ion series cells for overvoltage, undervoltage
- Monitors pack for overcurrent
- Designed for battery pack integration
- Minimal external components
- Drives external FET switches
- Selectable overvoltage (V_{OV}) thresholds
  - Mask-programmable by Unitrode
  - Standard version–4.25V
- Supply current: 12µA typical
- Sleep current: 0.7µA typical
- 16-pin 150-mil narrow SOIC

General Description

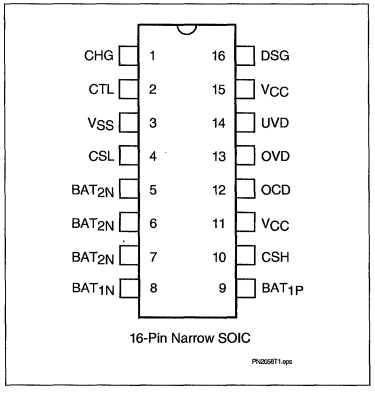
The bq2058T Lithium Ion Pack Supervisor is designed to control the charge and discharge cell voltage limits for two lithium-ion (Li-Ion) series cells, accommodating battery packs containing series/parallel configurations. The low operating current does not overdischarge the cells during periods of storage and does not significantly increase the system discharge load. The bq2058T can be part of a low-cost Li-Ion charge control system within the battery pack.

The bq2058T controls two external FETs to limit the charge and discharge potentials. The bq2058T allows charging when each individual cell voltage is below V_{OV} (overvoltage limit). If the voltage on any cell exceeds V_{OV} for a user-configurable delay period (t_{OVD}), the open-drain CHG pin goes to the high-impedance state, shutting off charge to the battery pack. This safety feature prevents overcharge of any cell within the battery pack. After an overvoltage condition occurs, each cell must fall below V_{CE} (charge enable voltage) for the bq2058T to re-enable charging.

The bq2058T protects batteries from overdischarge. If the voltage on any cell falls below V_{UV} (undervoltage limit) for a user-configurable delay period (t_{UVD}), the DSG output is driven low, shutting off the battery discharge. This safety feature prevents overdischarge of any cell within the battery pack.

The bq2058T also stops discharge on detection of an overcurrent condition, such as a short circuit. If an overcurrent condition occurs for a user-configurable delay period (t_{OCD}), the DSG output is driven low, disconnecting the load from the pack. DSG remains low until removal of the short circuit or overcurrent condition.

Pin Connections



16-Pin Narrow SOIC

PN2058T1.eps

Pin Names

CHG	Charge control output
CTL	Pack disable input
V_{SS}	Low potential input
CSL	Overcurrent sense low-side input
BAT_{2N}	Battery 2 negative input
BAT_{1N}	Battery 1 negative input
DSG	Discharge control output
UVD	Undervoltage delay input
OVD	Overvoltage delay input
OCD	Overcurrent delay input
V_{CC}	High potential input
CSH	Overcurrent sense high-side input
BAT_{1P}	Battery 1 positive input

Pin Descriptions

CHG **Charge control output**

This open-drain output controls the charge path to the battery pack. Charging is allowed when high.

CTL **Pack disable input**

When high, this input allows an external source to disable the pack by making both DSG and CHG inactive. For normal operation, the CTL pin is low.

V_{SS} **Low potential input**

CSL **Overcurrent sense low-side input**

This input is connected between the low-side discharge FET (or sense resistor) and BAT_{2N} to enable overcurrent sensing in the battery pack's ground path.

BAT_{2N} **Battery 2 negative inputs (3 pins)**

These pins are connected to the negative terminal of the cell designated BAT2 in Figure 2.

BAT_{1N} **Battery 1 negative input**

This input is connected to the negative terminal of the cell designated BAT1 in Figure 2.

DSG **Discharge control output**

This push-pull output controls the discharge path to the battery pack. Discharge is allowed when high.

UVD **Undervoltage delay input**

This input uses an external capacitor to V_{CC} to set the undervoltage delay timing.

OVD **Overvoltage delay input**

This input uses an external capacitor to V_{CC} to set the overvoltage delay timing.

OCD **Overcurrent delay input**

This input uses an external capacitor to V_{CC} to set the overcurrent delay timing.

V_{CC} **High potential inputs (2 pins)**

CSH **Overcurrent sense high-side input**

This input is connected between the high-side discharge FET (or sense resistor) and BAT_{1P} to enable overcurrent sense in the battery pack's positive supply path.

BAT_{1P} **Battery 1 positive input**

This input is connected to the positive terminal of the cell designated BAT1 in Figure 2.

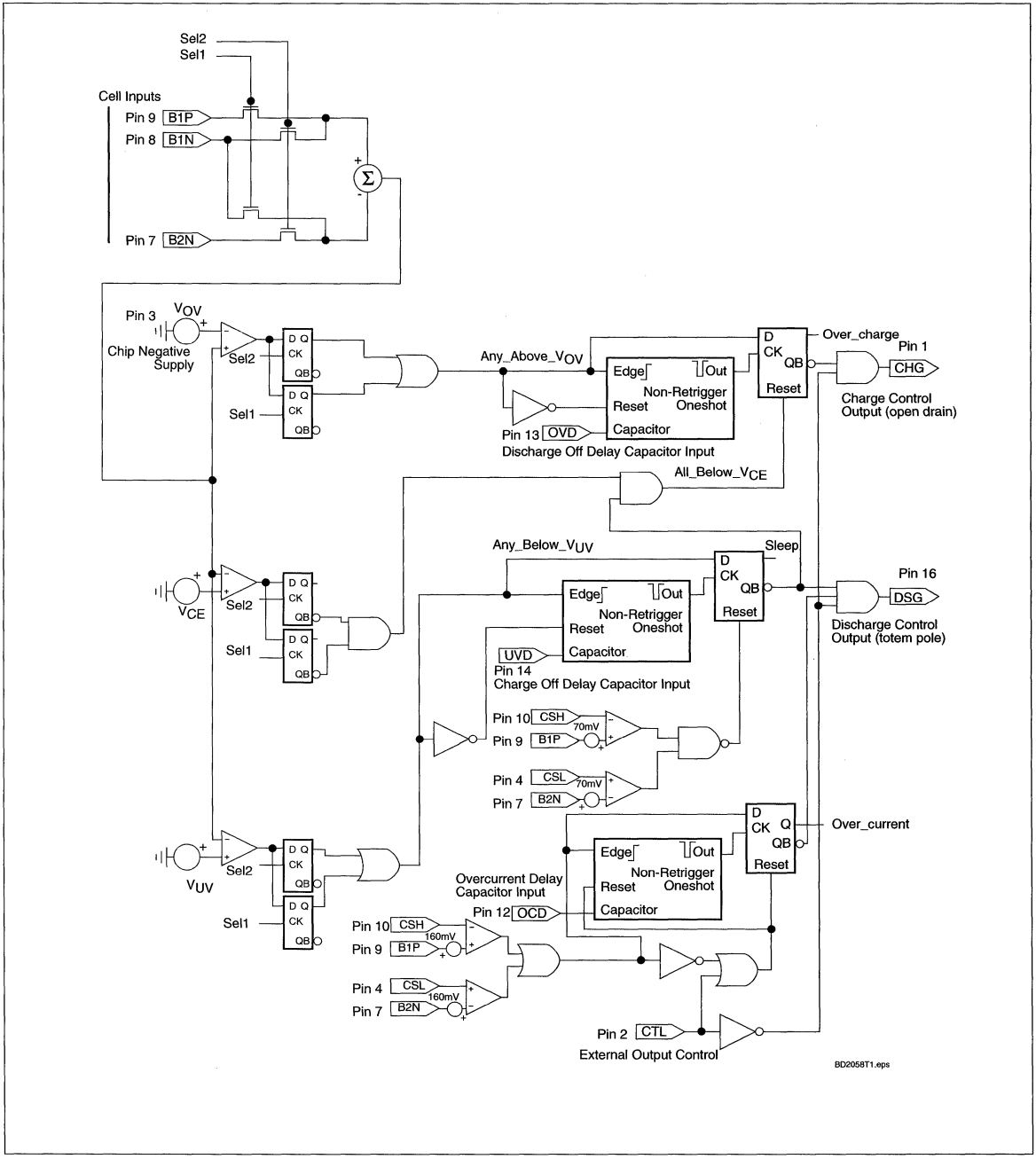


Figure 1. Block Diagram

Functional Description

Figure 1 is a block diagram outlining the major components of the bq2058T. Figure 2 shows a low-side control connection diagram. The following sections detail the various functional aspects of the bq2058T.

Thresholds

The bq2058T monitors the lithium ion pack for the conditions listed below. Shown with these conditions are the respective thresholds used to determine if that condition exists:

- Overvoltage (V_{OV})
- Undervoltage (V_{UV})
- Overcurrent (V_{OCH}, V_{OCL})
- Charge Enable (V_{CE})
- Charge Detect (V_{CD})

The bq2058T samples a cell every 60ms (typical). Every sample is a fully differential measurement of each cell. During this sample period, the bq2058T compares the measurements with these thresholds to determine if any of the these conditions exist: V_{OV}, V_{UV}, and V_{CE}.

Overcurrent and charge detect are conditions that are not sampled, but are continuously monitored.

Initialization

On initial power-up, such as connecting the battery pack for the first time to the bq2058T, the bq2058T enters the low-power sleep mode, disabling the DSG output. **It is recommended that a top to bottom cell connection be made at pack assembly for proper initialization.** A charging supply must be applied to the bq2058T circuit to enable the pack. See Low-Power Sleep Mode and Charge Detect sections.

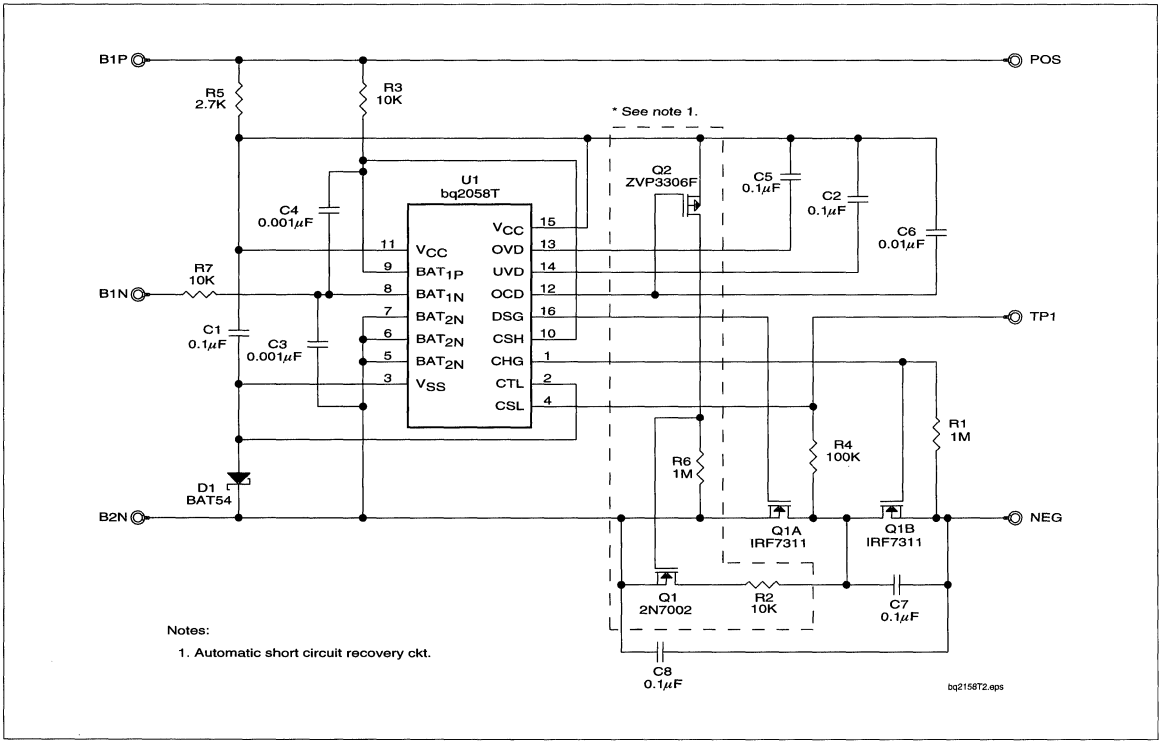


Figure 2. Two-Cell Connection Diagram, Low-Side Control

Low-Power Sleep Mode

The bq2058T enters the low-power sleep mode in two different ways:

1. On initial power-up.
2. After the detection of an undervoltage condition–V_{UV}.

When the bq2058T enters the low-power sleep mode, DSG is driven low and the device consumes 0.7µA (typical). The bq2058T only comes out of low-power sleep mode when a valid charge detect condition exists.

Charge Detect

The bq2058T continuously monitors for a charge detect condition. A valid charge detect condition exists when either of the conditions is true:

$$CSL < BAT_{2N} - 70mV\ (V_{CD})$$

$$CSH > BAT_{1P} + 70mV\ (V_{CD})$$

A valid charge detect enables the DSG output, allowing charging of the lithium ion cells. This is accomplished by applying the charging supply to the pack.

Undervoltage

Undervoltage (or overdischarge) protection is asserted when any cell voltage drops below the V_{UV} threshold and remains below the V_{UV} threshold for a time exceeding a user-configurable delay (t_{UVD}). The DSG output is driven low, disabling the discharge of the pack. The bq2058T then enters the low-power sleep mode. V_{UV} is defined as follows:

$$V_{UV} = 2.25V$$

Overvoltage

Overvoltage (or overcharge) protection is asserted when any cell voltage exceeds the V_{OV} threshold and remains above the V_{OV} threshold for a time exceeding a user-configurable delay (t_{OVD}). The CHG pin goes to the high impedance state, disabling charge into the battery pack. Since the charge control output is an open drain output, a pull-down resistor is needed from the CHG pin to the negative side of the pack. This pulls the gate of the charge FET low when the CHG pin goes to high impedance. Charging is disabled until a valid charge enable exists. See Charge Enable section.

Important note: If any battery pin floats (BAT_{1P}, BAT_{1N}, BAT_{2N}), the bq2058T assumes an overvoltage has occurred.

Because of different manufacturers' specifications for overvoltage thresholds, the bq2058T can be available with different V_{OV} options. Table 1 summarizes these different voltage thresholds.

5/12

Table 1. Overvoltage Threshold Options

Part No.	V_{OV} Limit
bq2058T	4.25V
bq2058TR	4.35V
bq2058TW	3.4V

The overvoltage threshold limits are programmed at Unitrode. The bq2058T is the standard option that is more readily available for sampling and prototyping purposes. Please contact Unitrode for other voltage threshold and tolerance options.

Charge Enable

A valid charge enable indicates that an overvoltage (overcharge) condition no longer exists and that the pack is ready to accept further charge. Once overvoltage protection is asserted, charging will not be enabled until all cell voltages fall below V_{CE}. The V_{CE} threshold is a function of V_{OV}, and changes with different V_{OV} limits.

$$V_{CE} = V_{OV} - 150mV$$

Overcurrent

The bq2058T detects an overcurrent (or short circuit) condition only in the discharge direction. Overcurrent protection is asserted when either of the conditions occurs and remain for a time exceeding a user-configurable delay (t_{OCD}):

$$CSL > BAT_{2N} + V_{OCL}$$

$$CSH < BAT_{1P} - V_{OCH}$$

where:

$$V_{OCL} = 160mV\ (low\text{-}side\ detect)$$

$$V_{OCH} = 160mV\ (high\text{-}side\ detect)$$

When either of these conditions occurs, DSG is driven low, disconnecting the load from the pack. DSG remains low until both of the voltage conditions are false, indicating removal of the short-circuit condition. The user can facilitate clearing these conditions by inserting the battery pack into a charger.

The high-side overcurrent sense can be disabled by connecting CSH to BAT_{1P}. This ensures that CSH is never greater than BAT_{1P}. If high-side detection is disabled, low-side detection must be used with CSL.

The FETs in the charge/discharge path controlled by the CHG and DSG pins affect the overcurrent level. The on-resistance of these FETs need to be taken into account when determining overcurrent levels.

CHG and DSG States

The CHG and DSG output truth table is shown below:

Condition	CHG pin	DSG pin
Normal operation	High	High
Overvoltage	Z	High
Undervoltage	High	Low
Overcurrent	High	Low
Floating battery input	Z	Indeterminate
CTL = high	Z	Low

The polarities of CHG and DSG are mask programmable at Unitrode. Push-pull vs. open-drain configuration is also mask-configurable at Unitrode. Please contact Unitrode for availability of these variations.

Pack Disable Input–CTL

The CTL pin is used to electrically disconnect the battery from the pack terminals through an externally supplied signal. When CTL is taken high, CHG goes to the high impedance state and DSG is driven low. Any load on the pack terminals will be interpreted as an overcurrent condition by the bq2058T with the overcurrent delay timer held in reset. When the CTL pin is driven low, the overcurrent delay timer is allowed to start. If the programmed delay (t_{OCD}) is too short, the overcurrent recovery circuit, if implemented, will be unable to correct the overcurrent situation prior to the delay timeout. It is recommended that a delay time of greater than 10ms ($C_{OCD} \geq 0.01\mu F$) be used if the CTL pin function is to be utilized.

Important note: If CTL floats, it is internally pulled high making both DSG and CHG inactive, thus disabling the pack. If CTL is not used, it should be tied to V_{SS}.

The polarity of CTL is mask-programmable at Unitrode. Please contact Unitrode for other polarity options.

Protection Delay Timers

The delay time between the detection of an overcurrent, overvoltage, or undervoltage condition and the deactivation of the CHG and/or DSG outputs is user-configurable by the selection of capacitor values between V_{CC} and OCD, OVD, and UVD pins (respectively. See Table 2 below.

The fault condition must persist through the entire delay period, or the bq2058T may not deactivate either FET control output.

Figure 3 shows a step-by-step event cycle for the bq2058T.

Table 2. Protection Delay Timers

Protection Feature	Delay Period	Capacitor from V_{CC} to:	Typical		Tolerance
			Capacitor	Time	
Overcurrent	t_{OCD}	OCD	0.010µF	12ms	±40%
Overvoltage	t_{OVD}	OVD	0.100µF	950ms	±40%
Undervoltage	t_{UVD}	UVD	0.100µF	950ms	±40%

Notes:

1. The delay time versus capacitance can be approximated by the following equations:.

   For t_{OCD}: $t_{(s)} \approx 1.2 * C_{(\mu f)}$, where $0.001\mu F \leq C \leq 0.1\mu F$
   For t_{OVD}, t_{UVD}: $t_{(s)} \approx 9.5 * C_{(\mu f)}$, where $0.01\mu F \leq C \leq 1\mu F$

2. Overvoltage and undervoltage conditions are sampled by the bq2058T. The delay in Table 2 is in addition to the time required for the bq2058T to detect the violation, which may vary from 0 to 120 ms depending on where in the sampling period the violation occurs. Overcurrent is continuously monitored and is subject to a delay of approximately 1.5ms.

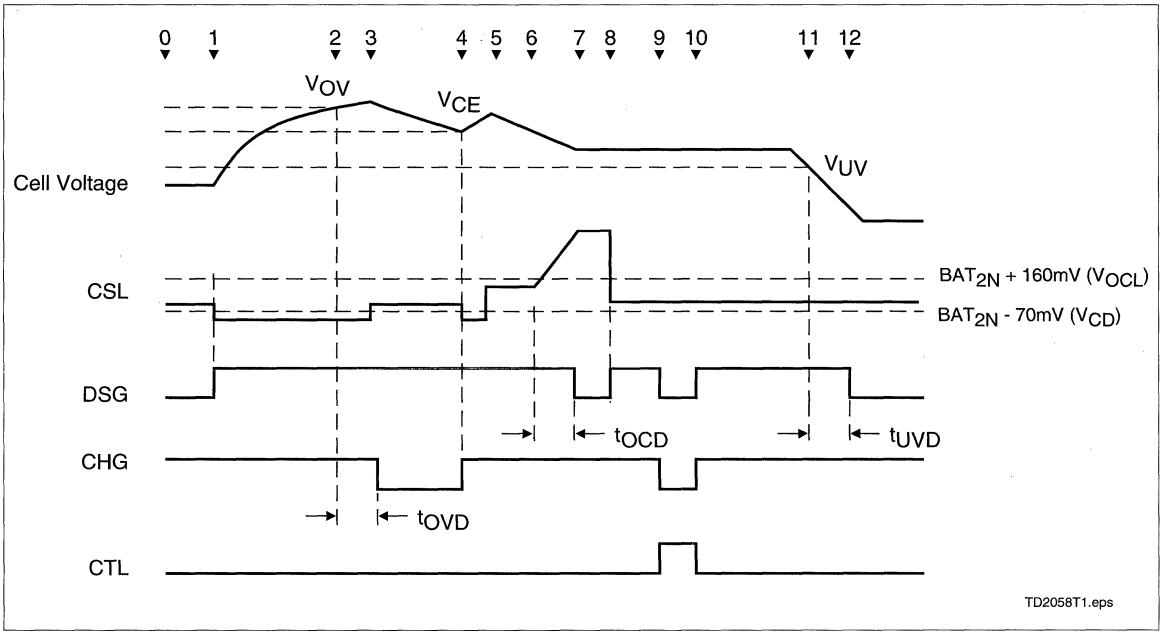


Figure 3. Protector Event Diagram

Event Definition:

0: The bq2058T is in the low-power sleep mode because one or more of the cell voltages are below V_{UV}.

1: A charger is applied to the pack, causing the difference between CSL and BAT_{2N} to become greater than 70mV. This awakens the bq2058T, and the discharge pin DSG goes high.

2: One or more cells charge to a voltage equal to V_{OV}, initiating the overvoltage delay timer.

3: The overvoltage delay time expires, causing CHG to go to high impedance (pulled low externally).

4: All cell voltages fall below V_{CE}, causing CHG to go high.

5: Stop charging, apply a load.

6: An overcurrent condition is detected, initiating the overcurrent delay timer.

7: The overcurrent delay time expires, causing DSG to go low.

8: The overcurrent condition is no longer present. DSG is driven high.

9: Pin CTL is driven high; both DSG and CHG go inactive.

10: Pin CTL is driven low; both DSG and CHG go active resuming their normal function.

11: One or more cells fall below V_{UV}, initiating the overdischarge delay timer.

12: Once the overdischarge delay timer expires, if any of the cells is below V_{UV}, the bq2058T drives DSG low and enters the low-power sleep mode.

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	Supply voltage	18	V	Relative to V_{SS}
T_{OPR}	Operating temperature	-30 to +70	°C	
T_{STG}	Storage temperature	-55 to +125	°C	
T_{SOLDER}	Soldering temperature	260	°C	For 10 seconds
I_{IN}	Maximum input current	±100	µA	All pins except V_{CC}, V_{SS}

Notes:
1. Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.
2. Internal protection diodes are in place on every pin relative to V_{CC} and V_{SS}. See Figure 4.

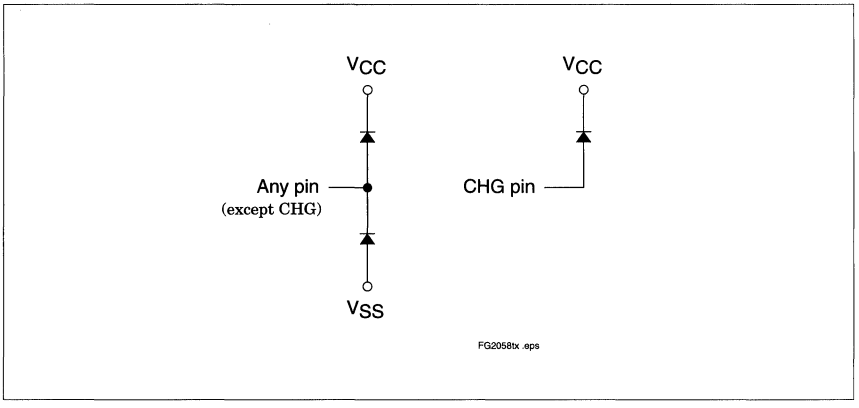


Figure 4. Internal Protection Diodes

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
V_{OH}	Output high voltage	V_{CC} - 0.5	-	-	V	I_{OH} = 10µA, CHG, DSG
V_{OL}	Output low voltage	-	-	V_{SS} + 0.5	V	I_{OL} = 10µA, CHG, DSG
V_{OP}	Operating voltage	4	-	9.0	V	V_{CC} relative to V_{SS}
V_{IL}	Input low voltage	-	-	V_{SS} + 0.5	V	Pin CTL
V_{IH}	Input high voltage	V_{SS} + 2.0	-	-	V	Pin CTL
I_{CCA}	Active current	-	12	25	µA	
I_{CCS}	Sleep current	-	0.7	1.5	µA	
R_{CELL}	Input impedance	-	10	-	MΩ	Pins BAT_{2N}, BAT_{1N}, and BAT_{1P}

DC Thresholds ($T_A = T_{OPR}$)

Symbol	Parameter	Value	Unit	Tolerance	Conditons
V_{OV}	Overvoltage threshold (see Figure 5)	4.25	V	±55mV	See note 1
		Table 1			Customer option
V_{CE}	Charge enable threshold	V_{OV} - 150mV	V	±55mV	
		V_{OV} - 200mV	V	±55mV	For bq2058TW only
V_{UV}	Undervoltage threshold	2.25	V	±100mV	
		2.10	V	±100mV	For bq2058TW only
V_{OCH}	Overcurrent detect high-side	160	mV	±35mV	
V_{OCL}	Overcurrent detect low-side	160	mV	±35mV	
V_{CD}	Charge detect threshold	70	mV	-60mV, +80mV	
t_{OVD}	Overvoltage delay threshold	950	ms	±40%	C_{OVD} = 0.100µF T_A = 30°C See note 2
t_{UVD}	Undervoltage delay threshold	950	ms	±40%	C_{UVD} = 0.100µF T_A = 30°C See note 2
t_{OCD}	Overcurrent delay threshold	12	ms	±40%	C_{OCD} = 0.01µF T_A = 30°C

Notes:
1. Standard device. Contact Unitrode for different thresholds and tolerance options
2. Does not include cell sampling delay, which may add up to 120ms of additional delay until the condition is detected.

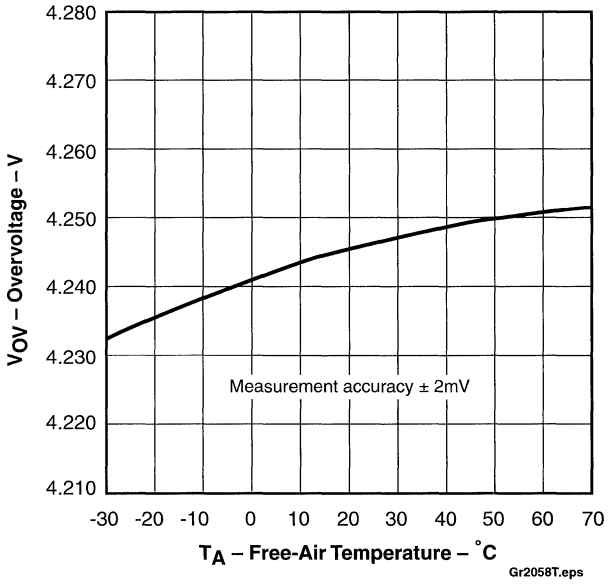


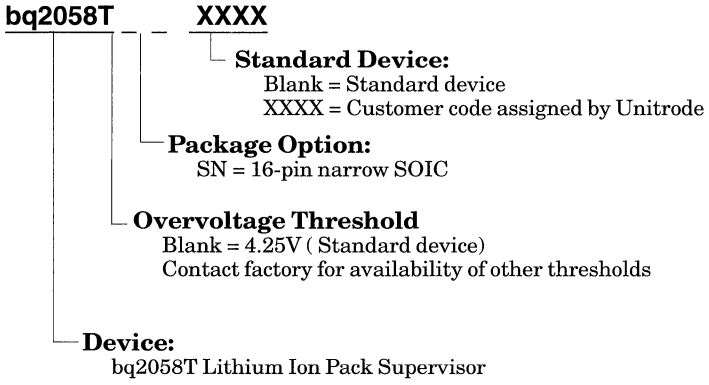
Figure 5. bq2058T 4.25V Overvoltage Threshold vs. Free-Air Temperature

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	5	CHG pin output state	CHG pin state at overvoltage and floating battery input was low, is now Z
1	9	Overcurrent limits	Was: V_{OCL} = 100mV ±25mV Is: V_{OCL} = 150mV ±25mV
1	9	Charge detect threshold	Was: 70mV +10mV, +80mV Is: 70mV -60mV, +80mV
2	4	Overvoltage options, Table 1	Added bq2058TR
2	4	Figure 2	Corrected schematic
2	6, 9	Delay thresholds	Was: t_{OCD} = 10ms ±30% t_{OVD} = 800ms ±30% t_{UVD} = 800ms ±30% Is: t_{OCD} = 12ms ±40% t_{OVD} = 950ms ±40% t_{UVD} = 950ms ±40%
2	7	DSG and CHG timing diagram	Inverted lines for proper logic levels
2	7	Timing Diagram	Was: CSH timing Is: CSL timing
2	8	Maximum input current	Added I_{IN}
2	9	V_{OV} tolerance	Was: ±50mV Is: ±55mV
2	9	Overcurrent limits	Was: V_{OCH} = 160mV +25mV V_{OCL} = 150mV +25mV Is: V_{OCH} = 160mV +35mV V_{OCL} = 160mV +35mV
2	9	V_{OP}	Was: 0V min, 18V max Is: 4V min, 9V max
3	5, 9	Overvoltage threshold Charge enable threshold Undervoltage threshold	Added bq2058TW

Notes: Change 1 = June 1997 B changes from April 1997.
Change 2 = July 1997 C changes from June 1997 B.
Change 3 = May 1998 D changes from July 1997 C.

Ordering Information



Package Devices		
T_A	V_{OV} Threshold	16-pin Narrow SOIC (SN)
-30°C to +70°C	3.4V	bq2058TWSN
	4.15V	bq2058TMSN
	4.20V	bq2058TFSN
	4.225V	bq2058TKSN
	4.25V	bq2058TSN
	4.30V	bq2058TDSN
	4.35V	bq2058TRSN
	4.36V	bq2058TJSN

Notes: bq2058TSN is Standard Device.
Contact factory for availability of other thresholds and tolerances.

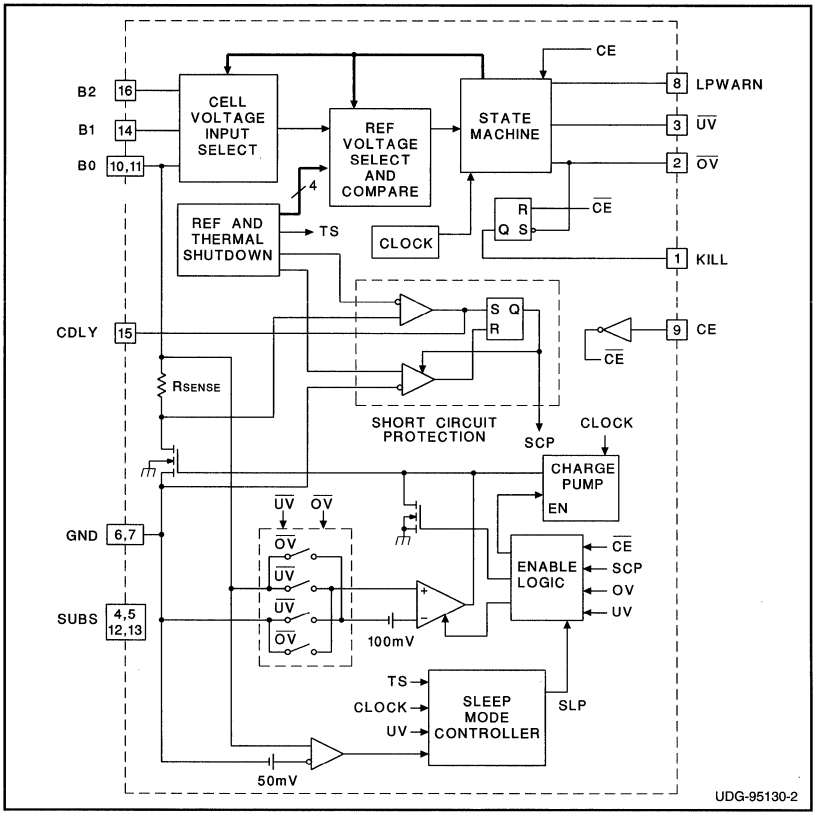
12/12

Lithium-Ion Battery Protector

FEATURES

- Protects Sensitive Lithium-Ion Cells from Overcharging and Over-Discharging
- Used for Two-Cell Lithium-Ion Battery Packs
- No External FETs Required
- Provides Protection Against Battery Pack Output Short Circuit
- Extremely Low Power Drain on Batteries of About 20µA
- Low Internal FET Switch Voltage Drop
- User Controllable Delay for Tripping Short Circuit Current Protector
- 3A Current Capacity

BLOCK DIAGRAM



DESCRIPTION

The UCC3911 is a two-cell lithium-ion battery pack protector IC that incorporates an on-chip series FET switch thus reducing manufacturing costs and increasing reliability. The IC's primary function is to protect both lithium-ion cells in a two-cell battery pack from being either overcharged or over-discharged. It employs a precision bandgap voltage reference that is used to detect when either cell is approaching an overcharged or over-discharged state. When on board logic detects either condition, the series FET switch opens to protect the cells.

A negative feedback loop controls the FET switch when the battery pack is in either the overcharged or over-discharged state. In the overcharged state the action of the feedback loop is to allow only discharge current to pass through the FET switch. In the over-discharged state, only charging current is allowed to flow. The op amp that drives the loop is powered only when in one of these two states. In the over-discharged state the chip enters sleep mode until it senses that the pack is being charged.

The FET switch is driven by a charge pump when the battery pack is in a normally charged state to achieve the lowest possible RDSON. In this state the negative feedback loop's op amp is powered down to conserve battery power. Short circuit protection for the battery pack is provided and has a nominal delay of 100µs before tripping. An external capacitor may be connected between CDLY and B0 to increase this delay time to allow longer overcurrent transients.

A chip enable (CE) pin is provided that while held low, inhibits normal operation of the chip to facilitate assembly of the battery pack.

The UCC3911 is specified for operation over the temperature range of –20°C to +70°C, the typical operating and storage temperature range of lithium-ion batteries.

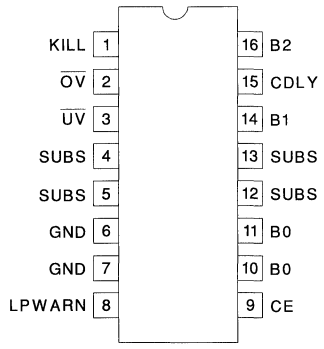
ABSOLUTE MAXIMUM RATINGS

Maximum Input Voltage (B2, GND) 14V
Minimum Input Voltage (B0, GND) 9.0V
Maximum Charge Current (B0, GND) 3.3A
Minimum Discharge Current (B0, GND) 3.3A
Storage Temperature . . . . . 65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

SOIC-16 (Top View)
DP Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, these specifications apply for –20°C to +70°C for the UCC3911, all voltages are referenced to B0, V_{B2} = 7.2V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
State Transition Threshold					
Normal to Overcharge		4.20	4.25	4.30	V
Overcharge to Normal		3.65	3.75	3.85	V
Normal to Undercharge		2.42	2.5	2.58	V
Undercharge to Normal		2.90	3.0	3.10	V
B0/GND Switch					
V_{B0} - V_{GND}	(Normal) I_{GND} = 2A	–320	–160		mV
	(Normal) I_{GND} = –2A		160	320	mV
	(Overcharge) I_{GND} = 1mA		–150		mV
	(Overcharge) I_{GND} = 2A		–450		mV
	(Undercharge) I_{GND} = –1mA		150		mV
	(Undercharge) I_{GND} = –2A		450		mV
I_{GND}	(Overcharge) V_{GND} = –5V	–5	0		µA
	(Undercharge) V_{GND} = 5V		0	5	µA
Chip Bias Current					
I_{B2}	Nominal		18	25	µA
I_{B2}	In Sleep Mode		3.5		µA
I_{B1}	(Note 3)	–5	0	5	µA
Short Circuit Protection					
$I_{THRESHOLD}$		3.5	5.25	7	A
T_{DLY}	CDLY = Open (Note 1)		100		µs
Internal Clock Frequency	(Note 2)		7.5		kHz
T_{DLY} - $\overline{OV}$	Delay for Chip to Register $\overline{OV}$ Condition	0.6	2	5	ms
T_{DLY} - $\overline{UV}$	Delay for Chip to Register $\overline{UV}$ Condition	0.3	1	3.5	ms
$\overline{OV}$, $\overline{UV}$ Output Characteristics	V_{B2} - V_{HIGH} with I_{PIN} = –1000µA			1.1	V
	V_{LOW} With I_{PIN} = 100µA			0.43	V
Thermal Shutdown	(Note 1)		165		°C

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, these specifications apply for –20°C to +70°C for the UCC3911, all voltages are referenced to B0, V_{B2} = 7.2V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Short Circuit Protection (cont.)					
KILL Output Characteristics	V_{B2} - V_{HIGH} With I_{KILL} = –0.5mA			0.29	V
KILL Output Characteristics	V_{LOW} With I_{KILL} = 0.5mA			0.27	V
LPWARN Output Characteristics	V_{B2} - V_{HIGH} With I_{LPWARN} = –0.1mA			0.42	V
	V_{LOW} With I_{LPWARN} = 0.1mA			0.37	V
CE Threshold Voltage	V_{B2} = 8.5V	5	6	7	V
	V_{DD} = 5V	2.05	2.45	4.05	V

***Note 1**: Guaranteed by design. Not 100% tested in production.*
***Note 2**: Tested at functional probe only.*
***Note 3:** The 5µA current listed is for test purposes. The current in this pin is guaranteed by design to be much less than 1µA.*

PIN DESCRIPTIONS

B0: Connects to the negative terminal of the lower cell in the battery pack.

B1: Connects to the junction of the positive terminal of the lower cell and the negative terminal of the upper cell in the battery pack.

B2: Connects to the positive terminal of the upper cell in the battery pack. This pin also connects to the positive of the two terminals that are presented to the user of the battery pack.

CDLY: Delay control pin for the short circuit protection feature. A capacitor connected between this pin and the B0 pin will lengthen the time delay from when an overcurrent situation is detected to when the protection circuitry is activated. This control will be useful for those applications where high peak load currents may momentarily exceed the protection circuit's threshold current and interruption of the battery current would be undesirable. The nominal delay time is internally set at 100µs. The equation for determining this delay is:

$$T_{DLY}\ (\mu s) = 25 + (25 + C_{DLY}\ (pF)) \bullet 0.4 \bullet V_{B2}$$

To recover from an overcurrent "shutdown" the load must be removed momentarily from the pack.

CE: Chip Enable. While this signal is held low, the internal FET is held off and the KILL latch is held in reset. CE is pulled high by a 2µA current source. This function was included to facilitate construction of the battery pack by preventing the KILL latch from being erroneously set during final assembly. The last step in the electrical assembly of the pack would be cutting a link to B0.

GND: The second of the two terminals that are presented to the user of the battery pack. The internal FET switch connects this terminal to the B0 terminal to give the battery pack user appropriate access to the batteries. In an overcharged state, current is allowed to flow only into this terminal. Similarly, in an over-discharged state, current is allowed to flow only out of this terminal.

KILL: This active-high signal indicates that one or both of the cells has been overcharged. It can be used to drive a circuit breaker of some sort to permanently disable the battery pack as a safety feature. Note that when KILL goes active the chip simultaneously enters the $\overline{OV}$ state which inhibits further charging of the pack. The KILL latch is asynchronously reset by the CE signal.

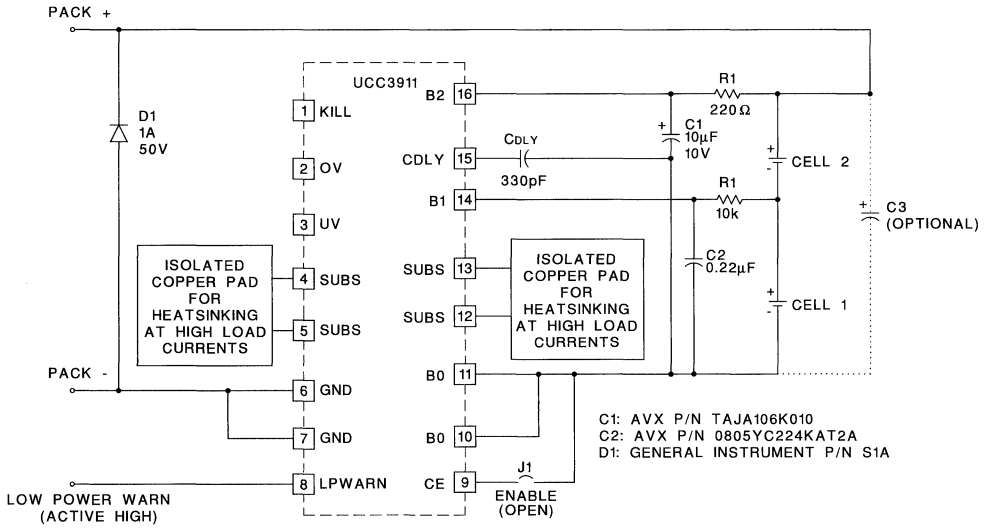
LPWARN: This active-high signal is the low Power Warning. The voltage on this pin goes high (to B2 potential) as soon as either of the battery's cells voltage falls below 3.0V. Once the $\overline{UV}$ state is entered, this output goes back to low.

$\overline{OV}$: This active-low signal indicates the state of the state machine's $\overline{OV}$ bit. When low, it indicates that one or both cells are overcharged. Further charging is inhibited by the opening of the FET switch. The internal signal also sets the KILL latch and activates the KILL output signal. The output buffer for this pin is sized to drive a very light load.

SUBS: The substrate connections for the UCC3911. Connect these points to a heat sink which is electrically isolated from all other IC pins.

$\overline{UV}$: This active-low signal indicates the state of the state machine's $\overline{UV}$ bit. When low, it indicates that one or both cells are over- discharged. Further discharging is inhibited by the opening of the FET switch. The chip enters the "Sleep" mode when $\overline{UV}$ goes high and waits in this state until the chip detects that the battery pack has been placed in a charging circuit. The output buffer for this pin is likewise sized to drive a very light load.

APPLICATIONS INFORMATION



Note: In this example, CDLY, C1 and C2 were selected to drive a 1500µF load.

Figure 1. UCC3911 Application Circuit including Components for Short Circuit Protection.

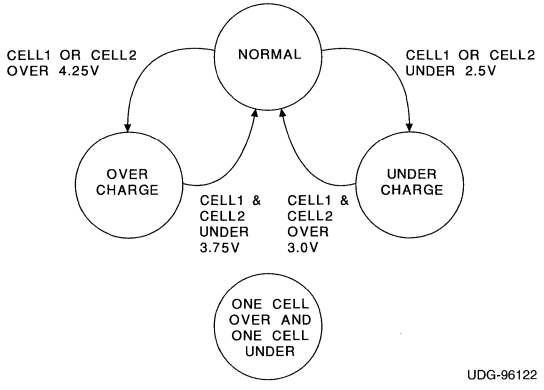
Figure 1 shows a typical application for the UCC3911 lithium-ion battery protector. All of the functions required to protect two series lithium-ion cells from overcharge and over-discharge, as well as provide short circuit protection, are included in a single chip. An internal state machine controls an internal power FET which allows either bi-directional or uni-directional battery current. An optional time delay capacitor can be included to slow the reaction time of the short circuit protection circuitry if desired.

While the IC is capable of providing overload and over/undervoltage protection of both cells with virtually no external parts, the demands of true short circuit protection require some passive external components.

State Machine Operation

The internal state machine constantly monitors the two cells for both overvoltage and undervoltage conditions. Figure 2 shows a state diagram which describes the operation of the protection circuitry. In the normal mode, both the $\overline{OV}$ and $\overline{UV}$ status bits are held high and full battery current is allowed through the internal power FET in either the charge or discharge direction.

If the voltage across one or both cells exceeds 4.25V, the $\overline{OV}$ signal goes low, and further charge current is not allowed. An internal feedback loop controls the power FET to allow only discharge current, allowing for battery recovery. The state machine will not reenter normal mode until the voltage across both cells decays to less than 3.75V. This feature is important to prevent circuit oscillation due to battery ESR when the circuitry transitions between states. The KILL output signal is also set high when the UCC3911 enters the OV state, and will remain



Note: The "One Cell Over and One Cell Under" state is entered whenever one cell is overcharged and the other cell is simultaneously over-discharged. When in this state, the series FET switch is turned off inhibiting both charging and discharging of the battery pack. If the battery pack ever gets into this condition, it should be discarded.

Figure 2. State Diagram

APPLICATIONS INFORMATION (cont.)

set unless the CE pin is brought low. The KILL latch can be used to permanently disable the battery pack with additional circuitry if desired.

If the voltage across one or both battery cells falls below 3V, the LPWARN signal goes high indicating a low power condition. This signal can be used to signal the user that the battery pack is in need of charge.

If the voltage across one or both cells falls below 2.5V, the $\overline{UV}$ signal goes low, and the feedback loop allows only charge current. The LPWARN signal goes low and the UCC3911 enters sleep mode which consumes only 3μA, limiting self discharge to a minimum. The circuit remains in this state until the voltage across both cells exceeds 3V. The battery pack can still be charged, unless the sum of the two cells voltages falls below 3.7V, which is the minimum guaranteed operating voltage for the IC.

If the battery cells become so poorly matched that the voltage across one cell exceeds 4.25V and the voltage across the other cell falls below 2.5V, the power FET will not pass either charge or discharge current, and both the $\overline{OV}$ and $\overline{UV}$ signals will be set low.

The normal high current path for battery current is through the B0 (10, 11) and GND (6, 7) pins of the UCC3911. The GND pins are intended to be connected to system ground for either the charger or the load. The SUBS pins (4, 5, 12, 13) are internally connected to the substrate of the UCC3911, which is internally referenced to B0 or GND depending on the direction of pack current. If high battery currents are anticipated, the SUBS pins can be thermally connected to a heat sink to control the IC temperature. However, this heat sink must be electrically isolated from all other IC pins including ground. This is a critically important point, as heat sinking to the system ground is not possible.

The CE pin is used to initialize the state of the battery pack during assembly. Holding this pin low forces the state machine to hold the FET off. The last step in the assembly process would be to cut the trace between this pin and B0 which allows the internal pull up to start the state machine.

Short Circuit Protection

As stated earlier, the demands of true short circuit protection requires that careful attention be paid to the selection of a few external components. This selection is discussed below.

In the Application circuit of Figure 1, diode D1 acts as a clamp across the battery pack output terminals to prevent damage to the IC from inductive kick when the pack current is shut off due to an overcurrent or over/undervoltage condition. (It also provides reverse polarity protection during charge.)

To prevent a momentary cell voltage drop, caused by large capacitive loads, from causing an erroneous undervoltage shutdown, an RC filter is required in series with the two battery sense inputs, B1 and B2. The resistors (R1 and R2) are sized to have a negligible impact on voltage sensing accuracy. The capacitors (C1 and C2) should be sized to provide a time constant longer than the overcurrent delay time. In the example of Figure 1, they are sized for a nominal 2.2ms time constant. They do not need to be low ESR style capacitors, as they see no ripple current. A larger resistor value and smaller capacitor value can be used on the B1 input due to the extremely low input current on this pin.

The overcurrent delay capacitor, C_{DLY}, sets the time delay, after the overcurrent threshold is exceeded, before turning off the UCC3911's internal FET. If no capacitor is used, the nominal delay is 100μs. To charge large capacitive loads without tripping the overcurrent circuit, a small capacitor (typically less than 1000pF) is used to extend the delay time. The approximate delay time is given below and shown graphically in Figure 3.

$$t_{DLY}(\mu s) = 25 + \left(25 + C_{DLY}(pF)\right) \bullet 0.4 \bullet V_{B2}$$

The amount of time required will be a function of the load capacitance, battery voltage, and the total circuit impedance, including the internal resistance of the cells, the UCC3911's on resistance, and the load capacitor ESR. The required delay time can be calculated from:

$$t = -R \bullet C \bullet 1n\left(\frac{I \bullet R}{V}\right)$$

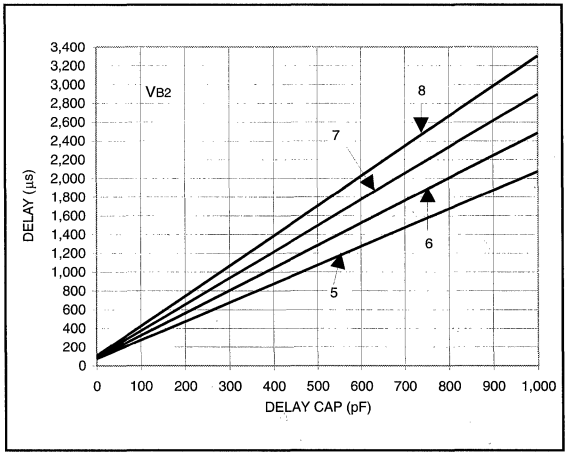


Figure 3. Nominal Overcurrent Delay Time vs CDLY and B2 Voltage.

APPLICATIONS INFORMATION (cont.)

In this equation, R is the total circuit resistance, C is the capacitor being charged, I is the overcurrent trip current (5.25A nominal), and V is the battery voltage. Using the minimum trip current of 3.5A and the maximum battery voltage of 8.4V, the worst case maximum delay time required is defined as:

$$t\max(\mu s) = -R \bullet C(\mu F) \bullet 1n \bullet \left(\frac{R}{2.4}\right)$$

In the example of Figure 1, CDLY, C1 and C2 are sized to drive a 1500μF load capacitor.

If large capacitive loads (or other loads with surge currents above the overcurrent trip threshold) are not being applied to the pack terminals, the overcurrent delay time can be short. In this case, it may be possible to eliminate CDLY, as well as R2 and C2 altogether (replacing R2 with a short). In addition, the time constant of R1 and C1 can be made much shorter. R1 and C2 are still necessary, however, to assure proper operation under short circuit conditions. It is important to maintain a minimum R1/C1 time constant of 100μs. (For example, R1 and C1 could be reduced to 100Ω and 1μF.)

Capacitor C3 is recommended, for the case where the wires connecting to the top and bottom of the cell stack are more than an inch long (not likely in a small battery pack). In this case, a 10μf, low ESR tantalum capacitor is recommended to prevent excessive overshoot at turn-off due to wiring inductance. It should be placed close to D1's cathode and pins 10 and 11 of the UCC3911.

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Enhanced Single Cell Lithium-Ion Battery Protection IC

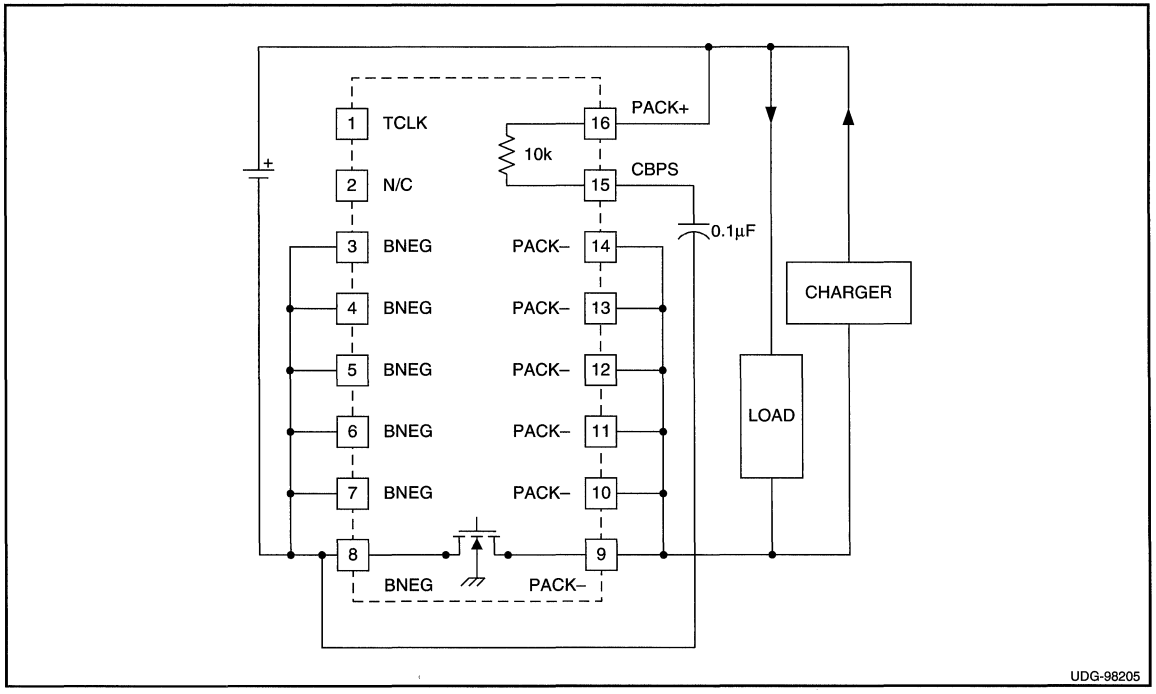
FEATURES

- Protects sensitive Lithium Ion cells from over-charging and over-discharging
- Dedicated for one cell applications
- Integrated low impedance MOSFET switch and sense resistor
- Precision trimmed overcharge and overdischarge voltage limits
- Extremely low power drain
- 2A current capacity
- Overcurrent and Short Circuit Protection
- Reverse Charger Protection
- Thermal Protection

DESCRIPTION

The UCC3952 is a monolithic BiCMOS lithium-ion battery protection circuit that is designed to enhance the useful operating life of one cell rechargeable battery pack. Cell protection features consist of internally trimmed charge and discharge voltage limits, discharge current limit with a delayed shutdown and an ultra low current sleep mode state when the cell is discharged. Additional features include an on chip MOSFET for reduced external component count and a charge pump for reduced power losses while charging or discharging a low cell voltage battery pack. This protection circuit requires one external capacitor and is able to operate and safely shutdown in the presence of a short circuit condition.

APPLICATION DIAGRAM

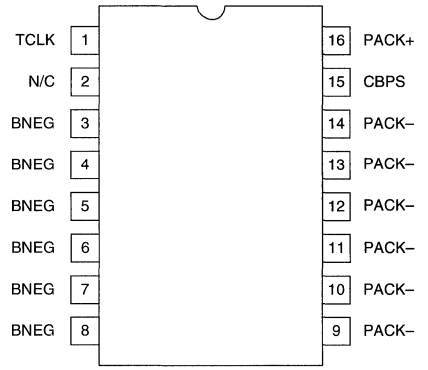


ABSOLUTE MAXIMUM RATINGS

Supply Voltage (PACK+ to BNEG–) 5V
Maximum Forward Voltage (PACK+ to PACK–) 16V
Maximum Reverse Voltage (PACK+ to PACK–) . . . . . –8V
Maximum Cell Continuous Charge Current 3A
Junction Temperature . . . . . –55°C to 150°C
Storage Temperature Range . . . . . –40°C to 125°C

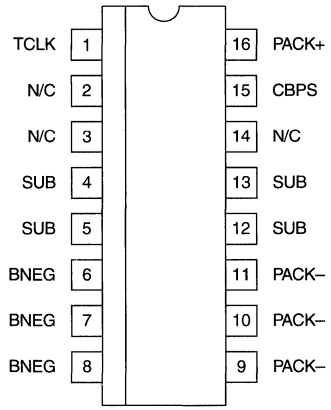
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

TSSOP-16 (TOP VIEW)
PW Package



CONNECTION DIAGRAMS

SOIC-16 (TOP VIEW)
DP Package



6

ELECTRICAL CHARACTERISTICS: Temperature Range: $-20°C < T_A < 70°C$, Unless otherwise stated. All voltages are with respect to BNEG. $T_A = T_J$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
State Transition Thresholds Section					
NORM to OV (V_{OV})	UCC3952-1	4.15	4.20	4.25	V
OV to NORM (V_{OVR})	UCC3952-1	3.85	3.90	3.95	V
NORM to OV (V_{OV})	UCC3952-2	4.20	4.25	4.30	V
OV to NORM (V_{OVR})	UCC3952-2	3.90	3.95	4.00	V
NORM to OV (V_{OV})	UCC3952-3	4.25	4.30	4.35	V
OV to NORM (V_{OVR})	UCC3952-3	3.95	4.00	4.05	V
NORM to OV (V_{OV})	UCC3952-4	4.30	4.35	4.40	V
OV to NORM (V_{OVR})	UCC3952-4	4.00	4.05	4.10	V
OV Delay Time (T_{OV})		1		2	sec
NORM to UV (V_{UV})	UCC3952-1, UCC3952-2, UCC3952-3, UCC3952-4	2.25	2.35	2.45	V
UV to NORM (V_{UVR})	UCC3952-1, UCC3952-2, UCC3952-3, UCC3952-4	2.55	2.65	2.75	V
Overdischarge Delay Time (T_{OD})		5	15	30	ms

ELECTRICAL CHARACTERISTICS: Temperature Range: $-20°C < T_A < 70°C$, Unless otherwise stated. All voltages are with respect to BNEG. $T_A = T_J$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Short Circuit Protection Section					
ITHLD	Discharge current limit, PACK+ = 3.7V	3.0		4.5	A
TDLY	Discharge current delay, PACK+ = 3.7V	1		2	ms
R_{RESET}	Discharge current reset resistance, PACK+ = 4.0	7.5			MΩ
Bias Section					
IDD	Normal operating current. $V_{PACK} > V_{UV}$		5	14	µA
IDD	Shutdown operating current $V_{PACK} < V_{UV}$			2.5	µA
V_{MIN}	Minimum cell voltage when all circuits are guaranteed to be fully functional			1.7	V
FET Switch Section					
V_{PACK-}	PACK+ > V_{OV}, I(SWITCH) = 1mA to 2A Battery overcharged state switch permits discharge current only.		100	400	mV
V_{PACK-}	PACK+ = 2.5V, I(SWITCH) = −1mA to −2A Battery overdischarged state switch permits charge current only.	−600	−100		mV
R_{ON}	In Normal Mode (when not in OV or UV). This value includes package and bondwire resistance. PACK+ = 2.5V		50	75	mΩ
Thermal Shutdown Section					
TS	Thermal shutdown temperature. (Note 1)		135		°C

Note 1. This parameter is guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

BNEG: Connect the negative terminal of the battery to this pin.

PACK+: Connect to the positive terminal of the battery. This pin is available to the user.

CBPS: This power supply bypass pin is connected to PACK+ through an internal 10K resistor. An external 0.1µF capacitor must be connected between this pin and BNEG.

PACK–: The negative terminal of the battery pack (negative terminal available to the user). The internal FET switch connects this terminal to the BNEG terminal to give the battery pack user appropriate access to the battery. In an over-charged state, only discharge current is permitted. In an over-discharged state, only charge current is permitted.

SUB: (DP Package Only) Do not connect. These pins must be electrically isolated from all other pins. These pins may be soldered to isolated coppper pads for heatsinking. However, most applications do not require heatsinking.

TCLK: Production Test Mode pin. This pin is used to provide a high frequency clock to the IC during production testing. In an application this pin may be left unconnected, or tied to BNEG.

APPLICATION INFORMATION

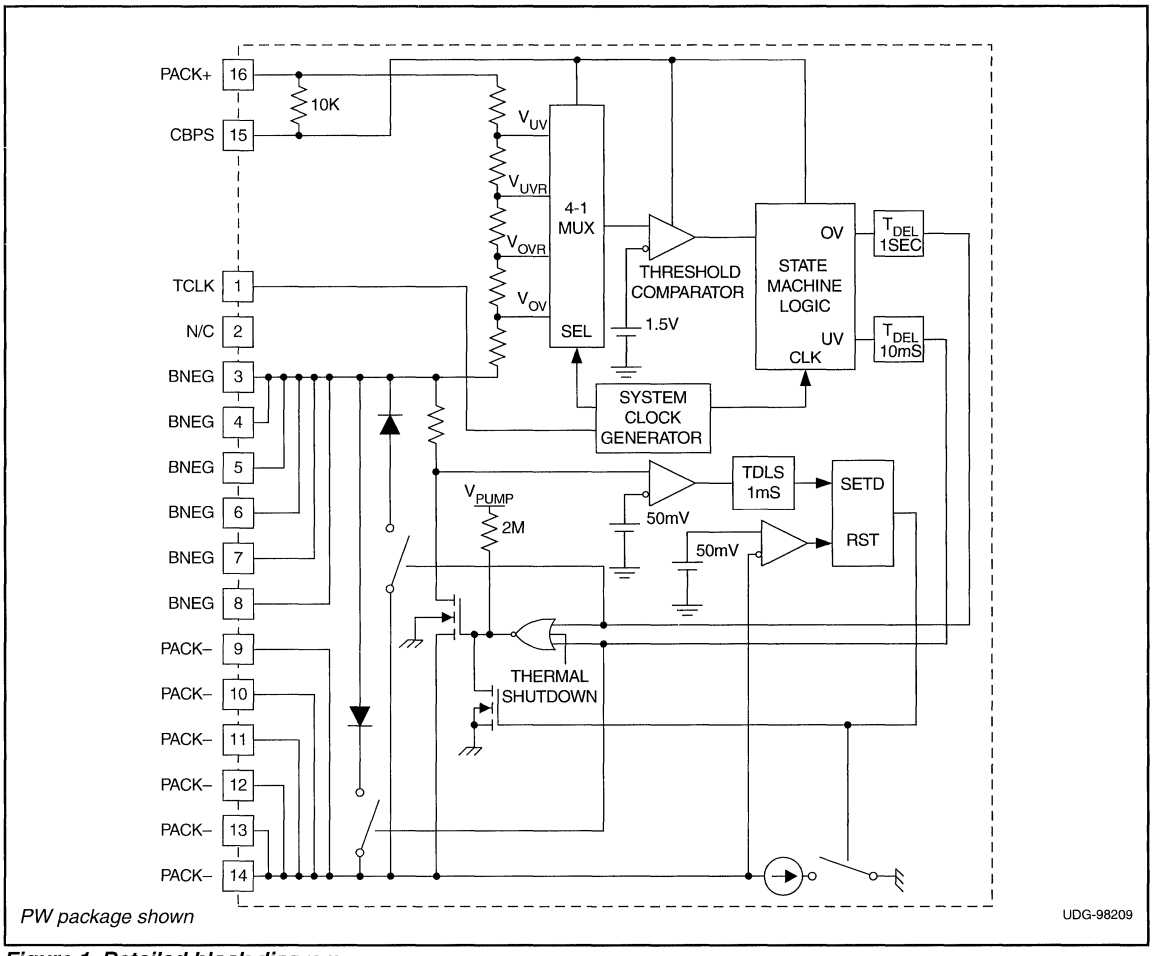


Figure 1. Detailed block diagram.

APPLICATION INFORMATION

Fig. 1 shows a detailed block diagram of the UCC3952.

Battery Voltage Monitoring

The battery cell voltage is sampled every 8ms by connecting a resistor divider across it and comparing the resulting voltage to a precision internal reference voltage. Under normal conditions (cell voltage is below Over Voltage threshold and above Under Voltage threshold), the UCC3952 consumes less than 10μA of current and the internal MOSFET is fully turned on with the aid of a charge pump.

When the cell voltage falls below the Under Voltage threshold for two consecutive samples, the IC disconnects the load from the battery pack and enters a super low power mode. The pack will remain in this state until it detects the application of a charger, at which point charging is enabled. The requirement of two consecutive readings below the UV threshold filters out momentary drops in cell voltage due to load transients, preventing nuisance trips.

If the cell voltage exceeds the Over Voltage threshold for 1sec, charging is disabled, however discharge current is still allowed. This feature of the IC is explained further in the section on Controlled Charge/Discharge Mode.

APPLICATION INFORMATION (cont.)

Over Current Monitoring and Protection

Discharge current is continuously monitored via an internal sense resistor. In the event of excessive current, an Over Current condition is declared if the high current (over 3A) persists for over 1ms. This delay allows for charging of the system bypass capacitors without tripping the overcurrent. A 0.1µF capacitor on the CBPS pin provides momentary holdup for the IC to assure proper operation in the event that a hard short suddenly pulls the cell voltage below the minimum operating voltage.

Once an Over Current condition has been declared, the internal MOSFET turns off. The only way to return the pack to normal operation is to remove the load by unplugging the pack from the system. The overcurrent is reset when an internal pull down brings PACK(–) to within 50mV of BNEG. At this point, the pack returns to its normal state of operation.

Controlled Charge/Discharge Mode

When the chip senses an over-voltage condition, it prevents any additional charging, but allows discharge. This is accomplished by activating a linear control loop which controls the gate of the MOSFET based on the differential voltage across its drain to source terminals. The linear loop attempts to regulate the differential voltage across the MOSFET to 100mV. When a light load is applied to the part, the loop adjusts the impedance of the MOSFET to maintain 100mV across it. As the load increases, the impedance of the MOSFET is decreased to maintain the 100mV control. At heavy loads (still below "over-current" limit level), the loop will not maintain regulation and will drive the gate of the MOSFET to the battery voltage (not the charge-pump output voltage). The MOSFET $R_{DS(on)}$ in the over-voltage state will be higher than $R_{DS(on)}$ during normal operation. The voltage drop (and associated power loss) across the internal MOSFET in this mode of operation is still significantly lower than the typical solution of two external back-to-back MOSFETs, where the body diode is conducting.

When the chip senses an under-voltage condition, it disconnects the load from the battery pack and shuts itself down to minimize current drain from the battery. Several circuits remain powered and will detect placement of the battery pack into a charger. Once the charger presence is detected, the linear loop is activated and the chip allows charging current into the battery. This linear control mode of operation is in effect until the battery voltage reaches a level of V_{UVR}, at which time normal operation is resumed.

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Three - Four Cell Lithium-Ion Protector Circuit

FEATURES

- Three or Four Cell Operation
- Two Tier Overcurrent Limiting
- 30µA Typical Supply Current Consumption
- 3.5µA Typical Supply Current in Sleep Mode
- Smart Discharge Minimizes Losses in Overcharge Mode
- 6.5V to 20V VDD Supply Range
- Highly Accurate Internal Voltage Reference
- Externally Adjustable Delays in Overcurrent Controller
- Detection of Loss of Cell Sense Connections

DESCRIPTION

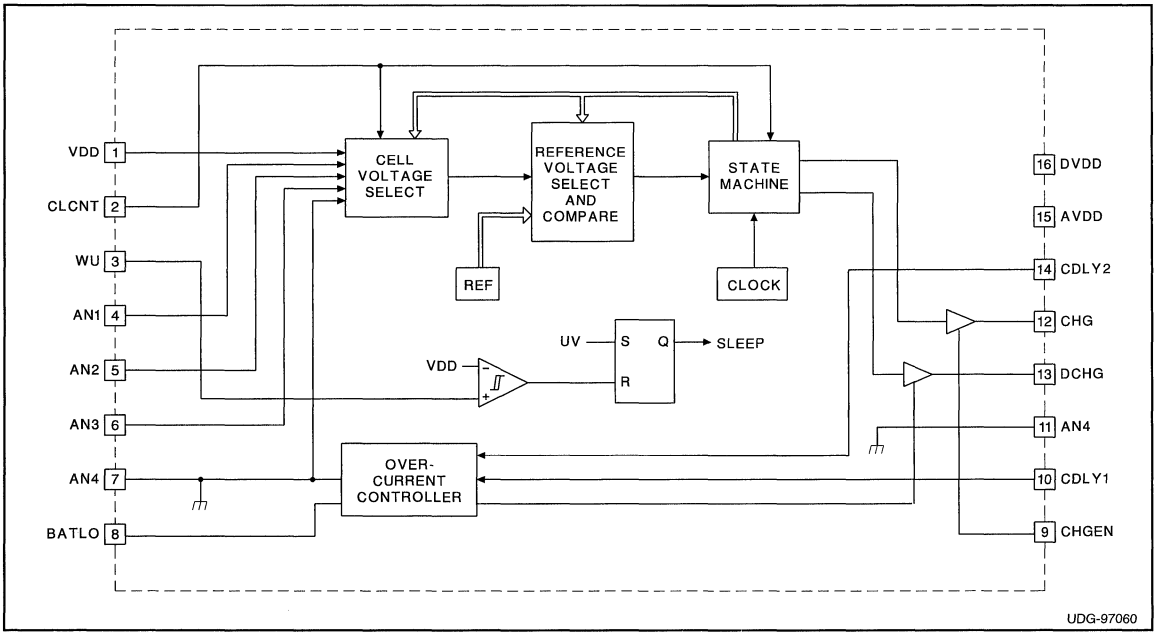
The UCC3957 is a BiCMOS three or four cell lithium-ion battery pack protector designed to operate with external P-channel MOSFETs. Utilizing external P-channel MOSFETs provides the benefits of no loss of system ground in an overdischarge state, and protects the IC as well as battery cells from damage during an overcharge state. An internal state machine runs continuously to protect each lithium-ion cell from overcharge and overdischarge. A separate overcurrent protection block protects the battery pack from excessive discharge currents.

If any cell voltage exceeds the overvoltage threshold, the appropriate external P-channel MOSFET is turned off, preventing further charge current. An external N-channel MOSFET is required to level shift to this high side P-channel MOSFET. Discharge current can still flow through the second PFET. Likewise, if any cell voltage falls below the undervoltage limit, the second P-channel MOSFET is turned off and only charge current is allowed. Such a cell voltage condition will cause the chip to go into low power sleep mode. Attempting to charge the battery pack will wake up the chip. A cell count pin (CLCNT) is provided to program the IC for three or four cell operations.

A two tiered overcurrent controller and external current shunt protect the battery pack from excessive discharge currents. If the first overcurrent threshold level is exceeded, an internal timing circuit charges an external capacitor to provide a user programmable blanking time.

(continued)

BLOCK DIAGRAM



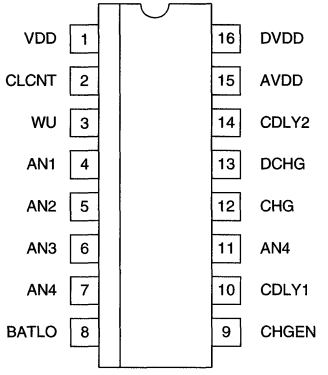
ABSOLUTE MAXIMUM RATINGS

Supply Voltage 20V
Supply Current 25mA
Output Current (CHG, DCHG) 25mA
WU Input Voltage 28V
BATLO Input Voltage ..... –0.3V to 2.5V
AN1 and AN3 Input Voltage ..... VAN4 – VDD
CLCNT and CHGEN ..... VAN4 – VDD
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Unless otherwise indicated, voltages are referenced to AN4. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

SSOP-16 (Top View)
M Package



DESCRIPTION (continued)

If at the end of the blanking time the overcurrent condition still exists, the external discharge FET is turned off for a period 17 times longer than the first blanking period, and then the discharge FET is turned back on. If at any time a second higher overcurrent threshold is exceeded for more than a user programmable time, the discharge FET is turned off, and will remain off for the same period as the first tier off time. This two tiered overcurrent protection scheme allows for charging capacitive loads while retaining effective short circuit protection.

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VDD = 16V and –20°C < T_A < 70°C, T_A = T_J. All voltages measured with respect to the AN4 terminal.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Section					
Minimum V_{DD}			5.0	5.5	V
Supply Current			30	40	µA
Sleep Mode Supply Current	V_{DD} = 10.4V		3.5	7.5	µA
Output Section					
DCHG Output Current	Driving Logic Low and V_O = 1V	40	70	100	µA
	Driving Logic High and V_O = VDD – 1	–20	–7	–3	mA
CHG Ouput Current	Driving Logic Low and V_O = 1V	40	70	100	µA
	Driving Logic High and V_O = VDD – 1V	–20	–7	–3	mA
State Transitions					
Normal to Overcharge	UCC3957-1	4.15	4.20	4.25	V
Overcharge to Normal	UCC3957-1	3.95	4.00	4.05	V
Normal to Overcharge	UCC3957-2	4.20	4.25	4.30	V
Overcharge to Normal	UCC3957-2	4.00	4.05	4.10	V
Normal to Overcharge	UCC3957-3	4.25	4.30	4.35	V
Overcharge to Normal	UCC3957-3	4.05	4.10	4.15	V
Normal to Overcharge	UCC3957-4	4.30	4.35	4.40	V
Overcharge to Normal	UCC3957-4	4.10	4.15	4.20	V
Undercharge to Normal		2.5	2.6	2.7	V
Normal to Undercharge		2.2	2.3	2.4	V
OV to CHG Delay	(Note 1)	10	17	23	ms

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VDD = 16V and –20°C < T_A < 70°C, T_A = T_J. All voltages measured with respect to the AN4 terminal.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
State Transitions (continued)					
UV to DCHG Delay	(Note 1)	10	17	23	ms
Cell Sample Rate	(Note 1)	5	8.5	11.5	ms
Smart Discharge Threshold	BATLO Voltage	12	15	20	mV
Wakeup Input Threshold	With Respect to VDD	50			mV
Charge Enable Input Threshold		0.8	1.3	2.6	V
Short Circuit Protection					
First Tier Threshold Level	V_{BATLO}	120	150	180	mV
Second Tier Threshold Level	V_{BATLO}	300	375	450	mV
First Tier Blanking Time	CDLY1 = 0.1µF	30	50	70	ms
Restart Time	CDLY1 = 0.1µF	300	500	700	ms
Second Tier Blanking Time	CDLY2 = 10pF	200	400	550	µs

Note 1: Tested at probe only.
Note 2: Other OV/UV thresholds are available. Please consult the factory.

PIN DESCRIPTIONS

AN1: Connects to the negative terminal of the top battery cell and the positive terminal of the second battery cell.

AN2: Connects to the bottom terminal of the second battery cell and the top terminal of the third battery cell.

AN3: Connects to the bottom terminal of the third battery cell and the top terminal of the fourth battery cell in a four cell stack. In a three cell pack it connects to the bottom terminal of the third battery and to AN4.

AN4: Connects to the bottom terminal of the battery stack and the top of the current sense resistor.

AVDD: Internal analog supply bypass cap pin. Connect a 0.1µF capacitor between this pin and AN4. This pin is nominally 7.3V.

BATLO: Connects to the bottom of the current sense resistor and the negative terminal of the battery pack.

CHGEN: The charge enable input for the protection IC. This point must be driven high to allow charging of the battery pack. This pin has a very weak pulldown.

CDLY1: Delay control pin for the short circuit protection feature. A capacitor connected between this point and AN4 will determine the time delay from when an overcurrent situation is detected to when the FET is turned off. This capacitor also controls the hiccup mode timeout period.

CDLY2: An external cap can be tied between this pin and AN4 to extend the blanking time on the second current limit tier.

CLCNT: This pin programs the IC for three or four cell operation. Tying this pin low (to AN4) sets four cell operation, while tying it high (to VDD or the preferred DSPLY or ASPLY) sets three cell operation. This pin is internally pulled low, so open circuit conditions will always result in four cell mode.

DCHG: This pin is used to prevent overdischarge. If the state machine indicates that any cell is undervoltage, this pin will be driven high with respect to chip substrate so that the external P-channel MOSFET will prevent further discharge. If all cell voltages are above the minimum threshold, this pin will be driven low.

CHG: This pin is used to control an external N-channel MOSFET, which in turn drives a P-channel MOSFET. If at least one cell voltage is over the OV threshold, this pin will be driven low with respect to AN4. If all cell voltages are below this threshold, this pin will be driven high.

DVDD: Internal digital supply bypass capacitor pin. Connect a 0.1µF capacitor between this pin and AN4. This pin is nominally 7.3V.

VDD: Supply voltage to the IC. Connect this point to the top of the lithium-ion battery stack.

WU: This pin is used to provide a wake up signal to the IC during sleep mode. Connect this pin to the drain of the N-channel level shift MOSFET.

APPLICATION INFORMATION

Overview

The UCC3957 provides complete protection against over-discharge, over-charge and overcurrent for a three or four cell Lithium-Ion battery pack. It uses a "flying capacitor" technique to sample the voltage across each battery cell and compare it to a precision reference. If any cell is in over or under-voltage, the internal state machine takes the appropriate action to prevent further charge or discharge. High-side P-MOSFETs are used to independently control charge and discharge current. Typical application circuits are shown in Figures 1 and 2.

Connecting the Cell Stack

When connecting the cell stack to the circuit, it is important to do it in the proper order. First, the bottom of the stack should be connected to AN4 . Next, the top of the stack should be connected to VDD. The cell taps can then be connected to AN1-AN3 in any order.

Choosing Three or Four Cells

For three cell packs, the cell count pin (CLCNT) should be connected to the DSPLY pin, and the AN3 pin should be tied to the AN4 pin. For four cell applications, the CLCNT pin should be grounded (to AN4) and the AN3 pin will be connected to the positive terminal of the bottom cell in the stack.

Under-voltage Protection

When any cell is found to be over-discharged (below the Normal to Undercharge threshold), the state machine turns off both high-side FETs and enters the sleep mode, where current consumption drops to about 3.5uA. It remains in sleep mode until the application of a charger is sensed by the Wake Up (WU) pin being raised above VDD.

Charging

Once a charger has been applied, the Charge FET will be turned on as long as the Charge Enable input (CHGEN) is pulled up to the DSPLY pin. If the CHGEN input is left open (or connected to AN4), the Charge FET will remain off.

During charge, the Discharge FET will be off (current will be conducted through its body diode) until the cell voltages are all above the Undercharge to Normal threshold. Once the cell voltages are above this threshold, the Discharge FET will be turned on, minimizing power dissipation.

Open Wire Protection

The UCC3957 provides protection against broken cell sense connections within the pack. If the sense connection to one of the cells (pins AN1, 2 or 3) should become disconnected, weak internal current sources will make the cells connected to that wire appear to be in overcharge and charging of the pack will be prevented.

Over-voltage Protection and the "Smart Discharge" Feature

If any cell is charged to a voltage exceeding the Normal to Overcharge threshold, the Charge FET will be turned off, preventing further charge current. Hysteresis keeps the Charge FET off until the cell voltages have dropped below the Overcharge to Normal threshold. In most protector designs, the Charge FET is held off completely within this voltage band. During this time, discharge current must be conducted through the body diode of the Charge FET. This forward voltage drop can be as high as 1V, causing significant power dissipation in the Charge FET and wasting precious battery power.

The UCC3957 has a unique "Smart Discharge" feature that allows the Charge FET to come back on (for discharge only) while still in the overcharge hysteresis band. This greatly reduces power dissipation in the Charge FET. This is accomplished by sensing the voltage drop across the current sense resistor. If this drop exceeds 15mV (corresponding to 0.6 amps of discharge current using a .025 sense resistor), the Charge FET is turned back on. This threshold assures that only discharge current will be conducted. In an example using a 20mΩ FET with a 1V body diode drop and a 1 amp load, the power dissipation in Q1 would be reduced from 1 watt to 0.02 watts. Note that a similar technique is not used during charge (when the Discharge FET is off due to cells being in undervoltage) because the charge current should be low while the cells are in undervoltage.

Protection Against a Runaway Charger

The use of a small N-channel level shifter (Q3 in the application diagrams) allows the IC to interface with the high-side Charge FET (Q1), even in the presence of a runaway charger. Only the drain-source voltage rating of the charge FET limits the charge voltage that the protection circuit can withstand. The Wakeup (WU) pin is designed to handle input voltages greater than VDD, as long as the current is limited. In the examples shown, the Charge FET's gate-source resistor (R1) provides this current limiting. Note that in Figure 2, a resistor and zener (R2 and VR1) have been added to protect Q1 against any possibility of a voltage transient exceeding its maximum gate-source rating.

Overcurrent Protection

The UCC3957 protects the battery pack from an overload or a hard short circuit using a two-tier overcurrent protection scheme. The overcurrent protection is de-

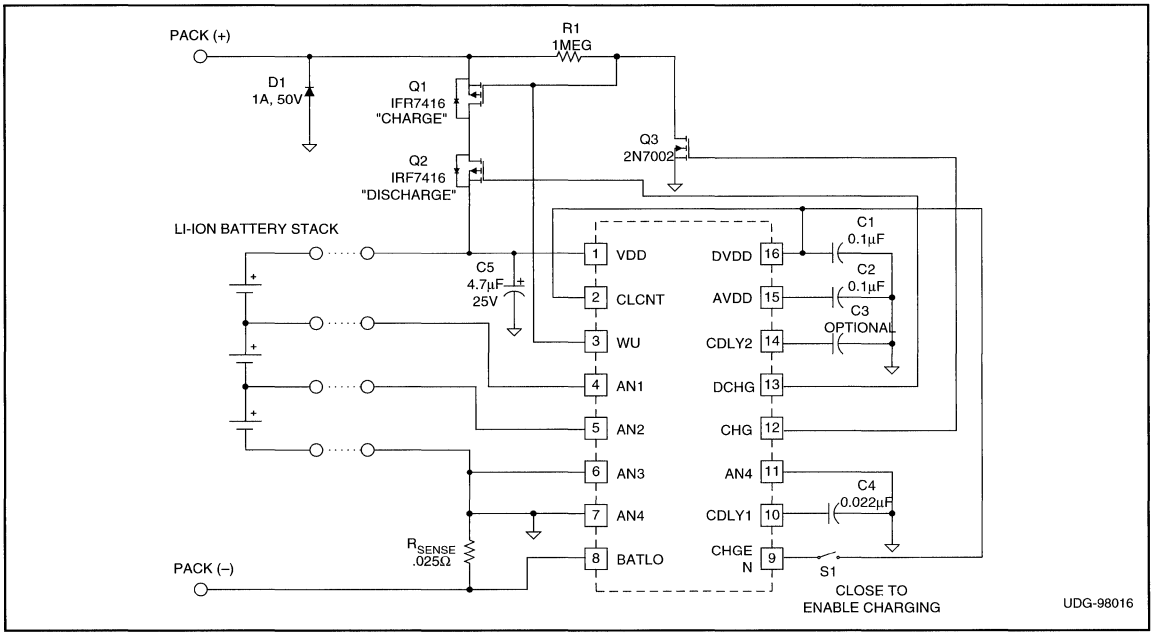


Figure 1. Three cell lithium-ion protector application diagram, showing optional charge enable switch.

Note: D1 protects Q2 from inductive kick at turn-off.

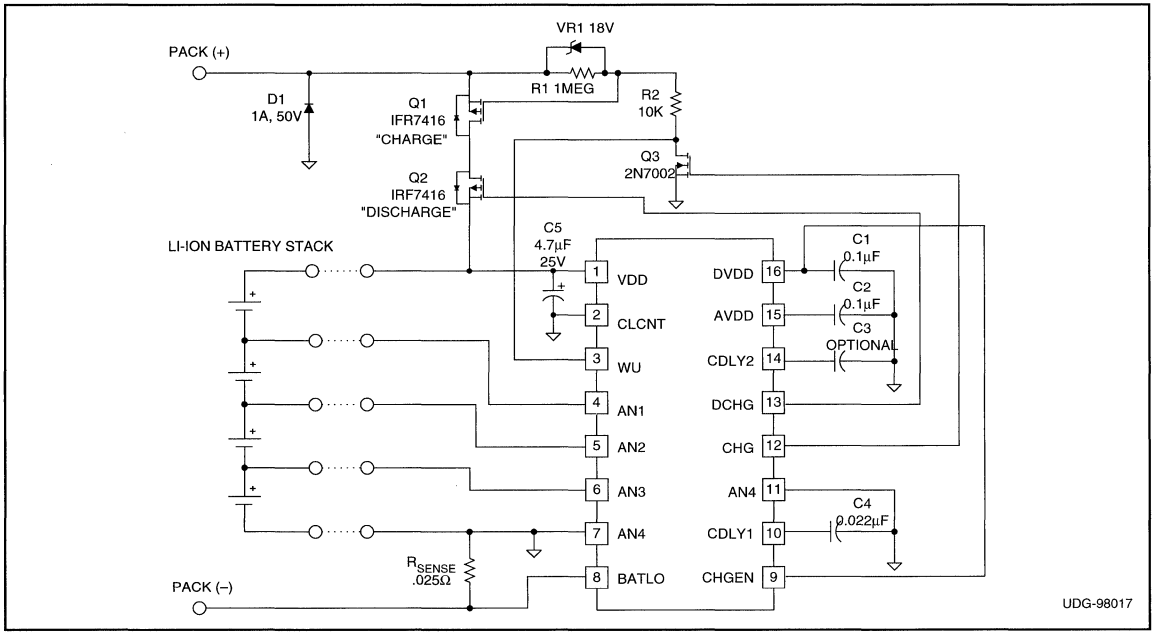


Figure 2. Four cell protector with optional components to protect the charge FET from excessive gate-source transients.

Note1. VR1 and R2 are optional. They protect Q1 from excessive open-circuit charger voltage.

Note 2. D1 protects Q2 from inductive kick at turn-off.

APPLICATION INFORMATION (continued)

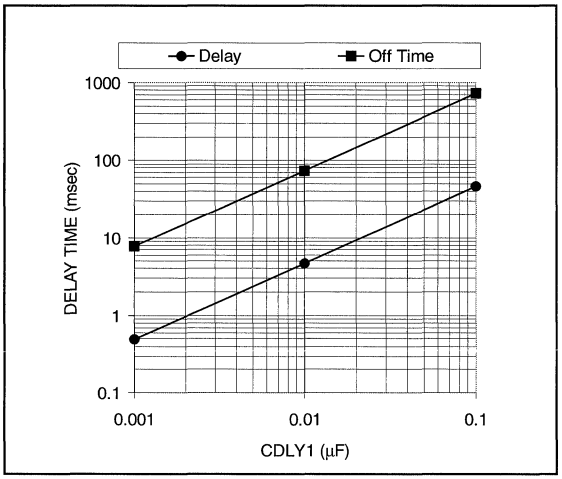


Figure 3. Typical tier 1 Overcurrent delay time and off time vs. CDLY1.

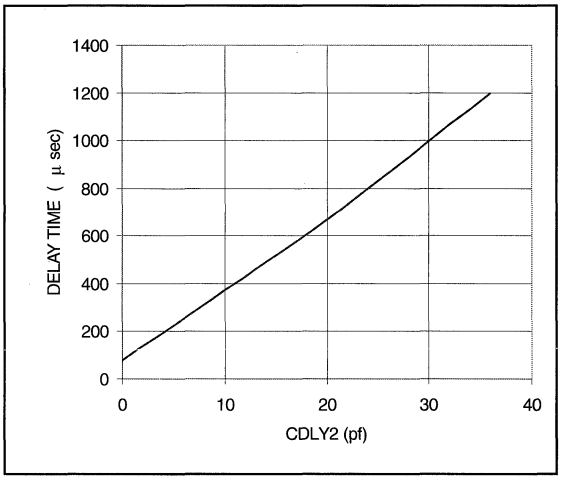


Figure 4. Typical tier 2 Overcurrent delay time vs. CDLY2.

signed to go into a hiccup mode when the voltage drop across an external sense resistor (connected to the AN4 and BATLO pins) exceeds a certain threshold. In this mode, the Discharge FET is periodically turned off and on until the fault is removed. Once the fault is removed, normal operation is automatically resumed.

To facilitate charging large capacitive loads, there are two overcurrent threshold voltages, each with its own user programmable time delay. This two-tier approach provides fast response to short circuits, while enabling the battery pack to provide short duration surge currents. It also facilitates the charging of large filter caps without causing nuisance overcurrent trips.

The first tier threshold is 150mV nominal, corresponding to 6 amps using a .025 sense resistor as shown in the examples of Fig's 1 & 2. If the pack discharge current exceeds this amount for a period of time, determined by the capacitor on the CDLY1 pin, then the hiccup mode will be entered. The first tier hiccup duty cycle is fixed at approximately 6%, minimizing power dissipation in the event of a sustained overload. The absolute on and off times of the Discharge FET (Q2) are controlled by the CDLY1 capacitor. A curve relating the delay (on) time to this capacitor value is shown in Figure 3. The off time is approximately 17 times longer than the on time.

The second tier overcurrent threshold is nominally 375mV, corresponding to 15 amps using a .025 sense resistor. If the pack current exceeds this value for a period of time, determined by the capacitor on the CDLY2 pin, then the hiccup mode will be entered with a much lower duty cycle, typically less than 1%. The relationship of this time delay (on time) to the CDLY2 capacitor value is shown in the curve of Figure 4. The off time during this hiccup mode is still determined by the CDLY1 capacitor, as previously described. This technique greatly reduces the stress and power dissipation in the FETs during short circuit conditions.

In the examples shown in Fig's 1 & 2 (with CDLY1=.022µF), the first tier overcurrent on time will be about 10msec, while the off time will be about 170msec, resulting in a 5.9% duty cycle for currents over 6 amps (but less than 15 amps). If no CLDY2 capacitor is used, the second tier on time will be less than 200µsec (assuming no stray capacitance), resulting in a duty cycle of about 0.1% for currents over 15 amps. If CDLY2=22pF, the typical on time for currents exceeding 15 amps will be about 800usec, resulting in a duty cycle of 0.5%.

Protecting Against Inductive Kick at Turn-off

In the case of a short circuit, the di/dt that occurs when the Discharge FET is turned off can result in a significant voltage undershoot at the pack output due to stray inductance. This undershoot can potentially exceed the breakdown voltage rating of the Discharge FET. A clamp diode (D1 in Fig's 1, 2 & 3), or a capacitor across the pack output, protects against this possibility. A diode also provides protection from a reverse polarity charger.

During turn-off, a voltage overshoot can occur at the top of the cell stack, due to wiring inductance and the cells' internal ESL (Equivalent Series Inductance). During very high di/dt conditions, such as that which occurs when turning off in response to a short circuit, this voltage overshoot can be significant and potentially damage the

APPLICATION INFORMATION (continued)

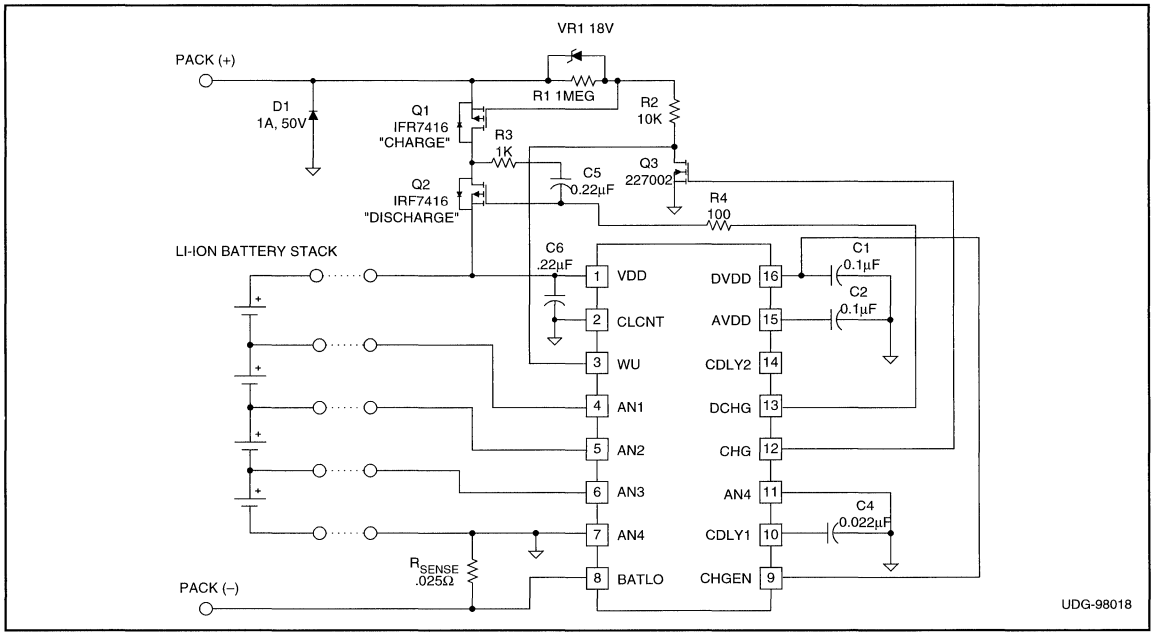


Figure 5. Four cell protector with slew rate limiting the discharge FET.

Note 1: VR1 and R2 are optional. They protect Q1 from excessive open-circuit charger voltage.

Note 2. R3 and C5 are chosen based on capacitive load that must be driven.

Note 3. R4 minimizes inductive kick at turn-off.

IC or the Discharge FET (Q2). For this reason, it is strongly recommended that a capacitor (C5 in Fig's 1 & 2) be placed across the cell stack, from VDD to AN4, and that stray inductance be minimized in the battery current path. An alternative to adding a capacitor across the cell stack is to reduce the di/dt. This is discussed in the next section.

Controlling Discharge FET Turn-on / Turn-off Times

By slew rate limiting the pack output voltage at turn-on, the surge current into large capacitive loads can be greatly reduced.

This allows the designer to select shorter overcurrent delay times, minimizing the stress on Q1 and Q2 in the event of a shorted pack output. A simple method of implementing slew rate limiting is shown in Figure 5. It consists of an RC network (R3 and C5) between gate and drain of the Discharge FET (Q2) to control its turn-on time. This circuit relies on the relatively high sink impedance (about 20K) of the UCC3957's DCHG output. The values shown for R3 and C5 will provide a pack output voltage rise time of about 4.5msec when the Discharge FET (Q2) is turned on. Note that the addition of R3 and C5 has made it possible to eliminate the CDLY2 capacitor, for the quickest response to a true short circuit. While this circuit will not prevent a large surge current when inserting a "live" battery pack into a highly capacitive load, it will allow it to restart (after one hiccup cycle) if this initial surge current trips the overcurrent protection.

Increasing the turn-off time of the Discharge FET (Q2) reduces the inductive kick that results during turn-off after an overcurrent condition. This is accomplished by adding a resistor (R4) in series with the DCHG output. This reduction of di/dt at turn-off will minimize (or eliminate) the need for a capacitor across the battery stack. It is recommended that this resistor value not exceed a few hundred ohms, or the ability to turn off quickly enough into a short may be compromised.

Due to the relatively low charge currents (typically a few amps max), controlling the turn-on and turn-off times of the Charge FET is not beneficial. In fact, the turn-off time of the Charge FET will be slow due to the large value of R1, the gate-source resistor.

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UNITRODE

PRELIMINARY

Single Cell Lithium-Ion Battery Protection Circuit

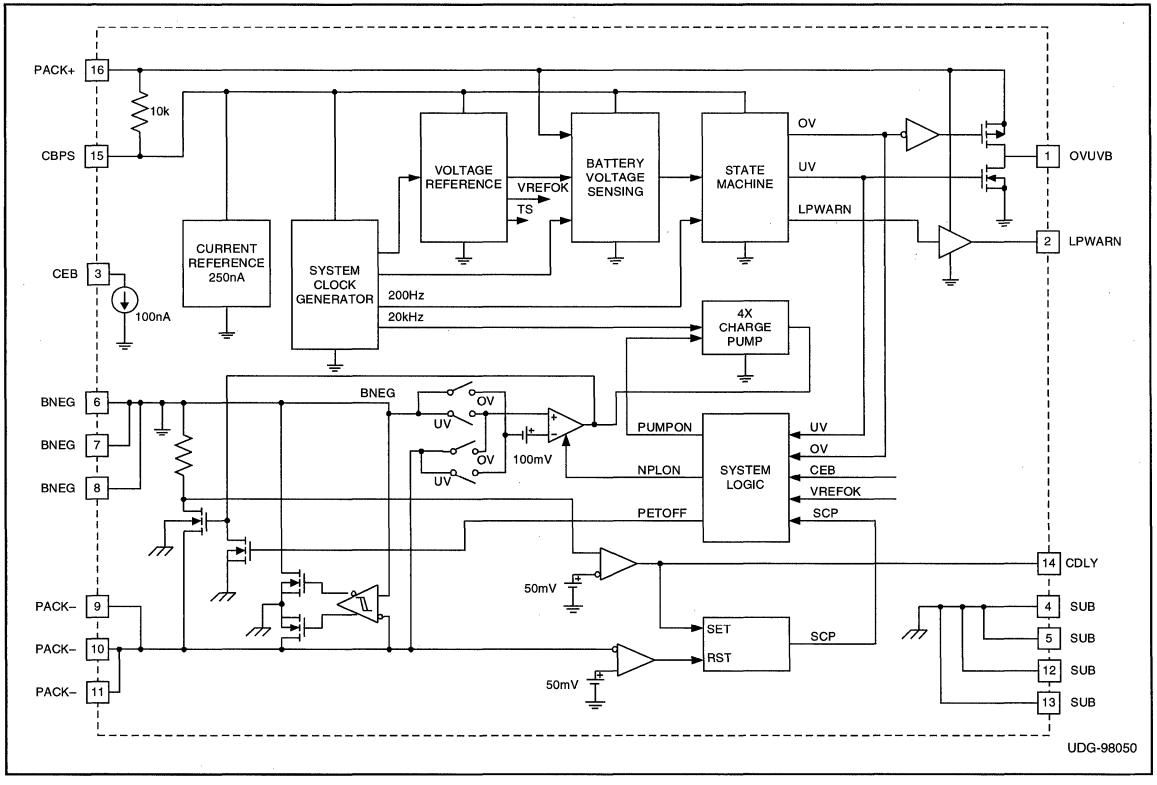
FEATURES

- Protects Sensitive Lithium-Ion Cells Form Over Charging and Over Discharging
- Dedicated for One Cell Applications
- Does Not Require External FETs or Sense Resistors
- Internal Precision Trimmed Charge and Discharge Voltage Limits
- Extremely Low Power Drain
- Low FET Switch Voltage Drop of 150mV Typical for 3A Currents
- Short Circuit Current Protection (with User Programmable Delay)
- 3A Current Capacity
- Thermal Shutdown
- User Controlled Enable Pin

DESCRIPTION

UCC3958 is a monolithic BCMOS lithium-ion battery protection circuit that is designed to enhance the useful operating life of one cell rechargeable battery packs. Cell protection features consist of internally trimmed charge and discharge voltage limits, discharge current limit with a delayed shutdown and an ultra low current sleep mode state when the cell is discharged. Additional features include an on chip MOSFET for reduced external component count and a charge pump for reduced power losses while charging or discharging a low cell voltage battery pack. This protection circuit requires a minimum number of external components and is able to operate and safely shutdown in the presence of a short circuit load.

BLOCK DIAGRAM



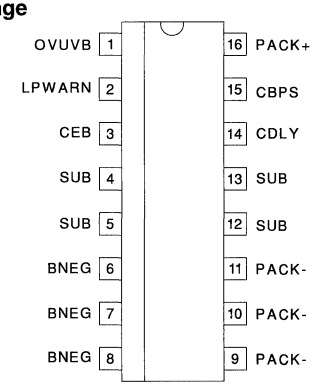
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (PACK+ to BNEG) 7.5V
Maximum Continuous Charge Current 3A
Maximum Charger Voltage (PACK+ to PACK–) 9V
Maximum Reverse Voltage (PACK+ to PACK–) . . . . . –8V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

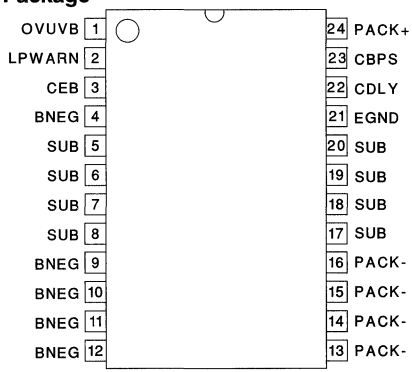
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

SOIC-16 (Top View)
DP Package



TSSOP-24 (Top View)
PWP Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, PACK+ = 4V, –20°C < T_A < 70°C. All voltages measured with respect to BNEG. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
State Transition Thresholds					
NORM to OV (V_{OV})	UCC3958-1	4.15	4.20	4.25	V
OV to NORM (V_{THI})	UCC3958-1	3.85	3.90	3.95	V
NORM to OV (V_{OV})	UCC3958-2	4.20	4.25	4.30	V
OV to NORM (V_{THI})	UCC3958-2	3.90	3.95	4.00	V
NORM to OV (V_{OV})	UCC3958-3	4.25	4.30	4.35	V
OV to NORM (V_{THI})	UCC3958-3	3.95	4.00	4.05	V
NORM to OV (V_{OV})	UCC3958-4	4.30	4.35	4.40	V
OV to NORM (V_{THI})	UCC3958-4	4.00	4.05	4.10	V
NORM to UV (V_{UV})	(Note 1)	2.25	2.35	2.45	V
UV to NORM (V_{TLO})		2.55	2.65	2.75	V
OV, UV Delay Time (T_D)	All Dash Numbers	7	18	34	msec

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, PACK+ = 4V, –20°C < T_A < 70°C. All voltages measured with respect to BNEG. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
BNEG/PACK - SWITCH					
V_{BNEG} - V_{PACK}	NORM, I_{SWITCH} = 2A		–100	–150	mV
	NORM, I_{SWITCH} = –2A		100	150	mV
	V_{PACK+} > V_{OV}, I_{SWITCH} = 20mA to 2A, (OV State)		–100	–300	mV
	V_{PACK+} = 2.5V, I_{SWITCH} = –20mA to –2A, (UV State)		100	600	mV
RDS_{ON}	NORM I_{SWITCH} = 2A		50	75	mΩ
	NORM I_{SWITCH} = –2A		50	75	mΩ
I_{BNEG} – (Charger Leakage Current in OV)	V_{PACK+} > V_{OV} (OV State) ([V_{PACK+}] – [V_{PACK-}]=6V)		1	20	µA
BIAS Current					
I_{PACK+}	V_{PACK+} > V_{UV}		7	20	µA
I_{PACK+}	In Super Low Power Mode (V_{PACK+} < V_{UV})		1	1.5	µA
V_{BAT}	Minimum Operating Cell Voltage			1.5	V
Battery Sample Rate (T_S)		7	12	17	ms
Short Circuit Protection					
ITHLD		2.75	5.25	7.25	A
TDLY	CDLY = 0		350		µs
	CDLY = 100pF (Maximum Recommended Value)		2.5		ms
R_{RESET}	Overcurrent Reset Resistance	7.5			MΩ
LPWARN Output					
LP Warn Threshold		2.55	2.65	2.75	V
TR	C_{LOAD} = 100pF, 10% to 90% of PACK+		280	560	ns
TF	C_{LOAD} = 100pF, 10% to 90% of PACK+		120	280	ns
V_{HIGH} (V_{PACK+} –V_{LPWARN})	I_{SINK} = 200µA, V_{UV} < V_{PACK+} < V_{TLO}		0.3	0.4	V
V_{LOW}	I_{SOURCE} = 200µA, V_{TLO} < V_{PACK+} < V_{UV}		0.3	0.4	V
Measure Delay			6		ms
OVUVB Output					
TR	C_{LOAD} = 100pF, Hi Z to 90% of PACK+		280	560	ns
TF	C_{LOAD} = 100pF, Hi Z to 10% of PACK+		140	280	ns
V_{HIGH} (V_{PACK+} – V_{OVUVB})	I_{SOURCE} = 200µA, V_{PACK+} ≥ V_{OV}		0.3	0.4	V
V_{LOW}	I_{SINK} = 200µA, V_{PACK+} ≤ V_{UV}		0.3	0.4	V
Z_{OUT}	Output Tristated		10		MΩ
Measure Delay			18		ms
CE Input					
I_{SINK}			150		nA

Note 1: Other threshold voltages are available.

PIN DESCRIPTIONS

BNEG: Connect the negative terminal of the battery to these pins.

CBPS: This power supply bypass pin is connected to PACK+ through an internal 10k resistor. An external capacitor must be connected between this pin and BNEG. This capacitor functions as temporary charge storage for high current conditions (short circuit). Minimum capacitor value is 0.15µF. This value should be increased if the CDLY cap is used.

CDLY: Delay control pin for the short circuit protection feature. A capacitor connected between this pin and the BNEG pin will increase the time delay for sensing an over current condition. This adjustment may be useful in those applications where high peak load currents may momentarily exceed the protection circuit's threshold and interruption of the battery current would be undesirable. The nominal delay time is set internally at 350µs

CEB: Chip Enable Bar. This pin is pulled low (wrt BNEG) by a 100nA current source. In order to disable the IC, the user must pull this pin high to PACK+.

LPWARN: Low Power Warning Indicator. This pin is forced high when the battery voltage drops below V_{TLO} (nominally 2.65V). This pin will stay high until the detected battery voltage goes above V_{TLO}, or UV condition is declared.

OVUVB: This pin is an overvoltage/undervoltage condition indicator. Under normal operating conditions this pin is tristated. When an overvoltage (OV) state is detected, this pin is pulled high. When undervoltage (UV) condition is detected, this pin is pulled low.

PACK+: Connect to the positive terminal of the battery. This pin is available to the user.

PACK-: These pins should be connected to the negative terminal of the battery pack (negative terminal available to the user). The internal FET switch connects this terminal to the BNEG terminal to give the battery pack user appropriate access to the battery. In an overcharged state, only discharge current is permitted. In an overdischarged state, only charge current is permitted.

SUB: Do not connect. These pins must be electrically isolated from all other pins. These pins may be soldered to isolated copper pads for heatsinking. This will improve heat transfer, which may be necessary at high load currents.

APPLICATION INFORMATION

Battery Voltage Monitoring

The battery cell voltage is sampled every 12ms by connecting a resistor divider across it and comparing the resulting voltage to a precision internal reference voltage. Under normal conditions (cell voltage is below Over Voltage threshold and above Under Voltage threshold), the UCC3958 consumes approximately 7µA of current and the internal MOSFET is turned on with an R_{DSON} of 50mΩ. The UCC3958 contains an on-chip Charge Pump to ensure that the internal MOSFET gate is driven high for complete turn-on, reducing power losses. The charge pump switches and capacitors are all internal.

When the cell voltage falls below the Under Voltage threshold for two consecutive samples, the IC disconnects the load from the battery pack and enters a super low power mode (nominally 1µA). The pack will remain in this state until it detects the application of a charger, at which point controlled charging is enabled. The requirement of two consecutive readings below the UV threshold filters out momentary drops in cell voltage due to load transients, preventing nuisance trips.

If the cell voltage exceeds the Over Voltage threshold for two consecutive samples, charging is disabled, however discharge current is still allowed. This feature of the IC is explained further in the section on Controlled Charge/ Discharge Mode.

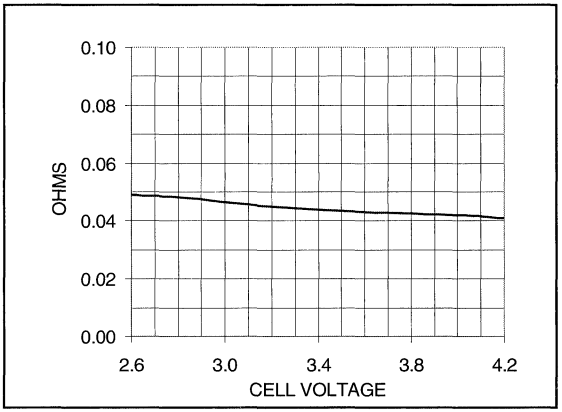


Figure 1. Typical Rdson vs Cell Voltage (DP Package Pin 7 to Pin 10, at 25°C, 1 Amp Load)

APPLICATION INFORMATION (continued)

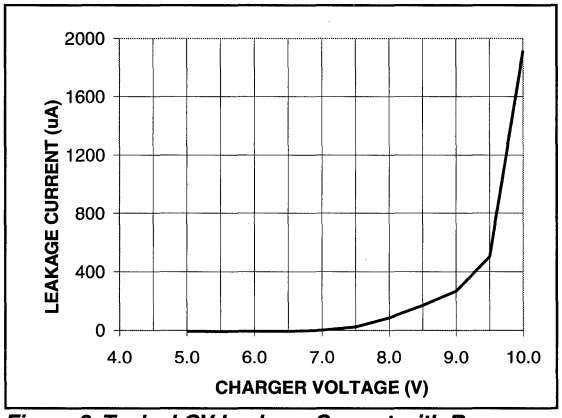


Figure 2. Typical OV Leakage Current with Runaway Charger at 25°C

Over Current Monitoring and Protection

Discharge current is continuously monitored via an internal sense resistor. In the event of excessive current, an Over Current condition is declared if the high current state persists for over 350µs. This delay allows for charging of the system bypass capacitors without tripping the overcurrent. A delay of 350µs guarantees that the pack can charge up to 680µF without declaring an Over Current condition. The delay may be extended to charge larger load capacitors by connecting an external delay capacitor from the CDLY pin to one of the BNEG pins.

Once an Over Current condition has been declared, the internal MOSFET turns off. The only way to return the pack to normal operation is to remove the load by unplugging the pack from the system. The overcurrent is reset when an internal pull down brings PACK– to within less than 0.05V above BNEG. At this point, the pack returns to its normal state of operation. A capacitor on the CBPS pin provides momentary holdup for the UCC3958 to assure proper operation in the event that a hard short suddenly pulls the cell voltage below the minimum operating voltage. This cap value can be 0.15µF if the optional CDLY capacitor is not used. An internal 10k resistor buffers the bypass capacitor from the Li-Ion cell.

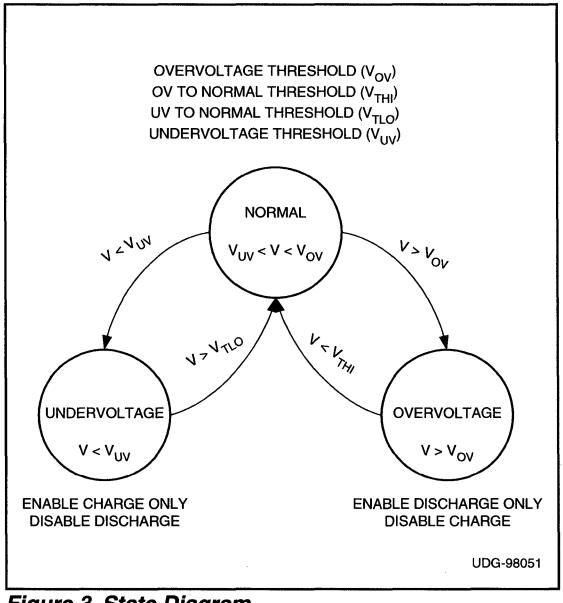


Figure 3. State Diagram

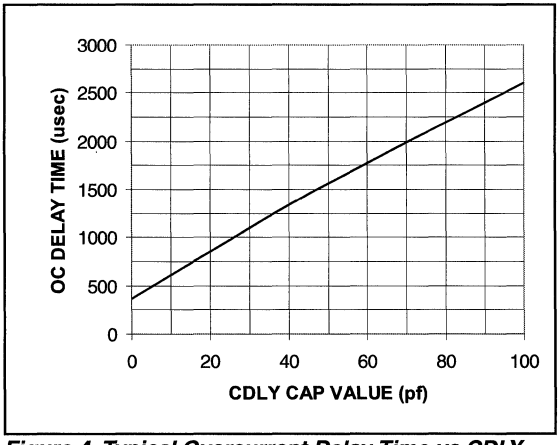


Figure 4. Typical Overcurrent Delay Time vs CDLY

System Status Indicators

The UCC3958 provides several convenient system monitoring signals. The first one is the Low Power Warning. This output goes high when the cell voltage is less than 300mV above the Under Voltage Threshold. It signals the system that the battery is getting close to its discharge limit.

The second monitoring signal is a tri-statable OV/UV output. Under normal operations conditions, this signal is tri-stated. When an Over Voltage condition is declared, the output is pulled high. When an Under Voltage condition is declared, the output is pulled low. This signal is especially useful during test, allowing easy verification of the OV and UV thresholds. These outputs are with respect to BNEG.

APPLICATION INFORMATION (continued)

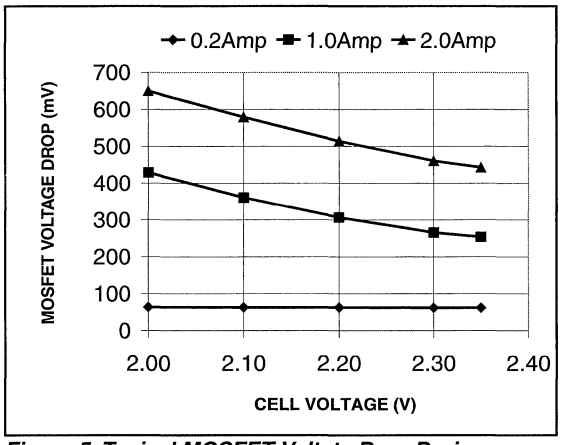


Figure 5. Typical MOSFET Voltate Drop During Charge in UV vs. Cell Voltage.

Controlled Charge/Discharge Mode

When the chip senses an over-voltage condition, it prevents any additional charging, but allows discharge. This is accomplished by activating a linear control loop which controls the gate of the MOSFET based on the differential voltage across its drain to source terminals. The linear loop attempts to regulate the differential voltage across the MOSFET to 100mV. When a light load is applied to the part, the loop adjusts the impedance of the MOSFET to maintain 100mV across it. As the load increases, the impedance of the MOSFET is decreased to maintain the 100mV control. At heavy loads (still below "over-current" limit level), the loop will not maintain regulation and will drive the gate of the MOSFET to the battery voltage (not the charge-pump output voltage). The MOSFET R_{DSON} in the over-voltage state will be slightly higher than R_{DSON} during normal operation. The voltage drop (and associated power loss) across the internal MOSFET in this mode of operation is lower than the typical solution of two external back-to-back MOSFETs, where the body diode is conducting.

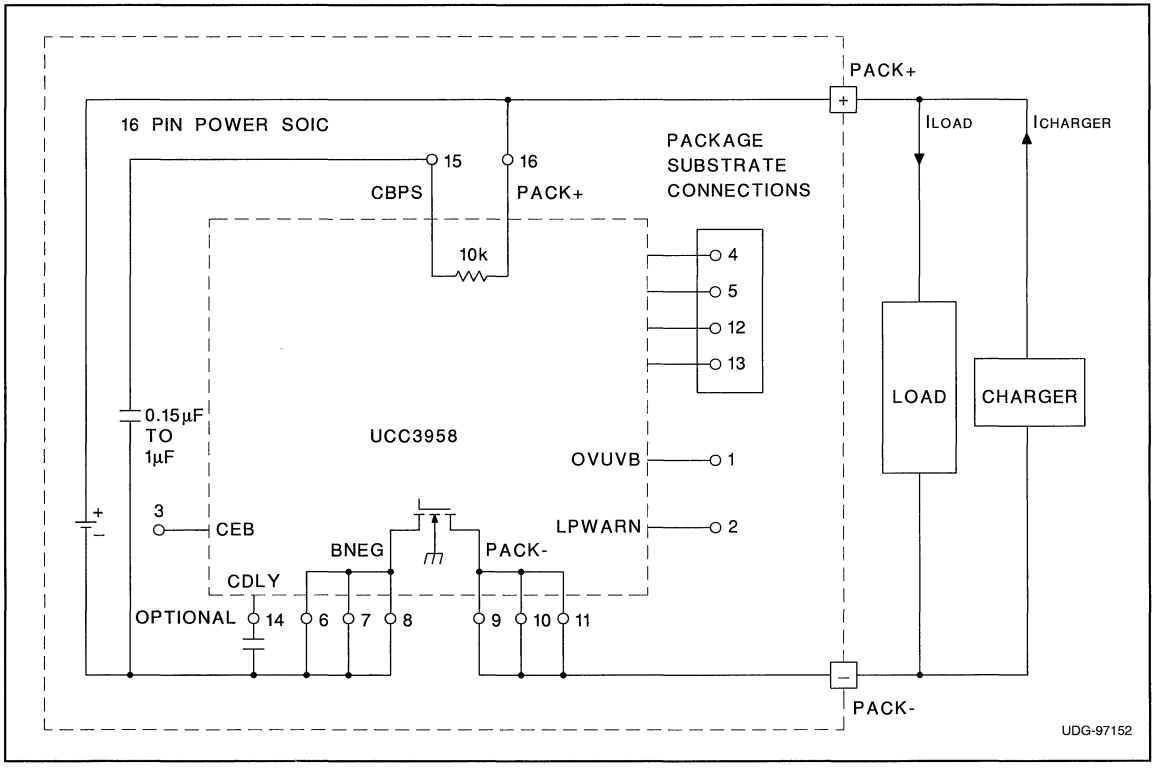


Figure 6. SIngle Cell Lithium-Ion Battery Protector IC Application Diagram

APPLICATION INFORMATION (continued)

When the chip senses an under-voltage condition, it disconnects the load from the battery pack and shuts itself down to minimize current drain from the battery. Several circuits remain powered and will detect placement of the battery pack into a charger. Once the charger presence is detected, the linear loop is activated and the chip allows charging current into the battery. This linear control mode of operation is in effect until the battery voltage reaches a level 300mV above the under-voltage threshold, at which time normal operation is resumed.

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Design Note

UCC3911 Demonstration Board

The UCC3911 demo board comes fully assembled, ready to test. It provides complete over-charge/over-discharge protection, as well as short circuit protection, for two Lithium-Ion cells. The user needs only to supply the two cells (or two power supplies) and a load (or a charger).

The board has been made approximately the size that would fit into a battery pack. The values selected for C1, C2 and CDLY will allow the charging of approximately 1500µf of load capacitance without tripping the overcurrent. This can be changed by the user if desired. Refer to the application section for more details.

The demo board schematic with the high current paths is shown in Figure 1. A parts list is given in Table 1. Note that test pads are provided for monitoring the KILL, OV, UV and LPWARN outputs, if desired.

Connecting the Cells

It is recommended that the Cell1(-) connection be made first, then the Cell2(+) connection. Pads for soldering to the battery tabs are provided on the back side of the board. They are labeled as Cell2 (+) and Cell1(-). This allows the board to sit right on top of the cells, eliminating the resistance and inductance associated with wiring. In addition, large plated through holes with the same labels are provided for attaching wires to an alternate power source, such as two adjustable lab supplies. The connection from the board to the middle of the two cells is made using the small plated through hole connected to R2, near the center of the board. This connection should be made after the other two, and can be done using a small wire, as the current is extremely low.

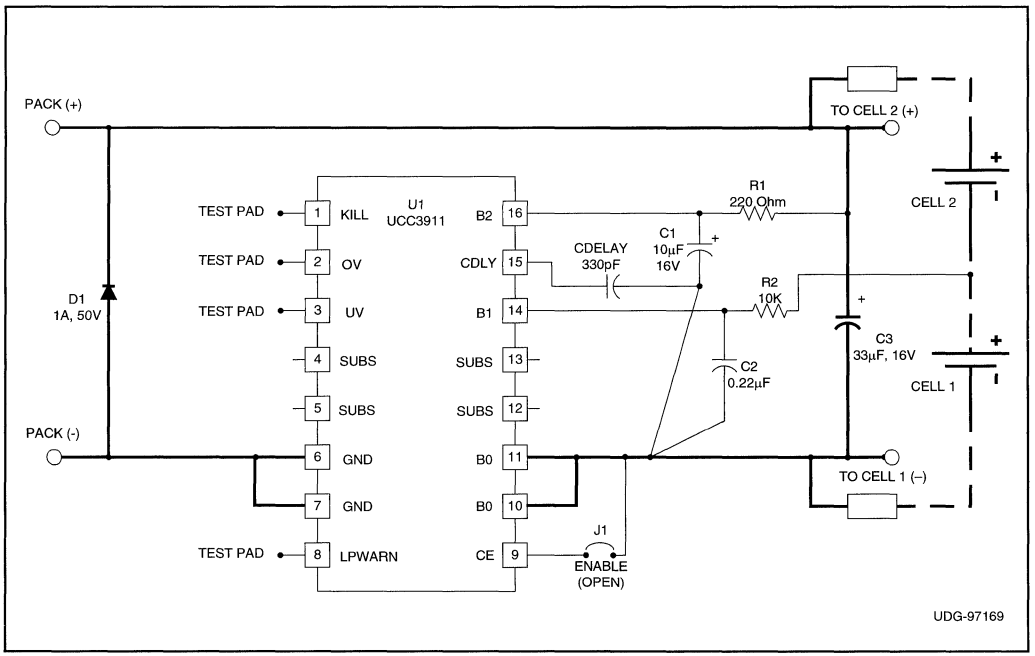

Figure 1. Demo Board Schematic

Capacitor C3 is required to assure a low supply impedance at the IC. This helps to mitigate the effects of battery ESR and ESL on circuit performance. This is especially important under short circuit conditions, where large di/dt's may otherwise cause a "rebound" or overshoot at turn-off.

Connecting the Load or Charger

The load (or Li-Ion charger) is connected to the circuit using the large plated through holes labeled Pack(+) and Pack(-).

Initializing & Enabling the IC

The UCC3911 may be disabled by placing a shorting jumper in the J1 location. This keeps the internal FET off, preventing charge or discharge of the cells, by holding the CE pin low. This also resets the "kill" latch and initializes the state machine. The circuit is enabled when the jumper is removed. The demo boards are shipped without the jumper in place. To initialize the IC, it is necessary to momentarily bridge the J1 pads after the cells are connected. When the jumper is removed, the circuit will be enabled. This only needs to be done once. To re-enable the IC after an overcurrent (or undervoltage) shutdown, momentarily connect the Pack output to a charger.

UCC3911 APPLICATION INFORMATION

While the UCC3911 is capable of providing overload and over and undervoltage protection of both cells with virtually no external parts, the demands of true short circuit protection require some passive external components. These are discussed in detail below.

Referring to Figure 1, diode D1 acts as a clamp across the battery pack output terminals to prevent damage to the IC from inductive kick when the pack current is shut off due to an overcurrent or over/undervoltage condition. It also provides reverse polarity protection during charge.

To prevent a momentary cell voltage drop, caused by large capacitive loads, from causing an erroneous undervoltage shutdown, an RC filter is required in series with the two battery sense inputs, B1 and B2. The resistors (R1 and R2) are sized to have a negligible impact on voltage sensing accuracy. The capacitors (C1 and C2) should be sized to provide a time constant longer than the overcurrent delay time. In the example of Figure 1, they are sized for a nominal 2.2msec time constant. They do not need to be low ESR style caps, as they see no ripple current. A larger resistor value and smaller cap value can be used on the B1 input due to the extremely low input current on this pin. (Note: the 5uA current listed in the data sheet for B1 is for test purposes. The current in this pin is guaranteed by design to be much less than 1uA.)

The overcurrent delay capacitor, C_{DELAY}, is discussed in the data sheet. This cap sets the time delay introduced before turning off the UCC3911's internal FET, after the overcurrent threshold is exceeded. If no capacitor is used, the nominal delay is 100μsec. To charge large capacitive loads without tripping the overcurrent circuit, a small cap (typically less than 1000pF) is used to extend the delay time. The approximate delay time is given below and shown graphically in Figure 2.

$$T_{DELAY}(\mu\,\text{sec}) = 25 + (25 + C_{DLY}(pf)) \bullet 0.4 \bullet V_{BATT}$$

The amount of time required will be a function of the load capacitance, battery voltage, and the total circuit impedance, including the internal resistance of the cells, the UCC3911's on resistance, and the load capacitor ESR. The required delay time can be calculated from:

$$T = -R \bullet C \bullet \ln\left(\frac{I \bullet R}{V}\right)$$

In this equation, R is the total circuit resistance, C is the capacitor being charged, I is the overcurrent trip current (5.25 Amps nominal), and V is the battery voltage. Using the minimum trip current of 3.5 Amps and the maximum battery voltage of 8.4V, the worst case maximum delay time required is defined as:

$$T_{MAX}(\mu\,\text{sec}) = -R \bullet C(\mu f) \bullet \ln\left(\frac{R}{2.4}\right)$$

In the example of Figure 1, Cdelay, C1 and C2 are sized to drive a 1500μF load capacitor. If large capacitive loads (or other loads with surge currents above the overcurrent trip threshold) are not being applied to the pack terminals, the overcurrent delay time can be short. In this case, it may be possible

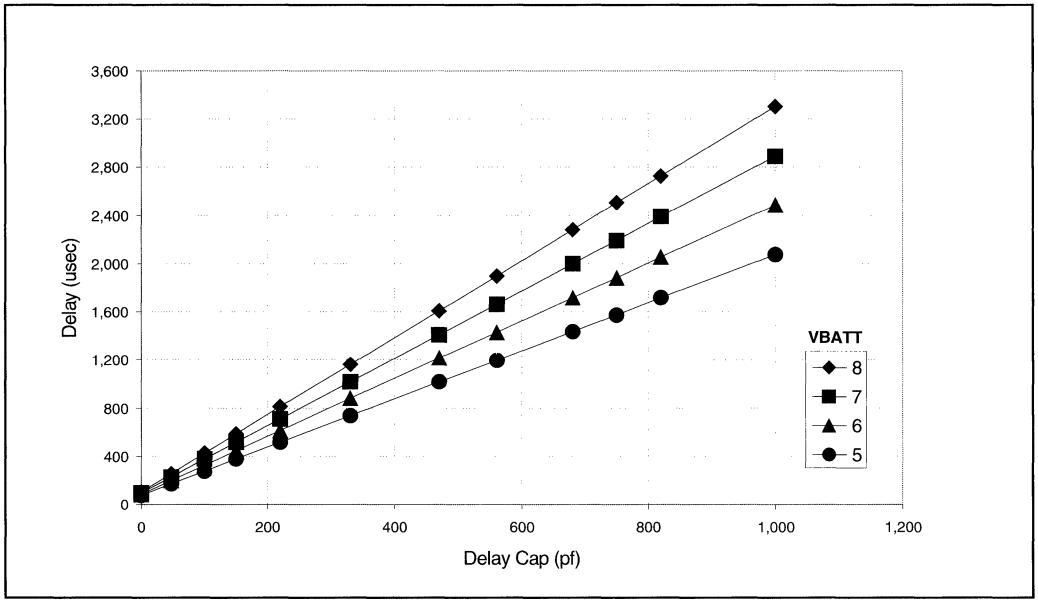

Figure 2. Nominal Overcurrent Delay Time vs. CLDY and VBATT

to eliminate Cdelay, as well as R2 and C2 altogether (replacing R2 with a short). In addition, the time constant of R1 and C1 can be made much shorter. R1 and C2 are still necessary, however, to assure proper operation under short circuit conditions. It is important to maintain a minimum R1/C1 time constant of 100μsec. (For example, R1 and C1 could be reduced to 100 Ohms and 1μF.)

Capacitor C3 prevents excessive overshoot at turn-off due to parasitic inductance. This is especially true under short circuit conditions, when a very high di/dt will occur at turn-off. A minimum of 22μf is recommended. It should be placed close to D1's cathode and pins 10 and 11 of the UCC3911.

Jumper J1, while in place, keeps the UCC3911 inhibited (pack output open). The jumper is removed or cut as the last step in manufacturing the battery pack to enable the output.

The four substrate pins (4, 5, 12, 13) may be soldered to electrically isolated copper pads to aid in heat transfer when operating at high load currents.

For more complete information, pin descriptions and specifications for the UCC3911, please refer to the datasheet or contact your Unitrode Field Applications Engineer.

Reference Designator	Part Description	Part Value	Manufacturer	Part Number
C1	Tantalum Capacitor	10μF, 16V, "B" Case	Sprague	595D106X0016B2T
C2	Ceramic Capacitor	0.22μF, 16V, 0805 Case	AVX	0805YC224KAT
C3	Tantalum Capacitor	33μF, 16V, "C" Case	AVX	TAJC336K016R
CDLY	Ceramic Capacitor	330pF, 50V, 0805 Case	COG	
D1	Fast Recovery Diode	1A, 50V, SMB Case	Diodes, Inc.	FR1A
R1	Metal Film Resistor	220Ω, 1/10W, 5%, 0805 Case		
R2	Metal Film Resistor	10KW, 1/10W, 5%, 0805 Case		
U1	Two Cell Protector IC		Unitrode	UCC3911

Table 1. Parts List

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Design Note

UCC3958 Demonstration Board Schematic and Bill of Materials

The UCC3958 demo board is designed to provide complete over-charge, under-charge and overload/short circuit protection for a single Lithium-ion cell. The schematic and parts list of the demo board are shown on the following page.

The over-current delay capacitor, CDLY, is optional and not installed on this demo board. The nominal internal over-current delay time of 360μsec is adequate for charging capacitive loads of up to 1000μF. If desired, the delay time can be extended by adding a small ceramic cap for CDLY. A graph of the over-current delay time as a function of cap value is given below.

Note that the bypass/energy storage capacitor (C1) supplied with the demo board is a 1μF tantalum. This provides more than enough energy storage to power U1 during a shorted pack condition, even with an extended over-current delay time. If the delay time is not extended, a smaller value of capacitor can be used for C1.

For more complete information, pin descriptions and specifications for the UCC3958, please refer to the datasheet or contact your Unitrode Field Applications Engineer.

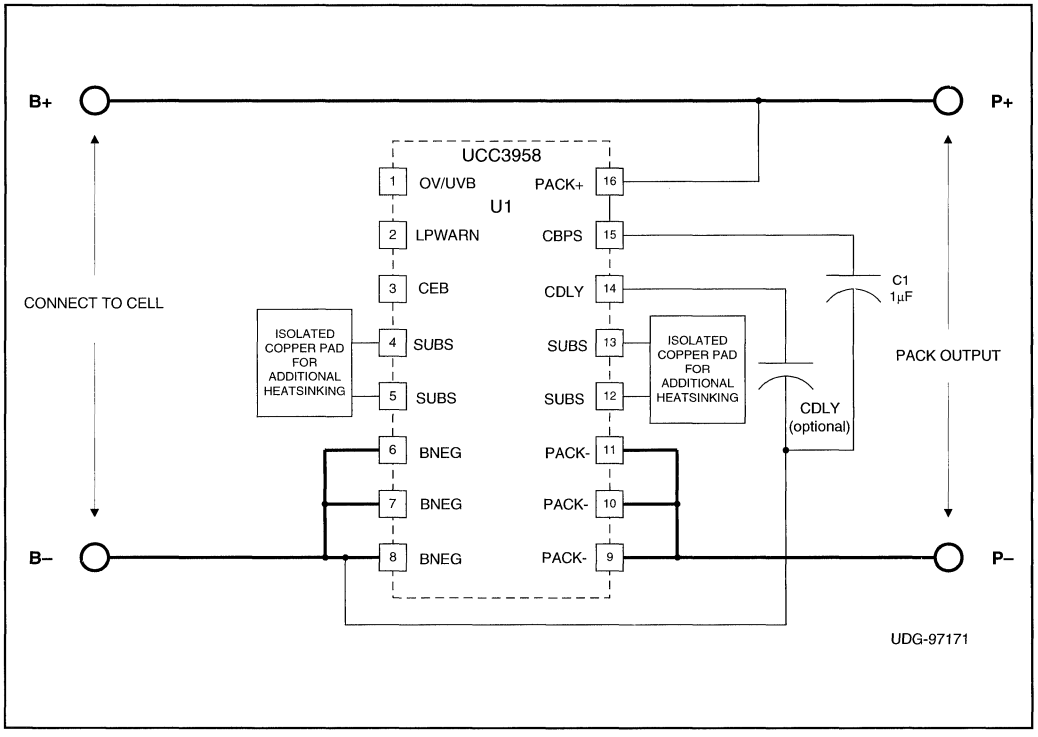

Figure 1. UCC3958 Demonstration Board Schematic

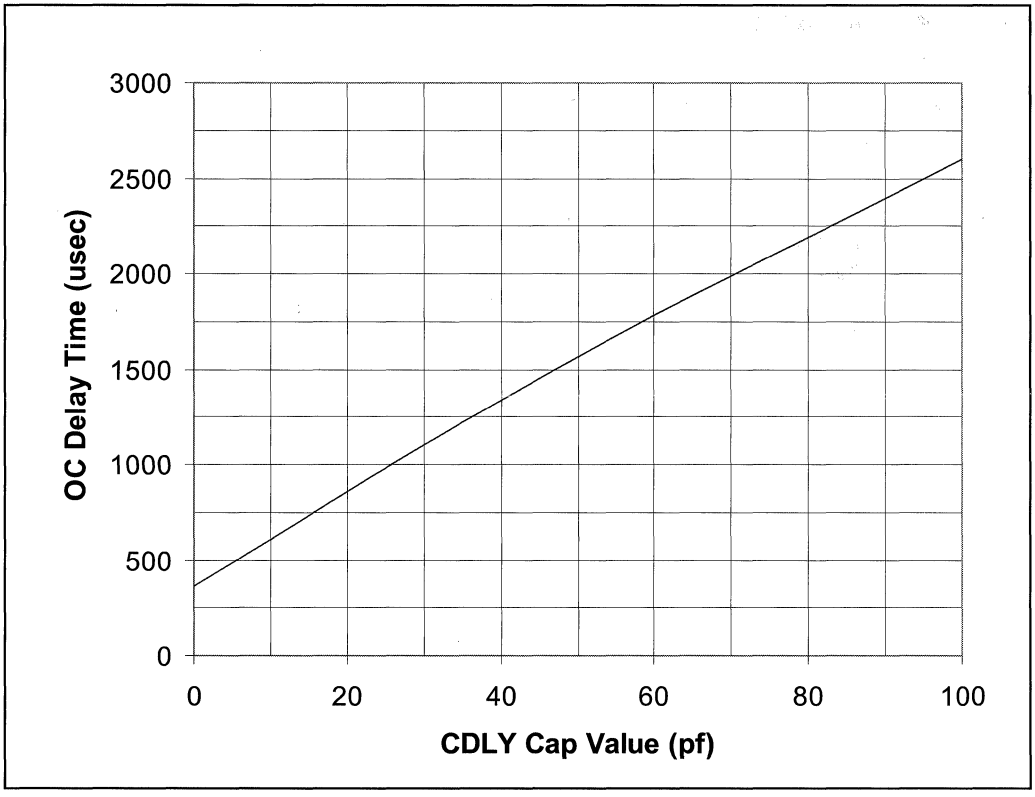

Figure 2. Nominal Overcurrent Delay Time vs. CDLY

Reference Designator	Part Description	Part Value	Manufacturer	Part Number
U1	Protector IC	Single cell Li-Ion	Unitrode	UCC3958
C1	Tantalum Capacitor	16V	Panasonic	ECS-T1CY105R

Table 1. Demo Board Parts List

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UCC3957 Three - Four Cell Lithium-Ion Protector Circuit, Evaluation Board and List of Materials

INTRODUCTION

The UCC3957 demo board is supplied fully assembled and ready to test. This board offers overcharge, over discharge and overcurrent protection for a 3 or 4 cell lithium ion battery pack. The user needs to supply the battery pack, load and charger. As supplied, the demo board should not be used with a cell stack that can supply more than 40A of short circuit current. This is due to limitations of the high side P-FETS used. See the data sheet for the IRF7416 for more information.

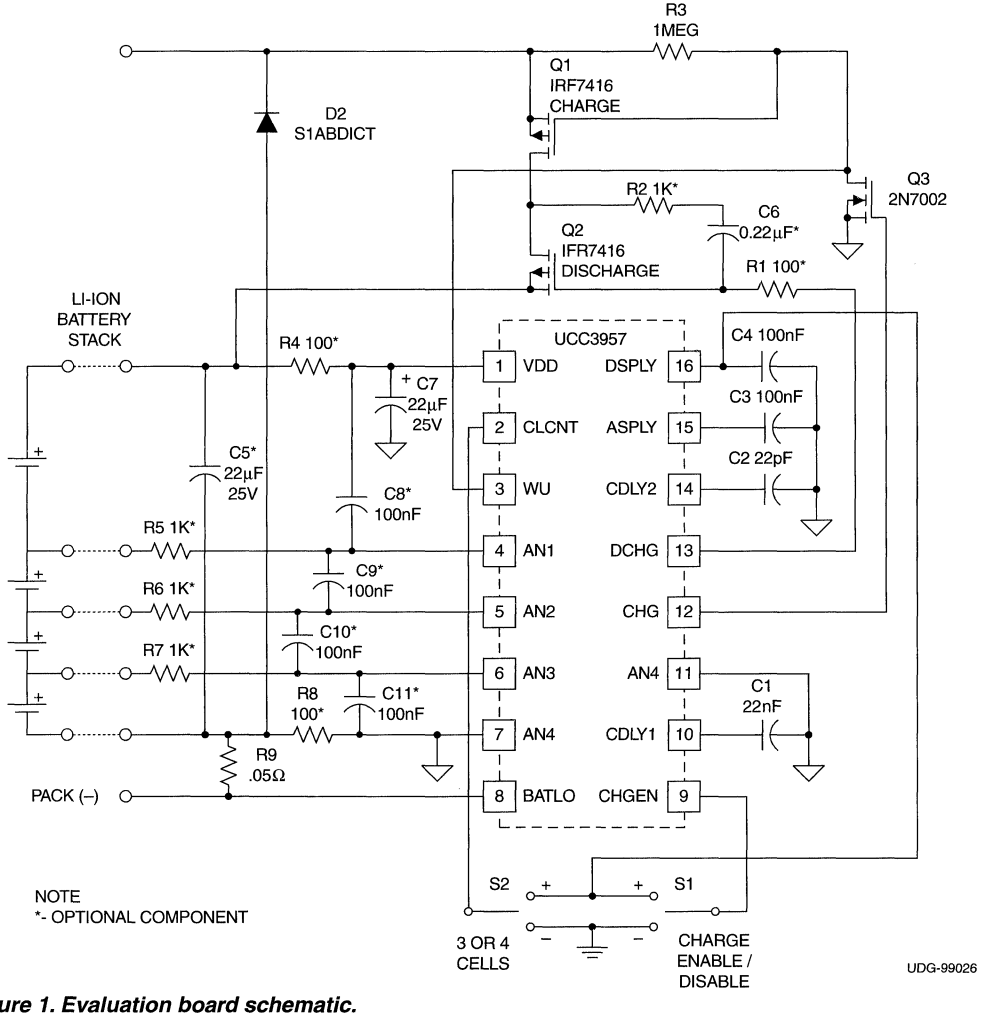

Figure 1. Evaluation board schematic.

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The board allows user control over battery pack cell count, and whether or not charging will be allowed. S1, see Fig. 1, determines whether or not charging will be allowed. When the switch is moved to the (+) position, the voltage at DVDD will be applied to the CHGEN pin and charging will be allowed to take place. If this switch is moved to the (–) position, the CHGEN pin will be grounded and charging will be disabled. A possible application of this feature is to fabricate the charger and battery pack in such a way that the CHGEN pin is shorted to DVDD only when the battery pack is in the charger, and not in the device being powered. This would allow a device to have multiple battery packs installed in parallel without risk of high circulating current due to one pack being almost fully charged and another depleted.

S2 determines whether or not the chip is in 3 cell or 4 cell mode. Moving S2 to the (+) position connects the CLCNT pin to DVDD, placing the chip in 3 cell mode. When the demo board is used in this mode, AN3 must be shorted to AN4 (GND) on J1.

CONNECTING THE BOARD

Fig. 2 shows the proper connections for both a three cell and a four cell pack to a load and/or charger. The circuit may come up in an under-voltage state. To make the pack operational in this case, it will be necessary to connect the PACK(+) terminal to a current limited voltage source, and bring it to a voltage that is a little higher than the VDD terminal.

Battery Stack Wire Length

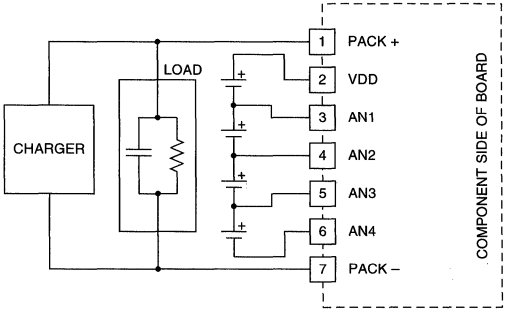
The current carrying wires to the battery stack (VDD and AN4), and the inter-cell connections should be short to minimize inductive effects when the protector circuit interrupts a large current. Excessively long wires can generate a voltage spike that may damage the circuit. C5's function is to control this spike for reasonable inductance in the wiring to the battery stack. In an actual pack, C5 may be unnecessary. R1 is used to slow the turn-off of the discharge FET and limit dI/dt caused voltage spikes. The wires from the battery stack to the AN1, AN2 and AN3 terminals should be short as well to minimize noise pickup.

Connection Order and Optional Components

The connection order for the battery stack is not important in the demo board. Resistors R5, R6 and R7 limit current flow and prevent damage to the IC. In a production environment, these three resistors are NOT required if the cells are connected in the proper order. The proper connection order (without R5 - R7) is:

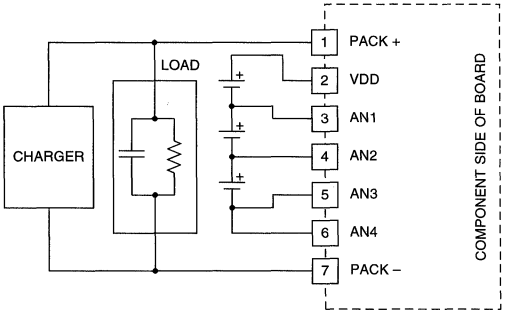
1. AN4 or VDD
2. VDD or AN4
3. AN1 through AN3 in any order.

C8, C9, C10 and C11 are not installed on the board as supplied. Their purpose is to provide some noise filtering capability for extremely noisy applications. Noise filtering may reduce or eliminate false OV or UV indications when a cell in the pack is nearing one of these thresholds. Note that the use of C8 - C11 WILL DISABLE the open sense wire detection capability of the UCC3957.



4 CELL CONNECTION S2 IN NEGATIVE (–) POSITION

UDG-98169



3 CELL CONNECTION S2 IN POSITIVE (+) POSITION

UDG-98170

Figure 2. Evaluation board connection diagrams.

When the PACK+ and PACK–terminals are shorted together, VCC for the chip collapses. In order to insure that the UCC3857 has enough stored energy available to turn off the discharge FET, the main supply de-coupling capacitor, C7, is de-coupled from the PACK+ to PACK– current path by an additional 100Ω resistor. On the demo board, this resistor can be either R4 or R8. As supplied, R8 is installed, and R4 is a short circuit. The reason that this is done is to allow the ground of the UCC3957 to "ride" transients caused by interruption of large currents by some means other than the discharge FET. This keeps the ground of the UCC3957 "fixed" in relation to the external FET's (Q1 and Q2), and prevents possible damage from exceeding the maximum rated gate-source voltage. This type of transient can occur when inserting a battery pack into a device that has a large bulk capacitor. If the contacts bounce a little bit upon insertion, large di/dt's can occur, giving rise to large transient voltages from stray inductances in the circuit.

LOAD VOLTAGE SLEW RATE LIMIT

Components R2 and C6 are the primary components used for limiting the load voltage rate of rise, and are optional. A positive change in the load voltage causes a current to flow in capacitor C6. This current will be forced into the DCHG pin on the UCC3957. Since this pin has a sink impedance of about 14K, the load dV/dt will be limited to a value that produces a current in C6 that causes the voltage at DCHG to be the battery stack voltage less the threshold voltage on the DCHG FET (Q2). R2 is primarily a damping resistor to prevent oscillations, and to limit current in the DCHG pin during transients. In practice the rate of rise is approximately:

$$\frac{dV}{dt} = \frac{V_{BATTERY} - V_{THRESH}}{14000 \bullet C_5} \; V/\text{sec}$$

Where:

- $V_{BATTERY}$ is the battery stack voltage
- V_{THRESH} is the threshold voltage of the discharge FET
- C_5 is in Farads

The nice thing about this circuit is that it allows the protection circuit to charge a capacitive load without tripping the overcurrent protection mechanism in the UCC3957. This allows a much lower setting for overcurrent (i.e. larger value for R9), a reduction in 2nd tier overcurrent delay time, or both.

The drawback to this circuit is that it will cause the discharge FET to go through a slow linear transition when the circuit is hiccuping into a fault. This causes the FET to get very warm if the condition persists. In extreme cases, the FET will fail. When using this circuit, it is imperative that the system operation and integrity be verified. The demo board is supplied with pads for these components, but without the components installed. If this circuit is used, some resistance (R1 or R2) is required to limit current drawn from the DCHG pin. The reason for this is as follows: When the battery pack is disconnected from a load and is not in an under-voltage state, the DCHG pin is held at GND or AN4, and C6 is charged to the battery voltage. When the pack is then connected to a capacitive load, the junction of Q1-drain, Q2-drain and R2 is taken to GND. Since the voltage across C6 cannot change instantaneously, the gate of the discharge FET is pushed below GND. If there is no impedance to limit the current drawn out of the DCHG pin, the UCC3957 could be damaged.

Table 1. UCC3957 evaluation board list of materials.

Reference Designator	Description	Manufacturer	Part Number
R1(2), R4(1), R8(2)	100Ω, 1/8W Metal film resistor, 1206 case		
R2(1), R5(2), R6(2), R7(2)	1.00KΩ, 1/8W Metal film resistor, 1206 case		
R3	1.00MΩ, 1/8W Metal film resistor, 1206 case		
R9	50mΩ, IRC type LR2512, 1W		
C1	22nF, 50V Ceramic Capacitor	Panasonic	ECU-V1H223KBM
C2	22pF, 50V Ceramic Capacitor	Panasonic	ECU-V1H220JCM
C3, C4, C8, C9, C10, C11	100nF, 50V Ceramic Capacitor	Murata	GRM42-6X7R104K050BL
C5(2), C7	22µF, 25V Tantalum Capacitor	Panasonic	ECS-T1ED226R
C6(1)	220nF, 50V Ceramic Capacitor	Kemet	C1210C224M5UAC

Table 1. UCC3957 evaluation board list of materials (cont.)

Q1, Q2	30V, 0.020Ω, PFET, IRF7416		
Q3	60V, 115mA NFET, 2N7002		
D2	50V, 1A Diode, S1ADICT		
S1,S2	SPDT Switch	EAO	09-0320102
J1	7 Position Compression Terminal Block	OST	ED1601 (2 req'd)
		OST	ED1602 (1 req'd)
U1	3-4 Cell Lithium-Ion Protector	Unitrode	UCC3957

Notes:
(1) - Optional components not installed on board as shipped
(2) - Optional component installed on board as shipped

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Design Note

UCC3952 Demonstration Board Schematic and List of Materials

INTRODUCTION

The UCC3952 demo board provides complete protection for a single Lithium-ion cell, including Overcharge, Over-discharge and short circuit protection. The application schematic is shown in Fig. 1 and a component placement is shown in Fig. 2. A list of materials, giving the component part numbers and case sizes is given in Table 1. Note that the UCC3952, using an internal MOSFET switch, requires only a single external decoupling capacitor to provide a complete protection solution.

DEMO BOARD FEATURES

Small (5.5mm x 22.5mm) two sided board with only two components.
Integrated low impedance MOSFET switch and current sensor (50mΩ typical)
Overcharge protection, with built-in 1.5 second time delay (typical)
High accuracy 1.0% tolerance on Overcharge threshold (over temperature)
Four standard Overcharge thresholds are available (4.20, 4.25, 4.30 4.35V)
Over-discharge protection, with built-in 15msec time delay (typical)
Overload/short circuit protection with built-in 1.5msec time delay (typical)
Automatic recovery from short circuit when load is removed
Reverse charger protection (up to –8V)
Runaway charger protection (up to +16V)
Overtemp protection
Low operating current of 5 A (typical)
Low Sleep mode current of 1.5 A (typical)

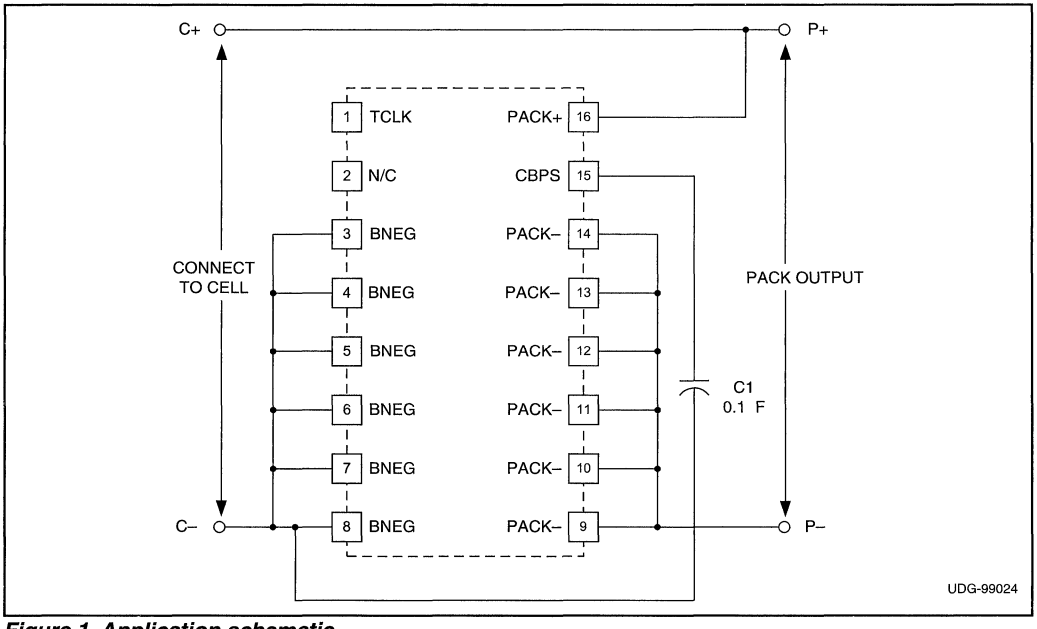

Figure 1. Application schematic

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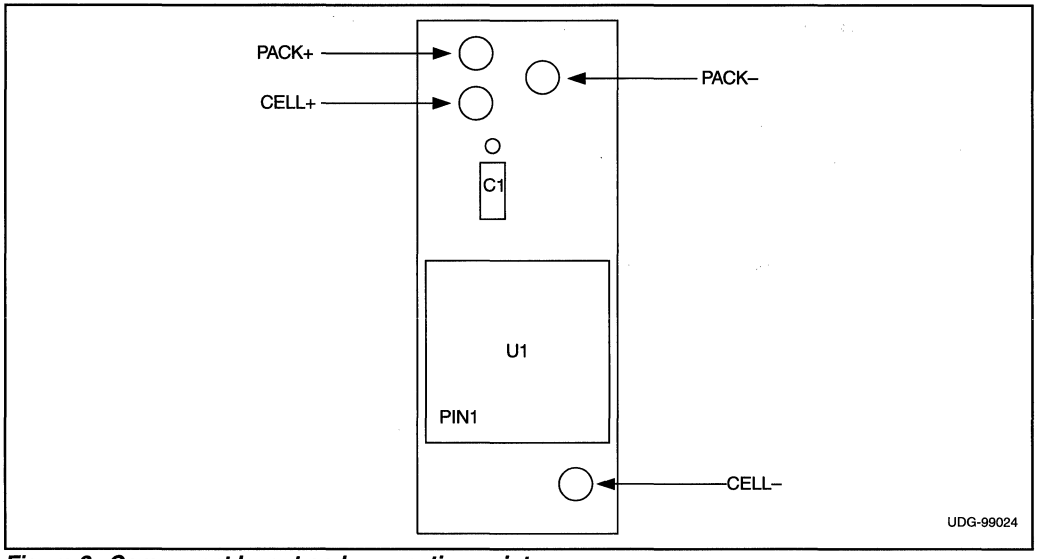

Figure 2. Component layout and connection points.

Table I. UCC3831 Evaluation board list of materials

Designator	Description	Manufacturer	Part Number
C1	0.1μF, 16V ceramic cap (X7R type), 0805 chip	AVX 0805YC104KAT2A	P5.90KHCT-ND
U1	16 pin TSSOP	UCC3952PW – 1/-2/-3/-4	P412FCT-ND

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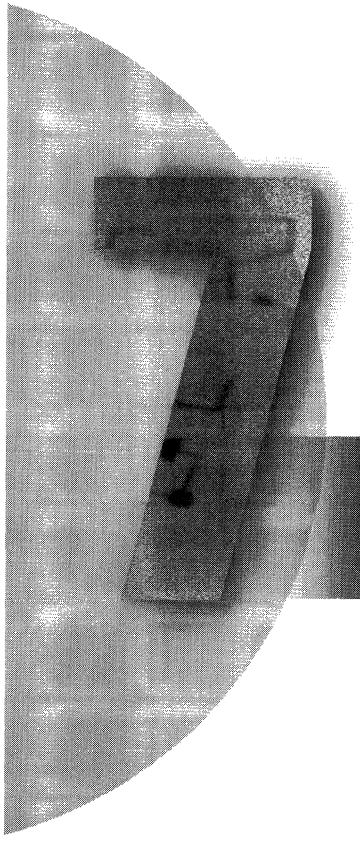


7

Power-Management ICs

Power-Management ICs Selection Guide

Features	Part Number UCC3581	UCC3809 -1/2	UCC3800/ 1/2/3/4/5	UCC3813- 0/1/2/3/4/5
Topology	Forward, flyback	Forward, flyback, buck, boost	Forward, flyback, buck, boost	Forward, flyback, buck, boost
Input voltage	Off-line AC	Off-line AC	Off-line AC, battery	Off-line AC, battery
Output voltage	NA	NA	NA	NA
Operating mode	Fixed/variable frequency	Fixed frequency (1MHz maximum)	Fixed frequency (1MHz maximum)	Fixed frequency (1MHz maximum)
Output	1A FET drives	0.8A FET drives	1A FET drives	1A FET drives
Output power	N / A	N / A	N / A	N / A
Supply current	300µA	500µA	500µA	500µA
Power limit	Yes	No	Yes	Yes
Application/design note	DN-48, DN-65	DN-65, DN-89, U-165, U-168	DN-42A, DN-43, DN-46, DN-48, DN-54, DN-56A, DN-65, DN-89, U-133A, U-97	DN-42A, DN-43, DN-46, DN-48, DN-54, DN-56A, DN-65, DN-89, U-133A, U-97
Pin count ❖	14	8	8	8
Page number	PS/8-128	PS/8-192	PS/8-169	PS/8-206

❖The smallest available pin count for thru-hole and surface-mount packages

Features	Part Number UCC39401	UCC3941 -3/-5/-ADJ	UCC39411 /2/3	UCC39421/2	UCC3946	UCC3954
Topology	Boost / battery charger	Boost	Boost	Boost/SEPIC/ flyback	Watchdog/ reset	Flyback
Input voltage	0.8V to (V_{OUT} + 0.5V)	0.8V to (V_{OUT} + 0.5V)	1.1V to (V_{OUT} + 0.5V)	1.8V–8V	2.1V–5.5V	2.5V–4.2V
Output voltage	ADJ to 5.0V	3.3V, 5V, ADJ	3.3V, 5V, ADJ	ADJ	V_{IN}–0.3V	3.3V
Operating mode	Variable frequency	Variable frequency	Variable	Fixed/variable frequency	Watchdog/ reset	Fixed frequency (200kHz)
Output	Internal power FETs	Internal power FETs	Internal power FETs	FET Drives	NA	Internal power FETs
Output power	200mW	500mW (1 cell) 1W (2 cells)	200mW	NA	NA	2W
Supply current	55µA	80µA	48µA	635µA	10µA	1mA
Power limit	Yes	Yes	Yes	Yes	NA	Yes
Application/ design note	-	DN-73	DN-97	-	-	DN-86
Pin count ❖	20	8	8	16/20	8	8
Page number	7-34	7-48	7-58	7-66	7-88	7-93

❖The smallest available pin count for thru-hole and surface-mount packages

Linear Regulation ICs Selection Guide

Linear Controller	Part Number UC3832	UC3833	UC3834	UC3835	UC3836	UCC3837
Type of output	Positive adjustable	Positive adjustable	Positive/ negative adjustable	5V fixed	Positive adjustable	Positive adjustable
Maximum input voltage	36V	36V	40V	40V	40V	12V
Minimum output voltage	2.0V	2.0V	+1.5V / –2.0V		2.5V	1.5V
Output drive	300mA	300mA	350mA	500mA	500mA	1.5mA
Type of short circuit limit	Duty cycle	Duty cycle	Foldback	Foldback	Foldback	Duty cycle
Reference voltage accuracy	2%	2%	3% / 4%	2%	2%	2%
Special features	Multiple pins accessible	-	-	Built-in Rsense	Built-in Rsense	Internal charge pump; Direct N-FET drive
Application/ design note	DN-32, DN-61, U-152	DN-32, DN-61, U-152	U-95			-
Pin count ❖	14, 16	8, 16	16	8, 16	8, 16	8
Page number	PS/3-11	PS/3-11	PS/3-18	PS/3-24	PS/3-24	PS/3-28

❖The smallest available pin count for thru-hole and surface-mount packages.
+ New product.

Low-Dropout Linear Regulator	Part Number UCC381	UC382-1	UC382-2	UC382-3	UC382-ADJ
Output voltage	3.3V, 5V, ADJ	1.5V	2.1V	2.5V	1.2V/ adjustable
Dropout voltage	0.5V at 1A	450mV at 3A	450mV at 3A	450mV at 3A	450mV at 3A
Output voltage accuracy	2.5%	1%	1%	1%	1%
Maximum input voltage	9V	7.5V	7.5V	7.5V	7.5V
Shutdown current	10μA	-	-	-	-
Operating current	400μA	-	-	-	-
Line regulation	0.01% / V	-	-	-	-
Load regulation	0.1%, I_{OUT} = 0 to 1A	-	-	-	-
Special features	Power limit	Fast transient response	Fast transient response	Fast transient response	Fast transient response
Pin count ❖	8	5	5	5	5
Page number	7-5	PS/3-5	PS/3-5	PS/3-5	PS/3-5

❖The smallest available pin count for thru-hole and surface-mount packages.
+ New product.

Linear Regulation ICs Selection Guide

Low Dropout Linear Regulators (Continued)	Part Number UCC383	UCC384	UC385-1	UC385-2	UC385-3
Output voltage	3.3V, 5V, ADJ	5V, 12V, ADJ	1.5V	2.1V	2.5V
Dropout voltage	0.45V at 3A	0.2V at 500mA	450mV at 5A	450mV at 5A	450mV at 5A
Output voltage accuracy	2.5%	2.5%	1%	1%	1%
Maximum input voltage	9V	–16V	7.5V	7.5V	7.5V
Shutdown current	40μA	17μA	-		
Operating current	400μA	240μA	-		
Line regulation	0.01% / V	0.01% / V	-		
Load regulation	0.1%, I_{OUT} = 0 to 1A	0.1%, I_{OUT} = 0 to 500mA	-		
Special features	Power limit	Power limit	Fast transient response	Fast transient response	Fast transient response
Pin count ❖	3	8	5	5	5
Page number	7-12	7-19	PS/3-35	PS/3-35	PS/3-35

❖The smallest available pin count for thru-hole and surface-mount packages.
+ New product.

Low Dropout Linear Regulators (Continued)	Part Number UC385-ADJ	UC386+	UC387+	UC388+
Output voltage	1.2V/adjustable	3.3V	5V	Adjustable down to 1.25V
Dropout voltage	450mV at 5A	0.2V at 200mA	0.2V at 200mA	0.2V at 200mA
Output voltage accuracy	1%	1.5%	1.5%	1.5%
Maximum input voltage	7.5V	9V	9V	9V
Shutdown current	-	2μA	2μA	2μA
Operating current	-	10μA	10μA	10μA
Line regulation	-	25mV max	25mV max	25mV max
Load regulation	-	10mV max	10mV max	10mV max
Special features	Fast transient response	TSSOP	TSSOP	TSSOP
Pin count ❖	5	8	8	8
Page number	PS/3-35	7-29	7-29	7-29

❖The smallest available pin count for thru-hole and surface-mount packages.
+ New product.

Linear Regulation ICs Selection Guide

Special Function Linear Regulators	Part number UC560	UCC561+	UC563+
Type of output	Positive	Positive	Positive
Application	Source/sink regulator for the 18- and 27-line SCSI termination	LVD SCSI regulator for the 18- and 27-line termination	32-line VME bus bias generator
Input voltage	4V-6V	2.7V- 5.25V	4.875V-5.25V
Output voltage	2.85V	1.3V, 1.75V, 0.75V	2.94V
Dropout voltage	0.9V at 750mA	-	-
Bus standard	SCSI-1,2,3	SPI-2, 3	VME / VME64
Sink/source current	300mA / –750mA	200mA / –200mA	475mA / –575mA
Application/design note	-	-	-
Pin count ❖	5, 8	16	3, 8
Page number	IF/4-3	IF/4-7	IF/4-10

❖The smallest available pin count for thru-hole and surface-mount packages.
+ New product.

Low Dropout 1 Ampere Linear Regulator Family

FEATURES

- Precision Positive Linear Voltage Regulation
- 0.5V Dropout at 1A
- Guaranteed Reverse Input/ Output Voltage Isolation with Low Leakage
- Low Quiescent Current Irrespective of Load
- Adjustable Output Voltage Version
- Fixed Versions for 3.3V and 5V Outputs
- Logic Shutdown Capability
- Short Circuit Power Limit of 3% • V_{IN} • Current Limit
- Remote Load Voltage for Accurate Load Regulation

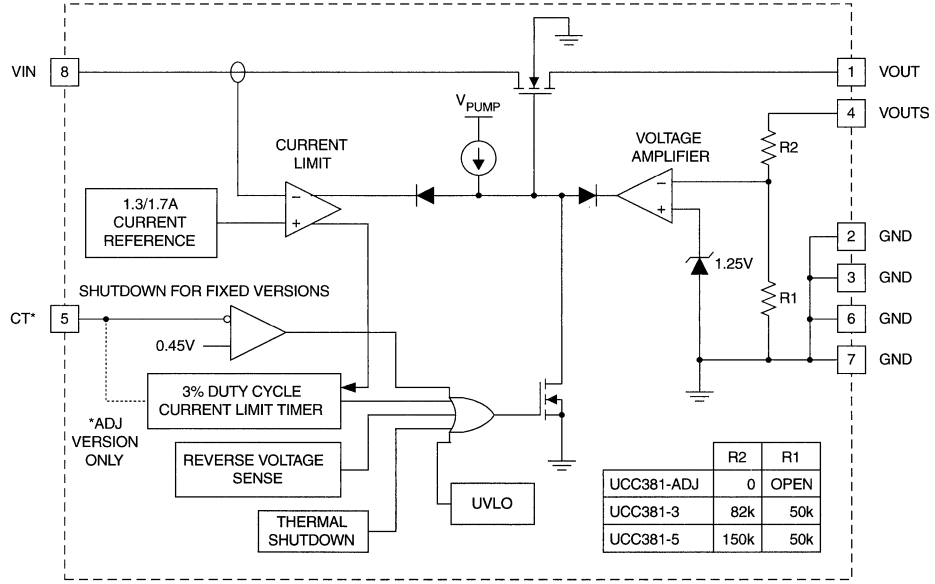
DESCRIPTION

The UCC381-3/-5/-ADJ family of positive linear series pass regulators is tailored for low drop out applications where low quiescent power is important. Fabricated with a BiCMOS technology ideally suited for low input to output differential applications, the UCC381 will pass 1A while requiring only 0.5V of input voltage headroom. Dropout voltage decreases linearly with output current, so that dropout at 200mA is less than 100mV. Quiescent current is always less than 450µA. To prevent reverse current conduction, on-chip circuitry limits the minimum forward voltage to typically 50mV. Once the forward voltage limit is reached, the input-output differential voltage is maintained as the input voltage drops until undervoltage lockout disables the regulator.

UCC381-3 and UCC381-5 versions have on-chip resistor networks preset to regulate either 3.3V or 5.0V, respectively. Furthermore, remote sensing of the load voltage is possible by connecting the VOUTS pin directly at the load. The output voltage is then regulated to 1.5% at room temperature and better than 2.5% over temperature. The UCC381-ADJ version has a regulated output voltage programmed by an external user-definable resistor ratio.

(continued)

BLOCK DIAGRAM



	R2	R1
UCC381-ADJ	0	OPEN
UCC381-3	82k	50k
UCC381-5	150k	50k

UDG-98112

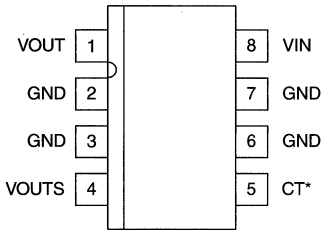
ABSOLUTE MAXIMUM RATINGS

VIN. 9V
CT . . . . . –0.3 to 3V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

CONNECTION DIAGRAMS

SOIC-8 (Top View)
DP Package



** ADJ version only*

DESCRIPTION (cont.)

Short circuit current is internally limited. The device responds to a sustained overcurrent condition by turning off after a T_{ON} delay. The device then stays off for a period, T_{OFF}, that is 32 times the T_{ON} delay. The device then begins pulsing on and off at the T_{ON} /(T_{ON}+T_{OFF}) duty cycle of 3%. This drastically reduces the power dissipation during short circuit such that heat sinking, if at all required, must only accommodate normal operation. On the fixed output versions of the device TON is fixed at 400µs – a guaranteed minimum. On the adjustable version an external capacitor sets the on time. The off time is always 32 times T_{ON}.

The UCC381 can be shutdown to 25µA (max) by pulling the CT pin low.

Internal power dissipation is further controlled with thermal overload protection circuitry. Thermal shutdown occurs if the junction temperature exceeds 165°C. The chip will remain off until the temperature has dropped 20°C.

The UCC281 series is specified for operation over the industrial range of –40°C to +85°C, and the UCC381 series is specified from 0°C to +70°C. These devices are available in the 8 pin DP surface mount power package. For other packaging options consult the factory.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications hold for T_A = 0°C to 70°C for the UCC381-X series and –40°C to +85°C for the UCC283-X series, V_{IN} = V_{OUT} + 1.5V, I_{OUT} = 0mA, C_{OUT} = 2.2µF. C_T = 1500pF for the UCC381-ADJ version and V_{OUT} set to 5V. T_J = T_A.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UCC381-5 Fixed 5V, 1A Family					
Output Voltage	T_J = 25°C	4.925	5	5.075	V
	Over Temperature	4.875		5.125	V
Line Regulation	V_{IN} = 5.15V to 9V		1	3	mV
Load Regulation	I_{OUT} = 0mA to 1A		2	5	mV
Drop Out Voltage, V_{IN} – V_{OUT}	I_{OUT} = 1A, V_{OUT} = 4.85V, TA < 85°C		0.5	0.6	V
	I_{OUT} = 200mA, V_{OUT} = 4.85V, TA < 85°C		100	200	mV
Peak Current Limit	V_{OUT} = 0V		2	3.5	A
Overcurrent Threshold		1		1.8	A
Current Limit Duty Cycle	V_{OUT} = 0V		3	5	%
Overcurrent Time Out, T_{ON}	V_{OUT} = 0V	400	750	1600	µs
Quiescent Current			400	650	µA
Quiescent Current in Shutdown	V_{IN} = 9V		10	25	µA
Shutdown Threshold	At C_T Input	0.25	0.45		V
Reverse Leakage Current	0V < V_{IN} < V_{OUT}, V_{OUT} < 5.1V, at VOUT			75	µA
UVLO Threshold	V_{IN} where V_{OUT} passes current	2.5	2.8	3.0	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications hold for T_A = 0°C to 70°C for the UCC381-X series and –40°C to +85°C for the UCC283-X series, V_{IN} = V_{OUT} + 1.5V, I_{OUT} = 0mA, C_{OUT} = 2.2µF. C_T = 1500pF for the UCC381-ADJ version and V_{OUT} set to 5V. T_J = T_A.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UCC381-3 Fixed 3.3V, 1A Family					
Output Voltage	T_J = 25°C	3.25	3.3	3.35	V
	Over Temperature	3.22		3.38	V
Line Regulation	V_{IN} = 3.45V to 9V		1	3	mV
Load Regulation	I_{OUT} = 0mA to 1A		2	5	mV
Dropout Voltage, V_{IN} - V_{OUT}	I_{OUT} = 1A, V_{OUT} = 3.15V, T_A < 85°C		0.6	0.8	V
	I_{OUT} = 200mA, V_{OUT} = 3.15V, T_A < 85°C		100	200	mV
Peak Current Limit	V_{OUT} = 0V		2	3.5	A
Overcurrent Threshold		1		1.8	A
Current Limit Duty Cycle	V_{OUT} = 0V		3	5	%
Overcurrent Time Out, T_{ON}	V_{OUT} = 0V	400	750	1600	µs
Quiescent Current			400	650	µA
Quiescent Current in Shutdown	V_{IN} = 9V		10	25	µA
Shutdown Threshold	At C_T Input	0.25	0.45		V
Reverse Leakage Current	0V < V_{IN} < V_{OUT}, V_{OUT} < 3.35V, at V_{OUT}			75	µA
UVLO Threshold	V_{IN} where V_{OUT} passes current	2.5	2.8	3.0	V
UCC381-ADJ Adjustable Output, 1A Family					
Regulating Voltage at ADJ Input	T_J = 25°C	1.23	1.25	1.27	V
	Over Temperature	1.22		1.28	V
Line Regulation, at ADJ Input	V_{IN} = V_{OUT} + 150mV to 9V		1	3	mV
Load Regulation, at ADJ Input	I_{OUT} = 0mA to 1A		2	5	mV
Dropout Voltage, V_{IN} - V_{OUT}	I_{OUT} = 1A, V_{OUT} = 4.85V		0.5	0.6	V
	I_{OUT} = 200mA, V_{OUT} = 4.85V		100	200	mV
Peak Current Limit	V_{OUT} = 0V		2	3.5	A
Overcurrent Threshold		1		1.8	A
Current Limit Duty Cycle	V_{OUT} = 0V		3	5	%
Overcurrent Time Out, T_{ON}	V_{OUT} = 0V, C_T = 1500pF	400	1000	1600	µs
Quiescent Current			400	650	µA
Quiescent Current in Shutdown	V_{IN} = 9V		10	25	µA
Shutdown Threshold	At C_T Input	0.25	0.45		V
Reverse Leakage Current	0V < V_{IN} < V_{OUT}, V_{OUT} < 9V, at V_{OUT}			100	µA
Bias Current at ADJ Input			100	250	nA
UVLO Threshold	V_{IN} where V_{OUT} passes current	2.5	2.8	3.0	V

PIN DESCRIPTIONS

CT: For UCC381-3 and UCC381-5 versions, this is the shutdown pin which, when pulled low, turns off the regulator output and puts the device in a low current state. For the UCC381-ADJ version, a capacitor is required between the CT pin and GND to set the T_{ON} time during overcurrent according to the following (typical) equation:

$$T_{ON} = 660{,}000 \bullet C_{CT}$$

GND: All voltages are measured with respect to this pin. This is the low noise ground reference input for regulation. The output decoupling capacitor should be tied to PIN 7.

VIN: Positive supply input for the regulator. Bypass this pin to GND with at least 1µF of low ESR, ESL capacitance if the source is located further than 1 inch from the device.

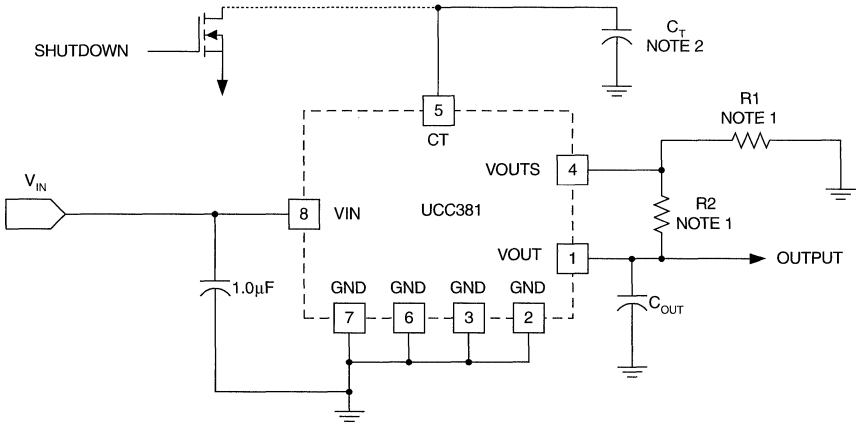
VOUT: Output for regulator. The regulator does not require a minimum output capacitor for stability. Choose the appropriate size capacitor for the application with respect to the required transient loading. For example, if the load is very dynamic, a large capacitor will smooth out the response to load steps.

VOUTS: Feedback for regulator sensing of the output voltage. For loads which are a considerable resistive distance from the VOUT pin, the VOUTS pin can be used to move the resistance into the control loop of the regulator, thereby effectively canceling the IR drop associated with the load path. For local regulation, merely connect this pin directly to the VOUT pin. For the UCC381-ADJ version, the output voltage can be set by two external resistors according to the following relationship:

$$V_{OUT} = 1.25 \bullet \left(1 + \frac{R2}{R1}\right)$$

where R1 is a resistor connected between VOUT and VOUTS and R2 is a resistor connected between VOUTS and GND.

TYPICAL APPLICATION CIRCUIT



Note 1: R1 and R2 for adjustable version only. For 3.3V and 5V versions connect VOUT to VOUTS. See Pin Descriptions.

Note 2: C_T timing capacitor is for adjustable version only. For 3.3V and 5V versions, the CT pin is used to enable or shutdown the part. See Pin Descriptions.

APPLICATION INFORMATION

Overview

The UCC381 family of low dropout linear (LDO) regulators provide a regulated output voltage for applications with up to 1A of load current. The regulator features a low dropout voltage and short circuit protection, making their use ideal for demanding high current applications requiring fault tolerance.

Short Circuit Protection

The UCC381 provides unique short circuit protection circuitry that reduces power dissipation during a fault. When an overload situation is detected, the device enters a pulsed mode of operation at 3% duty cycle reducing the heat sink requirements during a fault. The UCC381 has two current thresholds that determine its behavior during a fault as shown in Fig. 1.

When the regulator current exceeds the **Overcurrent Threshold** for a period longer than the T_{ON}, the UCC381 shuts off for a period (T_{OFF}) which is 32 times T_{ON}. If the short circuit current exceeds the **Peak Current Limit**, the regulator limits the current to peak current limit during the T_{ON} period. The peak current limit is nominally 1 Amp greater than the overcurrent threshold. The regulator will continue in pulsed mode until the fault is cleared as illustrated in Fig. 1.

A capacitive load on the regulator's output will appear as a short circuit during start-up. If the capacitance is too large, the output voltage will not come into regulation during the initial T_{ON} period and the UCC381 will enter pulsed mode operation. The peak current limit, T_{ON} period, and load characteristics determine the maximum value of output capacitor that can be charged. For a constant current load the maximum output capacitance is given as follows:

$$C_{OUT(max)} = (I_{CL} - I_{LOAD}) \bullet \frac{T_{ON}}{V_{OUT}} \ Farads \qquad (1)$$

For worst case calculations the minimum values of on time (T_{ON}) and peak current limit (I_{CL}) should be used. The adjustable version allows the T_{ON} time to be adjusted with a capacitor on the CT pin:

$$T_{ON(adj)}\ (\mu\ sec) = 660{,}000 \bullet C\ (\mu\ Farads) \qquad (2)$$

For a resistive load (R_{LOAD}) the maximum output capacitor can be estimated from:

$$C_{OUT(max)} = \frac{T_{ON}}{R_{LOAD} \bullet \ln\left(\frac{1}{1-\left(\frac{V_{OUT}}{I_{CL} \bullet R_{LOAD}}\right)}\right)} \ Farads \qquad (3)$$

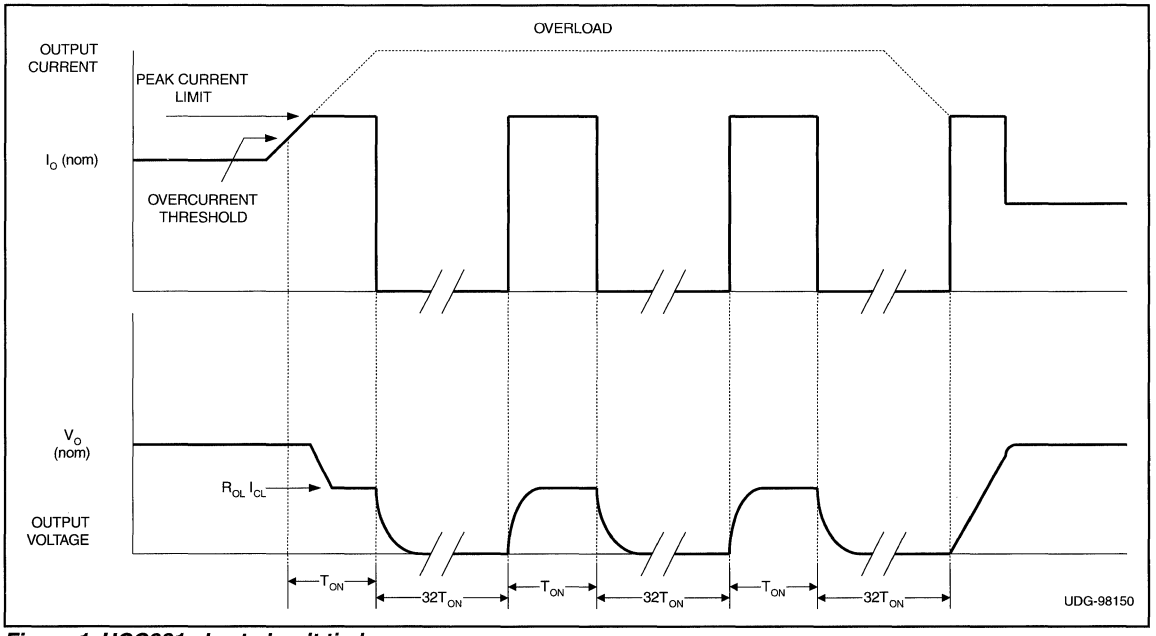


Figure 1. UCC381 short circuit timing.

APPLICATION INFORMATION (cont.)

Dropout Performance

Referring to the Block Diagram, the dropout voltage of the UCC381 is equal to the minimum voltage drop (V_{IN} to V_{OUT}) across the N-Channel MOSFET. The dropout voltage is dependent on operating conditions such as load current, input and load voltages, as well as temperature. The UCC381 achieves a low $Rds_{(ON)}$ through the use of an internal charge-pump (V_{PUMP}) that drives the MOSFET gate. Fig. 2 depicts typical dropout voltages versus load current for the 3.3V and 5V versions of the part, as well as the adjustable version programmed to 3.0V.

Fig. 3 depicts the typical dropout performance of the adjustable version with various output voltages and load currents.

Operating temperatures effect the RDS(ON) and dropout voltage of the UCC381. Fig. 4 graphs the typical dropout for the 3.3V and 5V versions with a 3A load over temperature.

Voltage Programming

Referring to the Typical Application Circuit, the output voltage for the adjustable version is externally programmed through a resistive divider at the VOUTS pin as shown.

$$V_{OUT} = 1.25 \bullet \left(1 + \frac{R2}{R1}\right) Volts \qquad (4)$$

For the fixed Voltage versions the resistive divider is internally set, and the VOUTS pin should be connected to the VOUT pin. The maximum programmed output voltage for the adjustable part is constrained by the 9V absolute rating of the IC (including the charge pump voltage) and its ability to enhance the N-Channel MOSFET. Unless the load current is well below the 1A rating of the device, output voltages above 7V are not recommended. The minimum output voltage can be programmed down to 1.25V, however, the input voltage must always be greater than the UVLO of the part.

Shutdown Feature

All versions include a shutdown feature, limiting quiescent current to 25µA typical. The UCC381 is shut down by pulling the CT pin to below 0.25V. As shown in the applications circuit, a small logic level MOSFET or BJT transistor connected to the CT pin can be driven with a digital signal, putting the device in shutdown. If the CT pin is not pulled low, the IC will internally pull up on the pin, enabling the regulator. The CT pin should not be forced high, as this will interfere with the short circuit protection feature. Selection of the timing capacitor for the adjustable version is explained in the *Short Circuit Protection* section.

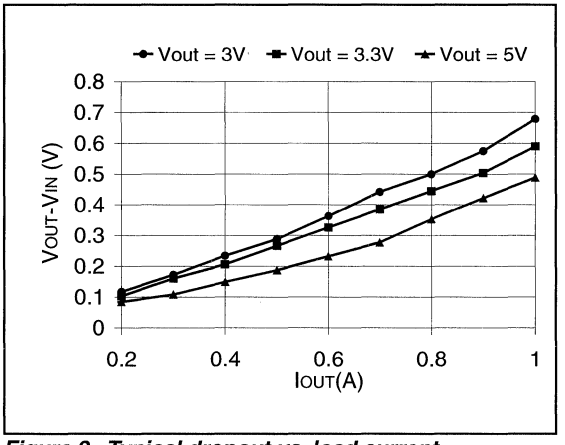


Figure 2. Typical dropout vs. load current.

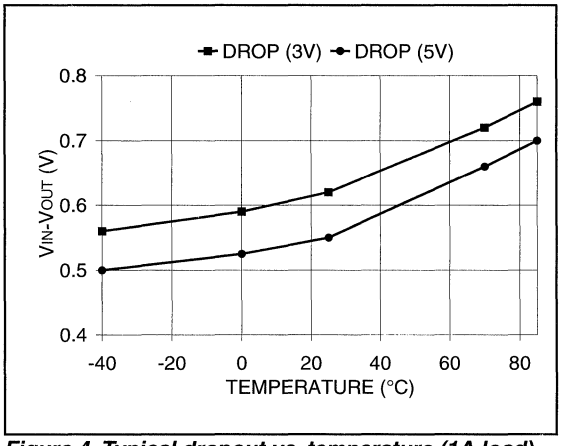


Figure 4. Typical dropout vs. temperature (1A load).

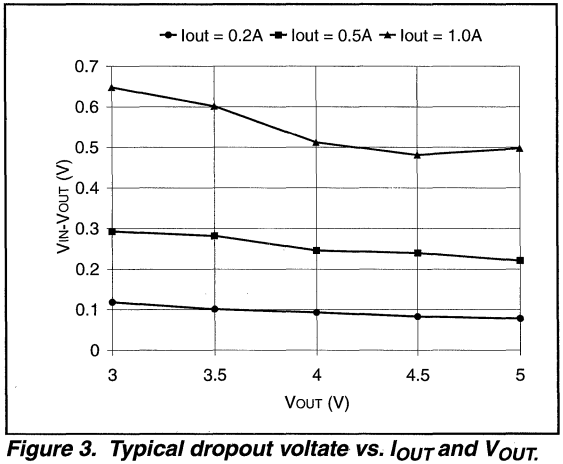


Figure 3. Typical dropout voltate vs. I_{OUT} and V_{OUT}.

APPLICATION INFORMATION (cont.)

Thermal Design

The Packing Information section of the data book contains reference material for the thermal ratings of various packages. The section also includes an excellent article *Thermal Characteristics of Surface Mount Packages*, that is the basis of the following discussion.

Thermal design for the UCC381 includes two modes of operation, normal and pulsed mode. In normal operation, the linear regulator and heat sink must dissipate power equal to the maximum forward voltage drop multiplied by the maximum load current. Assuming a constant current load, the expected heat rise at the regulator's junction can be calculated as follows:

$$T_{RISE} = P_{DISS} \bullet (\theta jc + \theta ca)\ ^{\circ}C \qquad (5)$$

Where theta is thermal resistance and P_{DISS} is the power dissipated. The thermal resistance of both the SOIC-8 DP package (junction to case) is 22 degrees Celsius per Watt. In order to prevent the regulator from going into thermal shutdown, the case to ambient theta must keep the junction temperature below 150C. If the LDO is mounted on a 5 square inch pad of 1 ounce copper, for example, the thermal resistance from junction to ambient becomes 40-70 degrees Celsius per Watt. If a lower thermal resistance is required by the application, the device heat sinking would need to be improved.

When the UCC381 regulator is in pulsed mode, due to an overload or short circuit in the application, the maximum *average* power dissipation is calculated as follows:

$$P_{PULSE\,(avg)} = \qquad (6)$$

$$(V_{IN} - V_{OUT}) \bullet I_{CL} \bullet \left(\frac{T_{ON}}{33 \bullet T_{ON}}\right) Watts$$

As seen in equation 6, the average power during a fault is reduced dramatically by the duty cycle, allowing the heat sink to be sized for normal operation. Although the peak power in the regulator during the T_{ON} period can be significant, the thermal mass of the package will generally keep the junction temperature from rising unless the T_{ON} period is increased to tens of milliseconds.

Ripple Rejection

Even though the UCC381 linear regulators are not optimized for fast transient applications (Refer to UC182 "Fast LDO Linear Regulator"), they do offer significant power supply rejection at lower frequencies. Fig 5. depicts ripple rejection performance in a typical application. The performance can be improved with additional filtering.

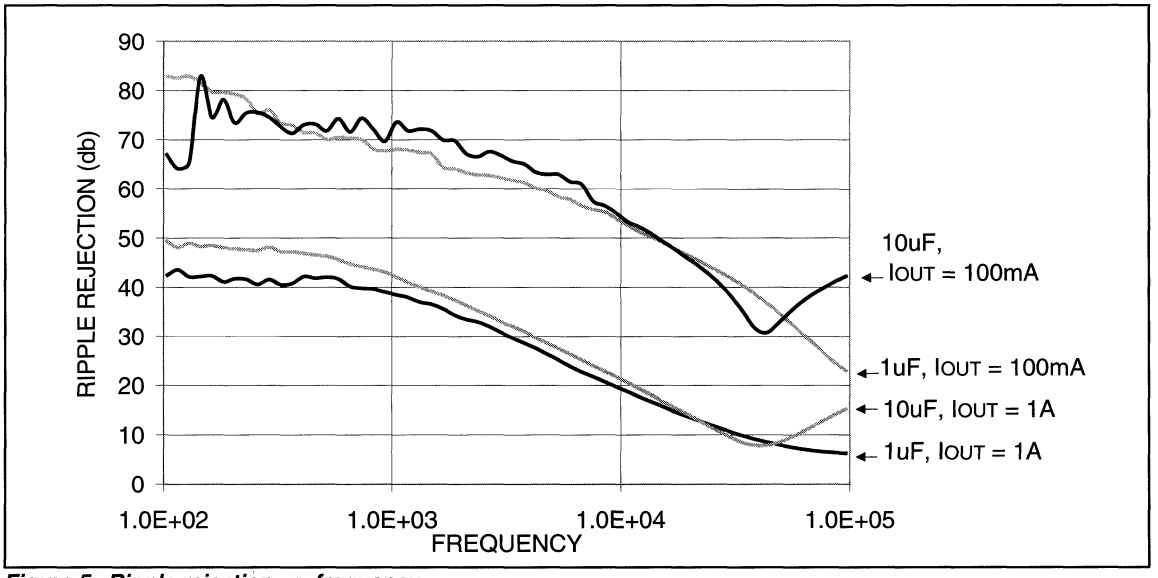


Figure 5. Ripple rejection vs. frequency.

UNITRODE CORPORATION
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Low Dropout 3 Ampere Linear Regulator Family

FEATURES

- Precision Positive Series Pass Voltage Regulation
- 0.45V Dropout at 3A
- 50mV Dropout at 10mA
- Quiescent Current Under 650µA Irrespective of Load
- Adjustable (5 Lead) Output Voltage Version
- Fixed (3 Lead) Versions for 3.3V and 5V Outputs
- Logic Shutdown Capability
- Short Circuit Power Limit of 3% •V_{IN} • I_{SHORT}
- Low V_{OUT} to V_{IN} Reverse Leakage
- Thermal Shutdown

DESCRIPTION

The UCC283-3/-5/-ADJ family of positive linear series pass regulators are tailored for low drop out applications where low quiescent power is important. Fabricated with a BiCMOS technology ideally suited for low input to output differential applications, the UCC283-5 will pass 3A while requiring only 0.45V of typical input voltage headroom (guaranteed 0.6V dropout). These regulators include reverse voltage sensing that prevents current in the reverse direction. Quiescent current is always less than 650µA. These devices have been internally compensated in such a manner that the need for a minimum output capacitor has been eliminated.

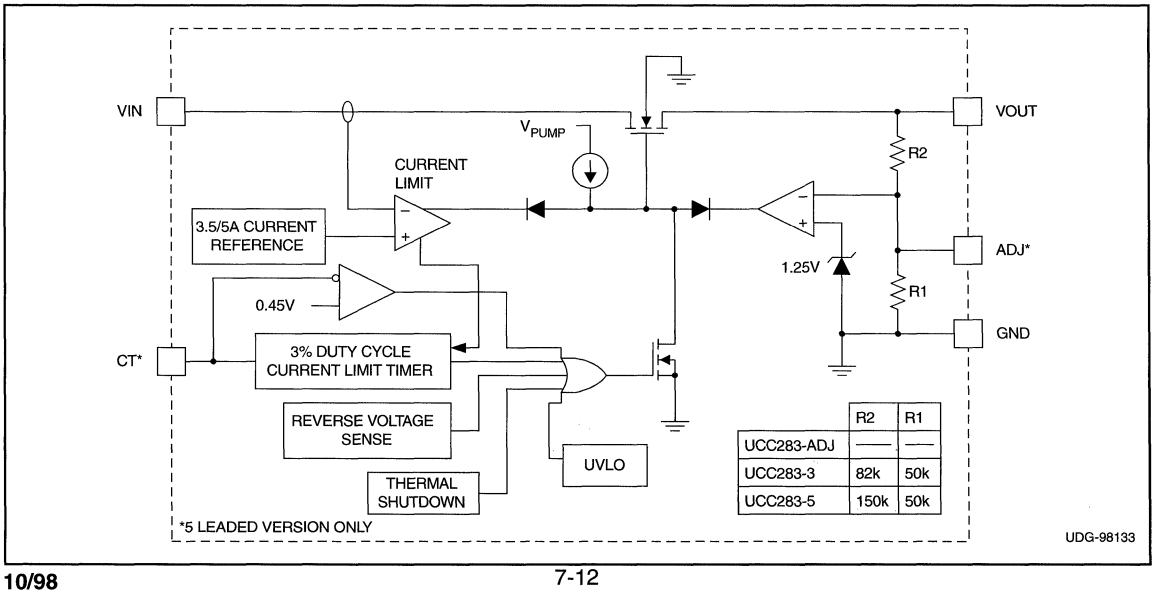
UCC283-3 and UCC283-5 versions are in 3 lead packages and have preset outputs at 3.3V and 5.0V respectively. The output voltage is regulated to 1.5% at room temperature. The UCC283-ADJ version, in a 5 lead package, regulates the output voltage programmed by an external resistor ratio.

Short circuit current is internally limited. The device responds to a sustained overcurrent condition by turning off after a T_{ON} delay. The device then stays off for a period, T_{OFF}, that is 32 times the T_{ON} delay. The device then begins pulsing on and off at the $T_{ON}/(T_{ON}+T_{OFF})$ duty cycle of 3%. This drastically reduces the power dissipation during short circuit and means heat sinks need only accommodate normal operation. On the 3 leaded versions of the device T_{ON} is fixed at 750µs, on the adjustable 5 leaded versions an external capacitor sets the on time — the off time is always 32 times T_{ON}. The external timing control pin, CT, on the five leaded versions also serves as a shutdown input when pulled low.

Internal power dissipation is further controlled with thermal overload protection circuitry. Thermal shutdown occurs if the junction temperature exceeds 165°C. The chip will remain off until the temperature has dropped 20°C.

The UCC283 series is specified for operation over the industrial range of –40°C to +85°C, and the UCC383 series is specified from 0°C to +70°C. These devices are available in 3 and 5 pin TO-220 and TO-263 power packages.

BLOCK DIAGRAM



	R2	R1
UCC283-ADJ	—	—
UCC283-3	82k	50k
UCC283-5	150k	50k

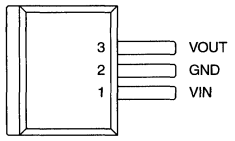
ABSOLUTE MAXIMUM RATINGS

VIN 9V
CT ..... –0.3 to 3V
ADJ ..... –0.3 to 9V
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

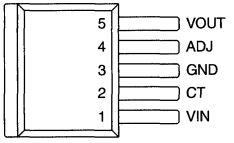
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

CONNECTION DIAGRAMS

TO-263-3 (Front View)
TD Package

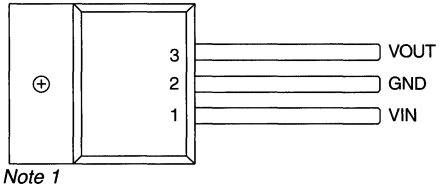


TO-263-5 (Front View)
TD Package



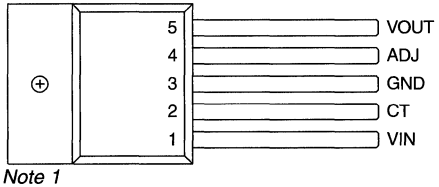
See Note 1

TO-220-3 (Front View)
T Package



See Note 1

TO-220-5 (Front View)
T Package



See Note 1

Note 1: Tab = GND

7

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications hold for T_A = 0°C to 70°C for the UCC383-X series, –40°C to +85°C for the UCC283-X, $V_{VIN} = V_{VOUT} + 1.5V$, I_{OUT} = 10mA, C_{IN} = 10µF, C_{OUT} = 22µF. For the 283-ADJ, V_{VIN} = 6.5V, CT = 750pF, $T_J = T_A$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UCC283-5 Fixed 5V, 3A Family					
Output Voltage	T_J = 25°C	4.925	5	5.075	V
	Over Temperature	4.875		5.125	V
Line Regulation	V_{VIN} = 5.15V to 9V		2	10	mV
Load Regulation	I_{OUT} = 10mA to 3A		10	20	mV
Dropout Voltage, $V_{DROPOUT} = V_{VIN} - V_{VOUT}$	I_{OUT} = 3A, VOUT = 4.85V		0.4	0.6	V
	I_{OUT} = 1.5A, VOUT = 4.85V		0.2	0.45	V
	I_{OUT} = 10mA, VOUT = 4.85V		50	150	mV
Peak Current Limit	V_{VOUT} = 0V	4	5	6.5	A
Overcurrent Threshold		3	4	5.5	A
Current Limit Duty Cycle	V_{VOUT} = 0V		3	5	%
Overcurrent Time Out, T_{ON}	V_{VOUT} = 0V	400	750	1400	µs
Quiescent Current	No load		400	650	µA
Reverse Leakage Current	$0V < V_{VIN} < V_{VOUT}$, $V_{VOUT} \leq 5.1V$, at V_{VOUT}		0	75	µA
UVLO	VIN where VOUT passes current	2.6	2.8	3	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications hold for T_A = 0°C to 70°C for the UCC383-X series, –40°C to +85°C for the UCC283-X, $V_{VIN} = V_{VOUT} + 1.5V$, I_{OUT} = 10mA, C_{IN} = 10µF, C_{OUT} = 22µF. For the 283-ADJ, V_{VIN} = 6.5V, CT = 750pF, $T_J = T_A$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UCC283-3 Fixed 3.3V, 3A Family					
Output Voltage	T_J = 25°C	3.25	3.3	3.35	V
	Over Temperature	3.22		3.38	V
Line Regulation	V_{VIN} = 3.45V to 9V		2	7	mV
Load Regulation	I_{OUT} = 10mA to 3A		7	15	mV
Dropout Voltage, $V_{DROPOUT} = V_{VIN} - V_{VOUT}$	I_{OUT} = 3A, VOUT = 3.15V		0.5	1	V
	I_{OUT} = 1.5A, VOUT = 3.15V		0.25	0.6	V
	I_{OUT} = 10mA, VOUT = 3.15V		50	150	mV
Peak Current Limit	V_{VOUT} = 0V	4	5	6.5	A
Overcurrent Threshold		3	4	5.5	A
Current Limit Duty Cycle	V_{VOUT} = 0V		3	5	%
Overcurrent Time Out, TON	V_{VOUT} = 0V	400	750	1400	µs
Quiescent Current	No load		400	650	µA
Reverse Leakage Current	$0V < V_{VIN} < V_{VOUT}$, $V_{VOUT} \leq 3.35V$, at V_{VOUT}		0	75	µA
UVLO	VIN where VOUT passes current	2.6	2.8	3	V
UCC283-ADJ Adjustable Output, 3A Family					
Regulating Voltage at ADJ Pin	T_J = 25°C	1.23	1.25	1.27	V
	Over Temperature	1.22		1.28	V
Line Regulation, at ADJ Input	$V_{VIN} = V_{VOUT}$ + 150mV to 9V		1	3	mV
Load Regulation, at ADJ Input	I_{OUT} = 10mA to 3A		2	5	mV
Dropout Voltage, $V_{DROPOUT}$ = VIN – VOUT	$V_{VIN} > 4V$, I_{OUT} = 3A		0.4	0.6	V
	$V_{VIN} > 3V$, I_{OUT} = 1.5A		0.2	0.45	V
	$V_{VIN} > 3V$, I_{OUT} = 10mA		50	150	mV
Peak Current Limit	V_{VOUT} = 0V, VIN = 6.5V	4	5	6.5	A
Overcurrent Threshold	V_{VIN} = 6.5V	3	4	5.5	A
Current Limit Duty Cycle	V_{VOUT} = 0V		3	5	%
Overcurrent Time Out, TON	V_{VOUT} = 0V, CT = 1500pF		750		µs
Reverse Leakage Current	$0V < V_{VIN} < V_{VOUT}$, $V_{VOUT} \leq 9V$, at V_{VOUT}		0	100	µA
Bias current at ADJ Input			100	250	nA
Quiescent Current	No load		400	650	µA
Shutdown Threshold	At CT Input	0.25	0.45		V
Quiescent Current in Shutdown	V_{VIN} = 10V		40	75	µA
UVLO	VIN where VOUT passes current	2.6	2.8	3	V

PIN DESCRIPTIONS

ADJ: Adjust pin for the UCC283-ADJ version only. Feedback pin for the linear regulator. Program the output voltage with R1 connected from ADJ to GND and R2 connected from VOUT to ADJ. Output voltage is given by:

$$VOUT = \frac{1.25V \bullet (R1 + R2)}{R1}$$

CT: Short circuit timing capacitor and shutdown input for the UCC283-ADJ version. Pulling CT below 0.25V turns off the regulator and places it in a low quiescent current mode. A timing capacitor, C, from CT to GND programs the duration of the pulsed short circuit on-time. On-time, T_{ON}, is approximately given by: $T_{ON} = 500k \bullet C$.

GND: Reference ground.

VIN: Input voltage, This pin must be bypassed with a low ESL/ESR 1µF or larger capacitor to GND. VIN can range from (VOUT + $V_{DROPOUT}$) to 9V. If VIN is reduced to zero while VOUT is held high, the reverse leakage from VOUT to VIN is less than 75µA.

VOUT: Regulated output voltage. A bypass capacitor is not required at VOUT, but may be desired for good transient response. The bypass capacitor must not exceed a maximum value in order to insure the regulator can start.

Table I. Package Information

Temperature Range	Package	Output Voltage
2: –40°C to +85°C	T: TO-220	3: 3.3V
3: 0°C to +70°C	TD: TO-263	5: 5V
		ADJ: Adjustable

ORDERING INFORMATION

UCC☐83☐-☐
- Output Voltage
- Package
- Temperature Range

APPLICATION INFORMATION

Overview

The UCC383 family of low dropout linear (LDO) regulators provide a regulated output voltage for applications with up to 3A of load current. The regulators feature a low dropout voltage and short circuit protection, making their use ideal for demanding high current applications requiring fault protection.

Short Circuit Protection

The UCC383 provides unique short circuit protection circuitry that reduces power dissipation during a fault. When an overload situation is detected, the device enters a pulsed mode of operation at 3% duty cycle reducing the heat sink requirements during a fault. The UCC383 has two current thresholds that determine its behavior during a fault as shown in Figure 1.When the regulator current exceeds the **overcurrent threshold** for a period longer than T_{ON}, the UCC383 shuts off for a period (T_{OFF}) which is 32 times T_{ON}. During an overload, the regulator actively limits the maximum current to the **peak current limit** value. The peak current limit is nominally 1 Amp greater than the overcurrent threshold. The regulator will continue in pulsed mode until the fault is cleared as illustrated in Figure 1.

Short Circuit Protection

A capacitive load on the regulator's output will appear as a short circuit during start-up. If the capacitance is too large, the output voltage will not come into regulation during the initial T_{ON} period and the UCC383 will enter pulsed mode operation. The peak current limit, T_{ON} period, and load characteristics determine the maximum value of output capacitor that can be charged. For a constant current load the maximum output capacitance is given as follows:

$$C_{OUT(max)} = (I_{CL} - I_{LOAD}) \bullet \frac{T_{ON}}{V_{OUT}} \ Farads \qquad (1)$$

For worst case calculations the minimum values of on time (T_{ON}) and peak current limit (I_{CL}) should be used. The adjustable version allows the T_{ON} time to be adjusted with a capacitor on the CT pin:

$$T_{ON(ADJ)} = 500{,}000 \bullet C(\mu Farad) \ microseconds \qquad (2)$$

$$T_{ON(\mu sec)} = 500{,}000 \bullet C(\mu Farads)$$

For a resistive load (R_{LOAD}) the maximum output capacitor can be estimated from:

$$C_{OUT(max)} = \frac{T_{ON(sec)}}{R_{LOAD} \bullet \ln\left(\frac{1}{1 - \frac{V_{OUT}}{I_{CL} \bullet R_{LOAD}}}\right)} \ Farads \qquad (3)$$

APPLICATION INFORMATION (cont.)

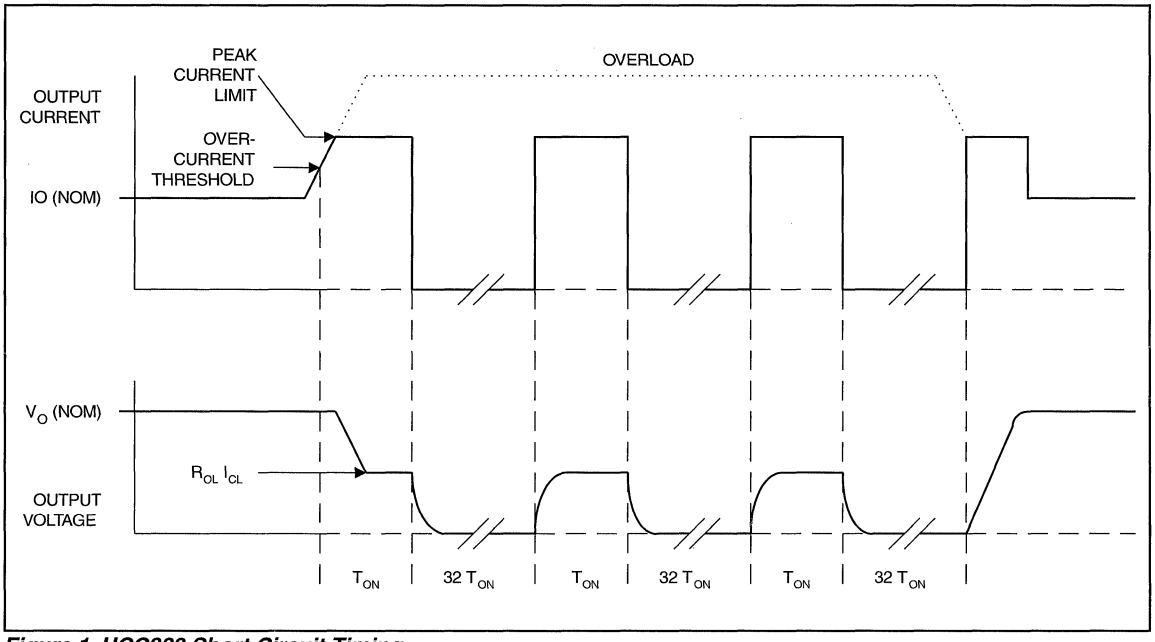


Figure 1. UCC383 Short Circuit Timing

Dropout Performance

Referring to the Block Diagram, the dropout voltage of the UCC383 is equal to the minimum voltage drop (V_{IN} to V_{OUT}) across the N-Channel MOSFET. The dropout voltage is dependent on operating conditions such as load current, input and load voltages, as well as temperature. The UCC383 achieves a low $RDS_{(ON)}$ through the use of an internal charge-pump (V_{PUMP}) that drives the MOSFET gate. Figure 2 depicts typical dropout voltages versus load current for the 3.3V and 5V versions of the part, as well as the adjustable version programmed to 3.0V.

Figure 3. depicts the typical dropout performance of the adjustable version with various output voltages and load currents.

Operating temperatures also effect the $RDS_{(ON)}$ and dropout voltage of the UCC383. Figure 4. graphs the typical dropout for the 3.3V and 5V versions with a 3A load over temperature.

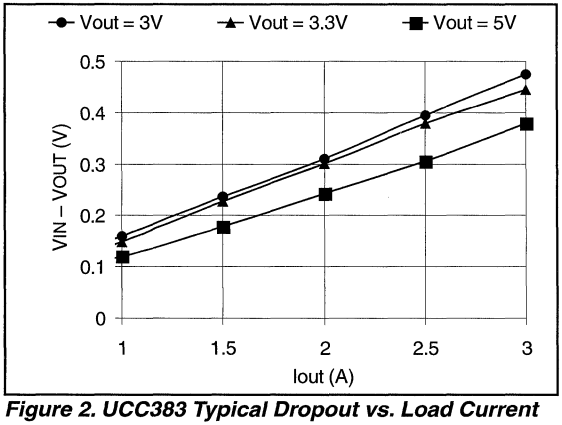


Figure 2. UCC383 Typical Dropout vs. Load Current

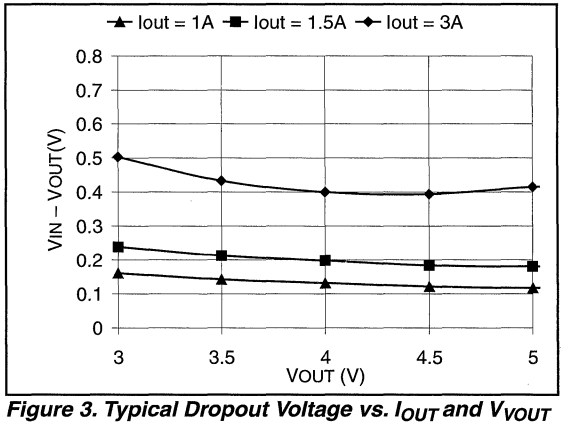


Figure 3. Typical Dropout Voltage vs. I_{OUT} and V_{VOUT}

Voltage Programming and Shutdown Feature for Adjustable Version

A typical application circuit based on the UCC383 adjustable version is shown in Figure 5. The output voltage is externally programmed through a resistive divider at the ADJ pin.

$$V_{OUT} = 1.25 \bullet \left(1 + \frac{R2}{R1}\right) volts \quad (4)$$

The maximum programmed output voltage is constrained by the 9V absolute rating of the IC (this includes the charge pump voltage) and its ability to enhance the N-Channel MOSFET. Unless the load current is below the 3A rating of the device, output voltages above 7V are not recommended. The minimum output voltage can be programmed down to 1.25V, however, the input voltage must always be greater than the UVLO of the part.

The adjustable version includes a shutdown feature, limiting quiescent current to 40uA typical. The UCC383 is shutdown by pulling the CT pin to below 0.25V. As shown in Figure 4, a small logic level MOSFET or BJT transistor in parallel with the timing capacitor can be driven with a digital signal, putting the device in shutdown. If the CT pin is not pulled low, the IC will internally pull up on the pin enabling the regulator. The CT pin should not be forced high, as this will interfere with the short circuit protection feature. Selection of the timing capacitor is explained in *Short Circuit Protection*.

The adjustable version can be used in applications requiring remote voltage sensing (i.e. monitoring a voltage other than or not directly tied to the VOUT pin). This is possible since the inverting input of the voltage amplifier (see Block Diagram) is brought out to the ADJ pin.

Thermal Design

The Packing Information section of the data book contains reference material for the thermal ratings of various packages. The section also includes an excellent article *Thermal Characteristics of Surface Mount Packages*, that is the basis of the following discussion.

Thermal design for the UCC383 includes two modes of operation, normal and pulsed mode. In normal operation, the linear regulator and heat sink must dissipate power equal to the maximum forward voltage drop multiplied by the maximum load current. Assuming a constant current load, the expected heat rise at the regulator's junction can be calculated as follows:

$$T_{RISE}(\theta) = P_{DISS} \bullet (\theta_{jc} + \theta_{ca})\ ^{\circ}C \quad (5)$$

Where theta, (θ) is thermal resistance and P_{DISS} is the power dissipated. The thermal resistance of both the TO-220 and TO-263 packages (junction to case) is 3 degrees Celsius per Watt. In order to prevent the regulator from going into thermal shutdown, the case to ambient theta must keep the junction temperature below 150°C. If the LDO is mounted on a 5 square inch pad of 1 ounce copper, for example, the thermal resistance from junction to ambient becomes 60 degrees Celsius per Watt. If a lower thermal resistance is required by the application, the device heat sinking would need to be improved.

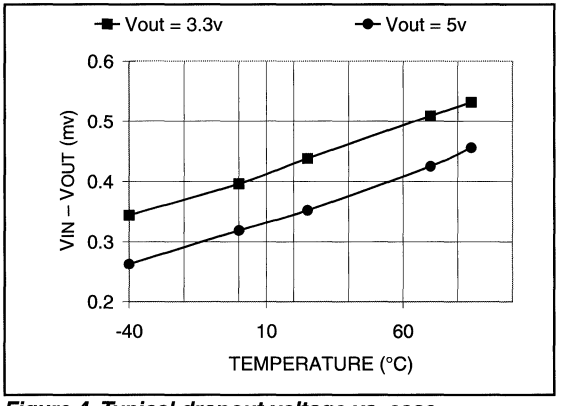


Figure 4. Typical dropout voltage vs. case temperature with a 3A load

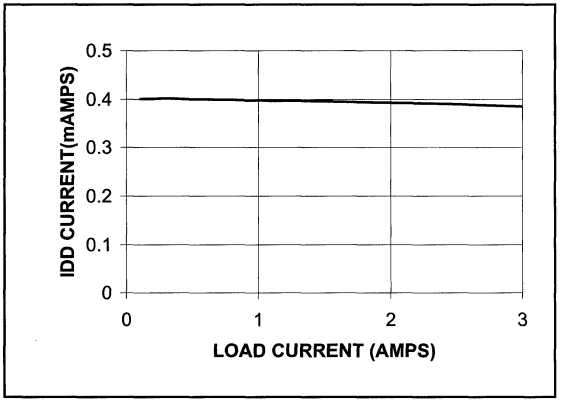


Figure 5. Typical application for the 5 pin adjustable version.

When the UCC383 regulator is in pulsed mode due to an overload or short circuit in the application, the maximum *average* power dissipation is calculated as follows:

$$P_{PULSE\_AVE} = (V_{IN} - V_{OUT}) \bullet I_{CL} \bullet \frac{T_{ON}}{33 \bullet T_{ON}} Watts \quad (6)$$

As seen in equation 6, the average power during a fault is reduced dramatically by the duty cycle, allowing the heat sink to be sized for normal operation. Although the peak power in the regulator during the T_{ON} period can be significant, the thermal mass of the package will generally keep the junction temperature from rising unless the T_{ON} period is increased to tens of milliseconds.

Ripple Rejection

Even though the UCC383 family of linear regulators are not optimized for fast transient applications (Refer to UC182 Fast LDO Linear Regulator), they do offer significant power supply rejection at lower frequencies. Figure 6 depicts ripple rejection performance in a typical application. The performance can be improved with additional filtering.

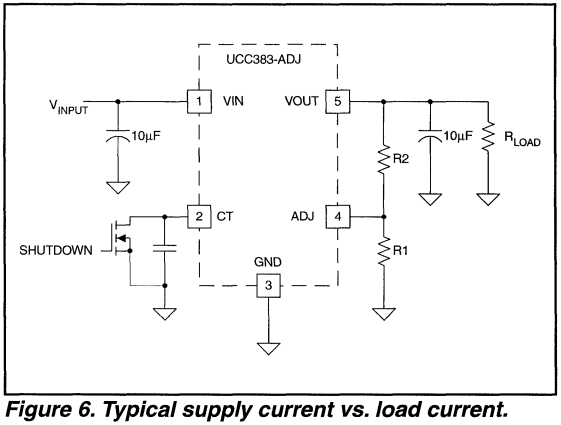


Figure 6. Typical supply current vs. load current.

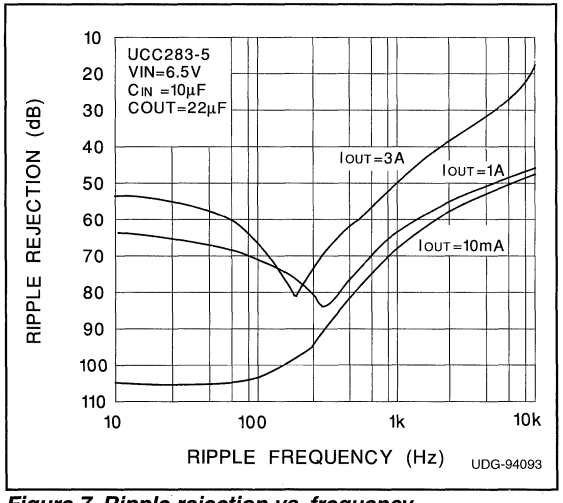


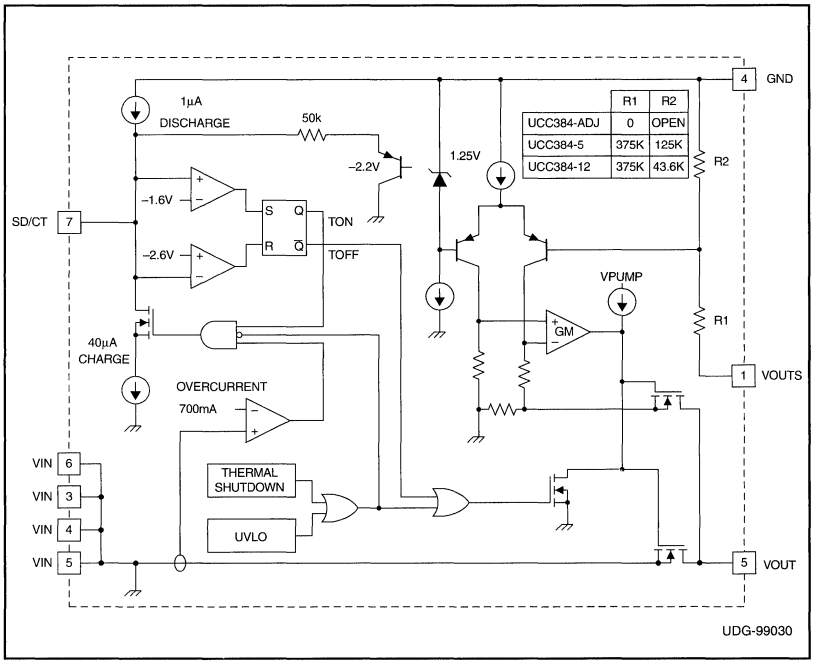
Figure 7. Ripple rejection vs. frequency.

Low Dropout 0.5A Negative Linear Regulator

FEATURES

- Precision Negative Series Pass Voltage Regulation
- 0.2V Drop Out at 0.5A
- Wide Input voltage Range –3.2V to –15V
- Low Quiescent Current Irrespective of Load
- Simple Logic Shutdown Interfacing
- –5V, –12V and Adjustable Output
- 2.5% Duty Cycle Short Circuit Protection
- Remote Load Sensing for Accurate Load Regulation
- 8-Pin DP Package

BLOCK DIAGRAM



DESCRIPTION

The UCC384 family of negative linear series pass regulators is tailored for low drop out applications where low quiescent power is important. Fabricated with a BCDMOS technology ideally suited for low input to output differential applications, the UCC384 will pass 0.5A while requiring only 0.2V of input voltage headroom. Drop out voltage decreases linearly with output current, so that drop out at 50mA is less than 20mV.

Quiescent current consumption for the device under normal (non-drop out) conditions is typically 200µA. An integrated charge pump is internally enabled only when the device is operating near drop out with low VIN. This guarantees that the device will meet the drop out specifications even for maximum load current and a VIN of –3.2V with only a modest increase in quiescent current. Quiescent current is always less than 350µA, with the charge pump enabled. Quiescent current of the UCC384 does not increase with load current.

Short circuit current is internally limited. The device responds to a sustained over current condition by turning off after a T_{ON} delay. The device then stays off for a period, T_{OFF}, that is 40 times the T_{ON} delay. The device then begins pulsing on and off at the T_{ON}/T_{OFF} duty cycle of 2.5%. This drastically reduces the power dissipation during short circuit such that heat sinking, if at all required, must only accommodate normal operation. An external capacitor sets the on time. The off time is always 40 times T_{ON}.

The UCC384 can be shutdown to 45µA (maximum) by pulling the SD/CT pin more positive than –0.6V. To allow for simpler interfacing, the SD/CT pin may be pulled up to +6V above the ground pin without turning on clamping diodes.

Internal power dissipation is further controlled with thermal overload protection circuitry. Thermal shutdown occurs if the junction temperature exceeds 140°C. The chip will remain off until the temperature has dropped 20°C.

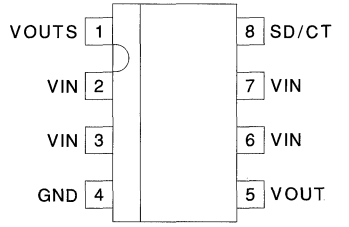
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, VIN ..... –16V
Shutdown Voltage, SD/CT ..... +6V to –5V
Storage Temperature ..... 65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal. All voltages are with respect to ground. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

SOIC-8 (Top View)
DP Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C for the UCC384 and –40°C to 85°C for the UCC284, VIN = VOUT – 1.5V, I_{OUT} = 0mA, C_{OUT} = 4.7µF, and CT = 0.015µF. For UCC384-ADJ, VOUT is set to –3.3V. $T_J = T_A$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UCC384-5 Fixed –5V 0.5A Regulation Section					
Output Voltage	T_A = 25°C	–5.075	–5	–4.925	V
	Over all conditions	–5.100		–4.850	V
Line Regulation	VIN = –5.3V to –15V		1.5	10	mV
Load Regulation	I_{OUT} = 0mA to 0.5A		0.1	0.25	%
Output Noise Voltage	T_A = 25°C, BW = 10Hz to 10kHz		200		µVRMS
Drop Out Voltage, VOUT – VIN	I_{OUT} 0.5A, VOUT = –4.8V		0.20	0.50	V
	I_{OUT} 50mA, VOUT = –4.8V		20	50	mV
UCC384-5 Fixed –5V 0.5A Power Supply Section					
Input Voltage Range		–15		–5.2	V
Quiescent Current Charge Pump On	VIN = –4.85V (Note 1)		280	350	µA
Quiescent Current	VIN = –15V		200	250	µA
Quiescent Current in Shutdown	VIN = –15V, SD/CT = 0V, No Load		24	45	µA
Shutdown Threshold	At Shutdown Pin	–1.0	–0.6	–0.4	V
Shutdown Input Current	SD/CT = 0V	5	17	25	µA
Output Leakage in Shutdown	VIN = –15V, VOUT = 0, 25 C		1	10	µA
	Over Temperature			50	µA
Over Temperature Shutdown			140		°C
Over Temperature Hysteresis			20		°C
UCC384-5 Fixed –5V 0.5A Current Limit Section					
Peak Current Limit	VOUT = 0V	0.7	1.1	1.5	A
Over Current Threshold		0.55	0.7	0.9	A
Current Limit Duty Cycle	VOUT = 0V		2.5	4	%
Overcurrent Time Out, T_{ON}	VOUT = 0V	300	450	650	µs
UCC384-12 Fixed 12V 0.5A Regulation Section					
Output Voltage	T_A = 25°C	–12.18	–12	–11.82	V
	Over all conditions	–12.24		–11.64	V
Line Regulation	VIN = –12.5V to –15V		5	15	mV
Load Regulation	I_{OUT} = 0mA to 0.5A		0.1	0.3	%
Output Noise Voltage	T_A = 25°C, BW = 10Hz to 10kHz		200		µVRMS
Drop Out Voltage, VOUT - VIN	I_{OUT} 0.5A, VOUT = –11.6V		0.15	0.5	V
	I_{OUT} 50mA, VOUT = –11.6V		15	50	mV

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C for the UCC384 and –40°C to 85°C for the UCC284, VIN = VOUT – 1.5V, I_{OUT} = 0mA, C_{OUT} = 4.7µF, and CT = 0.015µF. For UCC384-ADJ, VOUT is set to –3.3V. $T_J = T_A$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UCC384-12 Fixed –12V 0.5A Power Supply Section					
Input Voltage Range		–15		–12.2	V
Quiescent Current	VIN = –15V		220	350	µA
Quiescent Current in Shutdown	VIN = –15V, SD/CT = 0V, No Load		24	45	µA
Shutdown Threshold	At Shutdown Pin	–1.0	–0.6	–0.4	V
Shutdown Input Current	SD/CT = 0V	5	17	25	µA
Output Leakage in Shutdown	VIN = –15V, VOUT = 0, 25 C		1	10	µA
	Over Temperature			50	µA
Over Temperature Shutdown			140		°C
Over Temperature Hysteresis			20		°C
UCC384-12 Fixed -12V 0.5A Current Limit Section					
Peak Current Limit	VOUT = 0V	0.7	1.2	1.5	A
Over Current Threshold		0.55	0.7	0.9	A
Current Limit Duty Cycle	VOUT = 0V		2.5	4	%
Over Current Time Out, T_{ON}	VOUT = 0V	300	450	650	µs
UCC384-ADJ Adjustable 0.5A Regulation Section					
Reference Voltage	T_A = 25°C	–1.27	–1.25	–1.23	V
	Over Temperature	–1.275		–1.215	V
Line Regulation	VIN = –3.5V to –15V, VOUT = VOUTS		0.5	3	mV
Load Regulation	I_{OUT} = 0mA to 0.5A		0.1	0.18	%
Output Noise Voltage	T_A = 25°C, BW = 10Hz to 10kHz		200		µVRMS
Drop Out Voltage, VOUT - VIN	I_{OUT} 0.5A, VOUT = –3.15V		0.25	0.5	V
	I_{OUT} 50mA, VOUT = 3.15V		25	50	mV
Sense Pin Input Current			100	250	nA
UCC384-ADJ Adjustable 0.5A Power Supply Section					
Input Voltage Range		–15		–3.5	V
Undervoltage Lockout		–3.2		–2.7	V
Quiescent Current Charge Pump On	VIN = –3.15V (Note 1)		200	350	µA
Quiescent Current	VIN = –15V		200	250	µA
Quiescent Current in Shutdown	VIN = –15V, SD/CT = 0V, No Load		24	45	µA
Shutdown Threshold	At Shutdown Pin	–1.0	–0.6	–0.4	V
Shutdown Input Current	SD/CT = 0V	5	17	25	µA
Output Leakage in Shutdown	VIN = –15V, VOUT = 0, 25 C		1	10	µA
	Over Temperature			50	µA
Over Temperature Shutdown			140		°C
Over Temperature Hysteresis			20		°C
UCC384-ADJ Adjustable 0.5A Current Limit Section					
Peak Current Limit	VOUT = 0V	0.7	1.1	1.5	A
Over Current Threshold		0.55	0.7	0.9	A
Current Limit Duty Cycle	VOUT = 0V		2.5	4	%
Over Current Time Out, T_{ON}	VOUT = 0V	300	450	650	µs

Note 1: *Internal Charge Pump is enabled only for drop-out condition with low VIN. Only in this condition is the Charge Pump required to provide additional output FET gate drive to maintain drop-out specifications. For conditions where the Charge Pump is not required, it is disabled, which lowers overall device power consumption.*

PIN DESCRIPTIONS

GND: This is the low noise ground reference input. All voltages are measured with respect to the GND pin.

SD/CT: This is the shutdown pin and also the short circuit timing pin. Pulling this pin more positive than –0.6V will put the circuit in a low current shutdown mode. Placing a timing capacitor between this pin and GND will set the short circuit charging time, TON during an overcurrent condition. During an overcurrent condition, the output will be pulsed at approximately a 2.5% duty cycle.

Note: The CT capacitor must be connected between this pin and GND, not VIN, to assure that the SD/CT pin is not pulled significantly negative during power-up. This pin should not be externally driven more negative than –5V or the device will be damaged.

VIN: This is the negative input supply. Bypass this pin to GND with at least 1µF of low ESR, ESL capacitance.

VOUT: Regulated negative output voltage. A single 4.7µF capacitor should be connected between this pin and GND. Smaller value capacitors can be used for light loads, but this will degrade the load step performance of the regulator.

VOUTS: This is the feedback pin for sensing the output of the regulator. For the UCC384-5 and UCC384-12 versions, VOUTS can be connected directly to VOUT. If the load is placed at a considerable distance from the regulator, the VOUTS lead can be used as a Kelvin connection to minimize errors due to lead resistance. Connecting VOUTS at the load will move the resistance of the VOUT wire into the control loop of the regulator, thereby effectively canceling the IR drop associated with the load path.

When using a UCC384-ADJ, the output voltage can be programmed by placing a resistor divider across the output to GND. VOUTS is connected to the center tap of the divider providing the feedback for the regulator. This configuration is shown in Fig. 1.

APPLICATION INFORMATION

Overview

The UCC384 family of NEGATIVE low dropout linear (LDO) regulators provides a regulated output voltage for applications with up to 0.5A of load current. The regulators feature a low dropout voltage and short circuit protection, making their use ideal for demanding applications requiring fault protection.

Programming the output voltage on the UCC384

The UCC384-5 and UCC384-12 have fixed output voltages of –5V and –12V respectively. Connecting VOUTS to VOUT will give the proper output voltage with respect to ground.

The UCC384-ADJ can be programmed for any output voltage between –1.25V and –15V. This is easily accomplished with the addition of an external resistor divider connected between GND and VOUT with VOUTS connected to the center tap of the divider. For an output of –1.25V, no resistors are needed and VOUTS is connected directly to VOUT. The regulator input voltage cannot be more positive than the UVLO threshold, or approximately –3V. Thus, low drop out cannot be achieved when programming the output voltage more positive than approximately –3.3V. A typical Application circuit is shown in Fig. 1.

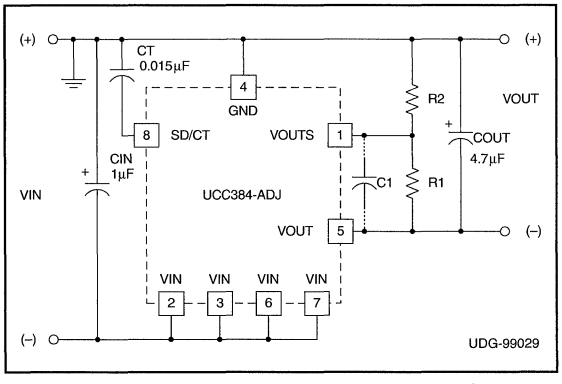


Figure 1. UCC384-ADJ application schematic.

For the UCC384-ADJ, the output voltage is programmed by the following equation:

$$VOUT = -1.25 \bullet \left(1 + \frac{R1}{R2}\right) \quad (1)$$

When R1 or R2 are selected to be greater than about 100kΩ, a small ceramic capacitor should be placed across R1 to cancel the input pole created by R1 and the parasitic capacitance appearing on VOUTS. Values of approximately 20pF should be adequate.

APPLICATION INFORMATION (cont.)

Dropout Performance

The UCC384 is tailored for low dropout applications where low quiescent power is important. Fabricated with a BCDMOS technology ideally suited for low input to output differential applications, the UCC384 will pass 0.5A while requiring only 0.2V of headroom. The dropout voltage is dependent on operating conditions such as load current, input and load voltages, and temperature. The UCC384 achieves a low $R_{DS}(on)$ through the use of an internal charge-pump that drives the MOSFET gate.

Fig. 2 shows typical dropout voltages versus output voltage for the UCC384–5V and –12V versions as well as the UCC384-ADJ version programmed between –3.3V and –15V. Since the dropout voltage is also affected by output current, Fig. 3 shows typical dropout voltages vs. load current for different values of V_{OUT}.

Operating temperatures also effect the $R_{DS}(on)$ and the dropout voltage of the UCC384. Fig. 4 shows typical dropout voltages for the UCC384 over temperature under a full load of 0.5A.

Short Circuit Protection

The UCC384 provides unique short circuit protection circuitry that reduces power dissipation during a fault. When an overcurrent condition is detected, the device enters a pulsed mode of operation, limiting the output to a 2.5% duty cycle. This will reduce the heat sink requirements during a fault. The operation of the UCC384 during an overcurrent condition is shown in Fig. 5.

UCC384 Short Circuit Timing

During normal operation the output voltage is in regulation and the SD/CT pin is held to –1.5V via a 50kΩ internal source impedance. If the output current rises above the Overcurrent Threshold, the CT capacitor will be charged by a 40µA current sink. The voltage on the SD/CT pin will move in a negative direction with respect to GND.

During an overcurrent condition, the regulator will actively limit the maximum output current to the Peak Current Limit. This will limit the output voltage of the regulator to:

$$V_{OUT} = I_{PEAK} \bullet R_L$$

If the output current stays above the Overcurrent Threshold, the voltage on the SD/CT pin will reach –2.5V with respect to GND and the output will turn off. The CT capacitor is then discharged by a 1µA current source. When the voltage on the SD/CT pin reaches –1.5V with respect to GND, the output will turn back on. This process will repeat until the output current falls below the Overcurrent Threshold.

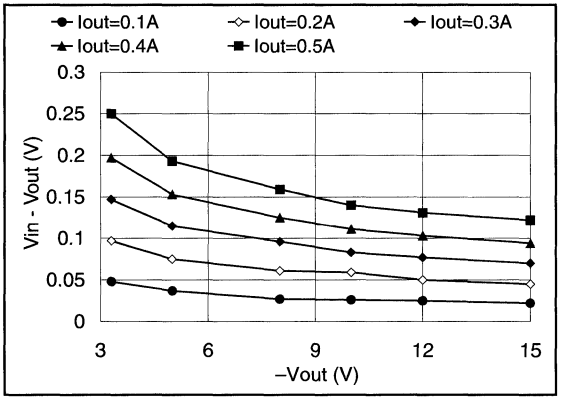


Figure 2. Dropout voltage vs. output voltage.

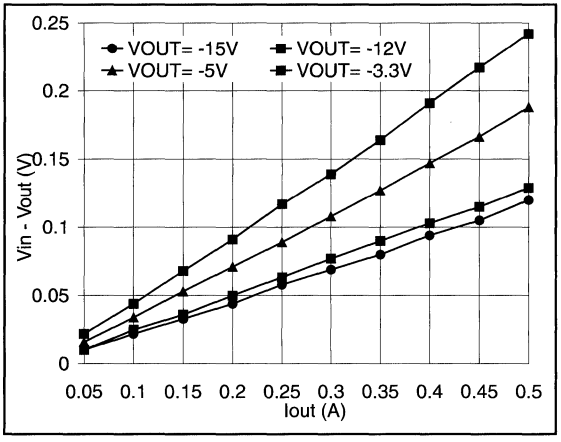


Figure 3. Dropout voltage vs. load current.

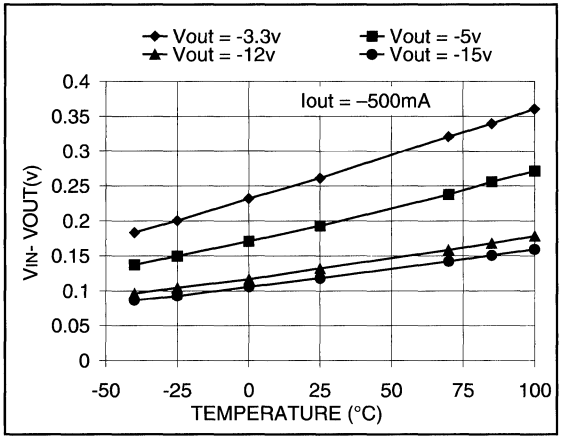


Figure 4. Dropout voltage vs. temperature.

APPLICATION INFORMATION (cont.)

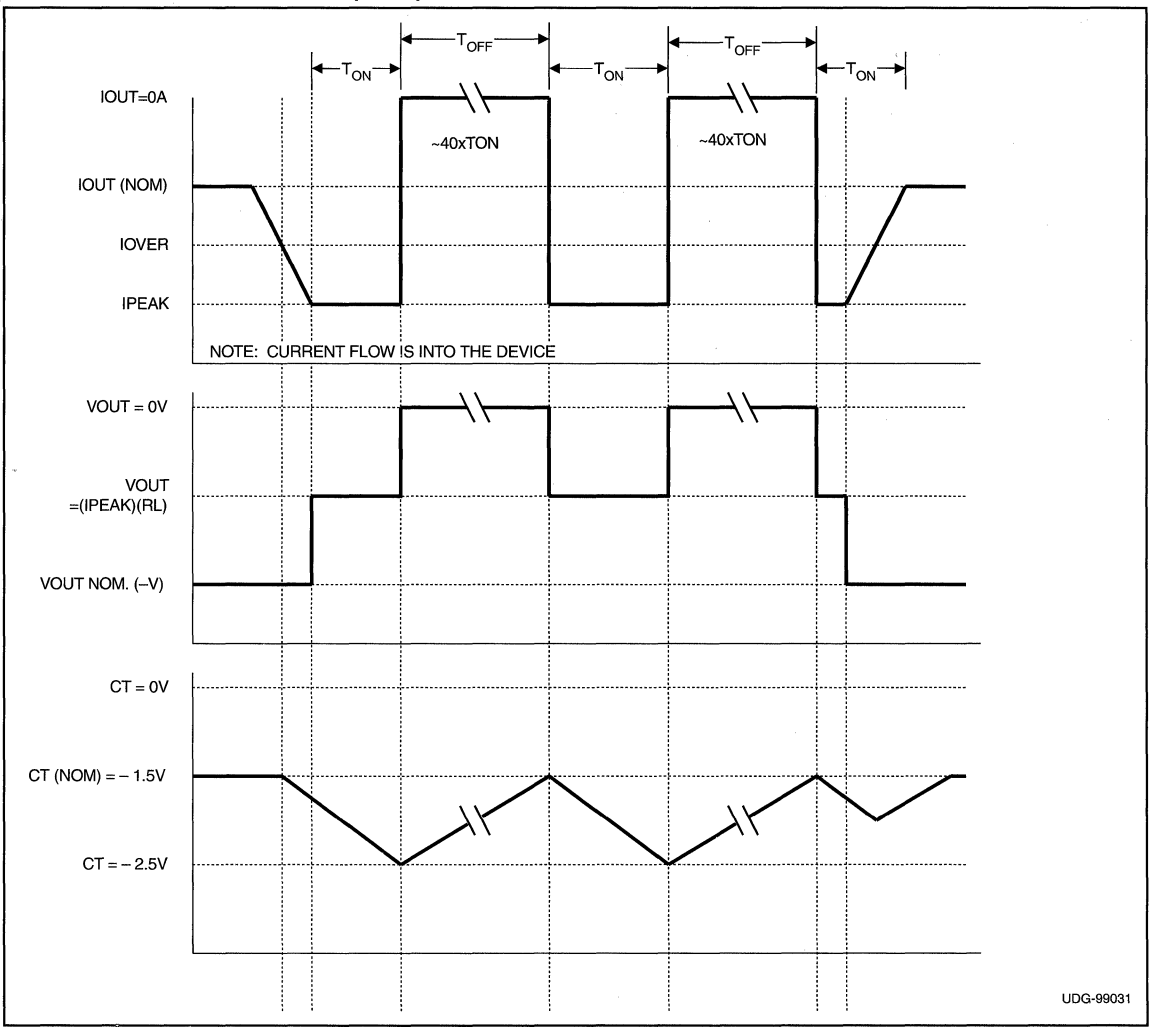


Figure 5. Short circuit timing.

T_{ON}, the time the output is on during an overcurrent condition is determined by the following equation:

$$T_{ON} = CT(\mu F) \bullet \frac{1V}{40\mu A} \quad \text{seconds} \qquad (2)$$

TOFF, the time the output is off during an overcurrent condition is determined by the following equation:

$$T_{OFF} = CT(\mu F) \bullet \frac{1V}{1\mu A} \quad \text{seconds} \qquad (3)$$

Capacitive Loads

A capacitive load on the regulator's output will appear as a short circuit during start-up. If the capacitance is too large, the output voltage will not come into regulation during the initial TON period and the UCC384 will enter a pulsed mode operation. For a constant current load the maximum allowed output capacitance is calculated as follows:

APPLICATION INFORMATION (cont.)

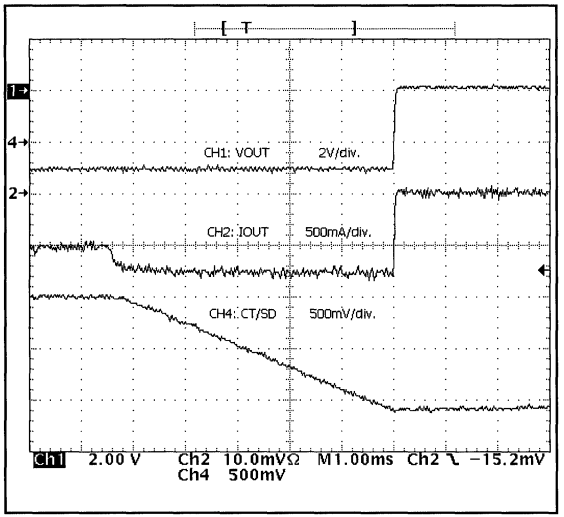


Figure 6. UCC384-ADJ operation during overcurrent condition (1ms/div).

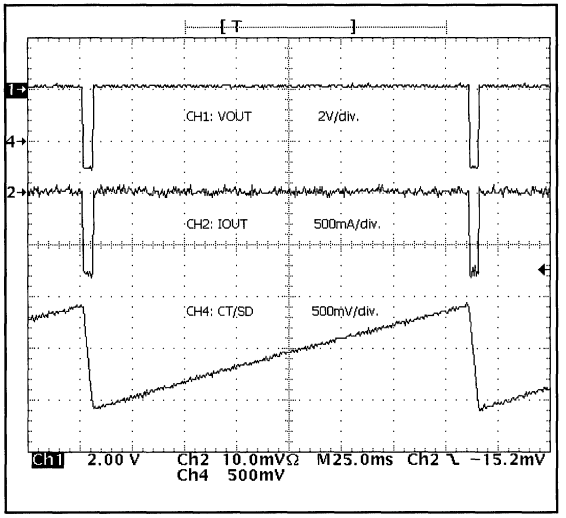


Figure 7. UCC384-ADJ operation during overcurrent condition (25ms/div.).

$$C_{OUT}(\max) = \left[I_{PEAK}(A) - I_{LOAD}(A)\right] \bullet \frac{T_{ON}(\sec)}{V_{OUT}(V)} \ \text{Farads} \quad (4)$$

For worst case calculations, the minimum value for TON should be used, which is based on the value of CT capacitor selected. For a resistive load the maximum output capacitor can be estimated as follows:

$$C_{OUT}(\max) = \frac{T_{ON}(\sec)}{R_{LOAD}(\Omega) \bullet \ln\left(\frac{1}{1 - \frac{V_{OUT}(V)}{I_{MAX}(A) \bullet R_{LOAD}(\Omega)}}\right)} \ \text{Farads} \quad (5)$$

Fig. 6 and Fig. 7 are oscilloscope photos of the UCC384-ADJ operating during an overcurrent condition. Fig. 6 shows operation of the circuit as the output current initially rises above the Overcurrent Threshold. This is shown on a 1ms/div. scale. Fig. 7 shows operation of the same circuit on a 25ms/div. scale allowing us to see one complete cycle of operation during an overcurrent condition.

Shutdown Feature of the UCC384

The shutdown feature of the UCC384 allows the device to be placed in a low quiescent current mode. The UCC384 is shut down by pulling the SD/CT pin more positive than –0.6V with respect to GND. Fig. 8 shows how a shutdown circuit can be configured for the UCC384 using a standard TTL signal to control it.

Controlling the SD/CT Pin

Forcing the SD/CT pin to any fixed voltage will affect the operation of the circuit. As mentioned before, pulling the SD/CT pin more positive than –0.6V will put the circuit in a shutdown mode, limiting the quiescent current to less than 45µA. Pulling this pin more positive than +6V with respect to GND will damage the device.

Forcing the SD/CT pin to any fixed voltage between –0.6V and –2.5V with respect to GND will cause the circuit to ignore an overcurrent condition. In this situation, the output will not be pulsed at a 2.5% duty cycle, but the output current will still be limited to the Peak Current Limit. This circuit maybe used where a fixed current limit is needed, while a 2.5% duty cycle is undesirable. The UCC384 will supply a maximum current in this configuration as long as the temperature of the device does not exceed the Over Temperature Shutdown. This will be determined by the Peak Current being supplied, the input and output voltages, and the type of heat sink being used. Thermal Design will be discussed later on in this data sheet.

APPLICATION INFORMATION (cont.)

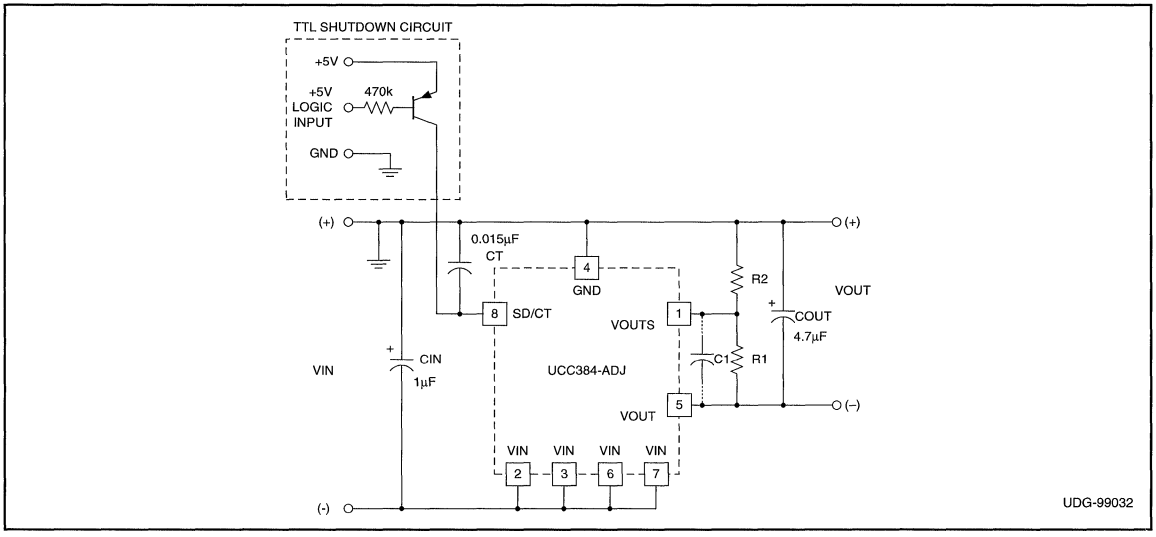


Figure 8. TTL controlled shutdown circuit for the UCC384.

Forcing the SD/CT pin to a voltage level between approximately –2.5V and –5V with respect to GND will turn the output off completely. The output will stay off as long as the voltage is applied. Pulling this pin more negative than –5V with respect to GND will damage the device.

Fig. 9 shows typical VOUT leakage current as a function of temperature during shutdown.

VIN to VOUT Delay

During power-up there is a delay between VIN and VOUT. The majority of this delay time is due to the charging time of the CT capacitor. When VIN moves more negative than the UVLO of the device with respect to GND, the CT capacitor will start to charge. A 17µA current sink is used only during power-up to charge the CT capacitor. When the voltage on the SD/CT pin reaches approximately –1.5V with respect to GND, the output will turn on and regulate. The larger the value of the CT capacitor, the greater the delay time between VIN and VOUT. Fig. 10 shows the VIN to VOUT startup delay, approximately 16ms, for a circuit with CT = 0.22µF.

Shorter delay times can be achieved with a smaller CT capacitor. The problem with a smaller CT capacitor is that with a very large load, the circuit may stay in overcurrent mode and never turn on. A circuit with a

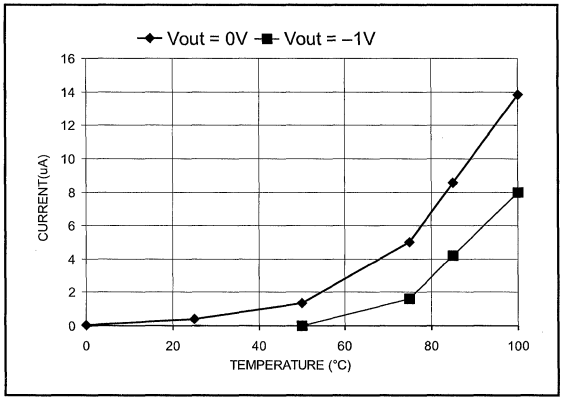


Figure 9. VOUT leakage current in shutdown (V_{IN} = –15V).

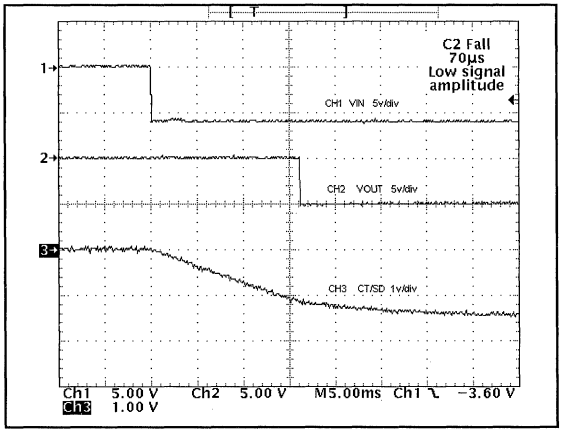


Figure 10. VIN to VOUT delay time during power-up with CT = 0.22µF.

APPLICATION INFORMATION (cont.)

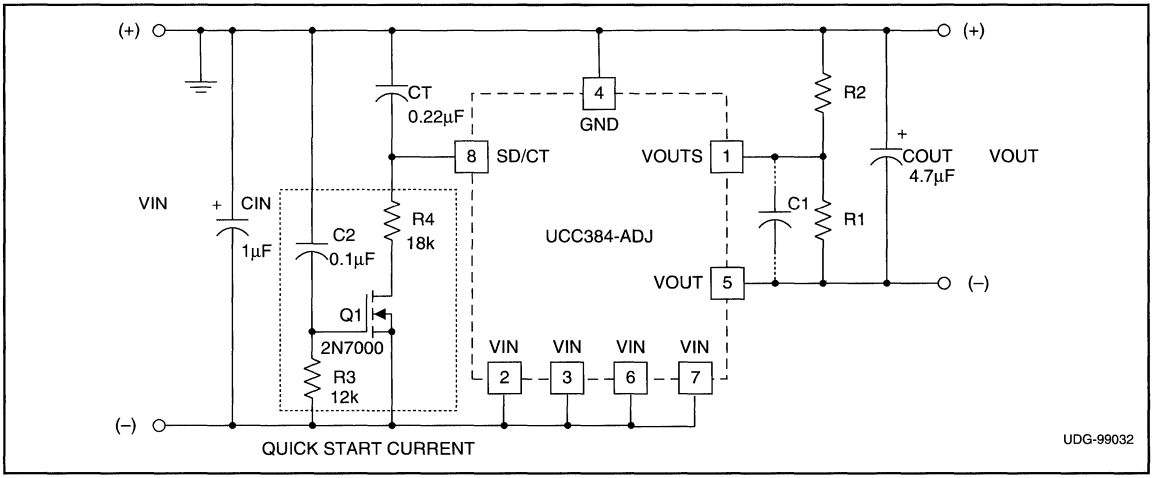


Figure 11. Quick start-up circuit for UCC384.

large capacitive load will need a large CT capacitor to operate properly.

One way to shorten the delay from VIN to VOUT during power-up, is by the use of the Quick Start-up circuit shown in Fig. 11.

With the Quick Start-Up circuit, the delay time between VIN and VOUT during start-up can be reduced dramatically. Fig. 12 shows that with the Quick Start-Up circuit, the VIN to VOUT delay time has been reduced to approximately 1ms.

Operation of the Quick Start-Up Circuit

During normal start-up, the UCC384 will not turn on until the voltage on the SD/CT pin reaches approximately –1.5V with respect to ground. It will take a certain amount of time for the CT capacitor to charge to this point. For a circuit that has a very large load, the CT capacitor will also need to be large in order for the overcurrent timing to work properly. A large value of capacitance on the SD/CT pin will increase the VIN to VOUT delay time.

The quick start-up circuit uses Q1 to quickly pull the SD/CT pin in a negative direction during start-up, thus decreasing the VIN to VOUT delay time. When VIN is applied to the circuit, Q1 turns on and starts to charge the CT capacitor. The current pulled through R4 will determine the rate at which CT is charged. R4 can be calculated as follows:

$$R4 = \frac{V_{IN}(V) \bullet T_D(\text{sec})}{1.5 \bullet CT(F)} \text{ Ohms} \qquad (6)$$

TD is the approximate VIN to VOUT delay time you wish to achieve.

Q1 will need to be turned off after a fixed time to prevent the SD/CT pin from going too far negative with respect to GND. If the SD/CT pin is allowed to go too far negative with respect to GND, the output will turn off again or possibly even damage the SD/CT pin. The maximum amount of time that Q1 should be allowed to be on is referred to as TM and can be calculated as follows:

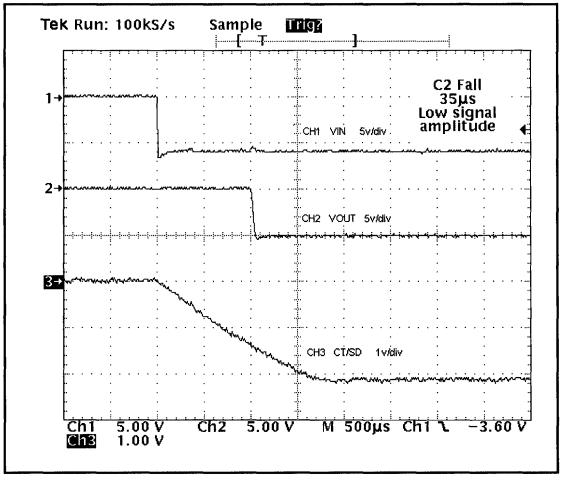


Figure 12. VIN to VOUT delay time with quick start-up circuit.

APPLICATION INFORMATION (cont.)

$$T_M = \frac{2.5}{1.5} \bullet T_D \text{ Seconds} \quad (7)$$

R3 along with C2 set the time that Q1 is allowed to be on. Since TM is the maximum amount of time that Q1 should be allowed to stay on, an added safety margin may be to use 0.9 • TM instead. This will ensure that Q1 is turned off in the proper amount of time. With a chosen value for C2, R3 can be calculated as follows:

$$R3 = \frac{0.9 \bullet T_M(\sec)}{C2(F) \bullet \ln \bullet \left(1 - \frac{V_{IN}(V) - 1.5}{V_{IN}(V)}\right)} \text{ Ohms} \quad (8)$$

After the CT capacitor has charged up for a time equal to 0.9 • TM , Q1 will turn off and allow the SD/CT pin to be pulled back to –1.5V with respect to GND through a 50k resistor. At this point , the SD/CT pin can be used by the UCC384 overcurrent timing control.

Minimum V_{IN} To V_{OUT} Delay Time

Although it may desirable to have as short a delay time as possible, a small portion of this delay time is fixed by the UCC384 and cannot be shortened. This is shown in Fig. 13, where the CT capacitor has been removed from the circuit completely, giving a fixed VIN to VOUT delay of approximately 150µs for a circuit with VIN = 6V and VOUT = 5V.

Thermal Design

The Packaging Information section of this data book contains reference material for the thermal ratings of various packages. The section also includes an excellent article entitled *Thermal Characteristics of Surface Mount Packages*, which is the basis for the following discussion.

Thermal design for the UCC384 includes two modes of operation, normal and pulsed. In normal mode, the linear regulator and heat sink must dissipate power equal to the maximum forward voltage drop multiplied by the maximum load current. Assuming a constant current load, the expected heat rise at the regulator's junction can be calculated as follows:

$$T_{RISE} = P_{DISS} \bullet (\theta jc + \theta ca)\ ^\circ C \quad (9)$$

Theta (θ) is the thermal resistance and P_{DISS} is the power dissipated. The junction to case thermal resistance (θ*jc*) of the SOIC-8 DP package is 22°C/W. In order to prevent the regulator from going into thermal shutdown, the case to ambient thermal resistance (θ*ja*) must keep the junction temperature below 150°C. If the UCC384 is mounted on a 5 square inch pad of 1 ounce copper, for example, the thermal resistance (θ*ja*) becomes 40-70 °C/W. If a lower thermal resistance is required by the application, the device heat sinking would need to be improved.

When the UCC384 is in a pulsed mode, due to an overcurrent condition, the maximum average power dissipation is calculated as follows:

$$P_{AVE} = \left[V_{IN}(V) - V_{OUT}(V)\right] \bullet I_{PEAK}(A) \bullet \left(\frac{T_{ON}(\sec)}{40 \bullet T_{ON}(\sec)}\right) Watts \quad (10)$$

As seen in equation 10, the average power during a fault is reduced dramatically by the duty cycle, allowing the heat sink to be sized for normal operation. Although the peak power in the regulator during the T_{ON} period can be significant, the thermal mass of the package will gener-

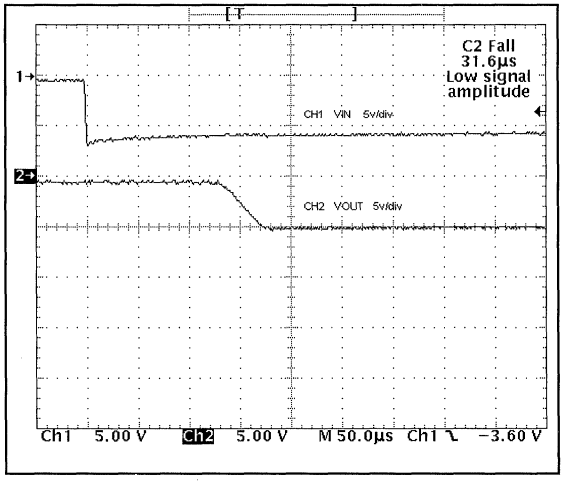


Figure 13. VIN to VOUT delay with CT capacitor removed.

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Low Dropout 200mA Linear Regulator

FEATURES

- Precision Positive Linear Voltage Regulator
- 0.2V Dropout at 200mA
- Guaranteed Reverse Input/Output Voltage Isolation with Low Leakage
- Adjustable Output Voltage (down to 1.25V)
- Load Independent Low Quiescent Current (10µA typ)
- Load Regulation of 5mV from 0mA to 200mA
- Logic Shutdown Capability
- Shutdown Quiescent Current below 2µA
- Short Circuit Protection - Duty Cycle Limiting
- Remote Load Voltage Sense for Accurate Load Regulation

DESCRIPTION

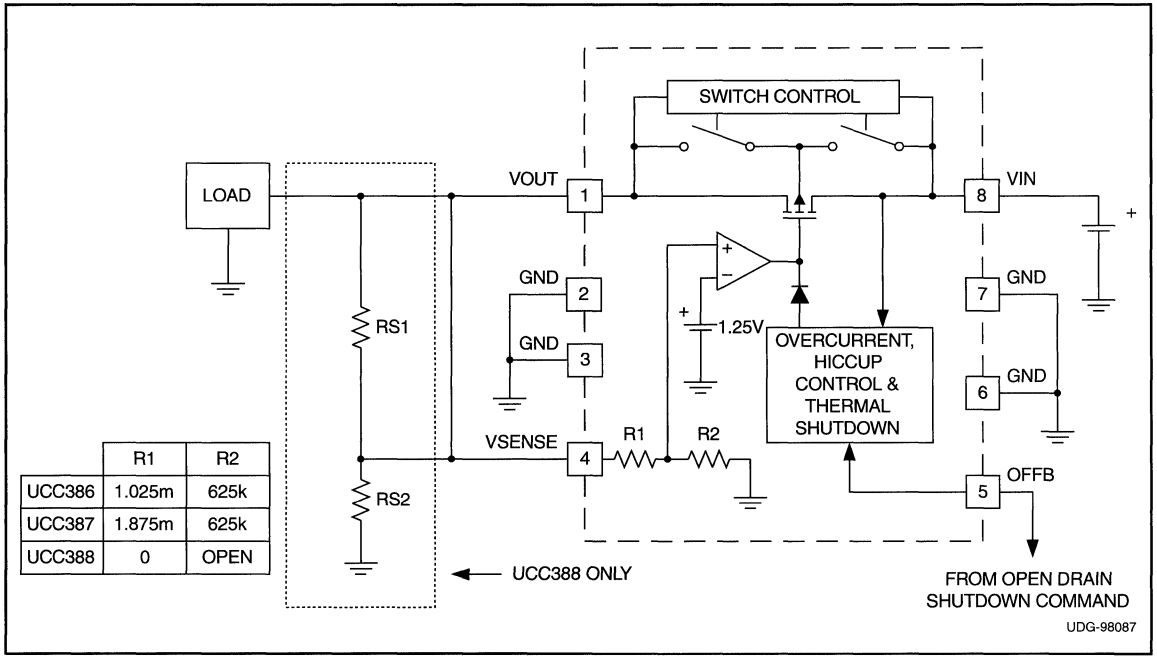
The UCC386/7/8 positive linear pass regulator series is tailored for low dropout applications where extremely low quiescent power is required. Fabricated with BiCMOS technology ideally suited for low input to output differential applications, the UCC386/7/8 will pass 200mA while requiring only 200mV of input voltage headroom. Quiescent current is typically less than 10µA. To prevent reverse current conduction, on-chip circuitry limits the minimum forward voltage to 50mV typical. Once the forward voltage limit is reached, the input-output differential voltage is maintained as the input voltage drops until undervoltage lockout disables the regulator.

The UCC386 has an on chip resistor network for preset to regulate at 3.3V, while the UCC387 has a fixed 5V output. The UCC388 requires an external resistor network which can be programmed for output voltages down to 1.25V. The output voltage is regulated to 1.5% at room temperature and better than 2.5% over the entire operating temperature range.

Short circuit current is internally limited. The device responds to a sustained overcurrent condition by limiting the duty cycle of the load to 12.5% typical. This drastically reduces the power dissipation during short circuit such that heat sinking, if at all required, must only accomodate normal operation.

(continued)

SIMPLIFIED BLOCK DIAGRAM AND APPLICATION CIRCUIT



	R1	R2
UCC386	1.025m	625k
UCC387	1.875m	625k
UCC388	0	OPEN

ABSOLUTE MAXIMUM RATINGS

VIN. 9V
OFFB . . . . . –0.3 to VIN+0.3V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature. . . . . –55°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

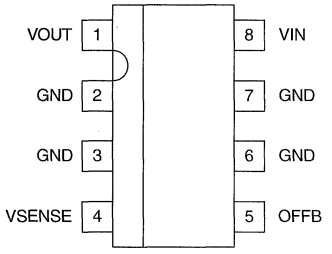
DESCRIPTION (cont.)

Internal power dissipation is further controlled with thermal overload protection circuitry. Thermal shutdown occurs if the junction temperature exceeds 140°C. The chip will remain in the off state until the temperature drops to 115°C.

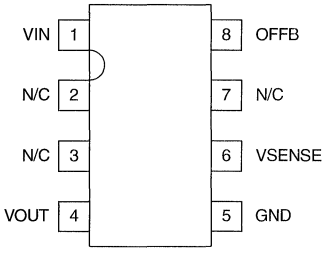
Pulling OFFB low commands a low power shutdown mode, which requires less than 2µA quiescent current. These devices are available in the 8 pin TSSOP (PW) and 8 pin SOIC (DP) surface mount power package. For other packaging options consult the factory.

CONNECTION DIAGRAMS

SOIC-8 (TOP VIEW)
DP Packages



TSSOP-8 (TOP VIEW)
PW Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications hold for: UCC386/7/8 $T_A = T_J = 0°C$ to 70°C; UCC286/7/8 $T_A = T_J = -40°C$ to 85°C; VIN = VOUT+1.5V, I_{OUT} = 0mA, C_{OUT} = 0.1µF

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UCC386 Fixed 3.3V Output					
Output Voltage	T_A=25°C	3.25	3.3	3.35	V
	Over Temperature	3.22	3.3	3.38	V
Line Regulation	VIN = 3.45V to 8.5V, I_{OUT} = 10mA		13	25	mV
Load Regulation	I_{OUT} = 1mA to 200mA		5	10	mV
Output Noise Voltage	T_J = 25°C, BW = 10Hz to 10kHz		200		μV_{RMS}
Dropout Voltage, VIN–VOUT	I_{OUT} = 200mA, VOUT = 3.20, T_A < 85°C		200	500	mV
	I_{OUT} = 50mA, VOUT = 3.20, T_A < 85°C		50		mV
Peak Current Limit	VOUT = 0V	350	550	750	mA
Overcurrent Threshold		225	325	400	mA
Current Limit Duty Cycle	VOUT = 0V		12.5	14	%
Overcurrent Timeout, T_{ON}	VOUT = 0V	550	750	950	µs
Quiescent Current	OFF = VIN		10	20	µA
Shutdown Quiescent Current	VIN ≤ 8.5V, OFF ≤ 0.5		2	5	µA
Shutdown Threshold	VIN = 8.5V	0		0.5	V
Reverse Leakage Current	0V < VIN < VOUT, VOUT < 3.35V, at VIN			10	µA
	0V < VIN < VOUT, VOUT < 3.35V, at VOUT			10	µA
Bias Current at VSENSE Pin			2		µA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications hold for: UCC386/7/8 $T_A = T_J = 0°C$ to 70°C; UCC286/7/8 $T_A = T_J = -40°C$ to 85°C; VIN = VOUT+1.5V, I_{OUT} = 0mA, C_{OUT} = 0.1µF

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UCC387 Fixed 5V Output					
Output Voltage	T_A=25°C	4.925	5	5.075	V
	Over Temperature	4.785	5	5.125	V
Line Regulation	VIN = 5.5V to 8.5V, I_{OUT} = 10mA		13	25	mV
Load Regulation	I_{OUT} = 1mA to 200mA		5	10	mV
Output Noise Voltage	T_J = 25°C, BW = 10Hz to 10kHz		200		μV_{RMS}
Dropout Voltage, VIN–VOUT	I_{OUT} = 200mA, VOUT = 4.75, T_A < 85°C		200	500	mV
	I_{OUT} = 50mA, VOUT = 4.75, T_A < 85°C		50		mV
Peak Current Limit	VOUT = 0V	350	550	750	mA
Overcurrent Threshold		225	325	400	mA
Current Limit Duty Cycle	VOUT = 0V		12.5	14	%
Overcurrent Timeout, T_{ON}	VOUT = 0V	550	750	950	µs
Quiescent Current	OFF = VIN		10	20	µA
Shutdown Quiescent Current	VIN ≤ 8.5V, OFF ≤ 0.5		2	5	µA
Shutdown Threshold	VIN = 8.5V	0		0.5	V
Reverse Leakage Current	0V < VIN < VOUT, VOUT < 3.35V, at VIN			10	µA
	0V < VIN < VOUT, VOUT < 3.35V, at VOUT			10	µA
Bias Current at VSENSE Pin			2		µA
UCC388 Adjustable Output					
Output Voltage	T_A=25°C	1.23	1.25	1.27	V
	Over Temperature	1.22	1.25	1.28	V
Line Regulation	VIN = VOUT +200mV to 8.5V for VIN > 2.0V, I_{OUT} = 10mA		10	40	mV
Load Regulation	I_{OUT} = 1mA to 200mA		5	10	mV
Output Noise Voltage	T_J = 25°C, BW = 10Hz to 10kHz		200		μV_{RMS}
Dropout Voltage, VIN–VOUT	I_{OUT} = 200mA, VOUT = 3.20, T_A < 85°C		200	500	mV
	I_{OUT} = 50mA, VOUT = 3.20, T_A < 85°C		50		mV
Peak Current Limit	VOUT = 0V	350	550	750	mA
Overcurrent Threshold		225	325	400	mA
Current Limit Duty Cycle	VOUT = 0V		12.5	14	%
Overcurrent Timeout, T_{ON}	VOUT = 0V	550	750	950	µs
Quiescent Current	OFF = VIN		10	20	µA
Shutdown Quiescent Current	VIN ≤ 8.5V, OFF ≤ 0.5		2	5	µA
Shutdown Threshold	VIN = 8.5V	0		0.5	V
Reverse Leakage Current	0V < VIN < VOUT, VOUT < 3.35V, at VIN			10	µA
	0V < VIN < VOUT, VOUT < 3.35V, at VOUT			10	µA
Bias Current at VSENSE Pin			50		nA

PIN DESCRIPTIONS

GND: Chip Ground. All voltages are measured with respect to this pin. This is the low noise ground reference for input regulation. The output decoupling capacitor should be tied between VOUT and GND.

OFFB: Shutdown, active low. This pin must be externally pulled to GND to turn off the IC. Pulling this pin high turns on the IC. This pin is internally pulled to VIN by 100nA current source.

VIN: Positive supply input for the regulator. Bypass this pin to GND with at least 0.1uF of low ESR, ESL capacitance if the source is located further than 1 inch from the device.

VOUT: Output of the regulator. The regulator does not require a minimum output capacitance for stability, however a small capacitor is recommended to improve transient response. Choose the appropriate size capacitor for the application with respect to the required transient loading. For example, if the load is very dynamic, a large capacitor will smooth out the response to load steps.

VSENSE: Externally programmable voltage sense node. For the UCC388, connect resistor divider network between VOUT, VSENSE and GND to provide custom regulation level. For the UCC386 and UCC387, connect this pin to VOUT as close to the load as possible.

APPLICATION INFORMATION

Load Independent Current Consumption. This series of LDO's is based on CMOS circuitry and uses a high side P channel pass element. Consequently, the current consumed by the LDO is extremely low at 10μA under normal operating conditions and does not vary with load. The shutdown mode (OFFB = GND) consumes only 2μA, making this series an excellent choice for battery applications.

Reverse Voltage Standoff. These LDO's are designed to operate with the voltage at the output greater than the voltage at the input. This can be an advantage where a circuit needs to be powered from two separate power sources that must be kept isolated, such as selecting between one of two or more batteries.

Overcurrent Protection. The UCC386/7/8 uses a fixed, absolute, current limit in conjunction with a timed overcurrent function that significantly reduces power dissipation in the event of a shorted load (see Figure 1). In this diagram, a 100mA load is applied to the output of the LDO. At some point, a fault is applied. When the current level exceeds the overcurrent threshold of about 300 mA, a timer is started. If the current does not fall below the overcurrent threshold before the timer times out, about 5.6ms, the LDO declares an overcurrent condition exists and turns off its output for about 5.6ms. Note that the output current is internally limited to 600mA. After the output has been off for 5.6ms, it is turned on for about 800μs and again limited to 600mA. If the current does not fall below the overcurrent threshold before the 800μs timer expires, the output is again turned off for 5.6ms. This process repeats itself until the fault condition is removed from the output of the LDO. The average current supplied to the faulted load by the LDO is approximately 112mA. This is well below the maximum rated current of 200mA o the LDO. Therefore, for most applications that have adequate thermal dissipation for the LDO to operate at full rated load, the thermal dissipation will also be adequate in a faulted condition.

Thermal Shutdown. The LDO's have a thermal shutdown circuit that will turn the LDO output off before the die temperature reaches damaging levels. When the die cools, the LDO will again function. The thermal shutdown circuit has a turn-off threshold of nominally 140°C, and a turn-on threshold of 115°C. These temperatures insure that the LDO will not be damaged due to excessive power dissipation.

Maximum Load Recovery. The LDO will start a load that has a large capacitance and a DC current component. One of the consequences of the LDO's fault behavior is a maximum output capacitor value and load current that the LDO can restart after an overcurrent condition has been declared. Fig. 2 shows the maximum load that the LDO can re-start from a faulted condition

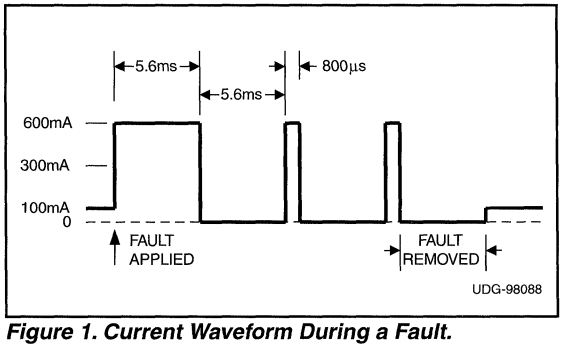


Figure 1. Current Waveform During a Fault.

APPLICATION INFORMATION (continued)

with a given output filter capacitor. Note that the LDO can start a much higher load than it can restart after a fault. If the LDO is hiccuping into a load that it cannot restart, either momentarily disconnecting the load or a power cycle will allow the LDO to start the load.

Using OFFB. The OFFB pin is used to turn the output of the LDO on or off from some external source. There are two things to note when using this pin. The first is that after taking OFFB high (on), the LDO will require up to about 2ms to start and stabilize. The second item is that OFFB is designed to be driven from an open drain type output. Internally, this pin is pulled high by a weak (100nA) current source, and will normally be at the input supply voltage, so the driving circuitry must be able to withstand the voltage applied to the input of the regulator. Also, depending upon load, if the OFFB pin is driven (overriding the internal pull-up) high with a fast edge signal, there may be a brief pulse on the output, followed by no output, with the regulator coming on and stabilizing about 2ms after the OFFB pin was driven high. This output pulse is never more than the normal output voltage of the regulator and is about 200μs in length.

Output Capacitance and Transient Response. The transient response of the regulator is heavily influenced by the capacitor on the output. In general, larger capacitors produce less voltage variation during load changes, but take longer to stabilize (quit wiggling). Note that no output capacitor is required for a stable output. However, if the load exhibits sharp changes in current requirements, and temporary deviations from the nominal output voltage must be minimized, some output filter capacitor will be needed.

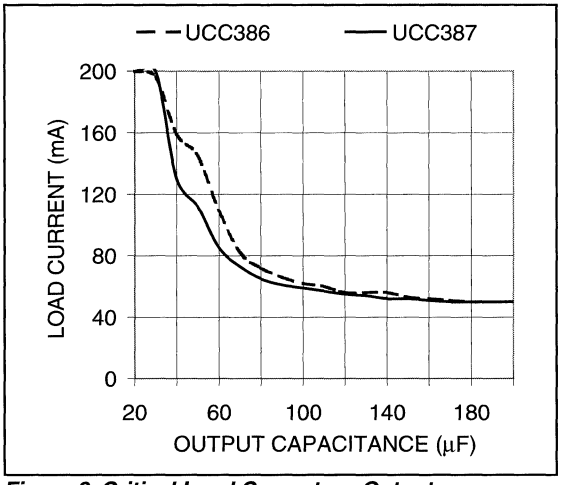


Figure 2. Critical Load Current vs. Output Capacitance

UCC388 Output Voltage Programming. Referring to the applications diagram on the front page of the data sheet, the output voltage is given by:

$$V_O = 1.25\left(\frac{R_{S1} + R_{S2}}{R_{S2}}\right)$$

Note that for the UCC388, the internal resistor R2 is open.

7

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Advanced Low Voltage Boost Controller With Backup Charger

FEATURES

- Synchronous Conversion with Internal MOSFETs
- FULL Load Operation and Start-up Guaranteed with 1V Input
- 85% Efficiency at 200mW Output, 85% Efficiency at 10mW Output
- Switch Mode Pulsed Charger for NiCD or SuperCap Backup
- Charger Efficiency: 82% at 45mA, 82% at 5mA
- LDO Post Regulation of Backup Source
- System Reset Function with Programmable Reset Period
- Programmable Low Output Voltage Warning Indicator and Battery Monitor
- Two General Purpose 1.5Ω switches

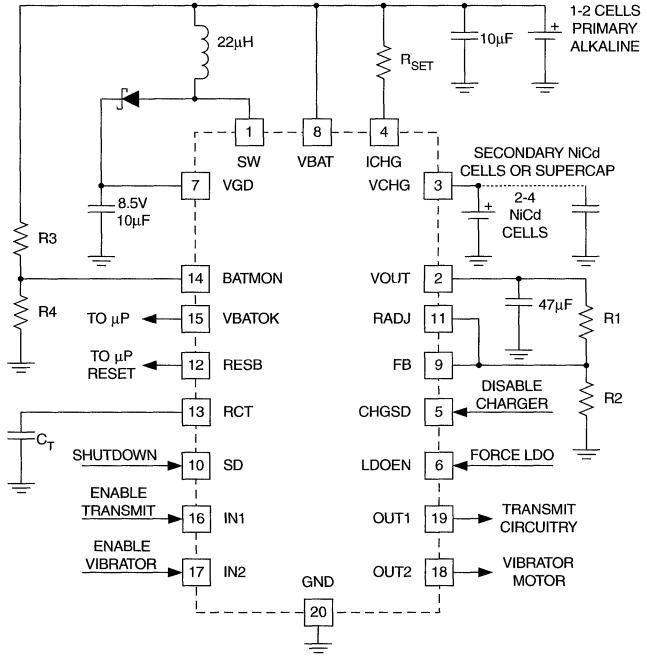
DESCRIPTION

The UCC39401 is a multi-output single inductor synchronous boost controller optimized to operate from a low input voltage such as a single or dual alkaline cell. The main output will start up under full load at input voltages typically as low as 0.8V, with a guaranteed maximum of 1V, and will operate down to 0.5V once the converter is operating. The input voltage range of the controller optimizes Alkaline cell utilization and can accommodate other chemistries such as NiCd and NiMH. Using internal MOSFETs, the main output is rated for 200mW and is adjustable from 1.5V to 5.0V. An auxiliary 8.5V 50mW output is also provided, primarily for the gate drive supply, which can be used for low current circuitry requiring a higher operating voltage.

The UCC39401 also incorporates a high efficiency pulsed current charger. The charger is used to maintain/restore capacity in a secondary power source such as a NiCd battery or SuperCap. The secondary power source can be used for memory back-up (through an integrated LDO) during primary battery replacement or failure. Power on Reset (POR) circuitry monitors the main output voltage during both normal and LDO backup operation.

(continued)

SIMPLIFIED APPLICATION DIAGRAM.



UDG-98155

ABSOLUTE MAXIMUM RATINGS

Voltage
VBAT, SD, CHGSD, LDOEN,IN1, IN2,
BATMON, VOUT, VCHG ..... –0.3V to 10V
VBATOK, RESB, OUT1, OUT2, SW, VGD .... –0.3V to 15V
RADJ Voltage ..... –0.3V to VOUT
RCT, FB, ICHG Voltage ..... –0.3V to VBAT

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

DESCRIPTION (cont.)

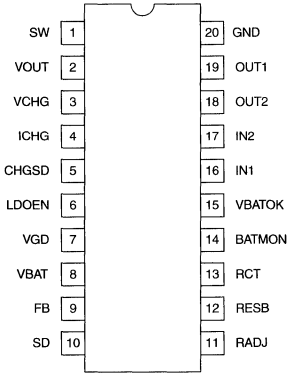
Demanding applications such as pagers, PDA's, and cell phones require high efficiency from several milli-watts to several hundred milli-watts. The UCC39401 accommodates these applications with >80% efficiencies over the wide range of operation. Efficiency at light loads is achieved by minimizing switching and conduction losses along with low controller operating currents. High efficiency at full load is realized with low Rdson synchronous switches along with continuous conduction mode operation.

The controller allows adjustment of the main output voltage, average charge current, reset threshold and reset period. Other features include a low battery detect circuit, two independent 1.5Ω alarm switches, and shutdown controls for the chip and charger. A typical pager application diagram is provided in this data sheet.

CONNECTION DIAGRAMS

DIP-20, (Top View)

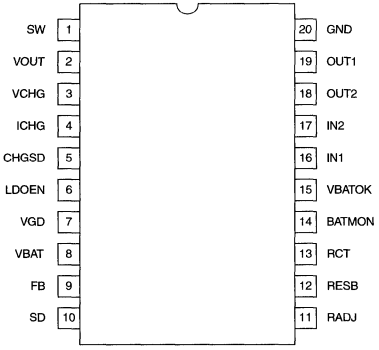
Packages



CONNECTION DIAGRAMS

TSSOP-20, (Top View)

Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise stated these parameters apply for T_J = 0°C to +70°C, for the UCC39401, –40°C to +85°C for the UCC29401, V_{BAT} = 1.25V $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VBAT Section					
Minimum Startup Voltage: No Ext. VDG Load, I_{OUT} = 200mW/VOUT	T_J = 25°C (Note 1)	0.4	0.8	1	V
	T_J = 0 to 70°C (Note 1)	0.5	0.9	1.1	V
Minimum Dropout Voltage	No External VGD Load, Iout = 10mA (note1)	0.3	0.4	0.5	V
Input Voltage Range				VOUT + 0.5V	V
Quiescent Supply Current			8	12	µA
Shutdown Supply Current	SD = Open (Internally pulled hi)		8	12	µA
Supply Current During Backup	LDOEN = Open (Internally pulled hi)		8	12	µA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated these parameters apply for T_J = 0°C to +70°C, for the UCC39401, –40°C to +85°C for the UCC29401, V_{BAT} = 1.25V $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VOUT Output Section					
Quiescent Supply Current			27	44	µA
Shutdown Supply Current	SD = Open (Internally pulled hi)		3	6	µA
FB Voltage 1V < VBAT < 3V	I_{OUT} = 0mA	1.16	1.20	1.24	V
	I_{OUT} < 200mW/VOUT (Note 1)	1.15	1.20	1.25	V
VGD Output Section					
Quiescent Supply Current due to VOUT only	SDCHRG = Open (internally pulled hi)		18	30	µA
Quiescent Supply Current due to VCHG only with R_{SET}=1MΩ	SDCHRG = GNDed		25	50	µA
Shutdown Supply Current	SD = Open (Internally pulled hi)		15	25	µA
Regulation Voltage 1V < VBAT < 3V	T_A = 25°C	8	8.5	9	V
	T_A = 0°C to 70°C	7.9	8.5	9.1	V
	0mA < I_{VGD} < 5.5mA (Note 1)	7.8	8.5	9.2	V
VCHG Output Section (2 to 4 NiCd Cells or a supercap) (L=22µH)					
Quiescent Supply Current			8	14	µA
Shutdown (charger only) Supply Current	CHGSD=Open (internally pulled hi)		8	14	µA
Shutdown Supply Current	SD = Open (Internally pulled hi)		3	5	µA
Quiescent Supply Current During BackUp	LDOEN = Open (Internally pulled hi)		45	70	µA
ICHG Range	Given by 6MEG/R_{SET}		6M/R_{SET}		mA
ICHG MINimum with R_{SET} = 1MΩ			6		mA
ICHG MAXimum Obtainable	Given by 0.180 X (VBAT/VCHG)		180 X (VBAT/VCHG)		mA
Inductor Charging Section (L = 22µH)					
ICHG Peak Discontinuous Current for VCHG		300	375	450	mA
Peak Discontinuous Current for V_{OUT} or VGD	Over Operating Range (Note 1)	180	225	270	mA
Peak Continuous Current for V_{OUT}	VBAT = 1.25V	385	550	715	mA
Charge Switch RDSon	PW Package		0.65	1	Ω
Current Limit Delay	(Note 1)		50		ns
Synchronous Rectifier Sections					
VOUT Nmos Rectifier RDSon	PW package		1.3	2	Ω
VCHG Nmos Rectifier RDSon	PW package		1.3	2	Ω
Shutdown Sections (SD, CHGSD, & LDOEN Pins)					
Threshold		500	750	1100	mV
Input Current	SD, CHGSD or LDOEN are Grounded	–1	–0.5	0	µA
RESET Section (@90% V_{OUT}); (RADJ pin Shorted to FB pin)					
Threshold		1.036	1.08	1.124	V
Reset Period	C_T = 150nF	110	160	210	ms
VOUT Finite Slope to Reset Delay	V_{OUT} falling @ –1mV/µs	30	60	90	µs
VOUT InFinite Slope to Reset Delay	V_{OUT} falling infinitely fast	10	20	30	µs
Sink Current		1	2	5	mA
Output Low Voltage	Sink Current = 2mA	20	50	100	mV
Output Hi Voltage Leakage Current	Open Drain Output @ 7V		0	0.5	µA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated these parameters apply for T_J = 0°C to +70°C, for the UCC39401, –40°C to +85°C for the UCC29401, V_{BAT} = 1.25V $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
LDO Section (via Backup Supply)					
Drop Out Voltage (VCHG – VOUT)	LDOEN = Open; I_{LOAD}VOUT = 10mA	50	100	200	mV
Automatic VCHG BackUp LDO Internal Comparator Threshold	Requires a Resistor Divider from VBAT (shared with VBATOK Comparators' Threshold); LDOEN = 0V	420	450	480	mV
Automatic VCHG BackUp LDO Internal Comparator Input Leakage Current		–0.5	0	0.5	µA
Low Battery Output Indicator					
VBATOK Comparator Threshold	Requires a Resistor Divider from VBAT	420	450	480	mV
Output Low Voltage	Sink Current = 1mA	20	100	200	mV
Output Hi Voltage Leakage Current	Open Drain Output @ 7V		0	0.5	µA
Alarm Switches					
Threshold		500	750	1100	mV
$R_{DS(on)}$	PW package		1	1.5	Ω

PIN DESCRIPTIONS

BATMON: This pin monitors the input voltage via a resistor divider. When the BATMON voltage falls below 450mV, VBATOK (open drain) pulls low and the backup LDO is automatically enabled.

CHGSD: When this pin is open a built-in 0.5µA current source pulls up on the pin, disabling the pulsed charger. When this pin is grounded the pulsed charger is enabled.

FB: This pin serves as the feedback control pin used to program the output voltage. Referring to the applications circuit, the output voltage is equal to 1.20V•(1+R1/R2).

GND: Ground of the IC.

ICHG: By placing a resistor (RSET) from this pin to VBAT, the user is able to program the amount of average charge current that the VCHG pin provides. The average charge current (when other outputs are not being serviced) is given by the following equation:

$$I_{AVE} = \frac{(280e6 \bullet L)}{R_{SET}}$$ (I in Amps, L in Henrys, R in Ω).

IN1: A high level (>1.1V) on this CMOS compatible pin drives OUT1 low.

IN2: A high level (>1.1V) on this CMOS compatible pin drives OUT2 low.

LDOEN: When this pin is open a built in 1µA current source pulls up on the pin, forcing the LDO to backup VOUT from the secondary power source (provided that VCHG >VOUT). When this pin is grounded, control of the LDO backup is relinquished to the internal battery comparator controlled by the BATMON pin. Should BATMON fall below 450mV, the LDO backup will automatically engage.

OUT1: An open drain alarm driver with a typical switch $R_{DS(on)}$ of 1Ω.

OUT2: An open drain alarm driver with a typical switch $R_{DS(on)}$ of 1Ω.

RADJ: This pin programs the level at which a reset is initiated. Noise glitch suppression is provided to prevent nuisance trips (see applications information). This pin is internally compared to 1.08V to determine the reset level. If wired directly to the FB pin, as in the applications diagram, the reset voltage is given by 1.08V•(1+R1/R2) or 10% below the regulated voltage.

RCT: This pin allows the user to adjust the reset period. The reset period is controlled by placing a capacitor CT from this pin to ground, where T (sec) = 1.20•C_T (µF).

RESB: This is the output pin of the reset circuit. If the RADJ pin goes below 1.08V (for a period longer than the glitch filter) RESB will produce a low level, resetting the system microprocessor. Once RADJ is brought above 1.08V, RESB will remain at a low level for a period set by the RCT pin.

PIN DESCRIPTIONS

SD: When this pin is open a built in 0.5µA current source pulls up on the pin, placing the IC in sleep or shutdown mode. When this pin is tied to ground the IC is enabled and both output voltages will regulate.

SW: This pin is the common switch node for the single inductor boost converter. The inductor, VGD Schottky diode, and 3 internal synchronous N-channel MOSFETs are connected at this pin. The N-channel MOSFETs are controlled by a state machine in the UCC39401, allowing 3 outputs to be serviced by time multiplexing energy in the inductor. During discontinuous portions of the inductor current a MOSFET resistively connects VBAT to SW, dampening excess circulating energy to eliminate undesired high frequency ringing.

VBAT: Input voltage to the converter. Bypass this pin to GND with a 10µF low ESR, ESL capacitor if the battery source is located further than 1 inch from the device.

VBATOK: Open drain output indication that the primary battery voltage is sufficient for operation. Should the battery voltage fall below the internal battery comparator level, set at the BATMON pin, this output will be pulled low.

VCHG: This pin provides the pulsed charge current for the secondary power source. The average charge current is programmed with the ICHG pin. This output has the lowest priority in the multiplexing scheme.

VGD: This pin is coarsely regulated around 8.5V and is primarily used for the gate drive supply for the power switches in the IC. This pin can be loaded with up to 50mW of additional load. The VGD supply can go as low as 7V without interfering with the servicing of the main output. Below 7V, VGD will have the highest priority, although practically the voltage should not decay to that level if the output capacitor is sized properly.

VOUT: Main output voltage, which is programmed with the FB pin, has highest priority in the multiplexing scheme (provided VGD is above its critical 7V level). This output is rated for 200mW with a 1V input using a 22µH inductor.

APPLICATION INFORMATION

Overview

A simplified block diagram of the UCC39401 in a typical application is shown in Fig. 1. The converter IC provides an integrated power solution for pagers and other portable devices that require operation from a low voltage primary battery source. The synchronous boost converter generates three outputs from a single inductor by time multiplexing the stored energy. The main output can be adjusted between 1.5V to 5.0V and provides up to 200mW of power.

An integrated pulsed charger is included to restore capacity to a secondary power source such as a NiCD battery or SuperCap. The average output current is adjustable with an RSET value placed between the VBAT and ICHG pins. If the VCHG output voltage rises above 5.75V, an internal safety comparator will prevent further charging. During replacement of the primary battery, the UCC39401 automatically backs-up the main output from the secondary power source via an internal low dropout regulator.

An auxiliary 8.5V output is also generated to provide for an increased gate drive voltage for the synchronous switches. This output can be used to power higher voltage circuitry (up to 50mW) such as an LCD display, Op-Amp circuit, communications port, or a 5V supply through a linear regulator. A reset function and various supervisory features are also included to improve system integration.

Multiplexed Coil Technique

The UCC39401 incorporates a unique multiplexed coil technique to generate three outputs from a single inductor. Energy pulses stored in the inductor are time shared between the outputs, depending upon loading and whether the pulsed charger is enabled. Fig. 2 shows a simplified schematic of the basic topology.

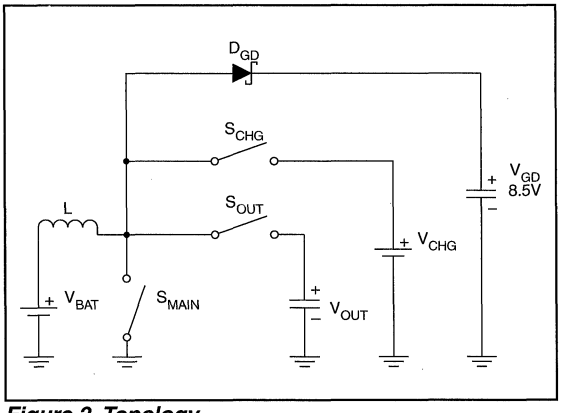


Figure 2. Topology.

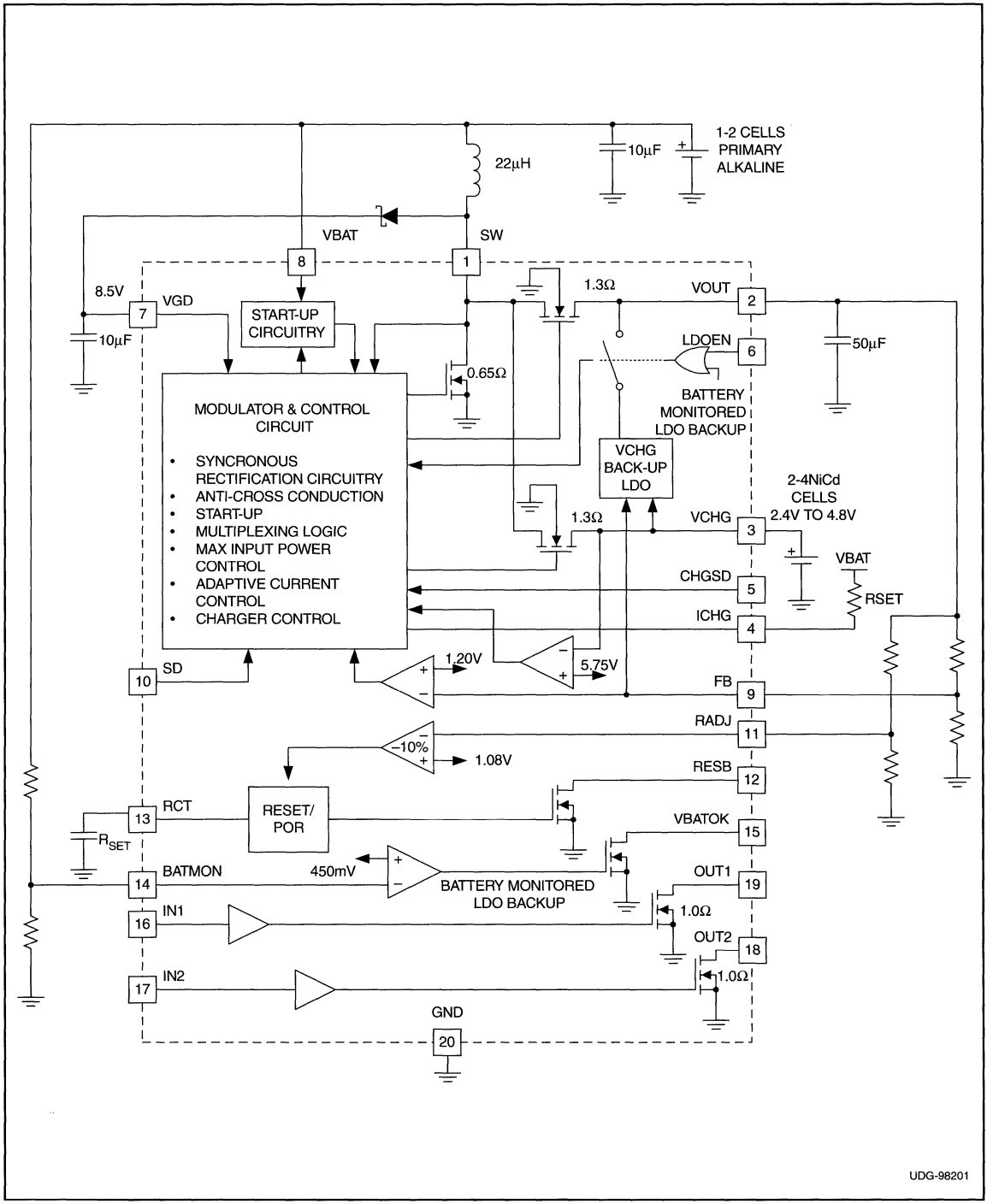


Figure 1. Advanced pager power controller.

APPLICATION INFORMATION

Referring to Fig. 2, VBAT is the primary battery source, VOUT is the main output voltage, VCHG is the output of the pulsed charger, and VGD is the gate drive voltage. If one of the outputs requires service Smain turns on, causing current to ramp up in the inductor (L). Once the inductor current reaches its peak value, the UCC39401 delivers the current to the proper output. If the main output (VOUT) requires service, Sout closes the instant Smain is open and energy is delivered to VOUT. The main output can be serviced with either discontinuous or continuous current in the inductor (discussed later). If the pulsed charger (VCHG) requires service, Schg closes the instant Smain is open and inductor current is delivered to the secondary source (VCHG). If VGD requires servicing, Sout and Schg are left open and inductor current is forced through Dgd to the gate drive supply (VGD). Due to the presence of large peak currents in the inductor, low ESL, ESR capacitors should be used to maintain low ripple voltages on the outputs.

Arbitration

A priority scheme is required to accommodate the multiple supply voltages, while providing effective start-up and servicing of the outputs at various load conditions. The arbitration rules for the main output (VOUT), gate drive supply (VGD), and pulsed charger (VCHG) are as follows:

- If VGD < 7.0V, VGD will get priority for service. (occurs during start-up)
- If VGD > 7.0V and VOUT < 1.20(1+R1/R2), VOUT will get priority for service.
- If VGD < 8.5V and VOUT > 1.20(1+R1/R2), VGD will get priority for service.
- If VGD > 8.5V, VOUT > 1.20(1+R1/R2), VCHG < 5.75V and the pulsed charger is enabled, VCHG will be serviced at a rate programmed by ICHG.

In order to guarantee an orderly start-up with input voltages below 1V, the gate drive supply (VGD) is given priority during start-up. Fig. 3 shows oscilloscope waveforms of current and voltage during startup (VOUT is programmed at 3.3V, VCHG is disabled).

At time t0, an internal 200kHz oscillator toggles the main switch at 50% duty cycle and starts VGD rising. VGD gets to a sufficient voltage at time t1 to run the IC in a normal operating mode. At time t2, VGD has reached its lower threshold of 7.0V and the arbitration allows VOUT to get started. VOUT has reached 3.3V at time t3, and VGD is allowed to charge to 8.5V. At time t4, both outputs are in regulation and the converter operates normally, servicing the outputs as the load demands.

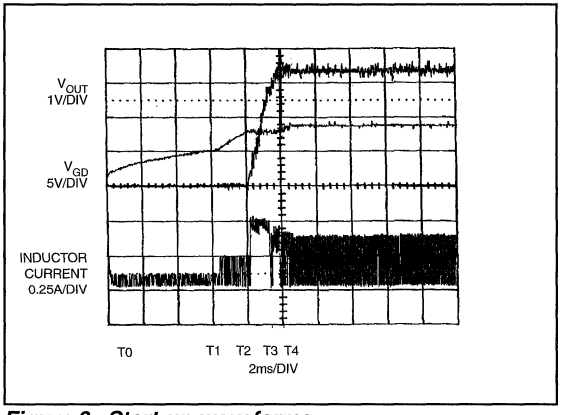


Figure 3. Start-up waveforms.

Multiplexed Waveforms (VOUT and VGD)

The UCC39401 converter operates with a hysteretic (variable frequency) control technique. Regulation is achieved by monitoring the various output voltages with comparators internal to the control IC. If an output falls below its voltage threshold, the converter will deliver a single or multiple energy pulses to that output until the output comes into regulation. A single 22µH inductor is used to generate the energy pulses.

Unique control circuitry provides high efficiency power conversion of the main output, for both light and heavy loads, by transitioning between discontinuous and continuous conduction based on load conditions (see Fig. 4). The inductor charge time is controlled by: Ton=5.0µs/VBAT. In discontinuous conduction mode, this results in a constant peak current regardless of the input voltage. For a 22µH inductor, the resulting peak current is approximately 225mA.

Constant on time control is maintained, unless the inductor current reaches the I_{MAX} limit. In order to provide for constant output power capability, the I_{MAX} limit scales slightly with input voltage. The I_{MAX} limit for a 1.25V input is 550mA, for example, while the Imax limit for 2.5V is 400mA. Once the inductor current becomes continuous, the discharge time is fixed at T_{OFF}=1.0µs, until the main output rises above its threshold voltage. The short off time reduces the inductor's ripple current in continuous mode operation and allows the inductor current to transition to the I_{MAX} limit if a single discontinuous pulse is not adequate.

APPLICATION INFORMATION (cont.)

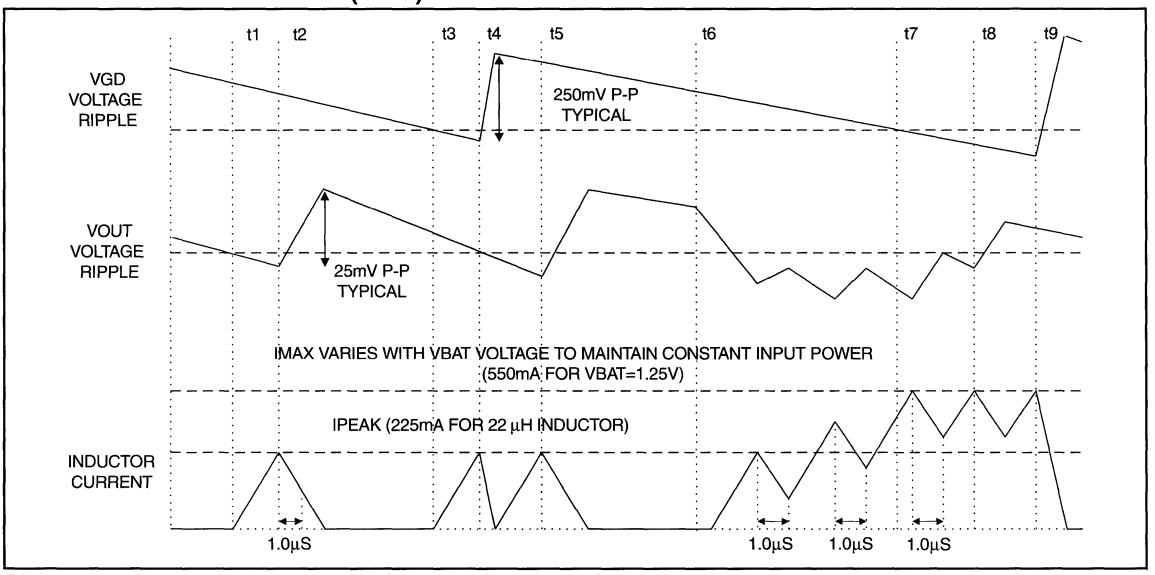


Figure 4. Multiplexed inductor servicing the VOUT and VGD outputs.

Typical Cycle

Fig. 4 depicts typical voltage and current waveforms of the converter servicing the VOUT and VGD outputs. It will be assumed that the pulsed charger is disabled or does not require servicing. At time t1, VOUT drops below its threshold, and the inductor is charged for 5.0µs/VBAT. At time t2, the inductor begins to discharge with a minimum off time of 1.0µs. Under lightly loaded conditions the amount of energy delivered in this single pulse would satisfy the voltage control loop, and the converter would not command any more energy pulses until the output again drops below the voltage threshold.

At time t3, the VGD supply has dropped below its threshold, but VOUT is still above its threshold point. This results in an energy pulse to the gate drive supply at t4. However, while the gate drive is being serviced, VOUT has dropped below its lower threshold, so the state machine commands an energy pulse to VOUT as soon as the gate drive pulse is completed (time t5). Hysteresis (250mV) is added to the VGD comparator to prevent oscillations between VOUT and VGD servicing.

Time t6, represents a transition between light and heavy loads. A single energy pulse is not sufficient to force the main output voltage above its threshold before the minimum off time has expired, and a second charge cycle is commanded. Since the inductor current does not reach zero in this case, the peak current is greater than 225mA at the end of the next charge on time. This results in a ratcheting of inductor current until either the output voltage is satisfied, or the converter reaches its maximum current limit (Imax). At time t7, the gate drive voltage has dropped below its higher 8.5V threshold but the converter continues to service the output because it has highest priority, unless VGD drops below its lower 7.0V threshold.

Between t7 and t8, the converter reaches its maximum current limit (Imax). Imax is determined by integrated power limit circuitry and varies with VBAT. Once this limit is reached, the converter operates in continuous mode with approximately 60mA of ripple current. A time t8, the output voltage is satisfied, and the converter can service VGD, which occurs at t9. During all of these times the pulsed charger is not serviced since it is disabled.

Pulsed Charger Operation

The UCC39401 provides an output that allows a secondary power source such as a NiCd battery or SuperCap to be charged during normal operation. This secondary source can be used to backup the main output during alkaline replacement or failure through an internal linear regulator. The source can also be used to provide a low impedance for an RF power amplifier. The average current delivered by the pulsed charger is programmed with the RSET resistor tied between VBAT and ICHG. The average charge current is given by:

$$I_{AVE} = \frac{(I_{PCHG})^2 \bullet L}{500 \bullet 10^{-12} \bullet R_{SET}} \ Amps \qquad (1)$$

APPLICATION INFORMATION (CONT.)

Where IPCHG is the peak current allowed through the inductor by the pulse charger which is approximately 375mA. Assuming a 22µH inductor, the expression for average current simplifies to:

$$I_{AVE} = \frac{6 \bullet 10^6}{R_{SET}}\ mA \qquad (2)$$

Minimum average current is a function of the R_{SET} value, a 1MΩ R_{SET} results in a 6mA average charge current. Since the charger is operated in discontinuous conduction mode (DCM) there is a maximum achievable average current given by:

$$I_{MAX} = \frac{I_{PCHG} \bullet VBAT}{2 \bullet VCHG}\ Amps = \frac{375 \bullet VBAT}{2 \bullet VCHG}\ mA \qquad (3)$$

A 1.25V battery, for example, can charge a 3 cell NiCd stack (3.6V) at 65mA.

Constant Trickle Charge:

If a secondary NiCd battery is used to provide backup during Alkaline replacement, a constant C/16 or C/40 trickle charge is typically applied to the NiCd to maintain capacity. Fig. 5 shows inductor current and V_{CHG} waveforms during a constant trickle charge. The R_{SET} pin programs the charge current resulting in a pulse rate T_{CHG}. The charger shutdown pin CHGSD is tied high or left floating, keeping the charger continually enabled.

At time t1, the charger's timer expires and the UCC39401 allows inductor current to ramp up to an I_{PCHG} of 375mA. The inductor energy is then transferred to the NiCd producing a small ripple voltage on V_{CHG} (caused by inductor current and the ESR of the battery). At time t2 the charge timer has again expired and the UCC39401 delivers a packet of energy to the NiCd. At time t3, VGD requests servicing but must wait until the NiCd cycle is completed. The system microprocessor requires continuous current at time t4, and the charge timer request at t5 is stored but not serviced. The charger is allowed to service the t5 request at time t6, only to have the charge timer request a new pulse at time t7.

Gated Full Rate Charging

If the secondary source is used for purposes other than backup (i.e. RF transmission) it may be necessary to control the charger with the system microprocessor in order to quickly restore energy to the backup battery. This situation is illustrated in Fig. 6, where the average current is programmed near the maximum rate and the CHGSD pin is used to gate the charging.

Between t1 and t2 the UCC39401 is servicing VOUT and VGD with heavy loading on the main output; the secondary battery has also been heavily utilized and needs to have capacity restored. At time t2 the V_{OUT} load is decreased and the system microprocessor toggles the CHGSD pin at time t3 allowing battery charging. A low R_{SET} value is connected to the ICHG pin, setting the charger near its maximum rate. Inductor current is allowed to ramp to the I_{PCHG} limit and repetitive pulses are applied to the battery, restoring capacity. VGD requires service at time t5, the charger attempts to catch up to the timer before it is disabled at time t6.

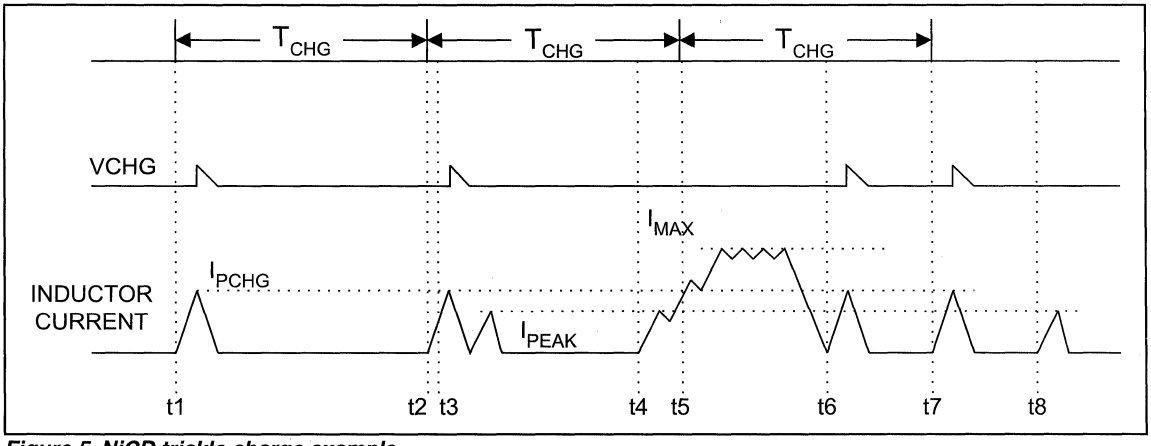


Figure 5. NiCD trickle charge example.

APPLICATION INFORMATION (cont.)

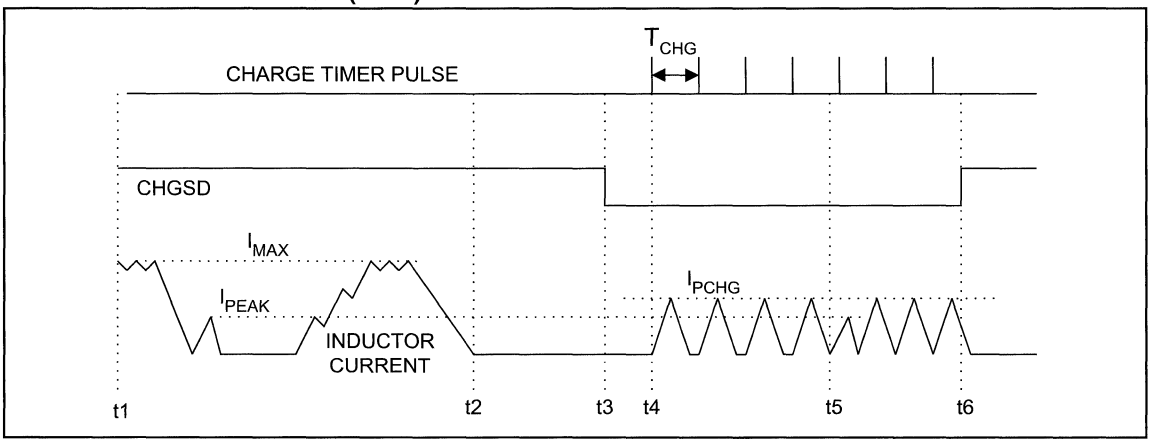


Figure 6. Gated full charge example.

SuperCap Charging

High capacity "super" capacitors are often used in place of traditional backup batteries for environmental and cost reasons. Unlike a NiCd battery, a constant trickle charge applied to a SuperCap will result in an increasing voltage. In order to prevent an over-voltage on the capacitor, the UCC39401 automatically disables the charger above 5.75V. If the SuperCap voltage needs to be regulated to a lower value, the CHGSD pin can be used to disable charge current above a specified voltage.

SYSTEM EFFICIENCY

Portable equipment requires the power converter to deliver 10's of milliamps to the load when the device is fully functioning. In standby mode however, where the device spends a majority of time, the equipment may require only 100's of microamps. The amount of time the device spends in various modes is heavily dependent upon the user. Because it is difficult to predict how often the device will be used, it is important that the converter operates efficiently over a wide dynamic load range in order to maximize battery lifetime.

Discontinuous Mode

In order to support a wide dynamic load range with a reasonably small value of inductance, the boost converter needs to operate in Discontinuous Conduction Mode (DCM) at medium and light loads. In order to maintain high efficiency over a wide load range, the UCC39401 uses a Pulsed Frequency Mode (PFM) of operation where the peak inductor current is held constant and cycle time (T_{CYCLE}) is varied to accommodate load variations. Fig. 7 shows inductor current in discontinuous conduction mode.

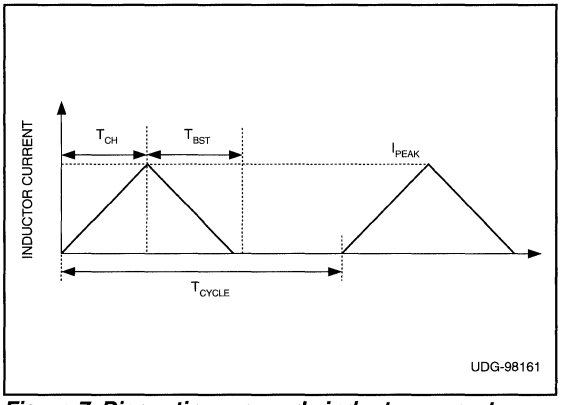


Figure 7. Discontinuous mode inductor current.

An analysis of the converter losses is useful in determining the peak inductor current that will optimize DCM efficiency. Fig. 8 shows a synchronous boost converter along with the equivalent circuit elements that are major contributors to power loss. This model is valid for either the VOUT or VCHG outputs of the UCC39401 (switch capacitances have been reflected to the gate for simplicity).

DCM efficiency for either the VOUT or VCHG output can be calculated from the input energy and loss energy for a single conversion cycle (T_{CYCLE}). Based on the waveforms of Fig. 7 and the circuit elements of Fig. 8, Table 1 gives equations for single cycle energy values and the resulting overall efficiency.

Once the values of the circuit elements (Fig. 8) are known, these equations can be used to determine the optimum peak inductor current for the converter in DCM. Fig. 9 depicts a typical efficiency curve for the UCC39401 main output (VOUT) as the peak inductor current is varied.

APPLICATION INFORMATION (cont.)

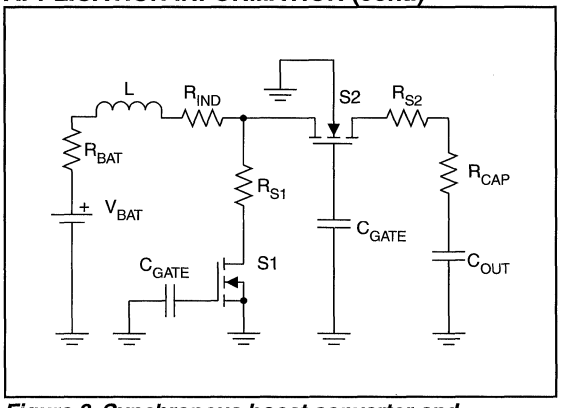


Figure 8. Synchronous boost converter and equivalent circuit elements.

Input Energy

$$E_{IN} = \frac{1}{2} \bullet I_{PEAK} \bullet V_{BAT} (T_{CH} + T_{BST}) \quad (4)$$

Conduction Energy Lost

$$E_{CONDUCTION} = \frac{(I_{PEAK})^2}{3} (R_{CH} T_{CH} + R_{BST} T_{BST}) \quad (5)$$

Where:

$$R_{CH} = R_{BAT} + R_{IND} + R_{S1}$$
$$R_{BST} = R_{BAT} + R_{IND} + R_{S2} + R_{CAP}$$

Switching Energy Lost

$$E_{SWITCH} = 2 \bullet C_{GATE} \bullet (V_{GD})^2 \quad (6)$$

Table 1. Input and lost energy for a single conversion cycle in discontinuous conduction mode (DCM)

As shown in Fig. 9, conduction losses dominate with large peak currents, where switching losses dominate with small peak currents. It is interesting to note that in discontinuous conduction mode, the optimum peak inductor current is independent of load current (see Table 1 equations). The optimum peak current calculated for VOUT is 225mA with an efficiency of 90%. The optimum peak current calculated for the charger output (VCHG) is

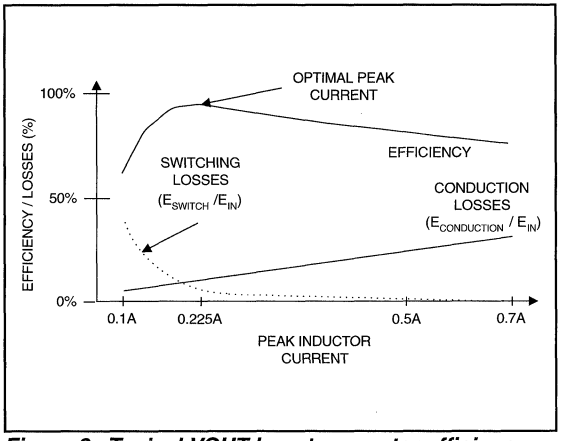


Figure 9. Typical VOUT boost converter efficiency vs. peak inductor current.

375mA with an efficiency of 85%. The peak current for both outputs was optimized for a 22µH boost inductor.

In previous discussions, the effects of control chip quiescent currents on efficiency have been ignored. The quiescent (I_{DD}) energy lost during a single conversion cycle is affected by the conversion period (T_{CYCLE}) which is a function of the load current. As T_{CYCLE} increases at light loads, the I_{DD} energy lost will also increase, thereby reducing efficiency. Equation 8 relates the optimal efficiency (ignoring I_{DD} and operating in DCM at the optimal peak current) to efficiency taking I_{DD} into account. Notice that optimal system efficiency is reduced by 50% when I_{DD} is equal to I_{LOAD}.

$$\eta_{WITH\_IDD} = \frac{\eta}{\left(1 + \frac{I_{DD}}{I_{LOAD}}\right)}\% \quad (8)$$

Since the VGD output supplies the gate drive voltage for both VOUT and VCHG, the I_{DD} current supplied by the VGD output has been broken into two components on the Electrical Characteristics Table, this way VOUT and VCHG efficiencies can be calculated separately.

Continuous Mode Operation

Discontinuous conduction mode results in a simple control scheme, however, the average load current (reflected to the input) is limited to less than half the peak current. If the peak current is increased, efficiency and the output voltage ripple will suffer. In order to provide increased load current, the converter is allowed to transition into Continuous Conduction Mode (CCM) when servicing the main output (see Fig. 10).

APPLICATION INFORMATION (cont.)

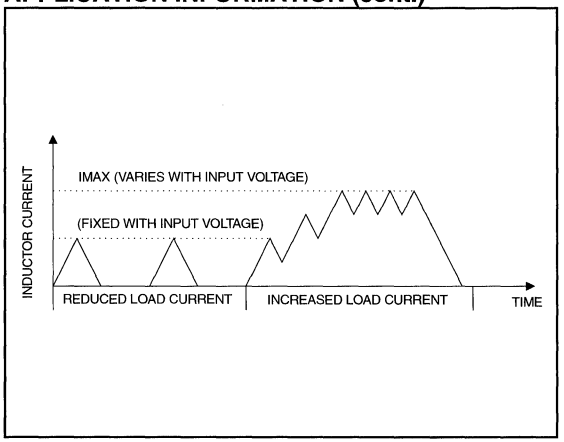


Figure 10. Adaptive current mode control.

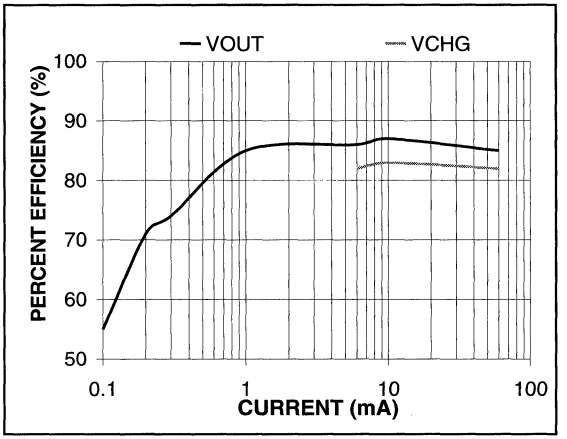


Figure 11. VOUT and VCHG efficiency as a function of load current. (VBAT=1.25V, VOUT=3.3V, VCHG=3.6V)

If a single discontinuous mode energy pulse is not sufficient to bring the main output into regulation, the current in the inductor is allowed to increase until a maximum current (I_{MAX}) is reached. In order to maintain a constant input power capability when the battery voltage decreases, I_{MAX} is automatically varied with input voltage as follows:

$$I_{MAX} \propto \frac{1}{V_{BAT}} \qquad (9)$$

For example, I_{MAX} with a 2.5V input is 400mA, for a 1.25V input it becomes 550mA. Since I_{MAX} is greater than the optimal peak current for the converter, efficiency in CCM is reduced slightly.

Efficiency Curves

Continuous conduction mode allows increased output power, while discontinuous PFM mode delivers optimal efficiency at light loads. By providing efficient conversion over the usable battery voltage in both modes, operation time is maximized. Fig. 11 shows efficiencies versus load current for the main and charger outputs over a wide load range.

Charger efficiency includes converter losses in transferring charge from the Alkaline battery to the backup source. If the backup source is a battery, it can typically be trickle charged at a reduced rate (C/16 for example) indefinitely, with the excess energy being converted to heat in the battery. In this case the charger efficiency may be high, but the energy pulled from the Alkaline is being wasted. Therefore, it is important to trickle charge the secondary battery at the lowest possible rate (just above the worst case self discharge) in order to maximize the runtime of the primary Alkaline battery.

Component Selection

An inductor value of 22µH will work well in most applications, but values between 10µH to 100µH are also acceptable. Lower value inductors typically offer lower ESR and smaller physical size. Due to the nature of the "bang-bang" controllers, larger inductor values will typically result in larger overall voltage ripple, because once the output voltage level is satisfied the converter goes discontinuous, resulting in the residual energy of inductor causing overshoot. It is recommended to keep the ESR of the inductor below 0.25Ω for 200mW applications. A Coilcraft DS1608C-223 surface mount inductor is one choice since it has a current rating of 0.7A and a maximum ESR of 110mΩ. Other choices for surface mount inductors are shown in Table 2.

Manufacturer Part Number	Phone	Nominal Value	Max ESR	Max Current
Coilcraft DO1608C-223	800-332-2645	22µH	370 mΩ	0.8 Amps
Coilcraft DS1608C-223	800-332-2645	22µH (shielded)	110 mΩ	0.7 Amps
Coiltronics CTX5-1P	561-241-7876	20µH (toroidal)	160 mΩ	1 Amp
Sumida CDH73	847-956-0666	22µH	180 mΩ	0.8 Amps

Table 2. Inductor recommendations.

Once the inductor value is selected the capacitor value will determine the ripple of the converter's main output. The worst case peak to peak ripple is primarily determined by two components of the capacitor (assuming the ESL is low for a surface mount package), one is due to

APPLICATION INFORMATION (cont.)

the charge storage characteristic, and the other is the ESR of the capacitor. The worst case ripple occurs when the inductor is operating at maximum current and is expressed as follows:

$$\Delta V = \frac{(I_{MAX})^2 L}{2C_{OUT}(VOUT - VBAT)} + I_{MAX}C_{ESR} \quad Volts \tag{10}$$

Where:

I_{MAX} = the peak inductor current

C_{OUT} = output capacitor value

C_{ESR} = ESR of the output capacitor

A Sanyo OS-CON series surface mount capacitor (10SN100M) is one recommendation. This part has an ESR rating of 90mΩ at 100µF. Other potential capacitor sources are shown in Table 3.

Manufacturer	Capacitor Family
Sanyo www.sanyo.com	OS-CON
AVX 803-448-9411	TPS series
Sprague 207-324-7223	593 and 594 series (591 low profile)
Kemet	T495, T510

Table 3. Capacitor Recommendations

VGD output ripple is primarily determined by the hysteresis of the internal comparator (250mV). A low ESR 10µF capacitor is recommended at this output to minimize additional output ripple due to the pulsed currents. Since the pulsed charger's holdup capacity is typically large, the VCHG output ripple is mainly a function of the secondary battery or Super Capacitor's ESR. Due to its low input voltage requirement, the UCC39401 does not require a large decoupling capacitor on the VBAT input to operate properly, a 10µF cap is sufficient for most applications. The addition of low value ceramic capacitors on the input and output pins (0.1µF for example) will reduce high frequency noise. For noise sensitive applications, further ripple rejection on the main output is possible with an LC filter and/or a linear post regulator.

The Backup Linear Regulator (LDO)

The backup circuitry is intended to prevent the loss of VOUT under low alkaline battery conditions. A block diagram of the UCC39401's backup circuitry is shown in Fig. 12. The backup circuitry is enabled with either the LDOEN or BATMON pins. When LDOEN is open or driven to a logic 1, the linear regulator is enabled (forced), regardless of the condition of the alkaline battery. When the LDOEN pin is grounded or driven to a logic 0, the backup circuity will be automatically enabled when the alkaline battery is too low. The low battery threshold is set by using 2 external resistors connected between VBAT, BATMON, and GND. If two equal value resistors are used, the VBATOK output will go low and an automatic LDO backup will occur when the alkaline battery decays below 0.9V.

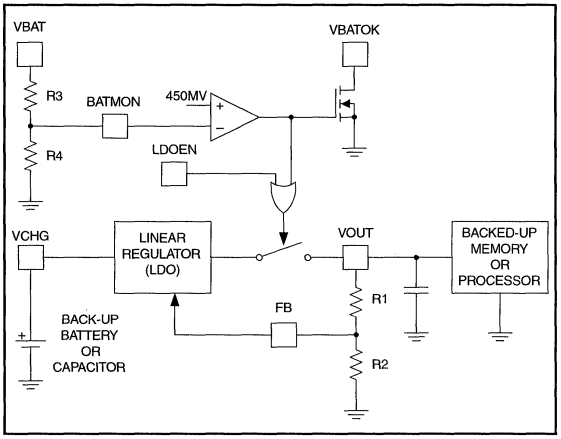


Figure 12. LDO backup circuitry.

During "Backup", the boost converter is shutdown and the LDO regulates the VOUT voltage (programmed at the FB pin). The output will maintain regulation as long as VCHG is greater than VOUT plus the dropout voltage of the LDO. The dropout voltage of the regulator is determined by the load current and minimum RDSon of the regulator. The RDSon of the regulator is guaranteed to be less than 20Ω, this corresponds to a 200mV dropout voltage with a 10mA load. If VCHG falls to within 50mV of VOUT, the internal LDO is disabled and the connection between VOUT and VCHG is "open".

Reset Circuit

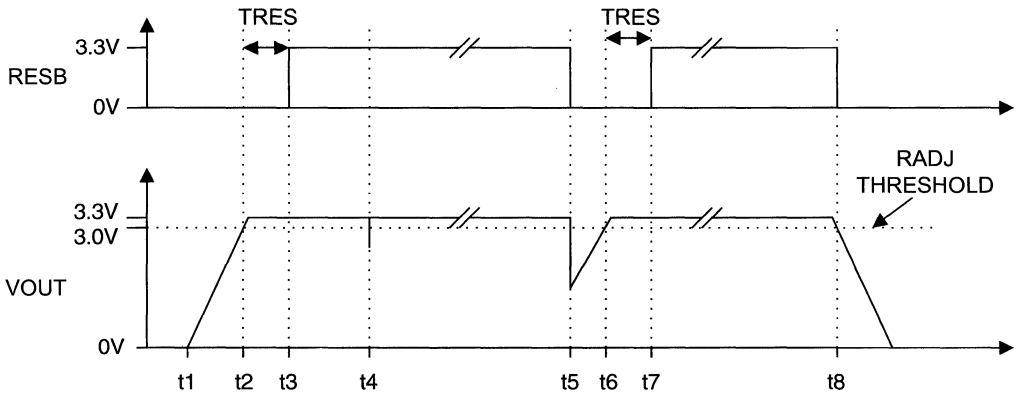
The UCC39401 allows the reset trip voltage to be programmed with two external resistors. By connecting the RADJ pin to the FB pin, the resulting reset level is 90% of the regulated output level. In most applications VOUT is monitored by the reset circuit, however, the design allows voltages other than VOUT to be monitored. Referring to the simplified applications diagram, the voltage below which reset will be asserted is determined by:

$$V_{RES} = 1.08 \bullet \left(1 + \frac{R1}{R2}\right) \bullet V_{OUT} \quad Volts \tag{11}$$

Once VOUT rises above the programmed threshold, RESB remains low for the reset period defined by:

$$t_{RES} = 1.20 \bullet C_T \quad seconds \tag{12}$$

APPLICATION INFORMATION (cont.)



t1: New Alkaline cell is inserted, RESB pulls low.

t2: VOUT boosted to greater than the programmed threshold, RESB remains low for TRES.

t3: TRES expires, RESB pulls high.

t4: Voltage glitch occurs, but is filtered at the RADJ pin, RESB remains high.

t5: Voltage glitch occurs whose magnitude and duration is greater than the RADJ filter, RESB is asserted.

t6: VOUT programmed threshold, RESB remains low for TRES.

t7: TRES expires, RESB pulls high.

t8: VDD dips below threshold and RESB is asserted.

Figure 13. Reset timing waveforms.

where t_{RES} is time in seconds and CT is capacitance in microfarads. CT is charged with a precision current source of 1μA, a high quality, low leakage capacitor (such as an NPO ceramic) should be used to maintain timing tolerances. The reset circuit stays operational as long as either VGD, VOUT, or VCHG is greater than 2 volts. Fig. 13 illustrates the voltage levels and timings associated with the reset circuit. The figure assumes a regulated VOUT of 3.3V and that RADJ is connected to FB.

Fig. 14. represents typical values for glitch supression accomplished by the RADJ filter. The actual filtering is dependent on both glitch duration and voltage undershoot.

General Purpose Switches

Two general purpose 1.5Ω alarm switches are included to control high current loads. Typical load examples would include a vibrator for a pager, a ring circuit for a cell phone, or an RF transmit amplifier. The N-Channel output switches are enabled with CMOS compatible voltage levels, a high level (1.1V) on the input (IN1, IN2) will turn on the corresponding outputs (OUT1, OUT2) as shown in the block diagram of Fig. 1.

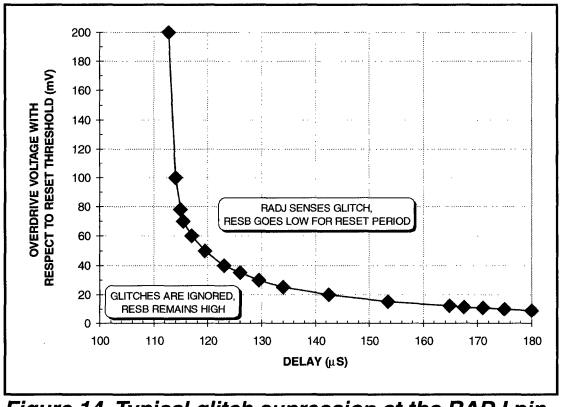


Figure 14. Typical glitch supression at the RADJ pin.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

application INFO available

1V Synchronous Boost Converter

FEATURES

- 1V Input Voltage Operation Startup Guaranteed Under Full Load on Main Output With Operation Down to 0.4V
- Input Voltage Range of 1V to V_{OUT} + 0.5V
- 500mW Output Power at Battery Voltages as Low as 0.8V
- Secondary 9V Supply From a Single Inductor
- Adjustable Output Power Limit Control
- Output Fully Disconnected in Shutdown
- Adaptive Current Mode Control for Optimum Efficiency
- 8µA Shutdown Supply Current

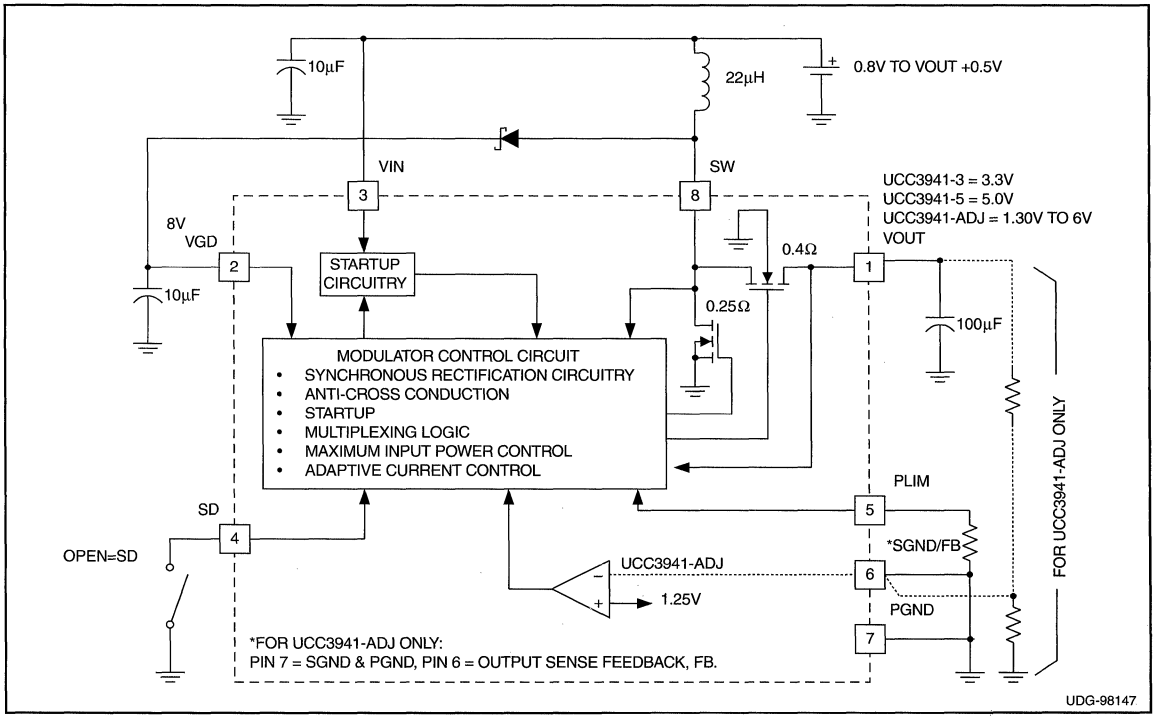
DESCRIPTION

The UCC3941 family of low input voltage single inductor boost converters are optimized to operate from a single or dual alkaline cell, and step up to a 3.3V, 5V, or an adjustable output at 500mW. The UCC3941 family also provides an auxiliary 9V 100mW output, primarily for the gate drive supply, which can be used for applications requiring an auxiliary output such as a 5V supply by linear regulating. The primary output will start up under full load at input voltages typically as low as 0.8V, with a guaranteed maximum of 1V, and will operate down to 0.4V once the converter is operating, maximizing battery utilization.

Demanding applications such as Pagers and PDA's require high efficiency from several milli-watts to several hundred milli-watts, and the UCC3941 family accommodates these applications with >80% typical efficiencies over the wide range of operation. The high efficiency at low output current is achieved by optimizing switching and conduction losses along with low quiescent current. At higher output current the 0.25Ω switch, and 0.4Ω synchronous rectifier, along with continuous mode conduction, provide high efficiency. The wide input voltage range on the UCC3941 family can accommodate other power sources such as NiCd and NiMH.

Other features include maximum power control and shutdown control. Packages available are the 8-pin SOIC (D) and 8-pin DIP (N or J).

SIMPLIFIED BLOCK DIAGRAM AND APPLICATION CIRCUIT



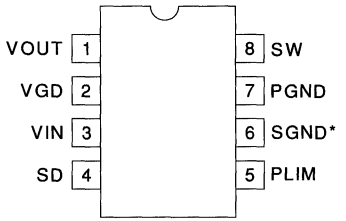
ABSOLUTE MAXIMUM RATINGS

VIN Voltage . . . . . –0.3V to 10V
SD Voltage . . . . . –0.3V to VIN
PLIM Voltage . . . . . –0.3V to 10V
VGD Voltage . . . . . –0.3V to 15V
SW Voltage . . . . . –0.3V to 15V
VOUT Voltage . . . . . –0.3V to 10V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
N or J Package, D Package



Pin 6 is FB for UCC3941-ADJ.

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C, VIN = 1.25V, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VIN Section					
Minimum Startup Voltage	No External VGD Load, T_J = 25°C, I_{OUT} = 100mA (Note 1)		0.8	1	V
Minimum Start Voltage	No External VGD Load, I_{OUT} = 100mA (Note 1)		0.9	1.1	V
Minimum Dropout Voltage	No External VGD Load, I_{OUT} = 100mA (Note 1)			0.5	V
Input Voltage Range		1		VOUT +0.5	V
Quiescent Supply Current	(Note 2)		10	25	µA
Supply Current at Shutdown	SD = Open		8	20	µA
Output Section					
Quiescent Supply Current	(Note 2)		40	80	µA
Supply Current at Shutdown	SD = Open		6	15	µA
Regulation Voltage (UCC3941-3)	1V < VIN < 3V	3.20	3.3	3.39	V
	1V < VIN < 3V, 0mA < I_{OUT} < 150mA (Note 1)	3.17	3.3	3.43	V
Regulation Voltage (UCC3941-5)	1V < VIN < 5V	4.85	5	5.15	V
	1V < VIN < 5V, 0mA < I_{OUT} 100mA (Note 1)	4.8	5	5.2	V
FB Voltage (UCC3941-ADJ)	1V < VIN < 3V	1.212	1.25	1.288	V
VGD Output Section					
Quiescent Supply Current	(Note 2)		30	60	µA
Supply Current at Shutdown	SD = Open		8	20	µA
Regulation Voltage	1V < VIN < 3V, T_A = 25°C	7.5	8.7	9.2	V
	1V < VIN < 3V	7.4	8.7	9.3	V
	1V < VIN < 3V, 0mA < I_{OUT} < 10mA (Note 1)	7.4	8.7	9.3	V
Inductor Charging Section (L = 22µH)					
Peak Discontinuous Current	Over Operating Range		0.5		A
Peak Continuous Current	R_{PLIM} = 6.2Ω	0.5	0.8	1.1	A
Inductor Charging Section					
Charge Switch R_{DSON}	N and D Package, I = 200mA		0.25	0.4	Ω
Current Limit Delay	(Note 1)		50		ns

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C, VIN = 1.25V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Synchronous Rectifier Section					
Rectifier RDS_{ON}	N and D Package, I = 200mA		0.35	0.6	Ω
Shutdown Section					
Shutdown Bias Current			7	10	µA

Note 1: *Performance from application circuit shown in Figures 3 - 5 guaranteed by design and alternate testing methods, but not 100% tested as shown in production.*

Note 2: *For the UCC3941-3, VOUT = 3.47V and VGD = 9.3V. For the UCC3941-5, VOUT = 5.25V, VGD = 9.3V. For the UCC3941-ADJ, FB = 1.315V, VGD = 9.3V.*

PIN DESCRIPTIONS

FB: Feedback control pin used in the UCC3941-ADJ version only. The internal reference for this comparator is 1.25V and external resistors provide the gain to the output voltage.

PGND: Power ground of the IC. The inductor charging current flows through this pin. For the UCC3941-ADJ signal ground and power ground lines are tied to a common pin.

PLIM: This pin is programmed to set the maximum input power for the converter. For example a 1A current limit at 1V would have a 333mA limit at 3V input keeping the input power constant at 1W. The peak current at VIN = 1V is programmed to 1.5A (1.5W) when this pin is grounded. The power limit is given by:

$$PL_{(W)} = \frac{11.8}{R_{PL} + 6.7} + V_{IN}(0.26)$$

where R_{PL} is equal to the external resistor from the PLIM pin to ground. The peak current limit is given by:

$$I_{PK(A)} = \frac{11.8}{V_{IN} \bullet (R_{PL} + 6.7)} + 0.26$$

Constant power gives several advantages over constant current such as lower output ripple.

SD: When this pin is open, the built in 7µA current source pulls up on the pin and programs the IC to go into shutdown mode. When this pin is tied to ground, the IC is enabled and both output voltages will regulate.

SGND: Signal ground of the IC. For the UCC3941-ADJ signal ground and power ground lines are tied to a common pin.

SW: An inductor is connected between this node and VIN. The VGD (Gate Drive Supply) flyback diode is also connected to this pin. When servicing the 3.3V supply, this pin will go low charging the inductor, then shut off, dumping the energy through the synchronous rectifier to the output. When servicing the VGD supply, the internal synchronous rectifier stays off, and the energy is diverted to VGD through the flyback diode. During discontinuous portions of the inductor current a MOSFET resistively connects VIN to SW damping excess circulating energy to eliminate undesired high frequency ringing.

VGD: The VGD pin which is coarsely regulated around 9V and is primarily used for the gate drive supply for the power switches in the IC. This pin can be loaded with up to 10mA as long as it does not present a load at voltages below 2V. This ensures proper startup of the IC. The VGD supply can go as low as 7.5V without interfering with the servicing of the 3.3V output. Below 7.5V, VGD will have the highest priority, although practically the voltage should not decay to that level if the output capacitor is sized properly.

VIN: Input voltage to supply the IC during startup. After the output is running the IC draws power from VOUT or VGD.

VOUT: Main output voltage (3.3V, 5V or adjustable) which has highest priority in the multiplexing scheme, as long as VGD is above the critical level of 7.5V. Loads over 150mA are achievable at 1V input voltage. This output will startup with 1V input at full load.

APPLICATION INFORMATION

A detailed block diagram of the UCC3941 is shown in Figure 1. Unique control circuitry provides high efficiency power conversion for both light and heavy loads by transitioning between discontinuous and continuous conduction based on load conditions. Figure 2 depicts converter waveforms for the application circuit shown in Figure 3. A single 22µH inductor provides the energy pulses required for a highly efficient 3.3V converter at up to 500mW output power.

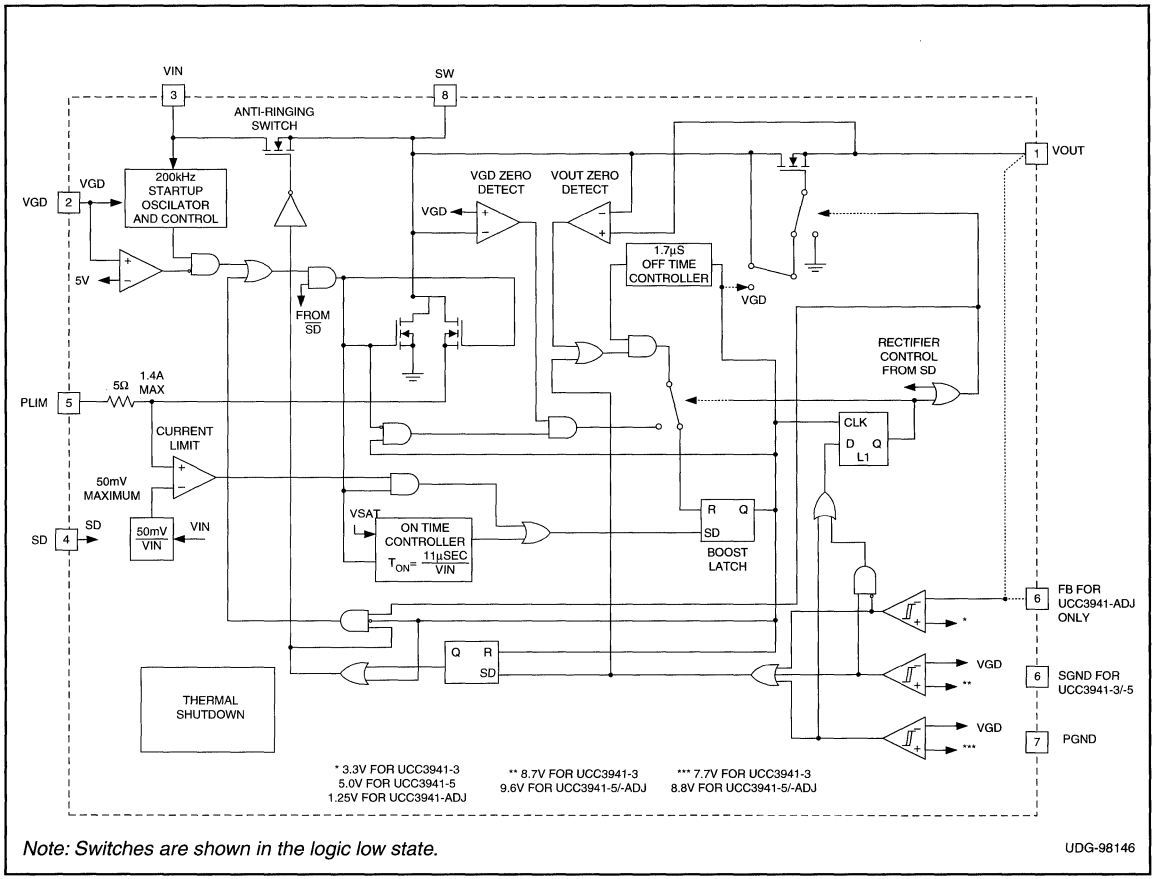


Figure 1. 1V Synchronous boost.

APPLICATION INFORMATION (cont.)

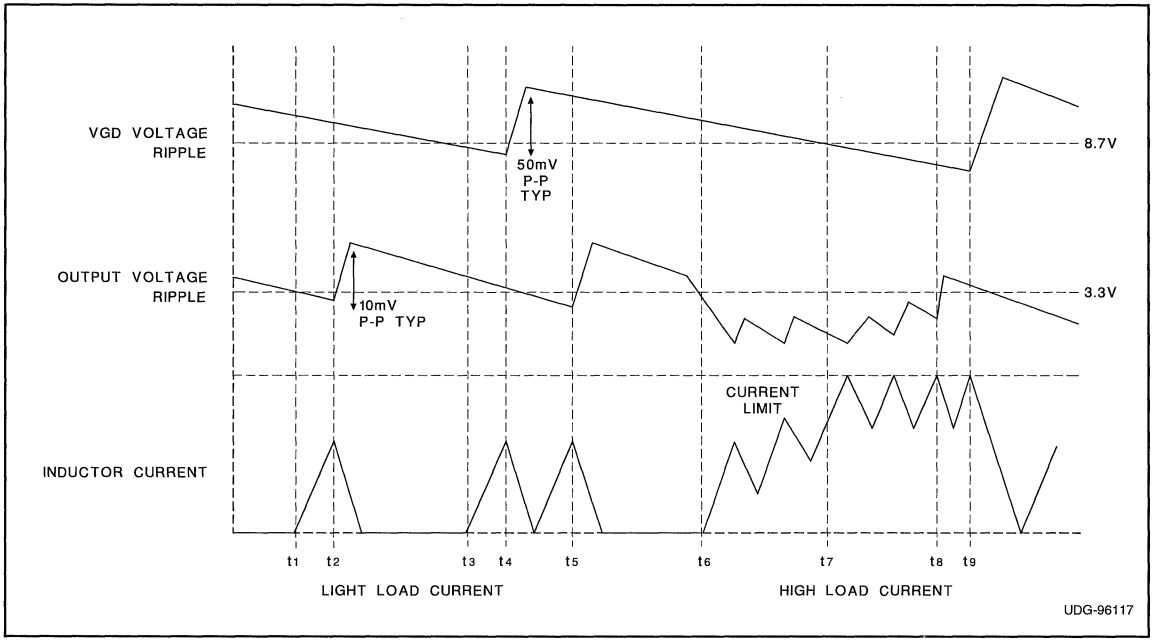


Figure 2. Inductor Current and output ripple waveforms.

At time t_1, the 3.3V output drops below its lower threshold, and the inductor is charged with an on time determined by:

$$T_{ON} = \frac{12\mu\, s}{VIN}$$

For a 1.25V input, and a 22µH inductor, the resulting peak current is approximately 500mA. At time t_2, the inductor begins to discharge with a minimum off time of 1.7µs. Under lightly loaded conditions, the amount of energy delivered in this single pulse would satisfy the voltage control loop, and the converter would not command any more energy pulses until the output again drops below the lower voltage threshold.

At time t_3, the VGD supply has dropped below its lower threshold, but the output voltage is still above its threshold point. This results in an energy pulse to the gate drive supply at t_4. However, while the gate drive is being serviced, the output voltage has dropped below its lower threshold, so the state machine commands an energy pulse to the output as soon as the gate drive pulse is completed.

Time t_6, represents a transition between light and heavy load. A single energy pulse is not sufficient to force the output voltage above its upper threshold before the minimum off time has expired, and a second charge cycle is commanded. Since the inductor current does not reach zero in this case, the peak current is greater than 0.5A at the end of the next charge on time. The result is a ratcheting of inductor current until either the output voltage is satisfied, or the converter reaches its programmed current limit. At time t_7, the gate drive voltage has dropped below its threshold but the converter continues to service the output because it has highest priority, unless VGD drops below 7.5V.

Between t_7 and t_8, the converter reaches its peak current limit which is determined by R_{PL} and VIN. Once the limit is reached, the converter operates in continuous mode with approximately 200mA of ripple current. At time t_8, the output voltage is satisfied, and the converter can service VGD, which occurs at t_9.

APPLICATION INFORMATION (cont.)

Programming the Power Limit

The UCC3941 incorporates an adaptive power limit control which modifies the converter current limit as a function of input voltage. In order to program the function, the user simply determines the output power requirements and makes an initial converter efficiency estimate. The programming resistor is chosen by:

$$R_{PL} = \frac{11.8 \bullet n}{P_{OUT} - V_{BAT}(0.26)} - 6.7$$

Where n is the initial efficiency estimate. For 500mW of output power, and an efficiency estimate of 0.75:

$$R_{PL} = \frac{11.8 \bullet 0.75}{0.5 - 1.25(0.26)} - 6.7 = 43.8\,\Omega$$

For decreasing values of R_{PL}, the power limit increases. Therefore, to insure that the converter can supply 500mW of output power, a power limiting resistor of less than 15Ω must be chosen. For the circuit shown in Figure 3, R_{PL} is chosen as 6.2Ω:

$$P_L = \frac{11.8}{43.8 + 6.7\,\Omega} + 1.25(0.26) = 0.56W$$

This power limiting setting will support 0.5W of output power. It should be noted that the power limit equation contains an approximation which results in slightly less actual input power than the equation predicts. This discrepancy results from the fact that the average current delivered to the load will be less than the peak current set by the power limit function due to current ripple. However, if the ripple component of the current is kept low, the power limit equation can be used as an adequate estimate of input power. Furthermore, since an initial efficiency estimate was required, sufficient margin can be built into this estimate to insure proper converter operation.

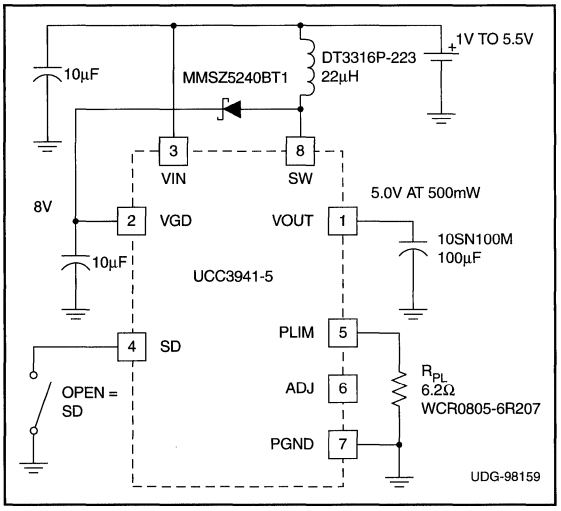


Figure 4. Dual output synchronous boost 5V version.

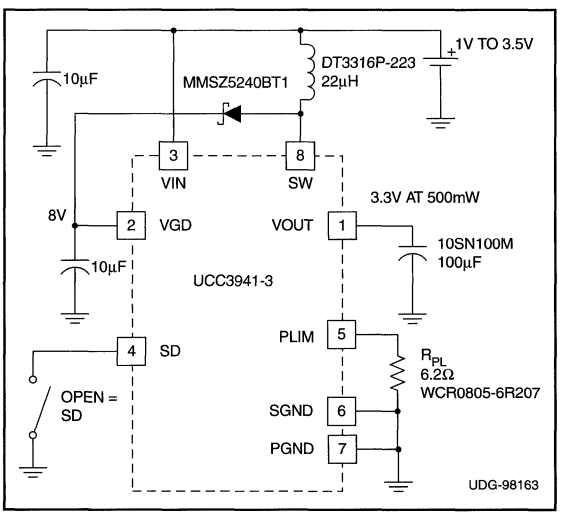


Figure 3. Dual output synchronous boost 3.3V version.

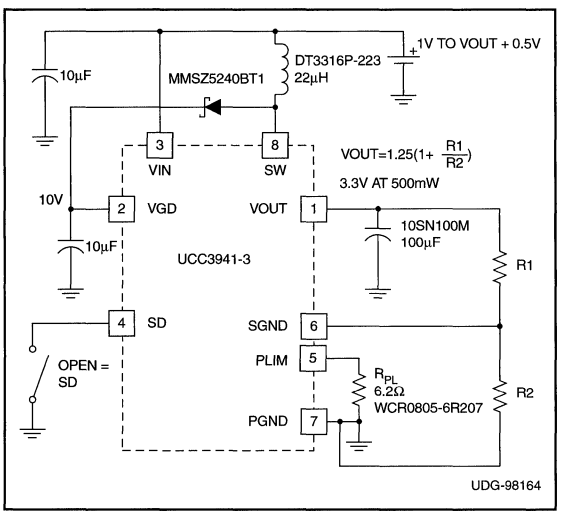


Figure 5. Dual output synchronous boost ADJ

APPLICATION INFORMATION (cont.)

Inductor Section

An inductor value of 22µH will work well in most applications, but values between 10µH and 100µH are also acceptable. Lower value inductors typically offer lower ESR and smaller physical size. Due to the nature of the "bang-bang" controllers, larger inductor values will typically result in larger overall voltage ripple, because once the output voltage level is satisfied the converter goes discontinuous, resulting in the residual energy of inductor causing overshoot.

It is recommended to keep the ESR of the inductor below 0.15Ω for 500mW applications. A Coilcraft DT3316P-223 surface mount inductor is one choice since it has a current rating of 1.5A and an ESR of 84mΩ. Other choices for surface mount inductors are shown in Table 1.

Table 1. Inductor Suppliers

MANUFACTURER	PART NUMBERS
Coilcraft Cary, Illinois Tel: 708-639-2361 Fax: 708-639-1469	DT Series
Coiltronics Boca Raton, Florida Tel: 407-241-7876	CTX Series

Output Capacitor Selection

Once the inductor value is selected the capacitor value will determine the ripple of the converter. The worst case peak to peak ripple of a cycle is determined by two components, one is due to the charge storage characteristic, and the other is the ESR of the capacitor. The worst case ripple occurs when the inductor is operating at maximum current and is expressed as follows:

$$\Delta V = \frac{(I_{CL})^2 \bullet L}{2 \bullet C \bullet (V_O - V_I)} + I_{CL} \bullet C_{ESR} \text{ where}$$

I_{CL} = the peak inductor current $\left(I_{CL} = \frac{Power\ Limit}{V_{IN}}\right)$

ΔV = output ripple
V_O = output voltage
V_I = input voltage
C_{ESR} = ESR of the output capacitor

A Sanyo OS-CON series surface mount capacitor (10SN100M) is one recommendation. This part has an ESR rating of 90mΩ at 100µF. Other potential capacitor sources are shown in Table 2.

Table 2. Capacitor Suppliers

MANUFACTURER	PART NUMBER
Sanyo Video Components San Diego, California Tel: 619-661-6322 Fax: 619-661-1055	OS-CON Series
AVX Sanford, Maine Tel: 207-282-5111 Fax: 207-283-1941	TPS Series
Sprague Concord, New Hampshire Tel: 603-224-1961	695D Series

Input Capacitor Selection

Since the UCC3941 family does not require a large decoupling capacitor on the input voltage to operate properly, a 10µF capacitor is sufficient for most applications. Optimum efficiency will occur when the capacitor value is large enough to decouple the source impedance. This usually occurs for capacitor values in excess of 100µF.

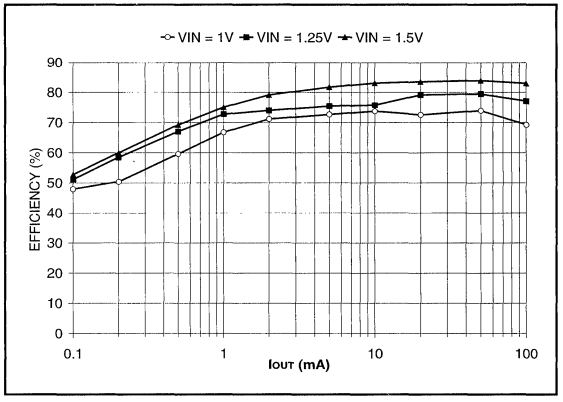


Figure 6. UCC3941 Efficiency vs. I_{OUT}

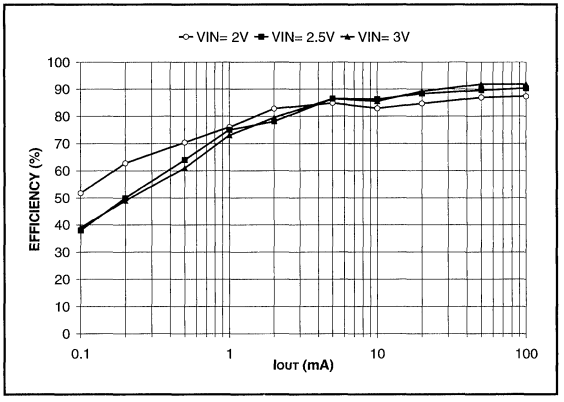
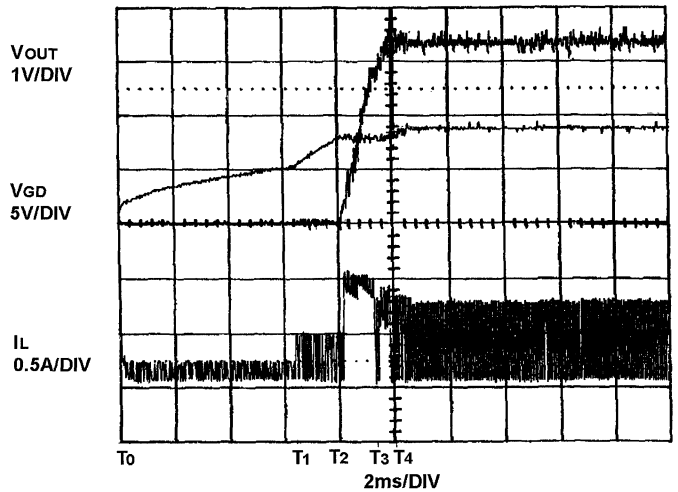


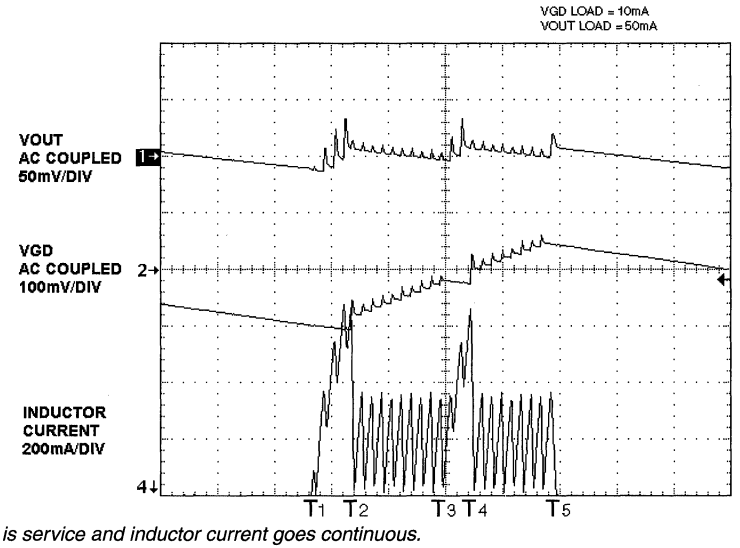
Figure 7. UCC3941 Efficiency vs. I_{OUT}



T_0: 200kHz startup oscillator starts VGD rising.
T_1: VGD gets to a sufficient voltage (5V) to run IC in normal operating mode.
T_2: VGD has reached a sufficient voltage (7.5V) to get VOUT started.
T_3: VOUT is serviced and starting up.
T_4: VOUT has reached a sufficient voltage and VGD is serviced until it reaches = 8.5V.

Figure 8. Startup characteristics.

APPLICATION INFORMATION (cont.)



T_1: *VOUT is service and inductor current goes continuous.*
T_2: *VGD is serviced with discontinuous operation and reaches 1st threshold (7.5V).*
T_3: *VOUT requires servicing so since VGD has at least reached its first threshold of 7.5V the VOUT has priority.*
T_4: *VOUT is satisfied and VGD is serviced until 2nd threshold is reached.*
T_5: *Both outputs are satisfied.*

Figure 9. Dual output example.

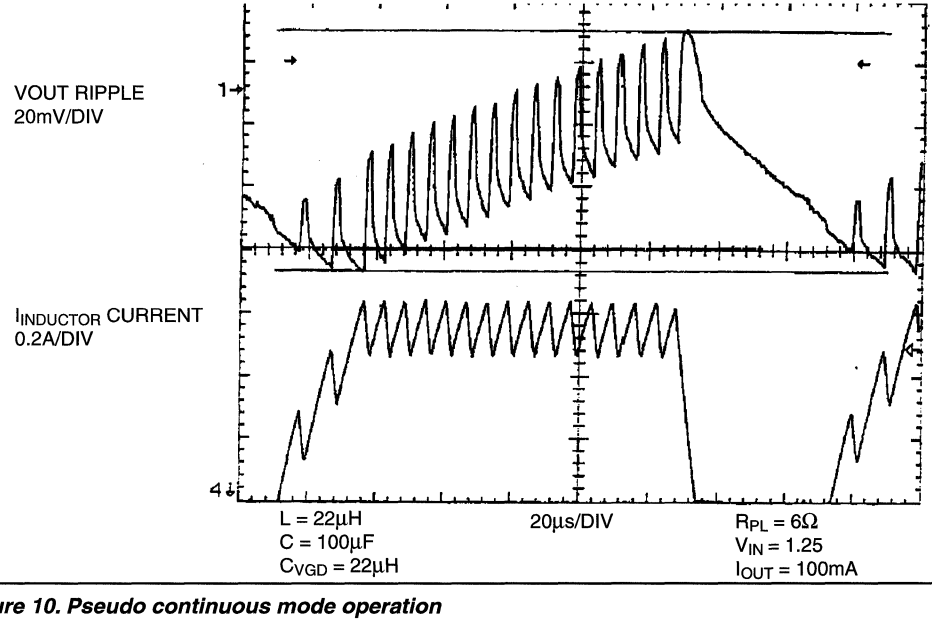


Figure 10. Pseudo continuous mode operation

APPLICATION INFORMATION (cont.)

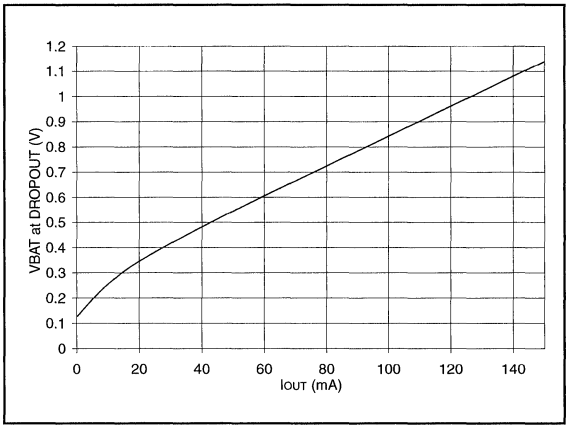


Figure 11. UCC3941-3 Dropout vs. I_{OUT}

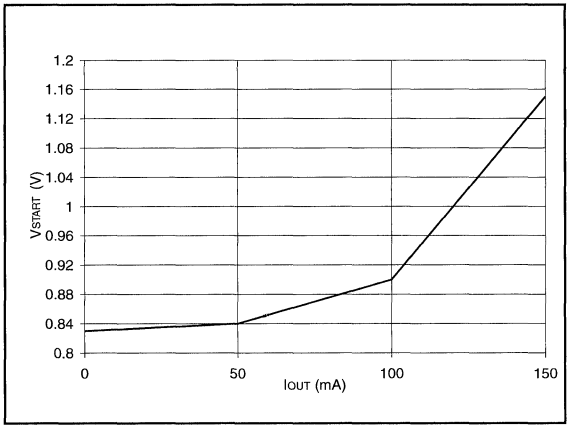


Figure 12. Minimum start voltage vs. I_{OUT}

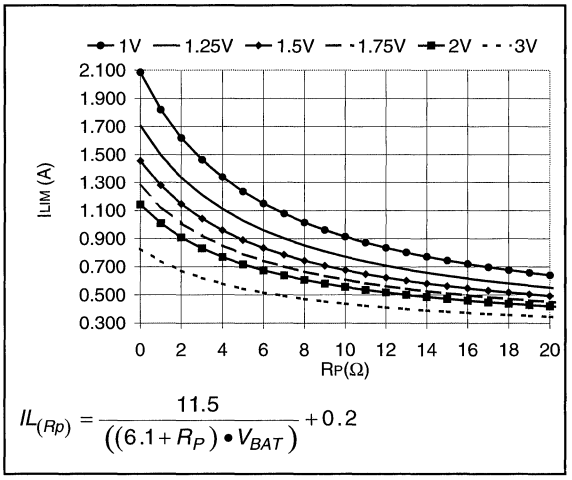


Figure 13. UCC3941-ADJ I_{LIM} vs. R_P (J package only)

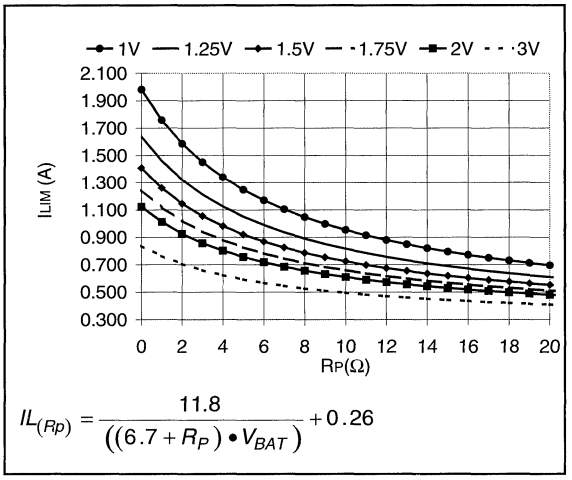


Figure 14. UCC3941-ADJ I_{LIM} vs. R_P (all other packages)

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Low Power Synchronous Boost Converter

FEATURES

- 1V Input Voltage Operation Start-up Guaranteed under FULL Load on Main Output, and Operation Down to 0.5V
- 200mW Output Power at Battery Voltages as low as 0.8V
- Secondary 7V Supply from a Single Inductor
- Output Fully Disconnected in Shutdown
- Adaptive Current Mode Control for Optimum Efficiency
- High Efficiency over Wide Operating Range
- 6µA Shutdown Supply Current
- Output Reset Function with Programmable Reset Period

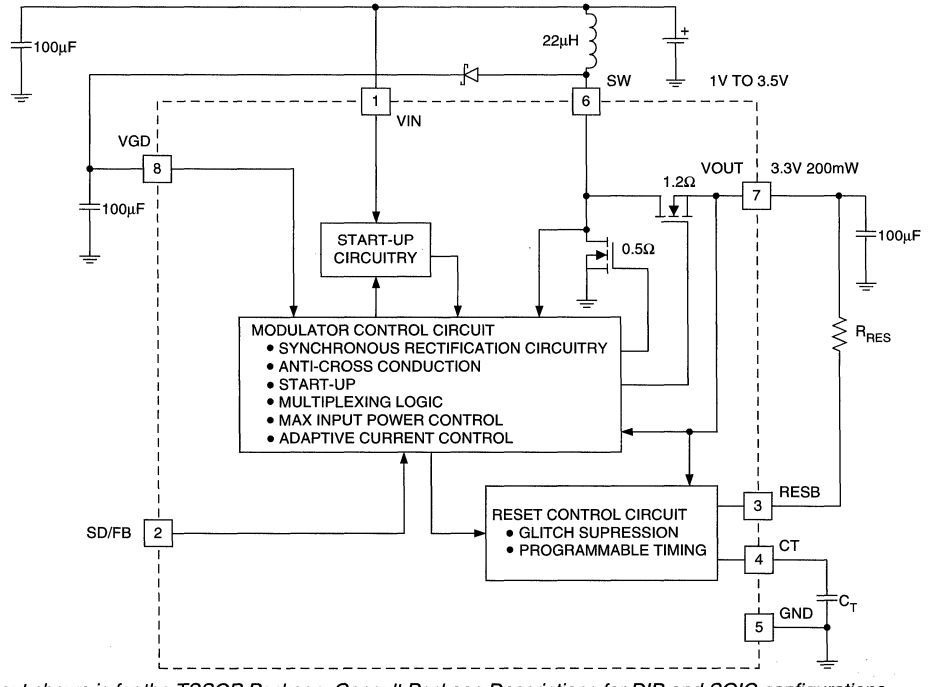
DESCRIPTION

The UCC39411 family of low input voltage, single inductor boost converters is optimized to operate from a single or dual alkaline cell, and steps up to a 3.3V, 5V, or adjustable output at 200mW. The UCC39411 family also provides an auxiliary 7V output, primarily for the gate drive supply, which can be used for applications requiring an auxiliary output, such as 5V, by linear regulating. The primary output will start up under full load at input voltages typically as low as 0.8V with a guaranteed max of 1V, and will operate down to 0.5V once the converter is operating, maximizing battery utilization.

The UCC39411 family is designed to accommodate demanding applications such as pagers and cell phones that require high efficiency over a wide operating range of several milli-watts to a couple of hundred milli-watts. High efficiency at low output current is achieved by optimizing switching and conduction losses with a low total quiescent current (50µA). At higher output current the 0.5Ω switch, and 1.2Ω synchronous rectifier along with continuous mode conduction provide high power efficiency. The wide input voltage range of the UCC39411 family can accommodate other power sources such as NiCd and NimH.

The 39411 family also provides shutdown control. Packages available are the 8 pin SOIC (D), 8 pin DIP (N or J), and 8 pin TSSOP (PW) to optimize board space.

SIMPIFIED BLOCK DIAGRAM AND APPLICATION CIRCUIT (UCC39412)



Note: Pinout shown is for the TSSOP Package. Consult Package Descriptions for DIP and SOIC configurations.

UDG-98067

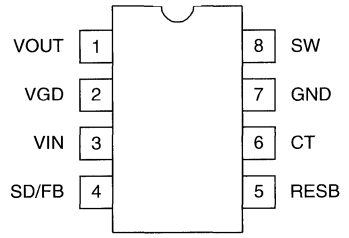
ABSOLUTE MAXIMUM RATINGS

VIN Voltage . . . . . –0.3V to 10V
SD Voltage . . . . . –0.3V to V_{IN}
VGD Voltage . . . . . –0.3V to 14V
SW Voltage . . . . . –0.3V to 15V

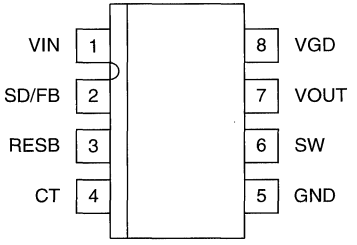
Currents are positive into, negative out of the specific terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-8, SOIC-8 (TOP VIEW)
N or J Package, D Package



TSSOP-8 (TOP VIEW)
PW Package



ELECTRICAL CHARACTERISTICS:

T_J= 0°C to +70°C for the UCC39411/2/3, T_J = –40°C to +85°C for the UCC29411/2/3, T_J = –55C to +125°C for the UCC19411/2/3, V_{IN} = 1.25V for UCC39411/2, V_{IN} = 2.5V for the UCC39413, T_A=T_J.

		UCC39411 UCC39412 UCC39413			UCC19411/2/3 UCC29411/2/3			
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
VIN Section								
Minimum Start-up Voltage	No External VGD Load, T_J=25°C, I_{OUT}=60mA (Note 1)		0.8	1		.08	1	V
	No External VGD Load, I_{OUT}=60mA (Note 1)		0.9	1.1		1.2	1.4	V
Minimum Dropout Voltage	No External VGD Load, I_{OUT}=10mA (Note 1)			0.5			0.7	V
Input Voltage Range		1.1		3.2	1.3		3.2	V
Quiescent Supply Current	(Note 2)		6	12		8	16	µA
Supply Current at Shutdown	SD = GND		6	12		8	16	µA

ELECTRICAL CHARACTERISTICS: T_J= 0°C to +70°C for the UCC39411/2/3, T_J = –40°C to +85°C for the UCC29411/2/3, T_J = –55C to +125°C for the UCC19411/2/3, V_{IN} = 1.25V for UCC39411/2, V_{IN} = 2.5V for the UCC39413, T_A=T_J.

		UCC39411 UCC39412 UCC39413			UCC19411/2/3 UCC29411/2/3			
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Output Section								
Quiescent Supply Current	(Note 2)		15	28		20	37	µA
Supply Current at Shutdown	SD = GND		3	6		5	10	µA
Regulation Voltage (UCC39412)	1V < V_{IN} < 3V	3.2	3.3	3.39	3.15	3.3	3.45	V
	1V < V_{IN} < 3V, 0mA<I_{OUT}<60mA (Note 1)	3.17	3.3	3.43	3.11	3.3	3.5	V
Regulation Voltage (UCC39413)	1V < V_{IN} < 5V	4.85	5	5.15	4.78	5	5.23	V
	1V < V_{IN} < 5V, 0mA<I_{OUT}<60mA (Note 1)	4.8	5	5.2	4.71	5	5.3	V
ADJ Voltage (UCC39411)	1V < V_{IN} < 3V	1.212	1.25	1.288	1.194	1.25	1.306	V
VGD Output Section								
Quiescent Supply Current	(Note 2)		20	40		27	55	µA
Supply Current at Shutdown	SD = GND		20	40		27	55	µA
Regulation Voltage (UCC39411/2)	1V < V_{IN} < 3V	6.3	7	7.7	6.3	7	7.7	V
	1V < V_{IN} < 3V, 0mA<I_{OUT}<10mA (Note 1)	6.3	7	7.7	6.3	7	7.7	V
Regulation Voltage (UCC39413)	1V < V_{IN} < 5V	7.7	8.5	9.3	7.7	8.5	9.3	V
	1V < V_{IN} < 5V, 0mA<I_{OUT}<10mA (Note 1)	7.7	8.5	9.3	7.7	8.5	9.3	V
Inductor Charging Section (L=22µH)								
Peak Discontinuous Current	Operating Range, L=22.1µH	180	250	300	180	250	300	mA
Peak Continuous Current		385	550	715	385	550	715	mA
Charge Switch RDS_{ON}	D Package		0.5	0.75		0.6	0.85	Ω
Current Limit Delay	(Note 1)		50			50		ns
Synchronous Rectifier Section								
Rectifier RDS_{ON}	D Package		1.2	1.8		1.4	2.16	Ω
Shutdown Section								
Threshold		0.4	0.6	0.8	0.2	0.6	0.9	V
Input Bias Current	SD = GND	2	5	15	2	5	15	µA
	SD = 1.25V		5	20		20	100	nA
Reset Section								
Threshold (UCC39411)		1.08	1.125	1.17	1.07	1.125	1.18	V
Threshold (UCC39412)		2.85	2.97	3.09	2.83	2.97	3.11	V
Threshold (UCC39413)		4.32	4.5	4.68	4.3	4.5	4.7	V
Reset Period	C_T = 0.15µF	113	188	263	94	188	282	ms
V_{OUT} to Reset Delay	V_{OUT} Falling at –1mV/µs (Note 1)		60			60		µs
Sink Current		1	20		1	20		mA
Output Low Voltage	I_{OUT} = 500µA			0.1			0.1	V
Output Leakage				0.5			0.5	µA

Note 1 : *Guaranteed by design and alternate test methods. Not 100% tested in production.*
Note 2: *For the UCC39411 FB=1.306V, VGD=7.7V, For the UCC39412 V_{OUT}=3.5V and VGD=7.7V, For the UCC39413 V_{OUT}=5.3V, VGD=9.3V.*

PIN DESCRIPTIONS

VIN: Input Voltage to supply the IC during start-up. After the output is running the IC draws power from VOUT or VGD.

SW: An inductor is connected between this node and VIN. The VGD (Gate Drive Supply) flyback diode is also connected to this pin. When servicing the main output supply this pin will pull low charging the inductor, then shut off dumping the energy through the synchronous rectifier to the output. When servicing the VGD supply the internal synchronous rectifier stays off and the energy is diverted to VGD through the flyback diode. During discontinuous portions of the inductor current, a MOSFET resistively connects VIN to SW damping excess circulating energy to eliminate undesired high frequency ringing.

VGD: The VGD pin which is coarsely regulated around 7V (8.5V for the UCC39413) is primarily used for the gate drive supply for the power switches in the IC. This pin can be loaded with up to 10mA as long as it does not present a load at voltages below 2V (this ensures proper start-up of the IC). The VGD supply can go as low as 6.3V without interfering with the servicing of the main output. Below 6.3V, VGD will have the highest priority.

VOUT: Main output voltage (3.3V, 5V, or adjustable) which has highest priority in the multiplexing scheme, as long as VGD is above the critical level of 6.3V. Startup at full load is achievable at input voltages down to 1V.

CT: This pin provides the timer for determining the reset period. The period is controlled by placing a capacitor to ground of value $C = (0.81e^{-6}) \bullet T$ where T is the desired reset period.

RESB: This pin provides an active low signal to alert the user when the main output voltage falls below 10% of its targeted value. The open drain output can be used to reset a microcontroller which may be powered off of the main output voltage.

SD/FB: For the UCC39411, this pin is used to adjust the output voltage via a resistive divider from VOUT. It also serves as the shutdown pin for all three versions. Pulling this pin low provides a shutdown signal to the IC.

GND: Ground of the IC.

APPLICATION INFORMATION

Operation

A detailed block diagram of the UCC39411 is shown in Figure 1. Unique control circuitry provides high efficiency power conversion for both light and heavy loads by transitioning between discontinuous and continuous conduction based on load conditions. Figure 2 depicts converter waveforms for the application circuit shown in Figure 3. A single 22µH inductor provides the energy pulses required for a highly efficient 3.3V converter at up to 200mW output power

At time t1 the 3.3V output voltage has dropped below its lower threshold, and the inductor is charged with an on time determined by: T_{ON} = 5.5µs/VIN. For a 1.25V input and a 22µH inductor, the resulting peak current is approximately 250mA. At time t2, the inductor begins to discharge with a minimum off time of approximately 1µs. Under lightly loaded conditions, the amount of energy delivered in this single pulse would satisfy the voltage control loop, and the converter would not command any more energy pulses until the output again drops below the lower voltage threshold

At time t3 the VGD supply drops below its lower threshold, but the output voltage is still above its threshold point. This results in an energy pulse to the gate drive supply at t4. In some cases, a single pulse supplied to VGD is insufficient to raise the VGD voltage level enough to satisfy the voltage loop. Under this condition, multiple pulses will be supplied to VGD. Note: when the UCC39411/2/3 is servicing VGD only, the IC will maintain a discontinuous mode of operation. After time t4, the 3.3V output drops below its threshold and requests to be serviced once the VGD cycle has completed, which occurs at time t5.

Time t6 represents a transition between light load and heavy load. A single energy pulse is not sufficient to force the output voltage above its upper threshold before the minimum off time has expired and a second charge cycle is commanded. Since the inductor current does not reach zero in this case, the peak current is greater than 250mA at the end of the next charge on time. The result is a ratcheting of inductor current until either the output voltage is satisfied, or the converter reaches its set current limit. At time t7, the gate drive voltage has dropped below its 7V threshold but the converter continues to service the output because it has higher priority unless VGD drops below ≈ 6.3V

Between time t7 and t8, the converter reaches its peak current limit.

Once the peak current is reached, the converter operates in continuous mode with approximately 60mA of inductor

APPLICATION INFORMATION (continued)

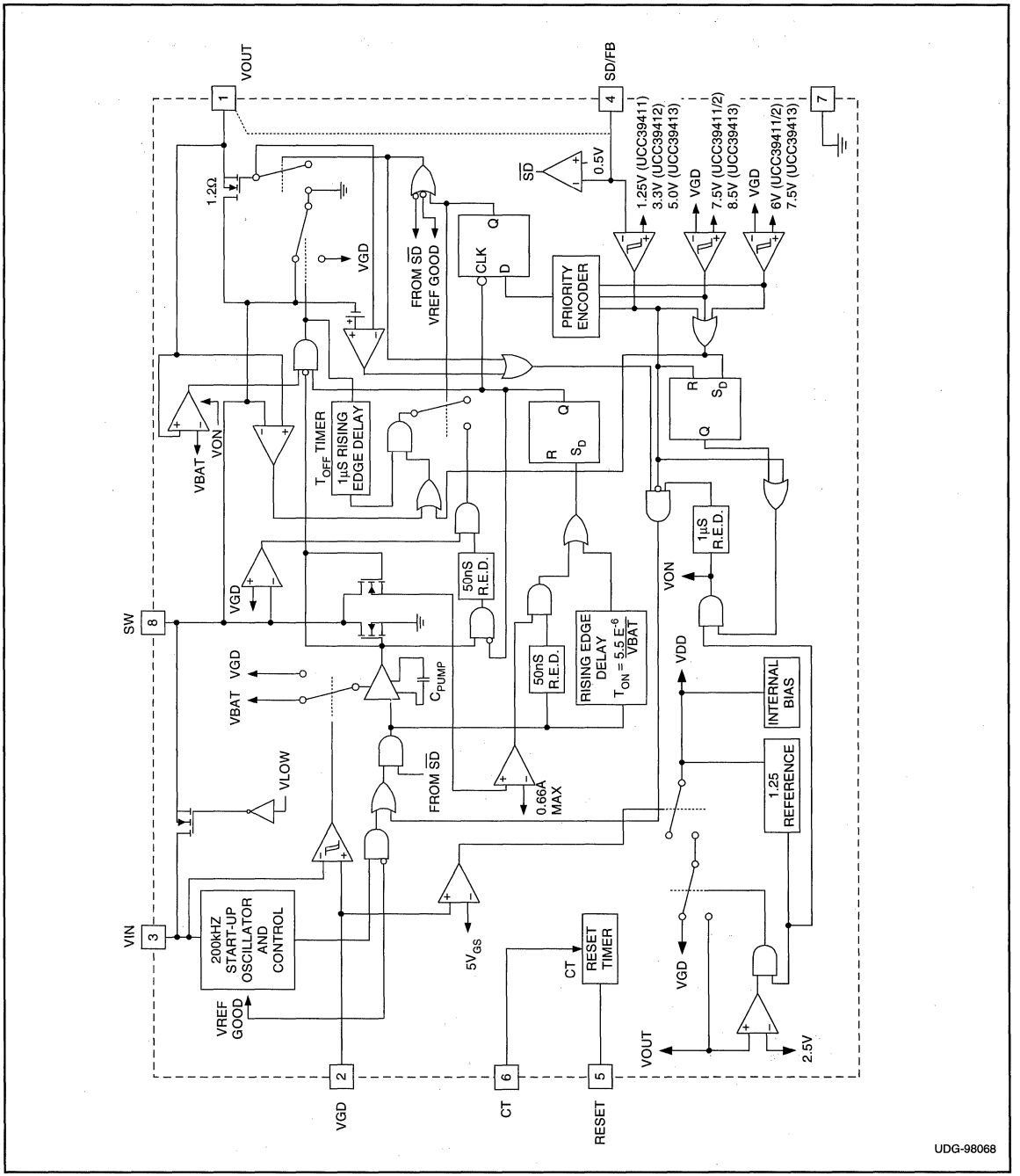


Figure 1. Low power synchronous boost.

Notes: *Switches are shown in the low state.*
Pinout as shown is for the 8 pin D, N or J. See Package Descriptions for 8 pin SOIC.

APPLICATION INFORMATION (continued)

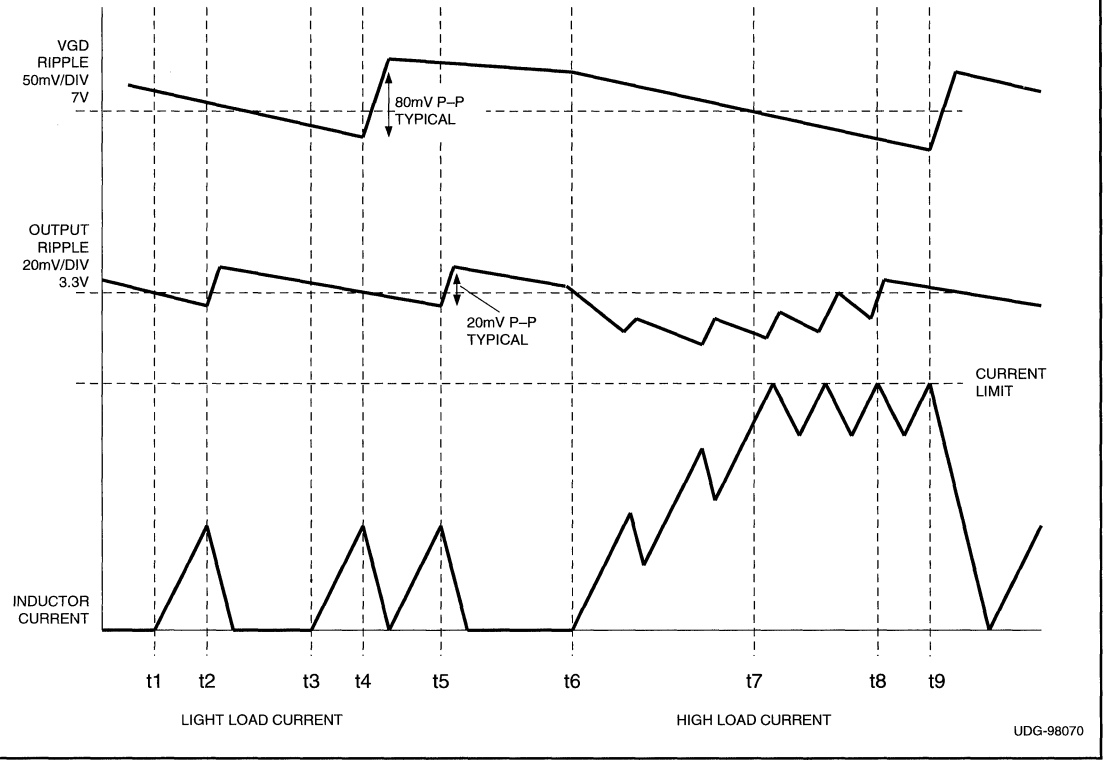
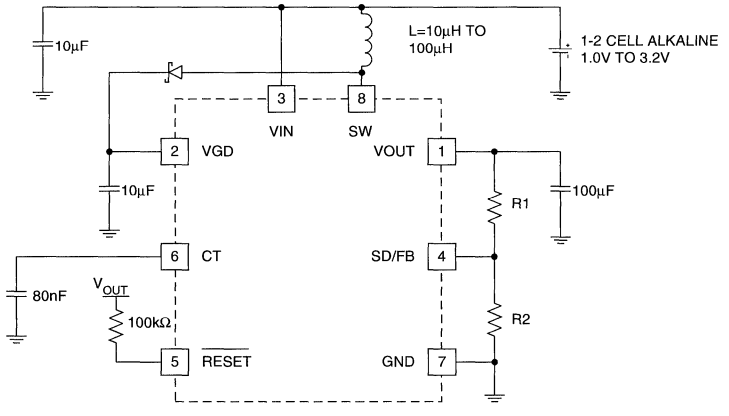


Figure 2. Inductor current and output ripple waveforms.



Note: *Shown pinout is for the TSSOP package. See Package Descriptions for DIP and SOIC pinouts.*

UDG-98069

Figure 3. Low power synchronous boost converter ADJ version –200mW.

APPLICATION INFORMATION (continued)

current ripple. At time t8, the 3.3V output is satisfied and the converter can service the gate drive voltage, VGD, which occurs at time t9

Shutdown Control

Shutdown of the UCC39411/2/3 is controlled via interface with the SD/FB pin. Pulling the SD/FB pin low, for all versions, causes the IC to go into shutdown. In the UCC39412/3, the SD/FB pin is used solely as a shutdown function. Therefore, the SD/FB pin for the UCC39412 and UCC39413 can be directly controlled using conventional CMOS or TTL technology. For the UCC39411, interface into the SD/FB is slightly more complicated due to the added feedback function. When feeding back the output voltage to the SD/FB pin on the UCC39411, the IC requires a thevenin impedance of at least 200kΩ (500kΩ for industrial/military applications) to ground. Then, to accomplish shutdown of the IC, an open drain device may be used.

Component Selection Inductor Selection

An inductor value of 22µH will work well in most applications, but values between 10µH to 100µH are also acceptable. Lower value inductors typically offer lower ESR and smaller physical size. Due to the nature of the "bang-bang" controllers, larger inductor values will typically result in larger overall voltage ripple, because once the output voltage level is satisfied the converter goes discontinuous, resulting in the residual energy of the inductor causing overshoot.

It is recommended to keep the ESR of the inductor below 0.15Ω for 200mW applications. A Coilcraft DT3316P-223 surface mount inductor is one choice since it has a current rating of 1.5A and an ESR of 84mΩ.

Other choices for surface mount inductors are shown in Table 1.

MANUFACTURER	PART NUMBERS
Coilcraft Cary, Illinois Tel: 708-639-2361 Fax: 708-639-1469	DT Series
Coiltronics Boca Raton, Florida Tel: 407-241-7876	CTX Series

Table 1. Inductor Suppliers

Output Capacitor Selection

Once the inductor value is selected the capacitor value will determine the ripple of the converter. The worst case peak to peak ripple of a cycle is determined by two components, one is due to the charge storage characteristic, and the other is the ESR of the capacitor. The worst case ripple occurs when the inductor is operating at max current and is expressed as follows:

$$\Delta V = \frac{(I_{CL})^2 L}{2C(V_O - V_I)} + I_{CL} C_{ESR}$$

- I_{CL} = the peak inductor current = 550mA
- ΔV= Output ripple
- V_O= Output Voltage
- V_I= Input Voltage
- C_{ESR}= ESR of the output capacitor.

A Sanyo OS-CON series surface mount capacitor (10SN100M) is one recommendation. This part has an ESR rating of 90mΩ at 100µF .

Other potential capacitor sources are shown in Table 2.

MANUFACTURER	PART NUMBER
Sanyo Video Components San Diego, California Tel: 619-661-6322 Fax: 619-661-1055	OS-CON Series
AVX Sanford, Maine Tel: 207-282-5111 Fax: 207-283-1941	TPS Series
Sprague Concord, New Hampshire Tel: 603-224-1961	695D Series

Table 2. Capacitor Suppliers

Input Capacitor Selection

Since the UCC39411 family does not require a large decoupling capacitor on the input voltage to operate properly, a 10µF cap is sufficient for most applications. Optimum efficiency will occur when the capacitor value is large enough to decouple the source impedance, this usually occurs for capacitor values in excess of 100µF.

TYPICAL CHARACTERISTICS

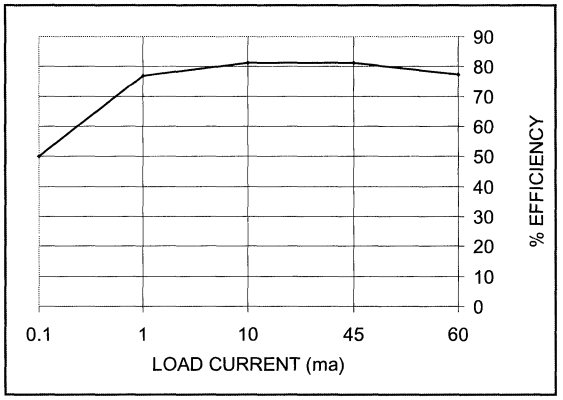


Figure 4. Percent Efficiency at V_{IN} = 1.0, V_{OUT} = 3.3V

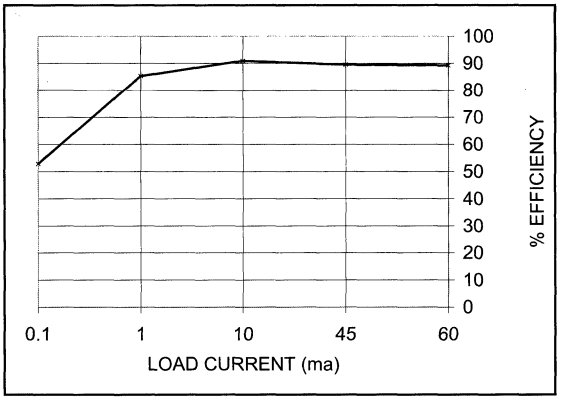


Figure 6. Percent Efficiency at V_{IN} = 2.5, V_{OUT} = 3.3V

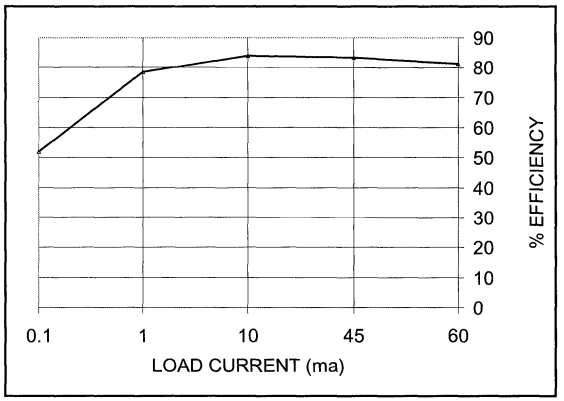


Figure 5. Percent Efficiency at V_{IN} = 1.25, V_{OUT} = 3.3V

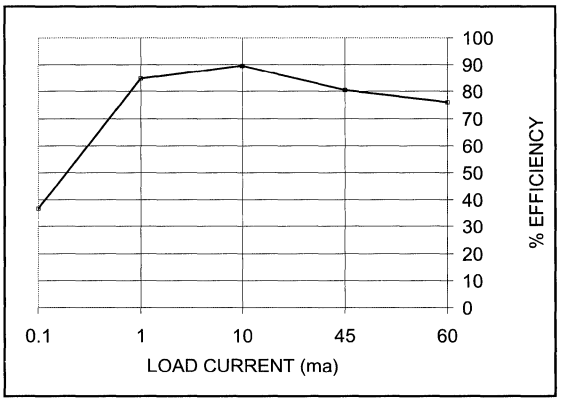


Figure 7. Percent Efficiency at V_{IN} = 3.3, V_{OUT} = 3.3V

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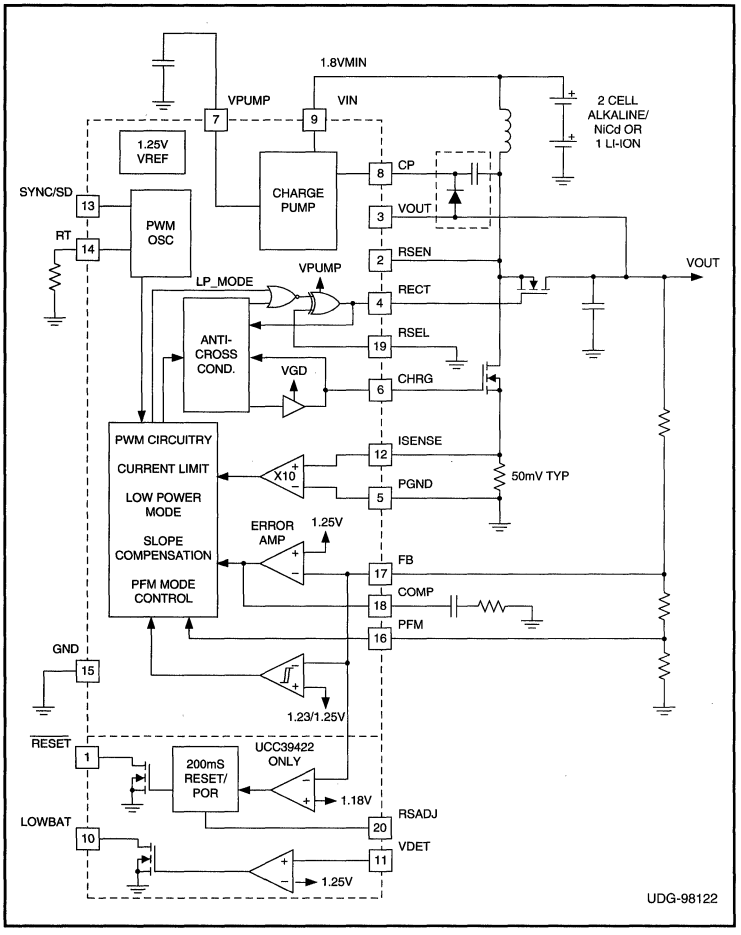
Multimode High Frequency PWM Controller

PRELIMINARY

FEATURES

- Operation Down to an Input Voltage of 1.8V
- High Efficiency Boost or Flyback (Buck-Boost) Topologies
- Drives External FETs for High Current Applications
- Up to 2MHz Oscillator
- Synchronizable Fixed Frequency Operation
- High Efficiency Low Power Mode
- High Efficiency at Very Low Power with Programmable Variable Frequency Mode
- Pulse by Pulse Current Limit
- 5µA Supply Current in Shutdown
- 150µA Supply Current in Sleep Mode
- Selectable NMOS or PMOS Rectification
- Built-in Power on Reset (UCC39422 Only)
- Built-in Low Voltage Detect (UCC39422 Only)

SIMPLIFIED BLOCK DIAGRAM AND APPLICATION CIRCUIT



DESCRIPTION

The UCC39421 family of synchronous PWM controllers is optimized to operate from dual Alkaline/NiCd cells or a single Lithium-Ion (Li-Ion) cell, and convert to adjustable output voltages from 2.5V to 8V. For applications where the input voltage does not exceed the output, a standard boost configuration is utilized. For other applications where the input voltage can swing above and below the output, a 1:1 coupled-inductor (Flyback or SEPIC) is used in place of the single inductor. Fixed frequency operation can be programmed, or synchronized to an external clock source. In applications where at light loads variable frequency mode is acceptable, the IC can be programmed to automatically enter PFM (Pulse Frequency Modulation) mode for an additional efficiency benefit.

Synchronous rectification provides excellent efficiency at high power levels, where N or P type MOSFETs can be used. At lower power levels (10-20% of full load) where fixed frequency operation is required, Low Power Mode is entered. This mode optimizes efficiency by cutting back on the gate drive of the charging FET. At very low power levels, the IC enters a variable frequency mode (PFM). PFM can be disabled by the user.

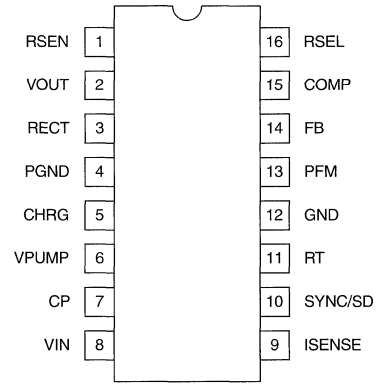
Other features include pulse by pulse current limiting, and a low 5µA quiescent current during shutdown. The UCC39422 incorporates programmable Power on Reset circuitry and an uncommitted comparator for low voltage detection. The available packages are 20 pin TSSOP, or 20 pin N for the UCC39422, and 16 pin TSSOP, or 16 pin N for the UCC39421.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VIN, VOUT,VPUMP) 8V
CP 8V
RSEN . . . . . –0.3 to 12V
SYNC/SD . . . . . –0.3 to 5V
ISENSE . . . . . –0.3 to 1V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

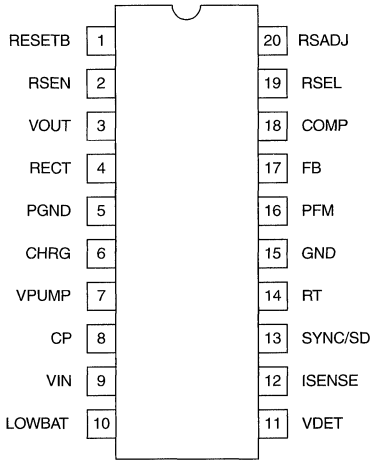
All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

TSSOP-16, DIL-16 (TOP VIEW)
N, PW Packages



CONNECTION DIAGRAMS

TSSOP-20, DIL-20 (TOP VIEW)
N, PW Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –40°C to +85°C for UCC29421/2, 0°C to +70°C for UCC39421/2; R_T=100K, V_{VPUMP}=6V, V_{VIN}=3V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VIN Section					
Minimum Start-up Voltage			1.5	1.8	V
Operating Current	Not in PFM Mode, No Load		35	60	µA
Sleep Mode Current	PFM Mode, No Load		35	60	µA
Shutdown Supply Current	SYNC/SD = High		1.5	4	µA
Startup Frequency	V_{IN} = 1.8V	60	120	190	kHz
Startup Off Time	V_{IN} = 1.8V		2	5	µs
Startup CS Threshold	V_{IN} = 1.8V		36	56	mV
Minimum PUMP or VOUT Voltage to Exit Startup		2.2	2.5	2.8	V
VPUMP Section					
Regulation Voltage	V_{VOUT}=3.3V	5.5		6.6	V
Operating Current	Outputs OFF		100		µA
Sleep Mode Current			5		µA
Shutdown Supply Current	SYNC/SD = High, V_{OUT} = 3V, V_{VPUMP} = 3V		1		µA
CP Voltage to Turn On Pump Switch	V_{VPUMP} = 5V		5.3	5.5	V
Pump Switch RDS_{ON}			4		Ω

ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –40°C to +85°C for UCC29421/2, 0°C to +70°C for UCC39421/2; R_T=100K, V_{VPUMP}=6V, V_{VIN}=3V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VOUT Section					
Operating Current			500	650	µA
Sleep Mode Current		50	100	150	µA
Shutdown Supply Current	SYNC/SD = High		1	2.2	µA
V_{PUMP} to V_{OUT} Threshold to Enable N-Channel Rectifier	V_{OUT} = 3.3V	1.4	1.7	2.0	V
Error Amp Section					
Regulation Voltage	2V < VIN < 5V	1.22	1.25	1.28	V
FB Input Current	V_{FB} = 1.25V		100	350	nA
Max Sinking Current, I_{OL}	V_{COMP} = 1V, V_{FB} = Regulation Voltage +50mV		50	100	µA
Max Sourcing Current, I_{OH}	V_{COMP} = 0V, V_{FB} = Regulation Voltage –50mV	–100	–60		µA
Transconductance	V_{FB} = Regulation Voltage 4mV		270		µS
Unity Gain Bandwidth	C_C = 330pF		100		kHz
Max Output Voltage	V_{FB} = 0V		1.9	2.3	V
Oscillator Section					
Frequency Stability	R_T = 350k	110	150	190	kHz
	R_T = 100k	375	475	575	kHz
	R_T = 35k	0.9	1.2	1.4	MHz
RT Voltage			0.625		V
SYNC Threshold		0.9	1.2	1.6	V
SYNC Input Current	SYNC/SD = 2.5V			100	nA
Max SYNC High Time	To Avoid Shutdown	11	20	29	µs
SYNC Range	R_T = 100k	1.1 o		1.5 o	kHz
Current Sense Section					
Gain		8	10	12	V/V
Overcurrent Limit Threshold			150	200	mV
Unity Gain Bandwidth			25		MHz
COMP Voltage to I_{SENSE} Accuracy	I_{SENSE} = 70mV	0.8	1.0	1.2	V
PWM Section					
Maximum Duty Cycle	V_{ISENSE} = 0V, VFB = 0V	80	88		%
Minimum Duty Cycle	V_{FB} = 1.5V			0	%
Low Power Mode V_{COMP} Threshold	At COMP pin	0.42	0.5	0.58	V
Slope Compensation Accuracy	R_T = 350k, R_{SLOPE} = 20k		2.8		A/s
Zero Current Threshold	(RECT_SEN_ = VIN & GND)	–20	0	20	mV
RSEL Threshold		0.5	0.9	1.3	V
PFM Section					
PFM Disable Threshold		0.17	0.22	0.27	V
Comp Hold During Sleep	V_{PFM} = 0.4		0.45		V
Startup Delay After Sleep	V_{FB} < 1.23V		4	8	µs
FB Voltage to Sleep Off		1.19	1.22	1.25	V
FB Voltage to Sleep On		1.22	1.25	1.29	V
Low Power Mode Timer After Sleep			250	450	µs

ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –40°C to +85°C for UCC29421/2, 0°C to +70°C for UCC39421/2; R_T=100K, V_{VPUMP}=6V, V_{VIN}=3V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VGSW Drive Section					
Rise Time	C_O = 1nF		18	35	ns
Fall Time	C_O = 1nF		14	30	ns
Output High	I_{OUT} = –100mA, Respect to VPUMP		0.4	0.65	V
	I_{OUT} = –1mA, Respect to VPUMP		4	10	mV
Output Low	I_{OUT} = 100mA		0.2	0.35	V
	I_{OUT} = 1mA		2	6	mV
Charge Off to Rectifier On Delay		10	30	50	ns
RECT Drive Section					
Rise Time	C_O = 1nF		18	35	ns
Fall Time	C_O = 1nF		14	30	ns
Output High	I_{OUT} = –100mA, Respect to VPUMP		0.2	0.5	V
	I_{OUT} = –1mA, Respect to VPUMP		5	10	mV
Output Low Rectifier	I_{OUT} = 100mA		0.2	0.35	V
	I_{OUT} = 1mA		2	6	mV
Rectifier Off to Charge On Delay		10	20	50	ns
RESET Section (UCC39422 Only)					
Reset Timeout	C_{RSADJ} = 0.33µF	100	250	400	ms
Reset Threshold	% Below Regulation Voltage	–7	–5.5	–4	%
Output Low Voltage	Reset Condition, I = 5mA		0.1	0.35	V
Output Leakage	RESET = 8V		0.05	0.15	µA
Voltage Detection Section (UCC39422 Only)					
Threshold Voltage		1.18	1.26	1.34	V
Output Low Voltage	I = 5mA		0.15	0.5	V
Output Leakage	LOWBAT = 8V		0.05	0.15	µA

PIN DESCRIPTIONS

COMP: This is the output of the transconductance error amplifier. Connect the compensation components from this pin to ground.

CHRG: This is the gate drive output for the N-channel charge MOSFET. Connect it to the gate directly, or through a low value gate resistor.

CP: This is the input for the charge pump. For applications requiring a charge pump, connect this pin to the charge pump diode and flying capacitor, as shown in the applications diagram of Fig 5. For applications where no charge pump is required, this pin should be grounded.

FB: The feedback input is the inverting input to the tran sconductance error amplifier. Connect this pin to a resistive divider between V_{OUT} and ground. The output voltage will be regulated to:

$$V_{OUT} = 1.25 \bullet \frac{R1}{(R1 + R2)}$$

where R1 goes to GND and R2 goes to VOUT.

GND: This is the signal ground pin for the device. It should be tied to the local ground plane.

ISENSE: This is the input to the X10 wide bandwidth current sense amplifier. Connect this pin to the high side of the current sense resistor. An internal current is sourced out this pin for slope compensation. For applications requiring slope compensation (or filtering of the current sense signal), use a resistor in series with this pin.

LOWBAT: This is the open drain output of the uncommitted comparator. (UCC39422 only). This output is low when the VDET pin is above 1.25V.

PIN DESCRIPTIONS (cont.)

PFM: This is the programming pin for the PFM (Pulse Frequency Modulation) Mode threshold. Connect this pin to a resistive divider off of the FB pin (or VOUT) to set the PFM threshold. To disable PFM Mode, connect this pin to ground (below 0.2V).

PGND: This is the power ground pin for the device. Connect it directly to the ground return of the current sense resistor.

RECT: This is the gate drive output for the synchronous rectifier. Connect it to the gate of the P or N channel MOSFET directly, or through a low value gate resistor.

RECTSEN: This pin is used to sense the voltage across the synchronous rectifier for commutation. In boost configurations, connect this pin through a 1K resistor to the junction of the two MOSFETs and the inductor. In flyback and SEPIC configurations, connect this pin through a 1K resistor to the junction of the drain of the synchronous rectifier and the secondary side winding of the coupled inductor.

RSADJ: A capacitor from this pin to ground sets the reset delay. (UCC39422 only)

RSEL: This pin programs the device for N channel or P channel synchronous rectifiers by inverting the phase of the RECT gate drive output. Connect this pin to ground for N-channel MOSFETs, connect it to V_{IN} for P-channel MOSFETs.

$\overline{\text{RESET}}$: This is the open drain output of the Reset comparator. (UCC39422 only) and is active low.

RT: A resistor from this pin to ground programs the frequency of the pulse width modulator.

SYNC/SD: This dual function pin is the SYNC and Shutdown input. To synchronize the internal clock to an external source, this pin must be driven above 2.0V. The clock syncs to the rising edge of the input. To shutdown the converter, this pin must be held high (above 2.0V) for a minimum of 20μsec. If not used, this pin should be grounded.

VPUMP: This is the output of the charge pump. For applications requiring a charge pump, connect a 1μF capacitor from this pin to ground. Otherwise, connect this pin to the higher of V_{IN} or V_{OUT}, and decouple with a 0.1μF capacitor.

VOUT: Connect this pin to the output voltage. This input is used for sensing the voltage across the synchronous rectifier and for bootstrapping the gate drive to the charge FET and should be decoupled with a 0.1μF capacitor.

VIN: This is the input power pin of the device. Connect this pin to the input voltage source. A 0.1μF decoupling capacitor should be connected between this pin and ground.

VDET: This is the non-inverting input to an uncommitted comparator. This input may be used for detecting a low battery condition. (UCC39422 only)

APPLICATION INFORMATION

The UCC39421 is a high frequency, synchronous PWM controller optimized for portable, battery powered applications where size and efficiency are of critical importance. It includes high speed, high current FET drivers for those converter applications requiring low RDS_{ON} external MOSFETs. A detailed block diagram is shown in Fig 1.

Optimizing Efficiency

The UCC39421 optimizes efficiency, extending battery life, by its low quiescent current and its synchronous rectifier topology. The additional features of Low Power Mode and PFM Mode maintain high efficiency over a wide range of load current. These features will be discussed in detail.

Power Saving Modes

Since this is a peak current mode controller, the error amplifier output voltage sets the peak inductor current required to sustain the load. The UCC39421 incorporates two special modes of operation designed to optimize efficiency over a wide range of load current. This is done by comparing the error amplifier output voltage (on the COMP pin) to two fixed thresholds (one of which is user programmable). If the error amplifier output voltage drops below the first threshold, Low Power (LP) mode will be entered. If the error amplifier output voltage drops even further, below a second user programmable threshold, PFM Mode will be entered. These modes of operation are designed to maintain high efficiency at light load, and are described in detail below. Refer to the simplified block diagram of Fig. 2 for the control logic.

APPLICATION INFORMATION (cont.)

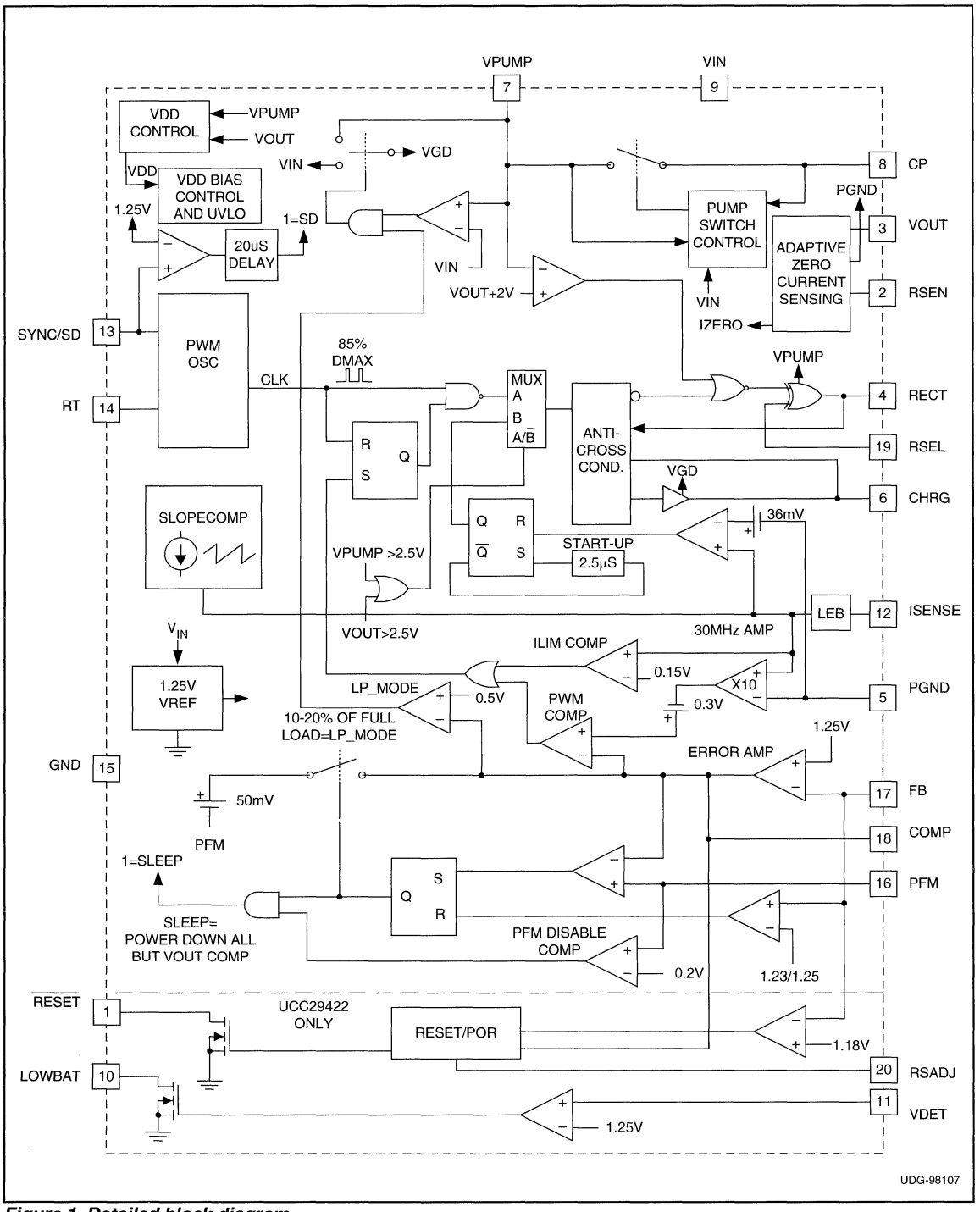


Figure 1. Detailed block diagram.

APPLICATION INFORMATION (cont.)

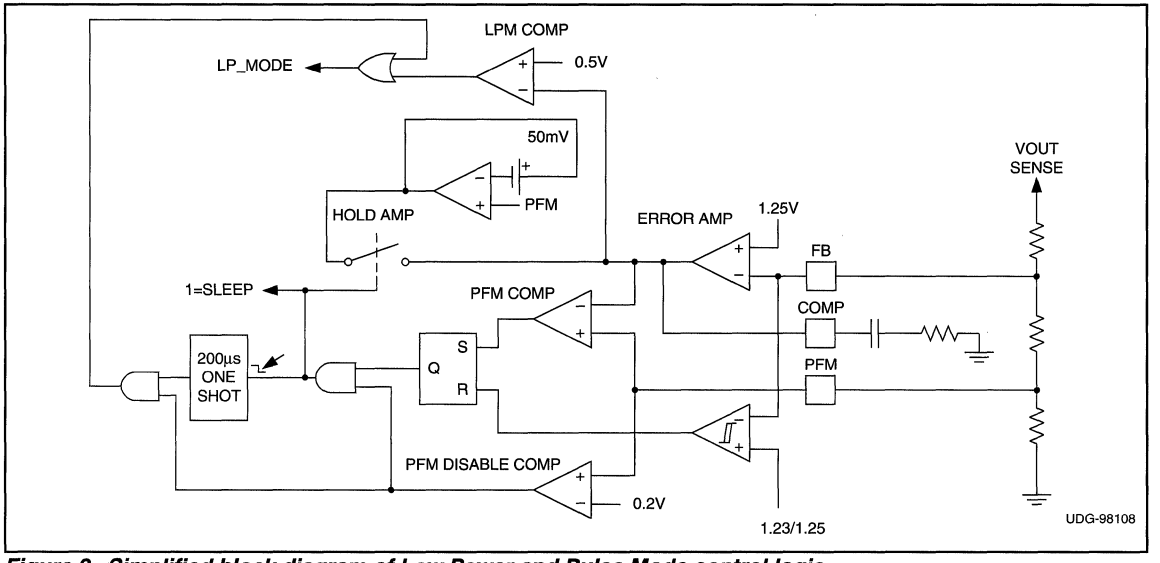


Figure 2. Simplified block diagram of Low Power and Pulse Mode control logic.

Low Power Mode

During normal operation, at medium to high load currents, the switching frequency remains fixed, programmed by the resistor on the RT pin. At these higher loads, the gate drive output on the CHRG pin (for the N channel charge FET) will be the higher of V_{IN} or V_{PUMP}. When the load current drops (sensed by a drop in the error amp voltage), the UCC39421 will automatically enter LP mode, and the gate drive voltage on the CHRG pin will be reduced to lower gate drive losses. This helps to maintain high efficiency at light loads where the gate drive losses begin to dominate and the lowest possible Rdson is not required. If the load increases, normal or "High Power" mode will resume. The expression for gate drive power loss is given by equation 1. It can be seen that the power varies as a function of the applied gate voltage squared.

$$P_{GATELOSS} = \frac{Q_G \bullet V_G^2 \bullet f}{V_S} \quad (1)$$

Where Q_g is the total gate charge and V_s is the gate voltage specified in the MOSFET manufacturer's data sheet, V_g is the applied gate drive voltage, and f is the switching frequency.

The nominal COMP voltage where LP mode will be entered is 0.5V. Given the internal offset and gain of the current sense amplifier, this corresponds to a peak switch current of:

$$I_{PEAK} = \frac{(0.5-0.3)}{K \bullet R_{SENSE}} = \frac{0.02}{R_{SENSE}} \quad (2)$$

Where 0.5V is the threshold for LP mode, 0.3V is the internal offset and K is the nominal current sense amplifier gain of 10 and R_{SENSE} is the value of the current sense resistor. If the peak inductor current is below this value, the UCC39421 will enter LP mode and the gate drive voltage on the CHRG pin will be equal to V_{in}. At peak currents higher than this, the gate drive voltage will be the higher of V_{IN} or VPUMP.

PFM Mode

At very light loads, the UCC39421 will enter PFM Mode. In this mode, when the error amplifier output voltage drops below the PFM threshold, the controller goes into sleep mode until V_{OUT} has dropped slightly (20mV measured at the feedback pin). At this time, the controller will turn back on and operate at fixed frequency for a short duration (typically a few hundred microseconds) until the output voltage has increased and the error amplifier output voltage has dropped below the PFM threshold once again. Then the converter will turn off and the cycle will repeat. This results in a very low duty cycle of operation, reducing all losses and greatly improving light load efficiency. During sleep mode, most of the circuitry internal to the UCC39421 is powered down, reducing quiescent current and maximizing efficiency.

APPLICATION INFORMATION (cont.)

The peak inductor current at which this mode will be entered is user programmable, by setting the voltage on the PFM pin. This can be done with a single resistor in series with the feedback divider, as shown in the application diagrams. The nominal peak current threshold for PM mode will be defined by:

$$I_{PEAK} \cong \frac{\left(\frac{1.25 \bullet R1}{(R1+R2)}\right) - 0.3}{K \bullet R_{SENSE}} \quad (3)$$

Where 0.3V is the internal offset and K is the nominal current sense amplifier gain of 10 and R_{SENSE} is the value of the current sense resistor. Note that in this case, the PFM pin voltage is set by the R1/R2 resistive divider off of the FB pin, which is regulated to 1.25V.

To further increase efficiency in Pulse mode, the gate drive on the CHRG pin will be held in the LP mode for 200µsec each time the controller comes on. This keeps gate drive losses low, even though the error amplifier output voltage may overshoot slightly when coming out of PFM. During sleep mode, the COMP pin is forced to 50mV above the PFM pin voltage. This minimizes error amplifier overshoot when coming out of sleep mode, and prevents erroneously tripping the PFM comparator.

Disabling PFM Mode

The user may disable PFM mode by pulling the PFM pin below 0.2V. In this case, the UCC39421 will remain on, in fixed frequency operation at all load currents. The PFM pin can also be driven, through a resistive divider, off of an output from the system controller. This allows the system controller to prepare for an expected step increase in load, improving the converter's large signal transient response. An example of this is shown in Fig 3.

Choosing a Topology and Optimal Synchronous Rectifier

The UCC39421 is designed to be very flexible, and can be used in Boost, Flyback and SEPIC topologies. It can operate from input voltages between 1.8 and 8.0V. Output voltages can be between 2.5V and 8.0V. (Note that at higher input voltages, such as from four or five Alkaline or Nickel cells or two Li-ion cells, a buck regulator would usually be employed.) It will also drive either N-channel or P-channel MOSFET synchronous rectifiers. Table 1 can be used to select the appropriate topology for a given combination of input and output voltage requirements. Although it is designed to operate as a peak current mode controller, it can also be configured for voltage mode control. This will be discussed in a later section.

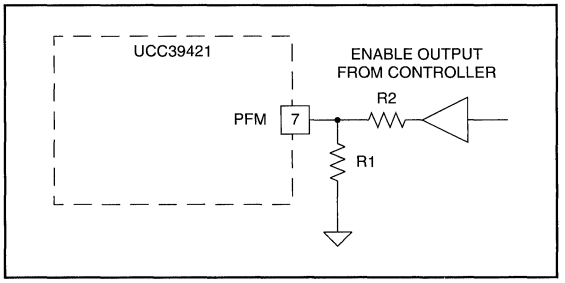


Figure 3. Driving the PFM pin from a controller output.

The user can program the gate drive output on the RECT pin for N-channel MOSFETs by grounding the RSEL pin, or for P-channel MOSFETs by connecting the RESEL pin to VIN. Table 2 is used to determine whether an N or P channel synchronous rectifier should be used.

Note: *In all cases, low voltage logic MOSFETs should be used to achieve the lowest possible on-resistance for the highest efficiency.*

The application diagrams in Figs 4-8 illustrate the use of the UCC39421 in all the topologies, using N and P channel rectifiers. They will be discussed in detail in the next section.

Note that the higher the frequency of operation, the more critical the MOSFET gate charge becomes for efficiency, particularly at light loads. However, high load currents demand lower RDS_{ON}, which will tend to increase gate charge. These two parameters should be balanced. At lower frequencies, the gate charge will become less important, at 1MHz or more, it is critical.

Table I. Selecting Topology Based on Input and Output Voltage Requirements

Cell Type	No. of Cells	V_{IN} Range	V_{OUT}	Topology
Alkaline or NiCd, NiMH	2	1.8V -3.0V	3.0 < V < 8.0	Boost
	3	2.7V - 4.5V	2.5 < V < 3.9	Flyback or SEPIC
			4.5 < V < 8.0	Boost
Li-Ion	1	2.3V - 4.2V	2.5 < V < 3.6	Flyback or SEPIC
			4.2 < V < 8.0	Boost

APPLICATION INFORMATION (cont.)

Boost Topology

The boost topology is simple and efficient, and should be used whenever the desired output voltage is greater than the maximum input voltage.

Boost Using Two N-Channel MOSFETs

A boost converter using two N-channel MOSFETs is shown in Fig 4. This configuration is optimal for output voltages below 4V, where the output voltage may not be high enough to provide optimal gate drive for a P-channel MOSFET. Note that in this case, a charge pump is required to provide proper gate drive levels. This is easily accomplished by adding an external diode and a capacitor, as shown. The diode connects from the output voltage to the CP pin. It should be an ultrafast or a Schottky diode. A 0.1μF ceramic capacitor is connected from the drain of the charge FET to the CP pin. This is the "flying" cap that will be charged to (V_{OUT} – V_{DIODE}) every time the charge FET is on. A charge pump reservoir cap is connected from the VPUMP pin to ground. It should be at least 1μF. A high speed active rectifier inside the UCC39421 charges the pump capacitor from the CP pin. The charge pump voltage will be:

Table II. Selecting Synchronous Rectifier Based on Topology and Output Voltage

Topology	VOUT	Synchronous Rectifier
Boost	3.0 < V < 8.0	P-channel (low voltage logic)
	V < 4.0	N-channel (low voltage logic) *Note: Requires a diode and a capacitor for the charge pump*
Flyback	2.5 < V < 3.0	N-channel (low voltage logic) *Note: Requires a diode and a capacitor for the charge pump*
	3.0 < V < 8.0	N-channel (low voltage logic)
SEPIC	3.0 < V < 8.0	P-channel (low voltage logic)

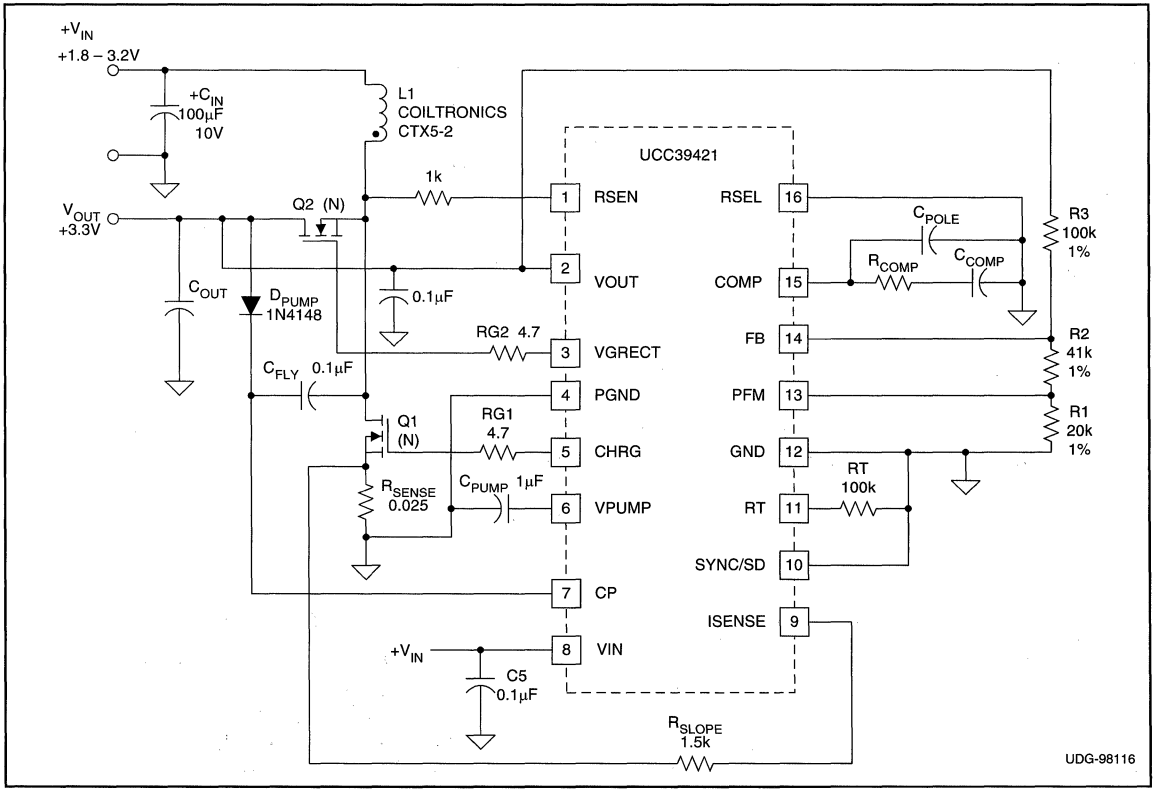


Figure 4. Application diagram for the boost topology using an N-channel synchronous rectifier.

APPLICATION INFORMATION (cont.)

$$V_{PUMP} \cong 2 \bullet V_{OUT} \quad (4)$$

For a block diagram of the charge pump logic, refer to Fig 12.

***Note**: A charge pump should not be used at output voltages over 4.0V to avoid pump voltages exceeding 8V.*

For other applications, where the charge pump is not required, the CP pin should be grounded and the VPUMP pin should be connected to either V_{OUT} or V_{IN}, whichever is greater.

Boost Using N & P Channel MOSFETs

For output voltages greater than the input and greater than about 3.0V, a P-channel MOSFET may be used for the synchronous rectifier. This configuration is shown in Fig 5. In this case, the VPUMP pin should be connected to V_{OUT}. This configuration can be used for a 3.3V output if a low voltage logic MOSFET is used.

Relating Peak Inductor Current to Average Output Current for the Boost Converter

For a continuous mode boost converter, the average output current is related to the peak inductor current by the following:

$$I_{PEAK} = \left(\frac{I_{OUT}}{(1-D)}\right) + \frac{di}{2} \quad (5)$$

where D is the duty cycle and the inductor ripple current, dI, is defined as:

$$di = \frac{t_{ON} \bullet V_{IN}}{L} = \frac{D \bullet V_{IN}}{f \bullet L} \quad (6)$$

where f is the switching frequency and L is the inductor value. The duty cycle is defined as:

$$D = \left(\frac{V_O - V_{IN}}{V_O}\right) \quad (7)$$

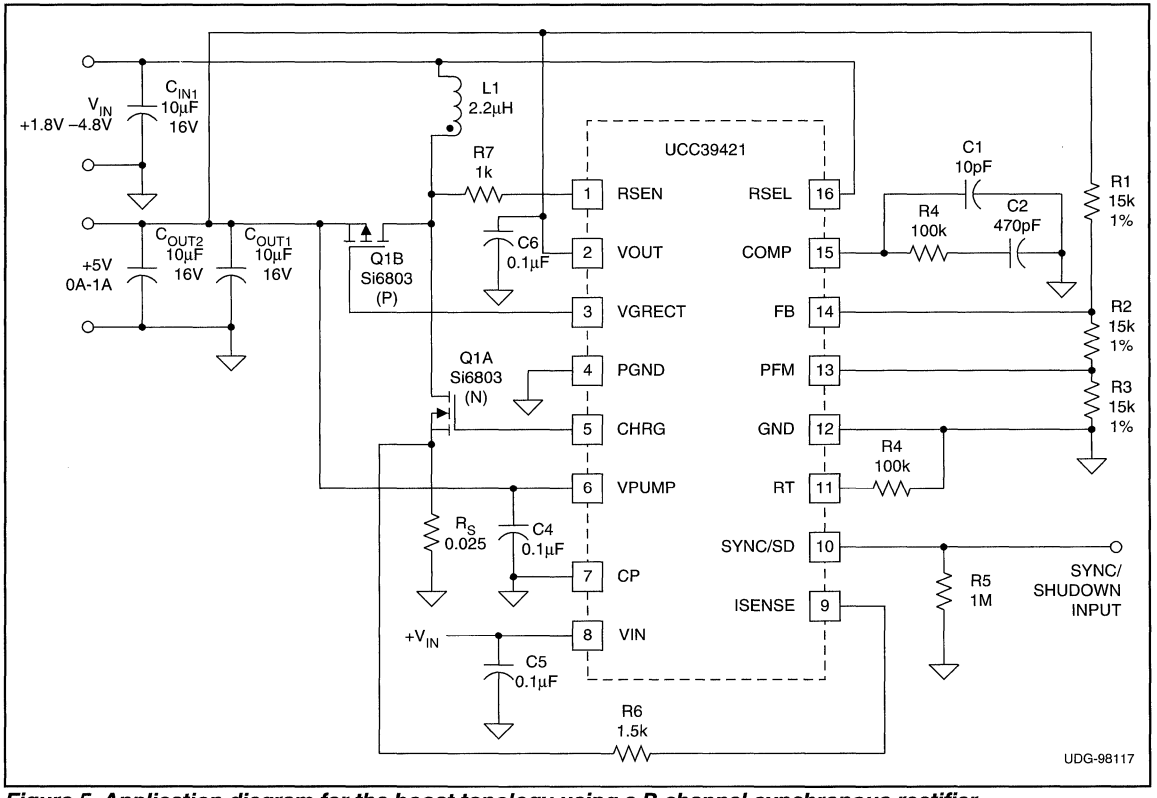


Figure 5. Application diagram for the boost topology using a P-channel synchronous rectifier.

APPLICATION INFORMATION (cont.)

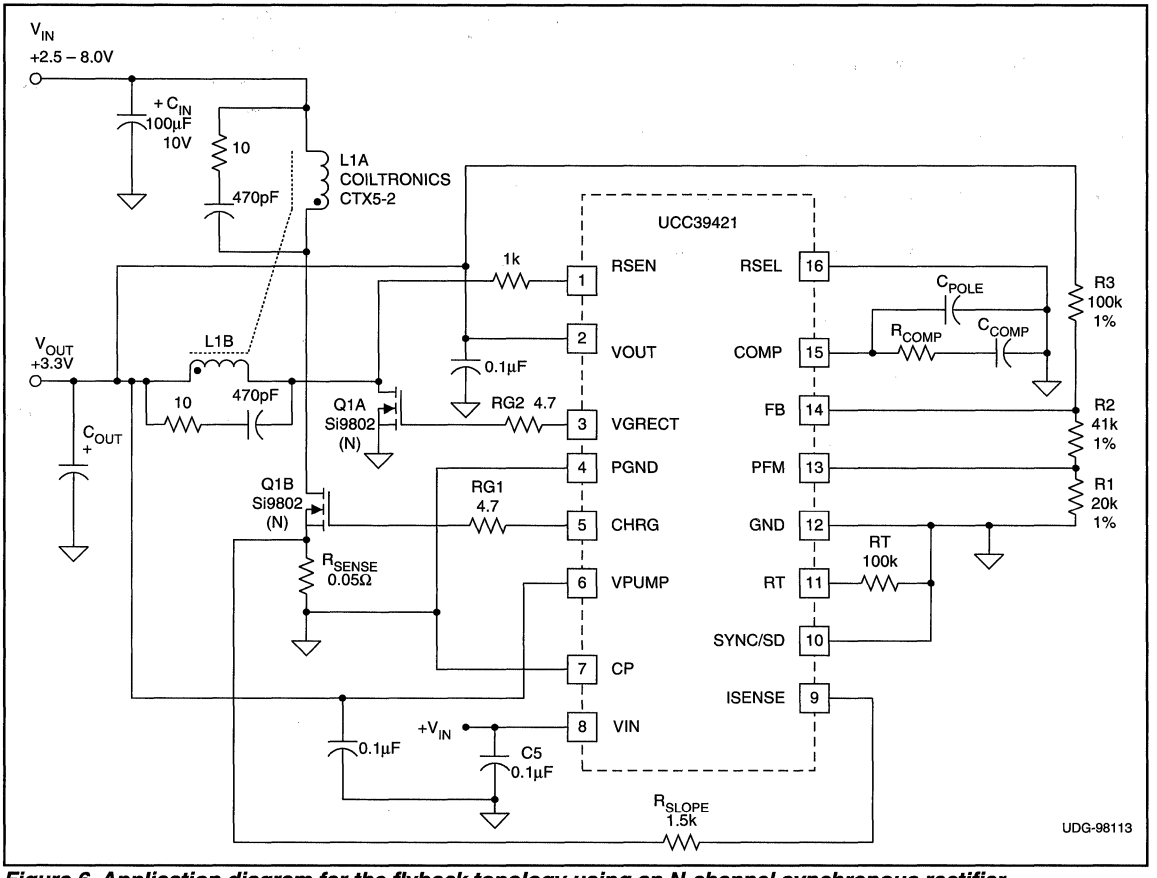


Figure 6. Application diagram for the flyback topology using an N-channel synchronous rectifier.

Substituting equations (6) and (7) into equation (5) yields:

$$I_{PEAK} = \frac{I_O}{\left(1-\left(\frac{V_O - V_{IN}}{V_O}\right)\right)} + \frac{V_{IN}}{2 \bullet f \bullet L} \bullet \left(\frac{V_O - V_{IN}}{V_O}\right) \quad (8)$$

***Note**: In these equations, the voltage drop across the rectifier has been neglected.*

Flyback Topology Using N-Channel MOSFETs

A flyback converter using the UCC39421 is shown in Fig 6. It uses a standard two-winding coupled inductor with a 1:1 turns ratio. The advantage of this topology is that the output voltage can be greater or less than the input voltage, as shown in Table 1. For example, this is ideal for generating 3.3V from a Lithium-Ion cell. Note that RC snubbers are placed across the primary and secondary windings to reduce ringing due to leakage inductance. These are optional, and may not be required in the application.

Note that for flyback converters where V_{IN} and V_{OUT} may both be below 3V, a charge pump is needed to provide adequate gate drive. This is illustrated in the example if Fig. 7.

APPLICATION INFORMATION (cont.)

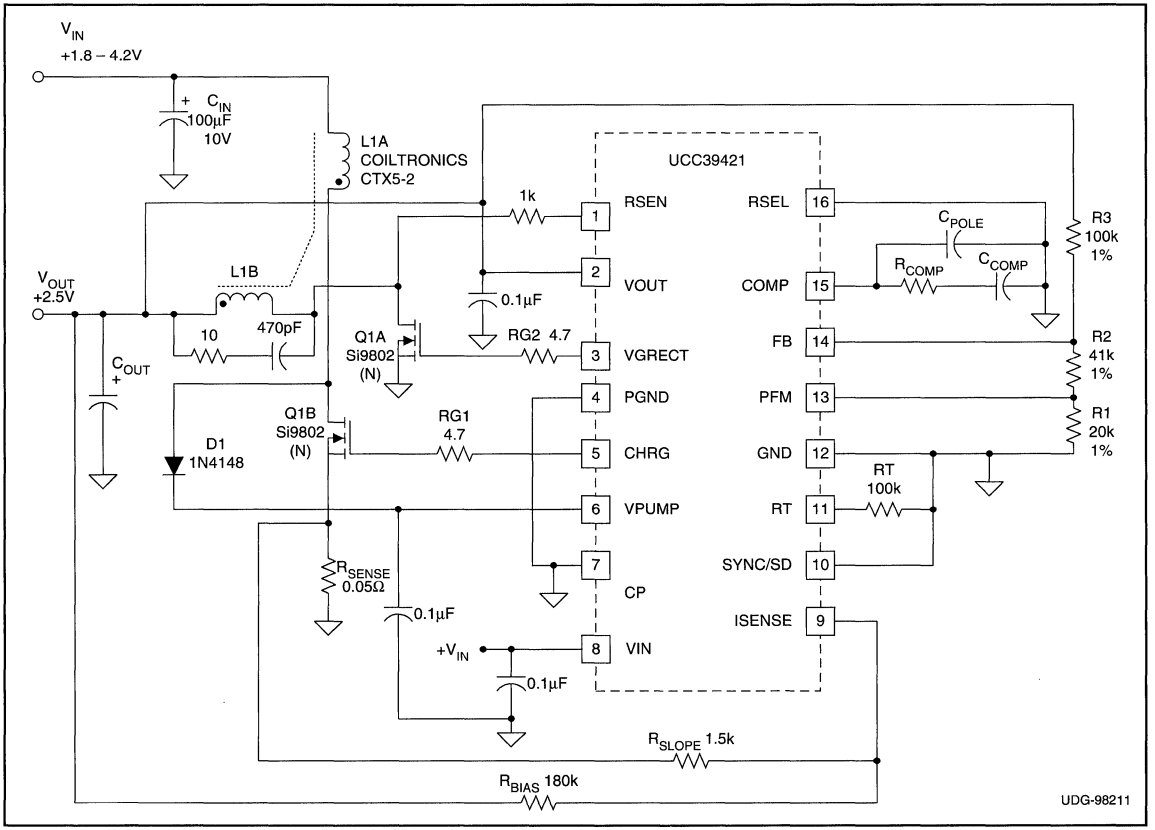


Figure 7. Flyback converter using charge pump input for low voltage operation.

Relating Peak Inductor Current to Average Output Current for the Flyback Converter

For a continuous mode flyback converter, the average output current is related to the peak inductor current by the following:

$$I_{PEAK} = \left(\frac{I_{OUT}}{1-D}\right) + \frac{di}{2} \quad (9)$$

Where D is the duty cycle and the inductor ripple current, dI, is defined as:

$$di = \frac{t_{ON} \bullet V_{IN}}{L} = \frac{D \bullet V_{IN}}{f \bullet L} \quad (10)$$

Where f is the switching frequency and L is the inductor value. The duty cycle is defined as:

$$D = \left(\frac{V_O}{V_{IN} + V_O}\right) \quad (11)$$

Substituting equations (10) and (11) into equation (9) yields:

$$I_{PEAK} = \frac{I_O}{\left(1 - \left(\frac{V_O}{V_{IN} + V_O}\right)\right)} + \frac{V_{IN}}{2 \bullet f \bullet L} \bullet \left(\frac{V_O}{V_{IN} + V_O}\right) \quad (12)$$

Figure 7 shows an example of a flyback converter where both V_{IN} and Vout may be quite low in voltage. In this case, a diode has been added to peak detect the voltage on the drain of the charge FET and use it for the pump input voltage. This is used to drive the gates of the FETs. To assure that the pump voltage will be used (rather than V_{IN}, which may be low), resistor R_{BIAS} has also been added to the ISENSE input to inhibit LP mode. This technique is discussed further in the section about Changing the Low Power Threshold.

APPLICATION INFORMATION (cont.)

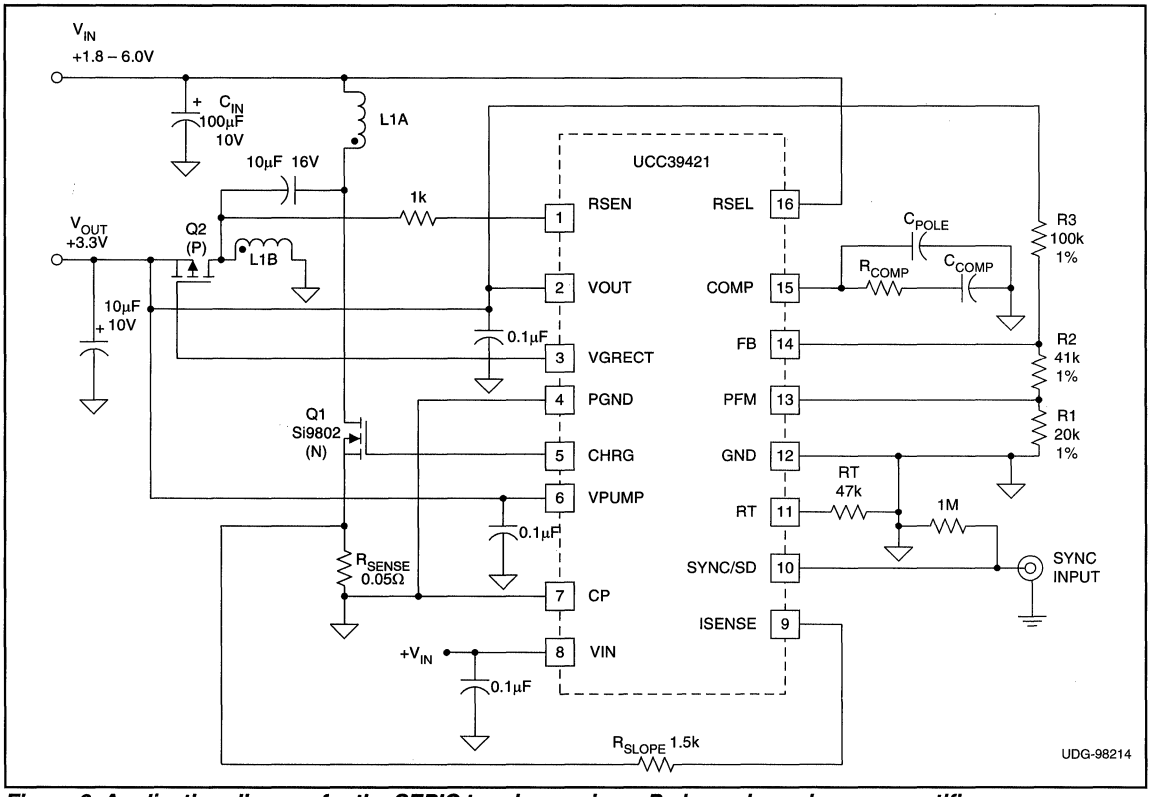


Figure 8. Application diagram for the SEPIC topology using a P-channel synchronous rectifier.

SEPIC Topology Using N & P Channel MOSFETs

The UCC39421 may also be used in the SEPIC (Single Ended Primary Inductance Converter) topology. This topology, which is similar to the flyback, uses a capacitor to aid in energy transfer from input to output. This configuration is shown in Fig 8. The N-channel synchronous rectifier has been changed to a P-channel and moved to the other end of the inductor's secondary winding, and a new capacitor has been placed across the dotted ends of the two windings. The SEPIC topology offers the same advantage of the flyback in that it can generate an output voltage that is greater or less than the input voltage. However it also offers improved efficiency. Although it requires an additional capacitor in the power stage, it greatly reduces ripple current in the input capacitor and improves efficiency by transferring the energy in the leakage inductance of the coupled inductor to the output. This also provides snubbing for the primary and secondary windings, eliminating the need for RC snubbers. Note that the capacitor must have low ESR, with sufficient ripple current rating for the application. Another advantage of the SEPIC is that the inductors don't have to be on the same core.

APPLICATION INFORMATION (cont.)

PWM Duty Cycle and Slope Compensation

All boost and flyback converters using peak current mode control are susceptible to a phenomenon known as sub-harmonic oscillation when operated in the continuous conduction mode beyond 50% duty cycle. Continuous conduction mode (CCM) means that the inductor current never goes to zero during the switching cycle. For a CCM boost converter, the required duty cycle for a given input and output voltage (neglecting voltage drops across the MOSFET switches) is given by equation (7). This is shown graphically for a number of common output voltages in Fig 9. For example, it can be seen that for a 3.3V output (using the boost topology) slope compensation will not be required because the duty cycle will never exceed 50%.

For the flyback topology, using a coupled inductor with a 1:1 turns ratio, the duty cycle is defined by equation (11). This is shown graphically for a number of common output voltages in Fig. 10.

To prevent sub-harmonic oscillation beyond 50% duty cycle, a technique called slope compensation is used, which modifies the slope of the current ramp. This is accomplished by adding a part of the timing ramp to the current sense input. In the UCC39421 this can be done by simply adding a resistor in series with the ISENSE input. A current is sourced within the IC which is proportional to the internal timing ramp voltage. The value of the resistor will determine the amount of slope compensation added.

The slope compensation output current at the ISENSE pin is equal to:

$$I_{SLOPE} = \frac{1}{R_T}\ A/\mu\,\text{sec} \qquad (13)$$

where R_T is the timing resister in Ohms (Ω), The required slope compensation resistor for a boost configuration is given by:

$$R_{SLOPE} = \frac{\left(V_{OUT} - 2 \bullet V_{IN(min)}\right) \bullet R_{SENSE} \bullet R_T}{L} \qquad (14)$$

where R_{SENSE} is the current sense resistor value in Ohms (Ω) and L is the inductor value in microHenries (μH), For a flyback topology, using a 1:1 turns ratio, the equation becomes:

$$R_{SLOPE} = \frac{\left(V_{OUT} - V_{IN(min)}\right) \bullet R_{SENSE} \bullet R_T}{L} \qquad (15)$$

If the converter is operated in the discontinuous conduction mode (inductor current drops to zero), no slope compensation is required. The point at which this mode boundary occurs is a function of switching frequency, input voltage, output voltage, load current and inductor value. However, in general the converter will be more efficient when operated in the continuous conduction mode due to the lower peak currents.

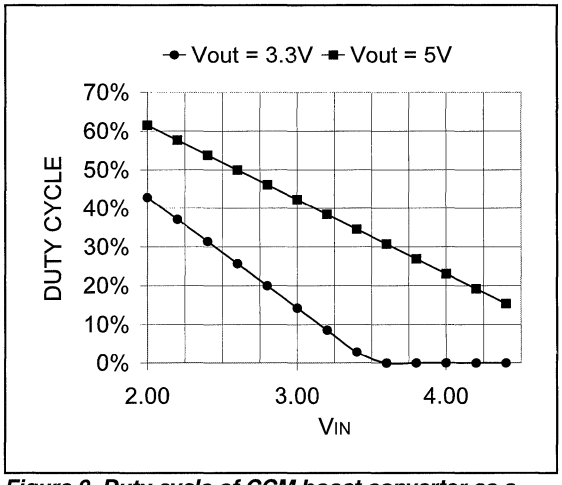


Figure 9. Duty cycle of CCM boost converter as a function of input and output voltage.

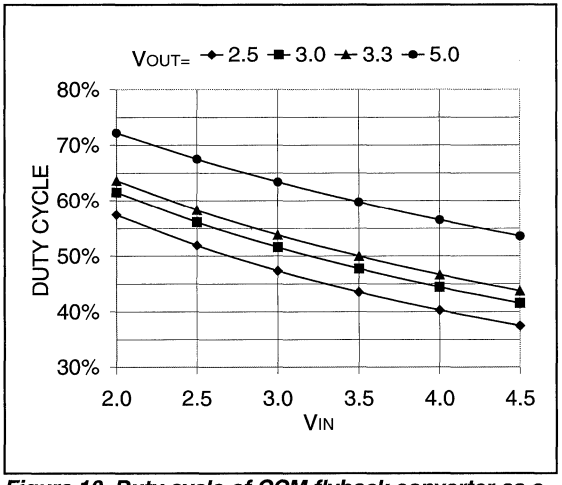


Figure 10. Duty cycle of CCM flyback converter as a function of input and output voltage.

APPLICATION INFORMATION (cont.)

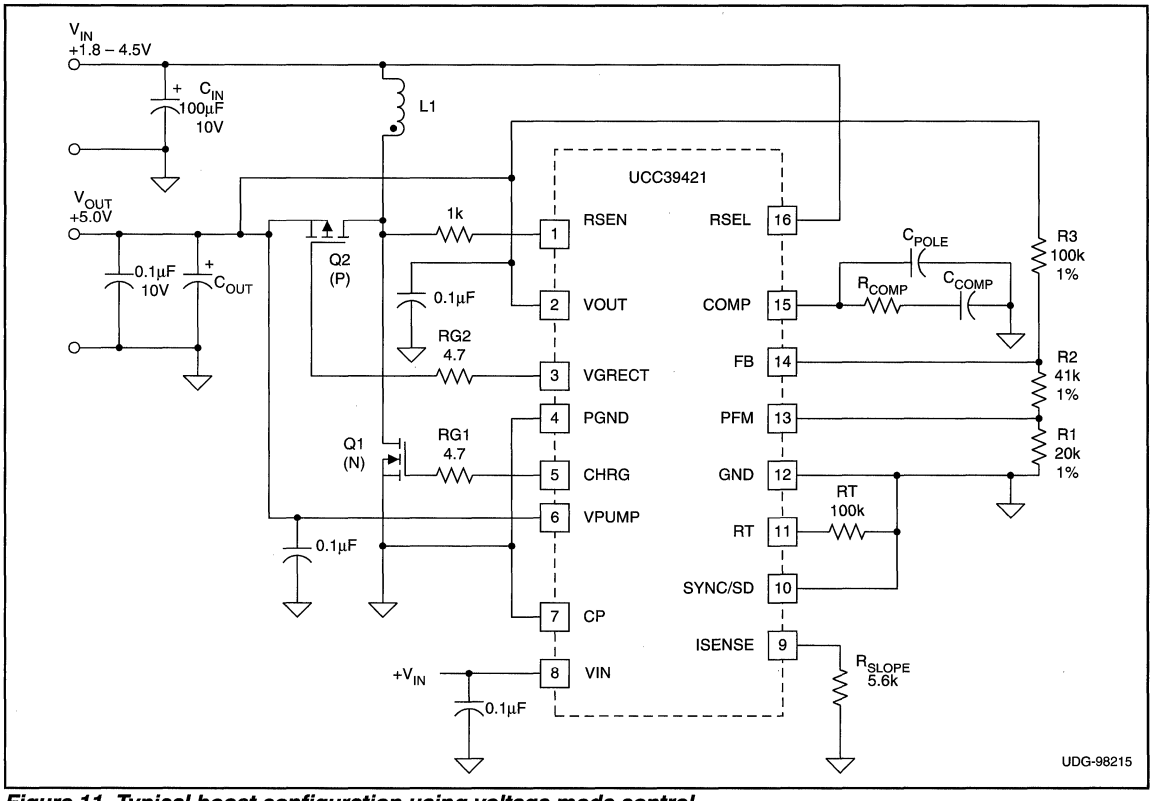


Figure 11. Typical boost configuration using voltage mode control

Voltage Mode Control

The UCC39421 can be operated as a voltage mode controller by connecting a 5.6k resistor from the ISENSE pin to ground. The internal current source will generate an artificial ramp voltage on this input. In this case, no slope compensation is required, and no current sense resistor is required in series with the source of the N-channel MOSFET. A typical application diagram is shown in Fig 11. However, in this configuration there will be no overcurrent protection. In addition, the Pulse and Low Power modes, designed to increase efficiency at light loads, will operate at different load currents. This is because the internal error amplifier's output voltage is no longer a direct function of load current, but rather of duty cycle. When operating in CCM, the duty cycle is largely a function of input and output voltage, not load current. At light enough loads however, the converter will go into discontinuous mode and the error amplifier voltage will drop low enough to activate the Low Power and Pulse modes.

Start Up

The UCC39421 incorporates a unique feature to help it start-up at low input voltages. If the input voltage is below 2.5V at start-up, a separate control circuit takes over until V_{OUT} or V_{PUMP} gets above 2.5V. In this mode, the charge MOSFET is turned on for 5µsec, or until the voltage on the ISENSE pin reaches 36mV, whichever occurs first. The charge MOSFET then remains off for a fixed time of 2.5µsec, and the body diode of the synchronous rectifier MOSFET is used to supply current to the output. This cycle repeats until either V_{OUT} or V_{PUMP} exceeds 2.5V. This results in constant off time control, with a minimum switching frequency of approximately 120kHz. During this low voltage start-up mode, all other internal circuitry is off, including the synchronous rectifier drive and the slope compensation current source. The peak inductor current during this mode is limited to:

$$I_{PEAK} = \frac{.036}{R_{SENSE}} \quad (13)$$

APPLICATION INFORMATION (cont.)

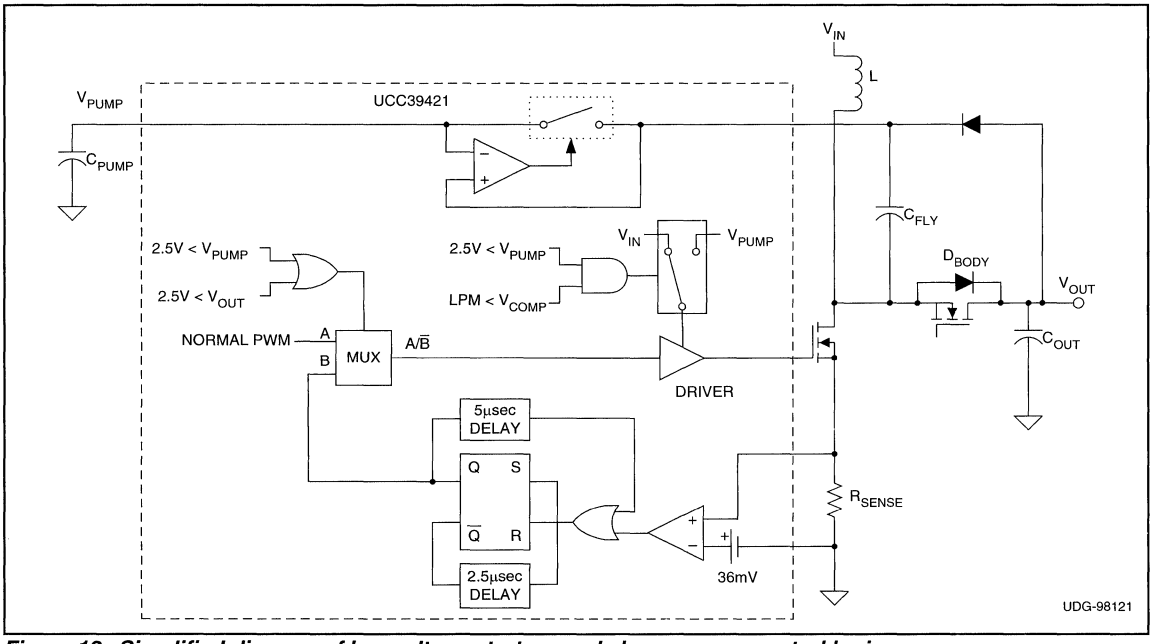


Figure 12. Simplified diagram of low voltage start-up and charge pump control logic.

If input voltages below 2.5V are expected, it is important to use a low voltage logic N-channel MOSFET (with a threshold voltage around 1V or less) to guarantee start-up at full load.

A block diagram of the low voltage start-up logic is shown in Fig 12.

Anti Cross-Conduction and Adaptive Synchronous Rectifier Commutation Logic

When operating in the continuous conduction mode (CCM), the charge MOSFET and the synchronous rectifier MOSFET are simply driven out of phase, so that when one is on the other is off. There is a built-in time delay of about 30nsec to prevent any cross-conduction.

In the event that the converter is operating in the discontinuous conduction mode (DCM), the synchronous rectifier needs to be turned off sooner, when the rectifier current drops to zero. Otherwise, the output will begin to discharge as the current reverses and goes back through the rectifier to the input. (This obviously cannot happen when using a conventional diode rectifier). To prevent this, the UCC39421 incorporates a high speed comparator which senses the voltage on the synchronous rectifier (using the RSEN input) for purposes of commutation. In the boost and SEPIC topologies, the synchronous rectifier is turned off when the voltage on the RSEN pin goes negative with respect to V_{OUT}. For this reason it is important to have the V_{OUT} pin well decoupled.

In the flyback topology however (using a ground referenced N-channel MOSFET rectifier), the rectifier voltage is sensed on the MOSFET drain, with respect to ground rather than V_{OUT}. The voltage polarity in this case is opposite that of the boost and SEPIC topologies. This problem is solved with the adaptive logic within the UCC39421. During each charge cycle, while the N-channel charge FET is on, a latch is set if the voltage on the RSEN pin exceeds $V_{IN}/2$. This indicates a flyback topology, since this node will be equal to or greater than V_{IN} at this time. In the case of the boost and the SEPIC, the voltage at the RSEN input will be near or below ground, and the latch will not be set. This allows the UCC39421 to sense which topology is in use and adapt the synchronous rectifier commutation logic accordingly. Note that the RSEN input must have a series resistor to limit the current when going below ground. Values less than or equal to 1k are recommended to prevent time delay due to stray capacitance.

APPLICATION INFORMATION (cont.)

Current Sense Amplifier and Leading Edge Blanking

The UCC39421 includes a high speed current sense amplifier with a nominal gain of 10 to minimize losses associated with the current sense resistor. The amplifier was designed to provide good response and minimal propagation delay, allowing switching frequencies over 2MHz. The current sense resistor should be chosen to provide a maximum peak voltage of 100mV at full load, with the minimum input voltage.

A leading edge blanking time of 40nsec is provided to filter out leading edge spikes in the current sense waveform. In most applications, this will eliminate the need for a filter cap on the ISENSE pin.

Overcurrent Protection

The UCC39421 includes a peak current limit function. If the voltage on the ISENSE pin exceeds 0.15V after the initial blanking period, the pulse will be terminated and the charge MOSFET will be turned off.

Sync/Shutdown Input

The SYNC/SD pin has two functions; it may be used to synchronize the UCC39421's switching frequency to an external clock, or to shutdown the IC entirely. In shutdown, the quiescent current is reduced to just a few microamps.

To synchronize the internal clock to an external source, the SYNC/SD pin must be driven high, above 2.0V minimum. The circuitry syncs to the rising edge of the input, the pulse width is not critical.

To shutdown the converter, the SYNC/SD pin must be held high (above 2.0V) for a minimum of 20µsec.

This pin should be grounded if not used.

Changing the Low Power Mode Threshold

For some applications the user may want to lower the Low Power (LP) mode threshold, or even eliminate this feature altogether. For example, if a boost topology is being used, and the input voltage is below 2.5V, the gate drive to the charge FET may want to be derived from the pump (or output) voltage under all load conditions, rather than from V_{IN}. This means the converter would never be allowed to operate in LP mode.

Although the LP mode threshold is internally fixed at 0.5V (referenced to the COMP pin), the point at which the LP mode is entered can be easily modified by adding a single resistor, as shown in Fig 13. Resistor R_{BIAS} forms a divider with R_{SLOPE} (used for slope compensation) and adds a DC offset to the current sense input, raising the output voltage of the sense amplifier and "fooling" the LP mode comparator into thinking the load is higher than it is. The required bias resistor to transition out of LP mode for a given peak current can be calculated using the following equation:

$$R_{BIAS} = \frac{R_{SLOPE} \bullet V_{OUT}}{0.02 - I_{PEAK} \bullet R_{SENSE}} \qquad (14)$$

Due to the current sense amplifier gain of 10 and the internal offset of 300mV, an offset of just 20mV or more at the ISENSE pin will inhibit LP mode altogether. Note that inhibiting LP mode does not prevent PFM from working, as long as the PFM pin is set to a voltage higher than:

$$(10 \bullet V_{ISENSE}) + 0.3V \qquad (15)$$

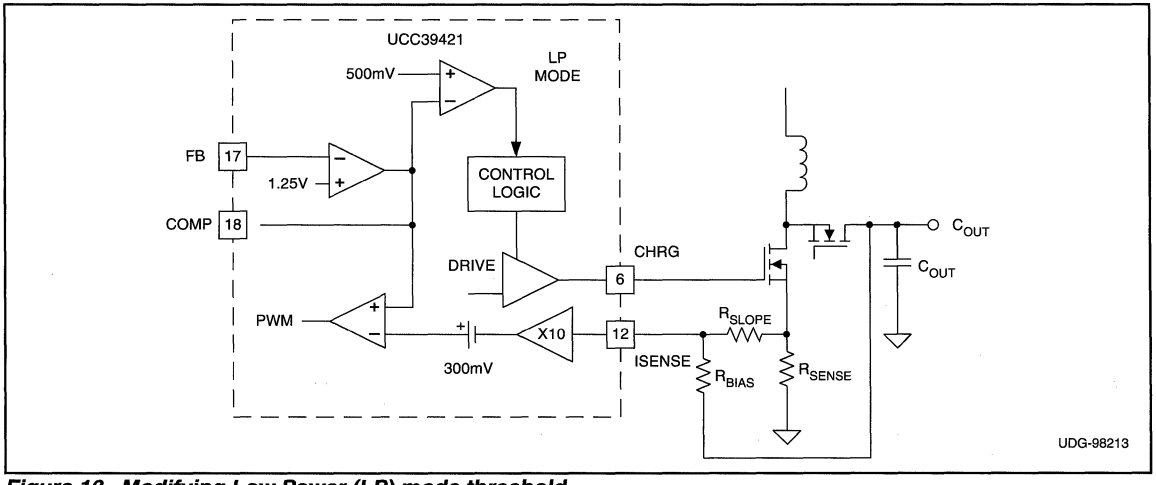


Figure 13. Modifying Low Power (LP) mode threshold.

APPLICATION INFORMATION (cont.)

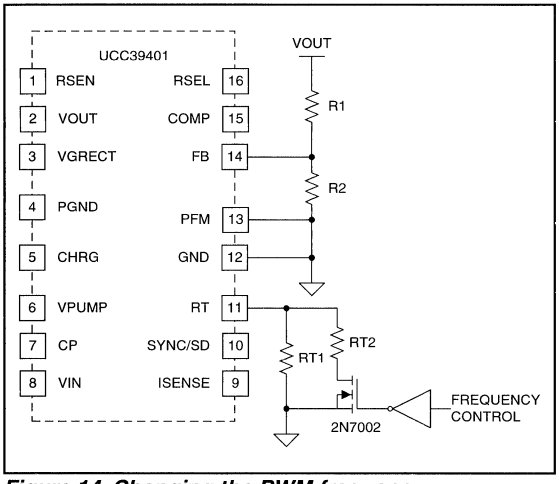


Figure 14. Changing the PWM frequency.

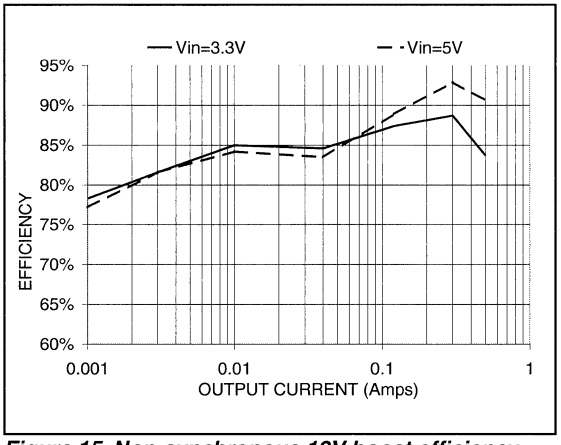


Figure 15. Non-synchronous 12V boost efficiency. (f=550KHz, L=6.8µH DT3316P-682, IRF7601, MBR0530, VPFM=0.5V)

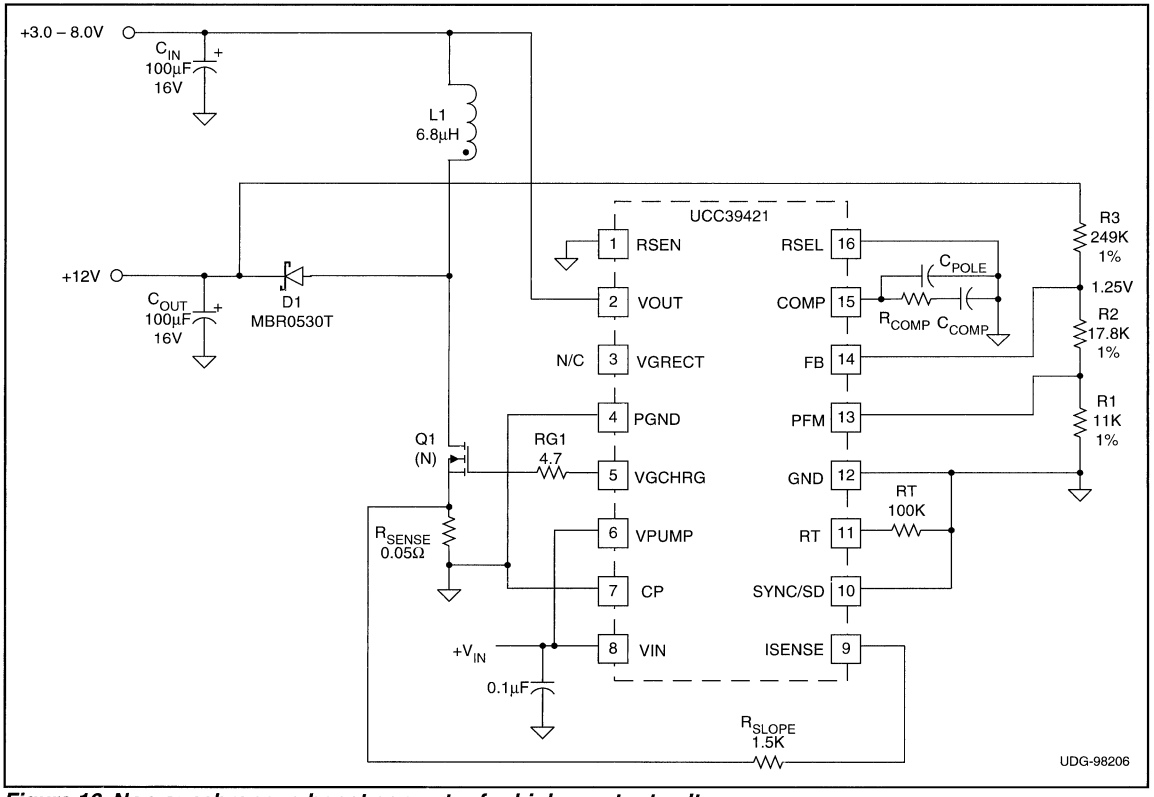


Figure 16. Non-synchronous boost converter for higher output voltages.

APPLICATION INFORMATION (cont.)

Programming the PWM Frequency

Some applications may want to remain in a fixed frequency mode of operation, even at light load, rather than going into PFM mode. This lowers efficiency at light load. One way to improve the efficiency while maintaining fixed frequency operation is to lower the PWM frequency under light load conditions. This can be easily done, as shown in Fig 14. By adding a second timing resistor and a small MOSFET switch, the host can switch between two discrete frequencies at any time.

Non-Synchronous Boost for Higher Output Voltage Applications

The UCC39421 can also be used in a non-synchronous application to provide output voltages greater than 8 volts from low voltage inputs. An example of a 12V boost application is shown in Fig 16. Since none of the IC pins are exposed to the boosted voltage, the output voltage is limited only by the ratings of the external MOSFET, rectifier and filter capacitor. At these higher output voltages, good efficiency is maintained since the rectifier drop is small compared to the output voltage. Note that PFM mode can still be used to maintain high efficiency at light load. Typical efficiency causes are shown in Fig. 15.

Since all the power supply pins (VIN, VOUT, VPUMP) operate off the input voltage, it must be >2.5V and high enough to assure proper gate drive to the charge FET.

UCC39422 Features

The UCC39422 is a 20 pin device which adds a reset function and an uncommitted comparator to the UCC39421. A simplified diagram of the reset circuit is shown in Fig 17.

The reset circuit monitors the voltage at the feedback (FB) pin and issues a reset if the feedback voltage drops below 1.175V. This represents a 6% drop in output voltage. Monitoring the voltage internally at the FB pin eliminates the need for another external voltage divider. The RESET output is an open drain output which is active low during reset. It stays low until the feedback voltage is above 1.175V for a period of time called the reset pulse width, which is user programmable. An external capacitor on the RSADJ pin and an internal 1µA current source determine the reset pulse width, according to the following equation:

$$t_{RESET} \cong C_{RESET} \bullet 1.18 \qquad (16)$$

where t_{RESET} is the reset pulse width in seconds, and C_{RESET} is the capacitor value in microFarads (µF).

An adaptive glitch filter is included to prevent nuisance trips. This is implemented using a gm amplifier to charge an 8pF capacitor to 1.175V before declaring a reset. This provides a delay which is inversely proportional to the magnitude of the feedback voltage error. The delay time is approximated by the following equation:

$$t_{DELAY} \cong \frac{0.25}{1.175 - V_{FB}} \mu \text{ sec} \qquad (17)$$

where t_{DELAY} is the filter delay time in microseconds. Note that the maximum current from the gm amplifier is limited to 2µA, limiting the minimum time delay to 4.8µsec.

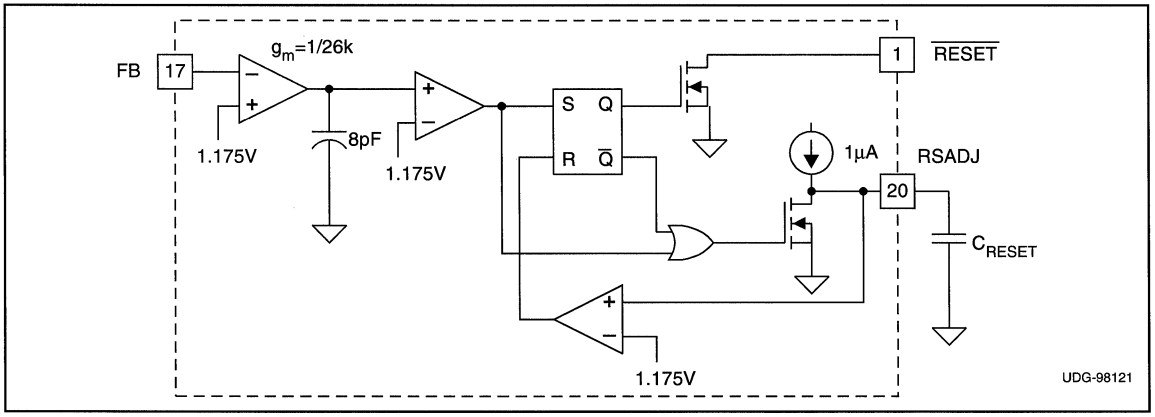


Figure 17. Reset circuitry.

APPLICATION INFORMATION (cont.)

A typical application schematic using the UCC39422 is shown in Fig. 18. In this example, R1 and R2 have been slected to trip the LOWBAT output when V_{IN} drops below 2.0V. Note that the $\overline{\text{RESET}}$ and LOWBAT outputs are open drain and require a pullup.

Selecting the Inductor

The inductor must be chosen based on the desired operating frequency and the maximum load current. Higher frequencies allow the use of lower inductor values, reducing component size. Higher load currents will require larger inductors with higher current ratings and less winding resistance to minimize losses. The inductor must be rated for operation at the highest anticipated peak current. Refer to equations (8) and (12) to calculate the peak inductor current for a boost or flyback design, based on V_{IN}, V_{OUT}, maximum load, frequency and inductor value.

Some manufacturers rate their parts for maximum energy storage in micro-Joules (µJ). This is expressed by:

$$E = 0.5 \bullet L \bullet I_{PEAK}^{\ 2} \qquad (18)$$

where E is the required energy rating in micro-Joules. L is the inductor value in microHenries (µH) (with current applied), and I_{PEAK} is the peak current in amps that the inductor will see in the application. Another way in which inductor ratings are sometimes specified is the maximum volt-seconds applied. This is given simply by:

$$E \bullet T = \frac{V_{IN} \bullet D}{f} \qquad (19)$$

where ET is the required rating in V-µsec, D is the duty cycle for a given V_{IN} and V_{OUT}, and f is the switching frequency in MHz. Refer to equations (7) and (11) to calculate the duty cycle for a CCM boost or flyback converter.

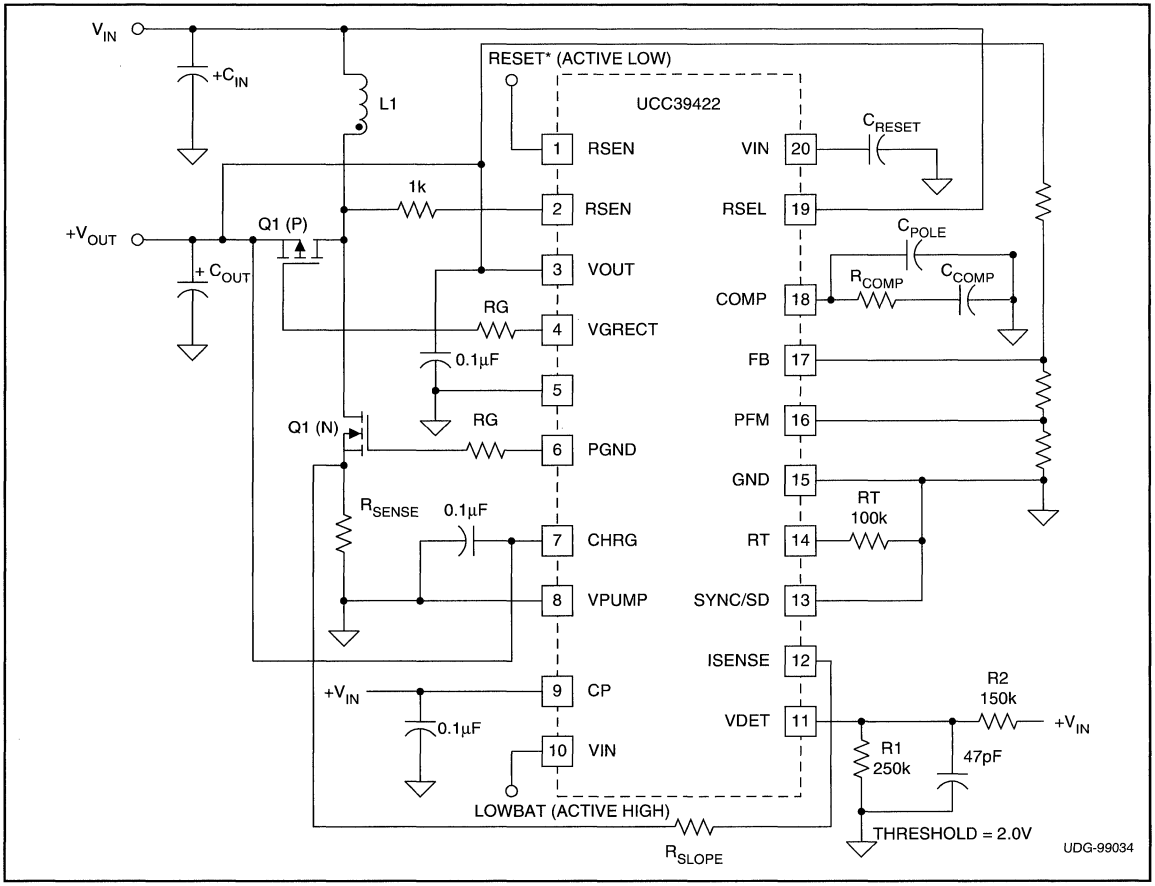


Figure 18. Typical UCC39422 application.

APPLICATION INFORMATION (cont.)

Table III. SMT commercial inductor manufacturers.

Coilcraft Inc. (800) 322-2645. 1102 Silver Lake RD, Cary, IL 60013
Coiltronics Inc. (407) 241-7876 6000 Park of Commerce Blvd, Boca Raton, FL 33487
Dale Electronics, Inc. (605) 665-9301 East Highway 50, Yankton, SD 57078
Pulse Engineering Ltd. (204) 633-4321 300 Keewatin Street, Winnipeg, MB R2X 2R9
Sumida Voice (65) 296-3388 Fax (65) 293-3390 Block 996, Bendemeer Rd., #04-05/06 Singapore 33944
BH Electronics (612) 894-9590 12219 Wood Lake Drive, Burnsville, MN 55337
Tokin America Inc. (408) 432-8020 155 Nicholson Lane, San Jose CA 95134

In any case, the inductor must use a low loss core designed for high frequency operation. High frequency ferrite cores are recommended. Some manufacturers of off-the-shelf surface mount designs are listed in Table III. For flyback and SEPIC topologies, use a two winding coupled inductor. SEPIC designs can also use two discrete inductors.

Selecting the Filter Capacitor

The input and output filter capacitors must have low ESR and low ESL. Surface mount tantalum, OSCON or multi-layer ceramics (MLC's) are recommended. The capacitor selected must have the proper ripple current rating for the application. Some recommended capacitor types are listed in Table IV.

Table IV. Recommended SMT Filter Capacitors

Manufacturer	Part Number	Features
AVX	TPS series	Low ESR tantalum
Kemet	T410 series	Low ESR tantalum
Murata	GRM series	Low ESR ceramic
Sanyo	OSCON series	Low ESR organic
Sprague	591D series	Low ESR, low profile tantalum
	594D series	Low ESR tantalum
Tokin	Y5U, Y5V Type	Low ESR ceramic

Circuit Layout and Grounding

As with any high frequency switching power supply, circuit layout, hookup and grounding are critical for proper operation. Although this may be a relatively low power, low voltage design, these issues are still very important. The MOSFET turn-on and turn-off times necessary to maintain high efficiency at high switching frequencies of 1MHz or more result in high dv/dt and di/dt's. This makes stray circuit inductance especially critical. In addition, the high impedances associated with low power designs, such as in the feedback divider, make them especially susceptible to noise pickup.

Layout

The component layout should be as tight as possible to minimize stray inductance. This is especially true of the high current paths, such as in series with the MOSFETs and the input and output filter caps.

The components associated with the feedback, compensation and timing should be kept away from the power components (MOSFETs, inductor). Keep all components as close to the IC pins as possible. Nodes that are especially noise sensitive are the FB and RT pins. Other sensitive pins are COMP and PFM.

Grounding

A ground plane is highly recommended. The PGND pin of the UCC39421 should be close to the grounded end of the current sense resistor, the input filter cap, and the output filter cap. The GND pin should be close to the grounded end of the RT resistor, the feedback divider resistor, the ISENSE cap (if used), and the compensation network.

MOSFET Gate Resistors

The UCC39421 includes low impedance CMOS output drivers for the two external MOSFET switches. The CHRG output has a nominal resistance of 4Ω, and the RECT has a nominal resistance of 2Ω. For high frequency operation using low gate charge MOSFETs, no gate resistors are required. To reduce high frequency ringing at the MOSFET gates, low value series gate resistors may be added. These should be non-inductive resistors, with a value of 2Ω to 10Ω, depending on the frequency of operation. Lower values will result in better switching times, improving efficiency.

Minimizing Output Ripple and Noise Spikes

The amount of output ripple will be determined primarily by the type of output filter capacitor and how it is connected in the circuit. In most cases, the ripple will be dominated by the ESR (Equivalent Series Resistance) and ESL (Equivalent Series Inductance) of the cap, rather than the actual capacitance value. Low ESR and ESL capacitors are mandatory in achieving low output ripple. Surface mount packages will greatly reduce the ESL of the capacitor, minimizing noise spikes. To further minimize high frequency spikes, a surface mount ceramic capacitor should be placed in parallel with the main filter cap. For best results, a capacitor should be chosen whose self-resonant frequency is near the frequency of the noise spike. For high switch frequencies, ceramic capacitors alone may be used, reducing size and cost.

APPLICATION INFORMATION (cont.)

For applications where the output ripple must be extremely low, a small LC filter may be added to the output. The resonant frequency should be below the selected switching frequency, but above that of any dynamic loads. The filter's resonant frequency is given by:

$$f_{RES} = \frac{1}{2\pi\sqrt{L \bullet C}} \quad (20)$$

Where f is the frequency in Hz, L is the filter inductor value in Henries and C is the filter capacitor value in Farads. It is important to select an inductor rated for the maximum load current and with minimal resistance to reduce losses. The capacitor should be a low impedance type, such as a tantalum.

If an LC ripple filter is used, the feedback point can be taken before or after the filter, as long as the filter's resonant frequency is well above the loop crossover frequency. Otherwise the additional phase lag will make the loop unstable. The only advantage to connecting the feedback after the filter is that any small voltage drop across the filter inductor will be corrected for in the loop, providing the best possible voltage regulation. However, the resistance of the inductor is usually low enough that the voltage drop will be negligible.

UNITRODE CORPORATION
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Microprocessor Supervisor with Watchdog Timer

FEATURES

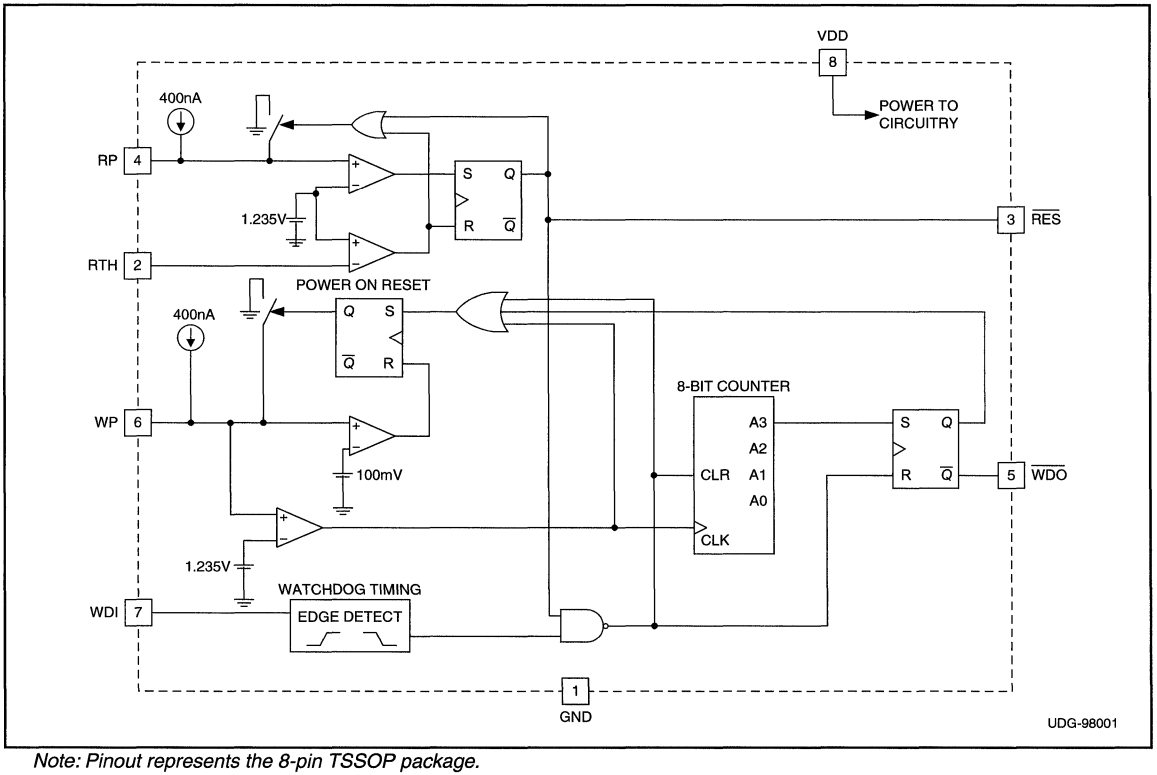
- Fully Programmable Reset Threshold
- Fully Programmable Reset Period
- Fully Programmable Watchdog Period
- 2% Accurate Reset Threshold
- VDD Can Go as Low as 2V
- 15µA Maximum IDD
- Reset Valid Down to 1V

DESCRIPTION

The UCC3946 is designed to provide accurate microprocessor supervision, including reset and watchdog functions. During power up, the IC asserts a reset signal $\overline{RES}$ with VDD as low as 1V. The reset signal remains asserted until the VDD voltage rises and remains above the reset threshold for the reset period. Both reset threshold and reset period are programmable by the user. The IC is also resistant to glitches on the VDD line. Once $\overline{RES}$ has been deasserted, any drops below the threshold voltage need to be of certain time duration and voltage magnitude to generate a reset signal. These values are shown in Figure 1. An I/O line of the microprocessor may be tied to the watchdog input (WDI) for watchdog functions. If the I/O line is not toggled within a set watchdog period, programmable by the user, $\overline{WDO}$ will be asserted. The watchdog function will be disabled during reset conditions.

The UCC3946 is available in 8-pin SOIC(D), 8-pin DIP (N or J) and 8-pin TSSOP(PW) packages to optimize board space.

BLOCK DIAGRAM



Note: Pinout represents the 8-pin TSSOP package.

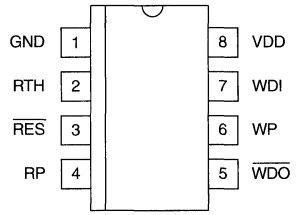
ABSOLUTE MAXIMUM RATINGS

V_{IN} 10V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature. . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

SOIC-8, TSSOP-8, DIL-8 (Top View)
D, PW, N or J Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VDD = 2.1V to 5.5V for UCC1946 and UCC2946; VDD = 2V to 5.5V for UCC3946; TA = 0°C to 70°C for UCC3946, –40°C to 85°C for UCC2946, and –55°C to 125°C for UCC1946; $T_A = T_J$

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
		UCC3946			UCC1946 & UCC2946			
Operating Voltage		2		5.5	2.1		5.5	V
Supply Current			10	15		12	18	µA
Minimum VDD	(Note 1)			1			1.1	V
Reset Section								
Reset Threshold	VDD Rising	1.21	1.235	1.26	1.15	1.235	1.26	V
Threshold Hysteresis			15			15		mV
Input Leakage				5			5	nA
Output High Voltage	I_{SOURCE} = 2mA	V_{DD} – 0.3			V_{DD} – 0.3			V
Output Low Voltage	I_{SINK} = 2mA			0.1			0.1	V
	VDD = 1V, I_{SINK} = 20uA			0.3			0.6	V
VDD to Output Delay	VDD = -1mV/µs (Note 2)		120			120		µs
Reset Period	C_{RES} = 64nF	160	200	260	140	200	320	ms
Watchdog Section								
WDI Input High		0.7· V_{DD}			0.7· V_{DD}			V
WDI Input Low				0.3· V_{DD}			0.3· V_{DD}	V
Watchdog Period	C_{WD} = 64nF	1.12	1.60	2.08	0.96	1.60	2.56	s
Watchdog Pulse Width		50			50			ns
Output High Voltage	I_{SOURCE} = 2mA	V_{DD} – 0.3			V_{DD} – 0.3			V
Output Low Voltage	I_{SINK} = 2mA			0.1			0.1	V

Note 1: This is the minimum supply voltage where $\overline{RES}$ is considered valid.
Note 2: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

GND: Ground reference for the IC.

$\overline{\text{RES}}$: This pin is high only if the voltage on the RTH has risen above 1.235V. Once RTH rises above the threshold, this pin remains low for the reset period. This pin will also go low and remain low if the RTH voltage dips below 1.235V for an amount of time determined by Figure 1.

RTH: This input compares its voltage to an internal 1.25V reference. By using external resistors, a user can program any reset threshold he wishes to achieve.

RP: This pin allows the user to program the reset period by adjusting an external capacitor.

VDD: Supply voltage for the IC.

WDI: This pin is the input to the watchdog timer. If this pin is not toggled or strobed within the watchdog period, $\overline{\text{WDO}}$ is asserted.

$\overline{\text{WDO}}$: This pin is the watchdog output. This pin will be asserted low if the WDI pin is not strobed or toggled within the watchdog period.

WP: This pin allows the user to program the watchdog period by adjusting an external capacitor.

APPLICATION INFORMATION

The UCC3946 supervisory circuit provides accurate reset and watchdog functions for a variety of microprocessor applications. The reset circuit prevents the microprocessor from executing code during undervoltage conditions, typically during power-up and power-down. In order to prevent erratic operation in the presence of noise, voltage "glitches" whose voltage amplitude and time duration are less than the values specified in Figure 1 are ignored.

The watchdog circuit monitors the microprocessor's activity, if the microprocessor does not toggle WDI during the programmable watchdog period $\overline{\text{WDO}}$ will go low, alerting the microprocessor's interrupt of a fault. The $\overline{\text{WDO}}$ pin is typically connected to the non-maskable input of the microprocessor so that an error recovery routine can be executed.

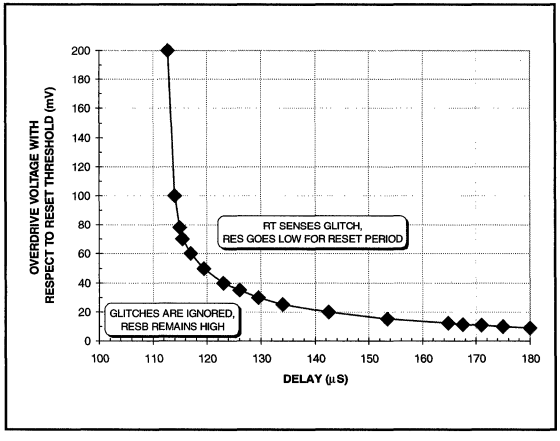


Figure 1.
Overdrive Voltage vs. Delay to Output Low on RESB

Slew rate: –1V/mS; Monitored Voltage = VDD

Programming the Reset Voltage and Reset Period

The UCC3946 allows the reset trip voltage to be programmed with two external resistors. In most applications VDD is monitored by the reset circuit, however, the design allows voltages other than VDD to be monitored. Referring to Figure 2, the voltage below which reset will be asserted is determined by:

$$V_{RESET} = 1.235 \bullet \frac{R1 + R2}{R2}$$

In order to keep quiescent currents low, resistor values in the megaohm range can be used for R1 and R2. A manual reset can be easily implemented by connecting a momentary push switch in parallel with R2. $\overline{\text{RES}}$ is guaranteed to be low with VDD voltages as low as 1V.

Once VDD rises above the programmed threshold, $\overline{\text{RES}}$ remains low for the reset period defined by:

$$T_{RP} = 3.125 \bullet C_{RP}$$

where TRP is time in milliseconds and CRP is capacitance in nanofarads. CRP is charged with a precision current source of 400nA, a high quality, low leakage capacitor (such as an NPO ceramic) should be used to maintain timing tolerances. Figure 3 illustrates the voltage levels and timings associated with the reset circuit.

Programming the Watchdog Period

The watchdog period is programmed with CWP as follows:

$$T_{WP} = 25 \bullet C_{WP}$$

where TWP is in milliseconds and CWP is in nanofarads. A high quality, low leakage capacitor should be used for CWP. The watchdog input WDI must be toggled with a high/low or low/high transition within the watchdog period to prevent $\overline{\text{WDO}}$ from assuming a logic level low. $\overline{\text{WDO}}$ will maintain the low logic level until WDI is toggled or $\overline{\text{RES}}$ is asserted. If at any time $\overline{\text{RES}}$ is asserted, $\overline{\text{WDO}}$

will assume a high logic state and the watchdog period will be reinitiated. Figure 4 illustrates the timings associated with the watchdog circuit.

Connecting $\overline{\text{WDO}}$ to $\overline{\text{RES}}$

In order to provide design flexibility, the reset and watchdog circuits in the UCC3946 have separate outputs. Each output will independently drive high or low, depending on circuit conditions explained previously.

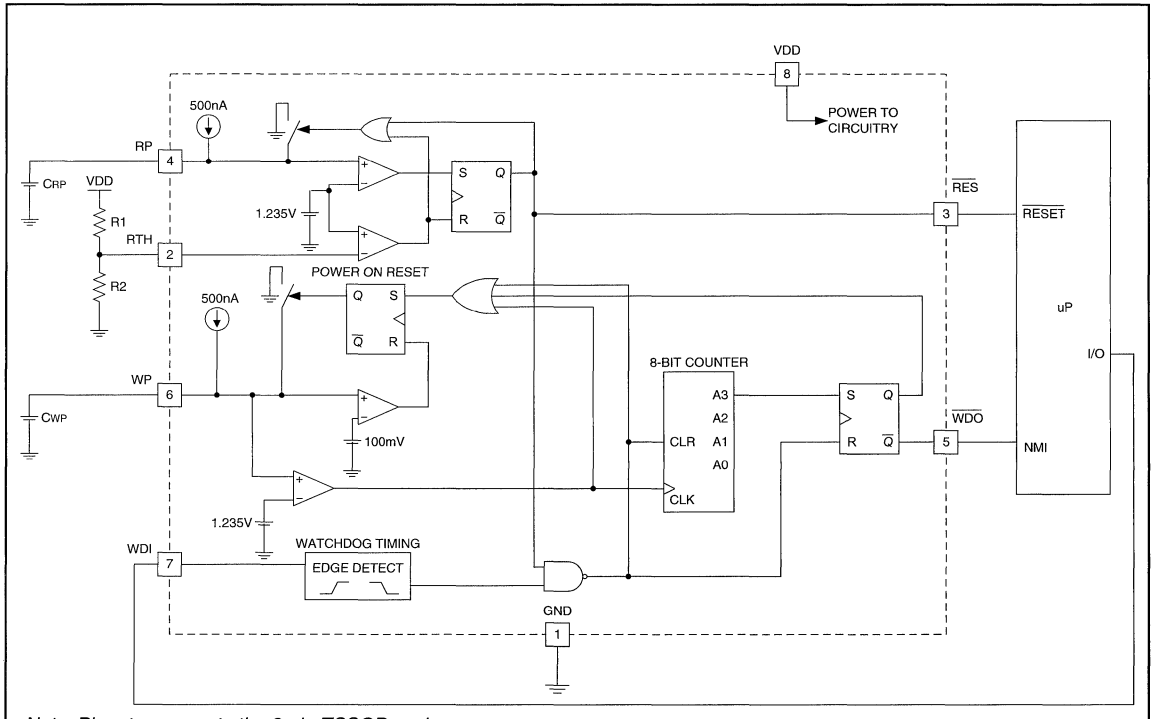
In some applications, it may be desirable for either the $\overline{\text{RES}}$ or $\overline{\text{WDO}}$ to reset the microprocessor. This can be done by connecting $\overline{\text{WDO}}$ to $\overline{\text{RES}}$. If the pins try to drive to different output levels, the low output level will dominate. Additional current will flow from VDD to GND during these states. If the application cannot support additional current (during fault conditions), $\overline{\text{RES}}$ and $\overline{\text{WDO}}$ can be connected to the inputs of an OR gate whose output is connected to the microprocessor's reset pin.

Layout Considerations

A 0.1µF capacitor connected from V_{DD} to GND is recommended to decouple the UCC3946 from switching transients on the V_{DD} supply rail.

Since RP and WP are precision current sources, capacitors C_{RP} and C_{WP} should be connected to these pins with minimal trace length to reduce board capacitance. Care should be taken to route any traces with high voltage potential or high speed digital signals away from these capacitors.

Resistors R1 and R2 generally have a high ohmic value, traces associated with these parts should be kept short in order to prevent any transient producing signals from coupling into the high impedance RTH pin.

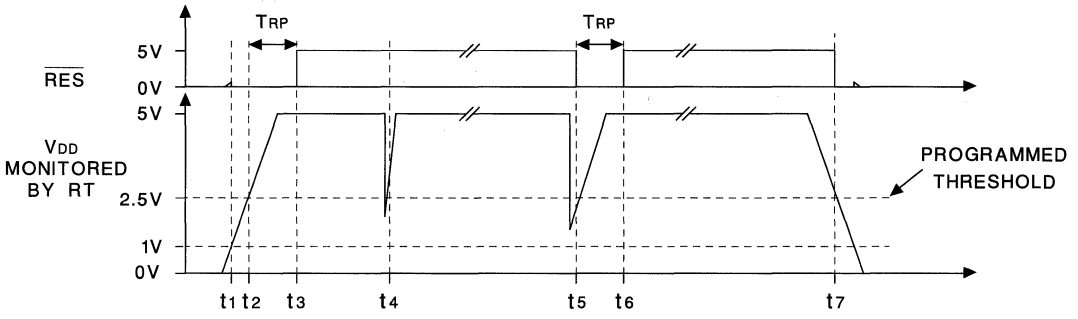


Note: Pinout represents the 8-pin TSSOP package.

UDG-98002

Figure 2. Typical Application Diagram

APPLICATION INFORMATION (cont.)



t1: V_{DD} > 1V, $\overline{RES}$ is guaranteed low.

t2: V_{DD} > programmed threshold, $\overline{RES}$ remains low for T_{RP}.

t3: T_{RP} expires, $\overline{RES}$ pulls high.

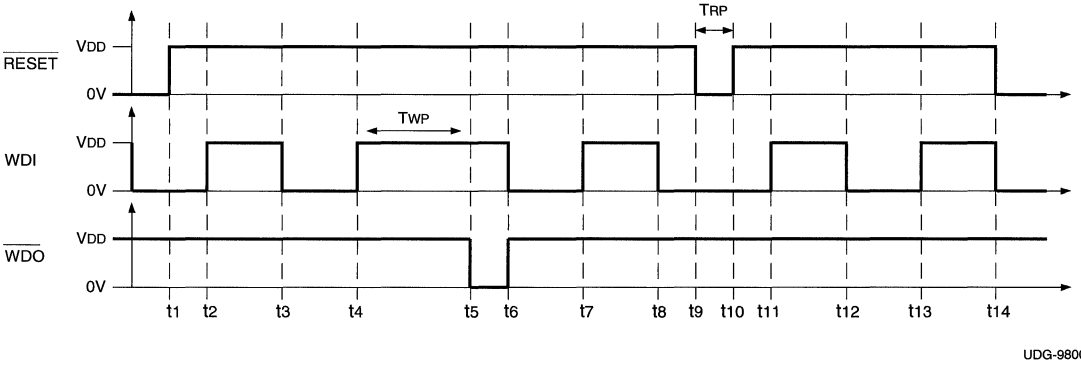
t4: Voltage glitch occurs, but is filtered at the RTH pin, $\overline{RES}$ remains high.

UDG-97067

t5: Voltage glitch occurs whose magnitude and duration is greater than the RTH filter, $\overline{RES}$ is asserted for T_{RP}.

t6: V_{DD} dips below threshold (minus hysteresis), $\overline{RES}$ is asserted.

Figure 3. Reset Circuit Timings



UDG-98007

t1: Microprocessor is reset.

t2: WDI is toggled some time after reset, but before T_{WP} expires.

t3: WDI is toggled before T_{WP} expires.

t4: WDI is toggled before T_{WP} expires.

t5: WDI is not toggled before T_{WP} expires and $\overline{WDO}$ asserts low, triggering the microprocessor to enter an error recovery routine.

t6: The microprocessor's error recovery routine is executed and WDI is toggled, reinitiating the watchdog timer.

t7: WDI is toggled before T_{WP} expires.

t8: WDI is toggled before T_{WP} expires.

t9: $\overline{RES}$ is momentarily triggered, $\overline{RES}$ is asserted low for T_{RP}.

t10: Microprocessor is reset, $\overline{RES}$ pulls high.

t11: WDI is toggled some time after reset, but before T_{WP} expires.

t12: WDI is toggled before T_{WP} expires.

t13: WDI is toggled before T_{WP} expires.

T14: V_{DD} dips below the reset threshold, $\overline{RES}$ is asserted.

Figure 4. Watchdog Circuit Timings

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Single Cell Lithium-Ion to +3.3V Converter

FEATURES

- Converts Lithium-Ion Cell to +3.3V at 700mA Load Current
- Load Disconnect in Shutdown
- High Efficiency Flyback Operation
- Internal 0.15Ω Switch
- Low Battery LED Driver
- Internal 2A Current Limit
- Internal 200kHz Oscillator
- 8 Pin D, N, 14 Pin PW Packages

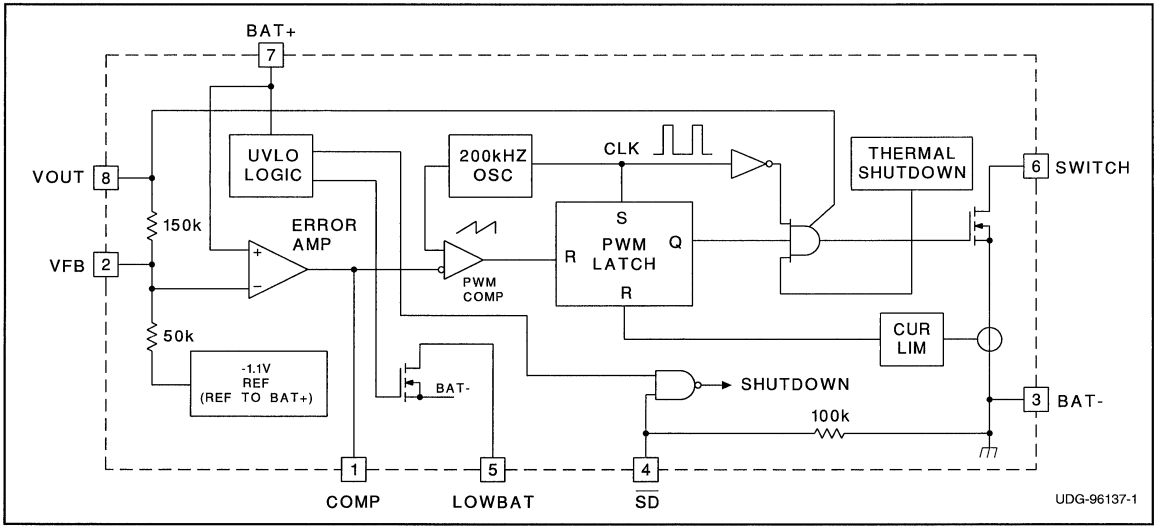
DESCRIPTION

The UCC3954, along with a few external components, develops a regulated +3.3V from a single lithium-ion battery whose terminal voltage can vary between 2.5V and 4.2V. The UCC3954 employs a simple flyback (Buck-Boost) technique to convert the battery energy to +3.3V. This is accomplished by referencing the lithium-ion cell's positive terminal to system ground. The negative terminal of the battery is the return point for the UCC3954. This approach enables the converter to maintain constant frequency operation whether the cell voltage is above or below the output voltage. An additional benefit of this technique is its inherent ability to disconnect the battery from the load in shutdown mode.

The UCC3954 operates as a fixed 200kHz switching frequency voltage mode flyback converter. The oscillator time base and ramp are internally generated by the UCC3954 and require no external components. A 2A current limit for the internal 0.15Ω power switch provides protection in the case of an output short circuit. When left open, an internal 100kΩ resistor pulls the $\overline{SD}$ pin to BAT–, which puts the UCC3954 in shutdown mode, and thereby reduces power consumption to sub-μA levels. A low battery detect function will drive the LOWBAT pin low (minimum of 5mA sink current) when the battery has been discharged to within 200mV of the predefined lockout voltage. The LOWBAT pin is intended for use with an external LED to provide visual warning that the battery is nearly exhausted. The lockout mode is activated when the battery is discharged to 2.55V. In lockout mode, the part consumes 15μA. Once the UCC3954 has entered lockout mode, the user must insert a fresh battery whose open circuit voltage is greater than 3.1V. This prevents a system-level oscillation of the lockout function due to the lithium-ion battery's large equivalent series resistance.

Additional features of the UCC3954 include a trimmed –1.1V reference and internal feedback scaling resistors, a precision error amplifier, low quiescent current drain in shutdown mode, and a softstart function. The UCC3954 is offered in the 8 pin D, 14 pin PW (surface mount), and N (through hole) packages.

BLOCK DIAGRAM



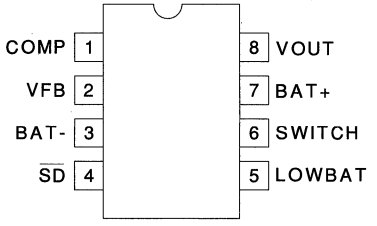
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (BAT+ to BAT–) 4.5V
VOUT
  Maximum Forced Voltage (ref. to BAT+) 5.5V
SWITCH
  Maximum Forced Voltage (ref. to BAT–) 10.2V
  Maximum Forced Current. . . . . Internally Limited
$\overline{SD}$
  Maximum Forced Voltage (ref. to BAT+) 5.5V
  Maximum Forced Current. 10mA
COMP
  Maximum Forced Voltage (ref. to BAT–) 4.5V
  Maximum Forced Current. . . . . Self Limiting
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature. . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

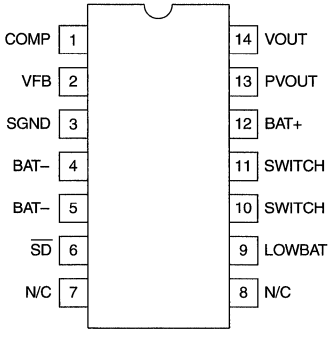
Unless otherwise indicated, voltages are reference to BAT– and currents are positive into, negative out of the specified terminal. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500µs. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-8, SOIC-8 (Top View)
D Package, N Package



SOIC-14 (Top View)
PW Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = –20°C to 70°C for the UCC3954, $\overline{SD}$ = V_{BAT+} = 3.5V (ref. to V_{BAT-}), VOUT = 3.3 (ref. to V_{BAT+}). $T_A = T_J$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
Supply Current (total) – active	$I_{BAT+} + I_{VOUT}$		1	2	mA
Supply Current (BAT+)– Shutdown	V_{SDB} = 0V (reference to BAT–)		0.2	5	µA
Supply Current (BAT+) –UVLO			30	40	µA
BAT+ Turn On Threshold	With Respect to BAT+ Turnoff	250	300	375	mV
BAT+ Turn Off Threshold		2.35	2.55	2.75	V
Low BAT+ Indicate Threshold	With Respect to BAT+ Turnoff	50	100	325	mV
Error Amplifier					
Output Voltage High	Maximum Duty Cycle, I_{OH} = 1ma	2.0	2.4		V
Output Voltage Low	Minimum Duty Cycle, I_{OL} = 1ma	0	0.14	0.5	V
VOUT Regulation Voltage	T_A = 25°C	3.22	3.3	3.38	V
		3.20	3.3	3.39	V

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = –20°C to 70°C for the UCC3954, $\overline{SD}$ = V_{BAT+} = 3.5V (ref. to V_{BAT-}), VOUT = 3.3 (ref. to V_{BAT+}). $T_A = T_J$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator/PWM					
Intital Accurancy	T_A = 25°C	180	200	220	kHz
		175	200	225	kHz
PWM Modulator Gain	V_{COMP} = 1.6V to 2V	40	50	60	%/V
PWM Maximum Duty Cycle		65	75	85	%
PWM Minimum Duty Cycle			3	5	%
Shutdown					
Disable Threshold	Reference to BAT–	0.8	1.5	2.5	V
Lowbat					
On Resistance	V_{LOWBAT} = 1V	40	100	220	Ω
Soft Start					
Rise TIme	Note 2, R_{LOAD} = 33Ω, C_{COMP} = 39nF, C_{LOAD} = 330µF		10		msec
Output Switch					
Saturation Voltage	I_{SWITCH} = 200mA		30	70	mV
Overcurrent Threshold	Note 2	2.0	3.0	3.5	Amps

Note 1: V_{BAT+} <2V to reset.

Note 2: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

BAT+: Logic supply voltage for the UCC3954. Connect to the positive terminal of the lithium-ion battery and system ground. Bypass with a low ESR, ESL capacitor if located more than 1 inch from the battery positive terminal. This is also the return for the +3.3V load

BAT–: Return for the UCC3954. Switch current flows through this pin to the negative terminal of the battery. Proper board layout precautions should be taken to minimize trace length in this path.

COMP: Output of the voltage error amplifier. Loop compensation component C_{COMP} is connected between COMP and VFB.

LOWBAT: An open drain output that will pull low and sink 10mA (typ) to drive an external LED if the battery voltage falls below the low BAT+ warning threshold. Note that this output pulls low to BAT–.

PVOUT: (PW Package only) This is the bootstrap input for the internal FET drive. It should be tied to the 3.3V output along with V_{OUT}.

$\overline{SD}$: Shutdown input for the UCC3954. An internal 100kΩ resistor pulls $\overline{SD}$ to BAT– when the circuit is left open. Pulling $\overline{SD}$ up to system ground (BAT+) or to V_{OUT}, starts the UCC3954. The UCC3954 enters a lockout mode when a dead battery is detected (<2.55V). Until a fresh battery is inserted (>3.1V), the part will remain in the low current lockout state.

SGND: (PW Package only) This is a separate signal ground pin which should be externally tied to BAT–.

SWITCH: Drain terminal of the internal 0.15Ω power switch. The current into this pin is internally limited.

VFB: This is the virtual ground of the error amplifier. Nominally at the same voltage as BAT+, the pin is provided for external compensation by means of a single capacitor to form a simple dominant pole.

VOUT: Regulated 3.3V supply feedback to the UCC3954.

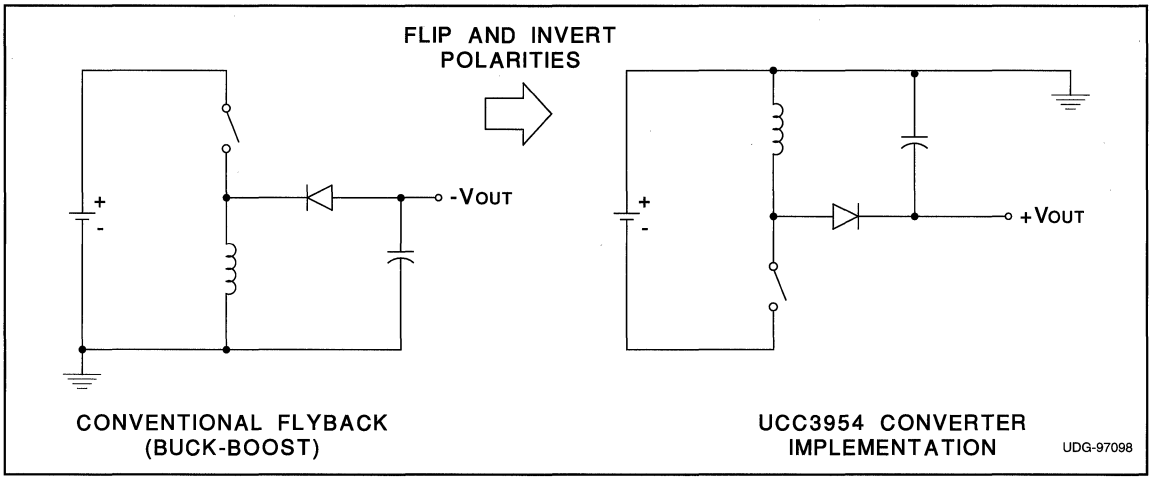


Figure 1. Simplified Circuit Diagram

APPLICATION INFORMATION

Circuit Topology

The UCC3954 uses a fixed frequency (200KHz), voltage mode PWM flyback topology. It can operate from a battery input voltage that is above or below the output voltage by referencing the battery's (+) terminal to the output (system) ground and the battery's (–) terminal to the IC's "ground" pin. It is typically operated in the continuous conduction mode (CCM), except at light loads to reduce losses due to high peak inductor current. The simplified diagram in Figure 1 helps to visualize the circuit topology. Figure 2 illustrates the current waveforms in the major circuit elements.

Only a few external components are required to develop a regulated 3.3V output from a single Lithium-Ion cell. A low ESR (Equivalent Series Resistance) and ESL (Equivalent Series Inductance) decoupling capacitor should be placed as close as possible to BAT+ and BAT–. This is especially important when operating at low battery voltages, where the peak current could cause excessive input ripple, causing the input voltage to drop below the UCC3954's shutdown threshold. The other parts required are a compensation capacitor, inductor, Schottky diode and output filter capacitor. The output filter capacitor should also be a good low ESR/ESL capacitor.

Choosing an Inductor

The inductor value selected, for a given input voltage and load current, will determine if the converter is operating in the continuous or the discontinuous conduction mode. In general, the efficiency will be higher in the continuous mode (larger inductor value), due to the lower peak currents. This also reduces the demands on the output filter capacitor and lowers output ripple voltage. However, a larger inductor value will also be physically larger for the same current rating, and reduces loop bandwidth, making it more difficult to compensate. For the input voltage range and fixed operating frequency of the UCC3954, an inductor value of around 33µH is a good compromise. See Table 1 for values and part numbers of inductors for specific ranges of load current.

Remember that the inductor must be able to maintain most of its inductance at the peak switching current.

Output Capacitor Selection

To minimize output voltage ripple, a good high frequency capacitor(s) must be used. Low ESR tantalums or Sanyo

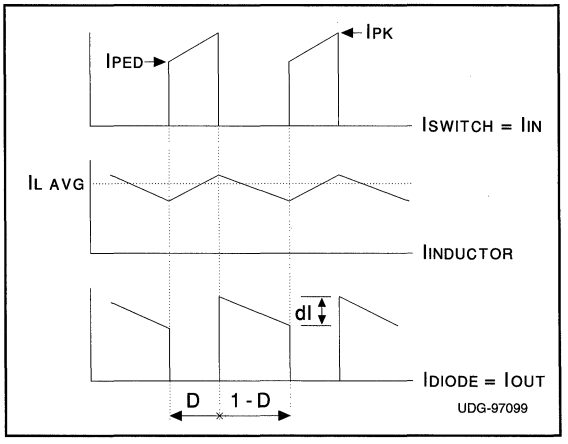


Figure 2. Current Waveforms

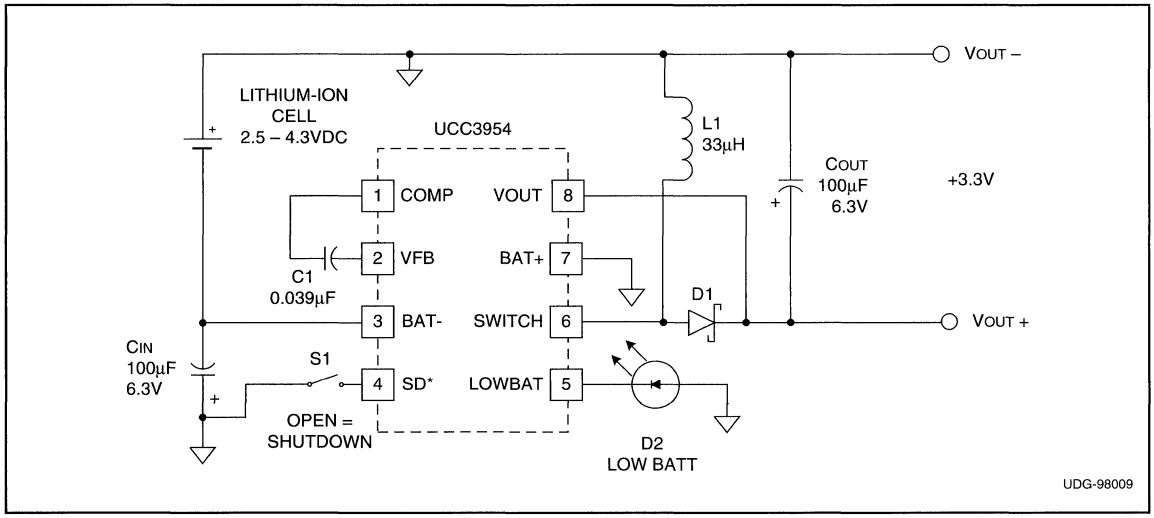


Figure 3. Application Circuit Using Dominant Pole Compensation. Typical Values are Shown.

APPLICATION INFORMATION (cont.)

OSCON's are recommended. Surface mounting will eliminate the lead inductance. Suggested values and part numbers for C_{OUT} at different load currents are given in Table 1.

Compensation Capacitor

For applications where the load is fairly constant, the loop may be compensated with a single capacitor between COMP and VFB. The value shown in the Application Circuit of Figure 3 provides good stability margin over a wide range of load, using the values shown for L1 and C_{OUT}.

Lead-Lag Compensation for Dynamic Loads

When large dynamic load transients are expected, the simple dominant pole compensation method may not provide adequate dynamic load regulation. In this case, lead-lag compensation is recommended, as shown in the application circuit of Figure 4. The addition of R1 and C1 in the error amp feedback loop provides significantly wider loop bandwidth, resulting in improved transient response. The optimum values of these compensation components will depend on a number of factors; including input voltage, load current, inductor value and output capacitance, as well as the ESR of the inductor and output capacitor. The compensation values shown in Figure 4 will provide good loop stability and good transient response over the full range of input voltage and output load. They were chosen assuming a nominal inductor value of 33µH.

Power Stage Component Selection

Recommended values and part numbers are given in Table 1 for C_{IN}, C_{OUT}, L1 and D1 for two ranges of load current. The ranges were selected based on the current ratings for two common surface mount inductor sizes.

Load Current	CIN	COUT	L1	D1
IOUT < 200mA	47µF, 6.3V AVX TPSC476M006R0350	100µF, 6.3V AVX TPSC107M06R0150	33µH Coilcraft DO1608C-333	0.5A, 20V Schottky Motorola MBR0520LT1
IOUT > 200mA	100µF, 10V AVX TPSD107M010R0100	330µF, 6.3V AVX TPSE337M006R0100	33µH Coilcraft DO3316P-333 Coiltronics CTX33-4	1A, 30V Schottky Motorola MBRS130LT3

Table 1. Power Stage Component Selection Guide

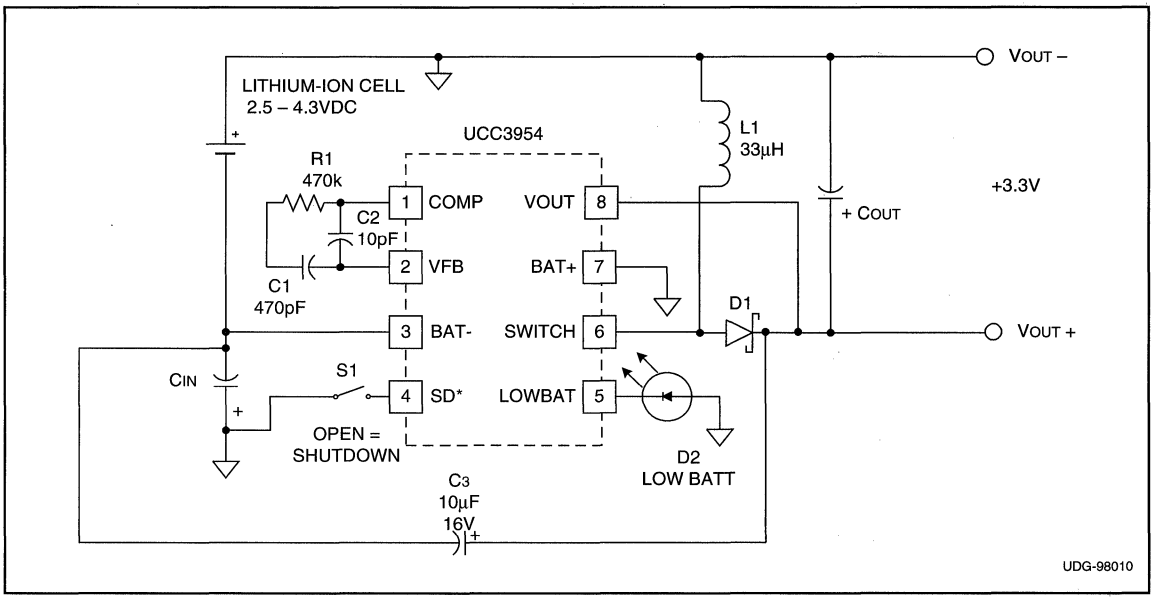


Figure 4. Application Circuit Showing Lead-Lag Compensation and Additional Cap to Reduce Output Ripple Using Cancellation Technique.

See Table 1 for Suggested Component Values and Part Numbers

Reducing Output Ripple for Noise Sensitive Applications

In some applications it may be necessary to have very low output voltage ripple. There are a number of ways to achieve this goal. Since the ripple is dominated by the ESR of the output filter capacitor, one way to reduce the ripple is to put multiple low ESR capacitors in parallel. However, this brute force method can be expensive and take up excessive board real estate.

A more effective method of ripple reduction is shown in Figure 4. By adding a small tantalum capacitor (C3) between the 3.3V output and the negative battery input (BAT–), both input and output voltage ripple are reduced. This technique is a kind of ripple current cancellation scheme, since the ripple voltage on these two nodes is 180° out of phase. Using this method, output ripple can be reduced by up to 50%. As with the other filter capacitors, it is imperative that stray inductance and resistance in series with the capacitor be minimized for maximum effectiveness. Note that this capacitor sees the sum of the input and output voltages; therefore an absolute minimum voltage rating of 10V is required.

For applications where extremely low output ripple is required, a small LC filter is recommended. This is shown in Figure 5. The addition of a small inductor and filter capacitor will reduce the ripple well below what could be achieved with capacitors alone. It is also very effective in eliminating any high frequency noise spikes resulting from the main output capacitor's ESL and the Schottky diode's parasitic capacitance. The LC values shown will provide significant ripple reduction while having a negligible effect on output regulation. Note that the corner frequency of 41kHz was chosen to be well below the 200kHz switching frequency, but high enough to avoid the loop crossover frequency, which is typically below 10kHz. This avoids loop stability issues in case the feedback is taken from the output of the LC filter. By leaving the feedback (VOUT) connection point before the LC filter, the filter cap value can be increased to achieve even higher ripple attenuation without affecting stability margin.

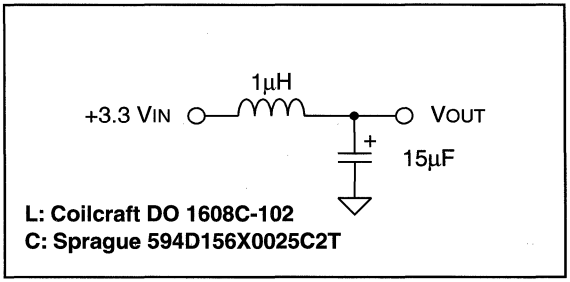


Figure 5. LC Filter for Very Low Noise Applications

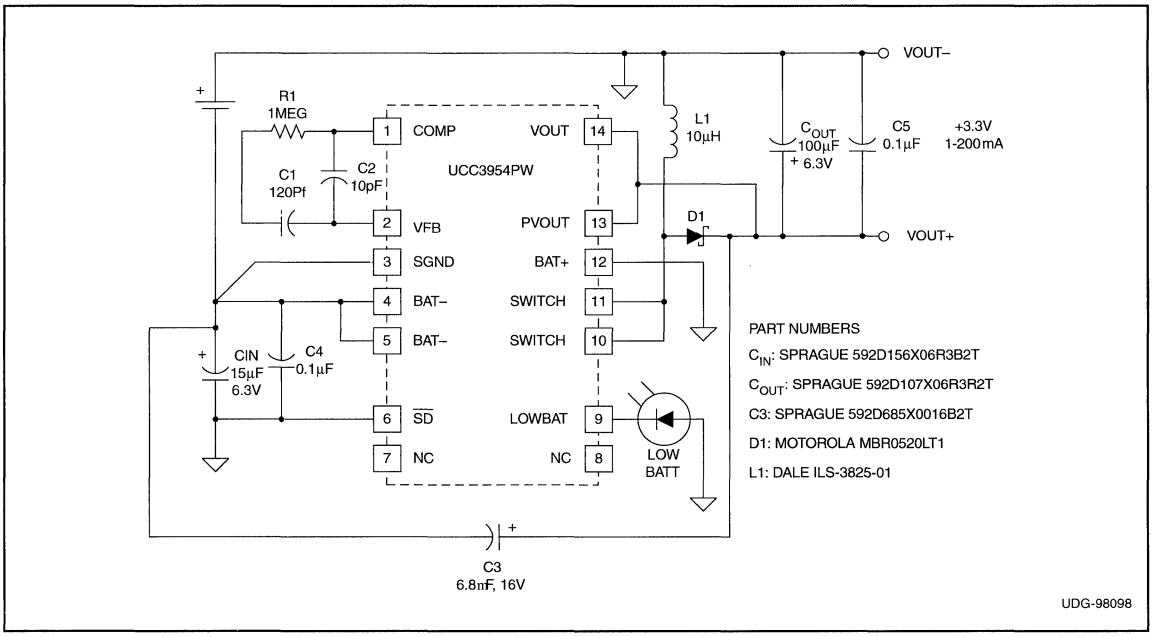


Figure 6. Application Circuit Using the 14 Pin TSSOP Package and Other Low Profile Components to Achieve 1.2mm Overall Maximum Height.*

**The maximum height on D1 is 1.35mm.*

Very Low Profile Applications

The UCC3954 is available in a low profile (1.2mm) 14 pin TSSOP package. The application circuit shown in Figure 6 is an example of a complete 200mA, 3.3V converter which will fit within a 1.2mm max height envelope*. Note that the low inductor value for L1 (10µH) requires a minimum load of at least 1mA to guarantee output regulation.

Minimum Load

Note that the pulse width modulator within the UCC3954 cannot go to zero percent duty cycle. Therefore, it stores a finite amount of energy in L1 every switching cycle. Normally, this would prevent regulation under no-load conditions. However, for inductor values greater than 15µH, no minimum load is required to maintain output regulation. This is because the current drawn by the VOUT pin, used for feedback and to bootstrap the internal MOSFET's gate drive, satisfies the minimum load requirement. However, the higher peak current resulting from inductor values below 15µH requires a small minimum load to maintain output regulation. These lower value inductors are not optimal, and will not be as efficient due to the higher peak currents, but may be necessary to reduce size in some applications, such as that of Figure 6.

Low Battery Warn Output

The UCC3954 includes an open drain Low Battery Warn output that turns on and pulls the LOWBAT pin down to BAT– when the battery input voltage drops to the Low Bat threshold. This indicates that the battery voltage is very low and approaching the UCC3954 turn off threshold.

The LOWBAT output switch is designed to have a high on-resistance, so an LED can be driven directly if desired, with no current limiting resistor. The anode of the LED can be connected to system ground (BAT+) or to the +3.3V output (this will result in a higher LED current).

For systems where it is desired to read the LOWBAT output as a digital signal referenced to the +3.3V ground, a level shifter is needed. The circuit shown in Figure 7 is a simple resistive level shifter, consisting of R1 and R2, which provides a +3.3V compatible output. The output will normally be pulled up to +3.3V until a low battery condition exists, at which point it will be about 0.3V above the 3.3V ground. Figure 8 shows the typical converter efficiency for different loads as a function of input voltage.

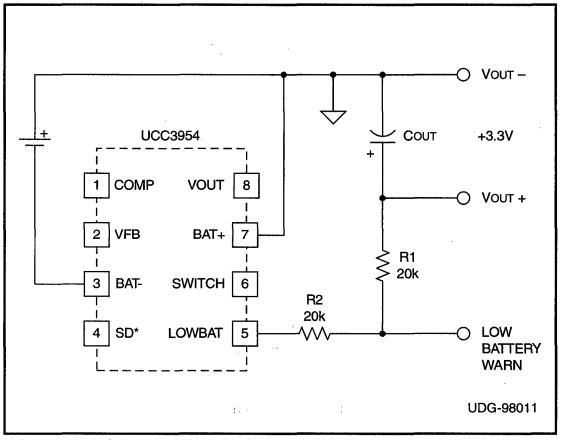


Figure 7. Simple Resistive Level Shifter for the Low Battery Warn Output

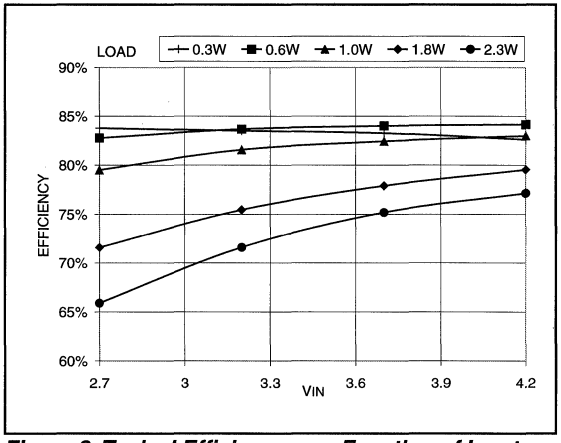


Figure 8. Typical Efficiency as a Function of Input Voltage and Load

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UCC3941 One Volt Boost Converter Demonstration Kit - Schematic and List of Materials

The UCC3941-3/-5/-ADJ Demonstration Kit allows the designer to evaluate the performance of the UCC3941-3/-5/-ADJ One Volt Boost Converter in a typical application circuit. Figure 1 shows a schematic for the UCC3941-3/-5/-ADJ Demonstration Kit. The UCC3941control chip is available in three output voltage configurations (VOUT = 3.3V, 5V, or adjustable). The kit can be populated to evaluate any of these three versions.

For the fixed output voltages, R1 is not populated and R2 is a 0Ω jumper, connecting pin 6 to ground. With the adjustable version, pin 6 is connected to the inverting input of a comparator whose non-inverting input is internally connected to 1.25V. R1 and R2 are used to program the output voltage, where

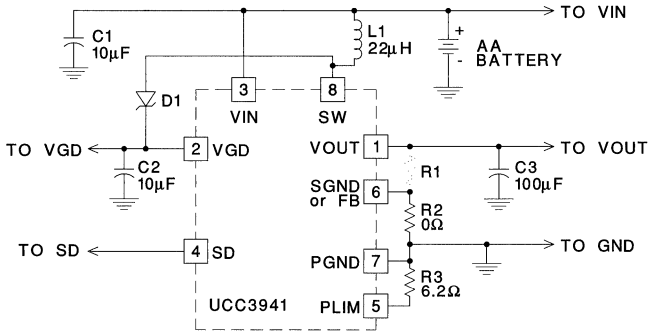
$$VOUT = 1.25 \bullet \left(1 + \frac{R1}{R2}\right)$$

SD needs to be grounded, or set to a logic level low, in order for the chip to operate. If SD is floating, or set to a logic level high, the UCC3941 enters a low power shutdown state. R3 sets the power limit of the device (see the UCC3941-3/-5/-ADJ Data Sheet). A value of 6.2Ω will limit the output power to 500mW.

Table 1 contains a parts list for the demonstration kit (fixed output versions). Reference designators are printed on the circuit board next to the associated components.

Alternate components can be substituted, however a few words of caution are in order.

High quality low ESL, low ESR, capacitors should be used in order to keep the output ripple voltage low and minimize noise that could effect circuit performance. Sprauge 594D/595D series, AVX TPS series, or Sanyo OS-CON series are good choices.



Note: Part values for 3.3V or 5V versions.

UDG-97112

Figure 1. Demonstration Kit Schematic

A 22µH inductor is recommended for most applications. An inductor value of less than 10µH should not be used since the rise and fall times will begin to approach internal timing limits of the IC. Larger values of inductors will typically result in larger ripple voltages on the outputs, due to the residual energy stored in the inductor. (Note: Data Sheet equations for the power limit and peak current assume a 22µH inductor). Inductors exist as standard part numbers from vendors such as Coilcraft, Coiltronics and Sumida.

A zener diode is used for D1 in order to guarantee that VGD does not rise above 10V during unloaded conditions.

For further information, contact a local Unitrode Representative or Field Applications Engineer at (603) 424-2410.

Reference Designator	Part Description	Part Value	Part Manufacturer	Part Number
C1	Tantalum Capacitor	10µF, 16V	Sprague	595D106X0016B2T
C2	Tantalum Capacitor	10µF, 16V	Sprague	595D106X0016B2T
C3	Tantalum Capacitor	100µF, 6.3V	Sprague	595D107X06R3C2T
D1	Zener Diode	10V	Motorola	1SMB5925BT3
L1	Inductor	22µH	Coilcraft	DT3316P-223
R1	Not Populated			
R2	Jumper	0Ω	Panasonic	ERJ-3GSY0R00

Table 1. Demonstration Kit Parts List

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Design Note

UCC3954 Single Cell Lithium-Ion to +3.3V Converter Evaluation Board, Schematic, and List of Materials

The UCC3954 evaluation kit allows the designer to evaluate the performance of the UCC3954 Single Cell Lithium-Ion to +3.3V converter. The UCC3954, along with a few external components, develops a regulated +3.3V from a single lithium-ion battery whose terminal voltage can vary between 2.5V and 4.2V. The UCC3954 employs a simple flyback (buck-boost) technique to convert the battery voltage to +3.3V. This is accomplished by referencing the battery's positive terminal to system ground. The schematic for the evaluation kit is shown in Figure 1.

UCC3954 Features

- Converts +3.3V @ 700mA Load Current
- Load Disconnect in Shutdown
- High Efficiency Flyback Operation
- Internal 0.15Ω MOSFET Switch
- Low Battery LED Driver
- Internal 2.5A Peak Current Limit
- Internal 200kHz Oscillator

Absolute Maximum Ratings

Input Supply Voltage (BAT+ to BAT-). 4.5V
OUT:
  Maximum Forced Voltage
  (ref. to BAT+) 5.5V
SWITCH:
  Maximum Forced Voltage
  (ref. to BAT+) 10.2V
  Maximum Forced Current . . . internally limited
SD
  Maximum Forced Voltage
  (ref. to BAT+) 5.5V
  Maximum Forced Current 10mA
COMP
  Maximum Forced Current. . . . . self limiting
  Maximum Forced Voltage
  (ref. to BAT+) 4.5V

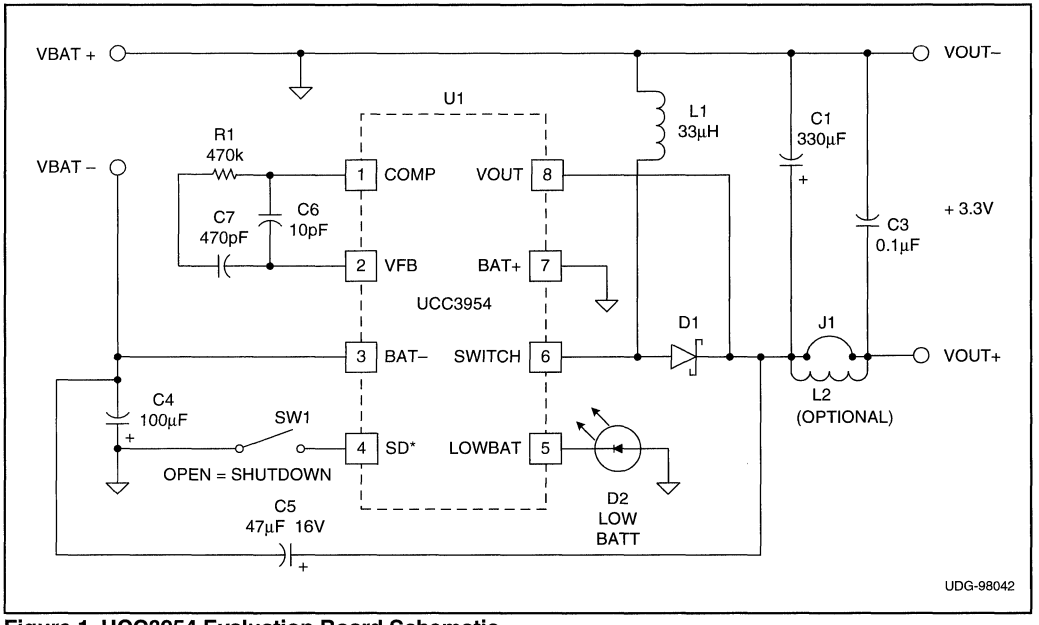

Figure 1. UCC3954 Evaluation Board Schematic

5/98

Function of SW1

SW1 provides the shutdown for the UCC3954 evaluation board. Pulling SD to BAT+ (On position) will enable the IC. An internal 100k pulldown to BAT– disables the IC when SD is left open (Off position). ***Note**: the switch positions for SW1 are reversed.*

Function of J1

J1 allows the user to evaluate additional output filtering for applications requiring even lower ripple and noise. J1 must be inserted if no additional filtering is added.

Function Of LED

The LED provides a low battery warning. The LED is illuminated by the LOWBAT output pulling low when the input battery voltage drops below the low battery warning threshold, 2.7V typical. Note: The LOWBAT output is referenced to BAT–.

Optional Components

The UCC3954 evaluation kit provides additional footprints for optional L-C output filtering. The inductor footprint (L2) is sized to accept Coilcraft D01608C size inductors. The 0.1μF Capacitor (C3) can be replaced with a small (case B) tantalum capacitor.

Choosing an Inductor (L1)

The input inductor value will determine if the converter is operating in the continuous or discontinuous conduction mode for a given input voltage and load current. The efficiency will be higher in the continuous mode (larger inductor value), due to the lower peak currents. However, a larger inductor value will be physically larger for the same current rating, and reduces loop bandwidth, making it more difficult to compensate. The evaluation kit is equipped with a 33μH inductor.

Output Capacitor Selection (C1)

To minimize output voltage ripple, a good high frequency capacitor must be used. Low ESR tantalums or *Sanyo Oscon's* are recommended. The evaluation kit is equipped with a low ESR 330μf surface mount tantalum capacitor.

Loop Compensation

The loop may be compensated utilizing the simple dominant pole method, by placing a capacitor between VFB and COMP. The dominant pole method provides good stability over a wide range of loads at the expense of loop bandwidth and dynamic regulation.

When large dynamic load transients are expected, the simple dominant pole compensation method may not provide adequate dynamic load regulation. In this case, lead-lag compensation is recommended, as shown in the evaluation circuit of Figure 1. The addition of R1 and C7 in the error amp feedback loop provides significantly wider loop bandwidth, resulting in improved transient response. The optimum values of these compensation components will depend on a number of factors; including input voltage, load current, inductor value and output capacitance, as well as the ESR of the inductor and output capacitor. The compensation values shown in Figure 1 will provide good loop stability and good transient response over the full range of input voltage and output load. They were chosen assuming a nominal inductor value of 33μH.

Reducing Output Ripple for Noise Sensitive Applications

In some applications it may be necessary to have very low output voltage ripple. There are a number of ways to achieve this goal. Since the ripple is dominated by the ESR of the output filter capacitor, one way to reduce the ripple is to put multiple low ESR capacitors in parallel. However, this brute force method can be expensive and take up excessive board real estate.

A more effective method of ripple reduction is shown in Figure 1. By adding a small tantalum capacitor (C5) between the 3.3V output and the negative battery input (BAT–), both input and output voltage ripple are reduced. This technique is a kind of ripple current cancellation scheme, since the ripple voltage on these two nodes is 180° out of phase. Using this method, output ripple can be reduced by up to 50%. As with the other filter capacitors, it is imperative that stray inductance and resistance in series with the capacitor be minimized for maximum effectiveness. Note that this capacitor sees the sum of the input and output voltages; therefore an absolute minimum voltage rating of 10V is required. (See the Optional Components section for additional information on L-C output filtering.)

For more complete information, pin descriptions and specifications for the UCC3954 Single Cell Lithium-Ion to +3.3V Converter, please refer to the UCC3954 datasheet or contact your Unitrode Field Applications Engineer at (603) 424-2410.

Table I.
UCC3954 Evaluation Board List of Materials

Reference Designator	Description	Manufacturer	Part Number
C1	330µF, 6.3V, Low ESR Tantalum Capacitor	Sprague	593D337X06R3E2W
C2	Unused		
C3	0.1µF, X7R Ceramic Capacitor		
C4	100µF, 10V, low ESR Tantalum Capacitor	Sprague	593D107X0010D2W
C5	47µF, 16V, low ESR Tantalum Capacitor	Sprague	594D476X0016C2T
C6	10pF NPO Ceramic Capacitor		
C7	470pF NPO Ceramic Capacitor		
D1	1A, 30V Schottky Diode		
D2	LED		
J1	Jumper (location for optional 1µH choke to reduce noise)		
L1	33µH Choke	Coilcraft	DO3316P-333
R1	470k, 1/10W, 5%, MF Resistor		
U1	Single Cell Lithium-Ion to +3.3V Converter	Unitrode	UCC3954
SW1	Slide Switch		

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Design Note

UCC39411 Low Power Synchronous Boost Converter, Evaluation Kit, Schematic and List of Materials

The UCC39411/2/3 Evaluation Kit allows the designer to evaluate the performance of the UCC39411/2/3 Low power Synchronous Boost converter in a typical application circuit. The schematic for the evaluation kit is shown in Figure 1. The kit can be configured to evaluate any version of the UCC39411 family.

UCC39411/2/3 Features

- 8 pin TSSOP package
- startup guaranteed under full load conditions at VBAT ≥ 1V
- Operation down to 0.5V after startup
- Wide input voltage range: 1V to 3.2V
- 200mW output power with VBAT as low as 0.8V
- Secondary supply voltage from a single inductor
- Output fully disconnected in shutdown
- Adaptive current mode control for optimum efficiency
- Low shutdown supply current
- Built-in Reset function with programmable reset pulse width

Programming the Output Voltage

The evaluation board is shipped with the UCC39411 adjustable version programmed for 3.3V. For the UCC39411 adjustable version the output voltage is programmed by the resistor divider R1 and R2 based on the internal reference voltage of 1.25V. For the fixed output voltages (UCC39412/3) R1 and R2 should be removed and Pin 4 is used solely for shutdown purposes.

$$V_{OUT} = 1.25 \bullet \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Note that the Thevenin impedance at the Feedback pin must be > 200kΩ.

When designing with the UCC39411 IC (adjustable output), it is important to populate capacitor C5. Capacitor, C5, provides feed forward from the output to the SD/FB pin to compensate for delays caused by the high impedance requirements of the SD/FB pin and the parasitic capacitance on that

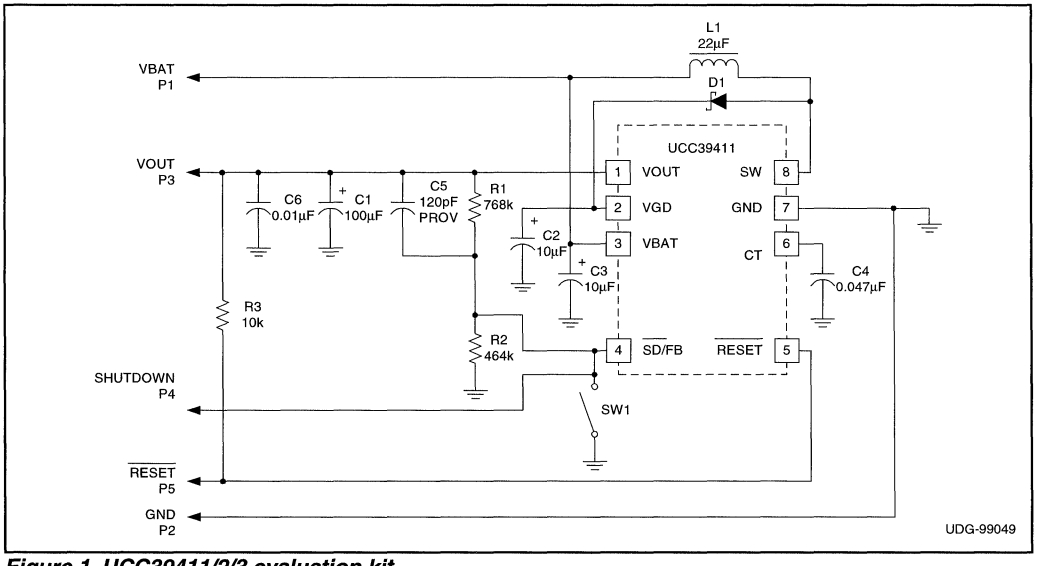

Figure 1. UCC39411/2/3 evaluation kit.

03/99

pin. Failure to populate C5 will result in excess output voltage ripple.

Shutting Down the IC

SW1 can be used to shutdown the IC and disable the output. Switching SW1 to the off position will pull the SD/FB, pin 4 to ground to shutdown the IC. Switching SW1 to the on position will allow the SD/FB pin to float thus enabling the IC.

Component Selection

Table 1 contains a parts list for the evaluation kit (fixed output version). Reference designations are provided on the circuit board next to the associated components.

Inductor Selection: An inductor value of 22µH will work best in most applications, but values between 10µH and 100µH are acceptable. Lower Value inductors typically offer lower ESR and smaller physical size. Due to the nature of hysteretic controllers, larger inductor values will typically result in larger overall voltage ripple, because once the output voltage level is satisfied the converter goes discontinuous, resulting in the residual energy of the inductor causing overshoot. It is recommended that the ESR of the inductor be less than 0.15Ω for full load operation.

Output Capacitor Selection: Once the inductor value is selected the output capacitor value will determine the output ripple voltage. The worst case peak to peak ripple voltage is due to two components, the ESR of the output capacitor, and the capacitor value. The worst case ripple occurs when the inductor is operating at maximum current and is expressed as follows:

$$\Delta V = \frac{I_{CL}^{\,2} \bullet L}{2 \bullet C \bullet (V_O - V_{BAT})} + I_{CL} \bullet ESR_{C_{OUT}} \qquad (2)$$

where,

L = Input inductance (H)

C = output capacitance (F)

ΔV = output voltage ripple (VP-P)

I_{CL} = the peak current limit (A)

V_O = output voltage (V)

V_{BAT} = input voltage (V)

The evaluation board is equipped with a 100µF Sprague Tantalum surface mount capacitor with an ESR of 100mΩ. Output voltage ripple is 20mV_{P-P} at 200mW out.

Input and VGD Capacitor Selections: The UCC39411 does not require a large decoupling capacitor on VBAT to operate properly, a 10µF capacitor is sufficient for most applications. Optimum efficiency occurs when the capacitor value is large enough to decouple the source impedance.

A 10µF capacitor on VGD should be sufficient to provide proper operation of the UCC39411 under full load conditions.

Setting the Reset Period

The $\overline{\text{RESET}}$ pin (open drain) provides an indication about the status of VOUT. If VOUT drops below 10% of its nominal value, $\overline{\text{RESET}}$, (pin 5) will go low. On power up, $\overline{\text{RESET}}$ will stay low until the output has reached 90% of its nominal value and the reset period has elapsed. The reset period is set by the capacitance placed on CT, (pin 6). The reset period is defined by:

$$T_{RESET} = CT \bullet 2.5x10^{6} \text{ seconds} \qquad (3)$$

where CT is in Farads.

The Molex Connector

In addition to the AA battery holder to which the board is mounted there is also a 5 pin Molex connector for the user to interface to if desired. The pin-out for the connector is specified in Figure 1. Pin 1 of the connector is at the top left-hand corner of the circuit board.

Table 1. UCC39411 evaluation board list of materials.

Designator	Description	Part Value	Manufacturer	Part Number
C1	Tantalum capacitor	100µF, 10V	Sprague	593D107X0010D2W
C2, C3	Tantalum capacitor	10µF, 16V	Sprague	595D106X0016B2T
C4	Ceramic capacitor, 1206, X7R	0.047µF	Panasonic/Digi-key	PCC473BCT-ND
C5	Ceramic capacitor, 0603, NPO	120pF	Digi-key	PCC121ACVCT-ND
C6	Ceramic capacitor, 0603	0.01µF	Digi-key	PCC103BVCT-ND
D1	Schottly Diode SOD-123	MBR0530T1	Newark	MBR0530T1
L1	Inductor	22µH	Coilcraft	DO1608C-223
R1	Resistor, 0603, 0.06W	768kΩ	Digi-key	P768KHCT
R2	Resistor, 0603, 0.06W	464kΩ	Digi-key	P464KHCT-ND
R3	Resistor, 0603, 0.06W	10kΩ	Digi-key	P10KHCT-ND
SW1	Switch		EAO Switch	09 10201 02
TB1	Connector, 5 pin		Molex	22-05-3051
U1	Control IC		Initrode	UCC39411
U2	Battery Holder, AA		Digi-key	BHAA-ND

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Back-Light Controllers

Back-Light Controller ICs Selection Guide

Back-Light Controllers	Part Number UC3871	UC3872	UCC3972
Application	Fluorescent lamp driver with LCD Bias	Fluorescent lamp driver	Fluorescent lamp driver
Voltage range	4.5V–20V	4.5V–24V	4.5V–25V
Reference tolerance	1.2%	1.2	NA
Open lamp detect	Yes	Yes	Yes
PWM synchronization	Yes	Yes	Yes
PWM frequency	Programmable	Programmable	80kH–160kH
Analog dimming	Yes	Yes	Yes
Low-frequency dimming	Yes	Yes	Yes
Operating current	8mA	6mA	1mA
Package	18-pin SOIC	16-pin SSOP	8-pin TSSOP
Application/design note	U-141, U-148	DN-75, U-141, U-148	-
Page number	8-2	8-8	8-13

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application INFO available

UC1871
UC2871
UC3871

Resonant Fluorescent Lamp Driver

FEATURES

- 1μA ICC when Disabled
- PWM Control for LCD Supply
- Zero Voltage Switched (ZVS) on Push-Pull Drivers
- Open Lamp Detect Circuitry
- 4.5V to 20V Operation
- Non-saturating Transformer Topology
- Smooth 100% Duty Cycle on Buck PWM and 0% to 95% on Flyback PWM

DESCRIPTION

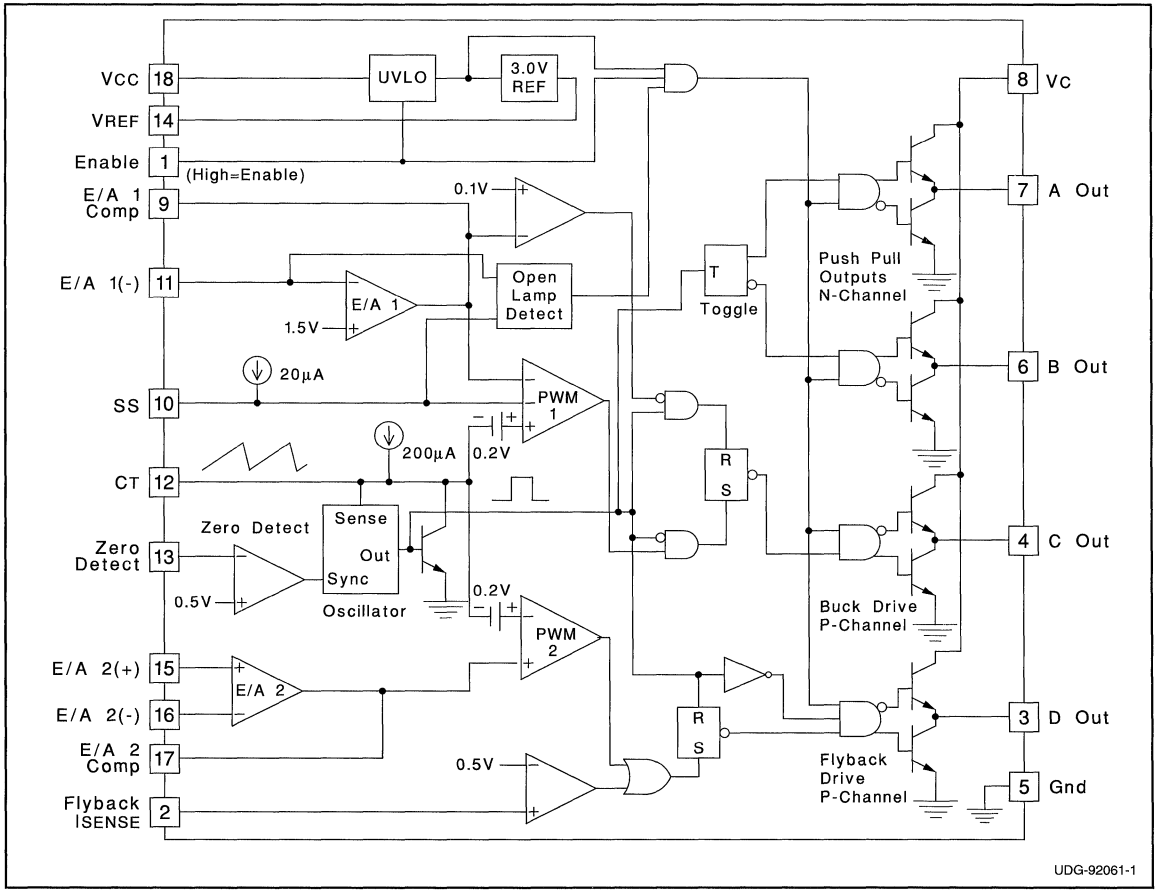
The UC1871 Family of IC's is optimized for highly efficient fluorescent lamp control. An additional PWM controller is integrated on the IC for applications requiring an additional supply, as in LCD displays. When disabled the IC draws only 1μA, providing a true disconnect feature, which is optimum for battery powered systems. The switching frequency of all outputs are synchronized to the resonant frequency of the external passive network, which provides Zero Voltage Switching on the Push-Pull drivers.

Soft-Start and open lamp detect circuitry have been incorporated to minimize component stress. An open lamp is detected on the completion of a soft-start cycle.

The Buck controller is optimized for smooth duty cycle control to 100%, while the flyback control ensures a maximum duty cycle of 95%.

Other features include a precision 1% reference, under voltage lockout, flyback current limit, and accurate minimum and maximum frequency control.

BLOCK DIAGRAM



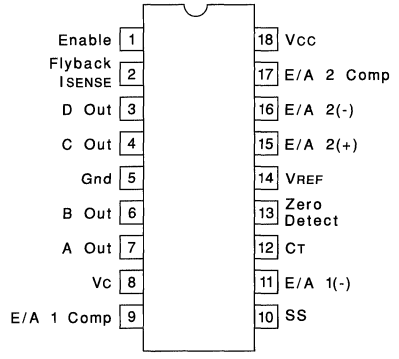
Note: Pin numbers refer to DIL-18 and SOIC-18 packages only.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs. . . . . –0.3 to +10V
Vcc, Vc Voltage . . . . . +20V
Zero Detect Input Current
High Impedance Source . . . . . +10mA
Zero Detect
Low Impedance Source . . . . . +20V
Power Dissipation at TA = 25°C 1W
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature . . . . . 300°C

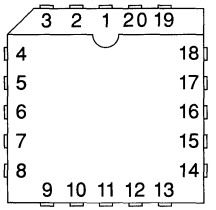
Note 1: *Currents are positive into, negative out of the specified terminal.*
Note 2: *Consult Packaging Section of Databook for thermal limitations and considerations of package.*

DIL-18, SOIC-18 (TOP VIEW)
J or N, DW Package



CONNECTION DIAGRAMS

PLCC-20 (Top View)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
Gnd	1
B Out	2
A Out	3
Vc	4
E/A 1 Comp	5
SS	6
E/A 1(-)	7
N/C	8
CT	9
Zero Detect	10
N/C	11
VREF	12
E/A 2(+)	13
E/A 2(-)	14
E/A 2 Comp	15
Vcc	16
Enable	17
Flyback ISENSE	18
D Out	19
C Out	20

ELECTRICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these parameters apply for T_A = –55°C to +125°C for the UC1871; –25°C to +85°C for the UC2871; 0°C to +70°C for the UC3871; V_{CC} = 5V, V_C = 15V, V_{ENABLE} = 5V, C_T = 1nF, Zero Det = 1V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	T_J = 25°C	2.963	3.000	3.037	V
	Overtemp	2.940	3.000	3.060	V
Line Regulation	V_{CC} = 4.75V to 18V			10	mV
Load Regulation	I_O = 0 to –5mA			10	mV
Oscillator Section					
Free Running Frequency	T_J = 25°C	57	68	78	kHz
Max Sync Frequency	T_J = 25°C	160	200	240	kHz
Charge Current	V_{CT} = 1.5V	180	200	220	µA
Voltage Stability				2	%
Temperature Stability			4	8	%
Zero Detect Threshold		0.46	0.5	0.56	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these parameters apply for T_A = –55°C to +125°C for the UC1871; –25°C to +85°C for the UC2871; 0°C to +70°C for the UC3871; V_{CC} = 5V, V_C = 15V, V_{ENABLE} = 5V, C_T = 1nF, Zero Det = 1V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Error Amp 1 Section					
Input Voltage	V_O = 2V	1.445	1.475	1.505	V
Input Bias Current			-0.4	-2	µA
Open Loop Gain	V_O = 0.5 to 3V	65	90		dB
Output High	V_{EA}(–) = 1.3V	3.1	3.5	3.9	V
Output Low	V_{EA}(–) = 1.7V		0.1	0.2	V
Output Source Current	V_{EA}(-) = 1.3V, Vo = 2V	-350	-500		µA
Output Sink Current	V_{EA}(-) = 1.7V, Vo = 2V	10	20		mA
Common Mode Range		0		V_{IN}-1V	V
Unity Gain Bandwidth	T_J = 25°C (Note 4)		1		MHz
Maximum Source Impedance	Note 5			100k	Ω
Open Lamp Detect Section					
Soft Start Threshold	V_{EA}(-) = 0V	2.9	3.4	3.8	V
Error Amp Threshold	V_{SS} = 4.2V	0.7	1.0	1.3	V
Soft Start Current	V_{SS} = 2V	10	20	40	µA
Error Amp 2 Section					
Input Offset Voltage	Vo = 2V		0	10	mV
Input Bias Current			-0.2	-1	µA
Input Offset Current				0.5	µA
Open Loop Gain	Vo = 0.5 to 3V	65	90		dB
Output High	V_{ID} = 100mV, Vo = 2V	3.6	4	4.4	V
Output Low	V_{ID} = -100mv, Vo = 2V		0.1	0.2	V
Output Source Current	V_{ID} = 100mV, Vo = 2V	-350	-500		µA
Output Sink Current	V_{ID} = -100mV, Vo = 2V	10	20		mA
Common Mode Range		0		V_{IN}-2V	V
Unity Gain Bandwidth	T_J = 25°C (Note 4)		1		MHz
Isense Section					
Threshold		0.475	0.525	0.575	V
Output Section					
Output Low Level	I_{OUT} = 0, Outputs A and B		0.05	0.2	V
	I_{OUT} = 10mA		0.1	0.4	V
	I_{OUT} = 100mA		1.5	2.2	V
Output High Level	I_{OUT} = 0, Outputs C and D	14.7	14.9		V
	I_{OUT} = -10mA	13.5	14.3		V
	I_{OUT} = -100mA	12.5	13.5		V
Rise Time	T_J = 25°C, Cl = 1nF(Note 4)		30	80	ns
Fall Time	T_J = 25°C, Cl = 1nF(Note 4)		30	80	ns
Output Dynamics					
Out A and B Duty Cycle		48	49.9	50	%
Out C Max Duty Cycle	V_{EA1}(-) = 1V	100			%
Out C Min Duty Cycle	V_{EA1}(-) = 2V			0	%
Out D Max Duty Cycle	V_{EA2}(+)- V_{EA2}(-) = 100mV		92	96	%
Out D Min Duty Cycle	V_{EA2}(+)- V_{EA2}(-) = -100mV			0	%

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these parameters apply for T_A = –55°C to +125°C for the UC1871; –25°C to +85°C for the UC2871; 0°C to +70°C for the UC3871; V_{CC} = 5V, V_C = 15V, V_{ENABLE} = 5V, C_T = 1nF, Zero Det = 1V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Under Voltage Lockout Section					
Start-Up Threshold		3.7	4.2	4.5	V
Hysterisis		120	200	280	mV
Enable Section					
Input High Threshold		2			V
Input low Threshold				0.8	V
Input Current	V_{ENABLE} = 5V		150	400	µA
Supply Current Section					
VCC Supply Current	V_{CC} = 20V		8	14	mA
VC Supply Current	V_C=20V		7	12	mA
ICC Disabled	V_{CC} = 20V, V_{ENABLE} = 0V		1	10	µA

Note 3: *Unless otherwise specified, all voltages are with respect to ground. Currents are positive into, and negative out of the specified terminal.*

Note 4: *Guaranteed by design but not 100% tested in production.*

Note 5: *Impedance below specified maximum guarantees proper operation of the Open Lamp Detect.*

APPLICATIONS INFORMATION

Figure 1 shows a complete application circuit using the UC3871 Resonant Fluorescent lamp and LCD driver. The IC provides all drive, control and housekeeping functions to implement CCFL and LCD converters. The buck output voltage (transformer center-tap) provides the zero crossing and synchronization signal. The LCD supply modulator is also synchronized to the resonant tank.

The buck modulator drives a P-channel MOSFET directly, and operates over a 0-100% duty-cycle range. The modulation range includes 100%, allowing operation with minimal headroom. The LCD supply modulator also directly drives a P-channel MOSFET, but it's duty-cycle is limited to 95% to prevent flyback supply foldback.

The oscillator and synchronization circuitry are shown in Figure 2. The oscillator is designed to synchronize over a 3:1 frequency range. In an actual application however, the frequency range is only about 1.5:1. A zero detect comparator senses the primary center-tap voltage, generating a synchronization pulse when the resonant waveform falls to zero. The actual threshold is 0.5V, providing a small amount of anticipation to offset propagation delay.

The synchronization pulse width is the time that the 4mA current sink takes to discharge the timing capacitor to 0.1V. This pulse width sets the LCD supply modulator minimum off time, and also limits the minimum linear control range of the buck modulator. The 200µA current source charges the capacitor to a maximum of 3 volts. A comparator blanks the zero detect signal until the capacitor voltage exceeds 1V, preventing multiple synchronization pulse generation and setting the maximum frequency. If the capacitor voltage reaches 3V (a zero detection has not occurred) an internal clock pulse is generated to limit the minimum frequency.

A unique protection feature incorporated in the UC3871 is the Open Lamp Detect circuit. An open lamp interrupts the current feedback loop and causes very high secondary voltage. Operation in this mode will usually breakdown the transformer's insulation, causing permanent damage to the converter. The open lamp detect circuit, shown in Figure 3 senses the lamp current feedback signal at the error amplifiers input, and shuts down the outputs if insufficient signal is present. Soft-start circuitry limits initial turn-on currents and blanks the open lamp detect signal.

Other features are included to minimize external circuitry requirements. A logic level enable pin shuts down the IC, allowing direct connection to the battery. During shutdown, the IC typically draws less than 1µA. The UC3871, operating from 4.5V to 20V, is compatible with almost all battery voltages used in portable computers. Under-voltage lockout circuitry disables operation until sufficient supply voltage is available, and a 1% voltage reference insures accurate operation. Both inputs to the LCD supply error amplifier are uncommitted, allowing positive or negative supply loop closure without additional circuitry. The LCD supply modulator also incorporates cycle-by-cycle current limiting for added protection.

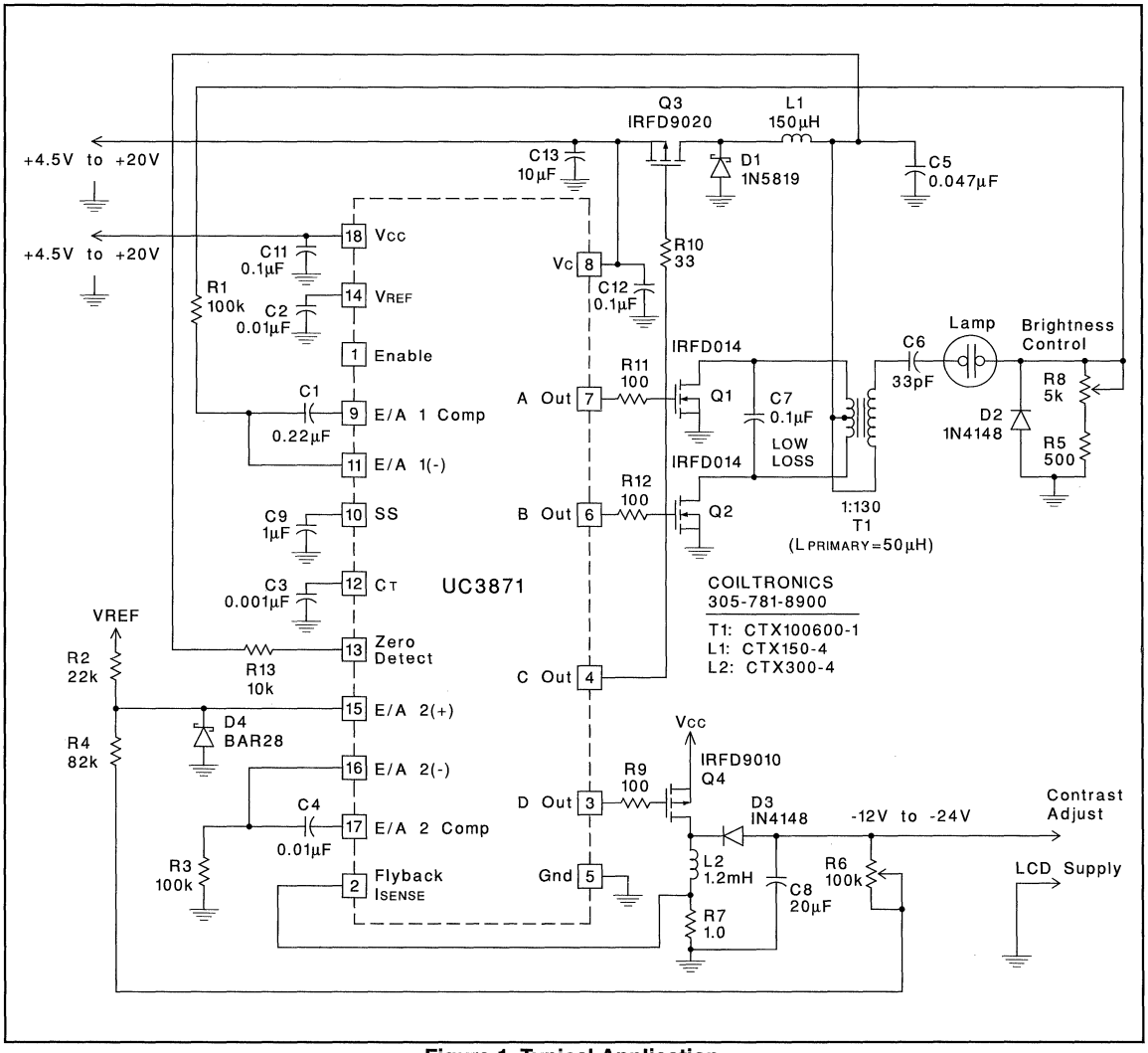


Figure 1. Typical Application.

APPLICATION INFORMATION (cont.)

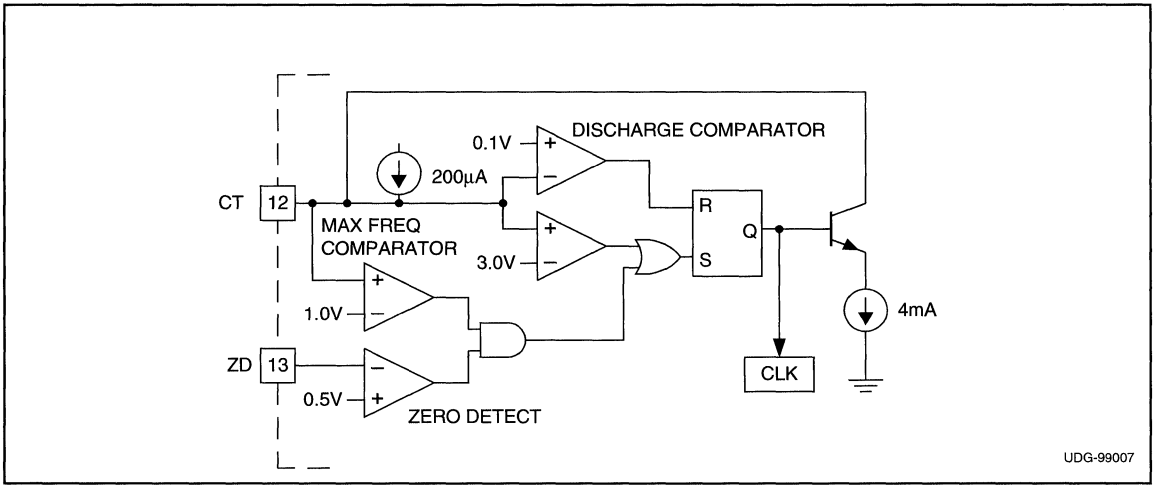


Figure 2. UC3871 Oscillator Section.

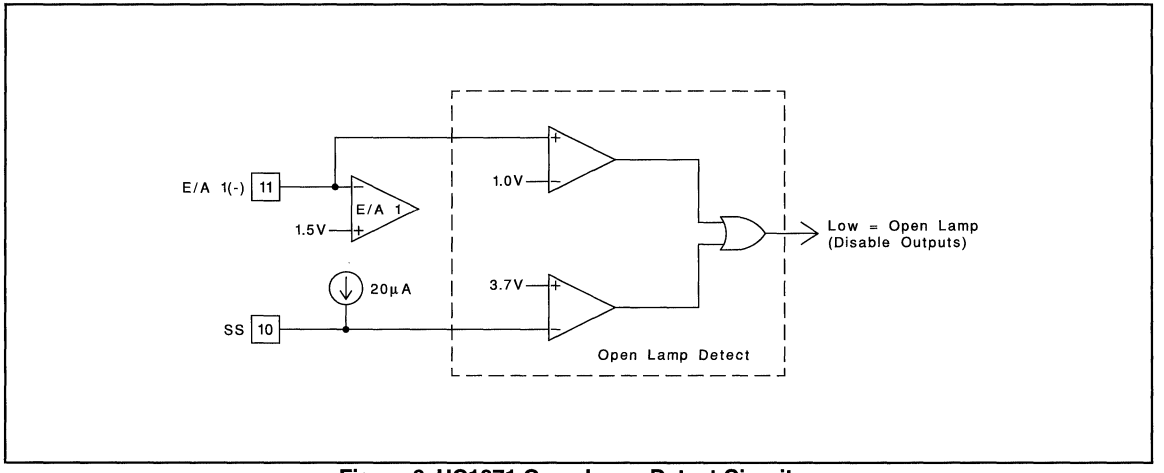


Figure 3. UC1871 Open Lamp Detect Circuitry.

UNITRODE

Resonant Lamp Ballast Controller

application INFO available

UC1872
UC2872
UC3872

FEATURES

- Controls Different Types of Lamps: Cold Cathode Fluorescent, Neon, and Gas Discharge
- Zero Voltage Switching (ZVS) of Push-Pull Drivers
- Accurate Control of Lamp Current
- Variable Lamp Intensity Control
- 1μA Disable Current
- 4.5V to 24V Operation
- Open Lamp Detection Circuitry

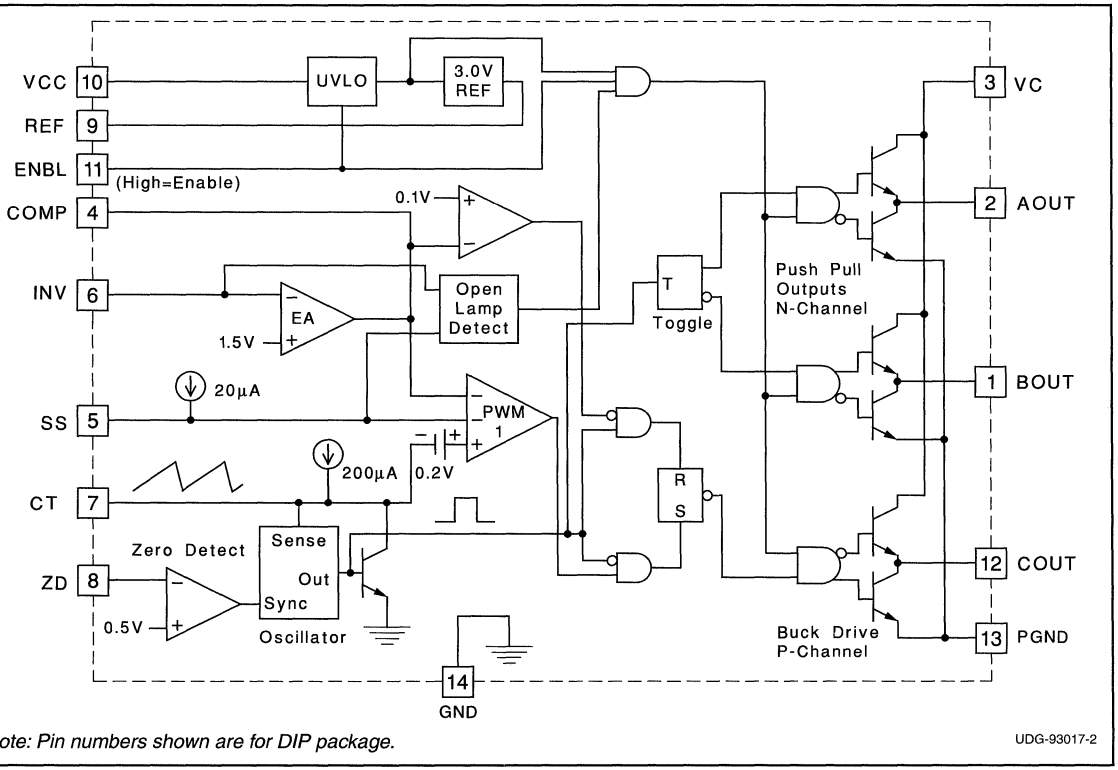
DESCRIPTION

The UC3872 is a resonant lamp ballast controller optimized for driving cold cathode fluorescent, neon, and other gas discharge lamps. The resonant power stage develops a sinusoidal lamp drive voltage, and minimizes switching loss and EMI generation. Lamp intensity adjustment is accomplished with a buck regulator, which is synchronized to the external power stage's resonant frequency. Suitable for automotive and battery powered applications, the UC3872 draws only 1μA when disabled.

Soft start and open lamp detect circuitry have been incorporated to minimize component stresses. Open lamp detection is enabled at the completion of a soft start cycle. The chip is optimized for smooth duty cycle control to 100%.

Other features include a precision 1.2% reference, undervoltage lockout, and accurate minimum and maximum frequency control.

BLOCK DIAGRAM



Note: Pin numbers shown are for DIP package.

UDG-93017-2

ABSOLUTE MAXIMUM RATINGS

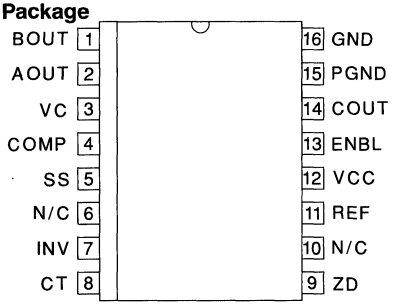
Analog Inputs. . . . . –0.3 to +10V
VCC, VC Voltage. . . . . +24V
ZD Input Current
  High Impedance Source . . . . . +10mA
ZD Input Voltage
  Low Impedance Source . . . . . +24V
Power Dissipation at T_A = 25°C 1W
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature . . . . . 300°C

Note 1: *Currents are positive into, negative out of the specified terminal.*

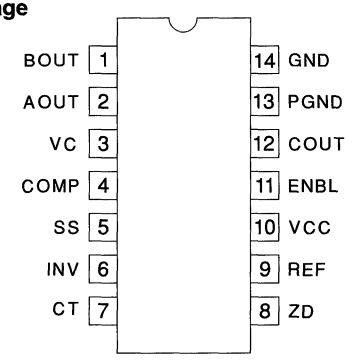
Note 2: *Consult Packaging Section of Databook for thermal limitations and considerations of package.*

CONNECTION DIAGRAMS

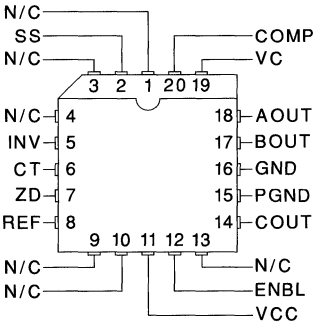
SOIC-16, SSOP-16 (TOP VIEW)
DW, M Package



DIL-14 (TOP VIEW)
N Package



PLCC-20 (Top View)
Q Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these parameters apply for T_J = –55°C to +125°C for the UC1872, –40°C to +85°C for the UC2872, –0°C to +70°C for the UC3872; VCC= 5V, VC = 15V, V_{ENBL} = 5V, CT = 1nF, ZD = 1V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	T_J = 25°C	2.963	3.000	3.037	V
	Over Temperature	2.940	3.000	3.060	V
Line Regulation	VCC = 4.75V to 18V			10	mV
Load Regulation	I_O = 0 to –5mA			10	mV
Oscillator Section					
Free Running Frequency	T_J = 25°C	57	68	78	kHz
Maximum Synchronization Frequency	T_J = 25°C	160	200	240	kHz
Charge Current	V_{CT} = 1.5V	180	200	220	µA
Voltage Stability				2	%
Temperature Stability			4	8	%
Zero Detect Threshold		0.46	0.5	0.56	V
Error Amp Section					
Input Voltage	V_O = 2V	1.445	1.475	1.505	V
Input Bias Current			–0.4	–2	µA
Open Loop Gain	V_O = 0.5 to 3V	65	90		dB
Output High	V_{INV} = 1.3V	3.1	3.5	3.9	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these parameters apply for T_J = –55°C to +125°C for the UC1872, –40°C to +85°C for the UC2872, –0°C to +70°C for the UC3872; VCC= 5V, VC = 15V, V_{ENBL} = 5V, CT = 1nF, ZD = 1V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Error Amp Section (cont.)					
Output Low	V_{INV} = 1.7V		0.1	0.2	V
Output Source Current	V_{INV} = 1.3V, V_O = 2V	–350	–500		µA
Output Sink Current	V_{INV} = 1.7V, V_O = 2V	10	20		mA
Common Mode Range		0		V_{IN}-1V	V
Unity Gain Bandwidth	T_J = 25°C (Note 4)		1		MHz
Open Lamp Detect Section					
Soft Start Threshold	V_{INV} = 0V	2.9	3.4	3.8	V
Open Lamp Detect Threshold	V_{SS} = 4.2V	0.6	1.0	1.4	V
Soft Start Current	V_{SS} = 2V	10	20	40	µA
Output Section					
Output Low Level	I_{OUT} = 0, Outputs A and B		0.05	0.2	V
	I_{OUT} = 10mA		0.1	0.4	V
	I_{OUT} = 100mA		1.5	2.2	V
Output High Level	I_{OUT} = 0, Output C	13.9	14.9		V
	I_{OUT} = –10mA	13.5	14.3		V
	I_{OUT} = –100mA	12.5	13.5		V
Rise Time	T_J = 25°C, Cl = 1nF(Note 4)		30	80	ns
Fall Time	T_J = 25°C, Cl = 1nF(Note 4)		30	80	ns
Output Dynamics					
Out A and B Duty Cycle		48	49.9	50	%
Out C Max Duty Cycle	V_{INV} = 1V	100			%
Out C Min Duty Cycle	V_{INV} = 2V			0	%
Under Voltage Lockout Section					
Startup Threshold Voltage		3.7	4.2	4.5	V
Hysteresis		120	200	280	mV
Enable Section					
Input High Threshold		2			V
Input Low Threshold				0.8	V
Input Current	V_{ENBL} = 5V		150	400	µA
Supply Current Section					
VCC Supply Current	VCC = 24V		6	14	mA
VC Supply Current	VC = 24V		5	12	mA
ICC Disabled	VCC = 24V, V_{ENBL} = 0V		1	10	µA

***Note 3**: Unless otherwise specified, all voltages are with respect to ground. Currents are positive into, and negative out of the specified terminal.*

***Note 4:** Guaranteed by design. Not 100% tested in production.*

PIN DESCRIPTIONS

AOUT, BOUT: These outputs provide complementary drive signals for the push-pull N-channel MOSFETs. Each one is high for 50% of the time, switching states each time a zero-detect is sensed.

COMP: COMP is the output terminal of the error amplifier. Compensation components are normally connected between COMP and INV. Connecting a capacitor from this pin to ground limits turn on current and blanks the open lamp detect signal allowing the lamp to start.

PIN DESCRIPTIONS (cont.)

COUT: This output directly drives the bulk regulator P-channel MOSFET. COUT turn-on is synchronized to each zero-detect, and therefore switches at twice the frequency of AOUT and BOUT. The modulator controlling COUT is designed to provide smooth control up to 100% duty cycle.

CT: A capacitor connected between this pin and GND ground sets the synchronization frequency range. The capacitor is charged with approximately 200μA, creating a linear ramp which is used by COUT's (buck regulator driver) PWM comparator.

ENBL: When ENBL is driven high the device is enabled. When ENBL is pulled low, the IC is shut down and typically draws 1μA.

GND: This pin is the ground reference point for the internal reference and all thresholds.

INV: This pin is the inverting input to the error amplifier and the input for the open lamp detect circuitry. If the voltage at INV is below the 1V open lamp detect threshold, the outputs are disabled.

PGND: This pin is the high current ground connection for the three output drivers.

REF: This pin is connected to the 3V reference voltage which is used for the internal logic. Bypass REF to ground with a 0.01μF ceramic capacitor for proper operation.

VC: VC is the power supply voltage connection for the output drivers. Bypass it to ground with a 0.1μF ceramic capacitor for proper operation.

VCC: VCC is the positive supply voltage for the chip. Its operating range is from 4.2V to 24V. Bypass VCC to ground with a 0.1μF ceramic capacitor for proper operation.

ZD: The zero-detect input senses when the transformer's primary center tap voltage falls to zero to synchronize the sawtooth voltage waveform on CT. The threshold is approximately 0.5V, providing a small amount of offset such that with propagation delay, zero-volt switching occurs. A resistor (typically 10k) should be connected between ZD and the primary center tap to limit input current at turn off.

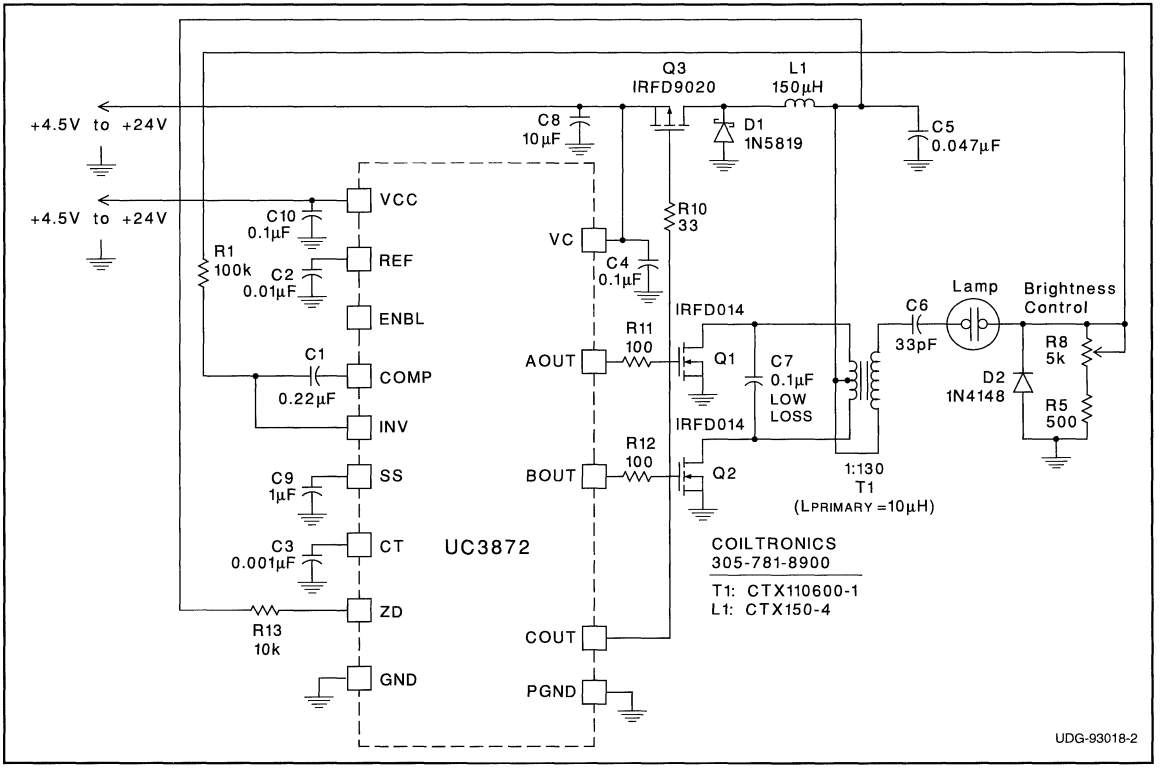


Figure 1. Typical Application

APPLICATIONS INFORMATION

Figure 1 shows a complete application circuit using the UC3872 Resonant Lamp Ballast Controller. The IC provides all drive, control and housekeeping functions. The buck output voltage (transformer center-tap) provides the zero crossing and synchronization signals.

The buck modulator drives a P-channel MOSFET directly, and operates over a 0-100% duty-cycle range. The modulation range includes 100%, allowing operation with minimal headroom.

The oscillator and synchronization circuitry are shown in Figure 2. The oscillator is designed to synchronize over a 3:1 frequency range. In an actual application however, the frequency range is only about 1.5:1. A zero detect comparator senses the primary center-tap voltage, generating a synchronization pulse when the resonant waveform falls to zero. The actual threshold is 0.5 volts, providing a small amount of anticipation to offset propagation delay.

The synchronization pulse width is the time required for the 4mA current sink to discharge the timing capacitor to 0.1 volts. This pulse width limits the minimum linear control range of the buck regulator. The 200µA current source charges the capacitor to a maximum of 3 volts. A comparator blanks the zero detect signal until the capacitor voltage exceeds 1 volt, preventing multiple synchronization pulse generation and setting the maximum frequency. If the capacitor voltage reaches 3 volts (a zero detection has not occurred) an internal clock pulse is generated to limit the minimum frequency.

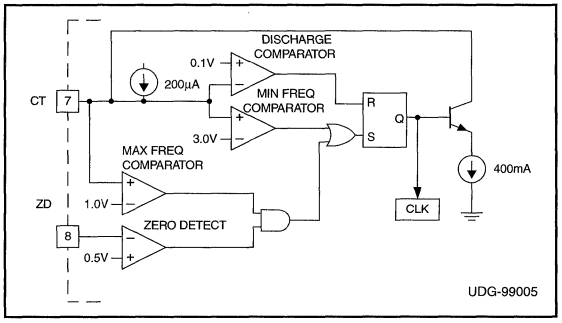


Figure 2. UC3872 Oscillator Section

A unique protection feature incorporated in the UC3872 is the Open Lamp Detect circuit. An open lamp interrupts the current feedback loop and causes very high secondary voltage. Operation in this mode will usually breakdown the transformer's insulation, causing permanent damage to the converter. The open lamp detect circuit, shown in Figure 3 senses the lamp current feedback signal at the error amplifier's input, and shuts down the outputs if insufficient signal is present. Soft start circuitry limits initial turn-on currents and blanks the open lamp detect signal.

Other features are included to minimize external circuitry requirements. A logic level enable pin shuts down the IC, allowing direct connection to a battery. During shutdown, the IC typically draws less than 1µA. The UC3872, operating from 4.5V to 24V, is compatible with almost all battery voltages used in portable computers and automotive applications. Undervoltage lockout circuitry disables operation until sufficient supply voltage is available, and a 1% voltage reference insures accurate operation.

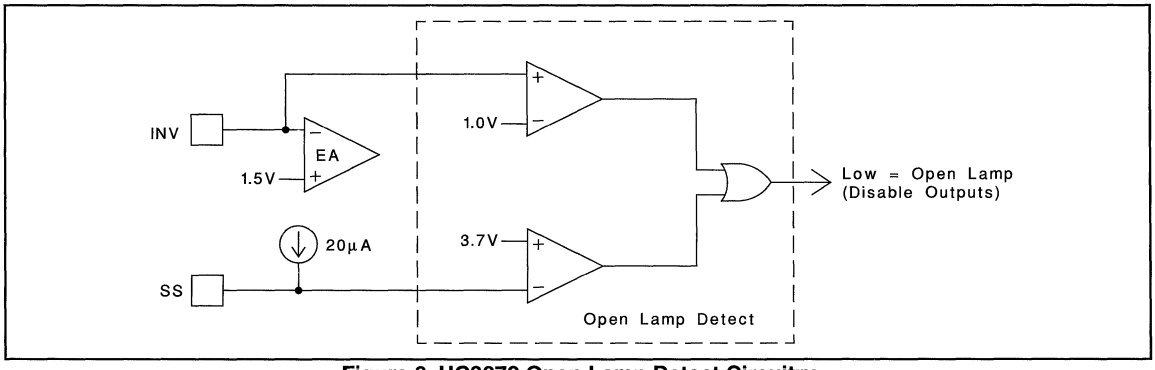


Figure 3. UC3872 Open Lamp Detect Circuitry

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 FAX (603) 424-3460

BiCMOS Cold Cathode Fluorescent Lamp Driver Controller

FEATURES

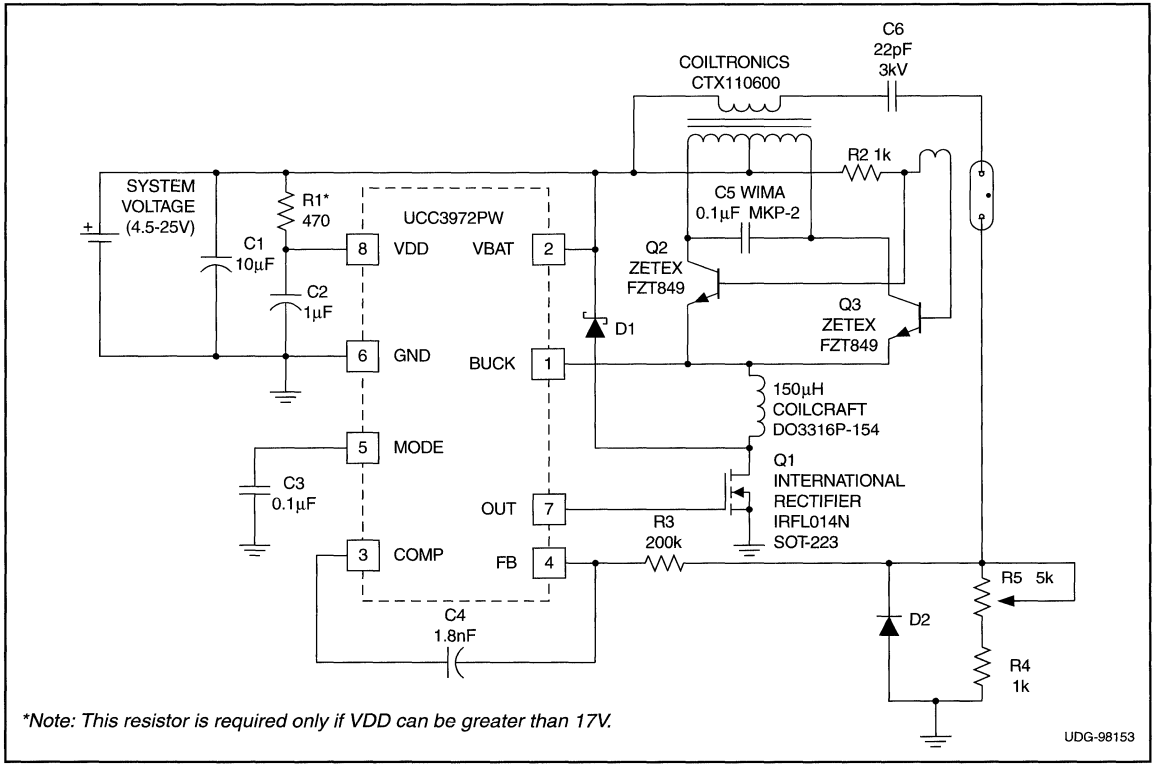
- 1mA Typical Supply Current
- Accurate Lamp Current Control
- Analog or Low Frequency Dimming Capability
- Open Lamp Protection
- 4.5 to 25V Operation
- PWM Frequency Synchronized to External Resonant Tank
- 8 Pin TSSOP and SOIC Packages Available

DESCRIPTION

Design goals for a Cold Cathode Fluorescent Lamp (CCFL) converter used in a notebook computer or portable application include small size, high efficiency, and low cost. The UCC3972 CCFL controller provides the necessary circuit blocks to implement a highly efficient CCFL backlight power supply in a small footprint 8 pin TSSOP package. The BiCMOS controller typically consumes less than 1mA of operating current, improving overall system efficiency when compared to bipolar controllers requiring 5 to 10mA of operating current.

External parts count is minimized and system cost is reduced by integrating such features as a feedback controlled PWM driver stage, open lamp protection, and synchronization circuitry between the buck and push-pull stages. The UCC3972 includes an internal shunt regulator, allowing the part to operate with input voltages from 4.5V up to 25V. The part supports both analog and low frequency dimming modes of operation.

TYPICAL APPLICATION CIRCUIT



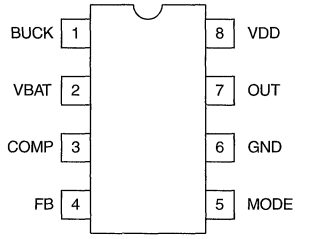
ABSOLUTE MAXIMUM RATINGS

VBAT . . . . . +27V
VDD Maximum Forced Current 30mA
Maximum Forced Voltage 17V
BUCK . . . . . –5V to VBAT
MODE . . . . . –0.3V to 3.2V
Operating Junction Temperature . . . . . –55°C to +150°C
Storage Temperature . . . . . –65°C to +150°C

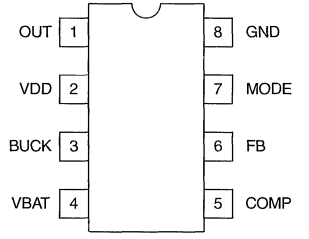
Unless otherwise indicated, currents are positive into, negative out of the specified terminal. Pulse is defined as less than 10% duty cycle with a maximum duration of 500µs. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

CONNECTION DIAGRAMS

TSSOP-8 (TOP VIEW)
PW Package



DIL-8 (TOP VIEW)
D, J, N Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise specified these specifications hold for T_A=0°C to +70°C for the UC3972, –40°C to +85°C for the UC2972, and –55°C to +125°C for the UC1972; T_A=T_J; VDD=VBAT=VBUCK=12V; MODE=OPEN. For any tests with VBAT>17V, place a 1K resistor from VBAT to VDD.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input supply					
VDD Supply Current	VDD = 12V		1	1.5	mA
	VBAT = 25V		7	10.5	mA
VBAT Supply Current	VBAT = 12V		30	60	µA
	VBAT = 25V		70	140	µA
VDD Regulator Turn-on Voltage	I_{SOURCE} = 2mA to 10mA	17	18	19	V
VDD UVLO Threshold	Low to high		4	4.4	V
UVLO Threshold Hysteresis		100	200	300	mV
Output Section					
Pull Down Resistance	I_{SINK} = 10mA to 100mA		50	75	Ω
Pull Up Resistance	I_{SOURCE} = 10mA to 100mA		50	75	Ω
Output Clamp Voltage	VBAT = 25V, Shunt Regulator on		16	18	V
Output Low	MODE = 0.5V, I_{SINK} = 1mA		0.05	0.2	V
Rise Time	CL = 1nF, Note 1		200		ns

ELECTRICAL CHARACTERISTICS: Unless otherwise specified these specifications hold for T_A=0°C to +70°C for the UC3972, –40°C to +85°C for the UC2972, and –55°C to +125°C for the UC1972; T_A=T_J; VDD=VBAT=VBUCK=12V; MODE=OPEN. For any tests with VBAT>17V, place a 1K resistor from VBAT to VDD.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Fall Time	CL = 1nF, Note 1		200		ns
Oscillator					
Minimum Frequency	BUCK = VBAT – 2	52	66	80	kHz
Maximum Synchronizable Frequency	BUCK = VBAT	160	200	240	kHz
Voltage Stability	BUCK = VBAT = 12V to 25V		5	7	%
Maximum Duty Cycle	FB = 1V	92	95		%
Minimum Duty Cycle	FB = 2V			0	%
BUCK Input Bias Current	BUCK = VBAT = 12V		40	90	µA
Zero Detect Threshold	Measured at BUCK w/respect to VBAT	–0.95	–0.75	–0.55	V
Error Amplifier					
Input Voltage	COMP = 2V	1.465	1.5	1.535	V
Input Bias Current		–500	–100		nA
Open Loop Gain	COMP = 0.5 to 3.0V	60	80		dB
Output High Voltage	FB = 1V	3.3	3.7	4.1	V
Output Low Voltage	FB = 2V		0.15	0.35	V
Output Source Current	FB = 1V, COMP = 2V		–1.2	–0.4	mA
Output Sink Current	FB = 2V, COMP = 2V	45	90		µA
Output Source Current	FB = 1V, COMP = 2V, MODE = 0.5V	–1		1	µA
Output Sink Current	FB = 2V, COMP = 2V, MODE = 0.5V	–1		1	µA
Unity Gain Bandwidth	YJ = 25C, Note 1		2		MHz
Mode Select					
Output Enable Threshold		0.85	1	1.15	V
Open Lamp Detect Enable Threshold		2.75	3	3.25	mV
Mode Output Current	MODE = 0.5V	15	20	25	µA
MODE Clamp Voltage	MODE = OPEN	3.3	3.7	4	V
DIM					
Open Lamp Detect Threshold	Measured at BUCK with respect to VBAT	–12	–10	–8	V

PIN DESCRIPTIONS

BUCK: Senses the voltage on the top side of the inductor feeding the resonant tank. The voltage at this point is used to synchronize the internally generated ramp, and is also used to detect whether an open lamp condition exists. An open lamp condition exists when this voltage is below the specified threshold for seven clock cycles. If the MODE pin is held below the open lamp detect enable threshold, this protective feature is disabled.

COMP: Output of the error amplifier. Compensation components set the bandwidth of the entire system and are normally connected between COMP and FB. The error amplifier averages lamp current against a fixed internal reference. The resulting voltage on the COMP pin is compared to an internally generated ramp, setting the PWM duty cycle. During UVLO, this pin is actively pulled low.

FB: This pin is the inverting input to the error amplifier.

GND: Ground reference for the IC.

MODE: The voltage on this pin is used to control start-up and various modes of operation for the part (refer to the table in the block diagram).

When the voltage is below 1V, OUT is forced low, open lamp detection is disabled and the error amplifier is tri-stated.

When the voltage is between 1V and 3V, OUT is enabled and the error amplifier output is connected to COMP. Open lamp detection is still disabled and a constant 20µA cur-

PIN DESCRIPTIONS (cont.)

rent is sourced from this pin. Placing an appropriate value external capacitor between this pin and ground allows the user to disable open lamp detection for a set period of time at start-up to allow the lamp to strike.

When MODE reaches 3V, open lamp detection is enabled and normal operation is activated.

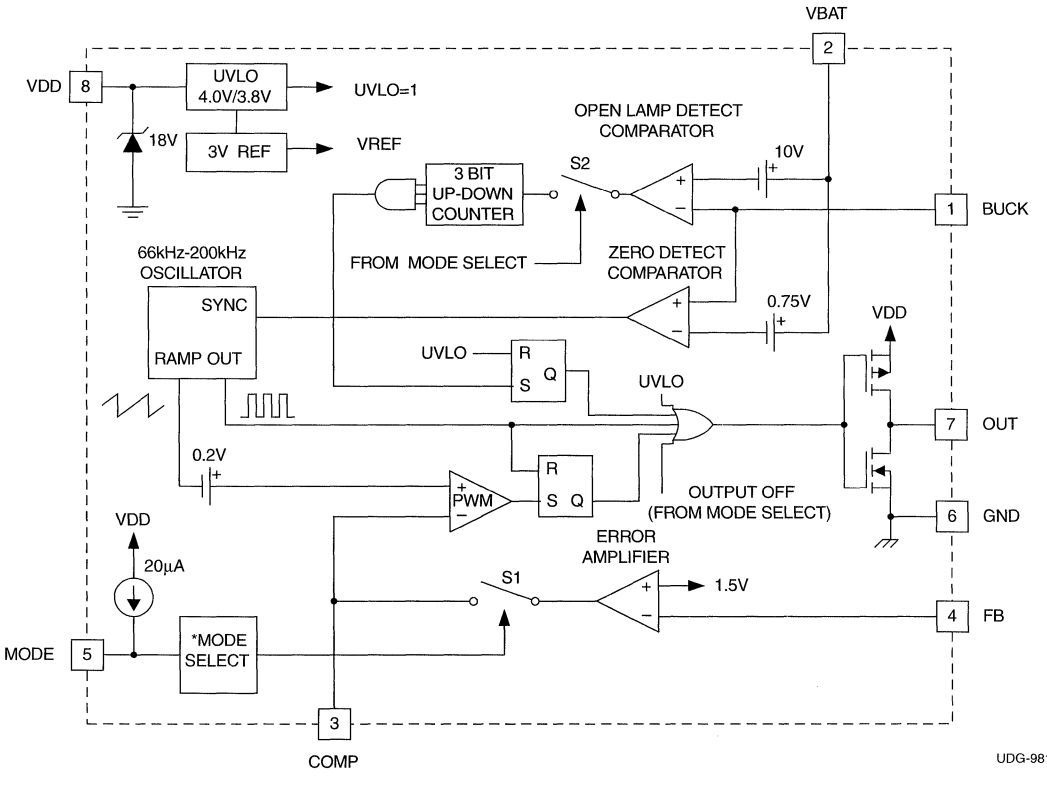
A square wave can be applied to this pin allowing a low frequency dimming technique to be implemented.

OUT: Drives the buck regulator N-channel MOSFET. OUT turn-on is synchronized to twice the tank resonant frequency. OUT is actively pulled low when in UVLO, an open lamp condition has been detected or MODE is less than 1V.

VBAT: Positive input supply to power stage. This voltage is required by internal control circuitry to provide open-lamp detection and synchronization. Operating range is from 4.5V to 25V.

VDD: This pin connects to the battery voltage from which the CCFL inverter will operate. If the potential on VBAT can exceed 18V in the application, a series resistor must be placed between VBAT and this pin (see applications section). The voltage at the VDD pin will then be regulated

BLOCK DIAGRAM



*MODE	Output	Open Lamp Detection	S2	Error Amplifier Output	S1
<1V	OFF	DISABLED	OPEN	DISCONNECTED FROM COMP	OPEN
1V< MODE< 3V	ON	DISABLED	OPEN	CONNECTED TO COMP	CLOSED
>3V	ON	ENABLED	CLOSED	CONNECTED TO COMP	CLOSED

APPLICATION INFORMATION (cont.)

Introduction

Cold Cathode Fluorescent Lamps (CCFL) are frequently used as the backlight source for Liquid Crystal Displays (LCDs). These displays are found in numerous applications such as notebook computers, portable instrumentation, automotive displays, and retail terminals. Fluorescent lamps provide superior light output efficiency, making their use ideal for power sensitive portable applications where the backlight circuit can consume a significant portion of the battery's capacity. The backlight converter must produce the high voltage needed to strike and operate the lamp. Although CCFLs can be operated with a DC voltage, a symmetrical AC operating voltage is recommended to maintain the rated life of the lamp. Sinusiodal voltage and current lamp waveforms are also recommended to achieve optimal electrical to light conversion and to reduce high voltage electromagnetic interference (EMI). A topology that provides these requirements while maintaining efficient operation is presented in Fig. 1.

Circuit Operation

A current fed push-pull topology is used to power the CCFL backlight shown in Fig. 1. This topology accommodates a wide input voltage and dimming range while retaining sinusoidal operation of the lamp. The converter consists of a resonant push-pull stage, a high voltage output stage, and a buck pre-stage used to regulate current in the converter.

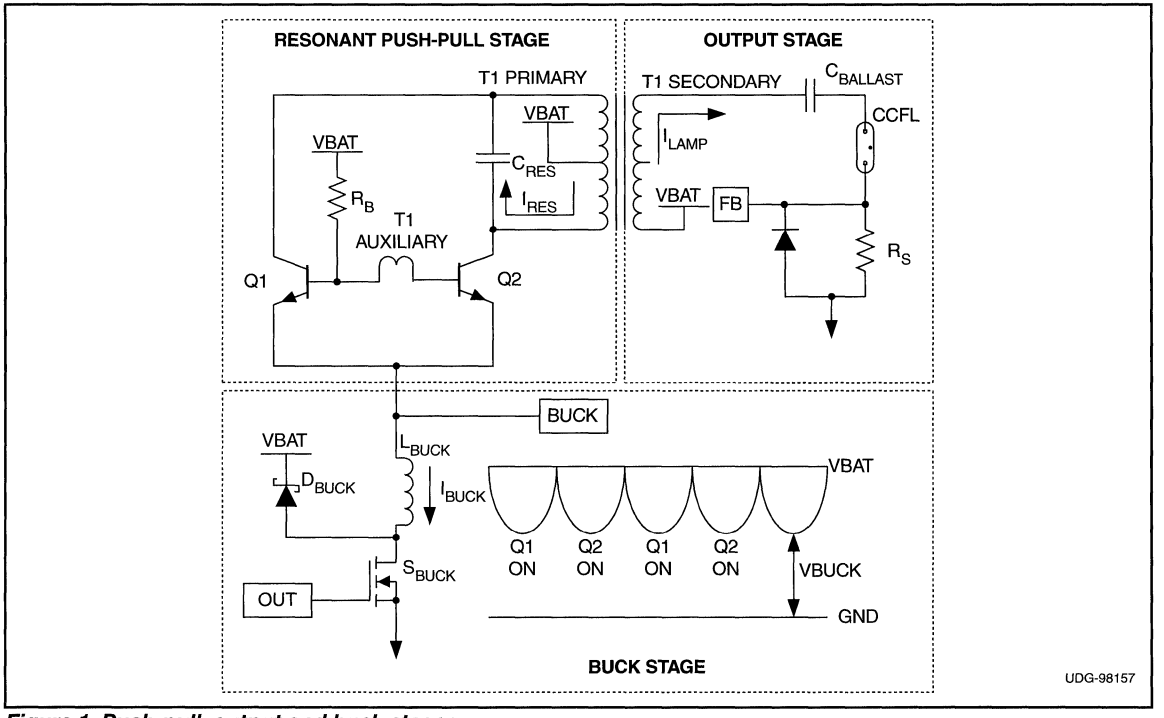


Figure 1. Push-pull, output and buck stages.

Referring to Fig. 1, the push-pull stage consists of C_{RES}, Q1, Q2, Rb, and T1's primary and auxiliary windings. The output stage consists of $C_{BALLAST}$, the lamp, the current sense resistor Rs, and T1's secondary. The resonant frequency of the tank is set by the primary inductance of T1, along with the resonant capacitor (C_{RES}), and the reflected secondary impedance. The secondary impedance includes the lamp, the ballast capacitor ($C_{BALLAST}$), the distributed winding capacitance of T1, and the stray capacitance which forms between the lamp, lamp wires, and the backlight reflector. Since the lamp impedance is nonlinear with operating current, the tank resonant frequency will vary slightly with load (typically 1.5:1).

The primary resonant tank consisting of T1's primary inductance and C_{RES} produces a sinusoidal current (I_{RES}) and is fed by a controlled DC current (I_{BUCK}) from the buck stage. Note that the BUCK node voltage is 1/2 the primary

APPLICATION INFORMATION (cont.)

tank voltage, as VBAT is located at the center tap of the transformer. The high turns ratio transformer (T1) amplifies the sinusoidal tank voltage to produce a sinusoidal secondary voltage that is divided between the lamp and ballast capacitor. Due to the winding construction of T1, the secondary voltage has a small DC offset (VBAT). This DC component is blocked by $C_{BALLAST}$ and has no effect on lamp operation. $C_{BALLAST}$ also provides high output impedance, allowing the secondary current (I_{LAMP}) to remain sinusoidal driving the highly nonlinear lamp load.

Transistors Q1 and Q2 are driven out of phase at 50 percent duty cycle with an auxiliary winding on T1. The winding provides a floating AC voltage source at the resonant frequency that is used to drive the transistor bases alternately on and off. One leg of the auxiliary winding is tied to the input voltage through base resistor Rb, which is sized to provide sufficient base current to the transistors. The transistors channel the buck inductor current into opposing ends of the tank at the resonant frequency, supplying energy for the lamp and system losses.

The buck power stage consists of inductor L_{BUCK}, MOSFET switch S_{BUCK}, and flyback diode D_{BUCK}. In order to prevent interactions between multiple switching frequencies, the UCC3972 synchronizes the buck frequency to the frequency of the push-pull stage. The traditional buck topology is inverted to take advantage of the lower R_{dsON} characteristics of an N-Channel MOSFET switch (S_{BUCK}). With a sinusoidal voltage across the tank, the resulting output of the buck stage (V_{BUCK}) becomes a full-wave rectified voltage referenced to VBAT as shown in Fig. 1.

Lamp current is sensed directly with Rs and a parallel diode on each half cycle. The resulting voltage across the sense resistor Rs is kept at a 1.5V average by the error amplifier, which in turn controls the duty cycle of S_{BUCK}. The buck converter typically operates in continuous current mode but can operate with discontinuous current as the CCFL is dimmed.

Typical Design Procedure

A notebook computer backlight circuit will be presented here to illustrate a design based on the UCC3972 controller. The converter will be designed to drive a single cold cathode fluorescent lamp (CCFL) with the following specifications:

Table 1. Lamp Specifications

Lamp Length	250mm (10")
Lamp Diameter	6mm
Striking Voltage (20C)	1000V (peak)
Operating Voltage (5mA)	375V (rms)
Full Rated Current	5mA
Full Rated Power	1.9 watt

Input Voltage Range

The notebook computer will be powered by a 4 cell Lithium-Ion battery pack with an operational voltage range of 10V to 16.8V. When the pack is being charged, the back light converter is powered from an AC adapter whose DC output voltage can be as high as 22V.

Resonant Tank and Output Circuit

The selection of components to be used in the resonant tank of the converter is critical in trading off the electrical and optical efficiencies of the system. The value of the output circuit's ballast capacitor plays a key role in this tradeoff. The voltage across the ballast capacitor is a function of the resonant frequency and secondary lamp current:

$$V_{CB} = \frac{I_{LAMP}}{2 \bullet \pi \bullet C_{BALLAST} \bullet F_{RESONANT}} \quad (1)$$

A voltage drop across $C_{BALLAST}$ many times the lamp voltage will make the secondary current insensitive to distortions caused by the non-linear behavior of the lamp, providing a high impedance sinusoidal current source with which to drive the CCFL. This approach improves the optical efficiency of the system, as capacitive leakage effects are minimized due to reduced harmonic content in the voltage waveforms. Unfortunately, from an electrical efficiency standpoint, an increased tank voltage produces increased flux losses in the transformer and increased circulating currents in the tank. In practice, the voltage drop across the ballast capacitor is selected to be approximately twice the lamp voltage (750Vin our case) at rated lamp current. Assuming a 50kHz resonant frequency and 5mA operating current, a ballast capacitance of 22pF is selected. Since the lamp and ballast capacitor impedances are 90 degrees out of phase, the vector sum of lamp and capacitor voltages determine the secondary voltage on the transformer.

$$V_{SEC} = \sqrt{(V_{CB})^2 + (V_{LAMP})^2} \quad (2)$$

The resulting secondary voltage at rated lamp current is 840V. Since the capacitor dominates the secondary impedance, the lamp current maintains a sinusiodal shape despite the non-linear behavior of the lamp. As the CCFL is dimmed, lamp voltage begins to dominate the secondary

APPLICATION INFORMATION (cont.)

impedance and current becomes less sinusiodal. Transformer secondary voltage is reduced, however, so high frequency capacitive losses are less pronounced. The value of ballast capacitor has no effect on current regulation since the average lamp current is sensed directly by the controller.

Once the ballast capacitor is selected, the resonant frequency of the push-pull stage can be determined from the transformer's inductance (L), turns ratio (N), and the selection of resonating capacitor (C_{RES}).

$$F_{RESONANT} = \frac{1}{2\pi\sqrt{L_{PRIMARY}\left(C_{RES} + \left(N^2 \bullet C_{BALLAST}\right)\right)}} \quad (3)$$

Output distortion is minimized by keeping the independent resonant frequencies of the primary and secondary circuits equal. This is achieved by making the resonant capacitor equal to the ballast capacitance times the turns ratio squared:

$$C_{RES} = N^2 \bullet C_{BALLAST} = (67)^2 \bullet 22pF = 0.1\mu F \quad (4)$$

The Coiltronics transformer selected for this application produces a of primary inductance of 44µH.

The resulting resonant frequency is about 50kHz, this frequency will vary depending upon the lamp load and amount of stray capacitance in the system.

Efficiency Considerations for the Resonant Tank and Output Circuit

Since high efficiency is a primary goal of the backlight converter design, the selection of each component must be carefully evaluated. Losses in the ballast capacitor are usually insignificant, however, its value determines the tank voltage which influences the losses in the resonant capacitor and transformer. Since the resonant capacitor has high circulating currents, a capacitor with low dissipation factor should be selected. Power loss in the resonant tank capacitor will be:

$$C_{RES\_LOSS}(watts) = (C_{TANK})^2 \bullet 2\pi \bullet F_{RESONANT} \bullet C_{RES} \bullet Dissipation\,Factor \quad (5)$$

Polypropylene foil film capacitors give the lowest loss; metalized polypropylene or even NPO ceramic may give acceptable performance in a smaller surface mount (SMT) package. Table 2 gives possible choices for the resonant and high voltage ballast capacitors.

The transformer is physically the largest component in the converter, making the tradeoff of transformer size and efficiency a critical choice. The transformer's efficiency will be determined by a combination of wire and core losses. A Coiltronics transformer (CTX110600) was chosen for this application because of its small size, low profile, and overall losses of about 5% at 1W.

Wire losses in the transformer are determined by the RMS current and the ESR of the windings. The primary winding resistance for the Coiltronics transformer is 0.16Ω. The RMS current of the primary winding includes the sinusoidal resonant current and the DC buck current on alternate half cycles (i.e. only 1/2 of the primary winding sees the buck current depending upon which transistor is on). Maximum resonant current is equal to:

$$I_{RES} = \frac{V_{PRIMARY}}{\sqrt{\frac{L_{PRIMARY}}{C_{RES}}}} = \frac{840}{67 \bullet \sqrt{\frac{44}{0.1}}} = 600\,mA \quad (6)$$

Buck inductor current is calculated in the next section. The secondary winding has 176Ω of resistance.The secondary current is simply the lamp current

Transformer core losses are a function of core material, cross sectional area of the core, operating frequency, and

Table 2. Capacitor Selection

Manufacturer	Capacitance Type	Series	Dissipation Factor (1kHz)
Ballast Capacitor			
Cera-Mite (414) 377-3500	High Voltage Disk Capacitor (3kV)	564C	
NOVA-CAP (805) 295-5920	SMT 1808 (3kV)	COG	
Murata Electronics	SMT 1808 (3kV)	GHM	
Resonant Capacitor			
Wima (914)347-2474	Polypropylene foil film FKP02	FKP02	0.0003
	Metalized Polypropylene	MKP2	0.0005
	SMT Metalized polyphenylene-sulfide	MKI	0.0015
Paccom (800)426-6254	SMT Metalized polyphenylene-sulfide	CHE	0.0006
NOVA-CAP	SMT Ceramic	COG	0.001

APPLICATION INFORMATION (cont.)

voltage. For ferrite material, the hysteresis core losses increase with voltage by a cubed factor; for a given core cross sectional area, doubling the tank voltage will cause the losses to increase by a factor of 8.

Other elements influencing the resonant tank and output circuit efficiency include the push-pull transistors, the base drive and sense resistors, as well as the lamp. High gain, low VCESAT bipolar transistor such as Zetek's FZT849 allow high efficiency operation of the push-pull stage. These SOT223 package parts have a typical current transfer ratio (hFE) of 200 and a forward drop (VCESAT) of just 35mV at 500mA. Rohm's 2SC5001 transistors provide similar performance. For low power, size sensitive applications, a SOT23 transistor is available from Zetek (FFMT619) with approximately twice the forward drop at 500mA. The base drive resistor R_B is sized to provide full VCE saturation for all operating conditions assuming a worst case hFE. For efficiency reasons, the base resistor should be selected to have the highest possible value. A 1kΩ resistor was selected in this application. Losses scale with buck voltage as:

$$LOSS_{RB(watts)} = \frac{(V_{BUCK})^2}{R_B} \quad (7)$$

The current sense resistor Rs provides direct control of lamp current. Since the current sense resistor voltage is controlled to a 1.5V reference, its power loss is inversely proportional to its value at a given lamp current. Finally, the efficiency of the lamp is typically not included in discussions about the electrical efficiency of the system. Electrical to optical efficiency of the lamp is discussed in a later section titled *Cold Cathode Fluorescent Lamp Characteristics.*

Synchronizing the Stages

An internal comparator at the BUCK node is used to synchronize the PWM buck frequency to twice the resonant tank frequency. Synchronization is accomplished with a sync pulse that is generated each time the BUCK node voltage is within 0.75Vof VBAT; the UCC3972 uses this sync pulse to reset the PWM oscillator's saw-tooth ramp. The sync circuit will operate with PWM frequencies between 66kHz and 200kHz, corresponding to a 33kHz to 100kHz tank frequency. If the resonant frequency of the tank is outside of this range, the PWM frequency will run asynchronous.

Buck Stage

The PWM output controls current in the buck inductor. The UCC3972's buck power stage differs from a traditional buck topology in a few respects:

- The topology is inverted using a ground referenced N-Channel MOSFET rather than a VDD referenced P-Channel.
- The output voltage is a full wave rectified sinewave at the switching frequency, rather than DC.

Referring back to Fig. 1, when OUT turns S_{BUCK} on, the buck node voltage VBUCK is placed across the inductor. This voltage is typically positive and current ramps up in the inductor (it is possible for the BUCK node voltage to go negative if VBAT is low and the lamp current is near maximum). When S_{BUCK} is turned off, VBAT–VBUCK+VDBUCK is placed across the inductor with opposite polarity. As with any buck converter, the volt-seconds across the inductor must be reversed on each switching cycle to maintain constant current. The duty cycle (D) relationship is complicated somewhat by the fact the output voltage is changing within a switching cycle. The equations below determine the relationship between on and off times in continuous conduction mode where T is the switching period, D = t_{ON}/T, and t_{OFF} = $T-t_{ON}$.

$$\int_0^{t_{ON}} V_{BUCK} \bullet dt = \int_{t_{ON}}^{T} (VBAT - V_{BUCK} + V_D) \bullet dt \quad (8)$$

Selecting the Buck Inductor

Maximum ripple current on the inductor occurs when lamp current and input voltage are at a maximum.

$$V_{BUCK(avg)} = V_{BAT} - \frac{V_{SEC} \bullet \sqrt{2}}{N \bullet \pi} \quad (9)$$

$$= V_{BAT} - \frac{840 \bullet \sqrt{2}}{67 \bullet \pi} = V_{BAT} - 5.6 \bullet Volts$$

The approximate on time using the maximum 22V input voltage ($V_{BUCK\ (avg)}$=16.4), a 100kHz switching frequency (two times the resonant frequency), and ignoring the diode drop can be calculated from the following:

$$\frac{t_{ON}}{T - t_{ON}} = \frac{VBAT - V_{BUCK(avg)}}{V_{BUCK(avg)}} \quad (10)$$

The resulting on time is 2.5 microseconds. A 150µH inductor will result in a peak to peak ripple current of 280mA. Average inductor current (with maximum lamp current) can be calculated by taking the lamp power divided by the tank efficiency and the RMS buck voltage.

APPLICATION INFORMATION (cont.)

$$I_{BUCK} = \left(\frac{V_{LAMP} \bullet I_{LAMP}}{Efficiency}\right) \bullet \frac{2 \bullet N}{V_{SEC}} = \frac{375 \bullet 0.005 \bullet 2 \bullet 67}{0.9 \bullet 840} \quad (11)$$

$$= 330\,mA$$

The resulting inductor ripple is less than 50%. A list of possible inductors are given below along with ESR and current rating (losses in the inductor are calculated with RMS current).

Table 3. Inductor Suppliers

Vendor	L	Part Number	ESR	Current Rating
Coilcraft (847) 639-6400	150µH	DO3316-154	0.38	1A
Coiltronics (407) 241-7876	150µH	CTX150-4	0.175	0.72A
Sumida (847) 956-0666	150µH	CDR125-151	0.4	0.85A

The choice of a MOSFET for the buck switch should take into consideration conduction and switching losses. The Rds_{ON} and gate charge are typically at odds, however, where minimizing one will typically result in the other increasing. An International Rectifier IRFL014 was selected (SOT-223 package) in this application with a gate charge of 11nC and Rds_{ON} of 0.2Ω. A Schottky diode should be used for the buck diode in order to minimize forward drop.

Dimming Techniques

Analog Dimming

A control circuit that implements analog dimming with a potentiometer (R_{ADJ}) is shown in Fig. 2. Average lamp current is controlled by adjusting R_{ADJ} to the appropriate value. Resistor R_L sets the low end dimming level of the lamp. When the secondary has a positive polarity current, D1 is reversed biased and lamp current is sensed directly through R_L and R_{ADJ}. When the current reverses direction, D1 conducts and the voltage on the sense node V is clamped to the forward drop of the diode. The resulting waveform at V_X is a half wave rectified sinusoid whose voltage is proportional to lamp current. This voltage is averaged by the feedback components (R_{FB}, C_{FB}) and held to 1.5V by the error amplifier when the control loop is active. The resulting voltage at the output of the error amplifier (COMP) sets the duty cycle of PWM stage.

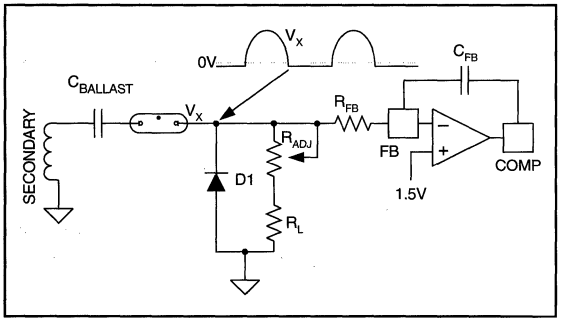


Figure 2. Analog dimmer with potentiometer.

Digitally Controlled Analog Dimming

Analog dimming control of the lamp can be achieved by providing a digital pulse stream from the system microprocessor as shown in Fig. 3. In this case the lamp current sense resistor (R1) is fixed and the VX node voltage is averaged against the digital pulse stream of the microprocessor. The averaging circuit consists of R2, R3, and C_{FB}. A higher average value from the pulse stream will result in less average lamp current. If a D/A converter is available in the system, a DC output can be used in place of the pulse stream.

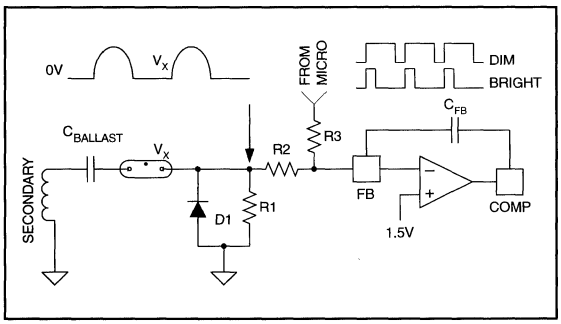


Figure 3. Analog dimming control from microprocessor

Low Frequency Dimming

Analog dimming techniques described previously can provide excellent dimming over a 10:1 range, depending upon the physical layout and the amount of stray capacitance in the backlight's secondary circuitry. Beyond this level the lamp may begin to exhibit the "*thermometer effect*" causing uneven illumination across the tube.

Low frequency dimming is accomplished by operating the lamp at rated current and gating the lamp on and off at a low frequency. Since the lamp is operated at full intensity when on, the system layout has little effect on dimming performance. The average lamp intensity is a function of the duty cycle and period of the gating signal.

APPLICATION INFORMATION (cont.)

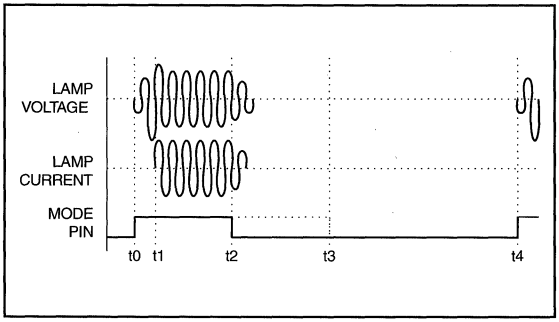


Figure 4. Low frequency dimming with the UCC3972 MODE pin.

The duty cycle can be controlled to a low minimum value, allowing a very wide dimming range. Low frequency dimming can be implemented by using the MODE pin on the UCC3972 as shown in Fig. 4.

Referring to Fig. 4, at time t0 the MODE pin is brought high, the UCC3972 is enabled and the voltage in the resonant tank begins to build. At time t1 there is sufficient voltage for the lamp to strike and the feedback loop controls the lamp at rated current using a fixed current sense resistor. When the mode pin is brought low at time T2, the feedback loop opens (retaining the voltage on CFB) and the PWM output is disabled. The resonant tank voltage decays until the lamp extinguishes. If the on time were extended to t3 the average lamp intensity would be increased accordingly, the next low frequency cycle begins at time t4. The time relationship between the resonant and gating frequency has been exaggerated so that the sinusoidal waveforms can be depicted. In order to avoid visible lamp flicker, the low frequency gating rate (t0-t4) should be greater than 100Hz. To prevent "beat" frequency interference, it may be advantageous to synchronize the gating frequency to a multiple of the monitor scan rate of the LCD display. This can be accomplished by controlling the MODE pin's duty cycle with a timer routine within the LCD's software program.

Depending on the striking characteristics of the lamp, the open lamp detection circuit may need to be altered to accomodate low frequency dimming. The open lamp threshold can be increased by adding a resistive divider at the buck node. An RC delay network can be added to the MODE pin to slow the slew rate between 1V and 3V. Finally, the open lamp protection can be disabled by restricting the MODE pin to toggle between 0V and 2V during frequency dimming.

Striking the Lamp

Before the lamp is struck, the lamp presents an impedance much larger than the ballast capacitor and the full output voltage of the transformer secondary is across the lamp. Since the buck converter must reverse the volt -seconds on the buck inductor, the average tank voltage at the primary can be no greater than the DC input voltage. This constraint along with the turns ratio of the push-pull transformer sets the peak voltage available to strike the lamp:

$$V_{STRIKE} = N_{S:P} \bullet \pi \bullet V_{INPUT} \quad (12)$$

The Coiltronics transformer has a 67:1 turns ratio, giving 2100 peak volts available to strike the lamp with the minimum 10V input. In our example this is more than sufficient for the 1000V required to strike the lamp. With the 22V maximum charger input, the available striking voltage could theoretically reach 5000V! The possibility of breaking down the transformer's secondary insulation becomes a real concern at this voltage. Fortunately, in practice the lamp will strike within the first few cycles once sufficient voltage is developed on the secondary. Difficulty with striking the lamp usually results from one or a combination of the following:

- Insufficient transformer turns ratio or input voltage.
- Increase in required striking voltage at cold temperature.
- Transformer secondary voltage is reduced due to voltage division between parasitic secondary capacitance and the ballast capacitor.

Open Lamp Protection / Detection

Open lamp protection provides safety and will often protect the transformer and converter circuitry in the event of a broken or open circuited lamp. Referring to the Block Diagram, the UCC3972 monitors the BUCK pin voltage with respect to VBAT to determine if an open lamp has occurred. If this voltage exceeds 10V for seven consecutive PWM cycles, an open lamp will be declared and the converter will latch off until power to the part is cycled off and on. If the open lamp fault level needs to be increased, an appropriate resistive divider from VBAT to BUCK can be added.

A capacitor on the MODE pin of the UCC3972 can be used to blank the open lamp protection circuitry during the initial lamp start-up. When the backlight is initially powered-up, a 20µA current out of the MODE pin charges the capacitor CMODE from ground potential. Since the PWM output is disabled when the MODE pin is between 0V and 1V, open lamp blanking occurs as CMODE is charged from 1V to 3V, giving a soft start period of:

APPLICATION INFORMATION (cont.)

$$T_{SS} = \frac{C_{MODE}}{10^{-6}} \text{ Seconds} \quad (13)$$

Voltage Regulator

The UCC3972 controller contains an internal 18V shunt regulator that provides a 5% accurate voltage clamp for the MOSFET gate drive while allowing the controller to operate in applications with input voltages up to 25V. Since only the VBAT and BUCK pins are rated for 25V, the shunt regulator limits the voltage on the VDD and OUT pins to 18V. The MODE, CS, and COMP pin voltages are typically less than 5V. If the UCC3972 is to be used in an application with input voltages greater than 18V, a resistor from VBAT to VDD is required to limit the current into the VDD pin. The resistor should be sized to allow sufficient current to operate the controller and drive the external MOSFET gate, while minimizing the voltage drop across the resistor. A bypass capacitor should be connected at the VDD pin to provide a constant operating voltage.

Selecting the Shunt Resistor

The first step in selecting the shunt resistor is to determine the current requirements for the application. With a 100kHz switching frequency and a maximum gate charge of 11nC for the IRFL014 MOSFET, the gate drive circuit requires 1.1mA of average current. The UCC3972 requires an additional maximum quiescent current of 1.5mA. The shunt resistor must therefore supply 2.6mA of current over the operating voltage of the part.

The application's maximum input voltage is 22V. With a regulator clamp voltage of 18V, the maximum value for the shunt resistor becomes 1.5kΩ [(22-18)V/2.6mA]. This resistor will minimize losses at maximum input voltage, but could produce a 4V drop (from VBAT to VDD) even when the regulator is not clamped. This drop reduces the available gate drive voltage, leaving only 6V with the minimum input voltage of 10V. Since the efficiency of the shunt regulator is not of primary importance when the charger is running, a smaller value of shunt resistor is selected to improve the available gate drive voltage. A 470Ω shunt resistor will produce a maximum 1.2V drop from VBAT to VDD when the shunt regulator is not clamped. When the regulator is clamped at 18V and the charger voltage is at its maximum of 22V, the power across the shunt resistor will be 35mW [(4V x 4V)/470].

Lamp Current Control Loop

The control loop for the CCFL circuit is discussed in detail in Unitrode Application Note U-148 and is briefly repeated here for completeness. A block diagram for the current control loop is shown in Fig. 5.

The PWM modulator small signal gain is inversely proportional to the internal saw tooth ramp and proportional to the input voltage (the inductor's current slope increases as VBAT increases). The resonant tank and buck inductor form a RLC filter at the center point of the push pull transformer. The effective L of the filter is dominated by buck inductor and the effective C is approximately 8 times the resonant capacitor (C_{RES}) value. This occurs because the reflected ballast capacitance is equal

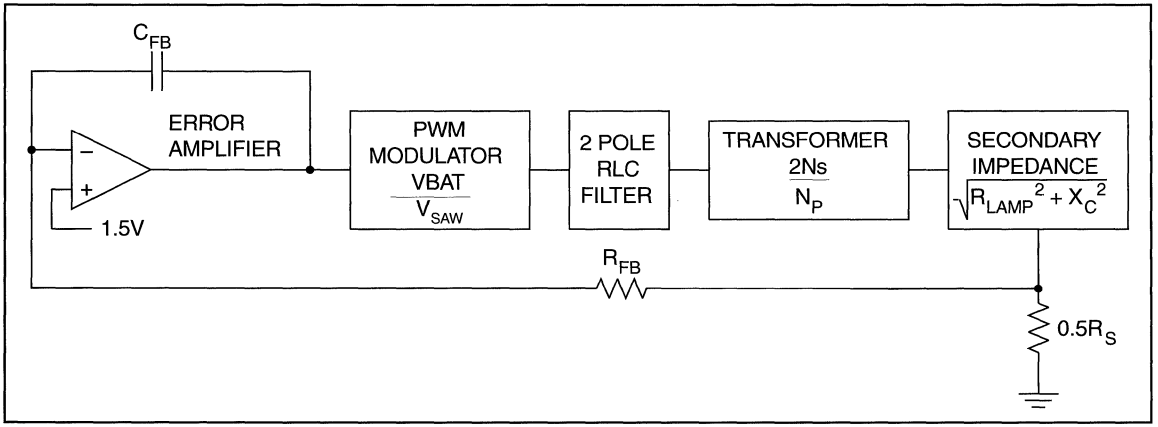


Figure 5. Current control loop block diagram.

APPLICATION INFORMATION (cont.)

to C_{RES} and the equivalent capacitance at the push-pull center point is four times the capacitance across the tank. The equivalent resistance at the push-pull center point is equal to 1/4 the tank voltage squared divided by the lamp power. The corner frequency and Q of the filter are:

$$F_{CORNER} = \frac{1}{2\pi\sqrt{L_{BUCK} \bullet 8 \bullet C_{RES}}} \quad (14)$$

$$Q = \frac{2 \bullet \pi \bullet f_{FILTER} \bullet L_{BUCK}}{R_{FILTER}} \quad (15)$$

The resulting gain of the RLC filter is unity below the 15kHz corner frequency, peaking up at the corner frequency with Q, and rolling off with a 2-pole response above the corner frequency. As shown in Fig. 5, the transformer turns ratio provides a voltage gain and the output circuit (whose impedance includes the lamp and ballast capacitor) converts the voltage into a current. The current sense resistor produces a voltage on each half cycle, leaving the error amplifier as the final gain block.

Loop gain is greatest at minimum lamp current and maximum input voltage. With a 22V input, 2V sawtooth, 375V lamp voltage, 1mA lamp current, and Rsense at 1kΩ, the DC gain of the circuit is 2. The error amplifier is configured as an integrator, giving a single pole roll-off and a high gain at DC. The 200k feedback resistor and 1.8nF feedback capacitor give a total loop crossover of 1kHz, avoiding any possible stability problems with the Q of the resonant tank.

Cold Cathode Lamp Characteristics

Before beginning a CCFL converter design, it is important to become familiar with the characteristics of the lamp. The lamp presents a non-linear load to the converter resulting in unique voltage -vs- current (VI) characteristics. The length, diameter, and physical construction of the lamp determine its performance, and thus impact the design of the converter. Fig. 6 shows the VI characteristics collected from various lengths of 6mm diameter lamps, where Fig. 7 shows the characteristics of several 3mm-diameter lamps.

It is interesting to note how the operating and striking voltages (V_{STRIKE}) of the lamps are related to length as well as lamp diameter. Since equal length CCFLs of different diameters have about the same lumens per watt efficiency, the smaller diameter lamps actually produce more light when driven at a given current since they operate at a higher voltage. The lamps have regions of positive and negative resistance with the voltage peaking at 4mA for the 6mm diameter lamps and at 1mA for the 3mm diameter lamps.

In order to successfully dim the lamp, the converter's resonant tank and step up transformer must provide enough voltage to keep the lamp operating over the whole range of operating current, this requirement becomes more difficult with longer length and smaller di-

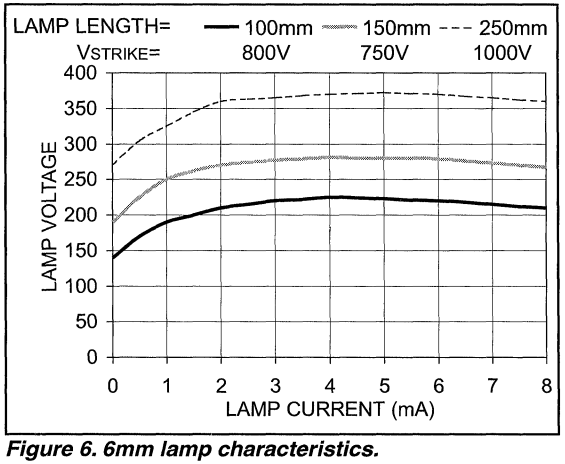


Figure 6. 6mm lamp characteristics.

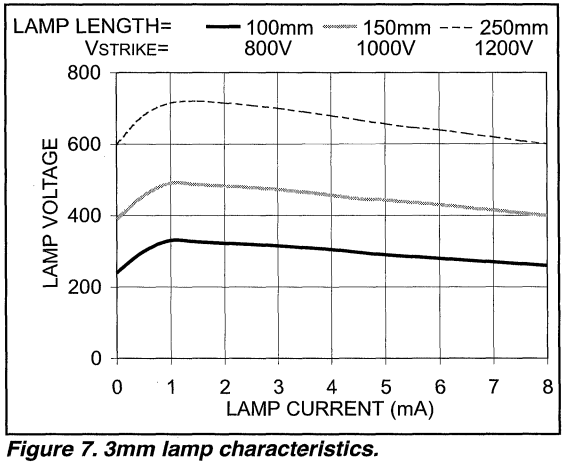


Figure 7. 3mm lamp characteristics.

APPLICATION INFORMATION (cont.)

ameter lamps. Since the lamp characteristics will vary with the manufacturing technique, it is a good idea to collect data from several lamp manufacturers and to include design margin for process variations.

Since a fluorescent lamp is a pressurized gas filled tube (usually Argon and Mercury vapor), it shouldn't be surprising that temperature plays a major role in the lamp characteristics. Fig. 8 depicts the variations in striking and operating voltage for a 150 x 3mm lamp over temperature, illustrating the importance of taking temperature effects into account when designing the converter. The lumen output of the backlight system is temperature dependent as well, and may need to be accounted for in applications requiring tight lumens regulation over a wide temperature range. Fig. 9 shows the temperature effects on lumens for the lamp operated at 5mA.

Since lamp current is roughly proportional to luminosity, it may be tempting to operate the lamp at a RMS current higher than specified in the manufacturer's data sheet. While the lamp will continue to operate tens of percent above the rated current, the luminosity gain becomes

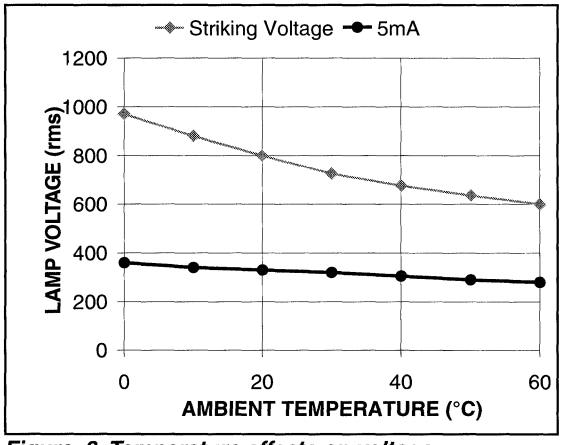


Figure 8. Temperature effects on voltage.

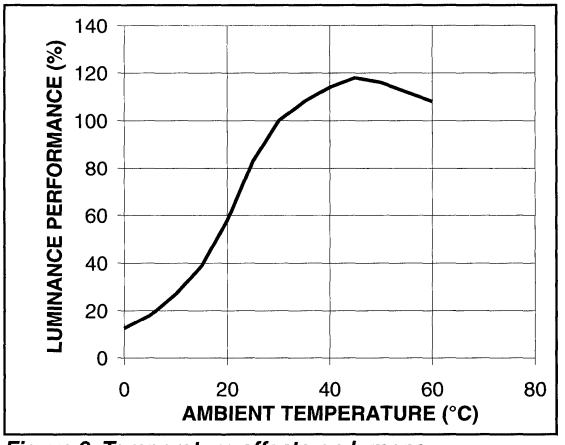


Figure 9. Temperature effects on lumens.

APPLICATION INFORMATION (cont.)

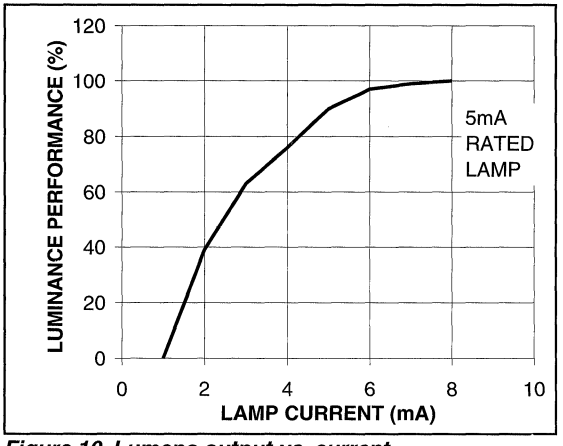


Figure 10. Lumens output vs. current.

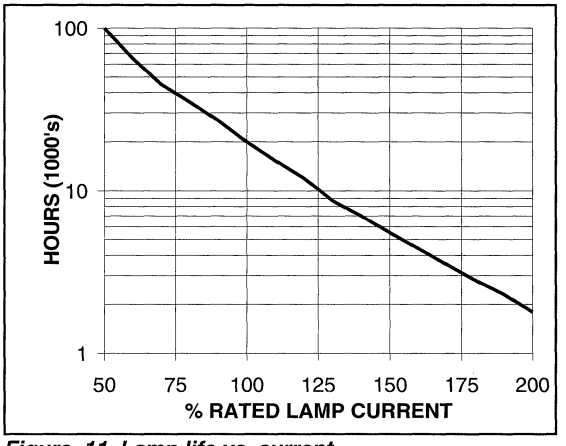


Figure 11. Lamp life vs. current.

less pronounced as the lamp is over-driven as shown in Fig. 10. The expected life of the lamp will also degrade, as illustrated in Fig. 11, when the lamp is operated above rated current.

Cold Cathode Fluorescent Lamp Efficiency

Although CCFLs offer high output light efficiency compared to other lamp types such as incandescent, only a percentage of the input energy is converted to light. As illustrated in Fig. 12, 35% of the energy is lost in the electrodes, 26% as conducted heat along the tube. A portion of the Ultra Violet energy gets converted into visible light by the lamp phosphor, where the remainder is converted into radiated heat. Finally, Mercury atoms convert 3% of the initial energy into visible light. The result is typically 15% overall electrical to optical energy conversion in the lamp.

In a practical backlight design, the physical spacing between the lamp and high voltage secondary wiring with respect to the foil reflector and LCD frame can be tight. With this tight spacing, distributed stray capacitance will form as shown in Fig. 12. The stray capacitance causes leakage currents from the high voltage secondary to circuit ground. Although the current through stray capacitance doesn't directly translate into losses, the extra current through the transformer, primary resonant tank, and switching devices does. A poor layout with excessive stray capacitance can reduce system efficiency by tens of percent.

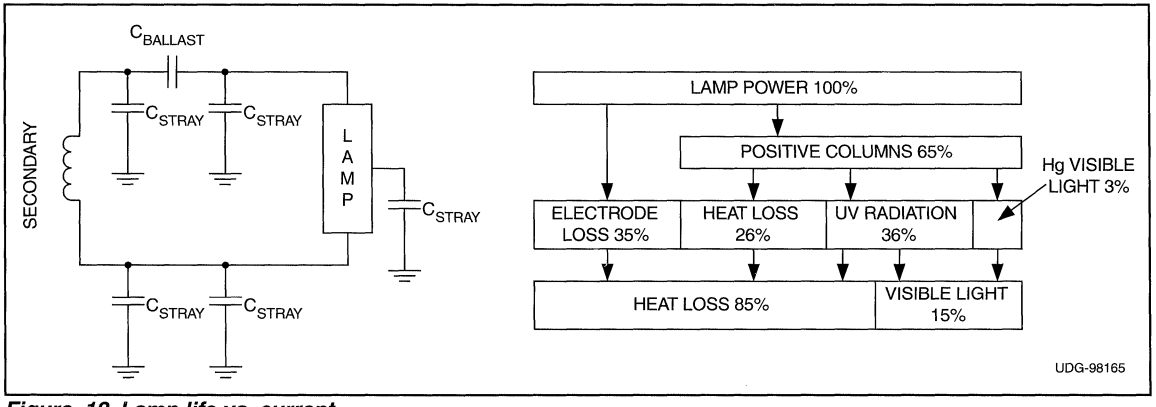


Figure 12. Lamp life vs. current.

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APPLICATION NOTES

Resonant Fluorescent Lamp Converter Provides Efficient and Compact Solution

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Abstract - **This paper describes a zero voltage switched (ZVS) resonant converter for driving cold cathode fluorescent lamps. Primarily intended for liquid crystal display (LCD) back-lighting, the circuit features minimal component count and size. A specially designed integrated circuit provides all control functions for a current fed push-pull ZVS converter, and also contains an auxiliary pulse width modulated (PWM) controller to develop a programmable supply voltage for the LCD. Analysis and simulation of the converter, and a complete circuit schematic are presented. The analysis and simulation results are validated by experimental circuit waveforms and critical performance parameters.**

Introduction

The proliferation of laptop and notebook computers places an ever increasing demand on display technology. High resolution and contrast are required to run today's graphics based programs, increasing the conflict between display performance, size and efficiency. The LCD with cold cathode fluorescent back lighting best satisfies this design requirement, however the lamp and its high voltage AC supply still remain the major contributor to battery drain.

The cold cathode fluorescent lamp (CCFL) requires 1-2 kV to fire. Sine wave drive is preferred to minimize RF interference and maximize lamp efficiency over time. Converter efficiency and size are extremely critical. These formidable requirements demand a highly efficient conversion topology and maximum circuit integration.

A zero voltage switched resonant topology will maximize efficiency by eliminating losses associated with charging parasitic capacitances to high voltages. This topology can be controlled using discrete circuitry. The most common implementation is a Royer oscillator modified to provide ZVS operation. While this at first appears to be a good solution, and is commonly used today, it suffers from several limitations.

High voltage DC to AC conversion is only part of the display supply. The average output current must be programmable for lamp intensity control, and the LCD requires a programmable low voltage supply for contrast adjustment. This additional circuitry, implemented discretely or with multiple ICs results in a large number of components, significantly impacting size and reliability. Synchronization is also preferred to eliminate beat frequency effects such as lamp intensity modulation, further complicating the design. Minimizing circuit complexity and bulk are best achieved through integration.

Cold Cathode Lamp Characteristics

The CCFL presents a highly nonlinear load to the converter as illustrated in fig. 1. Initially when the lamp is cold (inoperative for some finite time), the voltage to fire the lamp is typically more than three times higher than the sustaining voltage. The lamp characterized in fig. 1 fires at 1600V and exhibits an average sustaining voltage (V_{FL}) of 300V. Notice that the lamp initially exhibits a positive resistance and then transitions to a negative resistance above 1mA. These characteristics dictate a high output impedance (current source) drive to suppress the negative load resistance's effect and limit current during initial lamp firing. Since the ZVS converter has a low output impedance, an additional "lossless" series impedance such as a coupling capacitor must be added.

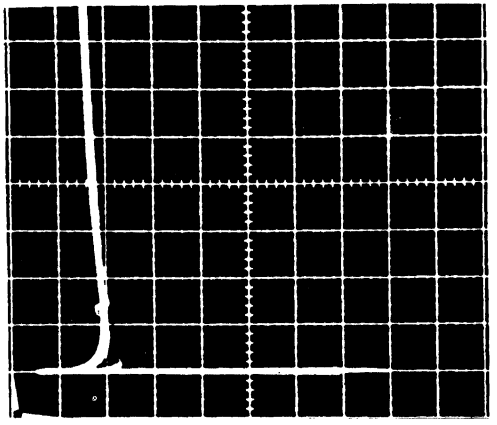

Fig. 1 Cold Cathode Lamp Current as a function of Voltage
Vertical: 2mA/div. Horizontal: 200V/div.

To facilitate analysis, the equivalent CCFL circuit shown in figure 2 is used. V_{FL} is the **average** lamp sustaining voltage over the operating range. The lamp impedance (R_{FL}) is a complex function but can be considered a fixed negative resistance at the sustaining voltage. Stray lamp and interconnect capacitance are lumped together as C_{FL}.

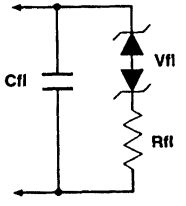

Fig. 2 CCFL equivalent circuit

ZVS Resonant Converter Topology

The current fed push-pull converter shown in fig. 3 is driven at it's resonant frequency to provide ZVS operation. The push-pull output MOSFETS (Q1 & Q2) are alternately driven at 50% duty cycle. Commutation occurs as V1 and V2 resonate through zero thereby insuring zero voltage switching. This virtually eliminates switching losses associated with charging MOSFET output and stray capacitance, and reduces gate drive losses by minimizing gate charge.

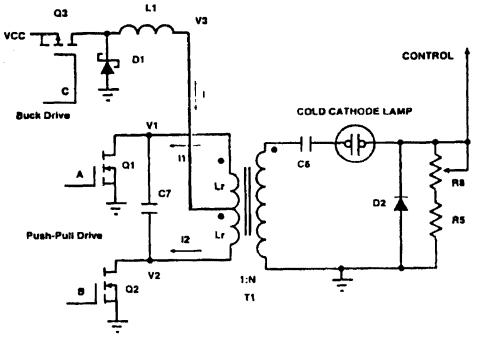

Fig. 3 Current Fed Push-Pull ZVS Resonant Converter

Current is supplied to the push-pullstage by a buck regulator (Q3). The control circuitry forces the average voltage across the current sense resistor (R8+R5) and rectifier (D2) to equal a reference voltage. Adjusted R8 varies the current and the lamp's brightness. The non-linearity introduced by D2 is insignificant since RS is adjusted for a particular brightness with no concern of the actual current level.

Winding inductance, L_R, and C_R, the combined effective capacitance of C7 and the reflected secondary capacitances make up the resonant tank. The secondary side of the transformer exhibits a symmetrical sine wave voltage varying from about 300V to 1500V peak. Capacitor C6 provides ballasting and insures that the converter is only subjected to positive impedance loads.

Waveform Analysis

Simulated converter voltage and current waveforms are shown in fig. 4. At time t_0, the primary current (I1 & I2) has reached it's peak value. The push-pull drain voltages (V1 & V2) have resonated to zero. The primary voltage (V3) has also resonated to zero, and through the control circuitry commutated Q1 off and Q2 on. The energy stored in L_R is also at it's peak. This energy is transferred from L_R to the effective resonant capacitance (C_R) during time t_0 to t_1, causing C_R's voltage to sinusoidally increase.

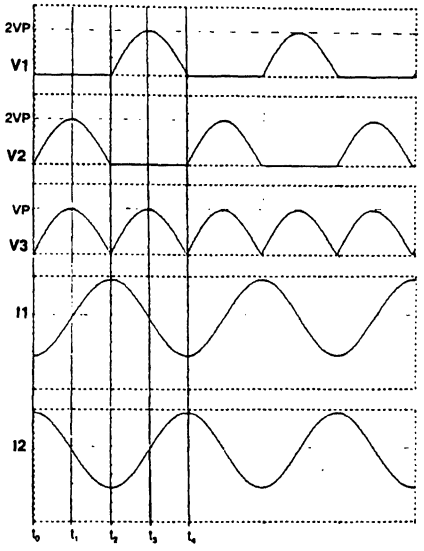

Fig. 4 Converter Voltage and Current Waveforms

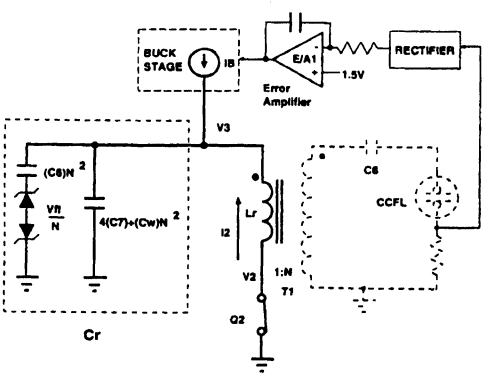

Fig. 5 Simplified converter model

At time t_1, all of the inductive energy in L_R has transferred to C_R, resulting in zero current through L_R and maximum voltage across C_R. From time t_1 to t_2, the energy transfers from C_R back to L_R, decreasing C_R's voltage while L_R's current increases.

The resonant current through L_R at time t_2 is equal and opposite to it's value at t_0. The reflected load current flows during the MOSFET on time, and is observed as a slight current amplitude asymmetry. The voltages at V1, V2, and V3 have resonated back to zero, causing the control circuitry to commutate Q2 off and Q1 on. The cycle continues symmetrically during the t_2 through t_4 interval, producing fully sinusoidal voltage and current waveforms.

Simplified Converter Model

The converter model shown in fig. 5, which is valid for one half cycle simplifies analysis by reflecting all impedances to the primary and eliminating the transformer. The differential voltage developed across the push-pull stage primary (V1-V2) exhibits twice the voltage excursion as the center-tap (V3). This reflects C7 to V3 through the turns ratio squared, resulting in 4(C7) at V3. The secondary winding capacitance is also reflected by the square of the turns ratio (n). Reflected winding capacitance is usually significant due to the high turns ratios typically employed. The buck stage operates in continuous current mode and is synchronized to the push-pull stage.

Lamp current is proportional to lamp intensity, and is used as the feedback variable. Buck current (I,) is the response variable, which in turn regulates the average push-pull primary voltage. The coupling capacitor's high impedance transforms the secondary voltage to lamp current.

Control Equations

Variable Summary:

C_R = Effective resonant tank capacitance
C_W = Secondary interwinding capacitance
F_L = Average lamp voltage
I_B = Average Buck output current
L_R = Primary Winding Inductance
n = Transformer turns ratio
Z_{sec} = Secondary impedance

Fig. 6 shows the buck output stage and forced output voltage waveform. The output voltage is a rectified sine wave, corresponding to the synchronous, resonant push-pull stage input

voltage. The inductor output configuration exhibits high impedance at the resonant frequency and averages the output voltage throughout the cycle. The buck output voltage as a function of time is:

$$V_{out}(t) = V_P \sin(\omega t)$$

Where the angular frequency is:

$$\omega = 2\pi f = \frac{2\pi}{2t_1} = \frac{\pi}{t_1}$$

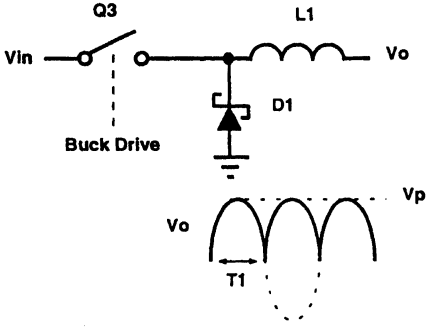

Fig. 6 Buck converter stage

The volts-second product across the inductor must be zero during steady state. Setting the on and off volt-second products equal and integrating gives the buck's transfer function:

$$V_{LR}(t_{on}) = -V_{LR}(t_{off})$$

$$\int_0^{t_{on}} V_{LR}dt = -\int_{t_{on}}^{t_1} V_{LR}dt$$

$$V_P = \frac{\pi}{2} Vi\ D \qquad (1)$$

This transfer function is identical to the familiar DC output buck transfer function, with the $\pi/2$ term accounting for peak versus average output voltage. As with the DC buck, primary voltage varies linearly with duty-cycle.

The peak primary voltage is also related to peak lamp current by:

$$V_P = \frac{(I_{FL(peak)})(Z_{sec}) + V_{FL}}{n} \qquad (2)$$

Setting (1) and (2) equal and solving for $I_{FL\ (avg)}$ expresses lamp current as a function of duty-cycle:

$$I_{FL(avg)} = \frac{DV_i\ n - \frac{2\ V_{FL}}{\pi}}{Z_{sec}} \qquad (3)$$

As expected from fig. 5, the lamp sustaining voltage, V_{FL} introduces a nonlinearity.

Buck output current is related to lamp current be equating input and output powers. The input power is:

$$P_{input} = \frac{1}{t}\int P dt$$

$$= \frac{1}{\pi/2}\int_0^{\pi/2} I\ V_P \sin(t)\, dt$$

$$P_{input} = \frac{2\ I_B\ V_P}{\pi}$$

The power to the load is:

$$P_{out} = V_{FL}\ I_{FL}\ (avg)$$

For analytical purpose, 100% power transfer is assumed:

$$P_{out} = P_{input}$$

$$V_{FL}\ I_{FL(avg)} = \frac{2 I_B V_P}{\pi}$$

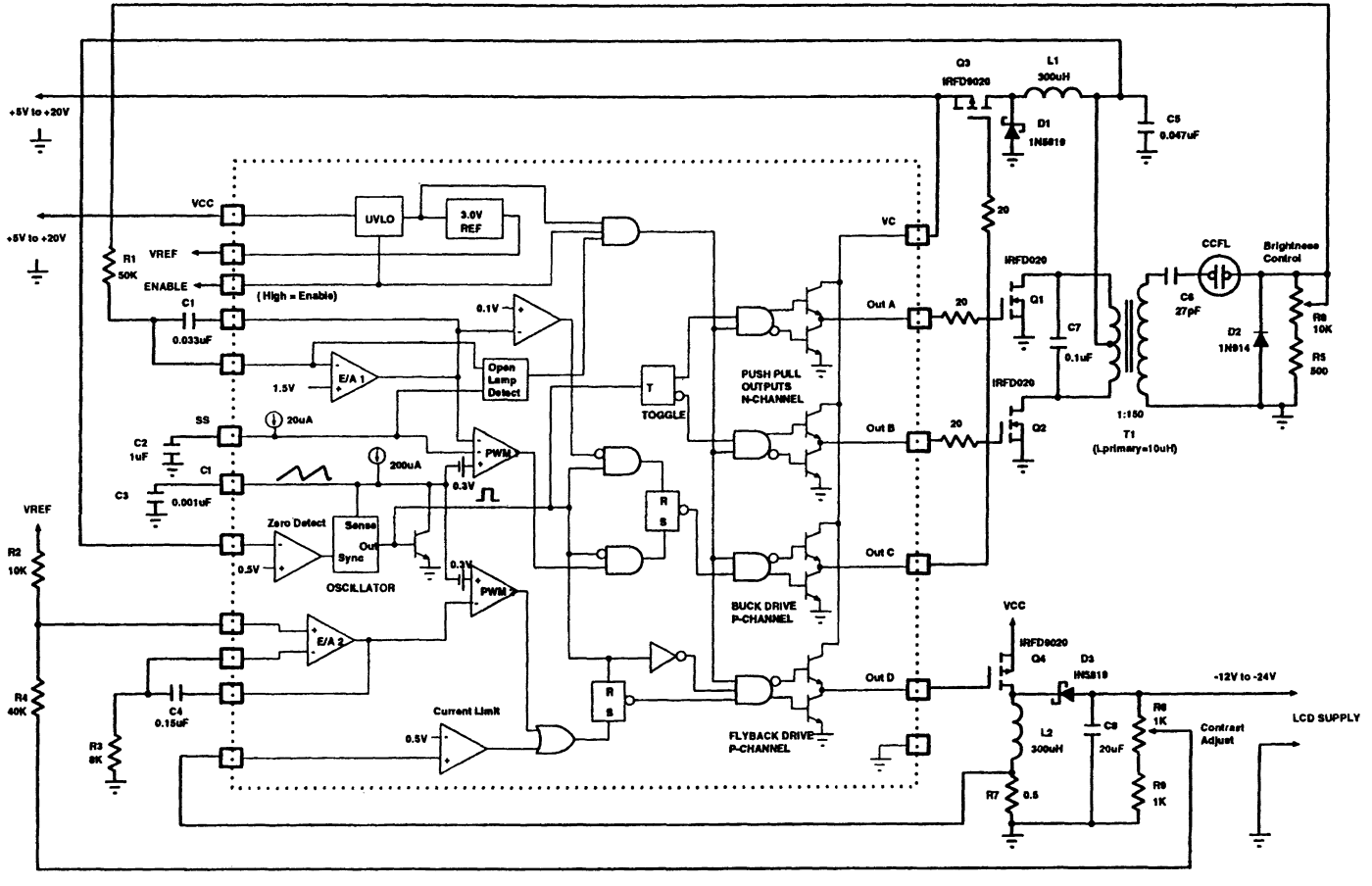

Fig. 7 UC3871 Application circuit

$$I_B = \frac{\pi I_{FL(avg)} V_{FL}}{2 V_P} \quad (4)$$

Substituting (2) for V_P in (4) gives the buck output current as a function of lamp current:

$$I_B = \frac{n V_{FL}}{Z_{sec} + \frac{V_{FL}}{\pi I_{FL(avg)}}} \quad (5)$$

The resonant frequency is approximately:

$$f_R \approx \frac{1}{2\pi\sqrt{L_R C_R}} \quad (6)$$

The nonlinearity introduced by V_{FL} causes the resonant frequency to vary with load. At very low lamp intensity the secondary voltage barely crests above V_{FL}. The effective resonant capacitance, C_R, is primarily the sum of C7 and C_W reflected to the primary. As the secondary voltage increase above V_{FL}, the reflected C6 value adds to the resonant capacitance, decreasing the frequency. The frequency range is approximated by assuming C6 has negligible effect at minimum lamp intensity, and fully adds to C_R at maximum intensity.

The peak resonant inductor current is the sum of the reflected load current from (5) and the resonant current:

$$I_{LR(peak)} = \frac{V_P}{Z_{tank}} + I_b \quad (7)$$

The tank impedance is determined by setting the resonant energy storage terms equal:

$$\frac{1}{2} L_R I^2 = \frac{1}{2} C_R V^2$$

Solving for V_R/I_R gives the tank impedance:

$$Z_{tank} = \sqrt{\frac{L_R}{C_R}} \quad (8)$$

Although relatively large currents are circulated through the resonant tank, the switches operate at low current levels. This is a direct result of the continuous resonant topology; the switches only must handle the energy that is removed by the load and lost in parasitics. The peak switch current is:

$$I_{sw(peak)} = I_b \quad (9)$$

The UC3871
A Completely Integrated Solution

Fig. 7 shows a complete application circuit using the UC3871 Synchronous Resonant Fluorescent lamp and LCD driver. The IC provides all drive, control and housekeeping functions to implement CCFL and LCD converters. The buck output voltage (transformer center-tap) provides the zero crossing and synchronization signal. The LCD supply modulator is also synchronized to the resonant tank.

The buck modulator drives a P-channel MOSFET directly, and operates over a 0-100% duty-cycle range. The modulation range includes loo%, allowing operation with minimal headroom. The LCD supply modulator also directly drives a P-channel MOSFET, but it's duty-cycle is limited to 95% to prevent flyback supply foldback.

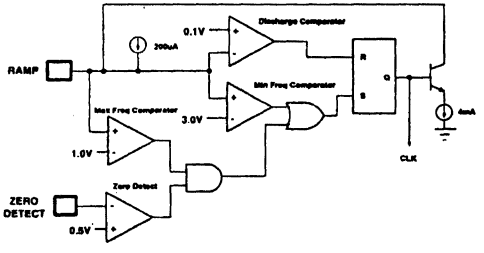

Fig. 8 UC3871 Oscillator Block Diagram

The Oscillator and synchronization circuitry are shown in fig. 8. The oscillator is designed to synchronize over a 3:1 frequency range. In an actual application however, the frequency range is only about 1.5:1. A zero detect comparator senses the primary center-tap voltage, generating

a synchronization pulse when the resonant waveform falls to zero. The actual threshold is 0.5 volts, providing a small amount of anticipation to offset propagation delay.

The synchronization pulse width is the time that the 4mA current sink takes to discharge the timing' capacitor to 0.1 volts. This pulse width sets the LCD supply modulator minimum off time, and also limits the minimum linear control range of the buck modulator. The 200µA current source charges the capacitor to a maximum of 3 volts. A comparator blanks the zero detect signal until the capacitor voltage exceeds 1 volt, preventing multiple synchronization pulse generation and setting the maximum frequency. If the capacitor voltage reaches 3 volts (a zero detection has not occurred) an internal clock pulse is generated to limit the minimum frequency.

A unique protection feature incorporated in the UC3871 is the Open Lamp Detect circuit. An open lamp interrupts the current feedback loop and causes very high secondary voltage. Operation in this mode will usually breakdown the transformer's insulation, causing permanent damage to the converter. The open lamp detect circuit, shown in fig. 9 senses the lamp current feedback signal at the error amplifiers input, and shuts down the outputs if insufficient signal is present. Soft-start circuitry limits initial turn-on currents and blanks the open lamp detect signal.

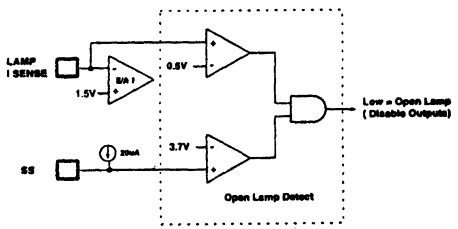

Fig. 9 Open Lamp Detect Circuit

Other features are included to minimize external circuitry requirements. A logic level enable pin shuts down the IC, allowing direct connection to the battery. During shut-down, the IC typically draws less than 100nA. The UC3871, operating from 4.5V to 20V, is compatible with almost all battery voltages used in portable computers. Under-voltage lockout circuitry disables operation until sufficient supply voltage is available, and a 1% voltage reference insures accurate operation. Both inputs to the LCD supply error amplifier are uncommitted, allowing positive or negative supply loop closure without additional circuitry. The LCD supply modulator also incorporates cycle-by-cycle current limiting for added protection.

Application Circuit Example

The application circuit shown in fig.7 resonates at approximately 50khz. This frequency allow a reasonable compromise between size and efficiency. This relatively low frequency by today's standards. results from high voltage insulation and spacing requirements, and practical limitations in reducing stray and interwinding capacitance. The half wave current sense signal is sensed by Error Amp 1 and averaged by integral compensation. The range of current control is 500µA to l0mA.

A flyback converter generates the LCD supply, outputting -12V to -24V to bias monochrome LCDs. Color displays normally require a positive bias voltage. Since this voltage typically must also be stepped up, a coupled inductor flyback is normally used.

Actual circuit waveforms agree with the spice simulated waveforms in fig. 4. Distortion caused by lamp nonlinearity is clearly visible at the operating extremes. At more nominal levels, the waveforms are more ideal, with only a small amount of observable distortion.

All of the following waveforms were taken at minimum and maximum lamp intensity to indicate worst case conditions. Nominal measured efficiency was 80%. Further improvement is possible with lower resistance magnetics and lower on resistance MOSFETs. Fig. 10 shows secondary output voltage, fig 11 shows lamp voltage, and fig. 12 shows lamp current. Notice that the lamp voltage is fairly constant with widely varying current. A frequency shift from about 48kHz to 57kHz is also observed over the lamp intensity range. The lamp current exhibits additional harmonics induced by it's nonlinearity. Push-pull MOSFET drain to source voltage is shown in fig. 13, and drain current is shown in fig. 14. The transformer center-tap voltage (buck output) is shown in fig. 15. All waveforms are sinusoidal, exhibiting minimal harmonic content.

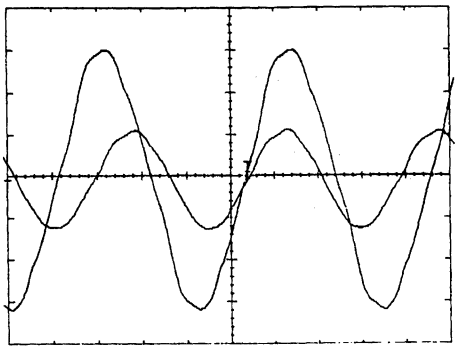

Fig. 10 secondary output voltage
vertical: 500V /div. Horizontal: 5µs/div.

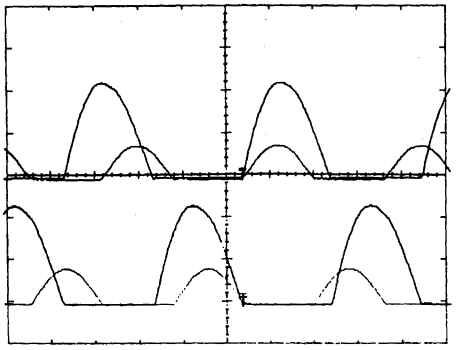

Fig. 13 Push-Pull MOSFET drain to source voltage
vertical: 10V /div. Horizontal: 5µs/div.

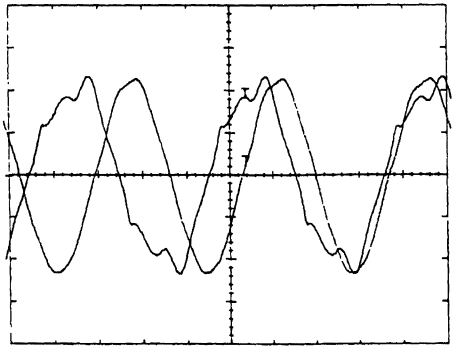

Fig. 11 lamp voltage
Vertical: 200V /div. Horizontal: 5µs/div.

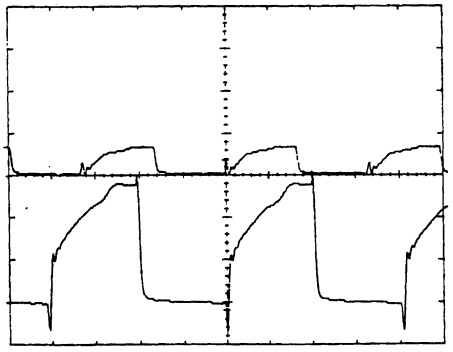

Fig. 14 Push-pull MOSFET drain current
Vertical: 200mA /div. Horizontal: 5µs/div.

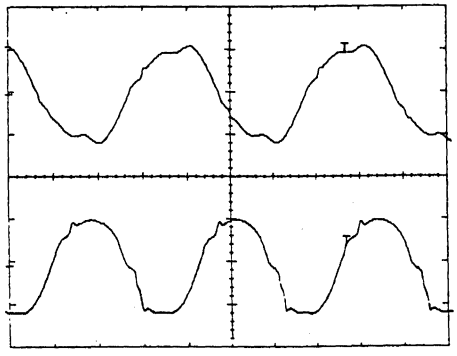

Fig. 12 Lamp current
Vertical: 10mA /div. Horizontal: 5µs/div.
500µA/div.

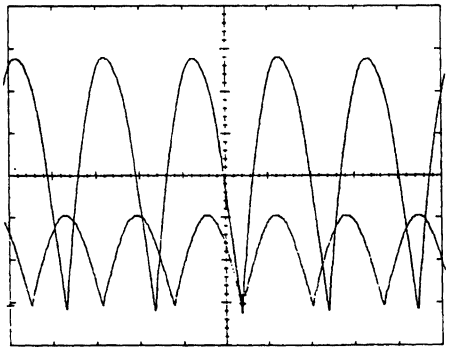

Fig. 15 Buck output voltage
Vertical: 200mA /div. Horizontal: 5µs/div.

Summary

The current fed push-pull ZVS converter efficiently develops high voltage, sinusoidal power for driving cold cathode fluorescent lamps. Design equations have been derived, and verified experimentally, simplifying application circuit design and analysis. The **UC3871** provides a complete solution for high performance back-light and LCD power supplies.

DIMMABLE COLD-CATHODE FLUORESCENT LAMP BALLAST DESIGN USING THE UC3871

ABSTRACT

This application note describes how to design a resonant cold-cathode fluorescent lamp converter and liquid crystal display (LCD) bias supply using the UC3871. A design method is presented and an example circuit is designed. Practical considerations regarding component selection and layout are discussed, and performance results are shown.

DESIGN CONSIDERATIONS

The UC3871 provides a complete power supply control solution for backlit LCDs that are typically used in laptop and notebook computers, and portable instrumentation. These applications require an adjustable high voltage AC current source to drive a cold cathode fluorescent lamp (CCFL) and an adjustable low voltage DC supply to bias the LCD. The UC3871 provides all control functions for these two supplies and also incorporates protection and synchronization circuitry. A low power shut-down input places the entire circuit into a very low current standby mode to reduce battery drain in portable systems and eliminate the need for a low-drop series switch.

The power circuitry illustrated in figure 1 consists of three sections:

1. A pulse width modulated (PWM) buck regulator to provide a variable, regulated voltage
2. A zero voltage switched (ZVS) resonant push-pull converter to transform the variable, regulated voltage to a high voltage AC output
3. A PWM flyback regulator to generate a variable DC voltage to bias an LCD

The buck and flyback regulators are synchronized to the ZVS push-pull converter, which free runs at its resonant frequency. Unitrode application note U-141 also covers the UC3871, along with further description and analysis of this topology and the application's requirements.

Most potential applications for the UC3871 are sensitive to both size and efficiency. EMI generation is also critical because only limited shielding is possible. The size/efficiency trade off is primarily in the magnetics, with the high voltage transformer by far the single most critical component. The design therefore must begin with an assessment of the performance and size goals, and their impact on the transformer design. In general, higher frequencies are preferred to minimize the size of the buck and flyback regulator magnetics, but excessively high frequencies will cause significant efficiency degradation.

DESIGN PROCEDURE

The ZVS resonant push-pull converter is designed first, and then the buck regulator and LCD bias flyback converter since both of these circuits are dependent on the push-pull converter. Resonant push-pull converter design requires an iterative approach because almost all of the variables are interdependent. A few initial variables come from the lamp and application specifications. These are normally the lamp starting voltage, operating voltage, and operating current, and the input supply voltage range. The desired resonant frequency is then chosen in order to calculate the remaining variables.

To help illustrate the design procedure, the following design example is presented which is typical of what a small computer would use for LCD power and back lighting. The application requirements are as follows:

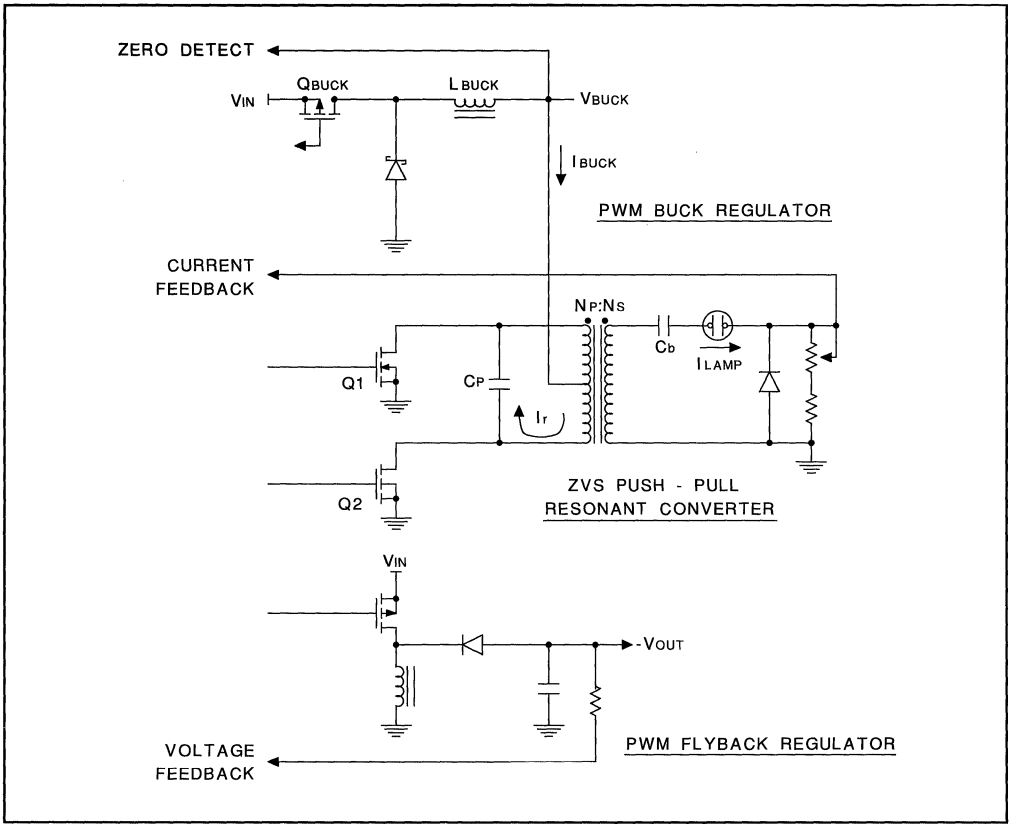

Figure 1. The power circuitry consists of three sections.

Input Voltage Range (Vin)	4.5V to 18V
LCD Bias Supply:	
Output Voltage (Vlcd)	-12V to -24V
Output Current (Ilcd)	25mA
Fluorescent Lamp Ballast:	
Starting Voltage (Vlamp)	900V (peak)
Operating Voltage (Vlamp)	350V (peak)
Operating Current (Ilamp)	0.5mA to 5mA (avg.)

The desired minimum resonant frequency is 50kHz so that the buck and flyback operating frequency will be at least 100kHz. At this frequency, switching losses will be low. Increasing the frequency will allow smaller magnetics, but efficiency will most likely suffer. The complete schematic of the design example circuit is shown in figure 2.

ZVS RESONANT PUSH-PULL CONVERTER

The minimum input voltage and maximum lamp starting voltage determine the minimum transformer turns ratio. After calculating the initial transformer parameters, the turns ratio should be checked to make sure that full load current can be developed at the minimum input voltage. The minimum turns ratio is then:

$$\frac{N_S}{N_P} \geq \frac{V_{START(PEAK)}}{\pi V_{INmin}} \qquad (1)$$

$$\geq \frac{900}{4.5\pi}$$

$$\geq 64$$

Note that this ratio relates the entire primary winding to the secondary. Sometimes the turns ratio is specified to relate one-half of the primary winding (end to center-tap) to the secondary.

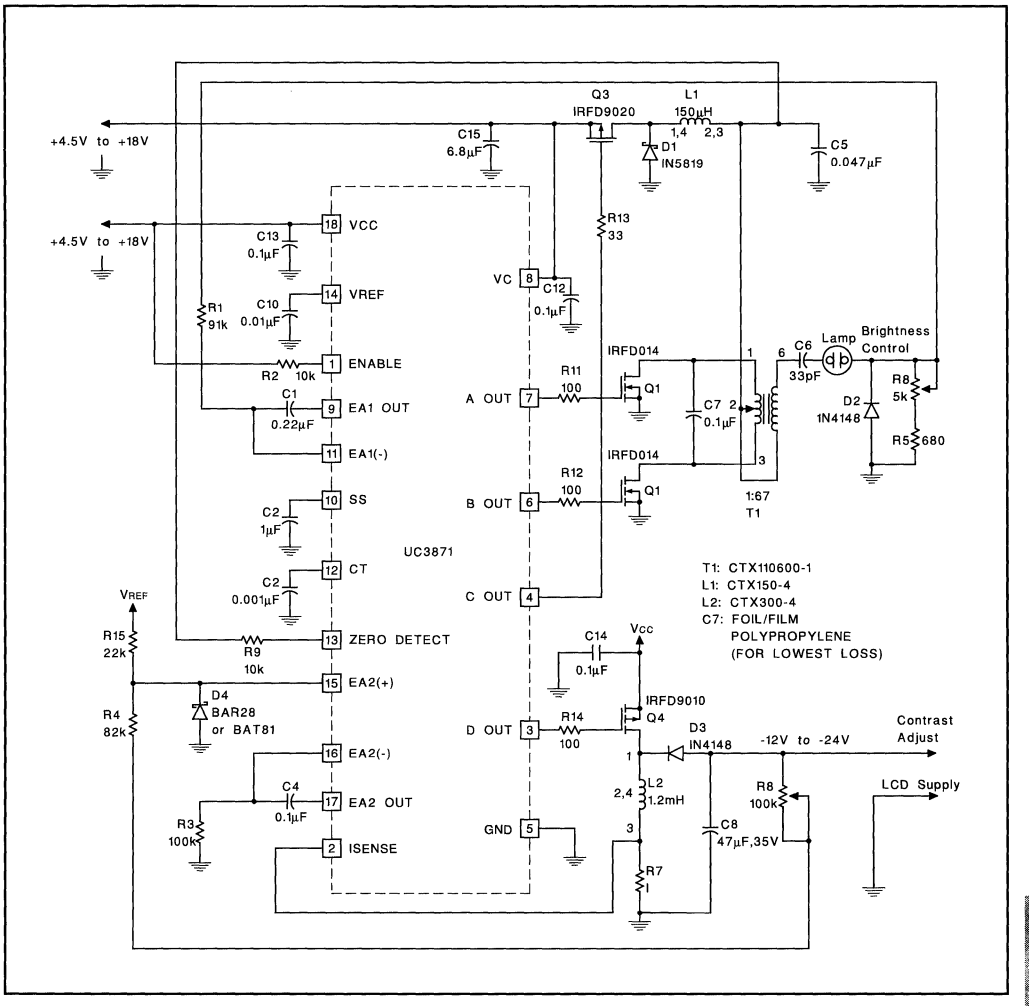

Figure 2. Complete circuit schematic.

A nominal ballast capacitor (Cb) value is calculated by setting the voltage across the ballast capacitor approximately twice the lamp sustaining voltage. This is an arbitrary relationship which serves as a starting point. Dropping a large voltage across the ballast capacitor voltage gives the converter a high output impedance and makes the converter relatively insensitive to the lamp's highly nonlinear impedance. Unfortunately, it also increases the circuit's losses. Tradeoffs between circuit size, distortion, and efficiency are governed by this component, so further iterations will usually result in a different final value. Setting the ballast capacitor's voltage equal to twice the lamp voltage at maximum current and minimum resonant frequency gives the value for Cb:

$$V_{CB} = \frac{I_{LAMP}}{2\pi F C_B} = 2V_{LAMP} \quad (2)$$

$$C_B = \frac{I_{LAMP}}{4\pi F V_{LAMP}}$$

$$= \frac{0.005}{4\pi(50 \bullet 10^3)(222)}$$

$$= 36pF$$

High secondary voltage and turns ratio result in poor coupling between the transformer's primary and secondary windings resulting in high leakage inductance. Capacitors across both the primary and secondary windings form two loosely coupled

parallel resonant circuits. To minimize output distortion, the independent primary and secondary resonant frequencies should be approximately the same. This requirement establishes a desired relationship between the primary (Cp) and secondary (Cs) capacitance:

$$C_P = \left(\frac{N_S}{N_P}\right)^2 C_S \quad (3)$$

$$= (64)^2 (36 \bullet 10^{-12})$$

$$= 0.15\mu F$$

The majority of the secondary capacitance comes from the series connected lamp and ballast capacitor. The lamp appears as an AC short circuit for much of the cycle, making the equivalent capacitance a little less than the ballast capacitor value. Distributed winding capacitance, stray PC board and lamp wiring capacitance contribute to the small secondary capacitance. Setting the load capacitance equal to the ballast capacitor value is therefore a reasonable initial estimate. Distributed transformer winding and stray capacitance are ignored for initial calculations. Parasitic capacitances have negligible effect on the primary capacitance since its value is several orders of magnitude larger than on the secondary.

With the independent primary and secondary resonant tank frequencies approximately equal, the secondary circuitry is reflected to the primary, allowing treatment as a single resonant tank. With both the primary and secondary resonant tanks set to the same frequency, the equivalent resonant capacitor (Cr) is simply twice Cp. The primary inductance is then calculated to give the desired resonant frequency:

$$L_P = \frac{1}{(2\pi F)^2 C_R} \quad (4)$$

$$= \frac{1}{(2\pi 50 \bullet 10^3)^2 (0.3 \bullet 10^{-6})}$$

$$= 34\mu H$$

Primary and secondary RMS currents are then calculated to determine maximum acceptable transformer winding resistances. The secondary current is mostly lamp current, although the currents to drive distributed winding and stray wiring capacitances are also factors. For now we will ignore these parasitic effects, since in most cases the additional loss they cause will not be enough to significantly alter the transformer design.

Each half of the primary winding sees an asymmetrical sinusoidal current which is the sum of the primary resonant current and the input current source from the buck regulator during one-half of the cycle. The primary voltage must be calculated first in order to determine the primary resonant current:

$$V_P = \frac{N_S}{N_P} V_S \quad (5)$$

$$= \frac{N_P}{N_S} \sqrt{V_{CB}^2 + V_{LAMP}^2}$$

$$= \frac{1}{64} \sqrt{(700)^2 + (350)^2}$$

$$= 12.2V(peak)$$

The primary resonant current is then:

$$I_R = \frac{V_P}{Z_P} \quad (6)$$

$$= \frac{V_P}{\sqrt{\frac{L_P}{C_P}}}$$

$$= \frac{12.2}{\sqrt{\frac{34}{0.15}}}$$

$$= 0.810A(peak)$$

The buck regulator current is calculated by equating input and output power while assuming 90% efficiency for the push-pull stage:

$$P_{IN} = \frac{P_{OUT}}{0.9} \quad (7)$$

$$= \frac{V_{LAMP(RMS)}\, I_{LAMP(RMS)}}{0.9}$$

$$= \frac{(248)(5.55 \bullet 10^{-3})}{0.9}$$

$$= 1.53W$$

The buck regulator sources current to the push-pull stage through the primary winding's centertap. The average voltage at this point is one-half of the total primary voltage. The average buck regulator output voltage is therefore one-half the average primary voltage calculated in (5):

$$V_{BUCK} = \frac{V_P}{\pi} \quad (8)$$

$$= \frac{12.2}{\pi}$$

$$= 3.88V\ (avg)$$

The buck output current is then:

$$I_{BUCK} = \frac{P_{IN}}{V_{BUCK}} \quad (11)$$

$$= \frac{1.53}{3.88}$$

$$= 0.394A$$

During the first half of the resonant cycle, one-half of the primary winding conducts the resonant current, while the other half of the primary winding conducts the sum of the resonant current and the buck regulator current. During the second half of the cycle the conditions reverse such that both halves of the primary conduct the same asymmetrical current 180 degrees out of phase from each other. A close approximation of the primary current is made by simply adding the average value of the buck output current to the peak resonant current for one-half of the cycle, and calculating the rms value as an asymmetrical sinewave:

$$I_{PRI} = \sqrt{\left(\frac{I_R}{2}\right)^2 + \left(\frac{I_R + I_{BUCK}}{2}\right)^2} \quad (12)$$

$$= \sqrt{\left(\frac{0.810}{2}\right)^2 + \left(\frac{0.810 + 0.394}{2}\right)^2}$$

$$= 0.725A(rms)$$

PUSH-PULL TRANSFORMER

All parameters necessary to design the transformer are now known and an initial design can be started. Optimal transformer design for this application is beyond the scope of this paper. The additional complexity of the resonant circuitry, along with the high output voltage and small required size present a significant mechanical design challenge. Any variable can be iterated since the ballast capacitor value was arbitrarily selected. Optimal design normally requires many design iterations.

Often the preceding analysis is done by a transformer manufacturer that specializes in resonant ballast design. A standard transformer from Coiltronics, Inc. [5], which is intended specifically for portable computer LCD back lighting was selected for the design example. Its specifications closely match the application's requirements. Selecting a standard transformer eliminated numerous iterations and reduced the design cycle considerably. The Coiltronics transformer has the following specifications:

CTX110600-1 specifications:

Primary Inductance	44mH
Ns/Np	67
Primary Resistance	0.160 ohms
Secondary Resistance	176 ohms

The CTX110600-1 employs a unique method of secondary winding termination. The secondary return lead terminates at the primary centertap, making it unnecessary to insulate it from the rest of the winding. Distributing the secondary across several sections of a multi-section bobbin also eliminates insulation between winding layers. The secondary current has negligible effect on the primary since its value is roughly two orders of magnitude smaller than the primary current. This connection scheme does add a small amount of asymmetry to the secondary voltage waveform, but again, this effect is negligible.

To design with an existing transformer, the equations are rearranged to calculate the nominal capacitor values, or the capacitor values are recommended by the transformer manufacturer. Some experimentation is usually necessary, regardless of how the initial paper design is done, to achieve the optimum circuit for a particular application.

BUCK REGULATOR

The ZVS push-pull converter's resonant frequency establishes the buck and flyback regulators' conversion frequency. Each time the push-pull converter's primary voltage crosses through zero, the UC3871's oscillator is reset. The design frequency for both the buck and flyback circuits is therefore twice the minimum push-pull resonant frequency.

The buck regulator provides a regulated, variable output voltage for the push-pull converter to reject input voltage variations and allow lamp brightness adjustment. Due to the absence of a large output capacitor, the buck regulator presents a high impedance to the push-pull converter at its resonant frequency. Neglecting the sawtooth ripple, the output inductor's current is nearly constant.

Inductor ripple current is greatest when the duty cycle and frequency are minimum. This occurs at maximum input voltage and lamp current, where the buck OFF time is maximum:

$$T_{OFF(MAX)} = \frac{1-D}{F_{MIN}} \left(1-\frac{V_{BUCK}}{V_{IN(MAX)}}\right) \quad (13)$$

$$= \frac{1}{10^5}\left(1-\frac{3.88}{18}\right)$$

$$= 7.84\mu s$$

To minimize inductor value, ripple current is normally 30% to 50% of the average value.

$$L > \frac{T_{OFF}\ V_{BUCK}}{I_{RIPPLE}} \quad (14)$$

$$> \frac{(7.84 \bullet 10^{-6})(3.88)}{(0.5)(0.394}$$

$$> 154\mu H$$

A Coiltronics part number CTX150-4 was selected for the buck inductor that has the following specifications:

Inductance	150µH
Resistance	0.175 ohms
Rated Current	0.72ADC

CONFIGURING THE CONTROL CIRCUITRY OSCILLATOR

The UC3871 contains a synchronizable oscillator internally configured to operate over a 3:1 frequency range. A 200µA current source is used to charge an external capacitor (Ct) from 0.1V to 3.0V. At the 3.0V threshold, a 4.0mA current sink discharges the capacitor back down to 0.1V. The zero detect input senses the transformer primary centertap voltage and indicates when the resonant tank voltage is crossing through zero. Under normal circumstances, the zero detect input will trigger the discharge circuit before the capacitor voltage reaches the 3.0V threshold, synchronizing the oscillator to twice the resonant tank frequency.

To improve noise immunity and prevent false triggering from comparator chatter, another comparator is used to lock out the zero detect input until Ct's voltage reaches 1.0V. The 3V maximum, 1V minimum peak oscillator amplitudes establish a 3:1 synchronization range. Ideally, the synchronization range should be centered around the resonant frequency range. A good starting point is to set the oscillator amplitude (Vct) to 2.2V at the minimum synchronization frequency, which is twice the minimum resonant frequency. The timing capacitor value is then:

$$C_T = \frac{10^{-4}}{F} \quad (15)$$

$$= \frac{10^{-4}}{10^5}$$

$$= 1.0nF$$

The resonant tank frequency must always be within the oscillator synchronization range to prevent severe output distortion and non-ZVS operation.

A 10k resistor in series with the zero detect input is recommended to protect against high voltages that occur during turn-off. The zero detect input is specified to withstand a maximum input current when driven from a high impedance source. A capacitor connected to the transformer center-tap limits the maximum voltage at turn-off by absorbing all of the inductive energy in the buck inductor when both of the push-pull MOSFETs turn off. This capacitor also attenuates noise and ringing which would otherwise be present at this node.

SOFT-START AND OPEN LAMP DETECT

The primary function of soft-start is to allow time for the lamp to strike and conduct the programmed level of current before enabling the open lamp detection circuitry. A 20µA current source charges an external capacitor (Css) when either the supply voltage exceeds the nominal 4.2V under-voltage lockout, or the IC is enabled. Once the external capacitor voltage exceeds 3.4V, the open lamp detect circuit is enabled. The soft-start time is normally determined empirically, since many factors such as minimum supply voltage and temperature influence the time it takes the lamp to strike. A 150ms soft-start was required to insure that the lamp started in the application example circuit. Once the soft-start time is determined, the capacitor value is calculated by:

$$C_{SS} = 5.9 \bullet 10^{-6}\ T_{SS} \quad (16)$$

$$= (5.9 \bullet 10^{-6})(0.15)$$

$$= 0.88\mu F \text{ (use} = 1\mu F)$$

An open lamp is detected by sensing that the current feedback loop has opened. During normal operation the current loop is closed, and the error amplifier inverting input is at 1.5V. If the lamp circuit either opens or shorts to ground, insufficient feedback voltage develops, and the inverting input voltage drops to a level determined by input offset current and radiated signal pickup. Input bias current limits the maximum feedback resistor value to 100k, with lower values providing greater margin at

the expense of requiring a larger compensation capacitor. Radiated signal pickup is a more complex problem, and is addressed later in the PC board layout considerations section.

LAMP CURRENT CONTROL LOOP

The UC3871 controls lamp intensity by closing an average current feedback loop around the buck regulator and push-pull resonant converter. Optimal compensation of this system is extremely difficult because of the complex output stage and load characteristics. High frequency response is dominated by a resonant double pole formed by the buck inductor and primary resonant and load capacitances reflected to the transformer center-tap. Typically, this double pole has a Q between 1 and 5, and occurs less than a decade below the resonant tank frequency unless an excessively large value is used for the buck inductor. Furthermore, the current feedback signal must be filtered sufficiently for correct PWM operation, requiring significant signal attenuation at the resonant tank frequency. These factors make it nearly impossible to cross the loop over above the output stage's double pole.

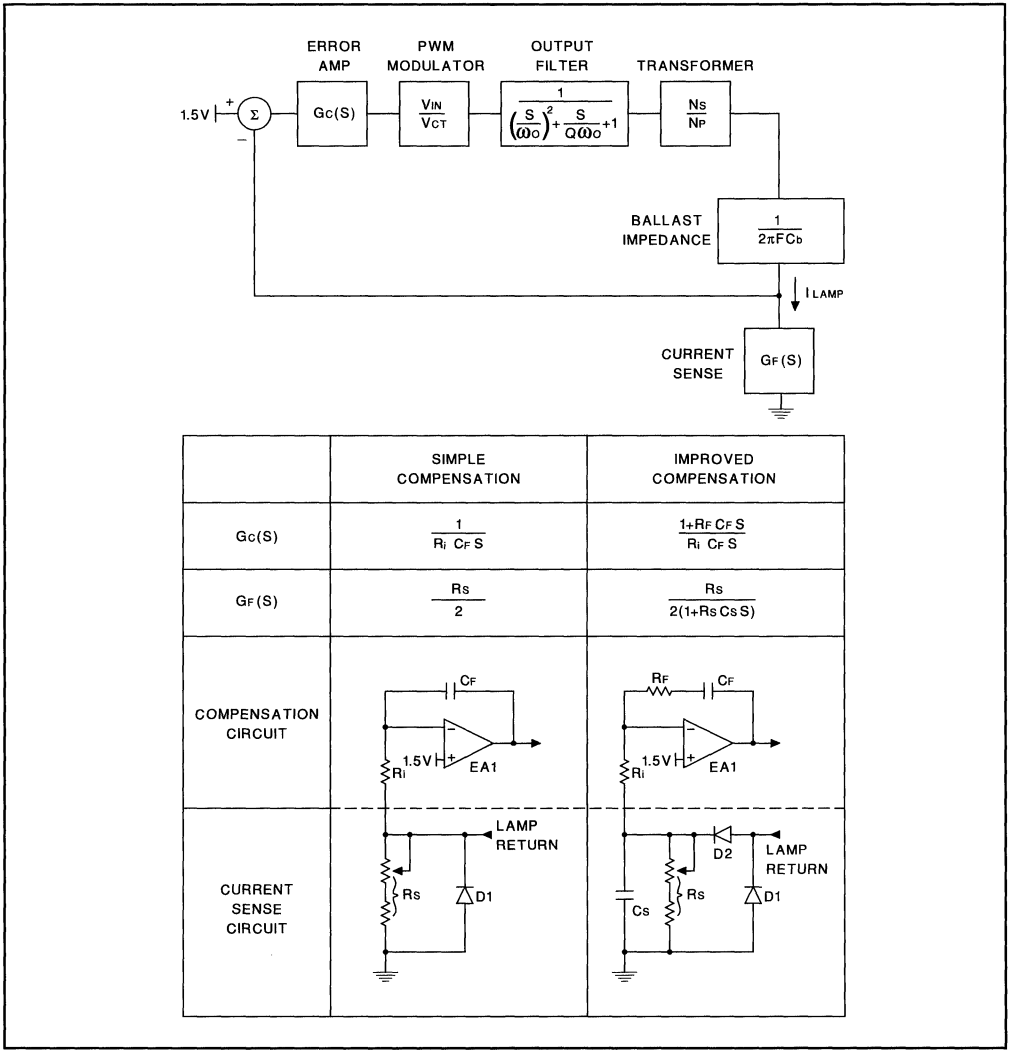

Figure 3. Control loop block diagram.

Below the double pole the power stage gain is flat. The simplest way to compensate the loop is to introduce a low frequency dominant pole that sets the unity gain crossover frequency well before the output filter double pole. This pole also sufficiently filters the half-wave rectified current feedback signal for proper PWM operation. The design example circuit shown in figure 2 employs this compensation technique, which requires a minimal number of components. Figure 3 shows the circuit's control loop block diagram. With the unity gain frequency set well below the resonant double pole, higher frequency effects caused by capacitor ESR and transformer leakage inductance can be ignored.

Three of the blocks exhibit gain variation with input or load changes. Most notable is the current sensing resistor, which in a typical application will cause a 25dB to 30dB gain change over the lamp current adjustment range. The ballast capacitor (Cb) is treated as a fixed impedance determined by the converter's resonant frequency, but since the resonant frequency varies about 20% in an actual application, the ballast impedance varies inversely by the same amount. The modulator gain is directly proportional to frequency since the PWM ramp amplitude (Vct) varies inversely with frequency, and to a first order, cancels the ballast impedance variation. The more dominant modulator gain variation however, is from the input supply voltage (Vin), which may vary more than 3:1.

The output filter resonant frequency is determined by the buck inductor value and the equivalent value of the primary resonant, output ballast, and output stray capacitances reflected to the buck regulator output:

$$\omega_O = \sqrt{L_{BUCK}\, C_{EQ}} \qquad (17)$$

$$C_{EQ} \approx 4C_P + \left(\frac{N_S}{N_P}\right)^2 C_B$$

$$\approx 8C_P$$

Output filter Q is the ratio of the resonant tank impedance to the effective series damping resistance:

$$Q = \frac{\omega_O L}{R_{SERIES}} \qquad (18)$$

The effective series resistance is the sum of all power circuit resistances reflected to the buck regulator output, plus the reflected load resistance transformed to its effective series value (Rseries). With every effort made to minimize series resistance for maximum efficiency, the reflected load term dominates.

$$R_{SERIES} \approx \frac{V_{BUCK}^2}{1.1\ P_{OUT}}\ (\text{ohms}) \qquad (19)$$

Output filter Q is greatest at minimum lamp current. Gain peaking at the filter resonant frequency is then:

$$G_{PEAK} = 20\ \log Q_{MAX}\ (\text{dB}) \qquad (20)$$

The maximum unity gain crossover frequency is typically set nearly a decade below the output filter resonant frequency to insure adequate gain margin. Loop gain (and crossover frequency) is greatest at maximum input voltage and minimum current. At minimum input voltage and maximum lamp current, the unity gain crossover frequency may decrease two decades or more. Fortunately, wide bandwidth and good transient response are not required in most applications.

The example circuit's output filter has a maximum Q of 3, and a resonant frequency of 13kHz. The maximum unity gain crossover frequency is 1.5kHz, giving a worst case gain margin of about 9dB.

IMPROVED LOOP COMPENSATION CIRCUIT

Some applications require quick transient response to prevent lamp flicker from input voltage disturbances. Systems which have poor input supply regulation, particularly those with transient loads or a pulsed current battery charger are examples of such applications. With the typical UC3871 circuit, lamp current is adjusted by varying the closed loop gain. This causes the unity gain crossover frequency to decrease one decade for each 20dB increase in lamp current.

The control loop block diagram in figure 3 shows an improved current sense and loop compensation scheme that makes the unity gain crossover frequency insensitive to lamp current adjustment. A capacitor (Cs) connected in parallel with the current sense resistor forms a pole that varies directly with the current sense gain. This configuration provides variable low frequency gain for lamp current adjustment with fixed high frequency gain for constant loop crossover frequency.

This pole can theoretically provide acceptable loop compensation with a fixed error amplifier gain, but the required value for Cs would be much to large for a practical circuit. Adding a pole-zero pair to the error amplifier allows for an acceptable Cs value and provides high DC gain by maintaining a pole at the origin. The current sense pole (1/(RsCs)) and

the error amplifier zero (1/(RfCf)) are placed at the control loop's unity gain crossover frequency with Rs set to its minimum value.

LCD BIAS SUPPLY FLYBACK REGULATOR

The design procedure for the flyback converter is not given here since it differs little from a conventional power supply application. The only unique condition is that the conversion frequency varies with the push-pull converter's frequency. As with the buck converter, the initial design frequency is twice the minimum resonant frequency (the design example's buck and flyback regulator's minimum frequency is 100kHz). At the lowest lamp brightness, the frequency will typically increase 15% to 25%, minimally influencing the flyback converter's operation.

For the design example, the flyback converter is operated in the continuous inductor current mode. For most power supply applications, this mode of operation is avoided because of the poor closed loop bandwidth dictated by the right-half plane zero in the transfer function. Continuous mode operation does result in lower power stage loss however, and since for this application power loss is usually more critical than dynamic response, it is normally the preferred mode of operation.

The minimum component compensation circuit shown in the design example schematic employs a dominant pole to cross over the loop before the output stage's resonant double pole. Output voltage overshoot at power-up can be significant with this configuration if the error amplifier's integration capacitor is allowed to fully charge as the output voltage slews to its nominal value. This large signal problem is exacerbated by the ground referenced error amplifier configuration, which only allows a small discharge current to be developed.

For the design example, a 0.1μF integration capacitor is used although a value nearly ten times smaller will provide maximum loop bandwidth. The 0.1μF capacitor charges slowly during power-up, and eliminates overshoot by soft-starting the supply. A shottky diode (BAT81) is used to clamp the non-inverting error amplifier input to prevent it from phase inverting and latching up the control loop. This diode should have a forward drop less than 0.5V at room temperature.

IMPROVED FLYBACK COMPENSATION

As with the lamp driver circuit, there are applications that require better transient response than is achievable with dominant pole compensation. A simple alternative technique, shown in figure 4, is to cancel one of the output stage's resonant poles by a zero in the compensation circuitry, and cross the loop over at about 1/4 the minimum right-half plane zero frequency. This technique does result in lower DC gain than the dominant pole circuit used in the design example, but offers much better large signal behavior and a decade or more increase in loop bandwidth. Another pole-zero pair can be added to improve DC load regulation and input line rejection, although this additional complexity appears unnecessary.

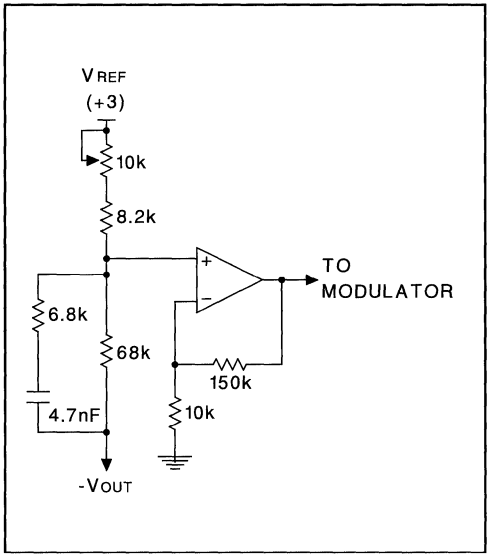

Figure 4. Improved flyback regulator compensation.

Discontinuous inductor current operation is also an option to significantly improve transient response if a small decrease in efficiency is tolerable. Discontinuous mode compensation is illustrated in the following positive output, coupled inductor flyback circuit.

POSITIVE OUTPUT VOLTAGE FLYBACK REGULATOR

A positive output LCD bias supply circuit is more complicated than the negative output, because the output voltage can be greater or less than the input voltage. This eliminates both buck and boost circuits, and makes the coupled inductor flyback converter a good choice for this application. Discontinuous inductor current operation is employed in the circuit shown in figure 5, allowing simple compensation and excellent transient response.

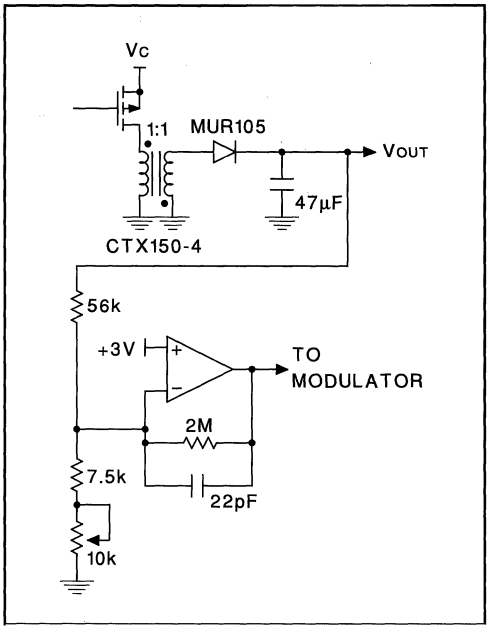

Figure 5. Positive output coupled inductor flyback regulator.

Since the output MOSFET is relatively large, and has significant output capacitance and avalanche energy capability compared to the current it must switch, a clamp or snubber network is not required to insure reliable operation. Snubbing may be necessary to reduce EMI however. This circuit can, of course be operated with continuous inductor current for a small improvement in efficiency. The compensation circuitry would then be similar to the previous flyback regulator examples. Flyback regulator and control loop design is covered in the references.

PRACTICAL CONSIDERATIONS

MEASUREMENT TECHNIQUES

The combination of low power, high voltage, and high frequency AC present a unique challenge in determining circuit efficiency. An absolute efficiency measurement is important because it allows meaningful comparison with work done by others. Since an electrical efficiency measurement removes lamp performance from the equation, it is the most universal performance index.

For an actual application however, high output light intensity for a given input power is the actual design goal. Once reasonable electrical efficiency is achieved, further circuit refinement should be based on relative light intensity efficiency improvements using the same lamp and test setup.

To measure electrical efficiency, extreme attention to measurement technique and equipment is required. Output current is relatively easy to measure with a current sense resistor in series with the lamp return to ground. For the design example circuit shown in figure 2, a small resistor can be added in series with R5 and D2 to measure both half cycles of the lamp current.

To measure lamp voltage, a 100X or 1000x oscilloscope probe with low input capacitance and good high frequency accuracy is required. Accurate AC probe calibration is critical in achieving a meaningful measurement. At low lamp current, both the lamp current and voltage exhibit clean sinusoidal waveforms with minimal harmonic distortion. The product of the RMS lamp current and voltage then give an accurate measurement of the output power. As current is increased, the lamp's nonlinearity becomes apparent, as significant distortion is observable in the lamp voltage waveform. The product of the RMS lamp current and voltage will no longer yield an accurate output power measurement.

A true RMS measurement that is insensitive to waveform shape is made by taking the average product of the instantaneous lamp voltage and current. Many digital oscilloscopes provide this function with reasonable accuracy. The accuracy of this technique can be further improved by calibrating to a known sinusoidal source.

EFFICIENCY OPTIMIZATION

Most of power lost in the lamp driver circuit is dissipated in the transformer, inductor, MOSFETs, primary resonant capacitor, buck regulator diode, and the UC3871. Although the output ballast capacitor (Cb) dissipates little power, its value greatly influences the performance of the circuit. Consider the effect of increasing Cb such that the secondary voltage drops 10%. The transformer's flux density and primary resonant current decrease 10%, reducing both transformer core and winding losses. Both of these losses are exponential, so the power savings can be significant. Smaller transformer losses decrease the input power required, reducing the current through, and the power lost in the other power handling components.

Of course the ballast capacitor cannot be continually increased, as waveform distortion will quickly become unacceptable, but there is an optimal value for a particular application that is best deter-

mined experimentally. The same is true for the primary resonant capacitor, where a decrease in value will increase the resonant frequency, and decrease the resonant current and associated losses. Again, there is an optimal value that yields the best distortion/efficiency tradeoff for a particular application.

The losses contributed by the other power components are more easily determined, as circuit operation is affected minimally by their variation. For lowest loss, MOSFETs are selected for minimal combined conduction and gate drive loss. Bigger is not necessarily better! Logic-level threshold devices are required for high efficiency at low input supply voltages, although standard threshold devices will usually function with reduced efficiency down to about 6V.

The primary resonant capacitor, Cp conducts the primary resonant current and must have low losses for good circuit efficiency. A monolithic ceramic capacitor, and several film capacitors from Electronic Components, Inc. [6], were evaluated to determine the relative performance differences among various dielectric and construction techniques. Polypropylene film/foil capacitors exhibit the lowest losses. Metalized polypropylene capacitors are usually smaller than foil/film construction, but will result in about a 1 percent decrease in efficiency.

Further size reduction is possible with polycarbonate or polyester capacitors, but efficiency will be about 1 percent to 3 percent lower than the foil/film polypropylene units. Since the capacitor value is too high for an NPO dielectric, ceramic capacitors must be avoided. The dissipation factor of Z5U and X7R ceramics is much too high for reasonable efficiency. A Z5U monolithic ceramic reduced efficiency more than 12% in the test circuit!

Separate bias (Vcc) and collector (Vc) supply inputs are provided by the UC3871 to take advantage of its ability to operate down to 4.5V. Supplying Vcc from a switching regulated supply while operating the rest of the circuit directly from the battery typically saves from 30mW to more than 100mW.

The buck inductor's winding resistance will dissipate significant power if its winding resistance is excessive. Minimum inductor values are therefore usually preferred to maintain reasonable size. This results in high ripple current that can lead to high core loss. Like all the other power components, every source of dissipation must be investigated and analyzed to squeeze maximum efficiency from the converter.

PC BOARD LAYOUT CONSIDERATIONS

As with all switching regulators, PC board layout is critical. The circuitry should be as compact as practical, particularly in the power stage areas that conduct pulsed current or high voltage. EMI generated by high di/dt is minimized by keeping the pulsed current loops as small as possible. For example, the buck regulator MOSFET and rectifier should be as close together as possible. A low impedance bypass capacitor (a 6.8µF tantalum was used in the application circuit) should also be connected directly between the MOSFET source and the rectifier anode.

The lamp's high operating voltage, and poorly shielded leads and terminals are a potential source of radiated EMI. A significant benefit of the sinusoidal voltages and currents inherent to a fully resonant power stage is the comparatively low voltage and current slew rates. Some high frequency harmonics are present due to distortion and conducted noise received from the buck and flyback regulator power stages, although these are normally very small.

Shielding is normally an effective technique for attenuating EMI generated by high dv/dt nodes, but the performance tradeoffs with the high voltage ballast circuity can be misleading. Shields (or ground planes) increase the capacitive loading on the circuit, but the shield itself dissipates negligible power. When a shield is added however, circuit efficiency will drop because the additional load capacitance will increase the resonant current, just as if the primary resonant capacitance were increased. This effect is minimized by making high voltage traces as short as possible.

Loss due to leakage current in the high voltage section is also possible, particularly as the assembly ages and the PC board surface becomes contaminated. Milling slots in the PC board is a good way to get sufficient creapage distance between the high voltage traces and the rest of the circuitry while maintaining a compact layout.

Another important consideration in the high voltage area is the length and routing of the return lead and PCB trace connecting to the current sense circuitry. If a fault opens the lamp circuit, the error amplifier will command maximum secondary voltage in an attempt to keep the current loop closed. The stray capacitance between the high voltage circuitry and the return lead may conduct sufficient current to keep the loop closed, particularly at low command current and maximum input voltage. This condition will prevent open lamp detection and severely over stress the circuitry.

This problem is avoided by keeping the lamp return path as short as possible, with the current sense resistor placed as close to the lamp as practical. Traces between the current sense resistor and the UC3871 are insensitive to noise and switching harmonics since the signal is DC at this point. Ideally, the majority of the return path length is placed between the current sense resistor and the feedback resistor.

Keeping the high voltage path as short as possible helps by reducing the radiated signal. Shielding around the high voltage area also reduces the radiated signal, but may not be practical in many application. The dimming range should be set no wider than necessary since high current sense resistor values increase sensitivity to this problem. The circuit described in the following section for wide dimming range applications is significantly more robust in this regard, and should be considered when packaging constraints force non-ideal layout.

WIDE DIMMING RANGE APPLICATIONS

Most cold cathode fluorescent lamps function acceptably down to about 1/20 of their rated current. Below this level, they begin to illuminate unevenly across the tube. This "thermometer" effect is caused by parasitic capacitive current, and is heavily influenced by shielding and grounding. Wide dimming ranges are accommodated without uneven lamp brightness by driving the lamp at maximum current, and pulse width modulating the current on and off at low frequency.

Figure 6 shows modifications to the standard application circuit for low frequency PWM control. A fixed current sensing resistor sets the maximum lamp current. An external PWM signal drives the inverting error amplifier input through a series diode and resistor. The input resistor value is chosen to force the lamp current to zero when the PWM input is pulled high. These modifications

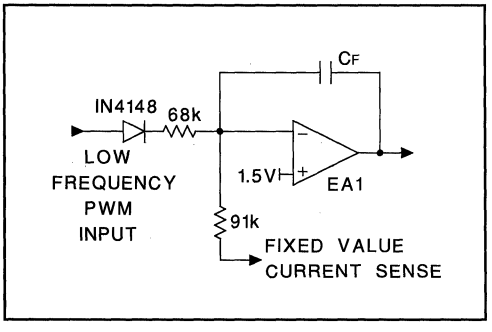

Figure 6. Low frequency PWM control for wide dimming range aplications.

where made to accept a 100Hz PWM signal from 5V CMOS logic through a 1N4148 and a 68k resistor. A 680 ohm current sense resistor set the continuous lamp current at approximately its rated value. Fixed current gain allowed the compensation capacitor (Cf) to be reduced to 4.7nF for more optimum loop performance.

With no further modifications, the circuit maintained uniform lamp intensity over a current range of more than a 500:1. Operation was linear with negligible effect from input voltage variation, down to about 1% of rated current. Below 1%, the current rise and fall time became significant, limiting the practical open loop dimming range to about 100:1. An accurate, stable dimming range greater than

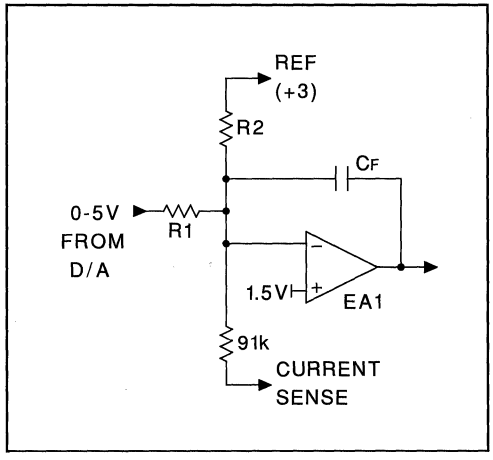

Figure 7. External voltage command interface.

500:1 can be achieved with the addition of a low bandwidth outer current or lamp intensity feedback loop.

DIGITAL LAMP CURRENT CONTROL

The preceding technique for wide dimming range applications is also the best method for digital lamp intensity control. A 100Hz PWM signal generated by a microprocessor combines excellent dimming range with single line digital control. An alternative approach is to use the circuit shown in figure 7, where a D/A injects a command signal into the control loop. This technique provides excellent performance for less than 20:1 dimming ranges, but unfortunately it also defeats the open lamp detect circuit. A third approach is to replace the current sense potentiometer with a digital pot or a multiplying D/A converter, but these devices can usually only handle low current.

BIPOLAR TRANSISTOR OUTPUT STAGES

When cost is more critical than performance, PNP bipolar transistors can be substituted for the P-channel MOSFETs. High gain, low saturation devices such as the Zetex [7] ZTX788B (3A, 20V PNP) perform quite well for the buck regulator when the input voltage is low. A PNP can also be used for the flyback converter, but at a greater efficiency reduction than the buck regulator because it requires a higher voltage device and has greater switching losses.

Simple high speed base drive is implemented by choosing a base resistor for sufficient drive at the minimum input voltage. A small capacitor in parallel with the base resistor improves switching speed. Bipolar NPNs in place of the N-channel MOSFETs are generally a poor cost/performance tradeoff, but can be used if performance is secondary.

CIRCUIT DISABLE

The UC3871 provides an enable input to shut down both converter power stages and put the control circuitry in a very low current standby mode. Applications that require disabling each converter independently require a different approach. The flyback section can be disabled by either pulling the current sensing input above its 0.5V threshold, or by pulling the inverting error amp input above Vref to force the duty cycle to zero.

The ballast converter is a little more difficult to disable because of the open lamp detect circuitry. Any technique that breaks the feedback loop, such as grounding the error amp output, will cause the converter to latch off. Grounding the soft-start input will not bring the duty cycle zero, and therefore will not completely disable the converter. The best shut down method is to source enough current into the inverting error amp input to force its output to ground. This saturates the loop, causing the duty cycle to go to zero without falsely indicating an open lamp condition.

MULTIPLE LAMP CIRCUITS

The ballast circuit is easily modified to drive two or more parallel lamps by splitting the ballast capacitance into two or more capacitors of equivalent value. Because of lamp mismatch, the dimming range must normally be less than single lamp circuits. Additionally, a higher ballast capacitor voltage than is optimum for a single lamp may be required to insure that both lamps start.

DESIGN EXAMPLE PERFORMANCE AND WAVEFORMS

Figures 8 through 10 show typical ballast waveforms from the design example (figure 2) delivering 1.0W into a lamp from a 10V input supply. Figure 8 shows the primary voltage waveforms. Note that the center-tap waveform is one-half the amplitude of the push-pull waveforms, and that no distortion or ringing is evident at the cusps of the waveform.

Figure 9 shows the primary current waveforms and the differentially sensed transformer primary voltage waveforms. The transient steps at the peaks of the primary current are from the push-pull switches turning on, which allow input (reflected load) current to conduct in addition to the resonant current.

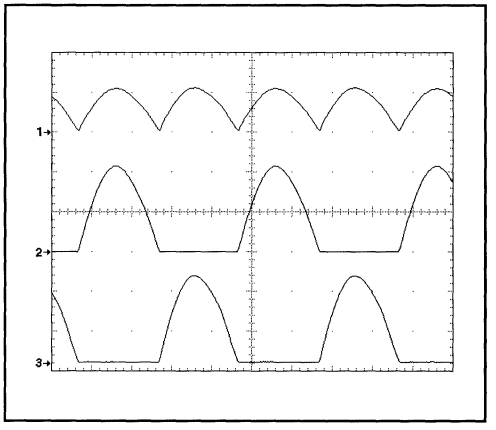

Figure 8. 1. Centertap voltage 5V/div
2. Q1 drain voltage 5V/div
3. Q2 drain voltage 5V/div
Horizontal: 5µs/div

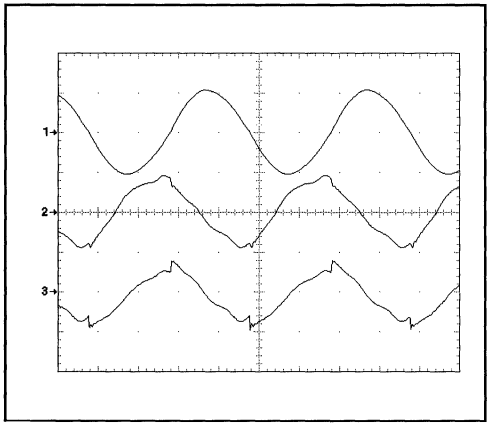

Figure 9. 1. Differential primary voltage 10V/div
2. Primary resonant capacitor current 0.5A/div
3. Primary transformer winding current 0.5A/div
Horizontal: 5µs/div

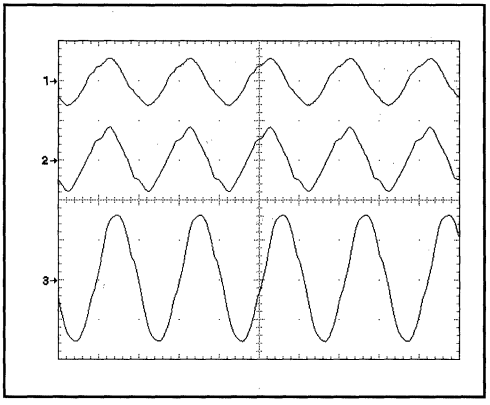

Figure 10. 1. Lamp current 10mA/div
2. Lamp voltage 500V/div
3. Transformer secondary voltage 500V/div
4. Horizontal: 10µs/div

Figure 10 shows the secondary voltage and current waveforms. Lamp current and voltage are in phase indicating that the lamp appears resistive. These waveforms lead the secondary voltage waveform because of the capacitive coupling. Distortion in the lamp voltage waveform is caused by lamp impedance nonlinearity, which also causes some distortion in the secondary voltage waveform.

Figures 11 and 12 illustrate circuit efficiency with varying input supply voltage and output power. In both cases a separate 5V supply powered Vcc, since this is available in most applications. Figure 11 shows the efficiency of the complete converter over an input supply range of 5.5V to 18V. For this plot, the lamp power was 1.0W, and the LCD bias power was 0.324W (18V across 1k). The sudden decrease in efficiency at low input voltage is from insufficient gate drive voltage. This efficiency drop can be eliminated by using logic level MOSFETs.

The efficiency curve in figure 12 was taken with the flyback converter output disabled, although the control circuitry was still active. The lamp power was then varied from 0.2W to 1.9W while keeping the supply voltage at 10V. Above about 3/4W, efficiency was greater than 80%. At light load, the control circuit and gate drive losses became significant, and efficiency was greatly reduced.

SUMMARY

The UC3871 provides a complete power supply control solution for backlit LCDs. A design method illustrated with a circuit example has been presented, along with alternate configurations and loop compensation techniques. Example circuit waveforms and efficiency graphs show that the UC3871 provides a simple, yet high performance solution.

References:

1. M. Jordan, J. O'Connor, "Resonant Fluorescent Lamp Converter Provides Efficient and Compact Solution", Unitrode application note U-141
2. L. Dixon, "Closing the Feedback Loop", Unitrode Power Supply Design Seminar Manual SEM-700
3. L. Dixon, "The Right-Half-Plane Zero - A Simplified Explanation", Unitrode Power Supply Design Seminar Manual SEM-700
4. L. Dixon, "Switching Power Supply Topology Review", Unitrode Power Supply Design Seminar Manual SEM-700
5. Coiltronics, Inc., Boca Raton, Florida, 561-241-7876
6. Electronics Concepts, Inc., Eatontown New Jersey, 908-542-7880
7. Zetex, Inc., Commack, New York, 516-864-7630

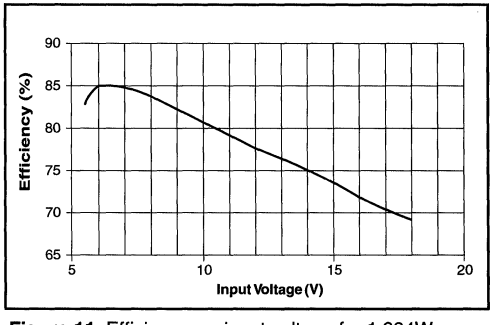

Figure 11. Efficiency vs. input voltage for 1.324W output.

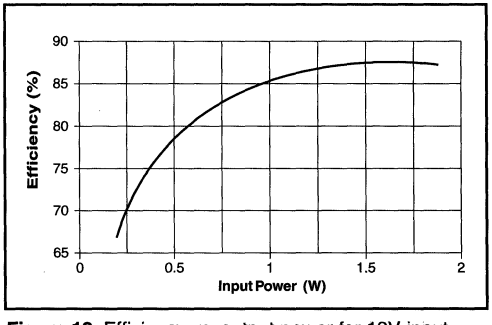

Figure 12. Efficiency vs. output power for 10V input.

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Using the UC3871 and UC3872 Resonant Fluorescent Lamp Drivers in Floating Lamp Applications

The UC3871 and UC3872 family of resonant lamp drivers contain all of the necessary control circuitry to implement a highly efficient cold cathode fluorescent back-light driver. The grounded lamp circuit topology is discussed in detail in both U-141 and U-148. This design note describes how to modify the circuit to accommodate a floating lamp topology.

In many back-light systems, the physical spacing between the lamp and lamp wires with respect to the foil reflector and LCD frame can be tight. With tight spacing, distributed capacitance will form. High voltage capacitive coupling effects may result in uneven illumination across the tube and a slight degradation in efficiency. A floating lamp topology can reduce these effects. Figure 1 compares the AC voltage gradient of a grounded lamp and a floating lamp.

In the grounded lamp application, one end of the lamp has a high AC voltage while the other end of the lamp is connected to circuit ground. Although the current passing through the lamp is uniform, the voltage along the lamp (with respect to the ground plane) is not. The resulting electromagnetic field gradient causes a non-uniform phosphor glow as shown in Figure 1. At low currents, when the lamp is dimmed, the non-uniformity may be visible. This is known as the "thermometer effect". A floating lamp reduces the thermometer effect by cutting the voltage gradient in half.

To a lesser degree, a floating lamp will also improve circuit efficiency. Referring to Figure 1, the stray capacitance causes leakage currents from the lamp to circuit ground. Although the current through stray capacitance doesn't directly trans-

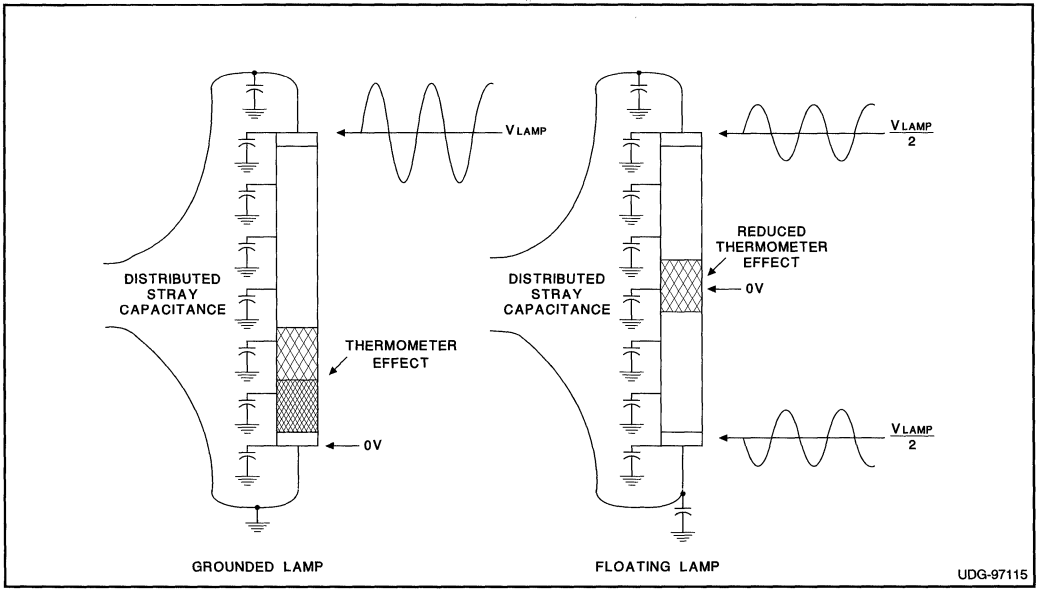


Figure 1.

late into losses, the extra current through the transformer and switching devices does. The floating topology cuts the average voltage along the lamp in half, this decreases the leakage current.

The UC3871 / 72 design can be converted to a floating lamp architecture as shown in Figure 2. A resistor added to the source of Q1 and Q2 is used to sense buck converter current. Buck current is proportional to the lamp current by the turns ratio of T1. A divider network connected between RSENSE, the inverting input of the error amplifier, and VREF is used to control lamp current. The non-inverting input of the error amplifier is internally derived off of VREF and should track within 0.5%. Resistors R1 and R3 should be chosen to have similar tolerances. When R2 is adjusted to zero ohms, lamp current is at a minimum. When R2 is adjusted to 2kΩ, lamp current is at a maximum. Several suppliers offer transformers for CCFL applications. A Coiltronics CTX110605 transformer was used for the circuit in Figure 2.

Optional Open Lamp Detection with a Floating Lamp

During normal operation, the voltage at the output of the buck converter will appear as a full wave rectified sinusoid at the resonant frequency. If the lamp is opened, current that initially fed the lamp will begin to feed the resonant tank, increasing the tank voltage. The transformer voltage will then increase until the buck current and the losses in the tank reach equilibrium. This increase in secondary voltage may result in a break down of the transformer's insulation. Open lamp detection can reduce voltage stress on the CCFL transformer during an open lamp condition by decreasing the buck current feeding the resonant tank. In many designs, the tank voltage will not increase to destructive levels and open lamp detection is not necessary.

The UC3871 / 72 open lamp detection circuitry will be invalidated by the floating lamp topology. Figure 3 shows a method for implementing open lamp detection with an open collector, quad comparator. If the buck output voltage increases

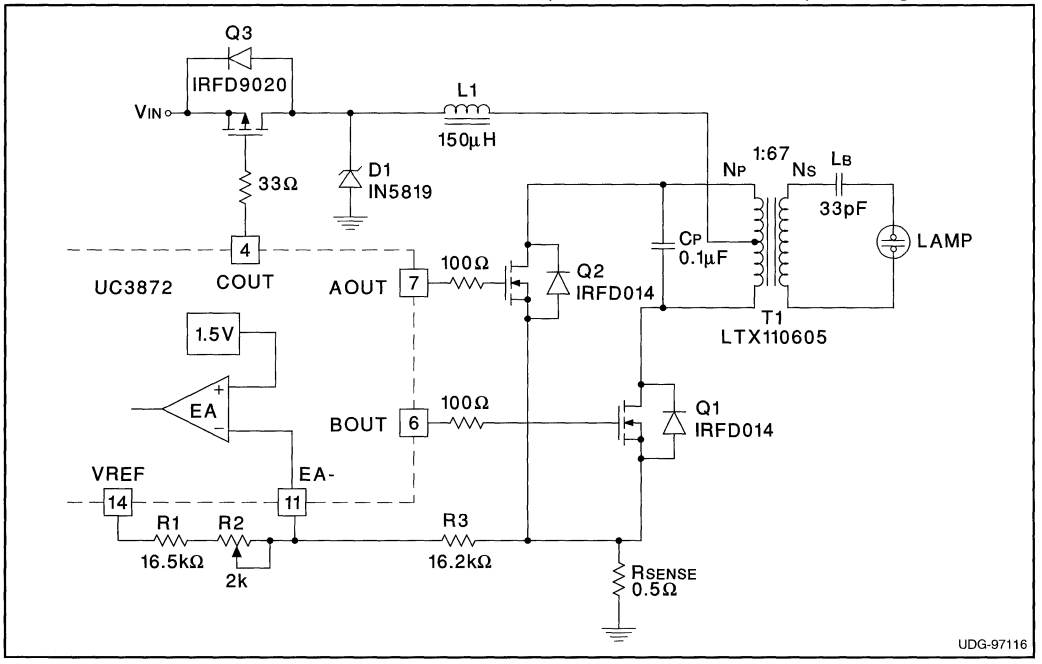


Figure 2. Floating Lamp with Primary Side Current Sense

above an acceptable level, comparator 1 will toggle high. A diode between the output and the positive input will latch the output high until power is cycled. A high output on comparator 1 will cause a low output on comparator 3, which is connected to the output of the error amplifier. Pulling low will force a minimum duty cycle on the buck coverter, decreasing the current feeding the tank, and the voltage on the transformer. Comparator 2 overrides the output of comparator 1 during soft start, allowing the tank voltage to ring up so the lamp can strike.

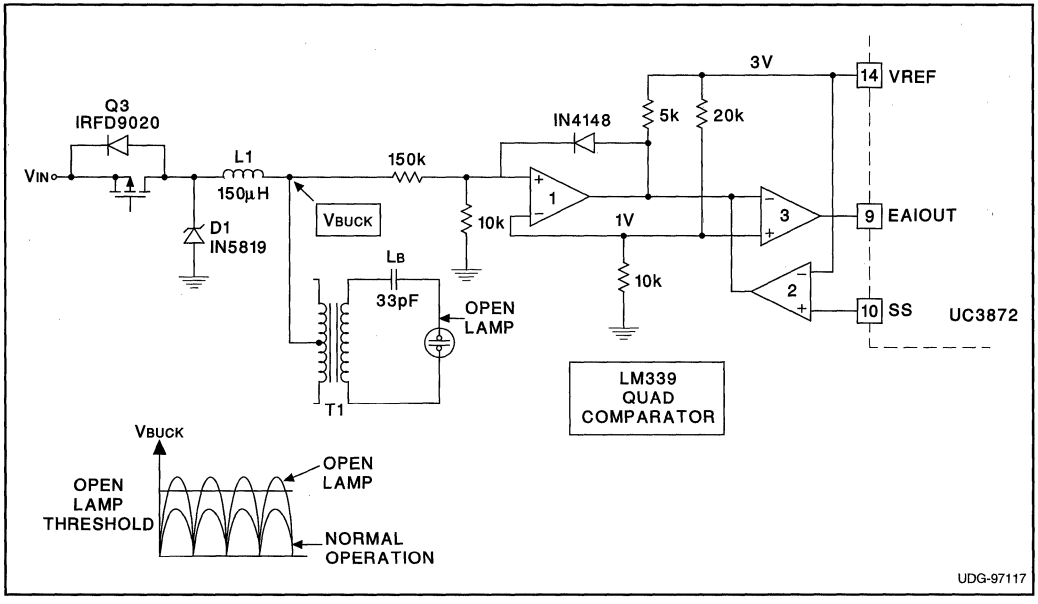
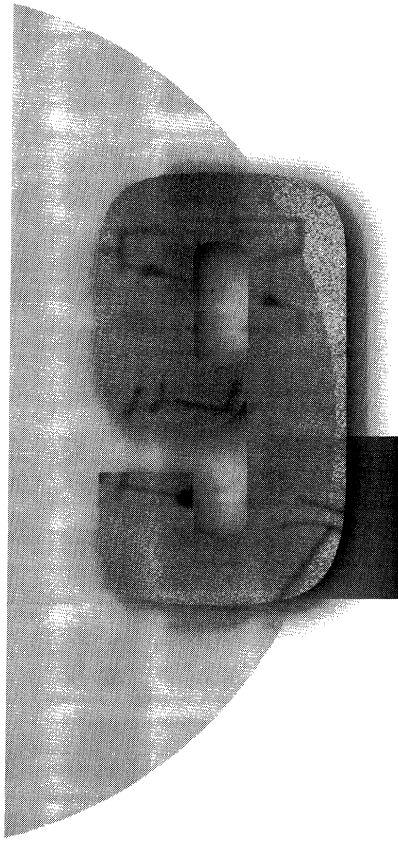


Figure 3. Optional Open Lamp Detection Circuit



IrDA

9

IrDA Selection Guide

Device Type	Supply Voltage	Data Rate	Dynamic Range	Quiescent Current	Encoder/ Decoder	IrDA Compliant	LED Driver	Part Number	Page Number
Receiver	3.3V or 5V	2.4kbps 115.2kbps	150nA 100mA	250μA	N	Y	N/A	UCC5341	9-2
Transceiver	3.3V or 5V	2.4kbps 115.2kbps	150nA 100m A	250μA	N	Y	500mA	UCC5342	9-6
Transceiver	3.3V or 5V	2.4kbps 115.2kbps	150nA 100mA	280μA	Y	Y	500mA	UCC5343	9-10

IrDA 115.2kbps Receiver

FEATURES

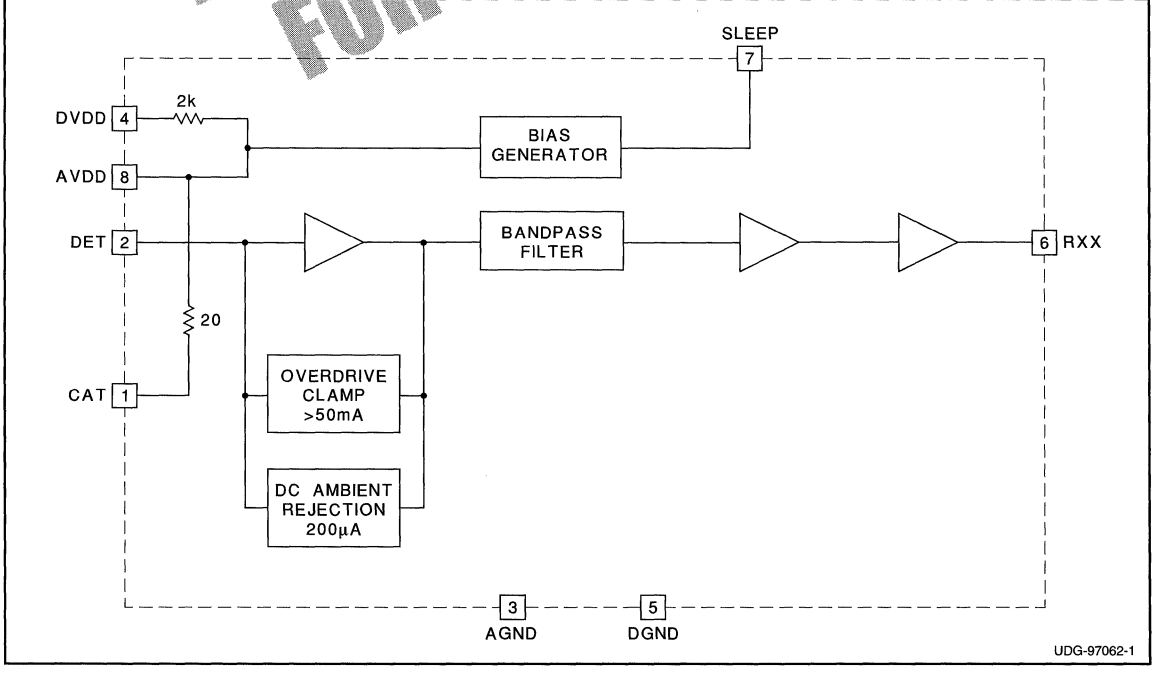
- Supports IrDA standard to 115.2kbps Data Rates
- 3V to 5V Operation
- Wide Dynamic Receiver Range from 200nA to 50mA Typical
- IrDA Compliant I/O
- Very Low Quiescent Current In Active Mode (250µA Typical)
- Ultra Low Quiescent Current In Sleep Mode (0.5µA Typical)
- Compatible with IrDA Detector Diodes

DESCRIPTION

The UCC5341 IrDA (Infrared Data Association) Receiver supports the analog section of the IrDA standard. It has a limiting transresistance amplifier to detect a current signal from a PIN diode and drives RXX pulses to a UART. The amplifier is capable of input currents ranging from 200nA to greater than 50mA. The UCC5341 is bandpass limited to reduce interference from other IR sources. The UCC5341 also has very low current consumption in the active mode (250µA typically), making it excellent for power sensitive applications.

The output of the receiver is designed to drive CMOS and TTL levels, for direct interfacing to IrDA compliant UARTs and Super I/O devices. Internal resistors are provided for decoupling the detector diode supply, thus minimizing the number of external components required.

BLOCK DIAGRAM



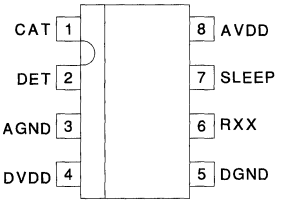
ABSOLUTE MAXIMUM RATINGS

AVDD, CAT, DVDD . . . . . –0.3V to 7V
CAT, DET, DVDD, SLEEP, ... –0.3V to AVDD + 0.3V
IRXX . . . . . –10mA to 10 mA
IDET 250mA
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10sec.) . . . . . +300°C

All voltages are with respect to respect to AGND. DGND must be connected to AGND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

ABSOLUTE MAXIMUM RATINGS

SOIC-8, DIL-8 (Top View)
D, N Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, TA = 0°C to 70°C, AVDD = 3.0V to 5.5V, CAVDD = 100nF, CDVDD = 100nF, CCAT = 4.7µF + 100nF, CRXX = 40pF, CDET < 56pF. All currents are positive into a specified pin. TA = TJ

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Supply Current Section					
IDD	No Output Load, SLEEP ≤ 0.5V		250	350	µA
IDD	SLEEP ≥ AVDD – 0.5V		0.5	3	µA
RDVDD	AVDD to DVDD	1.0	2	3.0	kΩ
RCAT	AVDD to CAT	10	20	32	Ω
Receiver Section					
Input Refered Noise	(Note 1)		10		$\frac{pA}{\sqrt{Hz}}$
Detection Threshold	1.6µs Input Pulse, 1µs ≤ Rxx ≤ 8µs		200	400	nA
Signal to Noise Ratio	IDET = 200nA, (Note 1)		11.8		nA
Lower Band Limit	(Note 1)		50		kHz
Upper Band Limit	(Note 1)		1		MHz
Output Pulse Width	IDET = 400nApk to 20mApk, 0 to 200µADC, 1.6µs Input Pulse	1.0		8.0	µs
RXX Output (VOL)	IRXX = 800µA		200	400	mV
RXX Output (VOH)	IRXX = –100µA, DVDD – RXX		200	400	mV
RXX Rise Time	From 10% to 90% of DVDD		150	200	ns
RXX Fall Time	From 90% to 10% of DVDD		100	150	ns

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

AGND: Ground reference for analog circuits. Connect to circuit board ground plane.

AVDD: Supply pin for analog circuits. Bypass to AGND with a 100nF or 1µF ceramic capacitor.

CAT: Filtered Supply for PIN diode cathode. Internally connected to AVDD through a 20Ω resistor. Bypass to AGND with a 4.7µF capacitor plus a 100nF ceramic capacitor.

DET: Input to receiver amplifier. Connect to PIN diode anode. Shield with AVDD and/or AGND from all other signals, especially RXX.

DGND: Ground pin for digital circuits. Connect to circuit board ground plane.

DVDD: Supply pin for digital circuits. Internally connected to AVDD through a 2kΩ resistor. Bypass to DGND with a 100nF or 1µF ceramic capacitor.

RXX: Output of the detect amplifier and buffer. Connect to UART. Avoid coupling the RXX signed to DET.

SLEEP: Sleep mode select pin. A logic high on SLEEP

APPLICATION INFORMATION

Ground Plane

There are 2 ground connections shown on the application drawing, representing the sensitive analog ground and the 'dirty' digital ground. These 2 points can simply be geographic groupings of connections to a ground plane. If a ground plane is not used, other provision to isolate the analog and digital ground currents should be provided. The use of a ground plane is strongly recommended.

DET Considerations

DET is flanked by AGND and CAT. This should be used to good advantage by fully enclosing the DET circuit board trace with AGND in order to shield leakage noise from DET. The DET circuit board trace length should be minimized. Since the PIN diode connected to DET is capacitive, noise coupling to the cathode of the diode will be coupled directly to DET. For this reason, the 100nF capacitor on CAT should be located physically close to the cathode of the PIN diode.

There is natural parasitic coupling from RXX to DET. RXX should be routed to minimize the parasitic capacitive coupling from RXX to DET.

Analog Power Supply Decoupling

The UCC3541 has a highly sensitive amplifier section capable of detecting extremely low current levels (200nA typical). Achieving this sensitivity requires quiet analog power supply rails. A 100nF high frequency capacitor in close proximity to AVDD and AGND is required for quiet analog rails.

Digital Power Supply

DVDD is fed directly from AVDD through an internal 2k resistor. The DVDD bypass capacitor handles all transient current produced by the digital section of the chip. If more drive is required from RXX than the internal 2k resistor will allow, an external resistor can shunt it. This should always be accompanied by increasing the value of the decoupling capacitor on DVDD and AVDD.

Economy Application

The diagram of the economy application shows only one bypass capacitor. This application is suitable where maxi-

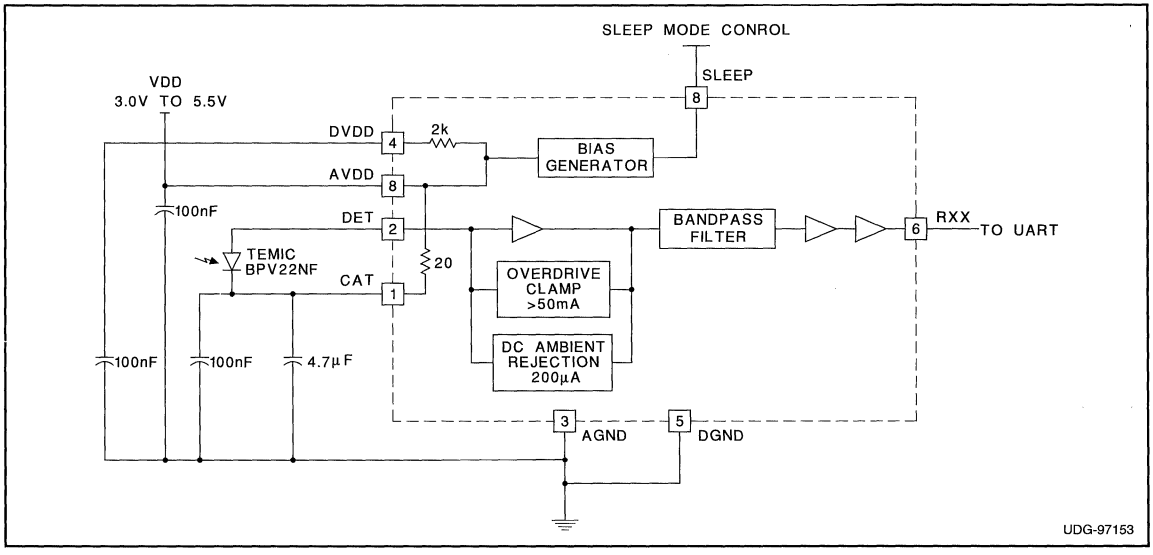


Figure 1. Typical Application of the UCC5341

APPLICATION INFORMATION (cont.)

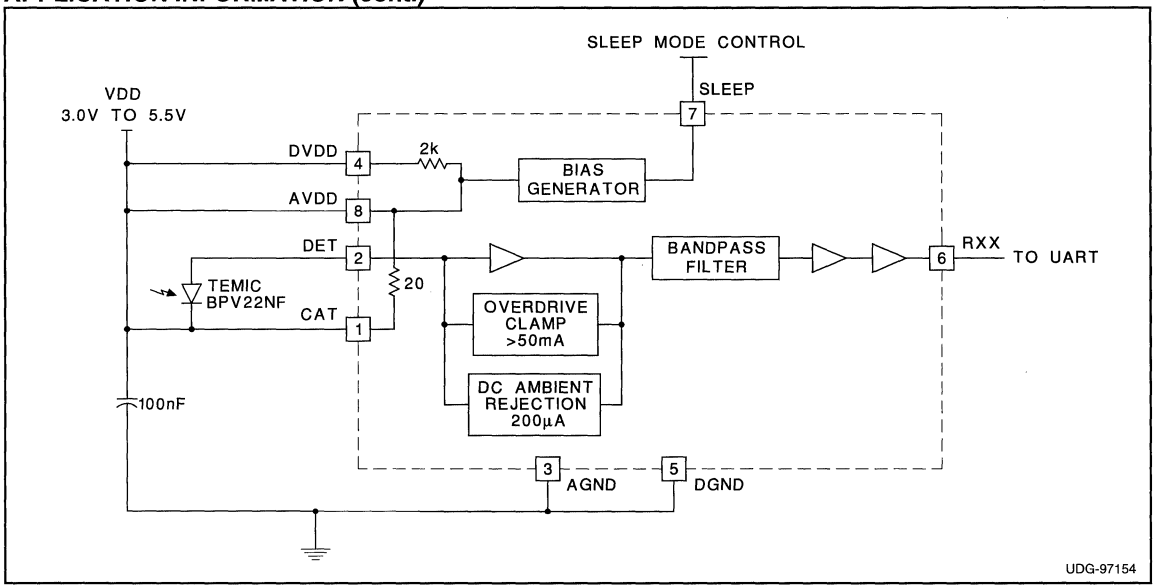


Figure 2. Economy Application of the UCC5341

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IrDA 115.2kbps Transceiver

FEATURES

- Supports IrDA Standard to 115kbps Data Rates
- 3V to 5V Operation
- Wide Dynamic Receiver Range from 200nA to 50mA Typical
- IrDA Compliant I/O
- 500mA LED Driver
- Very Low Quiescent Current in Active Mode (250µA Typical)
- Ultra Low Quiescent Current in Sleep Mode (0.5µA Typical)
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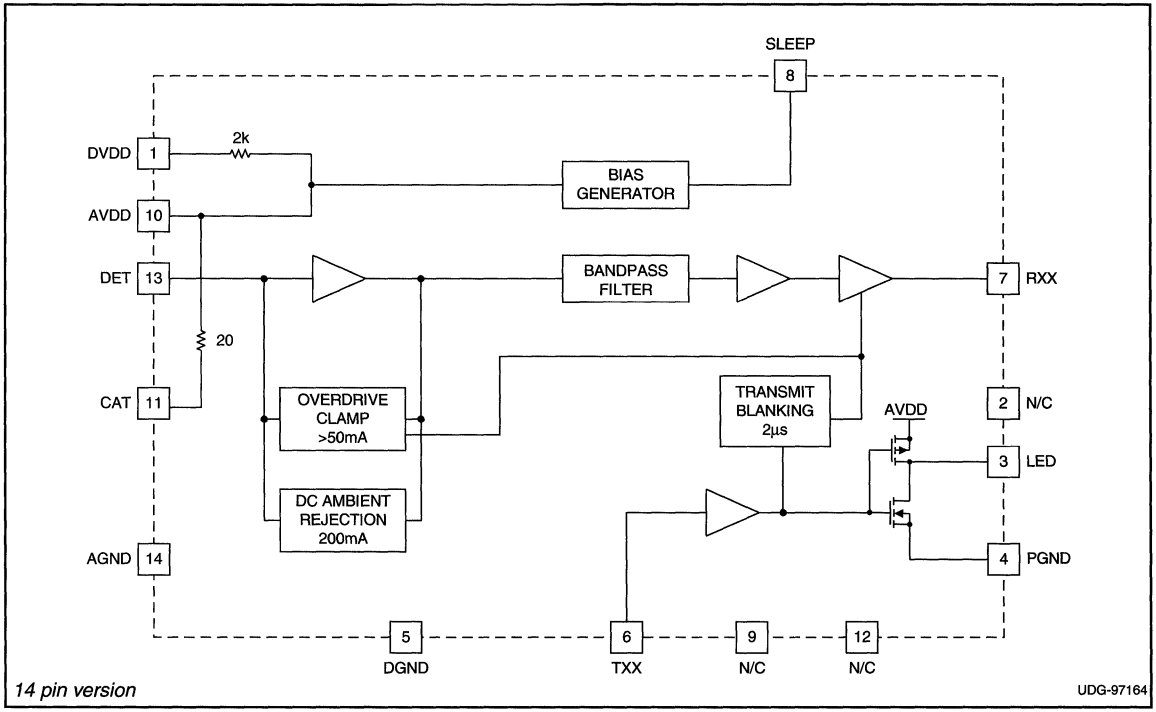
DESCRIPTION

The UCC5342 IrDA (Infrared Data Association) Transceiver supports the analog section of the IrDA standard. The receiver has a limiting transresistance amplifier to detect a current signal from a PIN diode and drives RXX pulses to a UART. The amplifier is capable of input currents ranging from 200nA to 50mA. The amplifier is bandpass limited to reduce interference from other IR sources.

The output of the receiver is designed to drive CMOS and TTL levels, for direct interfacing to IrDA compliant UARTs and Super I/O devices. Internal resistors are provided for decoupling the detector diode supply, thus minimizing the number of external components required.

The transmitter portion of the chip has a low impedance open drain MOSFET output. It is capable of sinking 300mA from an output LED at 3V, and 500mA at 5V.

BLOCK DIAGRAM



14 pin version

UDG-97164

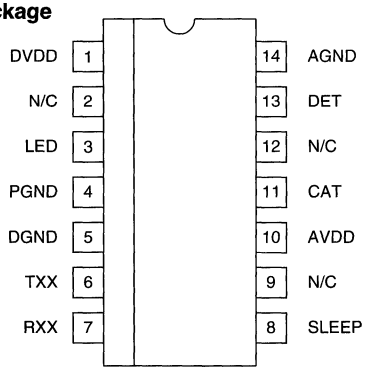
ABSOLUTE MAXIMUM RATINGS

AVDD, DVDD, CAT. . . . . –0.3V to 7V
SLEEP, DET, TXX, LED,
DVDD, CAT. . . . . –-0.3V to AVDD + 0.3V
IRXX . . . . . –10mA to 10 mA
IDET 250mA
ILED 1A
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature. . . . . –55°C to +150°C
Lead Temperature (Soldering, 10sec.) . . . . . +300°C

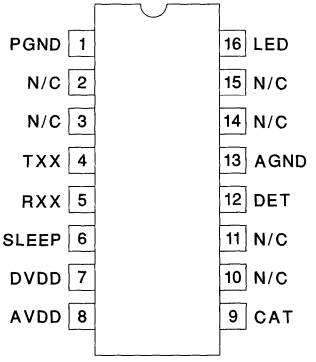
All voltages are with respect to respect to AGND. DGND and PGND must be connected to AGND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

SOIC-14, DIL-14 (Top View)
D,N Package



SSOP-16 (Top View)
M Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C, AVDD = 3.0V to 5.5V, C_{AVDD} = 100nF, C_{DVDD} = 100nF, C_{CAT} = 4.7µF + 100nF, C_{RXX} = 40pF, C_{DET} < 56pF. T_A = T_J.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Supply Current Section					
IDD	No Output Load, SLEEP ≤ 0.5V		250	350	µA
IDD	SLEEP ≥ AVDD – 0.5V, TXX ≤ 0.5V		0.5	3	µA
RDVDD	AVDD to DVDD	1.0	2	3.0	kΩ
RCAT	AVDD to CAT	10	20	32	Ω
Receiver Section					
Input Refered Noise	(Note 1)		10		$\frac{pA}{\sqrt{Hz}}$
Detection Threshold	1.6µs Input Pulse, 1µs ≤ RXX ≤ 8µs		200	400	nA
Signal to Noise Ratio	IDET = 200nA (Note 1)		11.8		
Lower Band Limit	(Note 1)		50		kHz
Upper Band Limit	(Note 1)		1		MHz
Output Pulse Width	IDET = 400nApk to 20mApk, 0 to 200µADC, 1.6µs Input Pulse	1.0		8.0	µs
RXX Output (VOL)	IRXX = 800µA		200	400	mV
RXX Output (VOH)	IRXX = –100µA, DVDD – RXX		200	400	mV
RXX Rise Time	From 10% to 90% of DVDD		150	200	ns
RXX Fall Time	From 90% to 10% of DVDD		100	150	ns
ITXX	TXX = 0 to AVDD	–10		10	µA

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, T_A = 0°C to 70°C, AVDD = 3.0V to 5.5V, C_{AVDD} = 100nF, C_{DVDD} = 100nF, C_{CAT} = 4.7µF + 100nF, C_{RXX} = 40pF, C_{DET} < 56pF. T_A = T_J.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
TXX (V_{IH})			2	2.5	V
TXX (V_{IL})		0.8	1		V
LED	TXX = AVDD = 4.5V, I_{LED} = 500mA		0.3	0.6	V
	TXX = AVDD = 3.0V, I_{LED} = 300mA		0.3	0.6	V
AVDD – LED	TXX = 0, AVDD = 3.0V, I_{LED} = –1mA		0.2	0.6	V

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

AGND: Ground reference for analog circuits. Connect to circuit board ground plane.

AVDD: Supply pin for analog circuits. Bypass to AGND with a 100nF or 1µF ceramic capacitor.

CAT: Filtered supply for PIN diode cathode. Internally connected to AVDD with a 20Ω resistor. Bypass to AGND with a 4.7µF capacitor plus a 100nF ceramic capacitor.

DET: Input to receiver amplifier. Connect to PIN diode anode. Shield with a AVDD and/or AGND from all other signals, especially RXX.

DGND: Ground pin for digital circuits. Connect to circuit board ground plane.

DVDD: Supply pin for digital circuits. Internally connected to AVDD with a 2kΩ resistor. Bypass to DGND with a 100nF or 1µF ceramic capacitor.

LED: Open drain of transmitter output transistor. Connect to an external IrDA compliant light emitting diode via an external resistor.

PGND: Source of transmitter output transistor. Connect to circuit board ground plane.

RXX: Output of the detect amplifier and buffer. Connect to UART. Avoid coupling the RXX signal to DET.

SLEEP: Sleep mode select pin. A logic high on SLEEP puts the chip into sleep mode, reducing IDD to 0.5µA typical.

TXX: Input from UART to transmit LED driver.

APPLICATION INFORMATION

Ground Plane

There are 3 ground connections shown on the application drawing, representing the sensitive analog ground, the 'dirty' digital ground and the high current transmitter ground. These 3 points can simply be geographic groupings of connections to a ground plane. If a ground plane is not used, other provision to isolate the analog and digital ground currents should be provided. The use of a ground plane is strongly recommended.

DET Considerations

DET is flanked by AGND and an unconnected pin. This should be used to good advantage by fully enclosing the DET circuit board trace with AGND in order to shield leakage noise from DET. The DET circuit board trace length should be minimized. Since the PIN diode connected to DET is capacitive, noise coupling to the cathode of the diode will be coupled directly to DET. For this reason, the 100nF capacitor on CAT should be located physically close to the cathode of the PIN diode.

There is natural parasitic coupling from RXX to DET. RXX should be routed to minimize the parasitic capacitive coupling from RXX to DET.

Analog Power Supply Decoupling

The UCC3542 has a highly sensitive amplifier section capable of detecting extremely low current levels (200nA typical). Achieving this sensitivity requires quiet analog power supply rails. A 100nF high frequency capacitor in close proximity to AVDD and AGND is required for quiet analog rails.

The transmitter section of the chip runs form the AVDD supply and draws high peak currents (~500mA in a typical application). A bulk capacitor may be required close to the AVDD and AGND pins if the connection length to the power supply is long, or if the supply is relatively high impedance. This bulk capacitor is in addition to the 100nF high frequency capacitor mentioned above. The bypass capacitors on CAT and AVDD should present very low equivalent series resistance and inductance to the circuit.

APPLICATION INFORMATION (cont.)

Digital Power Supply

DVDD is fed directly from AVDD through an internal 2k resistor. The DVDD bypass capacitor handles all transient current produced by the digital section of the chip. If more drive is required from RXX, than the internal 2k resistor will allow, an external resistor can shunt it. This technique should always be accompanied by increasing the value of the decoupling capacitor on DVDD and AVDD.

Economy Application

The diagram of the economy application shows only one bypass capacitor. This application is suitable where maximum sensitivity is not required and where the power supply feeding AVDD is relatively clean and low impedance.

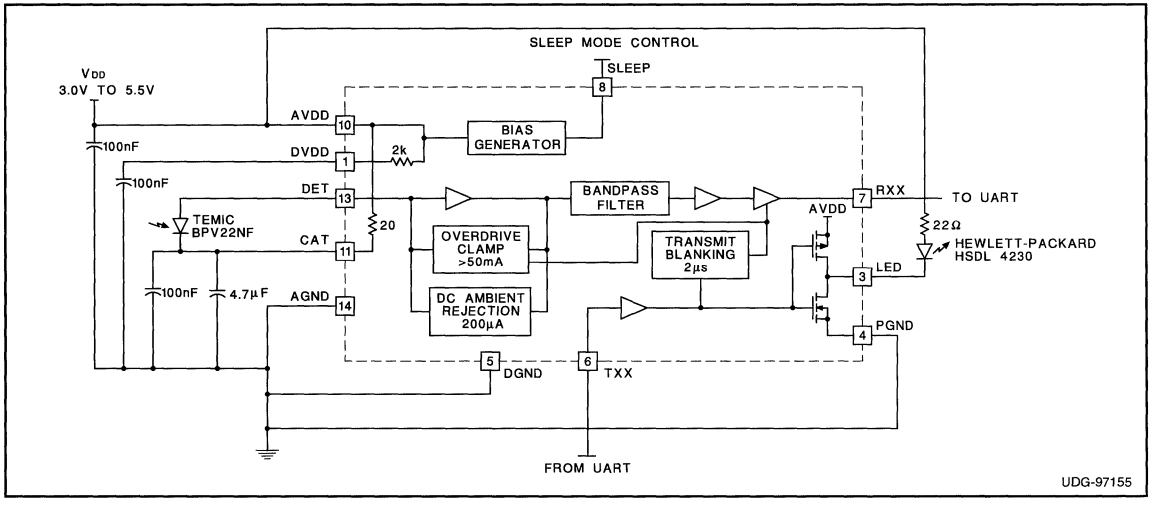


Figure 1. Typical Application of the UCC5342

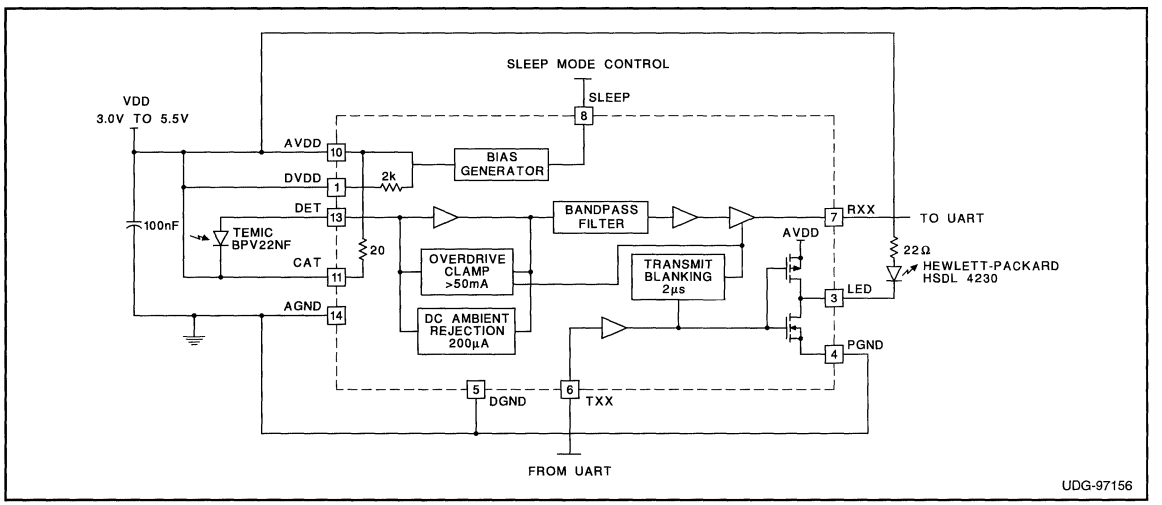


Figure 2. Economy Application of the UCC5342

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IrDA Transceiver with Encoder/Decoder

FEATURES

- Micropower in the Sleep Mode, (2µA)
- 3V to 5V Operation
- Wide Dynamic Receiver Range from 200nA to 50mA Typical
- Direct Interface to IrDA Compatible UARTs or Super I/O ICs
- Supports IrDA Standard to 115.2kbps Data Rates
- Transmitter Output Stage Capable to 500mA Sink Current
- IrDA Compliant Modulation & Demodulation Scheme
- Direct Interface to Standard UART
- 16 Pin SSOP, SOIC and DIL Package

DESCRIPTION

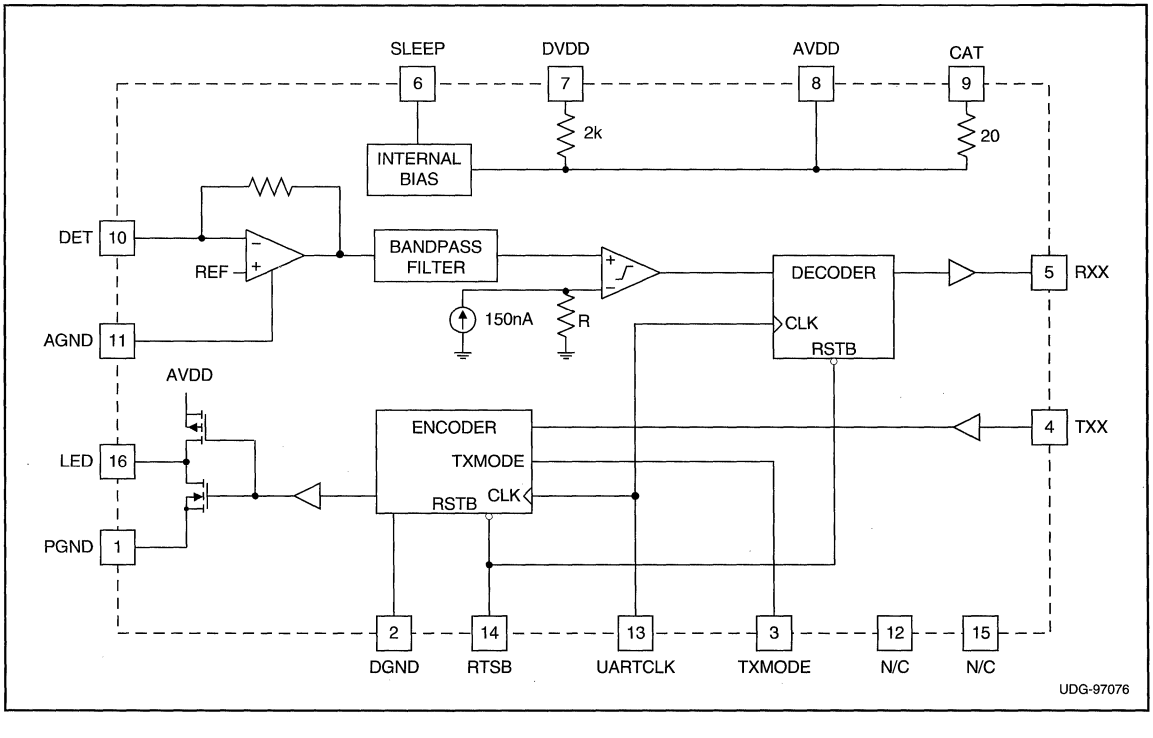
The UCC5343 IrDA Transceiver with Encoder/Decoder supports the Physical Layer specifications of the IrDA standard. Additional functionality is provided by data format translation between standard UART and IrDA formats. The UCC5343 is readily interfaced to a standard UART.

The Receiver has a limiting transresistance amplifier to detect a current signal from a PIN diode and drives RXX pulses into a UART. The receiver is capable of detecting input currents ranging from 200nA to greater than 50mA. The receiver signal path is frequency limited by an internal bandpass filter to reduce interference from other sources of IR energy.

The output of the receiver is designed for direct interface to standard UARTs and Super I/O devices up to 115.2kbps. Internal resistors are provided for decoupling the pin diode supply, minimizing the number of required external components.

The UCC5343 has low current consumption in the active mode, making it excellent for applications with low power requirements. The transmitter section has a low impedance open drain MOSFET output. It is capable of sinking 300mA from an output LED at 3V and 500mA at LED at 5V.

BLOCK DIAGRAM



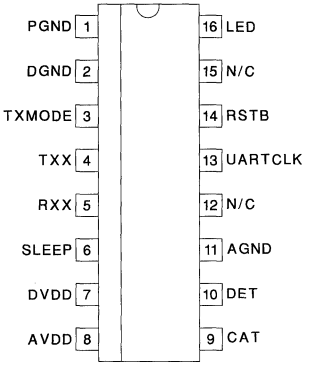
ABSOLUTE MAXIMUM RATINGS

AVDD, DVDD, CAT. . . . . –0.3V to 7V
SLEEP, DET, TXX, LED,
DVDD, CAT. . . . . –0.3mA to AVDD + 0.3mA
IRXX . . . . . –10mA to 10 mA
IDET 250mA
ILED 1A
Power Supply . . . . . TBA
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature. . . . . –55°C to +150°C
Lead Temperature (Soldering, 10sec.) . . . . . +300°C

All voltages are positive with respect to AGND. DGND and PGND must be connected to AGND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

SSOP-16, SOIC-16 and DIL-16 (Top View)
M Package, D and N Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, 0°C < TA < 70°C TA = 0°C to 70°C, AVDD = 3V to 5.5V, CAVDD = 100nF, CDVDD = 100nF, CCAT = 4.7µF + 100nF, CRXX = 40pF, CDET < 56pF. TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
IDD	No Output Load, SLEEP ≤ 0.5V		280	450	µA
	SLEEP > AVDD – 0.5V		1	3	µA
RVDD	AVDD to DVDD	1.0	2	3.0	kΩ
RCAT	AVDD to CAT	15	20	32	Ω
Receiver Section					
Input Referred Noise	(Note 1)		10		$\frac{pA}{\sqrt{Hz}}$
Detection Threshold			200	400	nA
DetectionThreshold Signal to Noise Ratio	IDET = 200nA (Note 1)		11.8		
Lower Band Limit	(Note 1)		50		kHz
Upper Band Limit	(Note 1)		1		MHz
Output Pulse Width	IDET = 200nA Peak to 20mA Peak and 0 to 200µADC, 1.6µS Peak fUARTCLK = 2MHz		8.95		µS
RXX Output (VOL)	IRXX = 800µA		200	400	mV
RXX Output (VOH)	IRXX = –100µA, DVDD - RXX		200	400	mV
RXX Rise Time	10% to 90% of DVDD		150	200	nS
RXX Fall Time	90% to 10% of DVDD		100	150	nS
Transmitter Section					
ITXX	TXX = 0 to AVDD	–1		1	µA
TXX (VIH)	DVDD = 5V	0.7 • DVDD		DVDD	V
TXX (VIL)	DVDD = 5V	0		0.3 • DVDD	V
LED	TXX = 0, AVDD = 4.5V, ILED = 500mA		0.3	0.6	V
	TXX = 0, AVDD = 3V, ILED = 300mA		0.3	0.6	V
Encoder Transmit Section					
Encoder Output Pulse Width	TXMODE = VDD	1.41		2.23	µS

Note 1: Guaranteed by Design. Not 100% tested in production.

PIN DESCRIPTIONS

AGND: Ground pin for analog circuits.

AVDD: Supply pin for analog circuits. Bypass to AGND with 100nF or 1μF capacitor.

CAT: This pin is a filtered supply for PIN diode cathode. Internally connected to AGND with a 20Ω resistor. Bypass to a GND with a 4.7μF electrolytic capacitor and a 100nF ceramic capacitor.

DET: This is the input to the receiver amplifier. Connect pin diode anode to this pin.

DGND: Ground pin for digital circuits.

DVDD: Supply pin for digital circuits. Internally connected to AVDD through 2k resistor. This pin must be bypassed to DGND with a 100nf or 1μF ceramic capacitor.

LED: LED pin is the output of the transmitter section of the chip. The signal on this pin is the IrDA encoded version of the UART transmit signal.

PGND: Ground pin for the transmitter power device. This pin should be connected to the circuit board ground plane.

RSTB: This active low input signal is used to reset the encoder and decoder sections of the chip. This signal must be provided by the system during startup.

RXX: RXX is the demodulated receive signal. Normally this pin is tied to SIN signal of UART. TTL/CMOS compatible output from the receiver stage to an IrDA UART. This output is digitally decoded (pulse stretched).

SLEEP: Sleep mode select pin. A logic high on SLEEP pin puts the chip into a low current mode.

TXMODE: TXMODE is used to select the modulation mode. If TXMODE is set high (1) the signal on TXD pin will have the output pulse width of 1.6μS. If TXMODE is set low (0), the output will have the pulse width of 3/16 of the UARTCLK frequency.

If TXMODE pin is left floating, the output will default to 1.6μS pulse width.

TXX: Input from the UART. This pin is normally tied to SOUT signal of UART.

UARTCLK: Input of the system clock. This frequency must set at 16 times the IrDA data rate, and must be available from the UART.

APPLICATION INFORMATION

Figures 1 and 2 outline the IrDA SIR encoding scheme. The encoding scheme relies on a clock being present. The clock must be set to 16 times the data transmission baud rate. The encoder sends a pulse for every space (0) that is sent. On a high to low transition of TXD signal, the generation of the pulse is delayed for 7 clock cycles of the 16XCLK before the pulse is set high for 3/16 of a bit time or 1.6μs the pulse width is selected by TXMODE. For consecutive spaces, pulses with 1 bit time delay are generated in series. If a logic 1 (mark) is sent, the encoder does not generate a pulse.

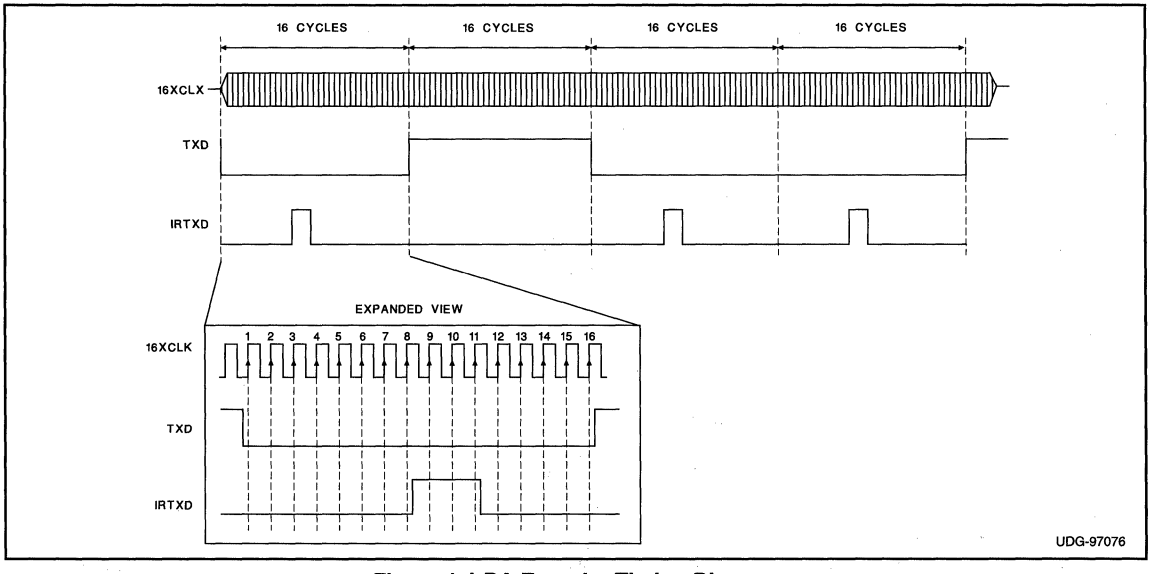


Figure 1. IrDA Encoder Timing Diagram

APPLICATION INFORMATION (cont.)

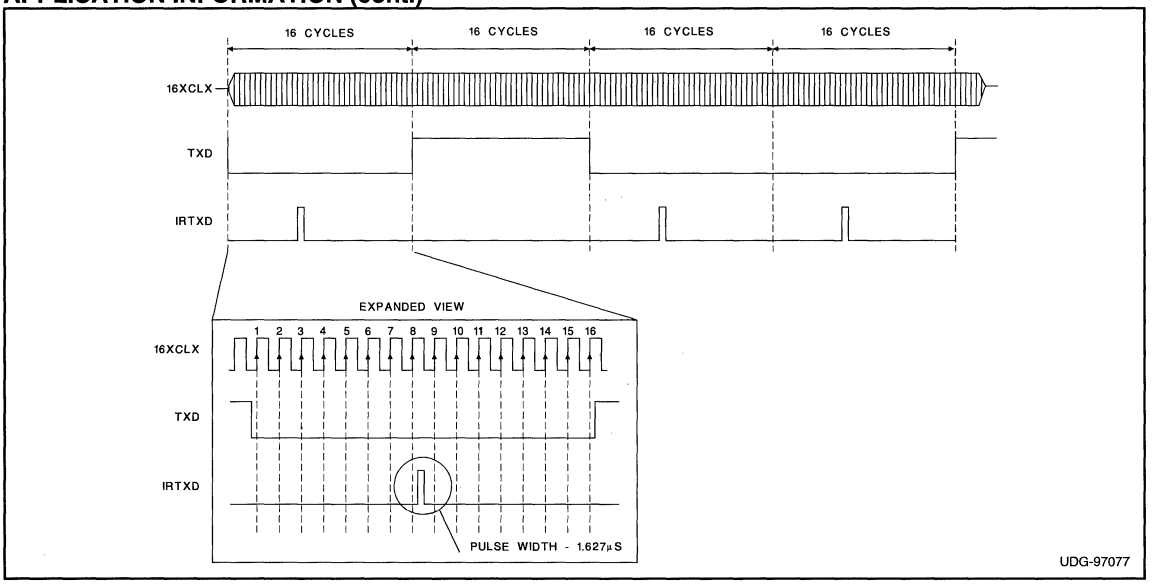


Figure 2. IrDA Encoder Timing Diagram (1.6µs Pulse Width)

The IrDA SIR decoding modulation method performs a pulse stretching function. Every high to low transition of the IRRXD line signifies an arrival of a 3/16th pulse. This pulse needs to be stretched to accommodate 1 bit time (or 16 of 16XCLK cycles). Every pulse that is received is translated into a space (0) on the RXD output. If a series of pulses separated by 1 bit time are received, then the result is a 1 bit time low pulse for every 3/16 pulse received. The decoding scheme is shown in Figure 3.

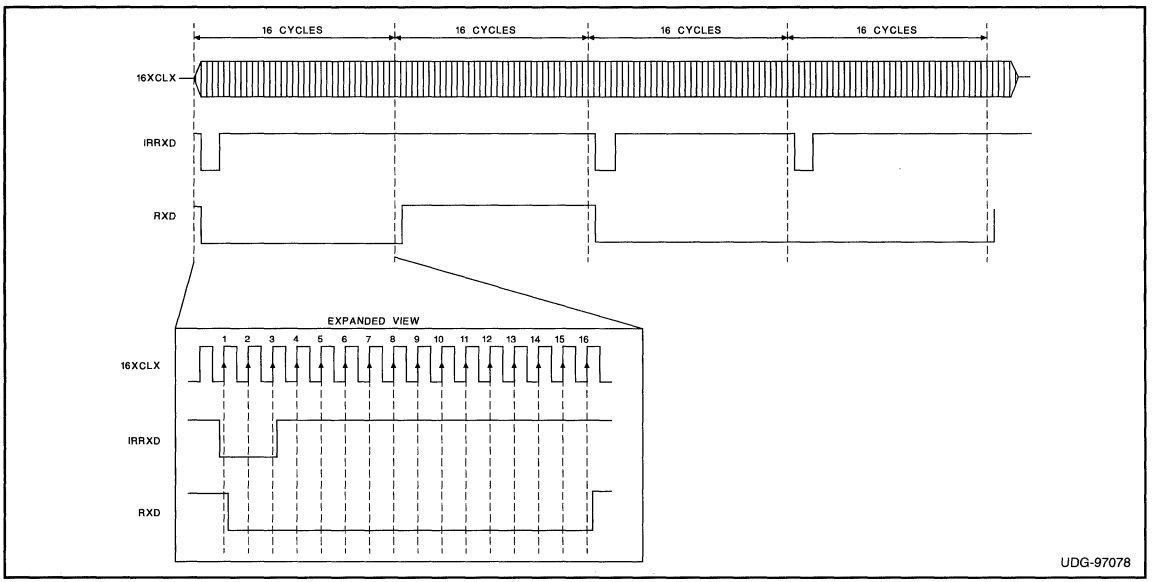


Figure 3. IrDA Decoder Timing Diagram

APPLICATION INFORMATION (cont.)

Ground Plane

There are 3 ground connections shown on the application drawing. They represent the sensitive analog ground, the dirty digital ground, and the high current transmitter ground. These 3 points can simply be geographic groupings of connections to a ground plane. If a ground plane is not used, other provision to isolate the analog and digital ground currents should be provided. The use of a ground plane is strongly recommended.

DET Considerations

The DET circuit board trace should be surrounded with AGND in order to shield leakage noise from DET. The DET circuit board trace length should be minimized. Since the PIN diode connected to DET is capacitive, noise coupling to the cathode of the diode will be coupled directly to DET. For this reason, the 100nF capacitor on CAT should be located physically close to the cathode of the PIN diode.

There is natural parasitic coupling from RXX to DET. RXX should be routed to minimize the parasitic capacitive coupling from RXX to DET.

Analog Power Supply De-coupling

The UCC5343 has a highly sensitive amplifier section capable of detecting extremely low current levels (200nA typical). Achieving this sensitivity requires quiet analog power supply rails. A 100nF high frequency capacitor in close proximity to AVDD and AGND is required for quiet analog rails.

The transmitter section of the chip runs from the AVDD supply and draws high peak currents (~ 500 mA in a typical application). A bulk capacitor may be required physically close to the AVDD and AGND pins if the connection length to the power supply is long or if the supply is or appears to be relatively high impedance. This bulk capacitor is in addition to the 100nF high frequency capacitor mentioned above. The bypass capacitors on CAT and AVDD should present very low equivalent series resistance and inductance to the circuit.

Digital Power Supply

DVDD is fed directly from AVDD through an internal 2k resistor. The DVDD bypass cap handles all transient current produced by the digital section of the chip. If more drive is required from RXX than the internal 2k resistor will allow, an external resistor can shunt it. This technique should always be accompanied by increasing the value of the de-coupling capacitor on DVDD and AVDD.

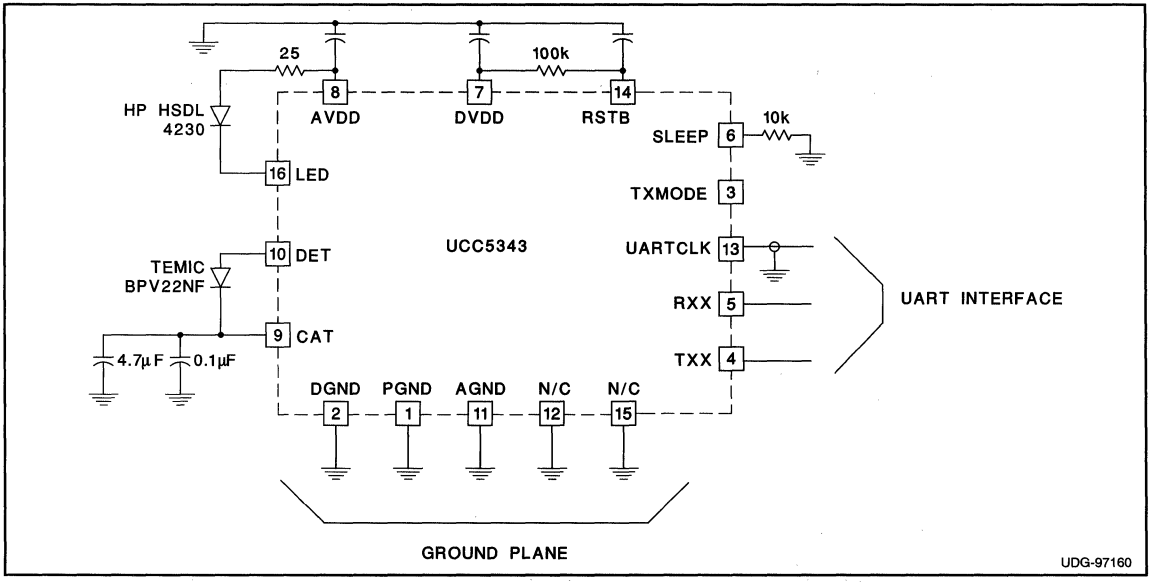


Figure 4. IrDA Transceiver with UART Encoder/Decoder Logic

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UNITRODE
Design Note

UCC5342 "IrDA 115.2kbps Transceiver" Evaluation Board, Schematic, and List of Materials

The UCC5342 demonstration board is supplied assembled and ready to test. This board is a complete implementation of the IrDA physical layer at speeds up to 115Kbps. The user needs to supply power and an IrDA compliant input pulse train to use the board.

The board was built to allow some user configuration. The jumper block JP1 allows the user to select the current through the IR led. JP2 will put the chip into its run or sleep modes. Shorting the pads of J2 and J3 will give a common supply with ability to use only one supply bypass capacitor. In this configuration, C1 and C3 may be removed. This will reduce the noise immunity of the board and adversely affect performance at low signal levels, but reduces parts count. An area is provided on the board where a mounting hole may be drilled or a clamp may be attached without affecting performance.

The schematic of the board as supplied is shown in Figure 1. Figure 2 shows the board equivalent schematic after removing C1 and C3 and bridging J2 and J3. Removing C1 and C3 and bridging J2 and J3 creates a minimally bypassed economy application that uses fewer components at the expense of some sensitivity. The amount of sensitivity reduction seen will vary with the individual application but should not be great.

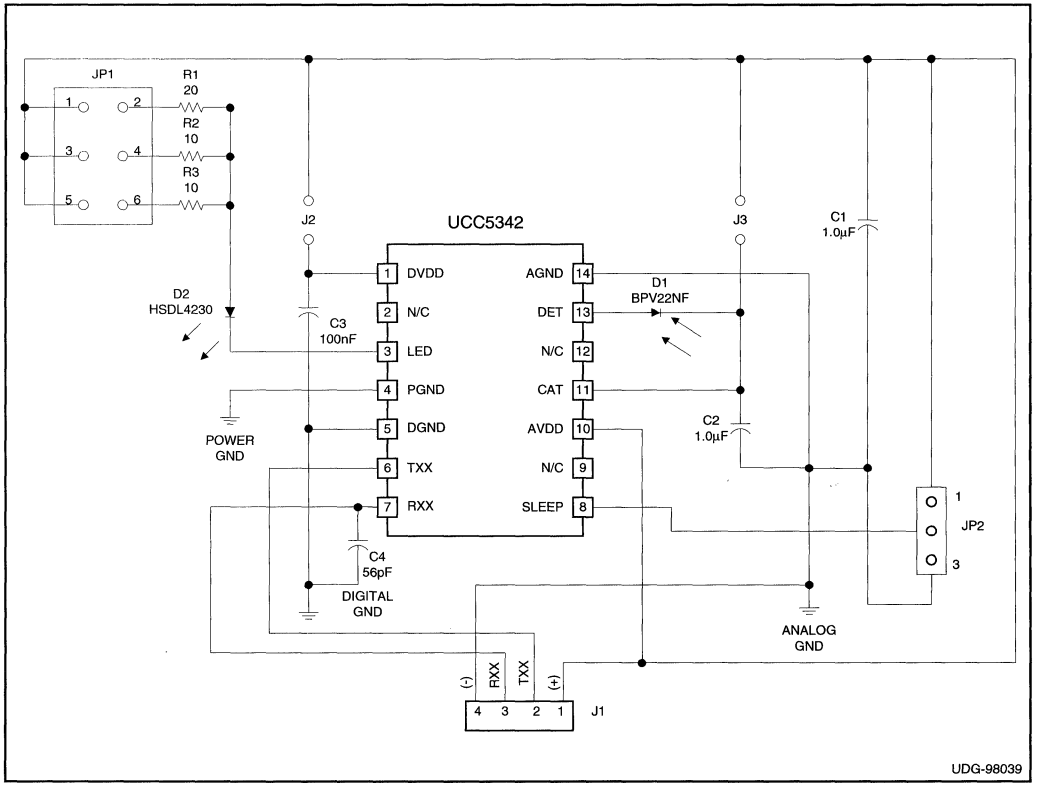

Figure 1. Fully Bypassed Schematic

CONNECTIONS TO THE BOARD

There are only four connections to make to the board – two power connections and two signal connections. Power connections are made at the terminals marked (+) and (-) on J1.

The power supply should be clean, as this is a part that is sensitive to noise on the power supply. The voltage must be between 2.7 and 5.5 volts. If two boards are being used to talk to each other, separate power supplies for each board are strongly recommended to reduce the possibility of noise coupling from the transmitter board to the receiving board's power supply.

The TXX terminal can be hooked to either a pulse generator or to the transmit output of an IrDA compatible UART. The voltage on this connection should not be allowed to go higher that the (+) terminal. The RXX terminal can be monitored with an oscilloscope or connected to the receive input of an IrDA compatible UART.

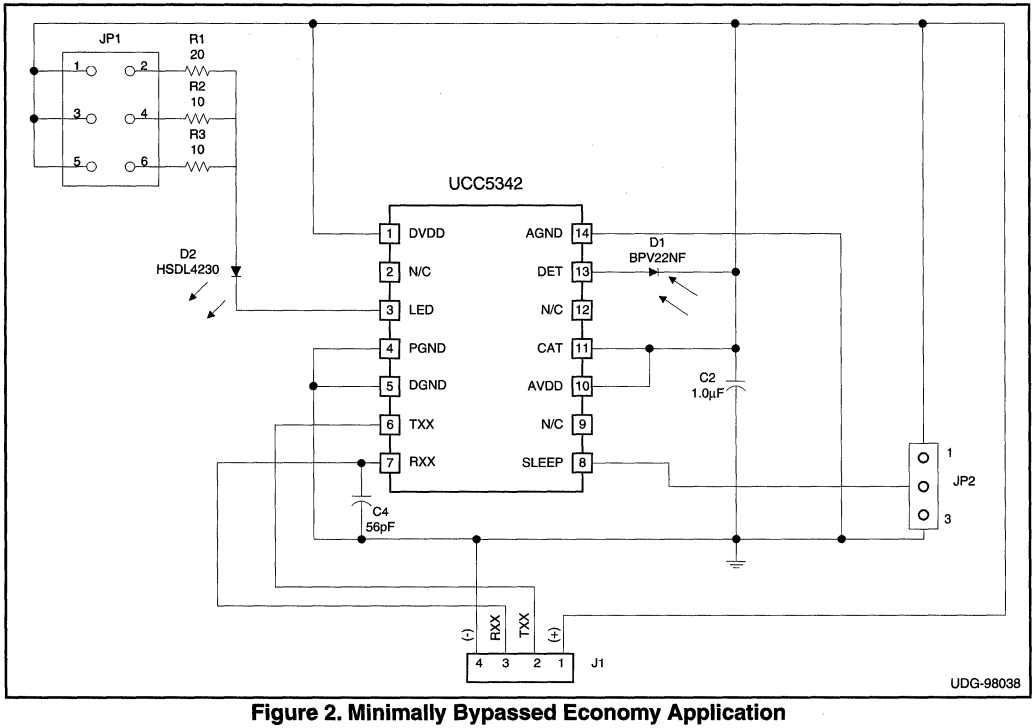

Figure 2. Minimally Bypassed Economy Application

APPLICATIONS INFORMATION

Ground Plane: There are three ground connections shown on the application drawing. They represent the sensitive analog ground, the 'dirty' digital ground, and the high current transmitter or power ground. These three points can simply be geographic groupings of connections to a ground plane. If a ground plane is not used, other provisions to isolate the analog and digital ground currents should be provided. The use of a ground plane is strongly recommended.

DET Considerations: DET is flanked by AGND and an unconnected pin. This should be used to good advantage by fully enclosing the DET circuit board trace with AGND in order to shield leakage noise from DET. The DET circuit board trace length should be minimized. Since the PIN diode connected to DET is capacitive, noise coupling to the cathode of the diode will be coupled directly to DET. For this reason, the 1.0mF capacitor on CAT should be located physically close to the cathode of the PIN diode.

There is natural parasitic coupling from RXX to DET. RXX should be routed to minimize the parasitic capacitive coupling from RXX to DET.

Analog Power Supply De-coupling: The UCC5342 has a highly sensitive amplifier section capable of detecting extremely low current levels (200nA typical). Achieving this sensitivity requires quiet analog power supply rails. A 100nF high frequency capacitor in close proximity to AVDD and AGND is required for quiet analog rails.

The transmitter section of the chip runs from the AVDD supply and draws high peak currents (~ 500 mA in a typical application). A bulk capacitor may be required physically close to the AVDD and AGND pins if the connection length to the power supply is long or if the supply is or appears to be relatively high impedance. This bulk capacitor is in addition to the 100nF high frequency capacitor mentioned above. The bypass capacitors on CAT and AVDD should present very low equivalent series resistance and inductance to the circuit. Suitable capacitors for this purpose are low ESR/ESL tantalums, or ceramic as used on the demo board.

Digital Power Supply: DVDD is fed directly from AVDD through an internal 2k resistor. The DVDD bypass cap handles all transient current produced by the digital section of the chip. If more drive is required from RXX than the internal 2k resistor will allow, an external resistor can shunt it. This should always be accompanied by increasing the value of the de-coupling capacitor on DVDD and AVDD.

Economy Application: The diagram of the economy application shows only one bypass capacitor. This application is suitable where maximum sensitivity is not required and where the power supply feeding AVDD is relatively clean and low impedance.

Digital Output (RXX) Loading Requirements. In most applications, it will be necessary to limit the edge rate on the RXX pin of the UCC5342. The reason for this is glitching on this output caused by coupling from this output to the DET pin. The edge rate is limited by capacitive loading on the pin. A 56pF capacitor will limit the edge rate to about a 100ns rise time. This value proved satisfactory for the demo board.

For more information, pin description and specifications for the UCC5342, please refer to the datasheet or contact your Unitrode Field Applications Engineer.

JUMPER SETTINGS

JP1: This jumper block selects one or a combination of three parallel resistors as a current limit for the IR LED. This setting will determine the transmitter output power. The actual current through the transmitter LED will depend upon the voltage supplied to the circuit. Any or all of the resistors may be used at the same time. See Table 1 and Table 2.

JP2: This jumper places the chip into its normal running mode or its sleep mode according to Table 3.

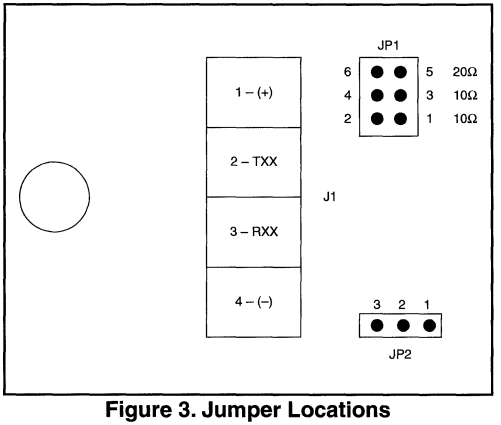

Figure 3. Jumper Locations

POSITION	ADDED RESISTOR
1-2	20Ω
3-4	10Ω
5-6	10Ω

Table 1. JP1 Settings

1-2	3-4	5-6	EFFECTIVE RESISTANCE
X			20Ω
	X		10Ω
X	X		6 2/3Ω
	X	X	5Ω
X	X	X	4Ω

Table 2. Effective LED Resistor

1-2	3-4	MODE
X		Sleep
	X	Run

Table 3. Run/Sleep Mode

REFERENCE DESIGNATOR	PART DESCRIPTION	MANUFACTURER	PART NUMBER
C1	1.0µF, 16V Ceramic Capacitor	Murata	GRM42-6Y5V105Z16BL
C2	1.0µF, 16V Ceramic Capacitor	Murata	GRM42-6Y5V105Z16BL
C3	100nF, 50V Ceramic Capacitor	Murata	GRM42-6X7R104K050BL
C4	56pF,50V Ceramic Capacitor	Murata	GRM42-6COG560J050BD
D1	Infrared Photodiode	Temic	BPV22NF
D2	Infrared LED	Hewlett Packard	HSDL4230
JP1	6 Position Dual Row Header,	AMP	4-103322-0
JP2	3 Position Single Row Header,	AMP	4-103321-0
J1	4 Position Compression Terminal Block	OST	ED1601 (2 required)
R1	20Ω, 1/8W, Metal Film Resistor		
R2	10Ω, 1/8W, Metal Film Resistor		
R3	10Ω, 1/8W, Metal Film Resistor		
U1	115Kbps IrDA Transceiver	Unitrode	UCC5342

Table 4. Parts List

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE
Design Note

UCC5343 Evaluation Board, Schematic and List of Materials

INTRODUCTION

The UCC5343 evaluation board is supplied assembled and ready to test. This board is a complete interface of the IrDA physical layer to a standard UART at speeds up to 115Kbps. The user needs to supply power, an IrDA compliant input pulse train and a UART with an available 16X baud clock to use the board.

The board was built to allow some user configuration. The jumper block J1 allows the user to select the transmitter mode. J2 will put the chip into its run or sleep modes. An area is provided on the board where a mounting hole may be drilled or a clamp may be attached without affecting performance.

The schematic of the board as supplied is shown in Fig. 1.

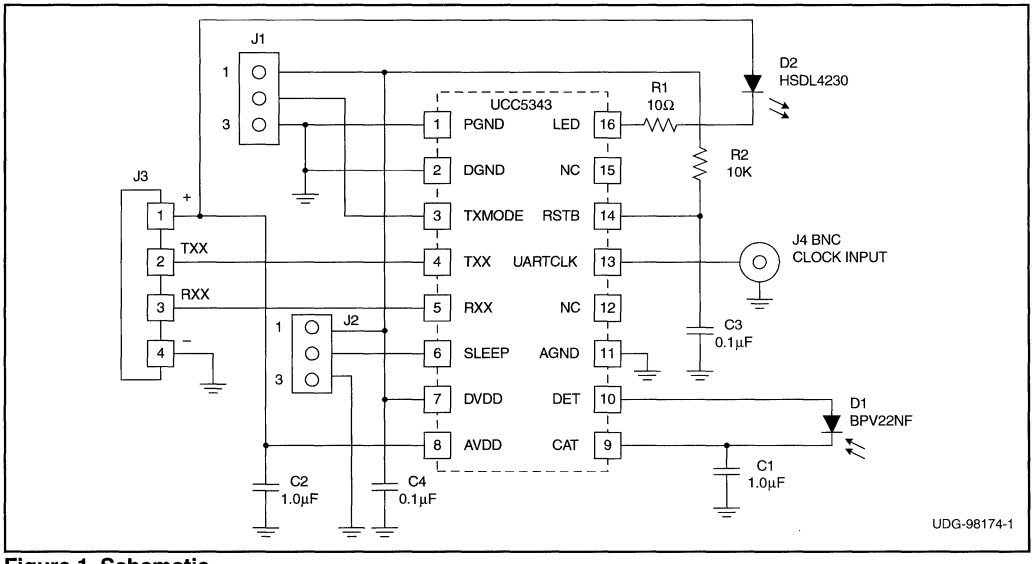

Figure 1. Schematic.

CONNECTIONS TO THE BOARD

There are only five connections to make to the board - two power connections, two signal connections (RXX and TXX) and a clock signal.

Power connections are made at terminals 1 and 4 (positive is 1, negative is 4) on J3. The power supply must be clean, since this part is sensitive to noise on the power supply. The voltage must be between 2.7V and 5.5V. If two boards are being used to talk to each other, separate power supplies for each board are strongly recommended to reduce the possibility of noise coupling from the transmitter board to the receiving board's power supply. The TXX terminal should be connected to the transmit output of a standard UART.

The voltage on this connection should not be allowed to go higher than the voltage at pin 1 of J3. The RXX terminal can be monitored with an oscilloscope or connected to the receive input of a standard UART. The connector marked J4 is for connecting the 16X baud clock from the UART. A BNC connector is used here to minimize the possibility of coupling the UARTCLK signal into the DET line on the UCC5343, and causing erroneous operation. If a coaxial cable is not used to connect this signal, twisted pair is recommended. Connect the pair to the bottom of the board, active line to the center terminal of J4, return line to one of the outer terminals of J4.

Fig. 2 shows a typical connection of the evaluation board to a 16550 type UART.

With this setup, a pair of UARTS can perform half duplex communication over an IR link.

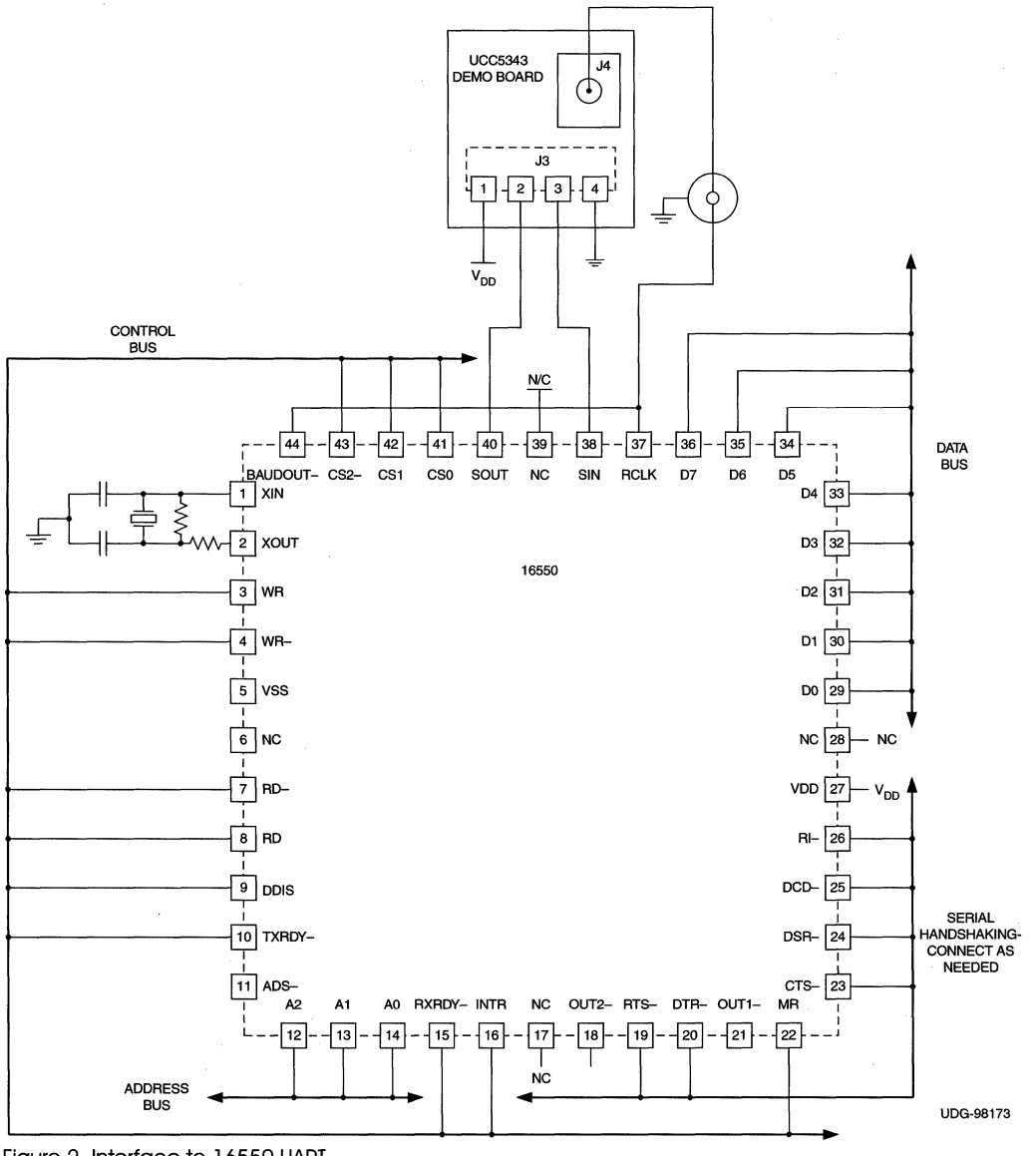

Figure 2. Interface to 16550 UART.

DET Considerations

The DET circuit board trace is surrounded with AGND in order to shield leakage noise from DET. The DET circuit board trace length is minimized. Since the PIN diode connected to DET is capacitive, noise coupling to the cathode of the diode will be coupled directly to DET. For this reason, the 1.0mF capacitor on CAT should be located physically close to the cathode of the PIN diode.

There is natural parasitic coupling from RXX to DET. RXX is routed to minimize the parasitic capacitive coupling from RXX to DET.

It is extremely important to keep the UARTCLK line as far away from the DET and CAT lines as possible. This relatively noisy signal will cause erroneous operation if it is allowed to couple into the IR detection circuitry. As an example, in one application the UARTCLK line was on the opposite side of the board and orthogonal to the DET trace. Even so, there was enough coupling between the two to cause problems.

Analog Power Supply De-coupling

The UCC5343 has a highly sensitive amplifier section capable of detecting extremely low current levels (200nA typical). Achieving this sensitivity requires quiet analog power supply rails. As a minimum, a 100nF high frequency capacitor in close proximity to AVDD and AGND is required for quiet analog rails.

The transmitter section of the chip runs from the AVDD supply and draws high peak currents (~ 500 mA in a typical application). A bulk capacitor may be required physically close to the AVDD and AGND pins if the connection length to the power supply is long or if the supply is or appears to be relatively high impedance. This bulk capacitor is in addition to the 100nF high frequency capacitor mentioned above. The bypass capacitors on CAT and AVDD should present very low equivalent series resistance and inductance to the circuit.

Digital Power Supply

DVDD is fed directly from AVDD through an internal 2K resistor. The DVDD bypass cap handles all transient current produced by the digital section of the chip. If more drive is required from RXX than the internal 2K resistor will allow, an external resistor can shunt it. This technique should always be accompanied by increasing the value of the de-coupling capacitor on DVDD and AVDD.

Jumper Settings

J1: This jumper selects the operating mode of the transmitter encoder in the UCC5343. The two modes available differ in the length of the transmitted pulse that the chip puts out. See Table 1.

J2: This jumper places the chip into its normal running mode or its sleep mode as described in Table 3.

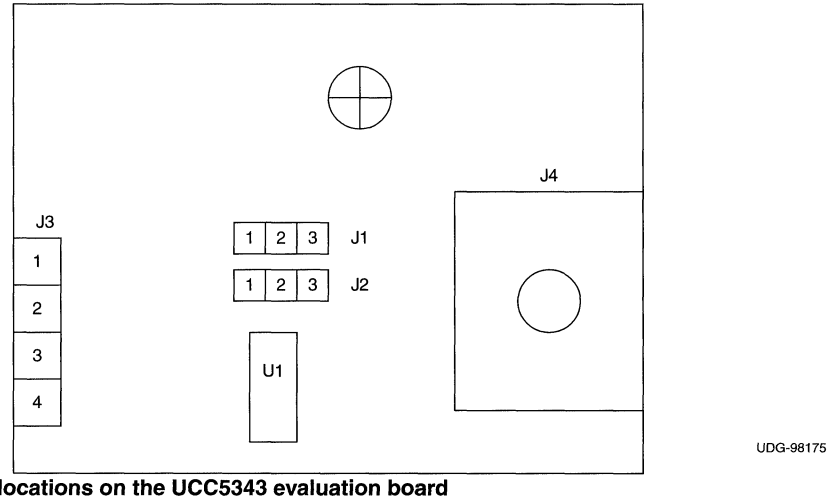

Figure 3. Jumper locations on the UCC5343 evaluation board

Table 1. J1 Settings

Position	Mode
1-2	1.6µs pulse
2-3	3/16 bit time pulse

Table 2. J2 Settings

Position	Mode
1-2	Sleep
2-3	Run

Table 3. Parts List

Designator	Description	Manufacturer	Part Number
C1	1.0µF 16V Ceramic Capacitor	Murata	GRM42-6Y5V105Z16BL
C2	1.0µF 16V Ceramic Capacitor	Murata	GRM42-6Y5V105Z16BL
C3	100nF 50V Ceramic Capacitor	Murata	GRM42-6X7R104K050BL
C4	100nF 50V Ceramic Capacitor	Murata	GRM42-6X7R104K050BL
D1	Infrared Photodiode	Temic	BPV22NF
D2	Infrared LED	Hewlett Packard	HSDL4230
J1	3 Position Single Row Header	AMP	4-103321-0
J2	3 Position Single Row Header	AMP	4-103321-0
J3	4 Position Compression Terminal Block	OST	ED1601 (2 req'd)
J4	BNC Jack	AMP	227699-2
R1	10W, 1/8W Metal Film		Resistor
R2	10K, 1/8W Metal Film		Resistor
U1	115Kbps IrDA Transceiver with Encoder/Decoder	Unitrode	UCC5343

For more complete information, pin descriptions and specifications for the UCC5343, IrDA Transceiver with Encoder/Decoder, please refer to the UCC5343 data sheet or contact your Unitrode Field Applications Engineer at (603) 424-2410.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
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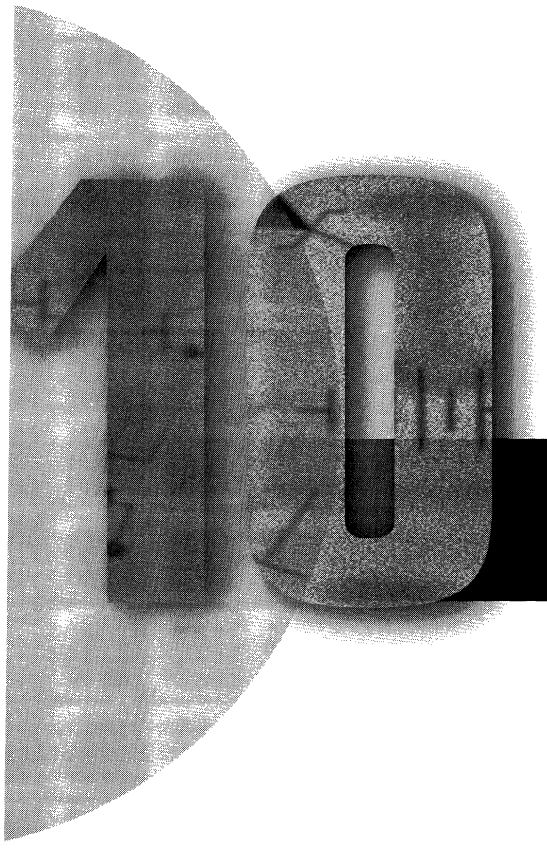


Unitrode Product Portfolio

Interface Products

Nonvolatile Products

Portable Power Products

Power Supply Control Products

SCSI

Multimode / LVD SCSI Active Terminators	UNITRODE PART NUMBER				
	UCC5628+	UCC5630	UCC5632	UCC5638+	UCC5639+
Channels	14	9	9	15	15
Channel Capacitance	4	4	4	4	4
Termination Impedance	Single110, Differential 105, Common Mode 150	Single110, Differential 105, Common Mode 150	Single 110, Differential 105, Common Mode 150	Single 110, Differential 105, Common Mode 150	Single 110, Differential 105, Common Mode 150
Disconnect High or Low	H	H	H	H	L
Termpwr Voltage Range	2.7 - 5.25	2.7 - 5.25	2.7 - 5.25	2.7 - 5.25	2.7 - 5.25
Supports Active Negation	Y	Y	Y	Y	Y
SCSI Hot Plug Current	<10nA	<10nA	<10nA	<10nA	<10nA
Type LVD or SE / LVD	LVD / SE	LVD / SE	LVD / SE	LVD / SE	LVD / SE
Page Number	IF/3-78	IF/3-83	IF/3-93	IF/3-94	IF/3-99

Multimode / LVD SCSI Active Terminators	UNITRODE PART NUMBER				
	UCC5640+	UCC5641+	UCC5646		
Channels	9	9	27		
Channel Capacitance	3	3	3		
Termination Impedance	Differential 105, Common Mode 150	Differential 105, Common Mode 150	Differential 105, Common Mode 150		
Disconnect High or Low	H	L	H		
Termpwr Voltage Range	2.7 - 5.25	2.7 - 5.25	2.7 - 5.25		
SCSI Hot Plug Current	<10nA	<10nA	<10nA		
Type LVD or SE / LVD	LVD	LVD	LVD		
Page Number	IF/3-104	IF/3-108	IF/3-112		

+ New Product

SCSI (cont.)

Multimode / LVD SCSI Active Terminators	UNITRODE PART NUMBER				
	UCC5510+	UCC5630A	UCC5672+	UCC5680	
Channels	9	9	9	9	
Channel Capacitance	4	4	4	4	
Termination Impedance	Single110, Differential 105, Common Mode 150	Single110, Differential 105, Common Mode 150	Single110, Differential 105, Common Mode 150	Single 110, Differential 105, Common Mode 150	
Diff B input filter	N	N	Y	Y	
Disconnect High or Low	N/A	H	H	H	
Termpwr Voltage Range	2.7 - 5.25	2.7 - 5.25	2.7 - 5.25	2.7 - 5.25	
Supports Active Negation	Y	Y	Y	Y	
SCSI Hot Plug Current	<10nA	<10nA	<10nA	<10nA	
Type LVD or SE / LVD	LVD / SE	LVD / SE	LVD / SE	LVD	
Page Number	IF/3-5	IF/3-87	IF/3-120	IF/3-121	

Single Ended SCSI Active Terminators	UNITRODE PART NUMBER				
	UC5601	UC5602	UC5603	UC5604	UC5605
Channels	18	18	9	9	9
Channel Capacitance	10	11	6	9	4
Termination Impedance	110	110	110	110	110
Disconnect High or Low	H	H	H	H	L
Termpwr Voltage Range	4 - 5.25	4 - 5.25	4 - 5.25	4 - 5.25	4 - 5.25
Supports Active Negation	N	N	Y	N	Y
SCSI Hot Plug Current	<10nA	<10nA	<10nA	<10nA	<10nA
Type SE, LVD or SE / LVD	SE	SE	SE	SE	SE
Page Number	IF/3-9	IF/3-13	IF/3-18	IF/3-22	IF/3-26

+ New Product

SCSI (cont.)

Single Ended SCSI Active Terminators	UNITRODE PART NUMBER				
	UCC5606	UC5607	UC5608	UC5609	UC5612
Channels	9	18	18	18	9
Channel Capacitance	1.8	8	6	6	4
Termination Impedance	110 & 2500	110	110	110	110
Disconnect High or Low	L	2L	H	L	H
Termpwr Voltage Range	2.7 - 5.25	4 - 5.25	4 - 5.25	4 - 5.25	4 - 5.25
Supports Active Negation	Y	Y	Y	Y	Y
SCSI Hot Plug Current	<10nA	<10nA	<10nA	<10nA	<10nA
Type SE, LVD or SE / LVD	SE	SE	SE	SE	SE
Page Number	IF/3-30	IF/3-34	IF/3-37	IF/3-40	IF/3-43

Single Ended SCSI Active Terminators	UNITRODE PART NUMBER				
	UC5613	UCC5614	UCC5617	UCC5618	UCC5619
Channels	9	9	18	18	27
Channel Capacitance	3	1.8	2.5	2.5	3
Termination Impedance	110	110 & 2500	110	110	110
Disconnect High or Low	H	H	L	H	L
Termpwr Voltage Range	4 - 5.25	2.7 - 5.25	4 - 5.25	4 - 5.25	4 - 5.25
Supports Active Negation	Y	Y	Y	Y	Y
SCSI Hot Plug Current	<10nA	<10nA	<10nA	<10nA	<10nA
Type SE, LVD or SE / LVD	SE	SE	SE	SE	SE
Page Number	IF/3-47	IF/3-51	IF/3-55	IF/3-59	IF/3-63

+ New Product

SCSI (cont.)

Single Ended SCSI Active Terminators	UNITRODE PART NUMBER				
	UCC5620	UCC5621	UCC5622		
Channels	27	27	27		
Channel Capacitance	3	3	3		
Termination Impedance	110	110	110		
Disconnect High or Low	H	Split Low	Split High		
Termpwr Voltage Range	4 - 5.25	4 - 5.25	4 - 5.25		
Supports Active Negation	Y	Y	Y		
SCSI Hot Plug Current	<10nA	<10nA	<10nA		
Type SE, LVD or SE / LVD	SE	SE	SE		
Page Number	IF/3-66	IF/3-70	IF/3-74		

Special Functions Circuit	UNITRODE PART NUMBER			
	UCC5661			
Part Name	Ethernet Coaxial Impedance Monitor			
Description	Contains all the Functions Required to Monitor Ethernet Coaxial Systems and is Compatible with IEEE 802.3, 10Base5, 10Base2, and 10BaseT			
Page Number	IF/3-112			

+ New Product

Bus Bias Generators

Special Functions	UNITRODE PART NUMBER				
	UC382	UC385	UC560	UCC561+	UC563+
Bus Standard	GTL / BTL	GTL / BTL	SCSI-1,2,3	SPI-2,3	VME / VME64
Sink / Source Current	Pgm / 3A	Pgm / 5A	300mA / –750mA	200mA / –200mA	475mA / –575mA
Page Number	PS/4-2	PS/4-8	IF/4-3	IF/4-7	IF/4-10

+ New Product

Hot Swap Power Managers

Hot Swap Power Managers	UNITRODE PART NUMBER				
	UCC3912	UCC3913	UC3914	UCC3915	UCC39151
Voltage Range	3V to 8V	–10.5V to External Limitation	5V to 35V	7V to 15V	7V to 15V
Current Range	0A to 3A	Externally Limited	Externally Limited	0A to 3A	0A to 3A
Integrated Power FET	Y	N	N	Y	Y
RDSon	150mΩ	N/A	N/A	150mΩ	150mΩ
Programmable Fault Threshold	Y	Y	Y	Y	Y
Programmable Time Delay	Y	Y	Y	Y	Y
Latched Fault Mode	N	Y	Y	N	N
Average Power Limiting	N/A	Y	Y	N/A	N/A
Application / Design Note	DN-58, DN-68, U-151	DN-67		DN-58, DN-68, U-151	DN-58, DN-68, U-151
Available Package	TSSOP, SOIC or PDIP	SOIC or PDIP	SOIC or PDIP	TSSOP, SOIC or PDIP	TSSOP, SOIC or PDIP
Page Number	IF/5-9	IF/5-15	IF/5-23	IF/5-37	IF/5-42

Hot Swap Power Managers	UNITRODE PART NUMBER				
	UCC3916	UCC39161	UCC3917+	UCC3918	UCC3919
Voltage Range	4V to 6V	4V to 6V	10V to External Limitation	3V to 6V	3V to 8V
Current Range	–1.8A to –1.5A	–1A to –0.7A	Externally Limited	0A to 4A	Externally Limited
Integrated Power FET	Y	Y	N	Y	N
RDSon	220mΩ	220mΩ	N/A	60mΩ	N/A
Programmable Fault Threshold	N	N	Y	Y	Y
Programmable Time Delays	Y	Y	Y	Y	Y
Latched Fault Mode	N	N	Y	N	Y
Average Power Limiting	N/A	N/A	Y	N/A	Y
Application / Design Note			DN-98	DN-87	DN-95
Available Package	SOIC or PDIP	SOIC or PDIP	SOIC or PDIP	SOIC or PDIP	SOIC or PDIP
Page Number	IF/5-47	IF/5-50	IF/5-53	IF/5-61	IF/5-68

+ New Product

Hot Swap Power Managers (cont.)

Hot Swap Power Managers	UNITRODE PART NUMBER				
	UCC3921	UCC3995+	UCC3996+		
Voltage Range	–10.5V to External Limitation	2.75V to 5.5V	2.75V to 13.6V Two Supplies Sequenced		
Current Range	Externally Limited	Externally Limited	Externally Limited		
Integrated Power FET	N	N	N		
RDSon	N/A	N/A	N/A		
Programmable Fault Threshold	Y	Y	Y		
Programmable Time Delay	Y	Y	Y		
Latched Fault Mode	Y	N	Y		
Average Power Limiting	Y	Y	Y		
Application / Design Note					
Available Package	SOIC or PDIP	TSSOP or SOIC	TSSOP, SOIC or PDIP		
Page Number	IF/5-78	IF/5-98	IF/5-100		

Special Functions	UNITRODE PART NUMBER				
	UCC3831	UCC38531	UCC3981+	UCC39811+	UCC3985+
Part Name	Universal Serial Bus Power Controller	Universal Serial Bus Power Controller	Universal Serial Bus Power Controller	Universal Serial Bus Power Controller	CompactPCI Hot Swap Power Manager
Description	Powers Four 5V Peripherals and One 3.3V USB Controller	Powers Four 5V Peripherals and One 3.3V USB Controller	Powers Four 5V Peripherals and One 3.3V USB Controller	Powers Four 5V Peripherals and One 3.3V USB Controller	Fully CompactPCI Compliant. Four Channels for Individual Control of Four Supplies 12V, –12V, 5V, and 3.3V
Application / Design Note					
Available Package	SOIC or PDIP	SOIC or PDIP	SOIC or PDIP	SOIC or PDIP	TSSOP, SOIC or PDIP
Page Number	IF/5-3	IF/5-6	IF/5-88	IF/5-91	IF/5-94

+ New Product

Drivers / Receivers Transceivers

Interface Drivers, Receivers	UNITRODE PART NUMBER				
	UC5170C	UC5171	UC5172	UC5180C	UC5181C
Drivers	8	8	8		
Receivers				8	8
Power	±10V	±10V	±10V	+5V	+5V
EIA232 / V.28	Y	Y	Y	Y	Y
EIA423 / V.10	Y	Y	Y	Y	Y
EIA422 / V.11	N	N	N	Y	Y
V.35	N	N	N	Y	Y
Appletalk	N	N	N	N	Y
Page Number	IF/6-3	IF/6-7	IF/6-11	IF/6-15	IF/6-18

+ New Product

Interface Transceivers	UNITRODE PART NUMBER				
	UC5350	UC5351+			
Drivers	1	1			
Receivers	1	1			
Power	+5V	+5V to 24V			
Control Area Network	Y	Y			
Device Net	Y	Y			
SDS	Y	Y			
Page Number	IF/6-21	IF/6-27			

+ New Product

Unitrode nonvolatile controllers provide power monitoring, write-protection, and supply switching to convert standard SRAM and a backup battery into a reliable, predictable nonvolatile memory. The nonvolatile controller modules are complete battery-backup solutions including an encapsulated 130mAh lithium cell that is isolated until power is applied.

- Power monitoring and switching for 3V battery-backup applications
- 5V V_{CC} operation
- Automatic write-protection during power-up/power-down cycles
- Automatic switching from V_{CC} to first backup battery and from first backup battery to second backup battery
- Battery internally isolated until power is first supplied
- Industrial temperature range available

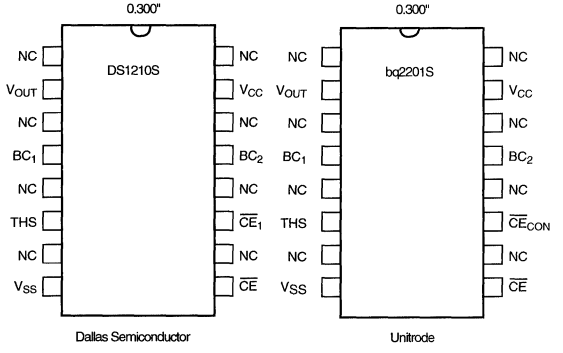
Static-RAM Nonvolatile Controller Selection Guide

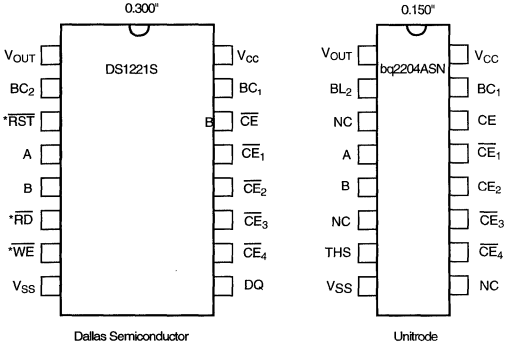
SRAM Banks Controlled	Battery Monitor Outputs	Reset Output	I_{OUT} (Typ.)	Pins / Package	Part Number	Page Number
1			160 mA	8 / NDIP, NSOIC 16 / NSOIC	bq2201	NV/3-3
2		✓	160 mA	16 / NDIP, NSOIC	bq2202	NV/3-11
2	✓	✓	160 mA	16 / NDIP, NSOIC	bq2203A	NV/3-19
4			160 mA	16 / NDIP, NSOIC	bq2204A	NV/3-27
2		✓	160 mA	12 / DIP module	bq2502	NV/3-35

Static-RAM Nonvolatile Controller Cross-Reference	
Dallas Semiconductor	**Unitrode**
DS1210	bq2201PN [1, 2]
DS1210S	bq2201S [1, 2]
DS1218	bq2201PN [1, 2]
DS1218S	bq2201SN [1, 2]
DS1221	bq2204APN [1, 3]
DS1221S	bq2204ASN [1, 3, 4]

Notes:

1. Unitrode's bq2201 and bq2204A do not incorporate a "check battery status" function.
2. Unitrode's bq2201 pins THS and BC_2 should be tied to V_{SS}.
3. Optional "security feature" DS1221 pins are no-connect on the bq2204A.
4. Unitrode's bq2204ASN is a small 16-pin, 150-mil SOIC, compared to the DS1221S, which is a 16-pin, 300-mil SOIC.





*These pairs must be connected to ground if the security option is not used.

Nonvolatile SRAMs and RTCs (NV) Selection Guides

Unitrode's NVSRAMs integrate extremely low standby power SRAM, nonvolatile control circuitry, and a long-life lithium cell in either a single DIP package or a two-piece LIFETIME LITHIUM SMT module. The NVSRAMs combine secure long-term nonvolatility (more than 10 years without power) with standard SRAM pinouts and fast, unlimited read/write operation.

- ➤ Data retention without power
- ➤ Automatic write-protection during power-up/power-down cycles
- ➤ Industry-standard pinout
- ➤ Conventional SRAM operation; unlimited write cycles
- ➤ 10 or 5 years minimum data retention in the absence of power
- ➤ Battery internally isolated until power is first supplied
- ➤ Industrial temperature range available

Nonvolatile Static RAM Selection Guide

Density	Config-uration	Access Time (ns)	Minimum Data-Retention Time	Pins / Package	Part Number[1]	Page Number
64Kb	8Kb x 8	70, 85[2], 150[2], 200	10 years	28 / DIP	bq4010/Y	NV/5-3
256Kb	32Kb x 8	70[2], 100, 150[2], 200	10 years	28 / DIP	bq4011/Y	NV/5-13
1Mb	128Kb x 8	70[2], 85[2], 120	10 years	32 / DIP 32 / SMT	bq4013/Y	NV/5-23
2Mb	256Kb x 8	85, 120	10 years	32 / DIP	bq4014/Y	NV/5-33
4Mb	512Kb x 8	70, 85, 120	10 years	32 / DIP 32 / SMT	bq4015/Y	NV/5-42
8Mb	1024Kb x 8	70	10 years	36 / DIP	bq4016Y	NV/5-52
16Mb	2048Kb x 8	70	5 years	36 / DIP	bq4017Y	NV/5-61
64Kb	8kB x 8	70	10 years	28 / SNAPHAT	bq4310/Y+	NV/5-70
256Kb	32kB x 8	70[3], 100[5]	10 years	28 / SNAPHAT	bq4311Y/L[4]+	NV/5-81

Notes:
1. "Y" version denotes 10% V_{CC} tolerance.
2. "Y" version available in -40°C to +85°C industrial temperature range.
3. "Y" version only.
4. "L" version denotes 3.2V typical Vcc operation.
5. "L" version only.

+ New Product

Nonvolatile Static RAM Cross-Reference			
Density	Dallas Semiconductor	STMicroelectronics	Unitrode
64Kb	DS1225AB	M48Z08	bq4010
	DS1225AD	M48Z18	bq4010Y
	-	M48Z58	bq4010/4823Y
	DS1225Y	M48Z58Y	bq4010Y
256Kb	DS1230AB	M48Z35	bq4011
	DS1230Y	M48Z35Y	bq4011Y/4833Y
1M	DS1245AB	M48Z128	bq4013
	DS1245Y	M48128Y	bq4013Y
2M	DS1258AB	-	bq4014
	DS1258Y	-	bq4014Y
4M	DS1250AB	M48Z512A	bq4015
	DS1250Y	M48Z512AY	bq4015Y
8M	DS1265AB	-	bq4016
	DS1265Y	-	bq4016Y
16M	DS1270AB	M48Z2M1	bq4017
	DS1270Y	M48Z2M1Y	bq4017Y

Nonvolatile SRAMs and RTCs (NV) Selection Guides

Unitrode's real-time clocks (RTCs) provide highly integrated clock/calendar solutions for microcomputer-based designs. Each *module* is a completely self-contained unit, including IC, crystal, and a battery ensuring operation for 10 years in the absence of power. The very compact, low-power *ICs* need only a battery and a crystal for operation. NVSRAM controller versions allow users to make inexpensive SRAM nonvolatile for data and configuration storage in computers, portable equipment, office machines, and other applications.

- ➤ Clock/calendar counts seconds through years with daylight savings and leap-year adjustments
- ➤ IBM PC AT-compatible clocks include:
  - — 5- or 3-Volt operation
  - — 114, 240, or 242 bytes of user nonvolatile RAM storage
- ➤ 32kHz output for power management
- ➤ Nonvolatile control for an external SRAM
- ➤ SRAM-based clocks feature:
  - — SRAM interface
  - — Up to 512 kilobytes of NVSRAM
  - — CPU supervisor
- ➤ One minute per month clock accuracy in modules
- ➤ IC versions require only a crystal and battery

Real-Time Clock Selection Guide

Onboard RAM (bytes)	NVRAM Control	Bus Interface	Voltage	32kHz Output	CPU Supervisor	Pins / Package	Part Number	Page Number
114		Muxed	5V			24 / DIP, SOIC	bq3285	NV/4-3
242		Muxed	5V	✓		24 / DIP, SOIC, SSOP	bq3285E	NV/4-22
242		Muxed	5V	✓		24 / SSOP	bq3285EC/ED	NV/4-46, NV/4-69
242		Muxed	3V	✓		24 / DIP, SOIC, SSOP	bq3285L	NV/4-22
242		Muxed	3V	✓		24 / SSOP	bq3285LC/LD	NV/4-46, NV/4-69
240		Muxed	3V			24 / SSOP	bq3285LF+	NV/4-92
114		Muxed	5V			24 / DIP module	bq3287/A	NV/4-111
242		Muxed	5V	✓		24 / DIP module	bq3287E/EA	NV/4-115
242		Muxed	3V			24 / DIP Module	bq3287LD+	NV/4-119
114	✓	Muxed	5V			24 / DIP, SOIC	bq4285	NV/4-123
114	✓	Muxed	5V	✓		24 / DIP, SOIC, SSOP,	bq4285E	NV/4-143
114	✓	Muxed	3V	✓		24 / DIP, SOIC, SSOP	bq4285L	NV/4-143
114	✓	Muxed	5V			24 / DIP module	bq4287	NV/4-168
0		SRAM	3V		✓	28 / DIP, SOIC 28 / SNAPHAT	bq4802+	NV/4-174
8K	✓	SRAM	5V		✓	28 / DIP module	bq4822Y	NV/4-176
8K		SRAM	5V			28 / SNAPHAT	bq4823Y+	NV/4-191

+ New Product

Real-Time Clock Selection Guide (Continued)

Onboard RAM (bytes)	NVRAM Control	Bus Interface	Voltage	CPU Supervisor	Pins / Package	Part Number	Page Number
32K		SRAM	5V		28 / DIP module	bq4830Y	NV/4-205
32K		SRAM	5V	✓	32 / DIP module	bq4832Y	NV/4-218
32K		SRAM	5V		28 / SNAPHAT	bq4833Y+	NV/4-233
128K		SRAM	5V	✓	32 / DIP module	bq4842Y	NV/4-247
0	✓	SRAM	5V	✓	28 / DIP, SOIC	bq4845/Y	NV/4-262
0	✓	SRAM	5V	✓	28 / DIP module	bq4847/Y	NV/4-279
512K		SRAM	5V	✓	32 / DIP module	bq4850Y	NV/4-282
512K		SRAM	5V	✓	36 / DIP module	bq4852Y	NV/4-295

+ New Product

Real-Time Clock Cross-Reference

Dallas Semiconductor	STMicroelectronics	Unitrode
DS1285/885	-	bq3285P
DS1285S/885S	-	bq3285S
DS1287/887	-	bq3287MT
DS1287A/887A	M48T86	bq3287A
DS14285	-	bq4285
DS14285	-	bq4285P
DS14285S	-	bq4285S
DS14287	-	bq4287
DS1643	M48T08/T18 M48T58Y/59Y	bq4822Y
DS1644	M48T35	bq4830Y[1]
DS1646	-	bq4842Y[2]

Notes:
1. Memory upgrade.
2. Additional bq4842 features: microprocessor reset, watchdog monitor, clock alarm, and periodic interrupt.

Portable Power (PP) Selection Guides

Unitrode battery charge-management ICs provide full-function, safe charge control for all types of rechargeable chemistries. Functions include pre-charge qualification and conditioning, charge regulation, and termination.

- ➤ Fast charging and conditioning of nickel cadmium, nickel metal hydride, lead acid, lithium ion, or rechargeable alkaline batteries
- ➤ Flexible charge regulation support:
  - — Linear
  - — Switch-mode
  - — Gating control (external regulator)
- ➤ Easily integrated into systems or as a stand-alone charger
- ➤ Direct LED outputs display battery and charge status
- ➤ Fast, safe, and reliable chemistry-specific charge-termination methods, including rate of temperature rise ($\Delta T/\Delta t$), negative delta voltage ($-\Delta V$), peak voltage detect (PVD), minimum current, maximum temperature, maximum voltage, and maximum time
- ➤ Optional top-off and maintenance charging
- ➤ Discharge-before-charge option for NiCd
- ➤ Complete set of development tools available for quick product-desig

Battery Charge-Management Selection Guide

Battery Technology	Key Features	Fast-Charge Termination Method	Pins / Package	Part Number	Page Number
Multi-Chemistry	Complete change management with integrated switching controller	PVD, minimum current, maximum temperature, maximum time	8/0.300" DIP, 8/0.150" SOIC	bq2000+	PP/3-7
		$\Delta T/\Delta$, minimum current, maximum temperature, maximum time	8/0.300" DIP, 8/0.150" SOIC	bq2000T+	PP/3-20
NiMH, NiCd	Gating control of an external regulator	$-\Delta V$, PVD, maximum temperature, maximum time	8/0.300" DIP, 8/0.150" SOIC	bq2002/C/E/F/G	PP/3-3
		$\Delta T/\Delta t$, maximum temperature, maximum time	8/0.300" DIP, 8/0.150" SOIC	bq2002D/T	PP/3-3
	PWM Controller	$-\Delta V$, $\Delta T/\Delta t$, maximum temperature, maximum time	16/0.300" DIP, 16/0.300" SOIC	bq2003	PP/3-73
	PWM controller, enhanced display mode	$-\Delta V$, PVD, $\Delta T/\Delta t$, maximum temperature, maximum time	16/0.300" DIP, 16/0.150" SOIC	bq2004/E/H	PP/3-5
	Dual sequential charge-controller for 2-bay chargers	$-\Delta V$, $\Delta T/\Delta t$, maximum temperature, maximum time	20/0.300" DIP, 20/0.300" SOIC	bq2005	PP/3-119
Lithium Ion	PWM controller	Minimum current, maximum time	16/0.300" DIP, 16/0.150" SOIC	bq2054	PP/3-6
	Low-dropout linear with AutoComp™ feature	-	8/0.150" SOIC	bq2056/T/V	PP/3-186
	PWM controller, enhanced display mode	Minimum current, maximum time	16/0.300" DIP, 16/0.150" SOIC	bq2954+	PP/3-6
	PWM controller, differential current sense	Minimum current, maximum time	20/0.300" DIP, 20/0.300" SOIC	UCC3956	PP/3-6

+ New Product

Continued on next page

Battery Charge-Management Selection Guide (Continued)

Battery Technology	Key Features	Fast-Charge Termination Method	Pins/ Package	Part Number	Page Number
Lead Acid	PWM controller, 3 charge algorithms	Maximum voltage, $-\Delta^2V$, minimum current, maximum time	16/0.300" DIP, 16/0.150" SOIC	bq2031	PP/3-154
	Linear controller	Maximum voltage, minimum current	16/0.300" DIP 16/0.300"SOIC	UC3906	PP/3-237
	PWM controller, differential current sense	Maximum voltage, minimum current	20/0.300" DIP 20/0.300"SOIC	UC3909	PP/3-244
Rechargeable Alkaline	2-cell charging	Maximum voltage	8/0.300"DIP, 8/0.150" SOIC	bq2902	PP/3-194
	3- or 4-cell charging	Maximum voltage	14/0.300" DIP, 14/0.150" SOIC	bq2903	PP/3-204

The bq2002 fast-charge control ICs are low-cost CMOS battery charge-control ICs providing reliable charge termination for both NiCd and NiMH battery applications. Controlling a current-limited or constant-current supply allows the ICs to be the basis for a cost-effective stand-alone or system-integrated charger. The bq2002 family includes options that integrate fast charge, top-off, and pulse-trickle charge control in a single IC for charging one or more NiCd or NiMH batteries.

A new charge cycle is started by the application of a charging supply or by replacement of the battery. For safety, fast charge is inhibited if the battery voltage or temperature is outside of configured limits. Fast charge may be inhibited using the INH input. In some versions, this input may be used to synchronize voltage sampling. A low-power standby mode reduces system power consumption.

- Fast-charge control of nickel cadmium or nickel-metal hydride batteries
- Fast-charge terminations available:
  - -ΔV
  - Peak Voltage Detection (PVD)
  - ΔT/Δt
- Direct LED output displays charge status
- Backup safety termination on maximum voltage, maximum temperature, and maximum time
- Top-off and pulse-trickle charge rates available
- Synchronized voltage sampling available
- Low-power mode
- 8-pin 300-mil DIP or 150-mil SOIC packaging

bq2002 Family Selection Guide

	Part Number						
	-ΔV or PVD Termination					ΔT/Δt Termination	
Feature	bq2002	bq2002F	bq2002C	bq2002E	bq2002G	bq2002T	bq2002D
Fast charge time limit options (minutes)	160/80/40	160/100/40	160/80/40	200/80/40	160/80/40	320/80/40	440/110/55
Hold-off period options (seconds)	600/300/10	600/300/10	300/150/75	300/150/75	300/150/75	none	none
Top-off options	C/32,C/16,0	C/32,C/16,0	none	C/16,0	C/16,0	C/64,C/16,0	none
Top-off period	4.6ms	4.6ms	n/a	1.17s	1.17s	4.6ms	n/a
Pulse-trickle options	C/64,C/32	C/64,C/32	C/32	C/32	C/32	C/256,C/128	none
Pulse-trickle period	9 or 18ms	9 or 18ms	1.17s	1.17s	1.17s	18 or 73ms	n/a
Synchronized voltage sampling	no	no	yes	yes	yes	no	no
Minimum voltage pre-charge qualification	no	no	yes	yes	yes	no	no

Continued on next page

bq2002 Family Selection Guide (Continued)

	Part Number						
	-ΔV or PVD Termination					ΔT/Δt Termination	
Feature	bq2002	bq2002F	bq2002C	bq2002E	bq2002G	bq2002T	bq2002D
Hysteresis on high-temperature cut-off	no	no	no	no	no	yes	yes
LED in "charge pending" phase	n/a	n/a	flashes	flashes	flashes	on	off
Page number	PP/3-35	PP/3-35	PP/3-43	PP/3-61	PP/3-61	PP/3-51	PP/3-51

The bq2004 fast-charge control ICs are low-cost CMOS battery charge control ICs providing reliable charge termination for both NiCd and NiMH battery applications. Integration of PWM current control circuitry allows the ICs to be the basis for a cost-effective stand-alone or system-integrated charger. The bq2004 family includes options that integrate fast charge, top-off, and pulse-trickle charge control in a single IC for charging one or more NiCd or NiMH batteries.

A new charge cycle is started by the application of a charging supply, replacement of the battery, or a logic-level pulse. For safety, fast charge is inhibited if the battery voltage or temperature is outside of configured limits. Fast charge may be inhibited using the INH input, which also puts the IC into a low-power standby mode, reducing system power consumption.

- Fast-charge control of nickel cadmium or nickel-metal hydride batteries
- Integrated PWM closed-loop current control
- Configurable, direct LED output displays charge status
- Low-power mode
- Top-off and pulse-trickle charging available
- Fast-charge terminations available:
  - $-\Delta V$
  - Peak Voltage Detection (PVD)
  - $\Delta T/\Delta t$
- Backup safety termination on maximum voltage, maximum temperature, and maximum time
- 16-pin 300-mil DIP or 150-mil SOIC packaging

bq2004 Family Selection Guide

Feature	Part Number bq2004	bq2004E	bq2004H
Maximum time-out selections (minutes)	360/180/90/45/23	325/154/77/39/19	650/325/154/77/39
Hold-off period selections (seconds)	137/820/410/200/100	137/546/273/137/68	273/546/546/273/137
Charge rate during hold-off period	full fast-charge rate	1/8*fast-charge rate	1/8*fast-charge rate
Top-off options	C/2,C/4,C/8,C/16,0	C/2,C/4,C/8,C/16,0	C/4,C/8,C/16,C/32,0
Top-off pulse width/period (seconds)	260/2080	260/2080	260/2080
Top-off duration	MTO	0.235*MTO	0.235*MTO
Pulse-trickle selections	C/32,C/64,0	C/512,0	C/512,0
Pulse-trickle period (ms)	4.17/8.3/16.7/33.3/66.7	66.7/133/267/532	33.3/66.7/133/267
Pulse-trickle pulse width (seconds)	260	260	260
DSEL floating disables pulse-trickle	no	yes	yes
VSEL high disables low-temperature fault threshold	yes	no	no
High-temperature fault threshold	1/4LTF + 3/4 TCO	1/3LTF + 2/3 TCO	1/3LTF + 2/3 TCO
Page number	PP/3-91	PP/3-105	PP/3-105

Li-Ion PWM Charge IC Selection Guide

Feature	Part Number bq2054	bq2954	UCC3956
Charge algorithm	During pre-qualification, the bq2054 charges using a low trickle current if the battery voltage is low. Then it charges using constant current followed by constant volatge. After fast-charge termination, charge is re-initiated by resetting the power to the IC or by inserting a new battery.	Performs similar to the bq2054, but the bq2954 also re-initiates a recharge if the battery voltage falls below a threshold level. This allows the bq2954 to maintain a full charge in the battery at all times.	Uses a 4-step charge algorithm: low-current trickle charge (when the cell voltage is below a user- programmable level); high- current bulk charge; constant-voltage overcharge; optional top-off with user-programmable timer
Current-sensing technique	Low-side current sensing	Low-side and high-side current sensing	Fully differential high-side current sensing can be used up to 20V common mode without the need for external level shifting.
Charge initiation	Application of power or detection of battery insertion	Application of power or detection of battery insertion	One-shot charge initiates charging, or a simple comparator initiates charging on battery insertion.
Detection of deeply discharged (bad) cells	Minimum cell voltage required for fast charge: 2V/cell Trickle-charge period: 1 * MTO	Minimum cell voltage required for fast charge: 3V/cell Trickle-charge period: 0.25 * MTO (for faster detection of bad cells)	User-programmable threshold limits charge current when battery cells are deeply discharged and provides short-circuit protection.
Charge termination based on minimum current	User-programmable minimum current is a ratio of the charging current: 1/10, 1/20, 1/30. A safety charge timer is also available.	User-programmable minimum current is a ratio of the charging current: 1/10, 1/15, 1/20. A safety charge timer is also available.	User-programmable minimum current or user-programmable overcharge timer
Temperature monitoring	Measured using an external thermistor. Fast charge is inhibited if the battery temperature is outside user-configured limits.	Measured using an external thermistor. Fast charge is inhibited if the battery temperature is outside user-configured limits.	No
Status display	3 LEDs for state of charge	2 LEDs or one bi-color LED optimize state of charge	2 LEDs for state of charge including end of charge
Full-charge indication	LEDs indicate full charge after charge termination	LEDs indicate full charge just before charge termination	LEDs indicate full charge on charge termination
Input voltage range	4.5V to 5.5V	4.5V to 5.5V	6.5V to 20V
Typical supply current	2mA	2mA	5mA
Voltage regulation accuracy	±1% at 25°C	±1% at 25°C	±1% at 25°C
Wakeup feature for battery pack protectors	No	Yes	No
Integrated PWM controller	Yes	Yes	Yes
Pins/package	16-pin narrow PDIP or SOIC	16-pin narrow PDIP or SOIC	20-pin SOIC or DIP
Page number	PP/3-170	PP/3-217	PP/3-253

Portable Power (PP) Selection Guides

Unitrode's Gas Gauge ICs measure the available charge, calculate self-discharge, and communicate the available charge of a battery pack over a serial port or by directly driving an LED display.

- Accurate measurement of available charge for nickel cadmium, nickel metal-hydride, lithium ion, lead-acid batteries, and primary lithium
- Designed for battery-pack integration
- 150µA or less typical operating current
- Serial port or direct LED display for remaining battery capacity indication
- Available capacity is compensated for charge/discharge rate and temperature
- Accurately measures across a wide range of currents

Battery Capacity-Monitoring ICs Selection Guide

Battery Technology	Approximate Pack Capacity (mAh)	Communication Interface	Additional Key Features	Pins / Package	Part Number	Page Number
NiCd/NiMH	800-5000	1-wire DQ	5 or 6 LED outputs	16 /SOIC	bq2010	PP/4-3
			Slow-charge control	16 /SOIC	bq2012	PP/4-81
			External charge-control support	16 /SOIC	bq2014	PP/4-123
		1-wire HDQ	Register-compatible with bq2050H	16 /SOIC	bq2014H+	PP/4-149
NiCd	800-2000	1-wire DQ	See bq2011 Family Selection Guide	16 /SOIC	bq2011 bq2011J bq2011K	PP/4-24, PP/4-45, PP/4-63
NiCd/NiMH/ Lead Acid	2000-10,000	1-wire HDQ	Programmable offset and load compensation	16 /SOIC	bq2013H	PP/4-103
Li-Ion	800-5000	1-wire DQ	Remaining power (Wh) indication	16 /SOIC	bq2050	PP/4-215
		1-wire HDQ	Register-compatible with bq2014H	16 /SOIC	bq2050H	PP/4-237
Primary Lithium	800-15,000	1-wire HDQ	Programmable discharge efficiency compensation	16 /SOIC	bq2052+	PP/4-259
NiCd/NiMH Lead Acid/ Li-Ion	800-10,000	2-wire SMBus	SBS rev. 1.0-compliant	16 /SOIC	bq2040	PP/4-185
			SBS rev. 0.95-compliant	16 / SOIC	bq2092	PP/4-314
			SBS rev. 1.0-compliant with 5 LEDs	16 /SOIC	bq2945	PP/4-340
		2-wire SMBus or 1-wire HDQ16	SBS rev. 1.1-compliant	28 / SSOP	bq2060+	PP/4-276
Any	Any	1-wire HDQ	Analog peripheral for µC	8 / SOIC or TSSOP	bq2018	PP/4-170

+ New Product

The bq2011 Gas Gauge ICs provide accurate capacity monitoring of rechargeable batteries in high discharge rate environments. The ICs can monitor a wide range of charge/discharge currents using the onboard V-to-F converter and a low-value sense resistor. The ICs track remaining capacity (NAC) and compensate it for battery self-discharge, charge/discharge rate, and temperature. Five LEDs can communicate remaining capacity in 20% increments. A serial port allows a host microcontroller to access the nonvolatile memory registers containing battery capacity, voltage, temperature, and other critical parameters.

- Accurate measurement of available charge in rechargeable batteries
- Designed for NiCd high discharge rate applications
- Drives 5 LEDs for capacity indication
- Automatic charge self-discharge and discharge compensation
- Low operating current
- 16-pin narrow SOIC

bq2011 Family Selection Guide

Feature	Part Number bq2011	bq2011J	bq2011K
Display	Relative or absolute	Absolute	Absolute
Programmed Full Count (PFC) range	4.5–10.5mVh	2.21–3.81mVh	2.21–3.81mVh
Nominal Available Capacity (NAC) on reset	NAC = 0	NAC = PFC or 0	NAC = PFC or 0
Self-discharge rate	NAC/80	NAC/80 or disabled	NAC/80 or disabled
Charge compensation	75–95% based on rate and temperature	65–95% based on rate and temperature	70–95% based on rate and temperature
Discharge compensation	75–100% plus temperature compensation	75–100% plus temperature compensation	100%
End-of-discharge voltage	0.9V/cell	0.9V/cell	0.96–1.16V/cell
Page number	PP/4-24	PP/4-45	PP/4-63

Portable Power (PP) Selection Guides

Unitrode's battery management module products provide true turn-key solutions for capacity monitoring and charge control of NiCd, NiMH, Li-Ion, or Rechargeable Alkaline battery packs. Designed for battery pack integration, the small boards contain all necessary components to easily implement intelligent or smart battery packs in a portable system. The wide selection of boards offers battery monitoring, capacity tracking, charge control, and remaining capacity communication to the host system or user. The boards are fully tested and provide direct cell connections for simple battery packs.

- Turnkey solutions for intelligent or smart batteries for portable equipment
  - Computers, cellular phones, and camcorders
  - Handheld terminals
  - Communication radios
  - Medical and test equipment
  - Power tools
- Capacity monitoring and charge control
- Pushbutton-activated LED capacity indication
- Designed for battery pack integration
  - Small size
  - Low power
  - Direct cell connections

Battery-Management Modules Selection Guide

Battery Technology	Key Features	Part Number	Page Number
NiCd/NiMH	Capacity monitoring, LED indication, serial communications port	bq2110	PP/5-2
	Capacity monitoring, slow-charge control, LED indication, serial communications port	bq2112	PP/5-14
	Capacity monitoring, charge control output, LED indication, serial communications port	bq2114	PP/5-24
	Capacity monitoring and fast charge control	bq2164	PP/5-71
NiCd	Capacity monitoring for high discharge rates, LED indication	bq2111L	PP/5-8
NiCd/NiMH, Lead Acid	Capacity monitoring, LED indication, single-wire serial communications port	bq2113H+	PP/5-20
Li-Ion	Capacity monitoring, Smart Battery data set and interface, LED indication, pack supervision, 4-segment LED indication	bq2148	PP/5-40
	Capacity monitoring, LED indication, serial communications port	bq2150 bq2150/H	PP/5-47 PP/5-53
	Pack supervision: overvoltage, undervoltage, and overcurrent control	bq2158 bq2158T	PP/5-57 PP/5-64
	Capacity monitoring, 3- or 4-cell pack supervision, and LED indication	bq2167+ bq2168+	PP/5-77 PP/5-85
NiCd/NiMH/ Lead Acid/ Li-Ion	Capacity monitoring, Smart Battery data set and interface, 5-segment LED indication	bq2145	PP/5-34
	Capacity monitoring, Smart Battery data set and interface, 4-segment LED indication	bq219XL	PP/5-93
Any	Charge and discharge counting, serial communication port, single-wire interface	bq2118	PP/5-30

+ New Product

Unitrode Lithium Ion Pack-Protection ICs provide reversible overvoltage, undervoltage, and overcurrent protection for lithium ion battery packs.

- ➤ Protects one to four Lithium Ion series cells from overvoltage, undervoltage, and overcurrent
- ➤ User-selectable thresholds mask-programmable by Unitrode
- ➤ Designed for battery-pack integration
  - — Small outline package, minimal external components and space, and low cost

Pack-Protection and Supervisory ICs Selection Guide

Battery Technology	Number of Cells Protected	Protection Types	Key Features	Pins / Package	Part Number	Page Number
Lithium Ion	3 or 4	Overvoltage, overcurrent, and undervoltage	Very low power	16/0.150" SOIC	bq2058	PP/6-2
	2				bq2058T	PP/6-14
		Overcharge, overdischarge, overcurrent	Internal MOSFET (80mΩ total)		UCC3911	PP/6-26
	1		Internal MOSFET (50mΩ total)	16/0.150" TSSOP	UCC3952+	PP/6-32
	3 or 4	Overvoltage, undervoltage, overcurrent	Smart-discharge circuitry	16/0.150" SSOP	UCC3957	PP/6-37
	1	Overcharge, overdischarge, overcurrent	Internal MOSFETS (50mΩ total)	16/0.150" SOIC	UCC3958	PP/6-44

+ New Product

Power-Management ICs Selection Guide

Features	Part Number: UCC3581	UCC3809 -1/2	UCC3800/ 1/2/3/4/5	UCC3813- 0/1/2/3/4/5
Topology	Forward, flyback	Forward, flyback, buck, boost	Forward, flyback, buck, boost	Forward, flyback, buck, boost
Input voltage	Off-line AC	Off-line AC	Off-line AC, battery	Off-line AC, battery
Output voltage	NA	NA	NA	NA
Operating mode	Fixed/variable frequency	Fixed frequency (1MHz maximum)	Fixed frequency (1MHz maximum)	Fixed frequency (1MHz maximum)
Output	1A FET drives	0.8A FET drives	1A FET drives	1A FET drives
Output power	N / A	N / A	N / A	N / A
Supply current	300µA	500µA	500µA	500µA
Power limit	Yes	No	Yes	Yes
Application/design note	DN-48, DN-65	DN-65, DN-89, U-165, U-168	DN-42A, DN-43, DN-46, DN-48, DN-54, DN-56A, DN-65, DN-89, U-133A, U-97	DN-42A, DN-43, DN-46, DN-48, DN-54, DN-56A, DN-65, DN-89, U-133A, U-97
Pin count ❖	14	8	8	8
Page number	PS/8-128	PS/8-192	PS/8-169	PS/8-206

❖The smallest available pin count for thru-hole and surface-mount packages.

Power-Management ICs Selection Guide (Continued)

Features	Part Number: UCC39401	UCC3941 -3/-5/-ADJ	UCC39411 /2/3+	UCC39421/2+	UCC3946	UCC3954
Topology	Boost / battery charger	Boost	Boost	Boost/SEPIC/ flyback	Watchdog/ reset	Flyback
Input voltage	0.8V to (V_{OUT} + 0.5V)	0.8V to (V_{OUT} + 0.5V)	1.1V to (V_{OUT} + 0.5V)	1.8V–8V	2.1V–5.5V	2.5V–4.2V
Output voltage	ADJ to 5.0V	3.3V, 5V, ADJ	3.3V, 5V, ADJ	ADJ	V_{IN}–0.3V	3.3V
Operating mode	Variable frequency	Variable frequency	Variable	Fixed/variable frequency	Watchdog/ reset	Fixed frequency (200kHz)
Output	Internal power FETs	Internal power FETs	Internal power FETs	FET Drives	NA	Internal power FETs
Output power	200mW	500mW (1 cell) 1W (2 cells)	200mW	NA	NA	2W
Supply current	55µA	80µA	48µA	635µA	10µA	1mA
Power limit	Yes	Yes	Yes	Yes	NA	Yes
Application/ design note	-	DN-73	DN-97	-	-	DN-86
Pin count ❖	20	8	8	16/20	8	8
Page number	PP/7-34	PP/7-48	PP/7-58	PP/7-66	PP/7-88	PP/7-93

+ New Product
❖The smallest available pin count for thru-hole and surface-mount packages.

Linear Controller ICs Selection Guide

Features	Part Number UC3832	UC3833	UC3834	UC3835	UC3836	UCC3837
Type of output	Positive adjustable	Positive adjustable	Positive/ negative adjustable	5V fixed	Positive adjustable	Positive adjustable
Maximum input voltage	36V	36V	40V	40V	40V	12V
Minimum output voltage	2.0V	2.0V	+1.5V / –2.0V		2.5V	1.5V
Output drive	300mA	300mA	350mA	500mA	500mA	1.5mA
Type of short circuit limit	Duty cycle	Duty cycle	Foldback	Foldback	Foldback	Duty cycle
Reference voltage accuracy	2%	2%	3% / 4%	2%	2%	2%
Special features	Multiple pins accessible	-	-	Built-in Rsense	Built-in Rsense	Internal charge pump; Direct N-FET drive
Application/ design note	DN-32, DN-61, U-152	DN-32, DN-61, U-152	U-95			-
Pin count ❖	14, 16	8, 16	16	8, 16	8, 16	8
Page number	PS/3-11	PS/3-11	PS/3-18	PS/3-24	PS/3-24	PS/3-28

❖The smallest available pin count for thru-hole and surface-mount packages.

Low-Dropout Linear Regulator ICs Selection Guide

Features	Part Number UCC381	UC382-1	UC382-2	UC382-3	UC382-ADJ
Output voltage	3.3V, 5V, ADJ	1.5V	2.1V	2.5V	1.2V/ adjustable
Dropout voltage	0.5V at 1A	450mV at 3A	450mV at 3A	450mV at 3A	450mV at 3A
Output voltage accuracy	2.5%	1%	1%	1%	1%
Maximum input voltage	9V	7.5V	7.5V	7.5V	7.5V
Shutdown current	10µA	-	-	-	-
Operating current	400µA	-	-	-	-
Line regulation	0.01% / V	-	-	-	-
Load regulation	0.1%, I_{OUT} = 0 to 1A	-	-	-	-
Special features	Power limit	Fast transient response	Fast transient response	Fast transient response	Fast transient response
Pin count ❖	8	5	5	5	5
Page number	PP/7-5	PS/3-5	PS/3-5	PS/3-5	PS/3-5

❖The smallest available pin count for thru-hole and surface-mount packages.

Low-Dropout Linear Regulator ICs Selection Guide (Continued)

Features	Part Number UCC383	UCC384	UC385-1	UC385-2	UC385-3
Output voltage	3.3V, 5V, ADJ	5V, 12V, ADJ	1.5V	2.1V	2.5V
Dropout voltage	0.45V at 3A	0.2V at 500mA	450mV at 5A	450mV at 5A	450mV at 5A
Output voltage accuracy	2.5%	2.5%	1%	1%	1%
Maximum input voltage	9V	–16V	7.5V	7.5V	7.5V
Shutdown current	40µA	17µA	-		
Operating current	400µA	240µA	-		
Line regulation	0.01% / V	0.01% / V	-		
Load regulation	0.1%, I_{OUT} = 0 to 1A	0.1%, I_{OUT} = 0 to 500mA	-		
Special features	Power limit	Power limit	Fast transient response	Fast transient response	Fast transient response
Pin count ❖	3	8	5	5	5
Page number	PP/7-12	PP/7-19	PS/3-35	PS/3-35	PS/3-35

❖The smallest available pin count for thru-hole and surface-mount packages.

Low-Dropout Linear Regulator ICs Selection Guide (Continued)

Features	Part Number UC385-ADJ	UC386+	UC387+	UC388+
Output voltage	1.2V/adjustable	3.3V	5V	Adjustable down to 1.25V
Dropout voltage	450mV at 5A	0.2V at 200mA	0.2V at 200mA	0.2V at 200mA
Output voltage accuracy	1%	1.5%	1.5%	1.5%
Maximum input voltage	7.5V	9V	9V	9V
Shutdown current	-	2µA	2µA	2µA
Operating current	-	10µA	10µA	10µA
Line regulation	-	25mV max	25mV max	25mV max
Load regulation	-	10mV max	10mV max	10mV max
Special features	Fast transient response	TSSOP	TSSOP	TSSOP
Pin count ❖	5	8	8	8
Page number	PS/3-35	PP/7-29	PP/7-29	PP/7-29

❖The smallest available pin count for thru-hole and surface-mount packages.
+ New product.

Special Function Linear Regulation ICs Selection Guide

Features	Part number UC560	UCC561+	UC563+
Type of output	Positive	Positive	Positive
Application	Source/sink regulator for the 18- and 27-line SCSI termination	LVD SCSI regulator for the 18- and 27-line termination	32-line VME bus bias generator
Input voltage	4V-6V	2.7V- 5.25V	4.875V-5.25V
Output voltage	2.85V	1.3V, 1.75V, 0.75V	2.94V
Dropout voltage	0.9V at 750mA	-	-
Bus standard	SCSI-1,2,3	SPI-2, 3	VME / VME64
Sink/source current	300mA / –750mA	200mA / –200mA	475mA / –575mA
Application/design note	-	-	-
Pin count ❖	5, 8	16	3, 8
Page number	IF/4-3	IF/4-7	IF/4-10

❖The smallest available pin count for thru-hole and surface-mount packages.
+ New product.

Back-Light Controller ICs Selection Guide

Features	Part Number UC3871	UC3872	UCC3972+
Application	Fluorescent lamp driver with LCD Bias	Fluorescent lamp driver	Fluorescent lamp driver
Voltage range	4.5V–20V	4.5V–24V	4.5V–25V
Reference tolerance	1.2%	1.2	NA
Open lamp detect	Yes	Yes	Yes
PWM synchronization	Yes	Yes	Yes
PWM frequency	Programmable	Programmable	80kH–160kH
Analog dimming	Yes	Yes	Yes
Low-frequency dimming	Yes	Yes	Yes
Operating current	8mA	6mA	1mA
Package	18-pin SOIC	16-pin SSOP	8-pin TSSOP
Application/design note	U-141, U-148	DN-75, U-141, U-148	-
Page number	PP/8-2	PP/8-8	PP/8-13

+ New Product

IrDA Selection Guide

Device Type	Supply Voltage	Data Rate	Dynamic Range	Quiescent Current	Encoder/ Decoder	IrDA Compliant	LED Driver	Part Number	Page Number
Receiver	3.3V or 5V	2.4kbps 115.2kbps	150nA 100mA	250µA	N	Y	N/A	UCC5341	PP/9-2
Transceiver	3.3V or 5V	2.4kbps 115.2kbps	150nA 100m A	250µA	N	Y	500mA	UCC5342	PP/9-6
Transceiver	3.3V or 5V	2.4kbps 115.2kbps	150nA 100mA	280µA	Y	Y	500mA	UCC5343	PP/9-10

PWM Control

PWM Control

Current Mode Controllers	UNITRODE PART NUMBER				
	UCC3800	UCC3801	UCC3802	UCC3803	UCC3804
Application	DC-DC and Battery	DC-DC and Battery	Off-line	DC-DC and Battery	Off-line
Topology	Buck, Boost	Buck, Boost	Forward, Flyback	Buck, Boost	Forward, Flyback
Voltage Reference Tolerance	1.5%	1.5%	1.5%	1.5%	1.5%
Peak Output Current	1A	1A	1A	1A	1A
Under Voltage Lockout	7.2V / 6.9V	9.4V / 7.4V	12.5V / 8.3V	4.1V / 3.6V	12.5V / 8.3V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current	100µA	100µA	100µA	100µA	100µA
Leading Edge Blanking	Y	Y	Y	Y	Y
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	100%	50%	100%	100%	50%
Separate Oscillator / Synchronization Terminal					
Application / Design Note	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A	DN-42A, DN-43, DN-46, DN-48, DN-54, DN-56A, DN-65, DN-89, U-97, U-133A	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A
Pin Count ❖	8	8	8	8	8
Page Number	PS/3-173	PS/3-173	PS/3-173	PS/3-173	PS/3-173

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UCC3805	UCC3806	UCC3807-1	UCC3807-2	UCC3807-3
Application	DC-DC and Battery	Isolated Output, Push-pull Controller	DC-DC	Off-line	DC-DC and Battery
Topology	Forward, Flyback	Push-pull, Full Bridge, Half Bridge	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost
Voltage Reference Tolerance	1.5%	1%	1.5%	1.5%	1.5%
Peak Output Current	1A	0.5A	1A	1A	1A
Under Voltage Lockout	4.1V / 3.6V	7.5V / 6.75V	7.2V / 6.9V	12.5V / 8.3V	4.3V / 4.1V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current	100µA	100µA	100µA	100µA	100µA
Leading Edge Blanking	Y		Y	Y	Y
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	50%	50% / 50%	Programmable	Programmable	Programmable
Separate Oscillator / Synchronization Terminal		Y			
Application / Design Note	DN-42A, DN-43, DN-46, DN-48, DN-54, DN-56A, DN-65, DN-89, U-97, U-133A	DN-45, DN-51, DN-65, U-97, U-110, U-144	DN-48, DN-65, U-97, U-133A	DN-48, DN-65, U-97, U-133A	DN-48, DN-65, U-97, U-133A
Pin Count ❖	8	16	8	8	8
Page Number	PS/3-173	PS/3-180	PS/3-187	PS/3-187	PS/3-187

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UCC3808-1	UCC3808-2	UCC3809-1	UCC3809-2	UCC3810
Application	Off-line	DC-DC and Battery	DC-DC	Off-line	Dual PWM Controller, Off-line, DC-DC
Topology	Push-pull, Full Bridge, Half Bridge	Push-pull, Full Bridge, Half Bridge	Forward, Flyback, Buck, Boost	Forward, Flyback, Buck, Boost	Forward, Flyback Buck, Boost
Voltage Reference Tolerance	2%	2%	5%	5%	1.5%
Peak Output Current	0.5A Source, 1A Sink	0.5A Source, 1A Sink	0.4A Source, 0.8A Sink	0.4A Source, 0.8A Sink	1A
Under Voltage Lockout	12.5V / 8.3V	4.3V / 4.1V	10V / 8V	15V / 8V	11.3V / 8.3V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole	Single, Totem Pole	Dual, Totem Pole
Startup Current	130µA	130µA	100µA	100µA	150µA
Leading Edge Blanking					Y
Soft Start	Y	Y	Y	Y	
Maximum Duty Cycle	50% / 50%	50% / 50%	90%	90%	50%
Separate Oscillator / Synchronization Terminal			N/A	N/A	Y
Application / Design Note	DN-65, U-97, U-110, U-170	DN-65, U-97, U-110, U-170	DN-65, DN-89, U-165, U-168	DN-65, DN-89, U-165, U-168	DN-65, U-97, U-110, U-133A
Pin Count ❖	8	8	8	8	16
Page Number	PS/3-192	PS/3-192	PS/3-198	PS/3-198	PS/3-205

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UCC3813-0	UCC3813-1	UCC3813-2	UCC3813-3	UCC3813-4
Application	DC-DC and Battery	DC-DC and Battery	Off-line	DC-DC and Battery	Off-line
Topology	Buck, Boost	Buck, Boost	Forward, Flyback	Buck, Boost	Forward, Flyback
Voltage Reference Tolerance	1.5%	1.5%	1.5%	1.5%	1.5%
Peak Output Current	1A	1A	1A	1A	1A
Under Voltage Lockout	7.2V / 6.9V	9.4V / 7.4V	12.5V / 8.3V	4.1V / 3.6V	12.5V / 8.3V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current	100µA	100µA	100µA	100µA	100µA
Leading Edge Blanking	Y	Y	Y	Y	Y
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	100%	50%	100%	100%	50%
Separate Oscillator / Synchronization Terminal					
Application / Design Note	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A	DN-42A, DN-43, DN-46, DN-48, DN-54, DN-56A, DN-65, DN-89, U-97, U-133A	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A
Pin Count ❖	8	8	8	8	8
Page Number	PS/3-212	PS/3-212	PS/3-212	PS/3-212	PS/3-212

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UCC3813-5	UC3823	UC3823A	UC3823B	UC3824
Application	DC-DC and Battery	DC-DC	DC-DC	Off-line	Synchronous Rectifier, Forward Converter
Topology	Forward, Flyback	Buck, Boost	Buck, Boost	Buck, Boost	Forward, Flyback
Voltage Reference Tolerance	1.5%	1%	1%	1%	1%
Peak Output Current	1A	1.5A	2A	2A	1.5A
Under Voltage Lockout	4.1V / 3.6V	9.2V / 8.4V	9.2V / 8.4V	16V / 10V	9.2V / 8.4V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Dual Complementary, Totem Pole
Startup Current	100µA	1.1mA	0.1mA	0.1mA	1.1mA
Leading Edge Blanking	Y		Y	Y	
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	50%	100%	Programmable, <100%	Programmable, <100%	100%
Separate Oscillator / Synchronization Terminal		Y	Y	Y	Y
Application / Design Note	DN-42A, DN-43, DN-46, DN-48, DN-54, DN-56A, DN-65, DN-89, U-97, U-133A	U-97, U-111, U-131	U-97, U-110, U-111, U-128, U-131	U-97, U-110, U-111, U-128, U-131	U-111
Pin Count ❖	8	16	16	16	16
Page Number	PS/3-212	PS/3-219	PS/3-225	PS/3-225	PS/3-233

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UC3825	UC3825A	UC3825B	UC3826❍	UC3827-1
Application	DC-DC	DC-DC	Off-line	Secondary Side, Average Current Mode	Multiple Output or High Voltage Output DC-DC Converters
Topology	Push-pull, Full Bridge, Half Bridge	Push-pull, Full Bridge, Half Bridge	Push-pull, Full Bridge, Half Bridge	Forward, Flyback, Buck, Boost	Buck Current Fed Push-pull
Voltage Reference Tolerance	1%	1%	1%	1%	4%
Peak Output Current	1.5A	2A	2A	0.25A	Floating 1A for Buck Stage, 0.8A for Push-pull Drivers
Under Voltage Lockout	9.2V / 8.4V	9.2V / 8.4V	16V / 10V	8.4V / 8.0V	9V / 8.4V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	500kHz
Outputs	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole	Floating Buck, Push-pull
Startup Current	1.1mA	0.1mA	0.1mA		1mA
Leading Edge Blanking		Y	Y	N/A	
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	50% / 50%	Programmable	Programmable, <50%	Programmable, <50%	90% for Buck Stage, 50% / 50% for Push-pull Stage
Separate Oscillator / Synchronization Terminal	Y	Y	Y	Y	Y
Application / Design Note	U-97, U-110, U-111	U-97, U-110, U-111, U-128, U-131	U-97, U-110, U-111, U-128, U-131	U-135, U-140	
Pin Count ❖	16	16	16	24	24
Page Number	PS/3-240	PS/3-225	PS/3-225	PS/3-247	PS/3-257

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
❍ Pulse- by-Pulse Current Limiting Not Applicable.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UC3827-2	UCC3830-4	UCC3830-5	UCC3830-6	UCC3839❍
Application	Multiple Output or High Voltage Output DC-DC Converters	Microprocessor Power	Microprocessor Power	Microprocessor Power	Secondary Side, Average Current Mode Control
Topology	Buck Voltage Fed Push-pull	Buck	Buck	Buck	Any Topology
Voltage Reference Tolerance	4%	1%*	1%*	1%*	1%
Peak Output Current	Floating 1A for Buck Stage, 0.8A for Push-pull Drivers	1.5A	1.5A	1.5A	10mA to Drive Opto-coupler
Under Voltage Lockout	9V / 8.4V	10.5V / 10V	10.5V / 10V	10.5V / 10V	
Maximum Practical Operating Frequency	500kHz	100kHz	200kHz	400kHz	1MHz
Outputs	Floating Buck, Push-pull	Single	Single	Single	Opto-coupler Drive
Startup Current	1mA				
Leading Edge Blanking					
Soft Start	Y				
Maximum Duty Cycle	90% for Buck Stage, 50% / 50% for Push-pull Stage	95%	95%	95%	
Separate Oscillator / Synchronization Terminal	Y				
Application / Design Note					U-140
Pin Count ❖	24	20	20	20	14
Page Number	PS/3-257	PS/3-263	PS/3-263	PS/3-263	PS/3-276

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
**** Combined Reference, DAC, and Error Amplifier Tolerance.***
❍ Pulse- by-Pulse Current Limiting Not Applicable.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UC3841	UC3842	UC3842A	UC3843	UC3843A
Application	Primary Side, Programmable, Off-line, DC-DC	Off-line	Off-line	DC-DC	DC-DC
Topology	Forward, Flyback, Buck, Boost	Forward, Flyback, Buck, Boost	Forward, Flyback, Buck, Boost	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost
Voltage Reference Tolerance	1%	1%	1%	1%	1%
Peak Output Current	1A	1A	1A	1A	1A
Under Voltage Lockout		16V / 10V	16V / 10V	8.4V / 7.6V	8.5V / 7.9V
Maximum Practical Operating Frequency	500kHz	500kHz	500kHz	500kHz	500kHz
Outputs	Single, Open Collector	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current	4.5mA	1mA	0.5mA	1mA	0.5mA
Leading Edge Blanking					
Soft Start	Y				
Maximum Duty Cycle	Programmable	100%	100%	100%	100%
Separate Oscillator / Synchronization Terminal					
Special Features			Trimmed Oscillator Discharge Current		Trimmed Oscillator Discharge Current
Application / Design Note	DN-28	DN-27, DN-40, DN-89, U-100A, U-111	DN-26, DN-27, DN-29, DN-30, DN-40, DN-89, U-100A, U-111	DN-27, DN-40, DN-89, U-100A, U-111	DN-26, DN-27, DN-29, DN-30, DN-40, DN-89, U-100A, U-111
Pin Count ❖	18	8, 14	8, 14	8, 14	8, 14
Page Number	PS/3-281	PS/3-289	PS/3-296	PS/3-289	PS/3-296

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UC3844	UC3844A	UC3845	UC3845A	UC3846
Application	Off-line	Off-line	DC-DC	DC-DC	Off-line, DC-DC
Topology	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost	Push-pull, Full Bridge, Half Bridge
Voltage Reference Tolerance	1%	1%	1%	1%	1%
Peak Output Current	1A	1A	1A	1A	0.5A
Under Voltage Lockout	16V / 10V	16V / 10V	8.4V / 7.6V	8.5V / 7.9V	7.7V / 6.95V
Maximum Practical Operating Frequency	500kHz	500kHz	500kHz	500kHz	500kHz
Outputs	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Dual Alternating, Totem Pole
Startup Current	1mA	0.5mA	1mA	0.5mA	
Leading Edge Blanking					
Soft Start					Y
Maximum Duty Cycle	50%	50%	50%	50%	50% / 50%
Separate Oscillator / Synchronization Terminal					Y
Special Features		Trimmed Oscillator Discharge Current		Trimmed Oscillator Discharge Current	
Application / Design Note	DN-27, DN-40, DN-89, U-100A, U-111	DN-26, DN-27, DN-29, DN-30, DN-40, DN-89, U-100A, U-111	DN-27, DN-40, DN-89, U-100A, U-111	DN-26, DN-27, DN-29, DN-30, DN-40, DN-89, U-100A, U-111	DN-45, U-93, U-97, U-100A, U-111
Pin Count ❖	8, 14	8, 14	8, 14	8, 14	16
Page Number	PS/3-289	PS/3-296	PS/3-289	PS/3-296	PS/3-302

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.

❖The smallest available pin count for thru-hole and surface mount packages.

+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UC3847	UC3848 ❍	UC3849 ❍	UC3851	UC3856
Application	Off-line, DC-DC	Average Current Mode, Off-line, DC-DC	Secondary Side, Average Current Mode	Off-line, Programmable, Primary Side Controller	Isolated Output, Push-pull Controller
Topology	Push-pull, Full Bridge, Half Bridge	Forward, Flyback	Forward, Flyback, Buck, Boost	Forward, Flyback, Buck, Boost	Push-pull, Full Bridge, Half Bridge
Voltage Reference Tolerance	1%	1%	1%	1%	1%
Peak Output Current	0.5A	2A	0.25A	0.2A	1.5A
Under Voltage Lockout	7.7V / 6.95V	13V / 10V	8.3V / 7.9V		7.7V / 7.0V
Maximum Practical Operating Frequency	500kHz	1MHz	1MHz	500kHz	1MHz
Outputs	Dual Alternating, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Dual Alternating, Totem Pole
Startup Current		500µA		4.5mA	
Leading Edge Blanking		N/A	N/A	Y	
Soft Start	Y		Y	Y	Y
Maximum Duty Cycle	50% / 50%	Programmable	Programmable	50%	50% / 50%
Separate Oscillator / Synchronization Terminal	Y		Y		Y
Application / Design Note	DN-45, U-93, U-97, U-100A, U-111	U-135, U-140	U-135, U-140	DN-28	DN-45, U-93, U-97, U-110
Pin Count ❖	16	16	24	18	16
Page Number	PS/3-302	PS/3-309	PS/3-317	PS/3-327	PS/3-333

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
❍ Pulse- by-Pulse Current Limiting Not Applicable.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UCC3880-4	UCC3880-5	UCC3880-6	UCC3882	UCC3884
Application	Microprocessor Power	Microprocessor Power	Microprocessor Power	Microprocessor Power	Off-Line or DC-DC Frequency Foldback Controller
Topology	Buck	Buck	Buck	Synchronous Buck	Forward, Flyback, Buck, Boost
Voltage Reference Tolerance	1%*	1%*	1%*	1%*	2%
Peak Output Current	1.5A	1.5A	1.5A	1.5A	0.5A Source, 1A Sink
Under Voltage Lockout	10.5V / 10V	10.5V / 10V	10.5V / 10V	10.5V / 10V	8.9V / 8.3V
Maximum Practical Operating Frequency	100kHz	200kHz	400kHz	700kHz	750kHz
Outputs	Single	Single		Dual, N-FET Drive	Single
Startup Current					200µA
Leading Edge Blanking					
Average Current Mode	Y	Y		Y	
Foldback Current Limiting	Y	Y		Y	
Soft Start					Y
Maximum Duty Cycle	95%	95%		95%	80%
Separate Oscillator / Synchronization Terminal					Y
Special Features	4 Bit Programmable Output Voltage, UV/OV Monitor	4 Bit Programmable Output Voltage, UV/OV Monitor	4 Bit Programmable Output Voltage, UV/OV Monitor	5 Bit Programmable Output Voltage, UV/OV Monitor	
Application / Design Note	U-140	U-140	U-140	U-140	DN-65, U-164
Pin Count ❖	24	18	16	28	16
Page Number	PS/3-373	PS/3-373	PS/3-373	PS/3-380	PS/3-393

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
**** Combined Reference, DAC, and Error Amplifier Tolerance.***
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UC3886				
Application	Microprocessor Power				
Topology	Buck				
Voltage Reference Tolerance	1.5%				
Peak Output Current	1.5A				
Under Voltage Lockout	10.3V / 10.05V				
Maximum Practical Operating Frequency	400kHz				
Outputs	Single				
Startup Current					
Leading Edge Blanking					
Average Current Mode					
Foldback Current Limiting					
Soft Start					
Maximum Duty Cycle	95%				
Separate Oscillator / Synchronization Terminal					
Special Features	External Reference Input, Use with UC3910				
Application / Design Note	U-140, U-156, U-157				
Pin Count ❖	16				
Page Number	PS/3-400				

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Dedicated DC/DC Controllers	UNITRODE PART NUMBER		
	UC2577-12	UC2577-15	UC2577-ADJ
Description	Simple Step-up Voltage Regulator	Simple Step-up Voltage Regulator	Simple Step-up Voltage Regulator
Application	3A Step-up Switching Regulator for Boost, Flyback, and Forward Converter Applications	3A Step-up Switching Regulator for Boost, Flyback, and Forward Converter Applications	3A Step-up Switching Regulator for Boost, Flyback, and Forward Converter Applications
Output Voltage	12V	15V	Adjustable
Special Features	•Circuit Requires Few External Components •NPN Output Switches 3A •Current Mode Operation for Improved Response •Fixed and Adjustable Output Versions Available	•Circuit Requires Few External Components •NPN Output Switches 3A •Current Mode Operation for Improved Response •Fixed and Adjustable Output Versions Available	•Circuit Requires Few External Components •NPN Output Switches 3A •Current Mode Operation for Improved Response •Fixed and Adjustable Output Versions Available
Application / Design Note	DN-47, DN-49	DN-47, DN-49	DN-49
Pin Count ❖	5	5	5
Page Number	PS/3-31	PS/3-31	PS/3-36

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Dedicated DC/DC Controllers	UNITRODE PART NUMBER				
	UC3572	UC3573	UC3578	UCC3585+	
Application	Low Power, High Efficiency, Spot Regulator	Low Power, High Efficiency, Spot Regulator	DC-DC	Low Input Voltage Synchronous Buck Regulator with Output Voltage Tracking	
Topology	Negative Output Flyback	Buck	Buck	Voltage Mode Synchronous Buck	
Voltage Reference Tolerance	2%	2%	2%	1%	
Peak Output Current	0.5A	0.5A	0.6A Source, 0.8A Sink	0.5A	
Maximum Practical Operating Frequency	300kHz	300kHz	100kHz Internal Oscillator	700kHz	
Outputs	Single, Totem Pole	Single, Totem Pole	Single, Floating Totem Pole	P FET/N FET Synchronous	
Startup Current			N/A	2.3mA	
Voltage Feedforward				N	
Soft Start			Y	Y	
Maximum Duty Cycle	100%	100%	90%	100%	
Separate Oscillator / Synchronization Terminal				N	
Application / Design Note		DN-70	U-167		
Pin Count ❖	8	8	16	16	
Page Number	PS/3-108	PS/3-112	PS/3-116	PS/3-154	

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Dedicated DC/DC Controllers	UNITRODE PART NUMBER		
	UCC39401+	UCC3941	UCC39411/2/3+
Description	Low Voltage Boost Controller / Charger	1V Synchronous Boost Converter	1V Low Power Boost Controller
Application	Pager Power	High Efficiency Integrated Boost Converter	High Efficiency Low Power Synchronous Boost Conversion
Special Features	•High Efficiency Boost •1V Input •Battery Charger •Backup LDO	•Full Load Startup at 1V •Power Limit Control •Auxiliary 9V Supply •Output Disconnect •Shutdown Mode	•200mW Output Power with Battery Voltages as low as 0.8V •Power Limit Control •Adaptive Current Mode Control •Auxiliary 7V Supply •Shutdown Mode
Application / Design Note			
Pin Count ❖	20	8	8
Page Number	PP/7-34	PP/7-45	PP/7-58

Dedicated DC/DC Controllers	UNITRODE PART NUMBER		
	UCC39421/2+	UCC3954	
Description	Multimode HF PWM Controller	Single Cell Lithium-Ion to 3.3V Converter	
Application	High Efficiency Boost, Sepic Flyback Converter	High Efficiency Flyback Converter	
Special Features	•2mHz Operation •1.8V Input •Current Limit •Power-on Reset •Low Voltage Detect	•Fixed 3.3V Output •750mA Output Current •Low Battery Warning •Low Battery Disconnect •Shutdown Mode	
Application / Design Note			
Pin Count ❖	16, 20	8	
Page Number	PP/7-66	PP/7-93	

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

MicroProcessor Power Controllers	UNITRODE PART NUMBER				
	UCC3588+	UCC3830-4	UCC3830-5	UCC3830-6	UCC3880-4
Application	Synchronous Buck Regulator with 5 Bit DAC	Microprocessor Power	Microprocessor Power	Microprocessor Power	Microprocessor Power
Topology	Voltage Mode Synchronous Buck	Buck	Buck	Buck	Buck
Voltage Reference Tolerance	1%	1%*	1%*	1%*	1%*
Peak Output Current	1A	1.5A	1.5A	1.5A	1.5A
Maximum Practical Operating Frequency	700kHz	100kHz	200kHz	400kHz	100kHz
Outputs	Dual NFET Synchronous	Single	Single	Single	Single
Soft Start	Y				
Average Current Mode		Y	Y	Y	Y
Foldback Current Limiting		Y	Y	Y	Y
Maximum Duty Cycle	100%	95%	95%	95%	95%
Special Features		5 Bit Programmable Output Voltage, UV/OV Monitor	5 Bit Programmable Output Voltage, UV/OV Monitor	5 Bit Programmable Output Voltage, UV/OV Monitor	4 Bit Programmable Output Voltage, UV/OV Monitor
Application / Design Note					U-140
Pin Count ❖	16	20	20	20	20
Page Number	PS/3-163	PS/3-263	PS/3-263	PS/3-263	PS/3-373

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
**** Combined Reference, DAC, and Error Amplifier Tolerance.***
+ New Product

PWM Control (cont.)

MicroProcessor Power Controllers	UNITRODE PART NUMBER				
	UCC3880-5	UCC3880-6	UCC3882		
Application	Microprocessor Power	Microprocessor Power	Microprocessor Power		
Topology	Buck	Buck	Synchronous Buck		
Voltage Reference Tolerance	1%*	1%*	1%*		
Peak Output Current	1.5A	1.5A	1.5A		
Maximum Practical Operating Frequency	200kHz	400kHz	700kHz		
Outputs	Single	Single	Dual, N-FET Drive		
Soft Start					
Average Current Mode	Y	Y	Y		
Foldback Current Limiting	Y	Y	Y		
Maximum Duty Cycle	95%	95%	95%		
Special Features	4 Bit Programmable Output Voltage, UV/OV Monitor	4 Bit Programmable Output Voltage, UV/OV Monitor	5 Bit Programmable Output Voltage, UV/OV Monitor		
Application / Design Note	U-140	U-140	U-140		
Pin Count ❖	20	20	28		
Page Number	PS/3-373	PS/3-373	PS/3-380		

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
**** Combined Reference, DAC, and Error Amplifier Tolerance.***
+ New Product

PWM Control (cont.)

MicroProcessor Power Support	UNITRODE PART NUMBER		
	UCC391+	UC3910	UCC3946
Description	5-Bit DAC 5V Operation	Reference, 4-bit DAC and Fault Monitor	Microprocessor Supervisor with Watchdog Timer
Application	Sets Control Voltage for UC3886 and other Precision PWMs	Sets Control Voltage for UC3886, UC3870 and other Precision PWMS	Accurate Microprocessor Supervision
Special Features	•5V Operation •1% Combined Reference and DAC Tolerance •Meets VID Code for Pentium II Processors	•4-bit DAC Sets Output Voltage of PWM, Meets Intel VID Code •1% Combined Reference and DAC Tolerance •Over and Under Voltage Monitoring and Protection	•Programmable Reset Period •Programmable Watchdog Period •1.5% Accurate Threshold •4mA IDD
Application / Design Note		U-157, U-158	
Pin Count ❖	8	16	8
Page Number	PS/3-434	PS/3-437	PP/7-88

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Post Regulation Controllers	UNITRODE PART NUMBER				
	UCC3583	UC3584	UC3838A		
Application	Secondary Side Post Regulation	DC-DC Secondary Side Synchronous Post Regulator	Mag-Amp Controller		
Topology	Buck	Buck			
Voltage Reference Tolerance	1.5%	1%	1%		
Peak Output Current	1.5A Source, 0.5A Sink	1.5A Source and Sink	120mA Reset Current		
Maximum Practical Operating Frequency	500kHz	1MHz			
Undervoltage Lockout	9.0V / 8.4V	10.5V / 8.8V	N/A		
Outputs	Single, Totem Pole	Single, Totem Pole			
Startup Current	100µA	N/A			
Voltage Feedforward	N/A				
Soft Start	Y	Y			
Maximum Duty Cycle	95%	94%			
Separate Oscillator / Synchronization Terminal	Y	Y			
Special Features	• For Both Single Ended and Center Tapped Secondary Circuits • Operation From Floating Supply Referenced to Output	• Can Use Existing Windings • Internally Regulated 15V Boost Supply Bias for Low Voltage Applications • Short Circuit Protection with Programmable Delay	• Dual Op-Amps • –120V Reset Driver		
Application / Design Note	DN-64	DN-64, DN-83	DN-47		
Pin Count ❖	14	16	16, 20		
Page Number	PS/3-139	PS/3-148	PS/3-272		

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Secondary Side PWM Control	UNITRODE PART NUMBER				
	UC3826	UCC3839❍	UC3849❍	UCC3960+	UCC3961+
Application	Secondary Side, Average Current Mode	Secondary Side, Average Current Mode Control	Secondary Side, Average Current Mode	Primary-Side Startup Control	Primary-Side Startup Control
Topology	Forward, Flyback, Buck, Boost	Any Topology	Forward, Flyback, Buck, Boost		
Voltage Reference Tolerance	1%	1%	1%	5%	5%
Peak Output Current	0.25A	10mA to Drive Opto-coupler	0.25A	1.5A	1.5A
Undervoltage Lockout	8.4V / 8V		8.3V / 7.9V	10V / 8V	10V / 8V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	400kHz Synchronizable Switching Frequency	400kHz Synchronizable Switching Frequency
Outputs	Single, Totem Pole	Opto-coupler Drive	Single, Totem Pole	Single	Single
Startup Current				150µA	150µA
Leading Edge Blanking	N/A		N/A	N/A	N/A
Soft Start	Y		Y	Y	Y
Maximum Duty Cycle	Programmable		Programmable		Programable V-S Clamp
Separate Oscillator / Synchronization Terminal	Y		Y		
Special Features					•Multimode OVC Protection, •Programable OV and UV, •Self Bias Regulation.
Application / Design Note	U-135, U-140	U-140	U-135, U-140	DN-99	DN-99
Pin Count ❖	24	14	24	8	14
Page Number	PS/3-247	PS/3-276	PS/3-317	PS/3-442	PS/3-450

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
❍ Pulse- by-Pulse Current Limiting Not Applicable.
+ New Product

PWM Control (cont.)

Soft Switching Controllers	UNITRODE PART NUMBER				
	UCC3580-1★	UCC3580-2★	UCC3580-3★	UCC3580-4★	UC3860
Application	Active Clamp / Reset PWM	Active Clamp / Reset PWM	Active Clamp / Reset PWM	Active Clamp / Reset PWM	Off-line, DC-DC, Zero Current Switching
Topology	Forward, Flyback	Forward, Flyback	Forward, Flyback	Forward, Flyback	Half Bridge, Full Bridge
Voltage Reference Tolerance	1.5%	1.5%	1.5%	1.5%	1%
Peak Output Current	1A / 0.5A	1A / 0.5A	1A / 0.5A	1A / 0.5A	2A
Undervoltage Lockout	9V / 8.5V	15V / 8.5V	9V / 8.5V	15V / 8.5V	17.3V / 10.5V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	2MHz
Outputs	Dual Complementary, Totem Pole	Dual Complementary, Totem Pole	Dual Complementary, Totem Pole, Inverted Out2	Dual Complementary, Totem Pole, Inverted Out2	Dual Programmable, Totem Pole
Startup Current	50µA	50µA	50µA	50µA	300µA
Voltage Feedforward	Y	Y	Y	Y	
Soft Start	Y	Y	Y	Y	
Maximum Duty Cycle	Programmable	Programmable	Programmable	Programmable	Programmable
Separate Oscillator / Synchronization Terminal	Y	Y	Y	Y	Y
Application / Design Note	DN-65	DN-65	DN-65	DN-65	
Pin Count ❖	16	16	16	16	24, 28
Page Number	PS/3-122	PS/3-122	PS/3-122	PS/3-122	PS/3-341

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
★ Does Not Feature Current Limiting.
+ New Product

PWM Control (cont.)

Soft Switching Controllers	UNITRODE PART NUMBER				
	UC3861	UC3862	UC3863	UC3864	UC3865
Application	Off-line, Zero Voltage Switching	DC-DC and Battery, Zero Voltage Switching	DC-DC and Battery, Zero Voltage Switching	DC-DC and Battery, Zero Voltage Switching	Off-line, Zero Current Switching
Topology	Half Bridge, Full Bridge	Forward, Flyback	Half Bridge, Full Bridge	Forward, Flyback	Half Bridge, Full Bridge
Voltage Reference Tolerance	1%	1%	1%	1%	1%
Peak Output Current	1A	1A	1A	1A	1A
Undervoltage Lockout	16.5V / 10.5V	16.5V / 10.5V	8V / 7V	8V / 7V	16.5V / 10.5V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Dual Alternating, Totem Pole	Single, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole	Dual Alternating, Totem Pole
Startup Current	150µA	150µA	150µA	150µA	150µA
Voltage Feedforward					
Soft Start					
Maximum Duty Cycle	50% / 50%	100%	50% / 50%	100%	50% / 50%
Separate Oscillator / Synchronization Terminal					
Application / Design Note	U-122, U-138	U-122, U-138	U-122, U-138	U-122, U-138	U-122, U-138
Pin Count ❖	16	16	16	16	16
Page Number	PS/3-349	PS/3-349	PS/3-349	PS/3-349	PS/3-349

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Soft Switching Controllers	UNITRODE PART NUMBER				
	UC3866	UC3867	UC3868	UC3875	UC3876
Application	Off-line, Zero Current Switching	DC-DC and Battery, Zero Current Switching	DC-DC and Battery, Zero Current Switching	Zero Voltage Transition, Phase Shifted Bridge	Zero Voltage Transition, Phase Shifted Bridge
Topology	Forward, Flyback	Half Bridge, Full Bridge	Forward, Flyback	Full Bridge	Full Bridge
Voltage Reference Tolerance	1%	1%	1%	1%	1%
Peak Output Current	1A	1A	1A	2A	2A
Undervoltage Lockout	16.5V / 10.5V	8V / 7V	8V / 7V	10.75V / 9.5V	15.25V / 9.25V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole	Quad Phase Shifted, Totem Pole	Quad Phase Shifted, Totem Pole
Startup Current	150µA	150µA	150µA	150µA	150µA
Soft Start				Y	Y
Maximum Duty Cycle	100%	50% / 50%	100%	100%	100%
Separate Oscillator / Synchronization Terminal				Y	Y
Application / Design Note	U-122, U-138	U-122, U-138	U-122, U-138	DN-63, U-111, U-136A	DN-63, U-111, U-136A
Pin Count ❖	16	16	16	20, 28	20, 28
Page Number	PS/3-349	PS/3-349	PS/3-349	PS/3-357	PS/3-357

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Soft Switching Controllers	UNITRODE PART NUMBER				
	UC3877	UC3878	UC3879	UCC3895+	
Application	Zero Voltage Transition, Phase Shifted Bridge	Zero Voltage Transition, Phase Shifted Bridge	Zero Voltage Transition, Phase Shifted Bridge	Zero Voltage Transition, Phase, Shifted Bridge	
Topology	Full Bridge	Full Bridge	Full Bridge	Full Bridge	
Voltage Reference Tolerance	1%	1%	1%	1%	
Peak Output Current	2A	2A	0.1A	0.1A	
Undervoltage Lockout	10.75V / 9.5V	15.25V / 9.25V	Selectable 10.75V / 9.5V, 15.25V / 9.25V	11V / 9V	
Maximum Practical Operating Frequency	1MHz	1MHz	300kHz	1MHz	
Outputs	Quad, Phase Shifted, Totem Pole	Quad Phase Shifted, Totem Pole	Quad Phase Shifted, Totem Pole	Quad, Phase Shifted, Totem Pole	
Startup Current	150µA	150µA	150µA	150µA	
Leading Edge Blanking					
Soft Start	Y	Y	Y	Y	
Maximum Duty Cycle	100%	100%	100%	100%	
Separate Oscillator / Synchronization Terminal	Y	Y	Y	Y	
Application / Design Note	DN-63, U-111, U-136A	DN-63, U-111, U-136A	DN-63, U-111, U-136A, U-154	DN-63, U-136A	
Pin Count ❖	20, 28	20, 28	20	20	
Page Number	PS/3-357	PS/3-357	PS/3-367	PS/3-425	

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Voltage Mode Controllers	UNITRODE PART NUMBER				
	UC3524✣	UC3524A	UC3525A	UC3525B	UC3526
Application	Fixed Frequency PWM, Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC
Topology	Forward, Flyback, Buck, Boost	Forward, Flyback, Buck, Boost	Full Bridge, Half Bridge	Full Bridge, Half Bridge	Full Bridge, Half Bridge
Voltage Reference Tolerance	4%	1%	1%	0.75%	1%
Peak Output Current	100mA	200mA	400mA	200mA	100mA
Undervoltage Lockout		7.5V / 7V	7V	7V	Y
Maximum Practical Operating Frequency	300kHz	500kHz	500kHz	500kHz	400kHz
Outputs	Dual Alternating, Uncommitted	Dual Alternating, Uncommitted	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole
Startup Current		4mA			
Voltage Feedforward					
Soft Start			Y	Y	Y
Maximum Duty Cycle	50% / 50%	50% / 50%	50% / 50%	50% / 50%	50% / 50%
Separate Oscillator / Synchronization Terminal	Y	Y	Y	Y	Y
Application / Design Note			DN-36	DN-36	
Pin Count ❖	16	16	16	16	16
Page Number	PS/3-43	PS/3-48	PS/3-54	PS/3-61	PS/3-68

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
✣ Does Not Feature UVLO.
+ New Product

PWM Control (cont.)

Voltage Mode Controllers	UNITRODE PART NUMBER				
	UC3526A	UC3527A	UC3527B	UC3548	UCC3570
Application	Fixed Frequency PWM Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC	Off-line, DC-DC	Wide Range, Off-line
Topology	Full Bridge, Half Bridge	Full Bridge, Half Bridge	Full Bridge, Half Bridge	Flyback, Forward	Forward, Flyback, Buck, Boost
Voltage Reference Tolerance	1%	1%	0.75%	1%	1%
Peak Output Current	100mA	400mA	200mA	2A	500mA
Undervoltage Lockout	Y	7V	7V	13V / 10V	13V / 9V
Maximum Practical Operating Frequency	550kHz	500kHz	500kHz	1MHz	500kHz
Outputs	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current				500µA	85µA
Voltage Feedforward				Y	Y
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	50% / 50%	50% / 50%	50% / 50%	Programmable	100%
Separate Oscillator / Synchronization Terminal	Y	Y	Y		
Application / Design Note		DN-36	DN-36		DN-48, DN-62, DN-65, U-150
Pin Count ❖	18	16	16	16	14
Page Number	PS/3-75	PS/3-54	PS/3-61	PS/3-83	PS/3-91

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Voltage Mode Controllers	UNITRODE PART NUMBER				
	UCC35701+	UCC3580-1★	UCC3580-2★	UCC3580-3★	UCC3580-4★
Application	Wide Range DC-DC and Off-line	Active Clamp / Reset PWM	Active Clamp / Reset PWM	Active Clamp / Reset PWM	Active Clamp / Reset PWM
Topology	Forward, Flyback, Buck and Boost	Forward, Flyback	Forward, Flyback	Forward, Flyback	Forward, Flyback
Voltage Reference Tolerance	1%	1.5%	1.5%	1.5%	1.5%
Peak Output Current	1.2A	1A / 0.5A	1A / 0.5A	1A / 0.5A	1A / 0.5A
Undervoltage Lockout	13V / 9V	9V / 8.5V	15V / 8.5V	9V / 8.5V	15V / 8.5V
Maximum Practical Operating Frequency	700kHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Dual Complementary, Totem Pole	Dual Complementary, Totem Pole	Dual Complementary, Totem Pole, Inverted Out2	Dual Complementary, Totem Pole, Inverted Out2
Startup Current	130µA	50µA	50µA	50µA	50µA
Voltage Feedforward	Y	Y	Y	Y	Y
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	100%	Programmable	Programmable	Programmable	Programmable
Separate Oscillator / Synchronization Terminal	Y	Y	Y	Y	Y
Application / Design Note	DN-48, DN-62, DN-65, U-150	DN-65	DN-65	DN-65	DN-65
Pin Count ❖	14	16	16	16	16
Page Number	PS/3-99	PS/3-122	PS/3-122	PS/3-122	PS/3-122

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
★ Does Not Feature Current Limiting.
+ New Product

PWM Control (cont.)

Voltage Mode Controllers	UNITRODE PART NUMBER				
	UCC3581	UCC3588+	UCC3888	UCC3889	UCC3890
Application	Off-line, Primary Side PWM for ISDN Applications	Synchronous Buck Regulator with 5 Bit DAC	Off-line Power Supply Controller	Off-line Power Supply Controller	Off-line Battery Charge Controller
Topology	Forward, Flyback	Voltage Mode Synchronous Buck	Flyback	Flyback	Flyback
Voltage Reference Tolerance	1.5%	1%	3%	3%	4%
Peak Output Current	1A	1A	0.15A	0.15A	0.15A
Undervoltage Lockout	7.3V / 6.8V	10.5V / 10V	8.4V / 6.3V	8.4V / 6.3V	8.6V / 6.3V
Maximum Practical Operating Frequency	100kHz	700kHz	250kHz	250kHz	250kHz
Outputs	Single, Totem Pole	Dual NFET Synchronous	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current	100µA		150µA	150µA	
Voltage Feedforward			Y	Y	Y
Soft Start	Y	Y			
Maximum Duty Cycle	Programmable	100%	55%	55%	N/A
Separate Oscillator / Synchronization Terminal	Y				
Application / Design Note	DN-48, DN65		DN-59A, U-149A	DN-59A, DN-65, U-149A	
Pin Count ❖	14	16	8	8	8
Page Number	PS/3-131	PS/3-163	PS/3-407	PS/3-412	PS/3-418

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Voltage Mode Controllers	UNITRODE PART NUMBER				
	UC494A/AC	UC495A/AC			
Application	DC-DC	DC-DC			
Topology	Buck, Boost, Push-Pull, Half Bridge	Buck, Boost, Push-Pull, Half Bridge			
Voltage Reference Tolerance	1%	1%			
Peak Output Current	200mA	200mA			
Undervoltage Lockout	5V / 4.7V	5V / 4.7V			
Maximum Practical Operating Frequency					
Outputs	Dual Floating	Dual Floating			
Startup Current	6mA	6mA			
Voltage Feedforward					
Soft Start					
Maximum Duty Cycle					
Separate Oscillator / Synchronization Terminal					
Special Features		On Chip 39V Zener			
Application / Design Note	DN-38	DN-38			
Pin Count ❖	16	18			
Page Number	PS/3-460	PS/3-460			

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Factor Correction

Power Factor Correction

Power Factor Correction Products	UNITRODE PART NUMBER				
	UCC3817+	UCC3818+	UCC38500+	UCC38501+	UCC38502+
Soft Switching					
Maximum Practical Operating Frequency	250kHz	250kHz	250kHz	250kHz	250kHz
Current Error Amplifier Bandwidth	3MHz	3MHz	3MHz	3MHz	3MHz
Average Current Mode	Y	Y	Y	Y	Y
Worldwide AC Input Voltage Operation	Y	Y	Y	Y	Y
Output Drive	1A	1A	1A	1A	1A
Startup Current	0.1A	0.1A	0.1A	0.1A	0.1A
Undervoltage Lockout	16V / 10V	10.5V / 10V	16V / 10V	10.5V / 10V	16V / 10V
UVLO 2 Hysteresis			1.2V (300V Turn-off)	1.2V (300V Turn-off)	3V (200V Turn-off)
Overvoltage Protection	Y	Y	Y	Y	Y
Enable Input	Y (with OVP)	Y	Y	Y	Y
Multiplier / Divider Feedforward	Y (Simplified)	Y (Simplified)	Y (Simplified)	Y (Simplified)	Y (Simplified)
Special Features			DC / DC Controller Included	DC / DC Controller Included	DC / DC Controller Included
Application / Design Note	DN-39E	DN-39E	DN-39E		
Pin Count ❖	16	16	20	20	20
Page Number	PS/4-5	PS/4-5	PS/4-15	PS/4-15	PS/4-15

❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Factor Correction (cont.)

Power Factor Correction Products	UNITRODE PART NUMBER				
	UC3854B	UC3855A	UC3855B	UCC3857	UCC3858
Soft Switching		ZVT	ZVT	ZCT	
Maximum Practical Operating Frequency	200kHz	500kHz	500kHz	500kHz	500kHz
Current Error Amplifier Bandwidth	5MHz	5MHz	5MHz	5MHz	5MHz
Average Current Mode	Y	Y	Y	Y	Y
Worldwide AC Input Voltage Operation	Y	Y	Y	Y	Y
Output Drive	1A	1.5A	1.5A	1A	0.5A
Startup Current	0.3mA	0.15mA	0.15mA	0.06mA	0.1mA
Undervoltage Lockout	10.5V / 10V	16V / 10V	10.5V / 10V	13.8V / 10V	13.8V / 10V
Overvoltage Protection		Y	Y		Y
Enable Input	Y	Y	Y		Y
Multiplier / Divider Feedforward	Y	Y	Y	Y (Faster Response)	Y (Faster Response)
Special Features		Current Synthesizer	Current Synthesizer	Single Stage Isolated Output	Improved Efficiency at Light Load
Application / Design Note	DN-39E, DN-44, DN-66	DN-39E, DN-66, U-153	DN-39E, DN-66, U-153	DN-39E	DN-39E, DN-90
Pin Count ❖	16	20	20	20	16
Page Number	PS/4-42	PS/4-48	PS/4-48	PS/4-56	PS/4-65

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Factor Correction (cont.)

Power Factor Correction Products	UNITRODE PART NUMBER				
	UCC38503+	UC3852	UC3853	UC3854	UC3854A
Soft Switching		ZCT			
Maximum Practical Operating Frequency	250kHz	Variable	125kHz	200kHz	200kHz
Current Error Amplifier Bandwidth	3MHz	N/A	1MHz	800kHz	5MHz
Average Current Mode	Y		Y	Y	Y
Worldwide AC Input Voltage Operation	Y		Y	Y	Y
Output Drive	1A	0.5A	1A	1A	1A
Startup Current	0.1A	1mA	0.25mA	1.5mA	0.3mA
Undervoltage Lockout	10.5V / 10V	16.3V / 11.5V	11.5V / 9.5V	16V / 10V	16V / 10V
UVLO 2 Hysteresis	3V (200V Turn-off)				
Overvoltage Protection	Y		Y		
Enable Input	Y			Y	Y
Multiplier / Divider Feedforward	Y (Simplified)	N/A	Y	Y	Y
Special Features	DC / DC Controller Included				
Application / Design Note		DN-39E, U-132	DN-39E, DN-77, DN-78, U-159	DN-39E, DN-41, U-134	DN-39E, DN-44, DN-66
Pin Count ❖	20	8	8	16	16
Page Number	PS/4-15	PS/4-22	PS/4-27	PS/4-32	PS/4-42

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Linear Regulation

Linear Regulation

Linear Controllers	UNITRODE PART NUMBER				
	UC3832	UC3833	UC3834	UC3835	UC3836
Type of Output	Positive Adjustable	Positive Adjustable	Positive / Negative Adjustable	5V Fixed	Positive Adjustable
Maximum Input Voltage	36V	36V	40V	40V	40V
Minimum Output Voltage	2.0V	2.0V	+1.5V / –2.0V		2.5V
Output Drive	300mA	300mA	350mA	500mA	500mA
Type of Short Circuit Limit	Duty Cycle	Duty Cycle	Foldback	Foldback	Foldback
Reference Voltage Accuracy	2%	2%	3% / 4%	2%	2%
Special Features	Multiple Pins Accessible	8 Pin Package		Built in Rsense	Built in Rsense
Application / Design Note	DN-32, DN-61, U-152	DN-32, DN-61, U-152	U-95		
Pin Count ❖	14, 16	8, 16	16	8, 16	8, 16
Page Number	PS/5-11	PS/5-11	PS/5-18	PS/5-24	PS/5-24

Linear Controllers	UNITRODE PART NUMBER				
	UCC3837				
Type of Output	Positive Adjustable				
Maximum Input Voltage	12V				
Minimum Output Voltage	1.5V				
Output Drive	1.5mA				
Type of Short Circuit Limit	Duty Cycle				
Reference Voltage Accuracy	2%				
Special Features	• Internal Charge Pump • Direct N-FET Drive				
Application / Design Note					
Pin Count ❖	8				
Page Number	PS/5-28				

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Linear Regulation (cont.)

Low Dropout Linear Regulators	UNITRODE PART NUMBER				
	UC381	UC382-1	UC382-2	UC382-3	UC382-ADJ
Output Voltage	3.3V, 5V, ADJ	1.5V	2.1V	2.5V	1.2V / Adjustable
Dropout Voltage	0.5V at 1A	450mV at 3A	450mV at 3A	450mV at 3A	450mV at 3A
Output Voltage Accuracy	2.5%	1%	1%	1%	1%
Maximum Input Voltage	9V	7.5V	7.5V	7.5V	7.5V
Shutdown Current	10µA				
Operating Current	400µA				
Line Regulation	0.01% / V				
Load Regulation	0.1%, I_{OUT} = 0 to 1A				
Special Features	Power Limit	Fast Transient Response	Fast Transient Response	Fast Transient Response	Fast Transient Response
Pin Count ❖	8	5	5	5	5
Page Number	PP/7-5	PS/5-5	PS/5-5	PS/5-5	PS/5-5

Low Dropout Linear Regulators	UNITRODE PART NUMBER				
	UC383	UC384	UC385-1	UC385-2	UC385-3
Output Voltage	3.3V, 5V, ADJ	5V, 12V, ADJ	1.5V	2.1V	2.5V
Dropout Voltage	0.45V at 3A	0.2V at 500mA	450mV at 5A	450mV at 5A	450mV at 5A
Output Voltage Accuracy	2.5%	2.5%	1%	1%	1%
Maximum Input Voltage	9V	–16V	7.5V	7.5V	7.5V
Shutdown Current	40µA	17µA			
Operating Current	400µA	240µA			
Line Regulation	0.01% / V	0.01% / V			
Load Regulation	0.1%, I_{OUT} = 0 to 1A	0.1%, I_{OUT} = 0 to 500mA			
Special Features	Power Limit	Power Limit	Fast Transient Response	Fast Transient Response	Fast Transient Response
Pin Count ❖	3	8	5	5	5
Page Number	PP/7-12	PP/7-19	PS/5-35	PS/5-35	PS/5-35

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Linear Regulation (cont.)

Low Dropout Linear Regulators	UNITRODE PART NUMBER				
	UC385-ADJ	UC386+	UC387+	UC388+	
Output Voltage	1.2V / Adjustable	3.3V	5V	Adjustable down to 1.25V	
Dropout Voltage	450mV at 5A	0.2V at 200mA	0.2V at 200mA	0.2V at 200mA	
Output Voltage Accuracy	1%	1.5%	1.5%	1.5%	
Maximum Input Voltage	7.5V	9V	9V	9V	
Shutdown Current		2µA	2µA	2µA	
Operating Current		10µA	10µA	10µA	
Line Regulation		25mV max	25mV max	25mV max	
Load Regulation		10mV max	10mV max	10mV max	
Special Features	Fast Transient Response	TSSOP	TSSOP	TSSOP	
Pin Count ❖	5	8	8	8	
Page Number	PS/5-35	PP/7-29	PP/7-29	PP/7-29	

Special Functions Linear Regulators	UNITRODE PART NUMBER				
	UC560	UCC561+	UC563+		
Type of Output	Positive	Positive	Positive		
Application	Source / Sink Regulator for the 18 and 27 Line SCSI Termination	LVD SCSI Regulator for the 18 and 27 Line Termination	32 Line VME Bus Bias Generator		
Input Voltage	4V-6V	2.7V- 5.25V	4.875V-5.25V		
Output Voltage	2.85V	1.3V, 1.75V, 0.75V	2.94V		
Dropout Voltage	0.9V at 750mA				
Bus Standard	SCSI-1,2,3	SPI-2, 3	VME / VME64		
Sink / Source Current	300mA / –750mA	200mA / –200mA	475mA / –575mA		
Application / Design Note					
Pin Count ❖	5, 8	16	3, 8		
Page Number	IF/4-3	IF/4-7	IF/4-10		

❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Drivers

Power and FET Drivers	UNITRODE PART NUMBER				
	L293/D	UC2950	UC3702	UC3705	UC3706
Power Driver	Quad	Single		Single	Dual
FET Driver					
Isolated Driver Pairs					
Relay Drivers			Quad		
Output Configuration	Non-Inverting	Sink / Source TTL	Non-Inverting	Complementary	Complementary
Enable					
Inhibit	Y		Y		Y
Analog Stop					Y
Output Rise Time	250ns			60ns	60ns
Maximum Voltage	36V	35V	42.5V	40V	40V
Peak Output Current	2.0A / 1.2A	4.0A	50mA per Relay	1.5A	1.5A
Application / Design Note				U-111, U-118, U-137	U-111, U-118, U-137
Pin Count ❖	16, 28	5	16	5, 8	16
Page Number	PS/6-5	PS/6-10	PS/6-12	PS/6-16	PS/6-19

Power and FET Drivers	UNITRODE PART NUMBER				
	UC3707	UC3708	UC3709	UC3710	UC3711
Power Driver	Dual	Dual			
FET Driver			Single	Single	Dual
Isolated Driver Pairs					
Relay Drivers					
Output Configuration	Complementary	Non-Inverting	Non-Inverting	Complementary	Non-Inverting
Enable		Y			
Inhibit	Y				
Analog Stop	Y				
Output Rise Time	50ns	75ns	40ns	40ns	20ns
Maximum Voltage	40V	35V	40V	20V	40V
Peak Output Current	1.5A	3.0A	1.5A	6.0A	1.5A
Application / Design Note	U-111, U-118, U-137	DN-35, U-111, U-137	U-111, DN-118, U-137	U-111	U-111
Pin Count ❖	16	8, 16	8, 16	5, 8, 16	8
Page Number	PS/6-24	PS/6-31	PS/6-35	PS/6-38	PS/6-41

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Drivers (cont.)

Power and FET Drivers	UNITRODE PART NUMBER				
	UC3714	UC3715	UC3724	UC3725	UC3726
Power Driver					Transmitter
FET Driver	Dual	Dual	Transmitter	Single	
Isolated Driver Pairs			FET Drv	FET Drv	IGBT Drv
Relay Drivers					
Output Configuration	Non-Inverting	One Inverting, One Non-Inverting	Non-Inverting	Non-Inverting	Non-Inverting
Enable	Y	Y			
Inhibit					
Analog Stop					
Output Rise Time	100ns / 50ns	100ns / 50ns	30ns	30ns	75ns
Maximum Voltage	20V	20V	40V	40V	40V
Peak Output Current	1.0A / 2.0A	1.0A / 2.0A	2.0A	2.0A	4.0A
Application / Design Note	U-111	U-111	DN-35, U-127	DN-35, U-127	DN-57, DN-60, U-143C
Pin Count ❖	8, 16	8, 16	8, 16	8, 16	16, 28
Page Number	PS/6-43	PS/6-43	PS/6-50	PS/6-53	PS/6-57

Power and FET Drivers	UNITRODE PART NUMBER				
	UC3727	UCC37423+	UCC37424+	UCC37425+	UCC37523+
Power Driver	Single				
FET Driver		Dual	Dual	Dual	Dual
Isolated Driver Pairs	IGBT Drv				
Relay Drivers					
Output Configuration	Non-Inverting	Inverting	Non-Inverting	One Inverting, One Non-Inverting	Inverting
Enable					Y
Inhibit					
Analog Stop					
Output Rise Time	75ns	20ns	20ns	20ns	20ns
Maximum Voltage	40V	20V	20V	20V	20V
Peak Output Current	4.0A	3.0A	3.0A	3.0A	3.0A
Special Features		UVLO	UVLO	UVLO	UVLO, Adaptive LEB
Application / Design Note	DN-57, DN-60, U-143C				
Pin Count ❖	20, 28	8, 16	8, 16	8, 16	8, 16
Page Number	PS/6-62	PS/6-68	PS/6-68	PS/6-68	PS/6-73

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Drivers (cont.)

Power and FET Drivers	UNITRODE PART NUMBER				
	UCC37524+	UCC37525+	UCC3776		
Power Driver					
FET Driver	Dual	Dual	Quad		
Isolated Driver Pairs					
Relay Drivers					
Output Configuration	Non-Inverting	One Inverting, One Non-Inverting	Non-Inverting		
Enable	Y	Y	Y		
Inhibit					
Analog Stop					
Output Rise Time (ns)					
Maximum Voltage	20V	20V	18V		
Peak Output Current	3.0A	3.0A	1.5A / 2.0A		
Special Features	UVLO, Adaptive LEB	UVLO, Adaptive LEB	UVLO		
Application / Design Note					
Pin Count ❖	8, 16	8, 16	16		
Page Number	PS/6-73	PS/6-73	PS/6-79		

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Supply Support

Power Supply Support

Feedback Signal Generators	UNITRODE PART NUMBER			
	UC3901	UC39431	UC39432	UC3965
Description	Isolated Feedback Generator	Precision Adjustable Shunt Regulator	Precision Analog Controller	Precision Reference with Low Offset Error Amplifier
Application	Amplitude Modulation System Used to Couple a Control Signal Across a Voltage Isolation Barrier	Adjustable 100mA Shunt Regulator, Voltage Reference Optocoupler Driver, Voltage to Current Converter	Adjustable 100mA Shunt Regulator, Optocoupler Driver, Programmable Transconductance Voltage to Current Converter	Used for High Precision PWM Switching Regulators
Key Features	•Transformer Couples Isolated Feedback Error Signal •Low Cost Alternative to Optical Couplers •5MHz Carrier Provides Fast Response Capability •Modulator Synchronizable to an External Clock	•Multiple On-chip Programmable Reference Voltages •2.2V to 36V Operating Supply Voltage and User Programmable Reference •Linear Transconductance for Optocoupler Feedback Applications	•Programmable, Linear Transconductance for Optimum Optocoupler Current Drive •Precision Reference and Error Amplifier Inputs Externally Available •2.2V to 36V Operating Supply Voltage and User Programmable Reference	•2.5V Precision Reference with 0.4% Accuracy •Low 1mV Offset Error Amplifier •2X Inverting Amplifier / Buffer Output •Drivers Optocoupler Diode for Isolated Applications
Application / Design Note	DN-19, DN-33, U-94		DN-52	U-165
Pin Count ❖	14, 16	8	8	8
Page Number	PS/7-21	PS/7-50	PS/7-56	PS/7-60

❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Supply Support (cont.)

Load Share Controllers	UNITRODE PART NUMBER		
	UC3902	UC3907	
Description	8-Pin Load Share Controller	Load Share Controller	
Application	Allows Multiple Independent Power Supplies to be Paralleled so that Each Unit Supplies Only its Proportional Share of Total Load Current	Allows Multiple Independent Power Supplies to be Paralleled so that Each Unit Supplies Only its Proportional Share of Total Load Current	
Key Features	•Highly Tolerant of Voltage Differences Between Power Supply Return •2.7V to 20V Operation •High Gain, Low Offset Current Sense Amplifier Permits Low Shunt Resistor Values •Single Capacitor Sets Load Share Filter Response	•Fully Differential High Impedance Voltage Sensing •Accurate Current Amplifier for Precise Load Sharing •Optocoupler Driving Capability •4.5V to 35V Operation	
Application / Design Note	U-129, U-163	U-129, U-163	
Pin Count ❖	8	16	
Page Number	PS/7-27	PS/7-44	

Schottky Diode Array / Bridges	UNITRODE PART NUMBER		
	UC3610	UC3611	UC3612
Description	Dual Schottky Diode Bridge	Quad Schottky Diode Array	Dual Schottky Diode
Application	Eight-diode Array for High Current, Low Duty Cycle Flyback Voltage Clamping for Inductive Loads	Four-diode Array for High Current Bridges and Voltage Clamps	Two-diode Array for High Current, Low Duty Cycle Flyback Voltage Clamping for Inductive Loads
Key Features	•Monolithic Eight-diode Array •High Peak Current •Low Forward Voltage •Fast Recovery Time	•Matched, Four-diode Monolithic Array •High Peak Current •Low Forward Voltage •Parallelable for Higher Current or Lower Voltage Drop	•Monolithic Two-diode Array •High Peak Current •Low Forward Voltage •Fast Recovery Time
Application / Design Note			DN-48
Pin Count ❖	8, 16	8, 16	8
Page Number	PS/7-10	PS/7-12	PS/7-15

❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Supply Support (cont.)

Supervisory and Monitor Circuits	UNITRODE PART NUMBER				
	UC3543	UC3544	UC3730	UC3903	UC3904
Power Supply Monitor	Single	Single		Quad	Quad
Temperature Monitor			Y		
Description	Power Supply Supervisory with OV, UV and Current Sensing	Power Supply Supervisory with OV, UV and Current Sensing	Combines a Temperature Transducer, Precision Reference, and Temperature Comparator for Maximum System Flexibility	Quad Supply and Line Monitor	Quad Supply and Line Monitor
Voltage Clamp					
Voltage Range	5V to 35V	5V to 35V		8V to 40V	4.75V to 18V
Window Adjust	N	N		Y	Y
Current Range					
Current Limit	Y	Y		N	N
Programmable Threshold	Y	Y		Y	Y
Programmable Time Delay	Y	Y		Y	Y
Special Features		Uncommitted OV Inputs			
Application / Design Note				DN-33	
Pin Count ❖	16	18	5, 8, 20	18	18
Page Number	PS/7-5	PS/7-5	PS/7-17	PS/7-32	PS/7-39

Supervisory and Monitor Circuits	UNITRODE PART NUMBER		
	UCC3946		
Description	Microprocessor Supervisor with Watchdog Timer		
Application	Accurate Microprocessor Supervision		
Key Features	• Programmable Reset Period • Programmable Watchdog Period • 1.5% Accurate Threshold • 4mA IDD		
Pin Count ❖	8		
Page Number	PP/7-88		

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Motion Control

Brushless Motor Products	UNITRODE PART NUMBER				
	UC3625	UCC3626+			
Hall Logic	Y	Y			
Tachometer	Y	Y			
Output Current per Output	0.1A	0.01A			
Operating Voltage	10V - 18V	11V - 15V			
Differential Current Sense Amplifier	Y	Y			
Current Limit	Y				
Application / Design Note	DN-50, U-115, U-120, U-130	U-120			
Pin Count ❖	28	28			
Page Number	PS/8-37	PS/8-50			

DC Motor Controllers	UNITRODE PART NUMBER				
	UC3637	UC3638			
Output Clamp Diodes					
Output Current per Output	0.1A	0.1A / 0.05A			
Operating Voltage	5V - 36V	10V - 36V			
Differential Current Sense Amplifier		Y			
Thermal Shutdown					
Current Limit	Y	Y			
Application / Design Note	DN-53A, U-102, U-112, U-120	DN-76, U-120			
Pin Count ❖	18, 20	20			
Page Number	PS/8-78	PS/8-84			

❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Motion Control (cont.)

Linear Power Amplifier Products	UNITRODE PART NUMBER				
	UC3173A	UC3175B	UC3176	UC3177	UC3178
Output Clamp Diodes	Y	Y	Y	Y	Y
Output Current per Output	0.55A	0.8A	2A	2A	0.45A
Operating Voltage	4V - 15V	4V - 15V	3V - 35V	3V - 35V	3V - 15V
Differential Current Sense Amplifier	Y	Y	Y	Y	Y
Thermal Shutdown	Y	Y	Y	Y	Y
Current Limit	Y	Y	Y	Y	Y
Four Quadrant	Y	Y	Y	Y	Y
Number of Outputs	2	2	2	2	2
BW	2MHz	2MHz	1MHz	1MHz	2MHz
Special Features			B+ Input Pin	Supply OK Pin	
Pin Count ❖	24	24	28	28	28
Page Number	PS/8-5	PS/8-16	PS/8-21	PS/8-21	PS/8-25

Phase Locked Frequency Controllers	UNITRODE PART NUMBER				
	UC3633	UC3634	UC3635		
Internal Oscillator	Y	Y	Y		
Divider Output Provided			Y		
External Phase Detector Inputs			Y		
2 Phase Drive Logic		Y	Y		
Divide Logic Select	4/5 & 2/4/8	2/4/8	2/4		
Operating Voltage	8V - 15V	8V - 15V	8V - 15V		
Maximum Frequency	10MHz	10MHz	10MHz		
Application / Design Note	U-113	U-113	U-113		
Pin Count ❖	16, 20	16, 20	16		
Page Number	PS/8-63	PS/8-70	PS/8-74		

❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Motion Control (cont.)

Stepper Motor Controllers	UNITRODE PART NUMBER				
	UC3517	UC3717	UC3717A	UC3770A	UC3770B
Output Clamp Diodes		Y	Y	Lower	Lower
Output Current per Output	0.35A	0.8A	1A	1.3A	1.3A
Operating Voltage	10V - 40V	10V - 45V	10V - 46V	10V - 50V	10V - 50V
Differential Current Sense Amplifier					
Thermal Shutdown		Y	Y	Y	Y
Current Limit		Y	Y	Y	Y
Current Sense Thresholds					Tailored for half stepping applications
Application / Design Note		U-99	U-99		
Pin Count ❖	16	16, 20	16, 20	16, 28	16, 28
Page Number	PS/8-30	PS/8-92	PS/8-100	PS/8-108	PS/8-108

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Special Functions

Special Functions

Current Sensors	UNITRODE PART NUMBER				
	UCC3926				
Application	Current Sensing				
Maximum Current	±20A				
Application / Design Note	DN-91				
Pin Count ❖	16				
Page Number	PS/9-43				

Lighting Controllers	UNITRODE PART NUMBER				
	UCC3305✣				
Application	Constant Power HID Lamp Controller				
Topology	Boost, Flyback				
Outputs	3 - Single and Dual Alternating, Totem Pole				
Reference Tolerance	2%				
Open Lamp Detect	Y				
Soft Start	Y				
External Synchronization	Y				
Shutdown Current	N/A				
Maximum Frequency	500kHz				
Lamp Intensity Control	Y				
Application / Design Note	DN-72, U-161				
Pin Count ❖	28				
Page Number	PS/9-5				

❖ The smallest available pin count for thru-hole and surface mount packages.
✣ Does Not Feature UVLO.
+ New Product

Special Functions (cont.)

Ring Generator Controllers	UNITRODE PART NUMBER		
	UCC3750	UCC3751+	UCC3752+
Description	Source Ringer Controller	Single Line Ring Generator Controller	Mulit-Line Ring Generator Controller
Application	4 Quadrant Flyback Controller Develops High Voltage AC Output	Controls Low Cost Circuit for Generating High Voltage AC Output with DC Offset	Controls Low Cost Circuit for Generating High Voltage AC Output with DC Offset
Key Features	• On Chip Low THD Sinewave Reference, Pin Selectable 20Hz, 25Hz, and 50Hz • Programmable Output Amplitude and DC Offset • AC and DC Current Limiting With Short Circuit Protection	• Off-hook Detection With Automatic Transition to DC Operation • Pin Selectable 20Hz, 25Hz, and 50Hz Output Frequency • Operates From a Single 12V Supply • AC Current Limiting and Short Circuit Protection	• Off-hook Detection and Indication • Pin Selectable 20Hz, 25Hz, and 50Hz Output Frequency • Operates From a Single 12V Supply • AC Current Limiting and Short Circuit Protection
Application / Design Note	DN-79, U-169		
Pin Count ❖	28	16	16
Page Number	PS/9-22	PS/9-32	PS/9-38

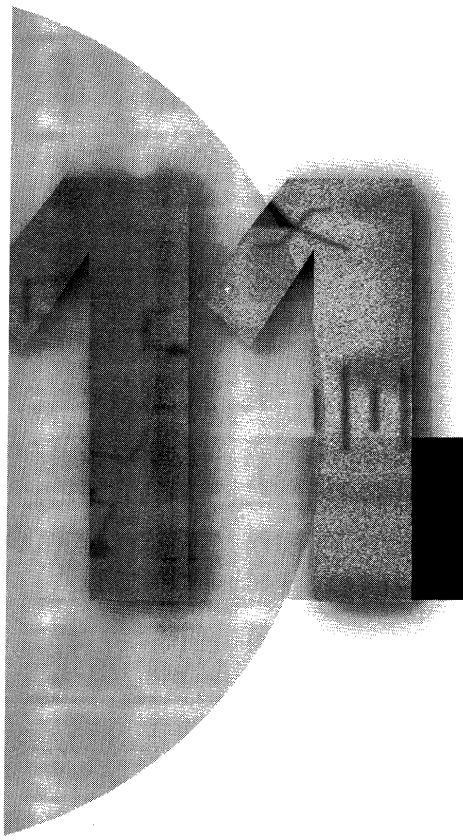
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Special Functions (cont.)

Sensor Drivers	UNITRODE PART NUMBER				
	UC37131+	UC37132+	UC37133+		
Part Name	Smart Power Switch	Smart Power Switch	Smart Power Switch		
Description	65V Universal Low Side Driver with Current Limiting	65V Universal High or Low Side Driver with Current Limiting	65V Universal High Side Driver with Current Limiting		
Pin Count ❖	8	14, 16	8		
Page Number	PS/9-13	PS/9-13	PS/9-13		

Serial DACs	UNITRODE PART NUMBER		
	UCC5950		
Part Name	Digital to Analog Converter		
Description	10-Bit BiCMOS Digital to Analog Converter for Servo and Instrumentation Systems		
Pin Count ❖	8		
Page Number	PS/9-48		

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product



Packaging Information

Index

Unitrode Portable Power Products Standard Packages

Unitrode's standard packages for portable power products are described in the following tables.

Package Type	Description	No. Pins	Device
DP	SOIC Narrow, 0.150"	8	UCC381 UCC384 UCC386/7/8
		16	UCC3911 UCC3952 UCC3958
J	Ceramic DIP, Glass Seal	8	UCC3941 UCC39411/2/3 UCC3946 UCC3972
		16	UC3906
		18	UC3871
		20	UC3909 UCC3956
L	Ceramic LCC	20	UC3906
		28	UC3909
PN (N)	Plastic DIP, 0.300"	8	bq2000/T bq2002/C/D/E/F/G/T bq2056/T/V bq2902 UCC3941 UCC39411/2/3 UCC3946 UCC3954 UCC3972 UCC5341
		14	bq2903 UC3872 UCC5342
		16	bq2003 bq2004/E/H bq2031 bq2054 bq2954 UC3906 UCC39421/2 UCC5343
		18	UC3871
		20	bq2005 UC3909 UCC3956 UCC39401 UCC39421/2
		24	bq2007
Q	Quad PLCC	20	UC3871 UC3872 UC3906
		28	UC3909
S (DW)	SOIC 0.300"	16	bq2003 UC3872 UC3906
		18	UC3871
		20	bq2005 UC3909 UCC3956
		24	bq2007

Package Type	Description	No. Pins	Device
SN (D)	SOIC Narrow, 0.150"	8	bq2000/T bq2002/C/D/E/F/G/T bq2018 bq2056/T/V bq2902 UCC3941 UCC39411/2/3 UCC3946 UCC3954 UCC3972 UCC5341
		14	bq2903 UCC5342
		16	bq2004/E/H bq2010 bq2011/J/K bq2012 bq2013H bq2014/H bq2031 bq2040 bq2050/H bq2052 bq2054 bq2058/T bq2092 bq2945 bq2954 UCC5343
SS (M)	SSOP/QSOP, 0.150"	16	UC3872 UCC3957 UCC5342 UCC5343
		28	bq2060
T	TO-220	3	UCC383
		5	UCC383
TD	TO-263, Power SMT	3	UCC383
		5	UCC383
TS (PW)	TSSOP 0.172"	8	bq2000/T bq2018 UCC386/7/8 UCC39411/2/3 UCC3946 UCC3972
		14	UCC3954
		16	UCC39421/2 UCC3952
		20	UCC39401 UCC39421/2
		24	UCC3958

Recommended Profile Limits

Packaging Information

The following are Unitrode's recommended profiles and limits for plastic package surface-mounting and de-soldering methods. To achieve and maintain the recommended conditions near the plastic package, time/temperature profiles of the surface-mount processing equipment may differ from those below, depending on board density, oven mass, exhaust rate, and other factors.

Unitrode uses a solder reflow pre-conditioning process with a 220°C peak temperature to determine moisture-sensitivity ratings for plastic packaged components. The profiles shown are used with Unitrode's moisture-sensitivity ratings of the plastic packaged surface-mount components. Published moisture-sensitivity ratings may not apply when a process with a more extreme peak temperature (such as wave solder) is used. If the temperatures or rates of temperature increase exceed those noted for IR reflow, then we recommend that the packaged component be either baked before surface-mount assembly or handled in consistence with the next lower moisture-sensitivity rating. (For example, handle a Level-2 rated part as Level 3.) For baking conditions and/or definitions of moisture-sensitivity level ratings, consult JEDEC J-STD-020A and J-STD-033.

For more than one soldering pass (e.g., on boards with components on top and bottom), time between the two soldering processes must be between 5 minutes and 48 hours. Between passes, if the environmental conditions of the plastic packaged component exceed 30°C/60% RH, then the component must be baked before the second pass.

Wave Solder *(Temperatures unless otherwise noted apply to the top-side of the component body.)*

- Maximum rate of increase for pre-heat 6°C/s
- Pre-heat temperature range 100–150°C
- Total pre-heat time 60–120 seconds
- Maximum rate of increase to maximum solder temperature 3°C/s
- Solder temperature of first (turbulent) wave < 250°C (4 seconds maximum)
- Solder temperature of second (broad) wave < 240°C (10 seconds maximum, 2°C/s maximum rate of cooling from first wave)
- Maximum cooling to room temperature 4°C/s maximum
- Total time over 183°C < 90s
- Difference between the maximum pre-heat and maximum soldering temperatures ≤ 100°C
- Maximum time from 25°C to peak temperature 6 minutes
- Minimum 5-minute cool-down time between cycles

NOTE: We **STRONGLY RECOMMEND** that the component's plastic body not contact the solder wave or bath during assembly. Contact can be prevented by shielding. If contact occurs, then do the following:

- Pre-bake parts within 4 hours before board-mount assembly (24 hours at 125°C or 192 hours at 40°C).
- Limit all rates of temperature change to 2.5°C/s.
- Limit total time over 183°C to less than 45s.

Recommended Profile Limits (cont.)

IR Reflow or Convection Reflow (Temperatures unless otherwise noted apply to the top-side of the component body.)

- Maximum rate of increase for pre-heat 6°C/s
- Pre-heat temperature range 100–150°C
- Total pre-heat time 60–120s
- Maximum rate of increase to maximum solder temperature 3°C/s
- Maximum reflow temperature < 240°C (20s maximum with 5°C of peak temperature)
- Maximum rate of decrease to room temperature 6°C/s
- Maximum time over 210°C < 40s
- Maximum total time over 183°C < 150s
- Difference between the maximum pre-heat and maximum soldering temperatures ≤ 100°C
- Maximum time from 25°C to peak temperature 6 minutes
- Minimum 5-minute cool-down time between cycles

Vapor Phase Reflow *(Temperatures unless otherwise noted apply to the top-side of the component body.)*

- Maximum rate of increase for pre-heat 6°C/s
- Pre-heat temperature range 100–150°C
- Total pre-heat time 60–120s
- Maximum rate of increase to maximum solder temperature 10°C/s
- Maximum reflow temperature < 219°C (60s maximum with 5°C of peak temperature)
- Maximum rate of decrease to room temperature 10°C/s
- Maximum time over 183°C < 80s
- Difference between the maximum pre-heat and maximum soldering temperatures ≤ 100°C
- Minimum 5-minute cool-down time between cycles

Rework *(Temperatures unless otherwise noted apply to the top-side of the component body.)*

To preserve the integrity of the plastic packaged component (for further analysis), we suggest the following steps to minimize damage from component removal:

- Always keep the package body temperature below 200°C.
- Bake out moisture in packages rated JEDEC Level 2-6 or in packages exposed to uncontrolled ambient conditions since being assembled.
- For hand de-soldering (i.e., with a soldering iron), do not allow maximum temperature at the leads to exceed 300°C for more than 5s.

For forced-hot-air de-soldering, the following limits apply:

- Limit the rate of temperature increase to 25°C/s between ambient and 100°C.
- Limit the rate of temperature increase to 4°C/s maximum from 100°C to de-soldering temperature.
- Limit maximum de-soldering temperature at leads to less than 240°C (10s maximum).
- Carefully minimize the cooling rate after removing the part from the printed circuit board.

Device Temperature Management

Introduction

All operating circuit components dissipate power, causing their temperature to rise. Unitrode integrated circuits are designed to operate in a considerable range of temperatures, but there are limits. This note suggests ways to ensure that specified temperature limits for each part are not exceeded.

Junction Temperature (Tj)

For reliability and long-term operating life of the device, the system designer must manage the power dissipated by the device in the system so junction temperature (Tj) not only does not exceed specified limits, but also is kept as low as possible. This temperature control is necessary, because higher junction temperatures adversely affect the operating life of the device.

Power Dissipation (Pd) and Thermal Resistance (q)

With power off, all components of a given circuit approach (and in time reach) ambient temperature. With the power on, the components are warmed by their internal power dissipation until a new equilibrium is reached. Some electrical power is dissipated as heat by an integrated circuit (Pd) during operation, raising the junction temperature. The effectiveness of the IC package and the system in dissipating this heat is "thermal resistance" (θ), a term analogous to electrical resistance in the sense that the materials of the IC, package, and system restrict the flow of heat from the higher junction temperature (Tj) to the lower ambient temperature of the system (Ta). Understanding the thermal resistance characteristics of the package and system facilitates management of the device junction temperature within desired limits.

The rate of heat flow depends on the temperature difference (DT) between the two endpoints (Tj and Ta), and also on the thermal resistance, θ, of the package and system. Heat is a form of energy, and if we choose the joule as the measuring unit we can specify the rate of heat flow in units of joules per second. Therefore,

$$Pd\left[joules\,per\,\mathrm{sec}ond\right] = \frac{\Delta T}{\theta}$$

and since one *joule per second* is the same as a watt (W), we have

$$\theta = \frac{\Delta T}{Pd}(^{\circ}C/W)$$

Thermal resistance is typically expressed in terms of resistance from junction-to-ambient (θja), which incorporates not only the internal resistance of the IC package, but also the resistance of the system as well. θja can be broken down into the sum of these two different thermal resistances, from junction-to-case, θjc (or in the case of power surface-mount packages, junction-to-lead, θjl), and case-to-ambient, θca. Therefore,

$$\theta ja = \frac{Tj - Ta}{Pd} = \theta jc + \theta ca$$

Variables Which Affect Θja

The thermal resistance of the package is a function of many variables, such as the leadframe material and design configuration, the plastic encapsulant material, the silicon die area, the die attach material, and others. However, as previously indicated, the effectiveness of the system in removing heat from the package also has a significant impact on θja. These variables include the material and configuration of the circuit board on which the package is mounted, the type of cooling used (i.e., conduction or convection), the size of the traces on the circuit board, the use of heatsinks, etc. It is essential that the system designer understand these variables and how they affect θja.

Unitrode Test Procedures

Table 1 shows thermal resistance values for Unitrode IC packages. Thermal resistance junction-to-case (θjc) is measured by mounting the device to an essentially infinite heat sink. Power leadframe surface-mount packages and the batwing DIP conduct most of the dissipated power through their leads rather than through the case. For these noted packages, the specified thermal resistance is junction-to-lead (θjl).

Junction-to-ambient (θja) thermal resistance is measured on a 5.0-square-inch printed circuit board in 1 cubic foot of still air. For through-hole packages, single-side FR-4 boards with 1-ounce copper traces are used. (See Figure 1.) However, since surface-mount devices, including those without power leadframes, conduct a significant amount of heat through their leads to the pc-board, various types of surface-mount boards are measured. (See Figure 2.) To indicate the effect of the pc-board on θja, a range of values is given. The lower value is for a device mounted on a 5.0-square-inch, 0.062 inch thick aluminum pc-board. The highest value is for a device mounted on a 5.0-square-inch single-sided pc-board. These values are intended to give the system designer an indication of the best and worst case conditions. Some interpolation may be needed based on an individual application to arrive at an accurate estimate of the actual θja.

To determine the device θja, a measurement of the device junction temperature is made under the above conditions using a technique called the "temperature-sensitive parameter" method. This technique involves measuring the voltage drop of calibrated component, typically a diode, which then allows calculation of the device junction temperature. Since Pd, Tj, and Ta are known, θja can be determined. For the case of power leadframe surface-mount packages, θjl is determined by measuring the temperature of the pc-board at the device leads and then using this temperature in place of the ambient temperature in the calculation. For a more detailed discussion on surface-mount packages, refer to "Thermal Characteristics of Surface-Mount Packages," found later in this section.

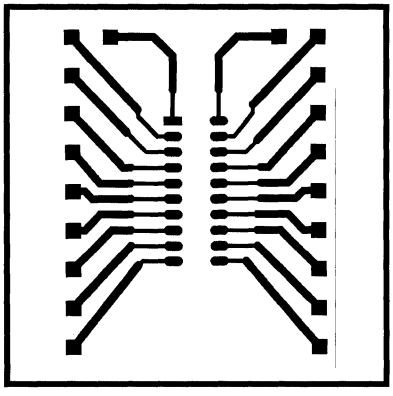


Figure 1. Typical through-hole pc-board design.

Example

Estimate the junction temperature of a UC5601DWP 18-Line SCSI Active Terminator on a 4-layer 0.062 inch thick multilayer pc-board at 1.0 watt power dissipation in a still-air environment at 30°C.

1. Determine θja. Table 1 shows that the the DWP package is a power leadframe surface-mount device, so the use of thermal resistance junction-to-lead (qjl) is appropriate. For the DWP package, qjl = 16°C/W. From Figure 8 in "Thermal Characteristics of Surface-Mount Packages," thermal resistance board-to-ambient (θba) = 19°C/W. We know that for a power leadframe surface-mount package, θja = θjl + θba, so, θja = 16°C/W + 19°C/W = 35°C/W.

2. Calculate the junction temperature, Tj.

Tj = (Pd x θja) + Ta
Tj = (1.0 W x 35°C/W) + 30°C
Tj = 65°C

This is well below the maximum rated junction temperature of 150°C listed in the Absolute Maximum Ratings section of the UC5601 product data sheet, so the thermal dissipation is satisfactory.

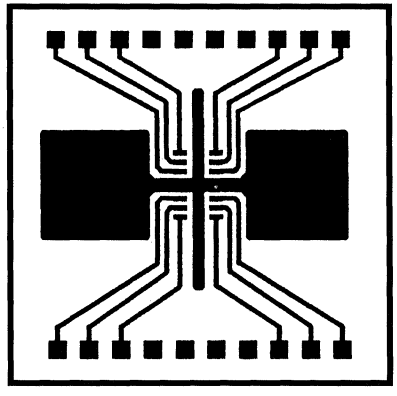


Figure 2. Typical surface-mount pc-board design for power leadframe SOIC packages.

System Design Considerations

Through-hole devices such as dual in-line packages (DIPs) can be cooled by forcing airflow over the device in order to improve the convection cooling performance, or by conduction cooling of the package case to a heat sink such as the system chassis or cold-wall. Plastic DIPs are not particularly well suited to either of these techniques since the plastic encapsulant is a relatively poor thermal conductor. However, Unitrode offers several through-hole packages which have been optimized for conduction cooling techniques, namely the batwing DIP, the SP power ceramic DIP and the power leadframe Zig-Zag (ZIP) package. All of these packages provide low thermal resistance paths from the junction to the pc-board. Refer to Table 1 for the applicable ratings.

Surface-mount packages are well suited to conduction cooling since, as previously indicated, the package leads conduct a significant amount of heat to the pc-board. The pc-board itself can be utilized effectively as a heat sink when designed properly. For example, as seen in the discussion "Thermal Characteristics of Surface Mount Packages," when a power leadframe package is mounted on a multi-layer pc-board such that the heat-sink leads are thermally coupled to a ground plane in the board, or an area of copper fan-out on the board, then the overall thermal resistance is considerably lower than on a single-sided board with no heat-sinking. Additionally, Unitrode offers a power ceramic leadless chip carrier with a metallized thermal grid on the package case, which can be soldered directly to the board, thus greatly reducing its overall thermal resistance.

In general, the system designer should attempt to use larger traces on the pc-board where possible in order to spread the heat away from the device more effectively. Also, one should avoid grouping higher power devices tightly together on the board. A better approach would be to spread out the higher power devices to the cooler areas of the board. The choice of pc-board material will greatly affect the overall thermal performance of the system as well, although there are many factors involved when selecting the board material, such as cost, mechanical properties and environmental requirements.

Summary

Thermal management has been shown to be an essential factor in the reliable use of Unitrode integrated circuits. Thermal characteristics of Unitrode packages have been provided to the system designer in order to ensure that the system design effectively dissipates the power generated by the integrated circuit during operation.

Package Thermal Resistance Data

Package	Lead Count	Unitrode Package Code	Body Size (mils unless noted)	Die Paddle or Cavity Size (mils)	Die Size Tested (mils) (16)
Ceramic DIP	8	J	390x288x140	150x200	N/A
	14		760x248x140	110x140	N/A
	16		760x288x140	160x250	N/A
	18		890x288x140	160x250	N/A
	20		950x288x140	160x250	N/A
	24		1250x520x170	250x250	N/A
	28		1450x520x165	250x250	N/A
Ceramic LCC	20	L	350x350x80	194x194	N/A
	28		450x450x80	250x250	N/A
Ceramic LCC Power	28	LP	450x450x80	250x250	N/A
LQFP	48	FQ	7x7x1.4 mm	200x200x5	100x100x12
	64		10x10x1.4 mm	260x260x5	100x100x12
	100		14x14x1.4 mm	276x276x5	100x100x12
LQFP Power	48	FQP	7x7x1.4 mm	185x185x5	100x100x12
	48		7x7x1.4 mm	190x190x5	100x100x12
MSOP	8	P	3x3x0.86 mm	68x94x6	50x50x8
	10		3x3x0.86 mm	68x98x6	50x50x8
PDIP	8	N	360x253x137	140x150x10	N/A
	14		760x253x137	110x140x10	N/A
	16		760x253x137	140x170x10	N/A
	18		905x253x137	160x250x10	N/A
	20		1020x253x137	150x190x10	N/A
	24		1250x525x137	180x220x10	N/A
	28		1425x525x137	200x200x10	N/A
PDIP Power	16	NP	760x253x137	160X170X10	N/A
PLCC	20	Q	350x350x155	180x180x10	N/A
	28		450x450x155	230x230x10	N/A
	44		650x650x155	230x230x10	N/A
PLCC Power	28	QP	450x450x155	200x200x10	N/A
	44		650x650x155	300x300x10	N/A

* = Estimated N/A = Not Available

** = Modeled Data. If value range given for θja, lower value is for 3x3 in. 1 oz. internal copper gnd plane, higher value is for 1x1 in. gnd plane. All model data assumes only one trace for each non-fused lead.

Package Thermal Resistance Data

θja (°C/W) (6)(15)	θjc (°C/W) (15)	Comments
125-160	28 (8)	
90-120	28 (8)	
80-120	28 (8)	
70-90	28 (8)	
70-85	28 (8)	
60-75	28 (8)	
50-65	28 (8)	
70-80	20 (8)	
60-70	20 (8)	
N/A	5-8*	θjc estimated for backside of device, through the metalized thermal conduction pads.
58-76**	15**	Modeled using .3 mm trace width
44-59**	12**	Modeled using .3 mm trace width
31-46**	11**	Modeled using .3 mm trace width
34 (9) 38-61**	8**	Leads 5,6,7,8,17, 18,19,29,30,31,32, 42,43 and 44 are fused to the die attach paddle. Modeled with 2 thermal vias to gnd plane per fused lead and .3 mm trace width.
35 (10) 43-65**	8**	Leads 4,5,6,7,8,9,28,29,30,31,32 and 33 are fused to the die attach paddle. Modeled with 2 thermal vias to gnd plane per fused lead and .3 mm trace width.
238-269** 312-373**(7)	41**	Modeled using .3 mm trace width.
210-241** 273-330**(7)	39**	Modeled using .3 mm trace width.
110 (3)	50	
90 (3)	45	
90 (3)	45	
85 (3)	40	
80 (3)	35	
60 (3)	30	
60 (3)	30	
25-50 (4)	12 (2)	Leads 4,5,12 and 13 are fused to the die attach paddle.
43-75 (3)	34	
40-65 (3)	30	
35-50 (3)	20	
28-50 (3)	14 (2)	Leads 12,13,14,15,16,17 and 18 are fused to the die attach paddle. Single layer board used 1.2 in^2 of 1 oz copper on top of PWB for heatsinking to fused leads.
24-38 (3)	12 (2)	Leads 6,7,17,29,39 and 40 are fused to the die attach paddle. Single layer board used 1.1 in^2 of 1 oz copper on top of PWB for heatsinking to fused leads.

Package Thermal Resistance Data

Package	Lead Count	Unitrode Package Code	Body Size (mils unless noted)	Die Paddle or Cavity Size (mils)	Die Size Tested (mils) (16)
QSOP	16	M	193x154x59	96x130x8	50x50x12
	20		340x154x59	96x140x8	50x50x12
	28		389x154x59	96x150x8	50x50x12
QSOP Wide Body Power	36	MWP	606x295x92	180x240x10	100x100x15 100x100x12**
	44		704x295x92	190x260x10	100x100x15 100x100x12**
SOIC Narrow Body	8	D	192x154x54	95x152x8	N/A
	14		340x154x54	83x142x8	N/A
	16		390x154x54	90x150x8	N/A
SOIC Narrow Power	8	DP	192x154x54	95x150x8	N/A
	16		390x154x54	95x165x8	N/A
SOIC Wide Body	16	DW	408x296x94	165x205x10	N/A
	18		458x296x94	145x190x10	100x100x12
	20		508x296x94	165x205x10	N/A
	24		602x296x94	165x205x10	100x100x12
	28		705x296x94	165x205x10	100x100x12
SOIC Wide Body Power	28	DWP	705x296x94	156x205x10	N/A
TO220	3	T, TH, TV	400x592x165	180x180x18	N/A
	5		400x605x165	180x180x18	N/A
TO263	3	TD	395x415x175	240x180x23	N/A
	5		395x415x175	240x180x23	N/A
TSSOP	8	PW	118x174x35	126x87x5	50x50x10
	14		197x174x35	118x150x5	100x100x10
	16		197x174x35	118x154x5	100x100x10
	20		255x174x35	118x165x5	100x100x10
	24		307x174x35	118x217x5	100x100x10
	28		382x174x35	118x217x5	100x100x10
TSSOP Power	24	PWP	307x174x35	118x217x5	100x100x10
	28		382x174x35	118x250x5	100x100x10
	28		382x174x35	118x250x5	100x100x10

* = Estimated N/A = Not Available

** = Modeled Data. If value range given for θ ja, lower value is for 3x3 in. 1 oz internal copper gnd plane, higher value is for 1x1 in. gnd plane. All model data assumes only one trace for each non-fused lead.

θja (°C/W) (6)(15)	θjc (°C/W) (15)	Comments
144-172**	38**	Modeled using .3 mm trace widths.
116-138**	36**	Modeled using .3 mm trace widths.
96-118**	33**	Modeled using .3 mm trace widths.
31 (11) 36-52**	8**	Leads 8,9,10,26,27 and 28 are fused to the die attach paddle. Modeled with 2 thermal vias to gnd plane per fused lead and .5 mm trace width.
29 (12) 32-46**	7**	Leads 10,11,12,13,32,33,34 and 35 are fused to the die attach paddle. Modeled with 2 thermal vias to gnd plane per fused lead and .5 mm trace width.
84-160 (3)	42	
50-120 (3)	35	
50-120 (3)	35	
40-70 (3)	22 (2)	Leads 2,3,6 and 7 are fused to the die attach paddle.
36-58 (3)	20 (2)	Leads 4,5,12 and 13 are fused to the die attach paddle. Single layer board used .68 in^2 of 1 oz copper on top of PWB for heatsinking to fused leads.
50-100 (3)	27	
89-102**	26**	Modeled using .3 mm trace widths.
45-95 (3)	25	
71-83**	24**	Modeled using .3 mm trace widths.
65-76**	21**	Modeled using .3 mm trace widths.
30-50 (3)	16 (2)	Leads 7,8,9,20,21 and 22 are fused to the die attach paddle. . Single layer board used 0.165 in^2 of 1 oz copper on top of PWB for heatsinking to fused leads.
83*	3*	
65-75*	3*	
50-87*	3	
65-75*	3	
232-257**	32**	Modeled using .3 mm trace widths.
132-158**	15**	Modeled using .3 mm trace widths.
123-147**	15**	Modeled using .3 mm trace widths.
102-125**	14**	Modeled using .3 mm trace widths.
150 (3) 88-109**	13**	Modeled using .3 mm trace widths.
77-96**	13**	Modeled using .3 mm trace widths.
30-70 (3) 63-87**	20 (2) 9**	Leads 5,6,7,8,17,18,19 and 20 are fused to the die attach paddle. Empirical tests used 1.1 in^2 of 1 oz top copper on top of PWB for heatsinking to fused leads. Modeled with 2 thermal vias to gnd plane per fused lead and .3 mm trace width.
33 (13) 61-80**	20 (2) 11**	Leads 8 and 21 are fused to the die attach paddle. Modeled with 2 thermal vias to gnd plane per fused lead gnd plane and .3 mm trace width.
30-70 (3) 57-79**	20 (2) 9**	Leads 7,8,9,20,21 and 22 are fused to the die attach paddle. Modeled with 2 thermal vias to gnd plane per fused lead and .3 mm trace width.

Data Book numbers for thermal resistance are for reference in making relative package-to-package performance comparisons and are not a statement of absolute performance in a system application.

Notes:

1. All data assume testing with the long side of the die coinciding with the long side of the die attach-mounting area.
2. Specified thermal resistance is jl (junction to lead) where noted.
3. Specified θja (junction to ambient) is for devices mounted to 5-in^2 FR4 PC board with one-ounce copper where noted. When the resistance range is given, lower values are for 5-square-inch aluminum PC board. Test PWB was .062 inches thick and typically used 0.635 mm trace-widths for power packages and 1.3 mm trace-widths for non-power packages, with a 100 x 100-mil probe land area at the end of each trace. See "Thermal Characteristics of Surface Mount Packages," by John O'Connor.
4. Lower value is for 5-in^2 multilayer PC board. The multilayer PWB was 0.062 inches thick and typically used 0.635 mm trace-widths for power packages, 1.3 mm trace-widths for non-power packages, with a 100 x 100-mil probe land area at the end of each trace. The backside of the PWB used 1.0 mm traces in the X and Y directions to simulate 20% coverage by multilayer traces. Thermal vias were not used to connect fused leads to backside traces. (See "Thermal Characteristics of Surface Mount Packages," by John O'Connor.)
5. Lower value is with a finned heat-sink.
6. θja tests were performed in still air. θja results will vary depending on test conditions and setup. Airflow can lower the θja value stated by 15-30%, depending on air speed, package type, and PWB configuration.
7. Modeled with no internal ground-plane. Lower value is for 0.5 mm trace-widths, higher value for 0.3 mm trace-widths.
8. θjc data values stated were derived from MIL-STD-1835B. MIL-STD-1835B states, "*The baseline values shown are worst case (mean + 2s) for a 60 x 60-mil microcircuit device silicon die and applicable for devices with die sizes up to 14400 square mils. For device die sizes greater than14400 square mils use the following values: dual-in-line, 11°C/W; flat pack, 10°C/W; pin grid array, 10°C/W*".
9. Tested on multilayer 3 x 4.5 x .062-inch PWB with 2 1-oz copper internal planes, 10-mil trace-widths and 2.43 in^2 of 1-oz copper on top of PWB for heat-sinking to fused leads. Thermal vias were not used to connect fused leads to inner copper planes.
10. Tested on multilayer 3 x 4.5 x .062-inch PWB with 2 1-oz copper internal planes, 10-mil trace-widths and 1.53 in^2 of 1-oz copper on top of PWB for heat-sinking to fused leads. Thermal vias were not used to connect fused leads to inner copper planes.
11. Tested on multilayer 3 x 4.5 x .062-inch PWB with 2 1-oz copper internal planes, 10-mil trace-widths and 2.28 in^2 of 1-oz copper on top of PWB for heat-sinking to fused leads. Thermal vias were not used to connect fused leads to inner copper planes.
12. Tested on multilayer 3 x 4.5 x .062-inch PWB with 2 1-oz copper internal planes, 10-mil trace-widths and 2.74 in^2 of copper on top of PWB for heatsinking to fused leads. Thermal vias were not used to connect fused leads to inner copper planes.
13. Tested on multilayer 3 x 4.5 x .062-inch PWB with 2 1-oz copper internal planes, 10-mil trace-widths and 2.2 in^2 of 1-oz copper on top of PWB for heatsinking to fused leads. Thermal vias were not used to connect fused leads to inner copper planes.
14. Trace width for test PWBs is typically 10 mils.
15. Test conditions typically use a 110-125C junction temperature with an ambient temperature of 25-30°C.
16. Die size noted is for a thermal test die with a uniformly distributed heating area.

Typical Materials Used for Assembly

Package	Unitrode Package Code	Die Thickness (mils)	Die Attach (2)	Leadframe Material Thermal Conductivity (1)	Molding Compound or Package Material
Ceramic DIP	J	15	Eutectic or Silver Glass	75	Alumina
Ceramic LCC	L	15	Eutectic or Silver Glass	N/A	Alumina
Ceramic LCC Power	LP	15	Eutectic or Silver Glass	N/A	Alumina
Ceramic Sidebraze Power	SP	15	Eutectic	N/A	Alumina
LQFP	FQ	12	Silver Filled Epoxy	85-110	Standard, non-thermally enhanced epoxy
LQFP Power	FQP	12	Silver Filled Epoxy	220	Standard, non-thermally enhanced epoxy
PDIP	N	12	Silver Filled Epoxy	150	Standard, non-thermally enhanced epoxy
MSOP	P	8	Silver Filled Epoxy	150	Standard, non-thermally enhanced epoxy
PDIP Power	NP	12	Silver Filled Epoxy	150	Standard, non-thermally enhanced epoxy
PLCC	Q	12	Silver Filled Epoxy	208	Standard, non-thermally enhanced epoxy
PLCC Power	QP	12	Silver Filled Epoxy	208	Standard, non-thermally enhanced epoxy
QSOP	M	12	Silver Filled Epoxy	150	Standard, non-thermally enhanced epoxy
QSOP Wide Body Power	MWP	12	Silver Filled Epoxy	208	Standard, non-thermally enhanced epoxy
SOIC Narrow Body	D	12	Silver Filled Epoxy	150	Standard, non-thermally enhanced epoxy
SOIC Narrow Power	DP	12	Silver Filled Epoxy	208	Standard, non-thermally enhanced epoxy
SOIC Wide Body	DW	12	Silver Filled Epoxy	150	Standard, non-thermally enhanced epoxy
SOIC Wide Body Power	DWP	12	Silver Filled Epoxy	208	Standard, non-thermally enhanced epoxy
TO220	T	12	Silver Filled Epoxy	150	Standard, non-thermally enhanced epoxy
TO263	TD	12	Silver Filled Epoxy	150	Standard, non-thermally enhanced epoxy
TSSOP	PW	10	Silver Filled Epoxy	85-110	Standard, non-thermally enhanced epoxy
TSSOP Power	PWP	10	Silver Filled Epoxy	85-110	Standard, non-thermally enhanced epoxy

Note 1: $\frac{BTU \bullet in}{ft^2 \bullet hr \bullet ^\circ F}$ Leadframe downset is typically 8–15 mils. Leadframe thickness is typically 5–10 mils.

Note 2 : Die attach thickness is 0.5–1.5 mils for plastic devices; 1.9–2.4 mils for ceramic.

Table 1. Typical materials used for assembly.

UNITRODE

THERMAL CHARACTERISTICS OF SURFACE MOUNT PACKAGES

John A. O'Connor

Introduction

Surface mount packaging continues to expand market share, displacing dual in-line packages (DIPs) at an ever increasing rate. Smaller surface mount devices allow a significant increase in circuit density with a corresponding decrease in system size. Miniaturization is not without penalty however, as thermal management can quickly dominate system packaging design.

With the familiar DIP, the majority of heat is removed through the case. Typically, this is accomplished by convection air currents, although forced air or conduction cooling is often used in more demanding applications. Unlike the DIP however, the majority of heat is removed from surface mount packages through the leads. This means that the PC board design directly affects the thermal capability of surface mounted circuitry. For optimal thermal design, the integrated circuit, the package, and the PC board must be considered as a system.

Many designers use steady-state thermal behavior (thermal resistance) to predict IC junction temperature. While this approach certainly is valid for devices subjected to continuous power dissipation, it often results in an overly conservative design when dissipation varies over time. Generating a model which accounts for transient thermal behavior allows the designer to fully exploit the system's thermal mass. Instantaneous junction temperature can then be calculated, insuring reliability with minimal system size.

Thermal Model

Figure 1 shows the basic model which is expanded for more complex situations. The power dissipated is represented by the current source. Resistance to heat flow is represented by the resistor, and the thermal mass is represented by the capacitor. The analogous thermal units for the current, thermal resistance, and thermal capacitance are also shown in figure 1. Ground is ambient temperature, so all values are temperature rise above ambient. With more complex systems, it is usually easiest to initially convert to electrical units, analyze the circuit, then convert back to thermal units. This approach allows standard electrical circuit analysis tools and techniques to be used without unnecessary confusion.

A surface mounted device on a PC board can be modeled as in figure 2. Each R-C section roughly

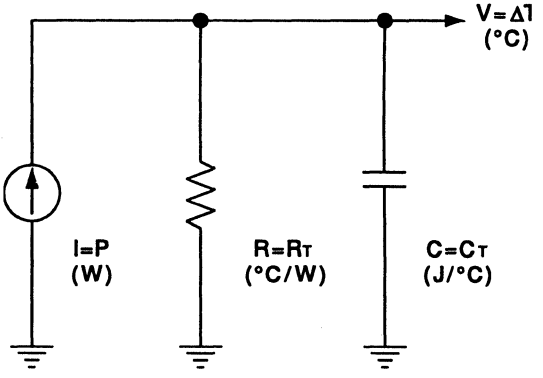


Figure 1. Basic Thermal Model

correlates to the physical system. The first R-C is the device die. The second is the lead frame and package, and the third is the PC board. Other parameters such as the junction to case and case to ambient thermal resistances, are lumped into the three R-C sections. This simplification does cause transient thermal response errors, although normally these errors are small. The additional elements can be broken out separately if greater accuracy is required. Although the physical correlation is far from perfect for the 3 R-C model, the thermal correlation can be very good.

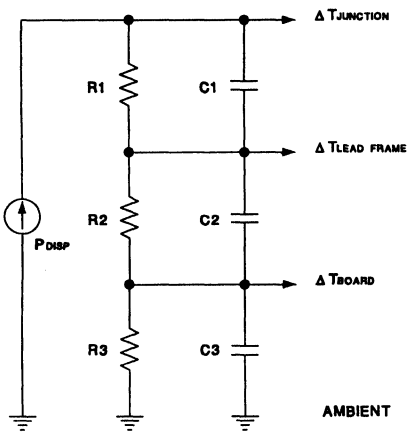


Figure 2. Surface Mounted Device on a PC Board Model

Parameter Measurement

The circuit technique shown in figure 3 can be used to evaluate the thermal performance of almost any IC. Device power dissipation must be known and constant. This is achieved with resistive loading for devices such as voltage regulators or amplifiers. Other devices may require additional circuitry to insure constant dissipation.

The change in forward voltage of a diode is typically utilized for temperature measurement, although any temperature dependant parameter could also be used. Ideally, the diode should be close to the output transistors for maximum accuracy. In practice, this is not critical since the temperature drop across the die will only be a few degrees C in a surface mountable IC. During the test, the measurement diode must not have any current other than the fixed bias current. The bias current should be as small as possible to avoid self-heating the diode.

Many devices have a diode intended for forward biased operation in the actual application circuit such as an output stage clamping diode. If such a diode is not available it may be necessary to forward bias a parasitic diode for measurement. While this approach should be considered a last resort, it can yield acceptable data. If a parasitic diode is forward biased, erratic or unspecified behavior is likely, even with low bias currents. Evaluate the test circuit carefully, insuring that dissipation is constant over the measurement temperature range.

Kelvin all connections to avoid interconnect voltage drops. Every 2mV is approximately 1°C, so even small DC offsets can cause significant error. Without any power applied to the device other than the diode bias current, characterize the diode's forward voltage in an oven at several temperatures over the expected operating junction temperature range. The slope of a best-fit line gives the thermal coefficient (T_C) which is used in subsequent calculations.

Thermocouples are used to sense PC board and ambient temperature. PC board temperature is measured as close to the device as possible.

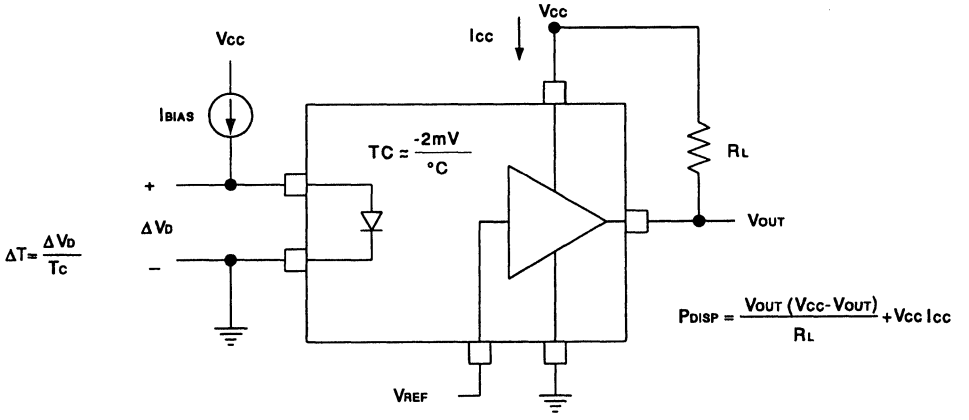


Figure 3. Typical Thermal Test Circuit

Some parameters are measured directly while others are derived by curve fitting. Junction to PC board, and PC board to ambient thermal resistance are measured by dissipating a constant power. Allow 15 minutes for the temperature to stabilize. The change in diode forward voltage and PC board temperature give the junction to ambient and board to ambient thermal resistance:

$$R_{(j\text{-}a)} = \Delta V_D / (T_C P_{DISP})$$
$$R_{(b\text{-}a)} = \Delta T_B / P_{DISP}$$

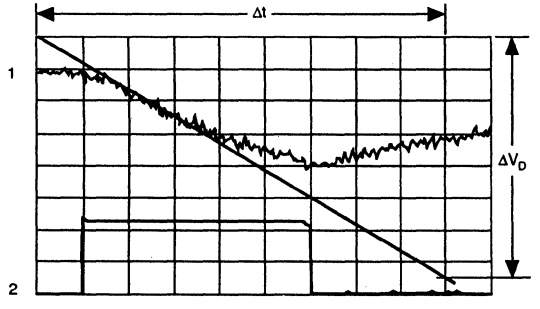
Note that these resistances are based on change in temperature - ambient is assumed constant for the duration of the test. These values correlate to R1, R2, and R3 by:

$$R1 + R2 = R_{(j\text{-}a)} - R_{(b\text{-}a)} \quad (1)$$

$$R3 = R_{(b\text{-}a)} \quad (2)$$

The thermal capacitance of the die is measured by applying a pulsed load and recording the junction temperature waveform. Varying the dissipation pulse width allows observation of each capacitance's effect, although only the die's thermal capacitance can be measured directly. A typical 10ms transient dissipation waveform is shown in figure 4. The thermal time constant of the die is on the order of 30ms. To minimize exponential decay error, the slope of the waveform is measured at (t) = 3ms. The die's thermal capacitance is then:

$$C1 = P_{DISP}\, \Delta t\, T_C / \Delta V_D \quad (3)$$



VERTICAL: (1) V_D, 1mV/DIV
(2) P_{DISP}, 1W
HORIZONTAL: 2ms/DIV

Figure 4: 10ms Transient Dissipation Waveform

Transient waveforms should also be taken for 100ms, 1s, and 10s dissipation intervals to generate an accurate temperature versus time curve. If transient thermal behavior is critical beyond 10 seconds then additional curves must be taken. The thermal time constant of the PC board can go out to several minutes, so a strip chart recorder or computer based data acquisition system will be required. For most systems, this additional data is unnecessary.

The remaining parameters are determined by curve fitting. Visual comparison of measured versus calculated curves is easily done with a spread sheet program. Measured junction temperature versus time data (4 points per decade is sufficient) is entered into the spread sheet. Junction temperature is then calculated at each point with estimated values for R2 and C2 and C3 using:

$$T(t) = P_{DISP}\,[R1(1-e^{-t/\tau 1}) + R2(1-e^{-t/\tau 2}) + R3(1-e^{-t/\tau 3})] \quad (4)$$

Data presented in the following section will help in estimating initial values. This procedure is iterated until an acceptable curve fit is achieved. C3's value is iterated only if the measured curve goes out to several minutes. Figure 5 is a typical measured and calculated junction temperature versus time curve. A logarithmic time axis aids in curve fitting by spreading data points evenly.

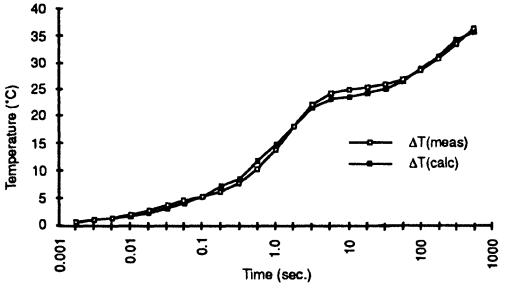


Figure 5. Juction Temperature versus Time for FQP48 Package Dissipating 1W.

Typical Data

The preceding technique was used to characterize two devices in nine different packages. Five different PC board types were also tested to provide relative comparison. This information should be used to help initially determine package, PC board type, and layout. It must be stressed that this typical data should not substitute for a rigorous thermal analysis of the actual application.

PACKAGE	R1 (°C/W)	C1 (J/°C)	τ1 (sec)	R2 (°C/W)	C2 (J/°C)	τ2 (sec)	R3 (°C/W)	C3 (J/°C)	τ3 (sec)	R(J-a) (°C/W)
D8	5	0.0035	0.02	64	0.030	1.9	15	24	360	84
D14	4	0.0045	0.02	45	0.035	1.6	16	24	384	65
DW16	4	0.0045	0.02	44	0.070	3.1	15	24	360	63
DW16	4	0.011	0.04	34	0.11	3.7	13	24	312	51
DWP28	2.5	0.008	0.02	13	0.13	1.7	15	24	360	30
Q20	3	0.010	0.02	26	0.12	3.1	14	24	336	43
Q28	2.5	0.008	0.02	25	0.12	2.9	13	24	312	40
QP28	2.5	0.009	0.02	12	0.25	3.0	14	24	336	28
FQ48	4	0.006	0.02	57	0.07	4.0	15	24	360	76
FQP48	4	0.005	0.02	21	0.08	1.7	14	25	350	39

Figure 6. Model Values Versus Package Type for 1W Dissipation on Aluminum PC Board.

Figure 6 shows model values and time constants versus package type, mounted on an aluminum PC board [1]. Junction to ambient thermal resistance is also shown to indicate overall steady state thermal performance. All data was taken with one watt dissipated. The values that were determined by curve fitting result in a fairly conservative model. Values were chosen which tended to predict higher temperature than actually measured where errors could not be eliminated. As indicated, two devices were used for testing. At 7,500 square mils, the UC3730 is representative of the smaller dies typically packaged in D8, D14, and DW16 packages. The UC3173 is 16,500 square mils, and is typical of the dies packaged in the other larger packages.

Both devices were packaged in the DW16 to isolate the effect of die size. The UC1730's smaller die increased R2 by about 30%. Interpolating between these two data points is difficult since the relationship between die size and thermal resistance is nonlinear. Curves are available which account for this dimensional difference [2], although the actual conditions differ and are more complicated than the configuration used to generate the curves. Fortunately, the resulting error will be small in most applications. Conservatively estimating R2 will minimally impact system size, but if a more accurate value is required the actual device can be characterized on a test PC board.

Figure 7 illustrates the power lead frame's dramatic improvement in thermal performance over standard lead frames by comparing the junction to ambient thermal resistances of the QP28 to the Q28, and the FQP48 to the FQ48. Standard lead frames connect the die to the leads thermally through the epoxy molding compound. Power lead frame packages incorporate a single piece for die attachment and ground leads. This uninterrupted, high thermal conductivity path offers a significant improvement over standard lead frames. Occasionally a stiffer but less conductive alloy is used for standard lead frames. The FQ48's poorer thermal performance is partially caused by the lower conductivity alloy.

Printed circuit board design significantly affects the overall thermal performance of the system, particularly with the power lead frame packages. The UC3173 in the DWP28 package was used to

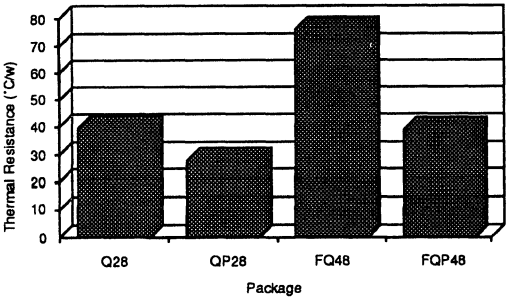


Figure 7. Power lead frames significantly reduce thermal resistance.

compare PC board thermal performance. Five different PC board types were evaluated with one watt dissipated:

1. Single side 1 oz. copper, 0.062 aluminum
2. Single side 1 oz. copper, 0.062 FR4 epoxy fiberglass
3. Single side 2 oz. copper, 0.062 FR4 epoxy fiberglass
4. Four layer (signal, ground, Vcc, signal) 1 oz. copper, 0.031 FR4 epoxy fiberglass
5. Four layer (signal, ground, Vcc, signal) 1 oz. copper, 0.062 FR4 epoxy fiberglass

PCB TYPE	R(b-a) (°C/W)	C(b-a) (J/°C)	τ (sec)
Aluminum	15	24	360
FR4 -1oz.	31	2.5	78
FR4 -2oz.	25	3	74
4 layer - 0.031	21	4	84
4 layer - 0.062	19	5	94

Figure 8. Board to ambient thermal resistance and capacitance versus PC board type for DWP28 package dissipating 1W.

The thermal resistance, capacitance, and time constants for the five PC boards are shown in figure 8. The PC board layouts used for testing are shown in figure 9. Only the component side is shown for the four layer boards. The back side, which has 10 mil traces on 50 mil centers to provide a typical amount of interconnect copper, and the Vcc plane were unconnected. The inner ground plane is connected to the small component side ground plane through 16 feed-throughs.

As expected, the aluminum PC board's significantly higher specific heat results in nearly an order of magnitude increase in thermal capacitance. Surprisingly the four layer 0.062 board's thermal resistance is nearly as low as the aluminum board's, indicating good heat distribution through the inner planes. Note that although the Vcc plane is unconnected, it does help distribute the heat across the board. Conduction or forced air cooling is necessary to fully exploit the aluminum board's capability.

Summary

A method for accurately modeling the thermal behavior of a surface mounted IC has been presented. The model relies on measured data, insuring excellent correlation to the physical system. Typical thermal behavior of nine different packages and five different PC boards were also presented, indicating relative thermal performance differences. Optimum thermal system design is achievable using the techniques and data presented.

References

1. Thermal Clad insulated metal substrates, The Bergquist Company, 5300 Edina Industrial Blvd., Minneapolis, MN 55439, 612-835-2322
2. R. Tummala, E. Rymaszewski, "Microelectronics Packaging Handbook", Van Nostrand Reinhold, 1989, pp173-179

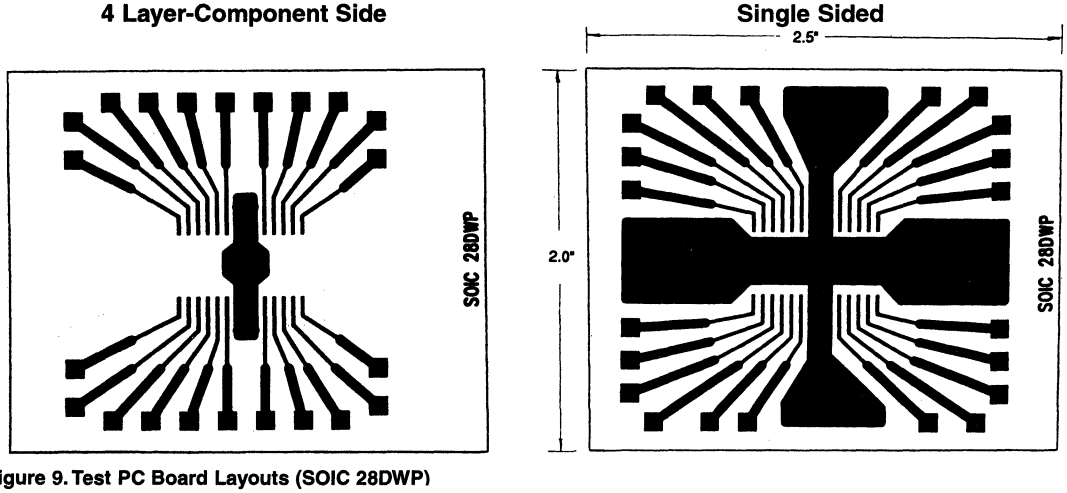
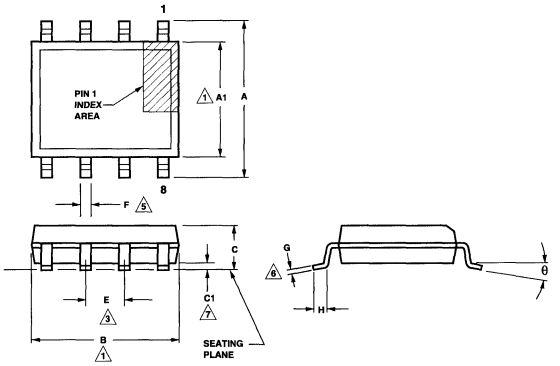


Figure 9. Test PC Board Layouts (SOIC 28DWP)

D: 8-Pin SOIC

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.228	.244	5.80	6.20
A1	.150	.158	3.80	4.00
B	.189	.196	4.80	4.98
C	.053	.069	1.35	1.75
C1	.004	.009	0.10	0.23
E	.050 BSC		1.27 BSC	
F	.014	.019	0.35	0.48
G	.007	.010	0.19	0.25
H	.016	.035	0.41	0.89
θ	0°	8°	0°	8°

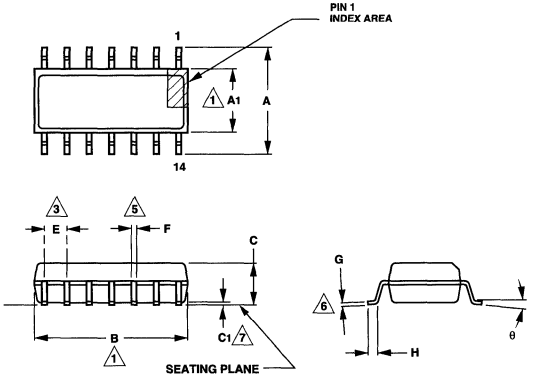


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

D: 14-Pin SOIC

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.228	.244	5.80	6.20
A1	.150	.158	3.80	4.00
B	.336	.344	8.55	8.75
C	.053	.069	1.35	1.75
C1	.004	.009	0.10	0.22
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.007	.010	0.19	0.25
H	.016	.035	0.41	0.89
θ	0°	8°	0°	8°



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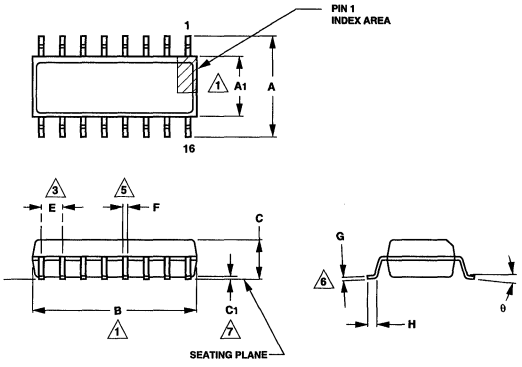
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

D: 16-Pin SOIC

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.228	.244	5.80	6.20
A1	.150	.158	3.80	4.00
B	.386	.393	9.80	9.98
C	.053	.069	1.35	1.75
C1	.004	.009	0.10	0.22
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.007	.010	0.19	0.25
H	.016	.035	0.41	0.89
θ	0°	8°	0°	8°

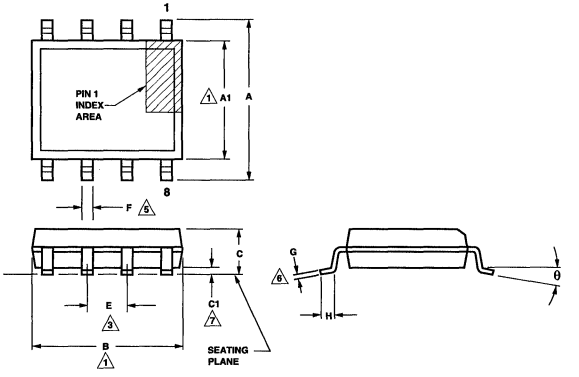


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

DP: 8-Pin SOIC

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.228	.244	5.80	6.20
A1	.150	.158	3.80	4.00
B	.189	.196	4.80	4.98
C	.053	.069	1.35	1.75
C1	.004	.009	0.10	0.23
E	.050 BSC		1.27 BSC	
F	.014	.019	0.35	0.48
G	.007	.010	0.19	0.25
H	.016	.035	0.41	0.89
θ	0°	8°	0°	8°

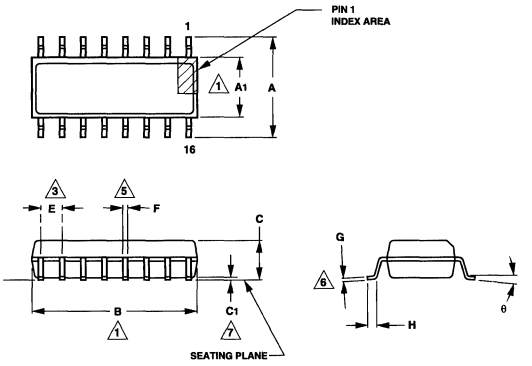


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

DP: 16-Pin SOIC

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.228	.244	5.80	6.20
A1	.150	.158	3.80	4.00
B	.386	.393	9.80	9.98
C	.053	.069	1.35	1.75
C1	.004	.009	0.10	0.22
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.007	.010	0.19	0.25
H	.016	.035	0.41	0.89
θ	0°	8°	0°	8°

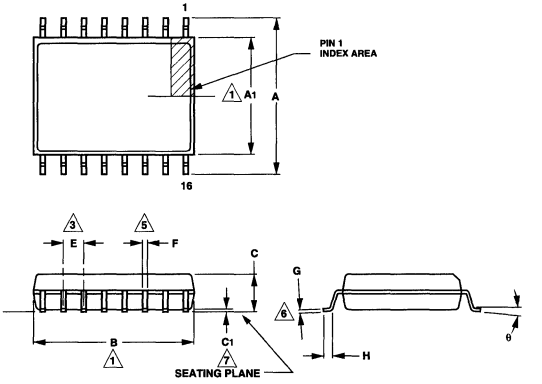


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

DW: 16-Pin SOIC

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.394	.419	10.00	10.64
A1	.292	.299	7.42	7.59
B	.403	.413	10.24	10.49
C	.097	.104	2.46	2.64
C1	.004	.011	0.10	0.28
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.009	.012	0.23	0.30
H	.018	.035	0.46	0.89
θ	0°	8°	0°	8°

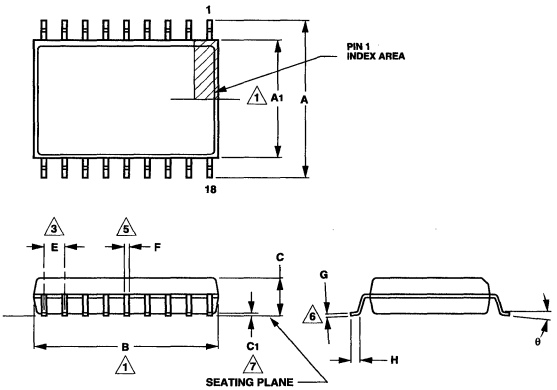


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

DW: 18-Pin SOIC

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.394	.419	10.00	10.64
A1	.292	.299	7.42	7.59
B	.453	.462	11.51	11.73
C	.097	.104	2.46	2.64
C1	.004	.011	0.10	0.28
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.009	.012	0.23	0.30
H	.018	.035	0.46	0.89
θ	0°	8°	0°	8°

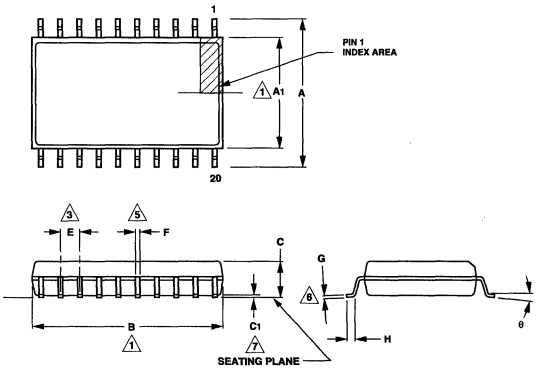


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

DW: 20-Pin SOIC

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.394	.419	10.00	10.64
A1	.292	.299	7.42	7.59
B	.504	.511	12.80	12.98
C	.097	.104	2.46	2.64
C1	.004	.011	0.10	0.28
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.009	.012	0.23	0.30
H	.018	.035	0.46	0.89
θ	0°	8°	0°	8°

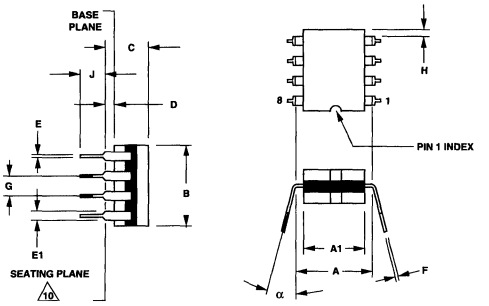


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

J: 8-Pin Ceramic DIP, Glass Seal

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	—	0.405	—	10.29	4
C	—	0.200	—	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	—	0.13	—	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	

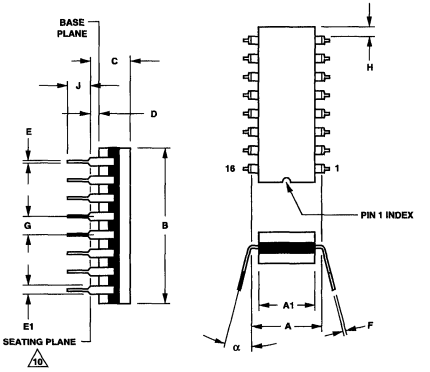


NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION "E1" MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 4, 5 AND 8 ONLY.
3. DIMENSION "D" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF–CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 4, 5 AND 8).
7. DIMENSION "A" SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0°$.
8. THE MAXIMUM LIMITS OF DIMENSIONS "E" AND "F" SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
10. THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.

J: 16-Pin Ceramic DIP, Glass Seal

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	—	0.840	—	21.34	4
C	—	0.200	—	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	—	0.13	—	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	



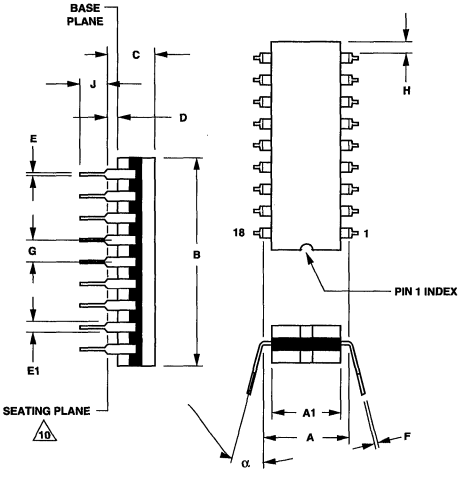
NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION "E1" MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 8, 9 AND 16 ONLY.
3. DIMENSION "D" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF–CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 8, 9 AND 16).
7. DIMENSION "A" SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0°$.
8. THE MAXIMUM LIMITS OF DIMENSIONS "E" AND "F" SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

10 THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.

J: 18-Pin Ceramic DIP, Glass Seal

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	—	0.960	—	24.38	4
C	—	0.200	—	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	—	0.13	—	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	

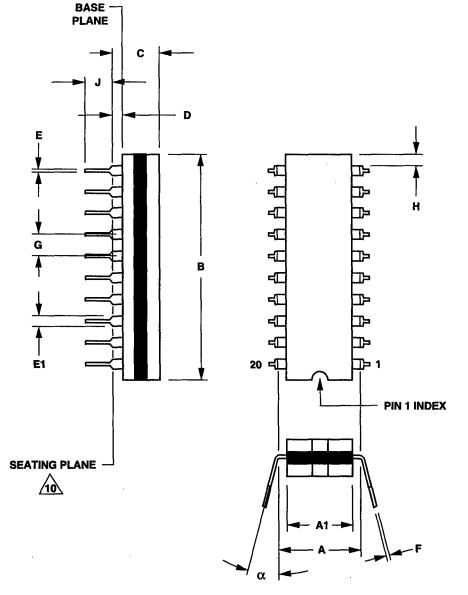


NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION "E1" MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 9, 10 AND 18 ONLY.
3. DIMENSION "D" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF–CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 9, 10 AND 18).
7. DIMENSION "A" SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0°$.
8. THE MAXIMUM LIMITS OF DIMENSIONS "E" AND "F" SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
10. THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.

J: 20-Pin Ceramic DIP, Glass Seal

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	—	1.060	—	26.92	4
C	—	0.200	—	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	—	0.13	—	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	

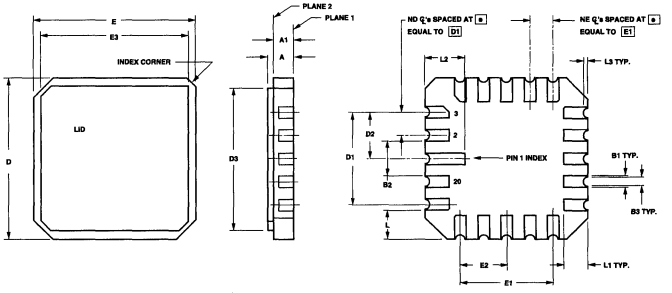


NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION "E1" MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 10, 11 AND 20 ONLY.
3. DIMENSION "D" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF–CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 10, 11 AND 20).
7. DIMENSION "A" SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0°$.
8. THE MAXIMUM LIMITS OF DIMENSIONS "E" AND "F" SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY,
10. THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.

L: 20-Pin Ceramic LCC

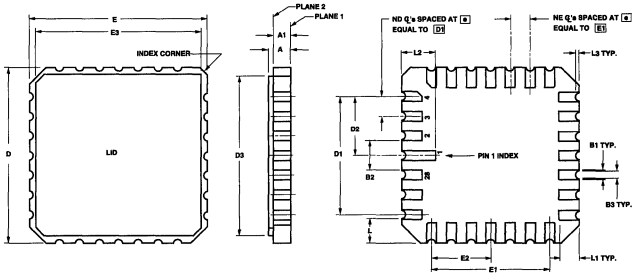
DIMENSIONS					
	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	NOTES
A	.060	.100	1.52	2.54	6
A1	.050	.088	1.27	2.24	
B1	.022	.028	0.56	0.71	1, 3
B2	.072 REF.		1.83 REF.		
B3	.006	.022	0.15	0.56	8
D/E	.342	.358	8.69	9.09	
D1/E1	.200 BSC		5.08 BSC		
D2/E2	.100 BSC		2.54 BSC		
D3/E3	–	.358	–	9.09	4
L	.045	.055	1.14	1.40	
L1	.045	.055	1.14	1.40	
L2	.075	.095	1.90	2.41	5
L3	.003	.015	0.08	0.38	
N	20		20		2
ND/NE	5		5		2
e	.050 BSC		1.27 BSC		10



NOTES:
1. A MINIMUM CLEARANCE OF 0.015 INCH (0.38 mm) SHALL BE MAINTAINED BETWEEN ADJACENT TERMINALS.
2. 'N' IS THE MAXIMUM QUANTITY OF TERMINAL POSITIONS. 'ND' AND 'NE' ARE THE NUMBERS OF TERMINALS ALONG THE SIDES OF LENGTH 'D' AND 'E' RESPECTIVELY.
3. ELECTRICAL CONNECTION TERMINALS ARE REQUIRED ON PLANE 1 AND OPTIONAL ON PLANE 2. HOWEVER, IF PLANE 2 HAS SUCH TERMINALS THEY SHALL BE ELECTRICALLY CONNECTED TO *OPPOSING TERMINALS ON PLANE 1.*
4. A MINIMUM CLEARANCE OR 0.015 INCH (0.38 mm) SHALL BE MAINTAINED BETWEEN A METAL LID AND OTHER METAL FEATURES (E.G., PLANE 2 TERMINALS, METALLIZED CASTELLATIONS, ETC.) THE LID SHALL NOT EXTEND BEYOND THE EDGES OF THE BODY.
5. THE INDEX FEATURE FOR NUMBER 1 TERMINAL IDENTIFICATION, OPTIONAL ORIENTATION OR HANDLING PURPOSES SHALL BE WITHIN THE AREA DEFINED BY DIMENSIONS 'B2' AND 'L2' ON PLANE 1.
6. DIMENSION 'A' CONTROLS THE OVERALL PACKAGE THICKNESS.
7. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
8. CASTELLATIONS ARE REQUIRED ON BOTTOM TWO LAYERS. CASTELLATIONS IN THE TOP LAYER ARE OPTIONAL.
9. WHEN SOLDER DIP LEAD FINISH APPLIES, SOLDER BUMP HEIGHT SHALL NOT EXCEED 0.007 INCHES AND SOLDER BUMP COPLANARITY SHALL NOT EXCEED 0.006 INCHES.
10. THE BASIC TERMINAL SPACING IS 0.050 INCHES BETWEEN CENTERLINES. EACH TERMINAL CENTERLINE SHALL BE LOCATED WITHIN ±0.004 INCHES OF ITS EXACT TRUE POSITION.

L: 28-Pin Ceramic LCC

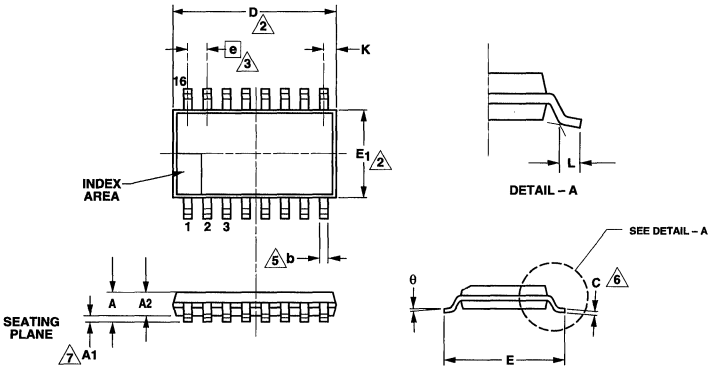
DIMENSIONS					
	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	NOTES
A	.060	.100	1.52	2.54	6
A1	.050	.088	1.27	2.24	
B1	.022	.028	0.56	0.71	1, 3
B2	.072 REF.		1.83 REF.		
B3	.006	.022	0.15	0.56	8
D/E	.442	.460	11.23	11.68	
D1/E1	.300 BSC		7.62 BSC		
D2/E2	.150 BSC		3.81 BSC		
D3/E3	–	.460	–	11.68	4
L	.045	.055	1.14	1.40	
L1	.045	.055	1.14	1.40	
L2	.075	.095	1.90	2.41	5
L3	.003	.015	0.08	0.38	
N	28		28		2
ND/NE	7		7		2
e	.050 BSC		1.27 BSC		10



NOTES:
1. A MINIMUM CLEARANCE OF 0.015 INCH (0.38 mm) SHALL BE MAINTAINED BETWEEN ADJACENT TERMINALS.
2. 'N' IS THE MAXIMUM QUANTITY OF TERMINAL POSITIONS. 'ND' AND 'NE' ARE THE NUMBERS OF TERMINALS ALONG THE SIDES OF LENGTH 'D' AND 'E' RESPECTIVELY.
3. ELECTRICAL CONNECTION TERMINALS ARE REQUIRED ON PLANE 1 AND OPTIONAL ON PLANE 2. HOWEVER, IF PLANE 2 HAS SUCH TERMINALS THEY SHALL BE ELECTRICALLY CONNECTED TO OPPOSING TERMINALS ON PLANE 1.
4. A MINIMUM CLEARANCE OR 0.015 INCH (0.38 mm) SHALL BE MAINTAINED BETWEEN A METAL LID AND OTHER METAL FEATURES (E.G., PLANE 2 TERMINALS, METALLIZED CASTELLATIONS, ETC.) THE LID SHALL NOT EXTEND BEYOND THE EDGES OF THE BODY.
5. THE INDEX FEATURE FOR NUMBER 1 TERMINAL IDENTIFICATION, OPTIONAL ORIENTATION OR HANDLING PURPOSES SHALL BE WITHIN THE AREA DEFINED BY DIMENSIONS 'B2' AND 'L2' ON PLANE 1.
6. DIMENSION 'A' CONTROLS THE OVERALL PACKAGE THICKNESS.
7. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
8. CASTELLATIONS ARE REQUIRED ON BOTTOM TWO LAYERS. CASTELLATIONS IN THE TOP LAYER ARE OPTIONAL.
9. WHEN SOLDER DIP LEAD FINISH APPLIES, SOLDER BUMP HEIGHT SHALL NOT EXCEED 0.007 INCHES AND SOLDER BUMP COPLANARITY SHALL NOT EXCEED 0.006 INCHES.
10. THE BASIC TERMINAL SPACING IS 0.050 INCHES BETWEEN CENTERLINES. EACH TERMINAL CENTERLINE SHALL BELOCATED WITHIN ±0.004 INCHES OF ITS EXACT TRUE POSITION.

M: 16-Pin SSOP

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.053	.069	1.35	1.75
A1	.004	.010	.10	.25
A2	–	.059	–	1.50
b	.008	.012	.20	.30
C	.007	.010	.18	.25
D	.189	.197	4.80	5.00
E	.228	.244	5.79	6.20
E_1	.150	.157	3.81	3.99
e	.025 BSC		.635 BSC	
K	.009 REF		.23 REF	
L	.016	.050	.41	1.27
θ	0°	8°	0°	8°

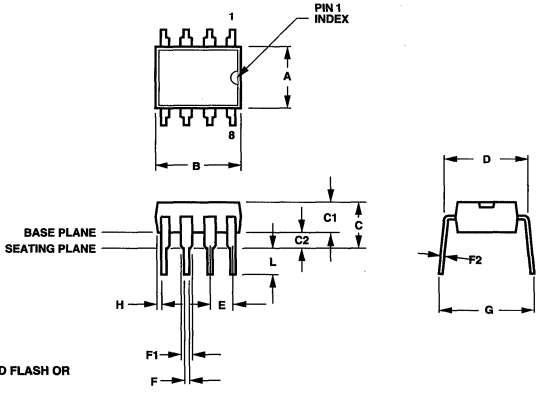


NOTES:

1. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
2. 'D' AND 'E_1' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
3. THE BASIC LEAD SPACING IS 0.025 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'b' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

N: 8-Pin P-DIP

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.320	.400	9.40	10.16	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	

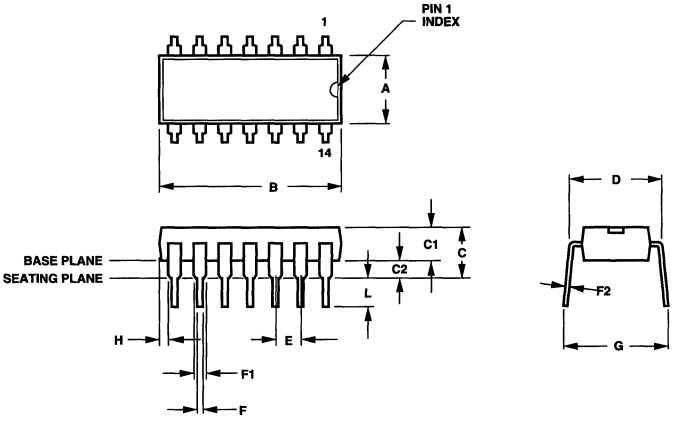


NOTES:

1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

N: 14-Pin P-DIP

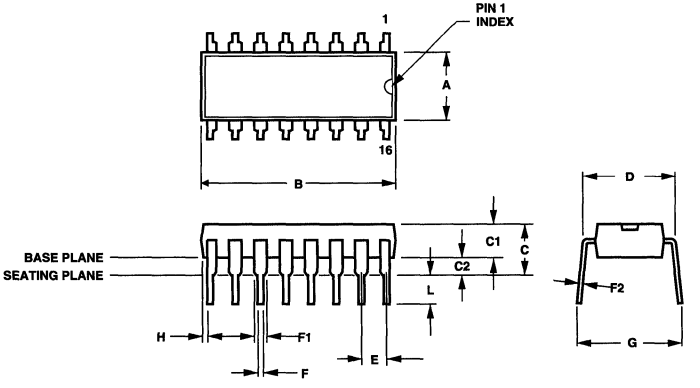
DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.745	.775	18.92	19.68	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



NOTES:
1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

N: 16-Pin P-DIP

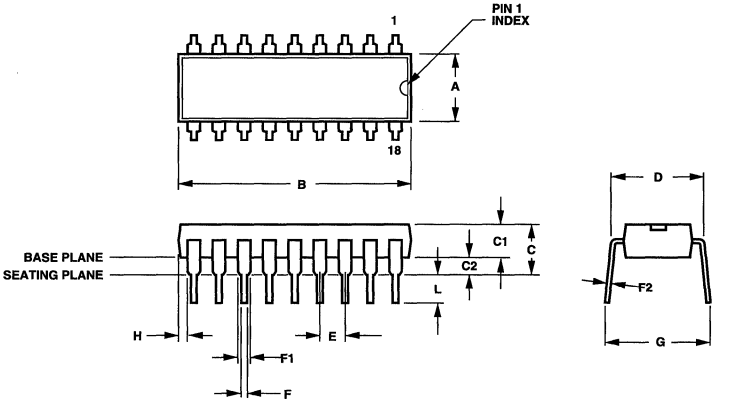
DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.745	.775	18.92	19.68	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



NOTES:
1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

N: 18-Pin P-DIP

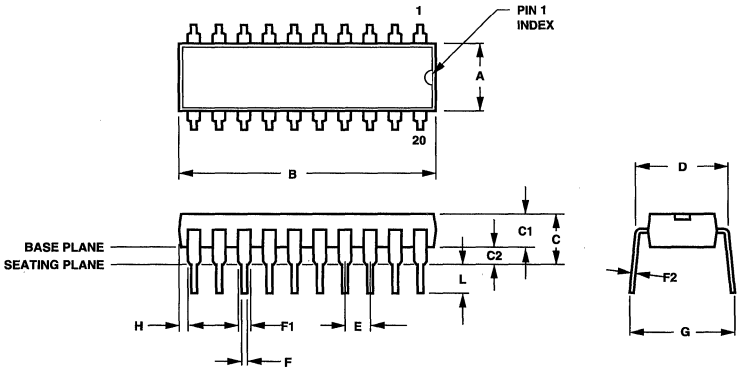
DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.890	.920	22.61	23.39	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



NOTES:
1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

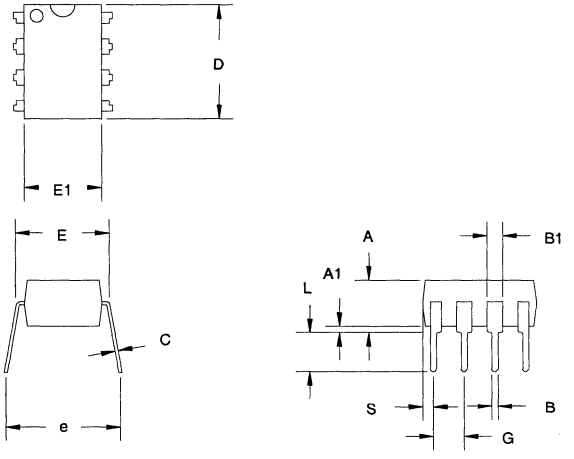
N: 20-Pin P-DIP

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	1.010	1.030	25.65	26.16	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



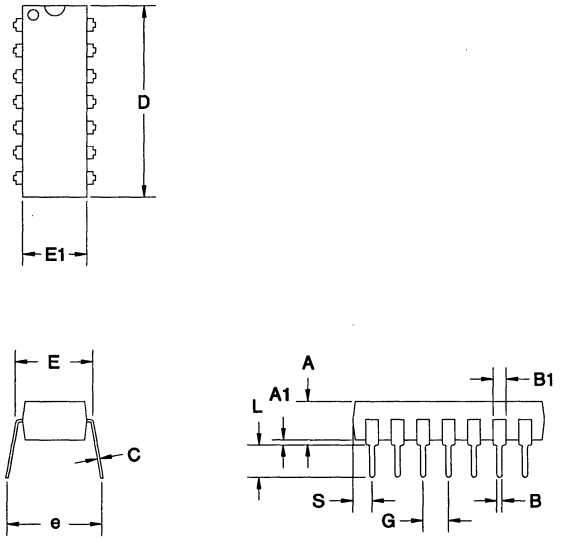
NOTES:
1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

PN: 8-Pin P-DIP (0.300")



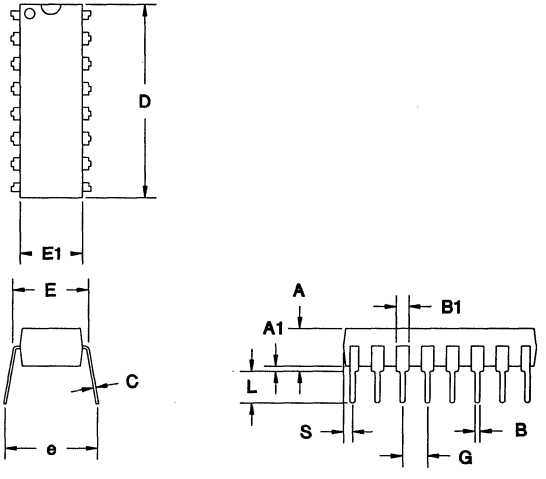
Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.180	4.06	4.57
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.055	0.065	1.40	1.65
C	0.008	0.013	0.20	0.33
D	0.350	0.380	8.89	9.65
E	0.300	0.325	7.62	8.26
E1	0.230	0.280	5.84	7.11
e	0.300	0.370	7.62	9.40
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.020	0.040	0.51	1.02

PN: 14-Pin P-DIP (0.300")



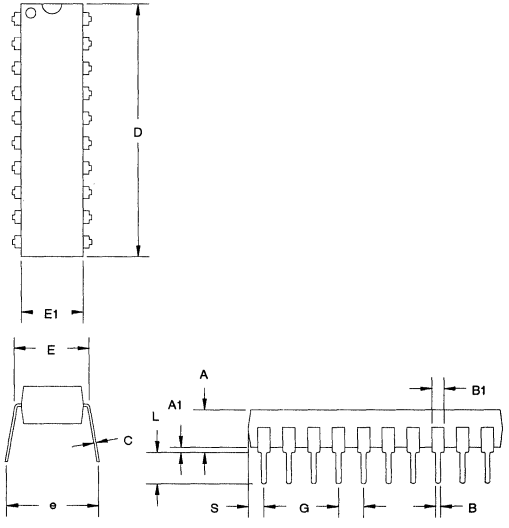
Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.180	4.06	4.57
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.055	0.065	1.40	1.65
C	0.008	0.013	0.20	0.33
D	0.740	0.770	18.80	19.56
E	0.300	0.325	7.62	8.26
E1	0.230	0.280	5.84	7.11
e	0.300	0.370	7.62	9.40
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.070	0.090	1.78	2.29

PN: 16-Pin P-DIP (0.300")



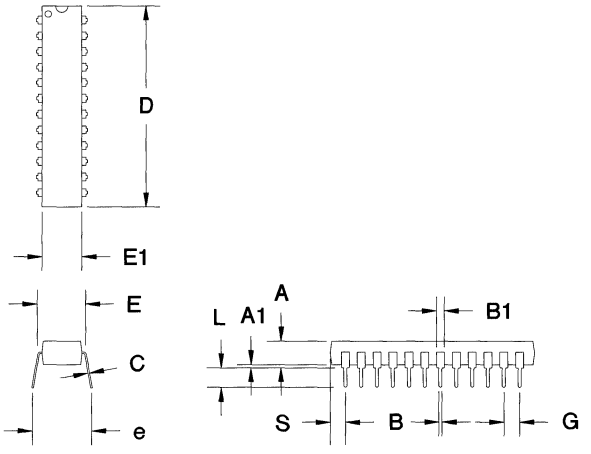
Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.180	4.06	4.57
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.055	0.065	1.40	1.65
C	0.008	0.013	0.20	0.33
D	0.740	0.770	18.80	19.56
E	0.300	0.325	7.62	8.26
E1	0.230	0.280	5.84	7.11
e	0.300	0.370	7.62	9.40
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.020	0.040	0.51	1.02

PN: 20-Pin P-DIP (0.300")



Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.180	4.06	4.57
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.055	0.065	1.40	1.65
C	0.008	0.013	0.20	0.33
D	1.010	1.060	25.65	26.92
E	0.300	0.325	7.62	8.26
E1	0.230	0.280	5.84	7.11
e	0.300	0.370	7.62	9.40
G	0.090	0.110	2.29	2.79
L	0.115	0.135	2.92	3.43
S	0.055	0.080	1.40	2.03

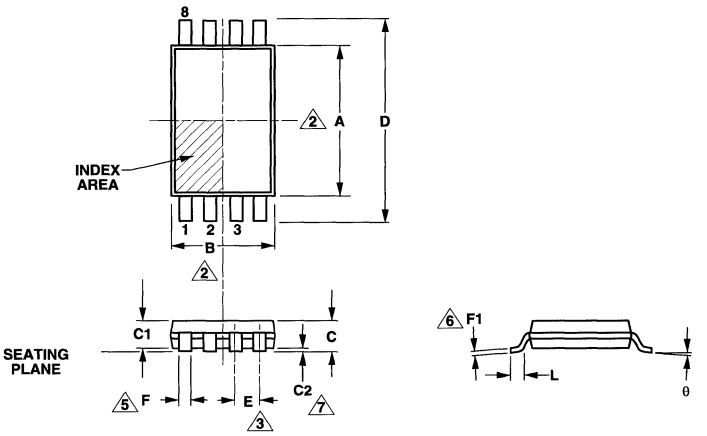
PN: 24-Pin P-DIP (0.300")



Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.180	4.06	4.57
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.045	0.055	1.14	1.40
C	0.008	0.013	0.20	0.33
D	1.240	1.280	31.50	32.51
E	0.300	0.325	7.62	8.26
E1	0.250	0.300	6.35	7.62
e	0.300	0.370	7.62	9.40
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.070	0.090	1.78	2.29

PW: 8-Pin TSSOP

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.3	4.5	0.170	0.177
B	2.9	3.1	0.114	0.122
C	–	1.10	–	0.043
C1	0.90 REF.		0.035 REF.	
C2	0.05	0.15	0.002	0.006
D	6.4 BSC		0.252 BSC	
E	0.65 BSC		0.0256 BSC	
F	0.18	0.30	0.007	0.012
F1	0.09	0.18	0.004	0.007
L	0.50	0.70	0.020	0.028
θ	0°	7°	0°	7°

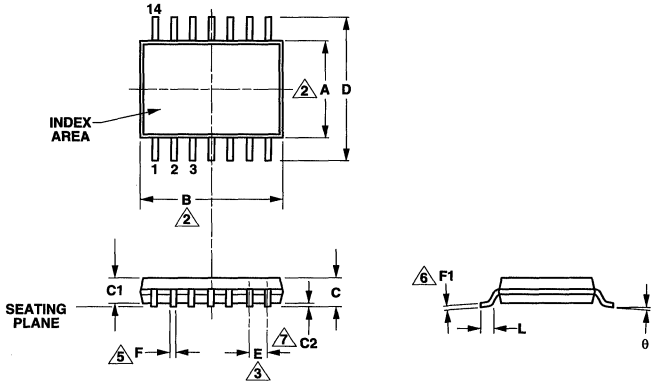


NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
3. THE BASIC LEAD SPACING IS 0.65mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN +0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. 'C2' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

PW: 14-Pin TSSOP

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.3	4.5	0.170	0.177
B	4.9	5.1	0.193	0.200
C	–	1.10	–	0.043
C1	0.90 REF.		0.035 REF.	
C2	0.05	0.15	0.002	0.006
D	6.4 BSC		0.252 BSC	
E	0.65 BSC		0.0256 BSC	
F	0.18	0.30	0.007	0.012
F1	0.09	0.18	0.004	0.007
L	0.50	0.70	0.020	0.028
θ	0°	7°	0°	7°

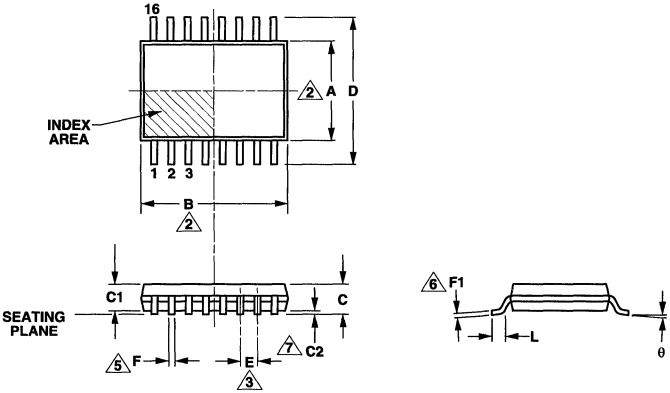


NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
3. THE BASIC LEAD SPACING IS 0.65mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. 'C2' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

PW: 16-Pin TSSOP

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.3	4.5	0.170	0.177
B	4.9	5.1	0.193	0.200
C	–	1.10	–	0.043
C1	0.90 REF.		0.035 REF.	
C2	0.05	0.15	0.002	0.006
D	6.4 BSC		0.252 BSC	
E	0.65 BSC		0.0256 BSC	
F	0.18	0.30	0.007	0.012
F1	0.09	0.18	0.004	0.007
L	0.50	0.70	0.020	0.028
θ	0°	7°	0°	7°

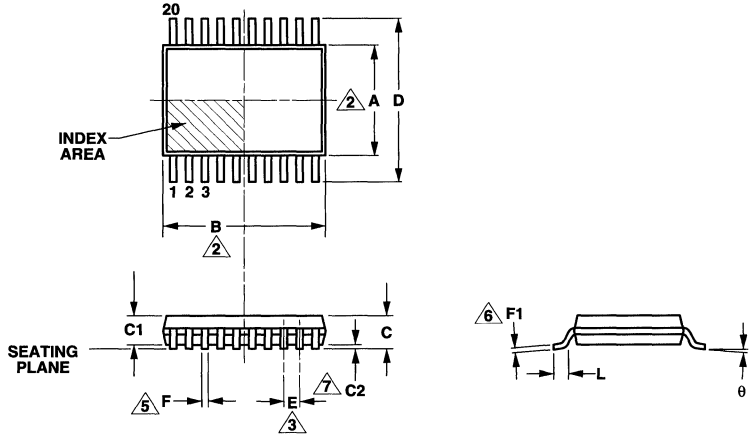


NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
3. THE BASIC LEAD SPACING IS 0.65mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN +0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. 'C2' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

PW: 20-Pin TSSOP

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.48	.169	.176
B	6.40	6.60	.252	.260
C	–	1.10	–	.043
C1	.90 REF.		.0354 REF.	
C2	.05	.15	.002	.006
D	6.25	6.50	.246	.256
E	.65 BSC		.0256 BSC	
F	.18	.30	.007	.012
F1	.09	.18	.003	.007
L	.50	.70	.020	.028
θ	0°	8°	0°	8°

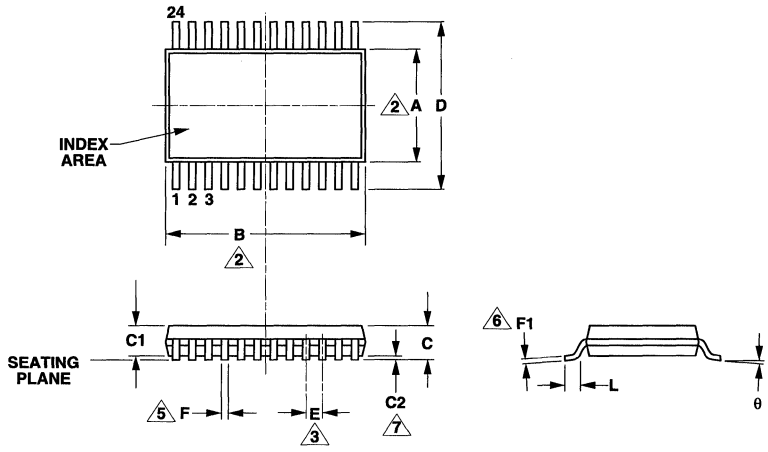


NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
3. THE BASIC LEAD SPACING IS 0.65mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.08mm.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. 'C2' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

PW: 24-Pin TSSOP

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.48	.169	.176
B	7.70	7.90	.303	.311
C	–	1.10	–	.043
C1	.90 REF.		.0354 REF.	
C2	.05	.15	.002	.006
D	6.25	6.50	.246	.256
E	.65 BSC		.0256 BSC	
F	.18	.30	.007	.012
F1	.09	.18	.003	.007
L	.50	.70	.020	.028
θ	0°	8°	0°	8°

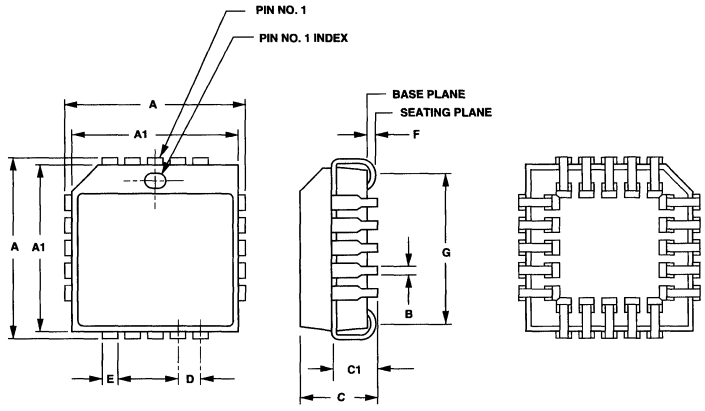


NOTES:

1. CONTROLLING DIMENSION : MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
3. THE BASIC LEAD SPACING IS 0.65 MM BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.08mm DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. 'C2' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

Q: 20-Pin Quad PLCC

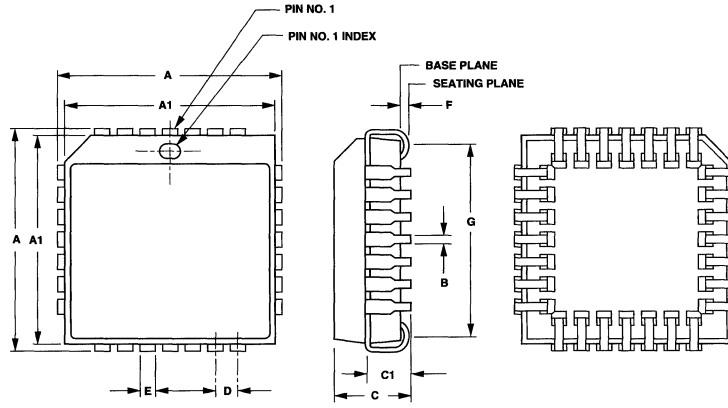
	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.385	.395	9.78	10.03	
A1	.350	.356	8.89	9.04	1
B	.013	.021	0.33	0.53	
C	.170	.180	4.32	4.57	
C1	.100	.110	2.54	2.79	
D	.050 BSC		1.27 BSC		2
E	.026	.032	0.66	0.81	
F	.020	–	0.51	–	3, 4
G	.290	.330	7.37	8.38	



NOTES:
1. 'A1' DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
3. 'F' IS MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
5. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

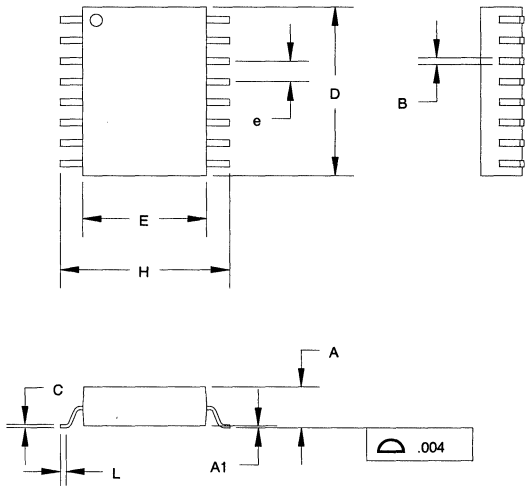
Q: 28-Pin Quad PLCC

	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.485	.495	12.32	12.57	
A1	.450	.456	11.43	11.58	1
B	.013	.021	0.33	0.53	
C	.170	.180	4.32	4.57	
C1	.100	.110	2.54	2.79	
D	.050 BSC		1.27 BSC		2
E	.026	.032	0.66	0.81	
F	.020	–	0.51	–	3, 4
G	.390	.430	9.91	10.92	



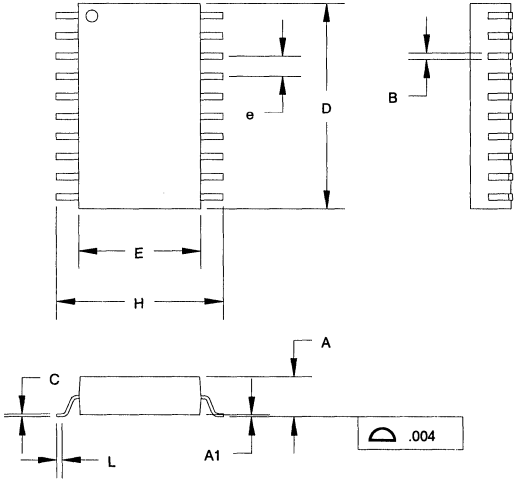
NOTES:
1. 'A1' DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
3. 'F' IS MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
5. CONTROLLING DIMENSION : INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

S: 16-Pin SOIC (0.300")



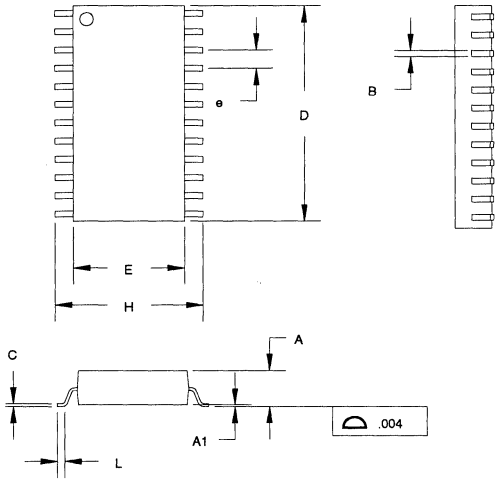
Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.095	0.105	2.41	2.67
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.008	0.013	0.20	0.33
D	0.400	0.415	10.16	10.54
E	0.290	0.305	7.37	7.75
e	0.045	0.055	1.14	1.40
H	0.395	0.415	10.03	10.54
L	0.020	0.040	0.51	1.02

S: 20-Pin SOIC (0.300")



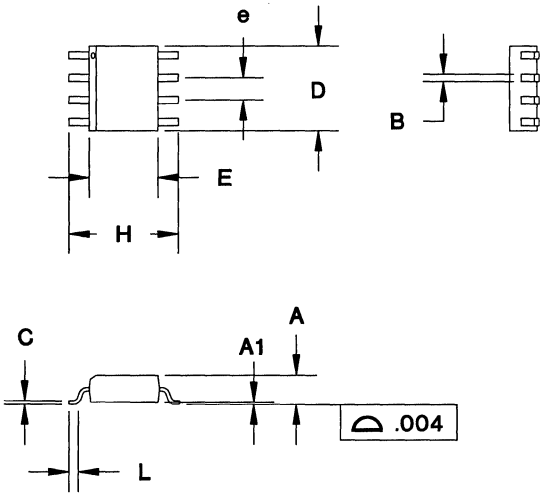
Dimension	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	2.41	2.67	0.095	0.105
A1	0.10	0.30	0.004	0.012
B	0.33	0.51	0.013	0.020
C	0.20	0.33	0.008	0.013
D	12.70	13.08	0.500	0.515
E	7.37	7.75	0.290	0.305
e	1.14	1.40	0.045	0.055
H	10.03	10.54	0.395	0.415
L	0.51	1.02	0.020	0.040

S: 24-Pin SOIC (0.300")



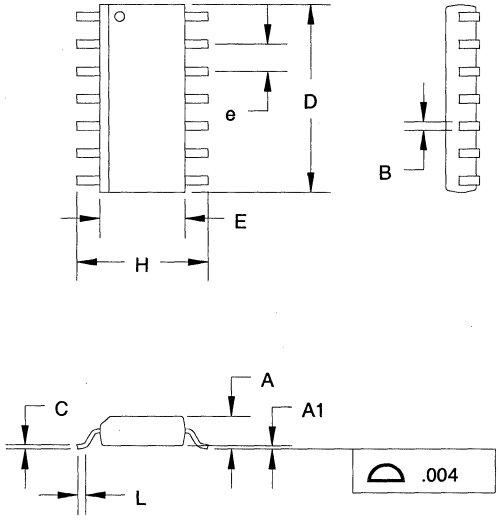
Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.095	0.105	2.41	2.67
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.008	0.013	0.20	0.33
D	0.600	0.615	15.24	15.62
E	0.290	0.305	7.37	7.75
e	0.045	0.055	1.14	1.40
H	0.395	0.415	10.03	10.54
L	0.020	0.040	0.51	1.02

SN: 8-Pin SOIC (0.150")



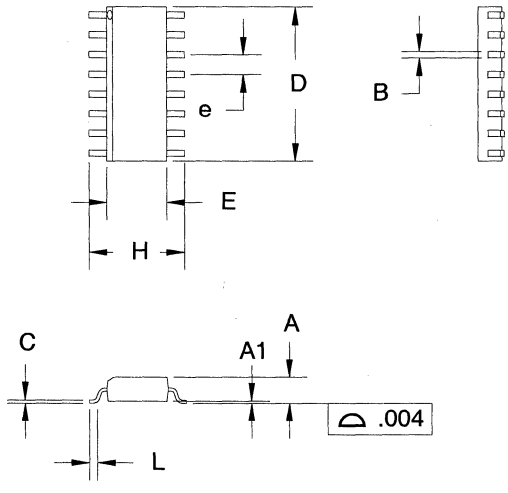
Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.060	0.070	1.52	1.78
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.18	0.25
D	0.185	0.200	4.70	5.08
E	0.150	0.160	3.81	4.06
e	0.045	0.055	1.14	1.40
H	0.225	0.245	5.72	6.22
L	0.015	0.035	0.38	0.89

SN: 14-Pin SOIC (0.150")



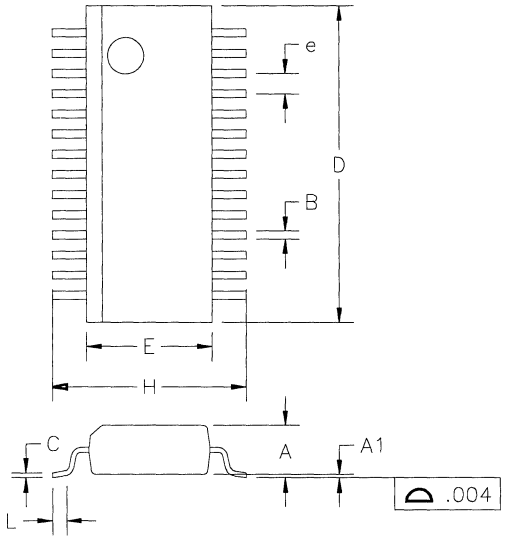
Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.060	0.070	1.52	1.78
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.18	0.25
D	0.335	0.350	8.51	8.89
E	0.150	0.160	3.81	4.06
e	0.045	0.055	1.14	1.40
H	0.225	0.245	5.72	6.22
L	0.015	0.035	0.38	0.89

SN: 16-Pin SOIC (0.150")



Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.060	0.070	1.52	1.78
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.18	0.25
D	0.385	0.400	9.78	10.16
E	0.150	0.160	3.81	4.06
e	0.045	0.055	1.14	1.40
H	0.225	0.245	5.72	6.22
L	0.015	0.035	0.38	0.89

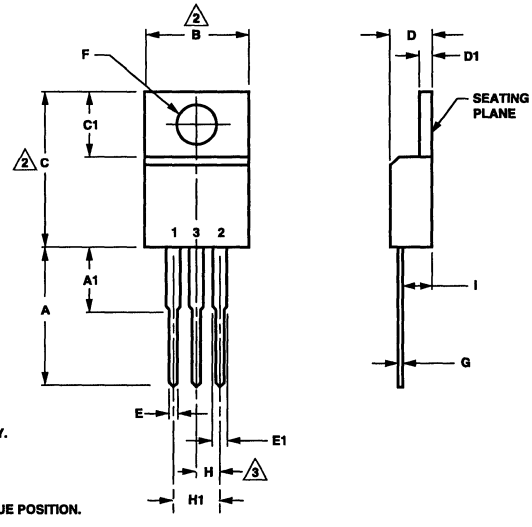
SS: 28-Pin SSOP/QSOP (0.150")



Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.008	0.012	0.20	0.30
C	0.007	0.010	0.19	0.25
D	0.386	0.393	9.80	9.98
E	0.150	0.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	0.228	0.244	5.79	6.20
L	0.016	0.050	0.40	1.27

T: 3-Pin TO-220

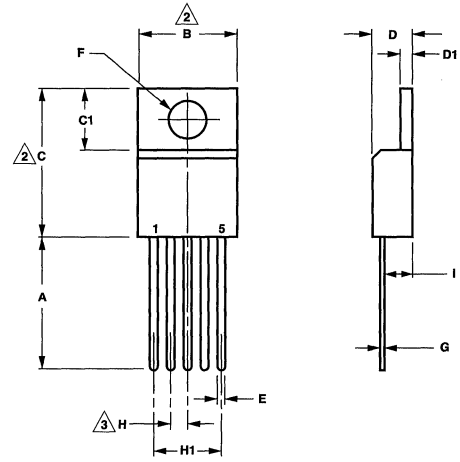
DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.500	.562	12.70	14.27
A1	–	.250	–	6.35
B	.380	.420	9.66	10.66
C	.560	.625	14.23	15.87
C1	.230	.270	5.85	6.85
D	.140	.190	3.56	4.82
D1	.045	.055	1.14	1.39
E	.020	.045	0.51	1.14
E1	.045	.070	1.14	1.77
F	.139	.161	3.53	4.09
G	.014	.022	0.36	0.56
H	.090	.110	2.29	2.79
H1	.190	.210	4.83	5.33
I	.080	.115	2.04	2.92



NOTES:
1. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
2. 'B' AND 'C' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
3. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.

T: 5-Pin TO-220

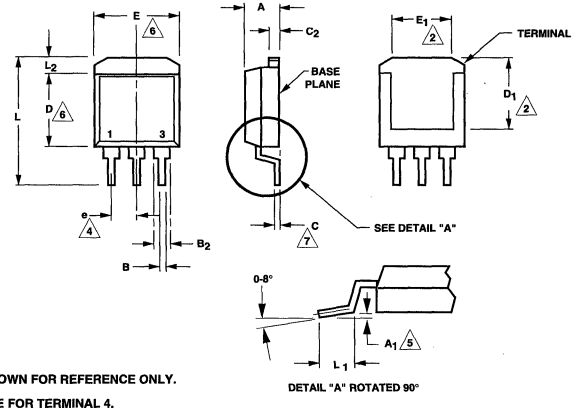
DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.500	.580	12.70	14.73
B	.380	.420	9.65	10.67
C	.560	.650	14.22	16.51
C1	.230	.270	5.84	6.86
D	.140	.190	3.56	4.83
D1	.045	.055	1.14	1.40
E	.020	.045	0.51	1.14
F	.139	.161	3.53	4.09
G	.014	.022	0.36	0.56
H	.057	.077	1.45	1.96
H1	.258	.278	6.55	7.06
I	.080	.115	2.03	2.92



NOTES:
1. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
2. 'B' AND 'C' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
3. THE BASIC LEAD SPACING IS 0.067 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.

TD: 3-Pin TO-263

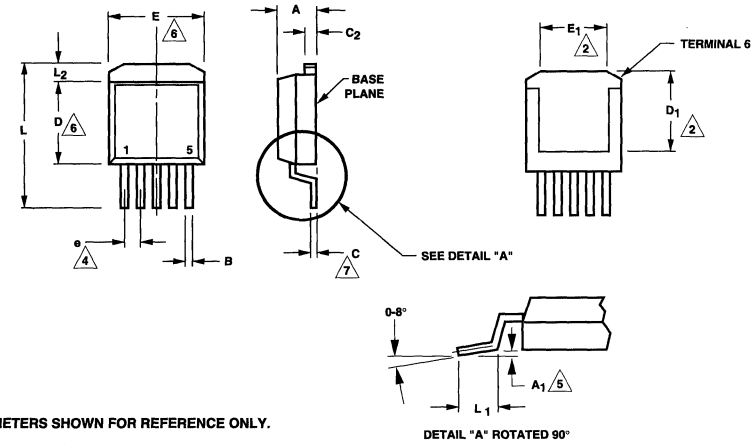
DIMENSIONS						
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.170	.175	.180	4.31	4.44	4.57
A_1	.000	—	.010	0.00	—	0.25
B	.020	.032	.039	0.51	0.81	0.99
B_2	.045	.050	.055	1.14	1.27	1.40
C	.018	—	.029	0.46	—	0.74
C_2	.045	.050	.055	1.14	1.27	1.40
D	.326	.331	.336	8.28	8.41	8.53
D_1	.305 REF.			7.75 REF.		
E	.396	.401	.405	10.05	10.18	10.31
E_1	.256 REF.			6.50 REF.		
e	.100 BSC			2.54 BSC		
L	.580	.600	.620	14.73	15.24	15.75
L_1	.090	.100	.110	2.29	2.54	2.79
L_2	.055	.061	.066	1.40	1.54	1.68



NOTES:
1. CONTROLLING DIMENSION : INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
2. D_1 AND E_1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSION E AND ZONE L_2.
4. THE BASIC LEAD SPACING IS 0.100 INCHES BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 INCHES OF ITS EXACT TRUE POSITION.
5. A_1 IS MEASURED FROM THE LEAD TIP TO THE BASE PLANE.
6. D AND E DO NOT INCLUDE MOLD FLASH ON PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
7. LEAD TIPS SHALL BE COPLANAR WITHIN 0.004 INCHES.

TD: 5-Pin TO-263

	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.170	.175	.180	4.31	4.44	4.57
A_1	.000	—	.010	0.00	—	0.25
B	.020	.032	.039	0.51	0.81	0.99
C	.018	—	.029	0.46	—	0.74
C_2	.045	.050	.055	1.14	1.27	1.40
D	.326	.331	.336	8.28	8.41	8.53
D_1	.305 REF.			7.75 REF.		
E	.396	.401	.405	10.05	10.18	10.31
E_1	.256 REF.			6.50 REF.		
e	.067 BSC			1.70 BSC		
L	.580	.600	.620	14.73	15.24	15.75
L_1	.090	.100	.110	2.29	2.54	2.79
L_2	.055	.061	.066	1.40	1.54	1.68

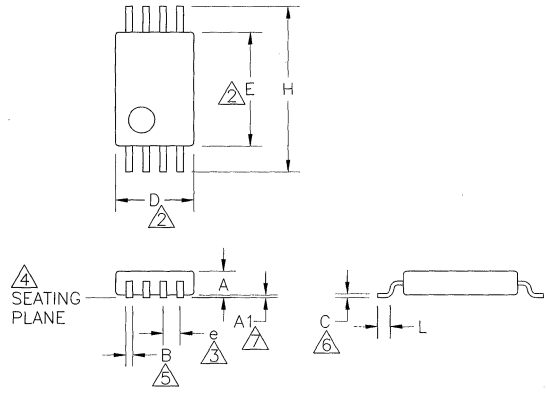


NOTES:

1. CONTROLLING DIMENSION : INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
2. D_1 AND E_1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 6.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSION E AND ZONE L_2.
4. THE BASIC LEAD SPACING IS 0.067 INCHES BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 INCHES OF ITS EXACT TRUE POSITION.
5. A_1 IS MEASURED FROM THE LEAD TIP TO THE BASE PLANE.
6. D AND E DO NOT INCLUDE MOLD FLASH ON PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
7. LEAD TIPS SHALL BE COPLANAR WITHIN 0.004 INCHES.

TS: 8-Pin TSSOP

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
B	0.007	0.012	0.18	0.30
C	0.004	0.007	0.09	0.18
D	0.114	0.122	2.90	3.10
E	0.169	0.176	4.30	4.48
e	0.0256BSC		0.65BSC	
H	0.246	0.256	6.25	6.50
L	0.020	0.028	0.50	0.70



Notes:

1. Controlling dimension: millimeters. Inches shown for reference only.
2. 'D' and 'E' do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side
3. Each lead centerline shall be located within ±0.10mm of its exact true position.
4. Leads shall be coplanar within 0.08mm at the seating plane.
5. Dimension 'B' does not include dambar protrusion. The dambar protrusion(s) shall not cause the lead width to exceed 'B' maximum by more than 0.08mm.
6. Dimension applies to the flat section of the lead between 0.10mm and 0.25mm from the lead tip.
7. 'A1' is defined as the distance from the seating plane to the lowest point of the package body (base plane).

TEXAS INSTRUMENTS

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