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Data Book

Volume 3

2000

Analog and Mixed Signal

Power Management Products

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Volume 3

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INTRODUCTION

The Texas Instruments 1999 Power Management Products Data Book Set showcases TI's broad portfolio of analog components for power supply designs. Featured in this set are most of the components previously found in the 1996 Power Supply Circuits Data Book, the new and exciting power management products introduced since then, and other components useful for power supply designs.

The set consists of three product area specific volumes:

- Power Management Products, Volume 1:
  - Linear voltage regulators
  - Shunt regulators
  - Voltage references
  - Precision virtual grounds
- Power Management Products, Volume 2:
  - Processor power supply controllers (DSP and CPU)
  - Switching power supply controllers and DC/DC charge pump converters
  - MOSFET drivers
  - Supervisory circuits
- Power Management Products, Volume 3:
  - Power distribution switches
  - LED drivers
  - Voltage Rail splitters
  - Special Functions

More than a collection of data sheets, this data book set is a tool for locating the best power management components for a successful design effort. It is structured to help you quickly find the devices best suited to your application. The set contains:

- An alphanumeric index at the beginning of each book to make finding known part numbers simple.
- Product selection guides with a condensed view of parametric information organized to help you choose the devices that most closely fit your needs.
- Key specifications and features presented for easy comparison.
- A section on mechanical specifications for all packages used with Texas Instruments power management devices.

While this data book offers design and specification data only for power management products, complete technical data for any TI semiconductor product is available from your nearest TI Field Sales Office, local authorized TI distributor, or from the TI web site at:

http://www.ti.com/sc

We believe you will find the 1999 Power Management Data Book set to be a valuable addition to your collection of technical literature.

TEXAS INSTRUMENTS
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FIXED-VOLTAGE LOW DROPOUT (LDO) VOLTAGE REGULATORS

Device	V_O (typ) (V)	I_O (max) (mA)	V_{do} (typ) (V)	V_{do} (max) (V)	I_q (typ) (mA)	Tolerance (%)	V_{IN} (max) (V)	Shutdown	SVS	Description	Page No.
TPS76912	1.224	100	0.122	0.245	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–345
TPS77012	1.224	50	0.06	0.125	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–359
TPS76515	1.5	150	0.19	0.33	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–261
TPS76615	1.5	250	0.31	0.54	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–277
TPS76715	1.5	1000	0.5	0.825	0.085	2	10	Yes	Yes	Fixed, LDO, Positive Output	2–293
TPS76815	1.5	1000	0.5	0.825	0.085	2	10	Yes	No	Fixed, LDO, Positive Output	2–329
TPS76915	1.5	100	0.122	0.245	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–345
TPS77015	1.5	50	0.06	0.125	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–359
TPS77515	1.5	500	0.169	0.287	0.085	2	13.5	Yes	Yes	Fixed, LDO, Positive Output	2–373
TPS77615	1.5	500	0.169	0.287	0.085	2	13.5	Yes	No	Fixed, LDO, Positive Output	2–373
TPS77715	1.5	750	0.26	0.427	0.085	2	13.5	Yes	Yes	Fixed, LDO, Positive Output	2–391
TPS77815	1.5	750	0.26	0.427	0.085	2	13.5	Yes	No	Fixed, LDO, Positive Output	2–391
TPS76316	1.6	150	0.36	0.6	0.085	4	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–231
TPS76318	1.8	150	0.3	0.5	0.085	3.7	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–231
TPS73HD318	1.8	750	0.353		0.55	2	10	Yes	Yes	Adjustable, Dual, Fixed, LDO, Positive Output	2–185
TPS76518	1.8	150	0.19	0.33	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–261
TPS76618	1.8	250	0.31	0.54	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–277
TPS76718	1.8	1000	0.5	0.825	0.085	2	10	Yes	Yes	Fixed, LDO, Positive Output	2–293
TPS767D318	1.8	1000	0.35	0.825	0.085	2	10	Yes	Yes	Dual, Fixed, LDO, Positive Output	2–311
TPS76818	1.8	1000	0.5	0.825	0.085	2	10	Yes	No	Fixed, LDO, Positive Output	2–329
TPS76918	1.8	100	0.122	0.245	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–345
TPS77018	1.8	50	0.06	0.125	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–359
TPS77518	1.8	500	0.169	0.287	0.085	2	13.5	Yes	Yes	Fixed, LDO, Positive Output	2–373
TPS77718	1.8	750	0.26	0.427	0.085	2	13.5	Yes	Yes	Fixed, LDO, Positive Output	2–391
TPS77618	1.8	500	0.169	0.287	0.085	2	13.5	Yes	No	Fixed, LDO, Positive Output	2–373
TPS77818	1.8	750	0.26	0.427	0.085	2	13.5	Yes	No	Fixed, LDO, Positive Output	2–391
TPS76325	2.5	150	0.36	0.6	0.085	3.7	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–231
TPS71025	2.5	500	0.33	0.5	0.29	2	10	Yes	No	Fixed, LDO, Positive Output	2–59
TPS7225	2.5	250			0.18	2	10	Yes	No	Fixed, LDO, Positive Output	2–113
TPS7325	2.5	500	0.27	0.6	0.34	2	10	Yes	Yes	Fixed, LDO, Positive Output	2–145
TPS73HD325	2.5	750	0.353		0.55	2	10	Yes	Yes	Adjustable, Dual, Fixed, LDO, Positive Output	2–185
TPS76425	2.5	150	0.36	0.6	0.085	3.7	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–247
TPS76525	2.5	150	0.19	0.33	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–261

FIXED-VOLTAGE LOW DROPOUT (LDO) VOLTAGE REGULATORS (continued)

Device	V_O (typ) (V)	I_O (max) (mA)	V_{do} (typ) (V)	V_{do} (max) (V)	I_q (typ) (mA)	Tolerance (%)	V_{IN} (max) (V)	Shutdown	SVS	Description	Page No.
TPS76625	2.5	250	0.31	0.54	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–277
TPS76725	2.5	1000	0.5	0.825	0.085	2	10	Yes	Yes	Fixed, LDO, Positive Output	2–293
TPS767D325	2.5	1000	0.35	0.825	0.085	2	10	Yes	Yes	Dual, Fixed, LDO, Positive Output	2–311
TPS76825	2.5	1000	0.5	0.825	0.085	2	10	Yes	No	Fixed, LDO, Positive Output	2–329
TPS76925	2.5	100	0.122	0.245	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–345
TPS77025	2.5	50	0.06	0.125	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–359
TPS77525	2.5	500	0.169	0.287	0.085	2	13.5	Yes	Yes	Fixed, LDO, Positive Output	2–373
TPS77625	2.5	500	0.169	0.287	0.085	2	13.5	Yes	No	Fixed, LDO, Positive Output	2–373
TPS77725	2.5	750	0.26	0.427	0.085	2	13.5	Yes	Yes	Fixed, LDO, Positive Output	2–391
TPS77825	2.5	750	0.26	0.427	0.085	2	13.5	Yes	No	Fixed, LDO, Positive Output	2–391
TPS76327	2.7	150	0.36	0.6	0.085	3.75	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–231
TPS76427	2.7	150	0.36	0.6	0.085	3.7	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–247
TPS76527	2.7	150	0.19	0.33	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–261
TPS76627	2.7	250	0.31	0.54	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–277
TPS76727	2.7	1000	0.5	0.825	0.085	2	10	Yes	Yes	Fixed, LDO, Positive Output	2–293
TPS76827	2.7	1000	0.5	0.825	0.085	2	10	Yes	No	Fixed, LDO, Positive Output	2–329
TPS76927	2.7	100	0.122	0.245	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–345
TPS77027	2.7	50	0.06	0.125	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–359
TPS76928	2.784	100	0.122	0.245	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–345
TPS77028	2.784	50	0.06	0.125	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–359
TPS7228	2.8	250			0.18	2	10	Yes	No	Fixed, LDO, Positive Output	2–113
TPS76328	2.8	150	0.35	0.55	0.085	3.75	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–231
TPS76428	2.8	150	0.36	0.6	0.085	3.8	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–247
TPS76528	2.8	150	0.19	0.33	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–261
TPS76628	2.8	250	0.31	0.54	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–277
TPS76728	2.8	1000	0.5	0.825	0.085	2	10	Yes	Yes	Fixed, LDO, Positive Output	2–293
TPS76828	2.8	1000	0.5	0.825	0.085	2	10	Yes	No	Fixed, LDO, Positive Output	2–329
TPS7230	3	250	0.39	0.9	0.18	2	10	Yes	No	Fixed, LDO, Positive Output	2–113
TPS7330	3	500	0.052	0.075	0.34	2	10	Yes	Yes	Fixed, LDO, Positive Output	2–145
TPS76030	3	50	0.12	0.18	0.85	3	16	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–211
TPS76130	3	100	0.17	0.28	2.6	3.6	16	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–221
TPS76330	3	150	0.35	0.55	0.085	3.75	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–231
TPS76430	3	150	0.36	0.6	0.085	3.8	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–247

TEXAS INSTRUMENTS
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FIXED-VOLTAGE LOW DROPOUT (LDO) VOLTAGE REGULATORS (continued)

Device	V_O (typ) (V)	I_O (max) (mA)	V_{do} (typ) (V)	V_{do} (max) (V)	I_q (typ) (mA)	Tolerance (%)	V_{IN} (max) (V)	Shutdown	SVS	Description	Page No.
TPS76530	3	150	0.16	0.28	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–261
TPS76630	3	250	0.31	0.54	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–277
TPS76730	3	1000	0.45	0.675	0.085	2	10	Yes	Yes	Fixed, LDO, Positive Output	2–293
TPS76830	3	1000	0.45	0.675	0.085	2	10	Yes	No	Fixed, LDO, Positive Output	2–329
TPS77030	3	50	0.048	0.1	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–359
TPS76930	3.09	100	0.115	0.23	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–345
TPS76032	3.2	50	0.12	0.18	0.85	3.1	16	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–211
TPS76132	3.2	100	0.17	0.28	2.6	3	16	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–221
TPS7133QPWP	3.3	500	0.047	0.06	0.285	2	10	Yes	No	Fixed, LDO, Positive Output	2–3
TPS7133	3.3	500	0.047	0.06	0.285	2	10	Yes	No	Fixed, LDO, Positive Output	2–29
TPS71H33	3.3	500	0.047	0.06	0.285	2	10	Yes	No	Fixed, LDO, Positive Output	2–75
TPS7233	3.3	250	0.14	0.18	0.155	2	10	Yes	No	Fixed, LDO, Positive Output	2–113
TPS7333	3.3	500	0.044	0.06	0.34	2	10	Yes	Yes	Fixed, LDO, Positive Output	2–145
TPS76033	3.3	50	0.12	0.18	0.85	3	16	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–211
TPS76133	3.3	100	0.17	0.28	2.6	3	16	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–221
TPS76333	3.3	150	0.3	0.5	0.085	3.7	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–231
TPS76433	3.3	150	0.3	0.5	0.085	3.7	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–247
TPS76533	3.3	150	0.14	0.24	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–261
TPS76633	3.3	250	0.23	0.4	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–277
TPS76733	3.3	1000	0.35	0.575	0.085	2	10	Yes	Yes	Fixed, LDO, Positive Output	2–293
TPS76833	3.3	1000	0.35	0.575	0.085	2	10	Yes	No	Fixed, LDO, Positive Output	2–329
TPS76933	3.3	100	0.098	0.2	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–345
TPS77033	3.3	50	0.048	0.1	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–359
TPS77533	3.3	500	0.169	0.287	0.085	2	13.5	Yes	Yes	Fixed, LDO, Positive Output	2–373
TPS77633	3.3	500	0.169	0.287	0.085	2	13.5	Yes	No	Fixed, LDO, Positive Output	2–373
TPS77733	3.3	750	0.26	0.427	0.085	2	13.5	Yes	Yes	Fixed, LDO, Positive Output	2–391
TPS77833	3.3	750	0.26	0.427	0.085	2	13.5	Yes	No	Fixed, LDO, Positive Output	2–391
TLV2217–33	3.3	500	0.4	0.5	19	1	12	No	No	LDO	2–461
TPS76038	3.8	50	0.12	0.18	0.85	2.6	16	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–211
TPS76138	3.8	100	0.17	0.28	2.6	3	16	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–221
TPS76338	3.8	150	0.36	0.6	0.085	3.5	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–231
TPS7148	4.85	500	0.03	0.037	0.285	2	10	Yes	No	Fixed, LDO, Positive Output	2–29
TPS71H48	4.85	500	0.03	0.047	0.285	2	10	Yes	No	Fixed, LDO, Positive Output	2–75

FIXED-VOLTAGE LOW DROPOUT (LDO) VOLTAGE REGULATORS (continued)

Device	V_O (typ) (V)	I_O (max) (mA)	V_{do} (typ) (V)	V_{do} (max) (V)	I_q (typ) (mA)	Tolerance (%)	V_{IN} (max) (V)	Shutdown	SVS	Description	Page No.
TPS7248	4.85	250	0.09	0.1	0.155	2	10	Yes	No	Fixed, LDO, Positive Output	2–113
TPS7348	4.85	500	0.028	0.037	0.34	2	10	Yes	Yes	Fixed, LDO, Positive Output	2–145
TPS7150	5	500	0.027	0.033	0.285	2	10	Yes	No	Fixed, LDO, Positive Output	2–29
TPS71H50	5	500	0.027	0.033	0.285	2	10	Yes	No	Fixed, LDO, Positive Output	2–75
TPS7250	5	250	0.76	0.85	0.155	2	10	Yes	No	Fixed, LDO, Positive Output	2–113
TPS7350	5	500	0.027	0.035	0.34	2	10	Yes	Yes	Fixed, LDO, Positive Output	2–145
TPS76050	5	50	0.12	0.18	0.85	2	16	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–211
TPS76150	5	100	0.17	0.28	2.6	2.8	16	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–221
TPS76350	5	150	0.18	0.3	0.085	4	10	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–231
TPS76550	5	150	0.085	0.15	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–261
TPS76650	5	250	0.14	0.25	0.038	3	13.5	Yes	No	Fixed, LDO, Positive Output	2–277
TPS76750	5	1000	0.23	0.38	0.085	2	10	Yes	Yes	Fixed, LDO, Positive Output	2–293
TPS76850	5	1000	0.23	0.38	0.085	2	10	Yes	No	Fixed, LDO, Positive Output	2–329
TPS76950	5	100	0.071	0.17	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–345
TPS77050	5	50	0.035	0.085	0.017	3	13.5	Yes	No	Fixed, LDO, Positive Output, SOT–23	2–359
TL750L05	5	150	0.2	0.6	10	4	26	No	No	Fixed, LDO, Positive Output	2–421
TL750M05	5	750	0.5	0.6	60	2	26	No	No	Fixed, LDO, Positive Output	2–429
TL751L05	5	150	0.2	0.6	10	4	26	Yes	No	Fixed, LDO, Positive Output	2–421
TL751M05	5	750	0.5	0.6	60	2	26	Yes	No	Fixed, LDO, Positive Output	2–429
TL750L08	8	150	0.2	0.7	10	4	26	No	No	Fixed, LDO, Positive Output	2–421
TL750M08	8	750	0.5	0.7	60	2	26	No	No	Fixed, LDO, Positive Output	2–429
TL751L08	8	150	0.2	0.7	10	4	26	Yes	No	Fixed, LDO, Positive Output	2–421
TL751M08	8	750	0.5	0.7	60	2	26	Yes	No	Fixed, LDO, Positive Output	2–429
TL750L10	10	150	0.2	0.8	10	4	26	No	No	Fixed, LDO, Positive Output	2–421
TL750M10	10	750	0.5	0.8	60	2	26	No	No	Fixed, LDO, Positive Output	2–429
TL751L10	10	150	0.2	0.8	10	4	26	Yes	No	Fixed, LDO, Positive Output	2–421
TL751M10	10	750	0.5	0.8	60	2	26	Yes	No	Fixed, LDO, Positive Output	2–429
TL750L12	12	150	0.2	0.9	10	4	26	No	No	Fixed, LDO, Positive Output	2–421
TL750M12	12	750	0.5	0.9	60	2	26	No	No	Fixed, LDO, Positive Output	2–429
TL751L12	12	150	0.2	0.9	10	4	26	Yes	No	Fixed, LDO, Positive Output	2–421
TL751M12	12	750	0.5	0.9	60	2	26	Yes	No	Fixed, LDO, Positive Output	2–429

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ADJUSTABLE OUTPUT-VOLTAGE REGULATORS

Device	V_O Adjustable (nom) (V)	I_O (max) (mA)	V_{do} (typ) (V)	V_{do} (max) (V)	I_q (typ) (mA)	Tolerance (%)	V_{IN} (max) (V)	Shutdown	SVS	Description	Page No.
TPS76501	1.2 – 5.5	150	0.16	0.33	0.038	3	13.5	Yes	No	Adjustable, LDO, Positive Output	2–261
TPS76601	1.2 – 5.5	250	0.23	0.54	0.038	3	13.5	Yes	No	Adjustable, LDO, Positive Output	2–277
TPS76701	1.5 – 5.5	1000	0.5	0.825	0.085	2	10	Yes	Yes	Adjustable, LDO, Positive Output	2–293
TPS767D301	1.2–5.5	1000	0.35	0.825	0.085	2	10	Yes	Yes	Adjustable, Dual, Fixed, LDO, Positive Output	2–311
TPS76801	1.5 – 5.5	1000	0.5	0.825	0.085	2	10	Yes	No	Adjustable, LDO, Positive Output	2–329
TPS76901	1.2 – 5.5	100	0.071	0.245	0.017	3	13.5	Yes	No	Adjustable, LDO, Positive Output, SOT–23	2–345
TPS77001	1.2 – 5.5	50	0.035	0.125	0.017	3	13.5	Yes	No	Adjustable, LDO, Positive Output, SOT–23	2–359
TPS77501	1.2 – 5.5	500	0.169	0.287	0.085	2	13.5	Yes	Yes	Adjustable, LDO, Positive Output	2–373
TPS77601	1.2 – 5.5	500	0.169	0.287	0.085	2	13.5	Yes	No	Adjustable, LDO, Positive Output	2–373
TPS77701	1.2 – 5.5	750	0.26	0.427	0.085	2	13.5	Yes	Yes	Adjustable, LDO, Positive Output	2–391
TPS77801	1.2 – 5.5	750	0.26	0.427	0.085	2	13.5	Yes	No	Adjustable, LDO, Positive Output	2–391
TPS76301	1.5 – 6.5	150	0.6	0.6	0.085	3	10	Yes	No	Adjustable, LDO, Positive Output, SOT–23	2–231
TPS7101	1.2 – 9.75	500	0.052	0.085	0.285	3	10	Yes	No	Adjustable, LDO	2–29
TPS71H01	1.2 – 9.75	500	0.052	0.085	0.285	3	10	Yes	No	Adjustable, LDO	2–75
TPS7201	1.2 – 9.75	250	0.16	0.27	0.155	3	10	Yes	No	Adjustable, LDO	2–113
TPS7301	1.2 – 9.75	500	0.052	0.085	0.34	3	10	Yes	Yes	Adjustable, LDO	2–145
TPS73HD301	1.2 – 9.75	750	0.353	0.6	1.1	3	10	Yes	Yes	Adjustable, Dual, Fixed, LDO, Positive Output	2–185
TL317	1.2 – 32	100	2.5	3	1.5	4	35	No	No	Adjustable	2–415
µA723	2 – 37	150		3	2.3	1	40	No	No	Adjustable	2–467
TL783	1.25 – 125	700	10	15	15	6	125	No	No	Adjustable	2–449
LM237	–1.2 – –37	1500			2.2			No	No	3-Terminal Adjustable Regulator	2–409
LM337	–1.2 – –37	1500			2.2			No	NO	3-Terminal Adjustable Regulator	2–409

FIXED POSITIVE-OUTPUT VOLTAGE VOLTAGE REGULATORS

Device	V_O (typ) (V)	I_O (max) (mA)	V_{do} (typ) (V)	V_{do} (max) (V)	I_q (typ) (mA)	Tolerance (%)	V_{IN} (max) (V)	Shutdown	SVS	Description	Page No.
µA78L02A	2	100	1.7	3	3.6	5	20	No	No	Fixed, Positive Output	2–493
TL–SCSI285	2.85	500		0.7	26	1	5.5	No		Fixed Reg. for SCSI Active Termination	2–527
TL2217–285	2.85	500		1	26	1.5	5.5	No		Fixed Reg. for SCSI Active Termination	2–533
µA7805	5	1500	2	3	4.2	4	25	No	No	Fixed, Positive Output	2–479
µA78L05	5	100	2	3	3.8	10	20	No	No	Fixed, Positive Output	2–493
µA78L05A	5	100	1.7	3	3.8	5	20	No	No	Fixed, Positive Output	2–493
µA78M05	5	500	2	3	4.5	4	25	No	No	Fixed, Positive Output	2–505
TL780–05	5	1500	2	3	5	1	25	No	No	Fixed, Positive Output	2–441
µA7806	6	1500	2	3	4.3	4	25	No	No	Fixed, Positive Output	2–479
µA78L06	6	100	1.7	3	3.9	10	20	No	No	Fixed, Positive Output	2–493
µA78L06A	6	100	1.7	3	3.9	5	20	No	No	Fixed, Positive Output	2–493
µA78M06	6	500	2	3	4.5	4	25	No	No	Fixed, Positive Output	2–505
µA7808	8	1500	2.5	3	4.3	4	25	No	No	Fixed, Positive Output	2–479
µA7885	8	1500	2	3	4.3	4	25	No	No	Fixed, Positive Output	2–479
µA78L08	8	100	1.7	3	4	10	23	No	No	Fixed, Positive Output	2–493
µA78L08A	8	100	1.7	3	4	5	23	No	No	Fixed, Positive Output	2–493
µA78M08	8	500	2.5	3	4.6	4	25	No	No	Fixed, Positive Output	2–505
µA78L09	9	100	1.7	3	4.1	10	24	No	No	Fixed, Positive Output	2–493
µA78L09A	9	100	1.7	3	4.1	5	24	No	No	Fixed, Positive Output	2–493
µA78M09	9	500	2.5	3	4.6	4	26	No	No	Fixed, Positive Output	2–505
µA7810	10	1500	2.5	3	4.3	4	28	No	No	Fixed, Positive Output	2–479
µA78L10	10	100	1.7	3	4.2	10	25	No	No	Fixed, Positive Output	2–493
µA78L10A	10	100	1.7	3	4.2	5	25	No	No	Fixed, Positive Output	2–493
µA78M10	10	500	2.5	3	4.6	4	28	No	No	Fixed, Positive Output	2–505
TL780–12	12	1500	2.5	3	5.5	1	30	No	No	Fixed, Positive Output	2–441
µA7812	12	1500	2.5	3	4.3	4	30	No	No	Fixed, Positive Output	2–479
µA78L12	12	100	1.7	3	4.3	10	27	No	No	Fixed, Positive Output	2–493
µA78L12A	12	100	1.7	3	4.3	5	27	No	No	Fixed, Positive Output	2–493
µA78M12	12	500	2.5	3	4.8	4	30	No	No	Fixed, Positive Output	2–505
TL780–15	15	1500	2.5	3	5.5	1	30	No	No	Fixed, Positive Output	2–441
µA7815	15	1500	2.5	3	4.4	4	30	No	No	Fixed, Positive Output	2–479
µA78L15	15	100	1.7	3	4.6	10	30	No	No	Fixed, Positive Output	2–493
µA78L15A	15	100	1.7	3	4.6	5	30	No	No	Fixed, Positive Output	2–493

TEXAS INSTRUMENTS
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FIXED POSITIVE-OUTPUT VOLTAGE VOLTAGE REGULATORS (continued)

Device	V_O (typ) (V)	I_O (max) (mA)	V_{do} (typ) (V)	V_{do} (max) (V)	I_q (typ) (mA)	Tolerance (%)	V_{IN} (max) (V)	Shutdown	SVS	Description	Page No.
µA78M15	15	500	2.5	3	4.8	4	30	No	No	Fixed, Positive Output	2–505
µA7818	18	1500	3	3	4.5	4	33	No	No	Fixed, Positive Output	2–479
µA78M20	20	500	3	3	4.9	4	35	No	No	Fixed, Positive Output	2–505
µA7824	24	1500	3	3	4.6	4	38	No	No	Fixed, Positive Output	2–479
µA78M24	24	500	3	3	5	4	38	No	No	Fixed, Positive Output	2–505

FIXED NEGATIVE-OUTPUT VOLTAGE VOLTAGE REGULATORS

Device	V_O (typ) (V)	I_O (max) (mA)	V_{do} (typ) (V)	V_{do} (max) (V)	I_q (typ) (mA)	Tolerance (%)	V_{IN} (max) (V)	Shutdown	SVS	Description	Page No.
µA79M05	–5	500	2	3	1	4	–25	No	No	Fixed, Negative Output	2–517
µA79M06	–6	500	2	3	1	4	–25	No	No	Fixed, Negative Output	2–517
µA79M08	–8	500	2.5	3	1	4	–25	No	No	Fixed, Negative Output	2–517
µA79M12	–12	500	2.5	3	1.5	4	–30	No	No	Fixed, Negative Output	2–517
µA79M15	–15	500	2.5	3	1.5	4	–30	No	No	Fixed, Negative Output	2–517
µA79M20	–20	500	3	3	1.5	4	–35	No	No	Fixed, Negative Output	2–517
µA79M24	–24	500	3	3	1.5	4	–38	No	No	Fixed, Negative Output	2–517

SHUNT REGULATORS

Device	V_{ref} (V)	I_Z (min) (μA)	I_Z (max) (mA)	V_O (min) (V)	V_O (max) (V)	Tolerance (%)	V_I (max) (V)	Temp Coeff (typ) (ppm/°C)	Description	Page No.
TLV431A	1.24	100	15	Vref	6	1	6	46	Adjustable Shunt	3–45
TL1431	2.5	1000	100	Vref	36	0.4	36	30	Adjustable Shunt	3–27
TL431	2.5	1000	100	Vref	36	2	36	30	Adjustable Shunt	3–9
TL431A	2.5	1000	100	Vref	36	1	36	30	Adjustable Shunt	3–9
TLV431	2.5	1000	100	Vref	36	2	36	30	Adjustable Shunt	3–45
TL430	2.75	2000	100	Vref	30	9	30	120	Adjustable Shunt	3–3

PRECISION VIRTUAL GROUNDS

Device	I_O (typ) (mA)	Output Regulation (typ) (μA)	V_O (min) (V)	V_O (max) (V)	V_I (max) (V)	Temp Coeff (typ) (ppm/°C)	Description	Page No.
TLE2425	20	–45 – 15	2.48	2.52	40	20	Precision Virtual Ground	4–3

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PROCESSOR POWER SUPPLY CONTROLLERS

Device	Droop Comp	OCP	Output Drive Current (A)	Outputs	OVP	Power Good	Soft Start	UVLO	V_{IN} (V)	V_O (typ) (V)	V_{ref} (tol) (±%)	Description	Page No.
TPS5102	No	Yes	1.5	2	No	No	Yes	Yes	4.5 – 25	1.2 – Vcc	1.5	Notebook	7–3
TPS5103	No	Yes	1.5	1	No	No	Yes	Yes	4.5 – 25	1.2 – Vcc	1.5	Multipurpose	7–33
TPS5210	Yes	Yes	2	1	Yes	Yes	Yes	Yes	5, 12	pgm 1.3 to 3.5	1	Pentium class	7–123
TPS5211	Yes	Yes	2.4	1	Yes	Yes	Yes	Yes	5, 12	pgm 1.3 to 3.5	1.5	Pentium class	7–69
TPS5602	No	Yes	1	2	No	No	Yes	Yes	4.5 – 25	1.2 – V_{CC}	2	DSP	7–149
TPS56100	No	Yes	2	1	Yes	Yes	Yes	Yes	5	0.9 – V_{CC}	1.5	DSP	7–171
TPS5615	No	Yes	2	1	Yes	Yes	Yes	Yes	5, 12	1.5	1	DSP	7–99
TPS5618	No	Yes	2	1	Yes	Yes	Yes	Yes	5, 12	1.8	1	DSP	7–99
TPS5625	No	Yes	2	1	Yes	Yes	Yes	Yes	5, 12	2.8	1	DSP	7–99
TPS5633	No	Yes	2.4	1	Yes	Yes	Yes	Yes	5, 12	3.3	1	DSP	7–99

SWITCHING POWER SUPPLY CONTROLLERS

Device	SHDN	Pulse-by-Pulse I_{sense}	V_{IN} Range (VDC)	Output Type	Output Current (mA)	Freq (max) (kHz)	Operating/ Standby Current (mA)	Reference Voltage (V)	V_{ref} Tol (%)	Duty Cycle (max) (%)	UVLO	Description	Page No.
SG2524	Yes	No	8–40	Single Switch	100	500	NA/8	5	4	90	No	Voltage-Mode PWM	8–97
SG3524	Yes	No	8–40	Single Switch	100	500	NA/8	5	8	90	No	Voltage-Mode PWM	8–97
TL494	No	No	7–40	Single Switch	200	300	7.5/6	5	5	90	No	Voltage-Mode PWM	8–111
TL497A	Yes	No	4.5–12	Single Switch	500	50	11/6	1.2	5		No	Fixed On-Time Voltage-Mode	8–121
TL499A	No	No	1.1–35	Single Switch	500	40	1.8/NA	1.26	5		No	Fixed On-Time Voltage-Mode	8–129
TL594	No	No	7–40	Single Switch	200	300	12.4/9	5	1	90	Yes	Voltage-Mode PWM	8–137
TL598	No	No	7–40	Totem Pole	–250	300	15/NA	5	1	90	Yes	Voltage-Mode PWM	8–149
UC2842	No	Yes	30	Totem Pole	–200	500	11/NA	5	1	97	Yes	Current-Mode PWM	8–159
UC2843	No	Yes	30	Totem Pole	–200	500	11/NA	5	1	97	Yes	Current-Mode PWM	8–159
UC2844	No	Yes	30	Totem Pole	–200	500	11/NA	5	1	97	Yes	Current-Mode PWM	8–159
UC2845	No	Yes	30	Totem Pole	–200	500	11/NA	5	1	97	Yes	Current-Mode PWM	8–159
UC3842	No	Yes	30	Totem Pole	–200	500	11/NA	5	2	97	Yes	Current-Mode PWM	8–159
UC3843	No	Yes	30	Totem Pole	–200	500	11/NA	5	2	97	Yes	Current-Mode PWM	8–159
UC3844	No	Yes	30	Totem Pole	–200	500	11/NA	5	2	97	Yes	Current-Mode PWM	8–159
UC3845	No	Yes	30	Totem Pole	–200	500	11/NA	5	2	97	Yes	Current-Mode PWM	8–159
TL5001	No	No	3.6–40	Single Switch	20	400	1.1/1	1	5	100	Yes	Voltage-Mode PWM	8–79
TL5001A	No	No	3.6–40	Single Switch	20	400	1.1/1	1	3	100	Yes	Voltage-Mode PWM	8–79
LT1054	No	No	3.6–15	Totem Pole	±100	2000	3.5/3.1	1.25	2.5	100	Yes	Dual Channel-Mode PWM	8–171

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DC/DC CHARGE PUMP CONVERTERS

Device	SHDN	VO (typ) (V)	Tolerance (%)	V_{IN} Range (VDC)	Output Current (mA)	Freq (max) (kHz)	Quiescent Current (μA)	Shut-down Current (μA)	UVLO	Description	Page No.
TPS60100	Yes	3.3	±4	1.8–3.6	200	300	50	0.05	Yes	Charge Pump DC/DC Converter, 3.3-V	8–3
TPS60101	Yes	3.3	±4	1.8–3.6	100	300	50	0.05	Yes	Charge Pump DC/DC Converter, 3.3-V	8–23
TPS60110	Yes	5	±4	2.7–5.4	300	300	60	0.05	Yes	Charge Pump DC/DC Converter, 5-V	8–43
TPS60111	Yes	5	±4	2.7–5.4	150	300	60	0.05	Yes	Charge Pump DC/DC Converter, 5-V	8–61

MOSFET DRIVERS

Device	I_{CC} (μA)	Internal Regulator	Output Current (max) (A)	Rise/Fall Time (max) (ns)	Supply Voltage(s) (V)	Description	Page No.
TPS2811	5	Yes (8 – 40 V)	2	20	4–14	Dual Channel	9–3
TPS2812	5	Yes (8 – 40 V)	2	20	4–14	Dual Channel	9–3
TPS2813	5	Yes (8 – 40 V)	2	20	4–14	Dual Channel	9–3
TPS2814	5	No	2	20	4–14	Dual Channel	9–3
TPS2815	5	No	2	20	4–14	Dual Channel	9–3
TPS2816	150	Yes (8 – 40 V)	2	25	4–14	Active Pullup, Internal Regulator, Single Channel	9–31
TPS2817	150	Yes (8 – 40 V)	2	25	4–14	Active Pullup, Internal Regulator, Single Channel	9–31
TPS2818	25	Yes (8 – 40 V)	2	25	4–14	Single Channel	9–31
TPS2819	25	Yes (8 – 40 V)	2	25	4–14	Single Channel	9–31
TPS2828	25	No	2	25	4–14	Single Channel	9–31
TPS2829	25	No	2	25	4–14	Single Channel	9–31
TPS2830	1	No	2	50 / 85	4.5–15	Fast Synchronous-Buck With Deadtime Control	9–49
TPS2831	1	No	2	50 / 85	4.5–15	Fast Synchronous-Buck With Deadtime Control	9–49
TPS2832	1	No	2	50 / 85	4.5–15	Fast Synchronous-Buck With Deadtime Control	9–61
TPS2833	1	No	2	50 / 85	4.5–15	Fast Synchronous-Buck With Deadtime Control	9–61

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SUPERVISORY CIRCUITS

Device	V_{CC} (nom) (V)	V_t (V)	Tolerance (%)	I_{CC} (max) (mA)	V_{IN} (min) (V)	Over Voltage Sense	Comp Outputs	Number of SVS	WDI	Description	Page No.
TPS3123J12	1.2	1.08	2	0.03	0.75	No	No	1	Yes	Fixed Delay, Micropower	10–21
TPS3124J12	1.2	1.08	2	0.03	0.75	No	Yes	1	Yes	Fixed Delay, Micropower	10–21
TPS3125J12	1.2	1.08	2	0.03	0.75	No	Yes	1	No	Fixed Delay, Micropower	10–21
TPS3123G15	1.5	1.4	2	0.03	0.75	No	No	1	Yes	Fixed Delay, Micropower	10–21
TPS3124G15	1.5	1.4	2	0.03	0.75	No	Yes	1	Yes	Fixed Delay, Micropower	10–21
TPS3125G15	1.5	1.4	2	0.03	0.75	No	Yes	1	No	Fixed Delay, Micropower	10–21
TPS3123J18	1.8	1.62	2	0.03	0.75	No	No	1	Yes	Fixed Delay, Micropower	10–21
TPS3124J18	1.8	1.62	2	0.03	0.75	No	Yes	1	Yes	Fixed Delay, Micropower	10–21
TPS3125J18	1.8	1.62	2	0.03	0.75	No	Yes	1	No	Fixed Delay, Micropower	10–21
TPS3305–18	1.8	1.68	2	0.04	2.7	No	Yes	2	Yes	Fixed Delay, Micropower	10–33
TPS3307–18	1.8	1.68	2	0.04	2	No	Yes	3	No	Fixed Delay, Micropower	10–43
TLC7725	2.5	2.25	3	0.016	1	No	Yes	1	No	Micropower, Programmable Delay	10–9
TPS3707–25	2.5	2.25	2	0.05	2	No	Yes	1	No	Fixed Delay, Micropower	10–53
TPS3801J25	2.5	2.25	2	0.012	2	No	No	1	No	Fixed Delay, Micropower	10–63
TPS3305–25	2.5	2.25	2	0.04	2.7	No	Yes	2	Yes	Fixed Delay, Micropower	10–33
TPS3809J25	2.5	2.25	2	0.012	2	No	No	1	No	Fixed Delay, Micropower	10–3
TPS3820–25	2.5	2.25	1.8	0.025		No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3823–25	2.5	2.25	1.8	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3824–25	2.5	2.25	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3825–25	2.5	2.25	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3828–25	2.5	2.25	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3307–25	2.5	2.25	2	0.04	2	No	Yes	3	No	Fixed Delay, Micropower	10–43
TLC7703	3	2.63	2.7	0.016	1	No	Yes	1	No	Micropower, Programmable Delay	10–9
TPS3125L30	3	2.64	2	0.03	0.75	No	Yes	1	No	Fixed Delay, Micropower	10–21
TPS3705–30	3	2.63	2	0.05	2	No	No	1	Yes	Fixed Delay, Micropower	10–53
TPS3707–30	3	2.63	2	0.05	2	No	Yes	1	No	Fixed Delay, Micropower	10–53
TPS3801L30	3	2.64	2	0.012	2	No	No	1	No	Fixed Delay, Micropower	10–63
TPS3809L30	3	2.64	2	0.012	2	No	No	1	No	Fixed Delay, Micropower	10–3
TPS3820–30	3	2.63	1.5	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3823–30	3	2.63	1.5	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3824–30	3	2.63	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71

SUPERVISORY CIRCUITS (continued)

Device	V_{CC} (nom) (V)	V_t (V)	Tolerance (%)	I_{CC} (max) (mA)	V_{IN} (min) (V)	Over Voltage Sense	Comp Outputs	Number of SVS	WDI	Description	Page No.
TPS3825–30	3	2.63	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3828–30	3	2.63	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TLC7733	3.3	2.93	2.4	0.016	1	No	Yes	1	No	Micropower, Programmable Delay	10–9
TPS3705–33	3.3	2.93	2	0.05	2	No	No	1	Yes	Fixed Delay, Micropower	10–53
TPS3707–33	3.3	2.93	2	0.05	2	No	Yes	1	No	Fixed Delay, Micropower	10–53
TPS3801K33	3.3	2.93	2	0.012	2	No	No	1	No	Fixed Delay, Micropower	10–63
TPS3809K33	3.3	2.93	2	0.012	2	No	No	1	No	Fixed Delay, Micropower	10–3
TPS3820–33	3.3	2.93	1.7	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3823–33	3.3	2.93	1.7	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3824–33	3.3	2.93	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3825–33	3.3	2.93	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3828–33	3.3	2.93	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TL7705A	5	4.55	2	3	3.6	No	Yes	1	No	Programmable Delay	10–91
TL7705B	5	4.55	2	3	1	No	Yes	1	No	Programmable Delay	10–113
TL7757	5	4.55	3	2.5	1	No	No	1	No	No Delay	10–123
TL7759	5	4.55	3	2	1	No	Yes	1	No	No Delay	10–133
TLC7705	5	4.55	1.5	0.016	1	No	Yes	1	No	Micropower, Programmable Delay	10–9
TL7770–5	5	4.55	1	5	1	Yes	Yes	2	No	Programmable Delay	10–139
TPS3705–50	5	4.55	2	0.05	2	No	No	1	Yes	Fixed Delay, Micropower	10–53
TPS3707–50	5	4.55	2	0.05	2	No	Yes	1	No	Fixed Delay, Micropower	10–53
TPS3801I50	5	4.55	2	0.012	2	No	No	1	No	Fixed Delay, Micropower	10–63
TPS3305–33	5	4.55	2	0.04	2.7	No	Yes	2	Yes	Fixed Delay, Micropower	10–33
TPS3809I50	5	4.55	2	0.012	2	No	No	1	No	Fixed Delay, Micropower	10–3
TPS3820–50	5	4.55	1.3	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3823–50	5	4.55	1.3	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3824–50	5	4.55	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3825–50	5	4.55	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3828–50	5	4.55	2	0.025	1.1	No	Yes	1	Yes	Fixed Delay, Micropower	10–71
TPS3307–33	5	4.55	2	0.04	2	No	Yes	3	No	Fixed Delay, Micropower	10–43
TL7709A	9	7.6	2	3	3.6	No	Yes	1	No	Programmable Delay	10–91

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SUPERVISORY CIRCUITS (continued)

Device	V_{CC} (nom) (V)	V_t (V)	Tolerance (%)	I_{CC} (max) (mA)	V_{IN} (min) (V)	Over Voltage Sense	Comp Outputs	Number of SVS	WDI	Description	Page No.
TL7712A	12	10.8	2	3	3.6	No	Yes	1	No	Programmable Delay	10–91
TL7770–12	12	10.9	1	5	1	Yes	Yes	2	No	Programmable Delay	10–139
TL7715A	15	13.5	2	3	3.6	No	Yes	1	No	Programmable Delay	10–91
TPS5510			3	1	4	Yes	Yes	3	No	Fixed Delay	10–79
TPS5511			3	1	4	Yes	Yes	3	No	Fixed Delay	10–85
TL7700	adj			0.016		No	Yes	1	No	Micropower, Programmable Delay	10–101
TL7702A	pgm	pgm	2	3	3.6	No	Yes	1	No	Programmable Delay	10–91
TL7702B	pgm	pgm	2	3	1	No	Yes	1	No	Programmable Delay	10–113
TLC7701	adj	1.1	5.4	0.016	1	No	Yes	1	No	Micropower, Programmable Delay	10–9

GENERAL PURPOSE DISTRIBUTION SWITCHES

Device	Number of FETs	$r_{DS(on)}$ (typ) (mΩ)	I_O (max) (A)	Current Limit (typ) (A)	V_{IN} Range (typ) (V)	Over Current Reporting	Over Temp Protection	Enable	Description	Page No.
TPS2010	1	75	0.2	0.4	2.7 – 5.5	No	Yes	Neg	Current–Limited	13–25
TPS2010A	1	30	0.2	0.3	2.7 – 5.5	No	Yes	Neg	Current–Limited	13–53
TPS2011	1	75	0.6	1.2	2.7 – 5.5	No	Yes	Neg	Current–Limited	13–25
TPS2011A	1	30	0.6	0.9	2.7 – 5.5	No	Yes	Neg	Current–Limited	13–53
TPS2012	1	75	1	2	2.7 – 5.5	No	Yes	Neg	Current–Limited	13–25
TPS2012A	1	30	1	1.5	2.7 – 5.5	No	Yes	Neg	Current–Limited	13–53
TPS2013	1	75	1.5	2.6	2.7 – 5.5	No	Yes	Neg	Current–Limited	13–25
TPS2013A	1	30	1.5	2.2	2.7 – 5.5	No	Yes	Neg	Current–Limited	13–53

V_{AUX} SWITCHES

Device	Number of Inputs	IN1 $r_{DS(on)}$ (typ) (mΩ)	IN2 $r_{DS(on)}$ (typ) (Ω)	IN1 Output Current (mA)	IN2 Output Current (mA)	IN1 Supply Current (typ) (uA)	IN2 Supply Current (typ) (uA)	IN1, IN2 Input Voltage Range (V)	Enable	Page No.
TPS2100	2	250	1.3	500	10	10	0.75	2.7 – 4.0	Neg	13–311
TPS2101	2	250	1.3	500	10	10	0.75	2.7 – 4.0	Pos	13–311

PCMCIA/CARDBUS DISTRIBUTION SWITCHES

Device	12-V Supply Required	3V/5V $r_{DS(on)}$ (typ) (mΩ)	Control Inputs	Current and Temperature Protection	VPP_Good and $\overline{OC}$ Reporting	Description	Page No.
TPS2205	No	110/140	8 Line Parallel	Yes	N/Y	Dual Channel	13–325
TPS2206	No	110/140	3 Line Serial w/Reset	Yes	N/Y	Dual Channel	13–349
TPS2211	No	50	4 Line Parallel	Yes	N/Y	Single Channel	13–375
TPS2212	No	160	4 Line Parallel	Yes	N/Y	Single Channel	13–395
TPS2214	No	60	3 Line Serial, w/independent VCC/VPP	Yes	N/Y	Dual Channel	13–413
TPS2216	No	60	3 Line Serial, w/independent VCC/VPP	Yes	N/Y	Dual Channel	13–437

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USB SWITCHES

Device	Number of FETs	$r_{DS(on)}$ (typ) (mΩ)	I_O (max) (A)	Current Limit (typ) (A)	V_{IN} Range (typ) (V)	Over Current Reporting	Over Temp Reporting	Enable	Description	Page No.
TPS2014	1	95	0.6	1.2	4.0 – 5.5	Yes	No	Neg	Current–Limited, UL Listed, USB	13–73
TPS2015	1	95	1	2	4.0 – 5.5	Yes	No	Neg	Current–Limited, USB	13–73
TPS2020	1		0.2	0.3	2.7 – 5.5	Yes	Yes	Neg	Current–Limited, USB	13–93
TPS2021	1		0.6	0.9	2.7 – 5.5	Yes	Yes	Neg	Current–Limited, USB	13–93
TPS2022	1		1	1.5	2.7 – 5.5	Yes	Yes	Neg	Current–Limited, USB	13–93
TPS2023	1		1.5	2.2	2.7 – 5.5	Yes	Yes	Neg	Current–Limited, USB	13–93
TPS2024	1		2	3	2.7 – 5.5	Yes	Yes	Neg	Current–Limited, USB	13–93
TPS2030	1	30	0.2	0.3	2.7 – 5.5	Yes	Yes	Pos	Current–Limited, USB	13–115
TPS2031	1	30	0.6	0.9	2.7 – 5.5	Yes	Yes	Pos	Current–Limited, USB	13–115
TPS2032	1	30	1	1.5	2.7 – 5.5	Yes	Yes	Pos	Current–Limited, USB	13–115
TPS2033	1	30	1.5	2.2	2.7 – 5.5	Yes	Yes	Pos	Current–Limited, USB	13–115
TPS2034	1	30	2	3	2.7 – 5.5	Yes	Yes	Pos	Current–Limited, USB	13–115
TPS2041	1	80	0.5	0.9	2.7 – 5.5	Yes	Yes	Neg	Current–Limited, Nemko Recognized	13–137
TPS2042	2	80	0.5	0.9	2.7 – 5.5	Each	Yes	Neg	Current–Limited, Nemko Recognized	13–157
TPS2043	3	80	0.5	0.9	2.7 – 5.5	Each	Yes	Neg	Current–Limited, Nemko Recognized	13–179
TPS2044	4	80	0.5	0.9	2.7 – 5.5	Each	Yes	Neg	Current–Limited, Nemko Recognized	13–203
TPS2045	1	80	0.25	0.44	2.7 – 5.5	Yes	Yes	Neg	Current–Limited, Nemko Recognized	13–227
TPS2046	2	80	0.25	0.44	2.7 – 5.5	Yes	Yes	Neg	Current–Limited, Nemko Recognized	13–247
TPS2047	3	80	0.25	0.44	2.7 – 5.5	Yes	Yes	Neg	Current–Limited, Nemko Recognized	13–267
TPS2048	4	80	0.25	0.44	2.7 – 5.5	Yes	Yes	Neg	Current–Limited, Nemko Recognized	13–289
TPS2051	1	80	0.5	0.9	2.7 – 5.5	Yes	Yes	Pos	Current–Limited, Nemko Recognized	13–137
TPS2052	2	80	0.5	0.9	2.7 – 5.5	Each	Yes	Pos	Current–Limited, Nemko Recognized	13–157
TPS2053	3	80	0.5	0.9	2.7 – 5.5	Each	Yes	Pos	Current–Limited, Nemko Recognized	13–179
TPS2054	4	80	0.5	0.9	2.7 – 5.5	Each	Yes	Pos	Current–Limited, Nemko Recognized	13–203
TPS2055	1	80	0.25	0.44	2.7 – 5.5	Yes	Yes	Pos	Current–Limited, Nemko Recognized	13–227
TPS2056	2	80	0.25	0.44	2.7 – 5.5	Yes	Yes	Pos	Current–Limited, Nemko Recognized	13–247
TPS2057	3	80	0.25	0.44	2.7 – 5.5	Yes	Yes	Pos	Current–Limited, Nemko Recognized	13–267
TPS2058	4	80	0.25	0.44	2.7 – 5.5	Yes	Yes	Pos	Current–Limited, Nemko Recognized	13–289

PMOS DISTRIBUTION SWITCHES

Device	Number of FETs	$r_{DS(on)}$ (typ) (mΩ)	V_{DS} (max) (V)	I_{DD} (max) (A)	ESD Circuitry	Description	Page No.
TPS1100	1	180	15	1.6	Yes	High–Side PMOS	13–3
TPS1101	1	90	15	2.3	Yes	High–Side PMOS	13–13
TPS1120	2	180	15	1.17	Yes	High–Side PMOS	13–23

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LED DRIVERS

Device	V_{ref} (V)	I_Z (min) (μA)	I_Z (max) (mA)	V_O (min) (V)	V_O (max) (V)	Tolerance (%)	V_I (max) (V)	Temp Coeff (typ) (ppm/°C)	Description	Page No.
TLC5904	2.5	1000	100	Vref	36	0.4	36	30	LED Driver	14–3

VOLTAGE RAIL SPLITTERS

Device	I_{CC} (μA)	V_{CC} (V)	I_O (mA)	V_O (min) (V)	V_O (max) (V)	Temp Coeff (typ) (ppm/°C)	Description	Page No.
TLE2426	280	4 – 40	20	1.98	20.2	25	Rail Splitter Precision Virtual Ground	15–3

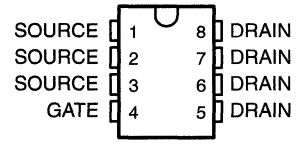
SPECIAL FUNCTIONS

Device	V_{ref} (V)	I_Z (min) (μA)	I_Z (max) (μA)	V_O (min) (V)	Input Clamp Current (mA)	Settling Time (μs)	Description	Page No.
TL7726	4.5		60		25	30	Hex Clamping Circuit	16–3
TL2218–285		–20.5		2.5			Excalibur Current-Mode SCSI Terminator	16–7

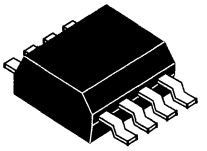
SLVS078C – DECEMBER 1993 – REVISED AUGUST 1995

- **Low $r_{DS(on)}$ . . . 0.18 Ω Typ at V_{GS} = −10 V**
- **3 V Compatible**
- **Requires No External V_{CC}**
- **TTL and CMOS Compatible Inputs**
- **$V_{GS(th)}$ = −1.5 V Max**
- **Available in Ultrathin TSSOP Package (PW)**
- **ESD Protection Up to 2 kV Per MIL-STD-883C, Method 3015**

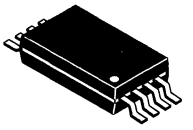
D OR PW PACKAGE
(TOP VIEW)



D PACKAGE



PW PACKAGE

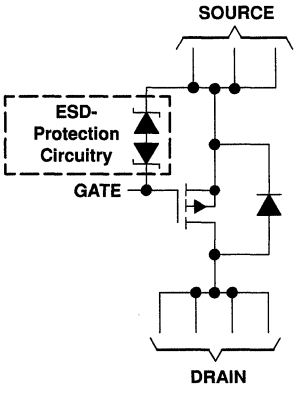


description

The TPS1100 is a single P-channel enhancement-mode MOSFET. The device has been optimized for 3-V or 5-V power distribution in battery-powered systems by means of Texas Instruments LinBiCMOS™ process. With a maximum $V_{GS(th)}$ of −1.5 V and an I_{DSS} of only 0.5 μA, the TPS1100 is the ideal high-side switch for low-voltage, portable battery-management systems where maximizing battery life is a primary concern. The low $r_{DS(on)}$ and excellent ac characteristics (rise time 10 ns typical) make the TPS1100 the logical choice for low-voltage switching applications such as power switches for pulse-width-modulated (PWM) controllers or motor/bridge drivers.

The ultrathin thin shrink small-outline package or TSSOP (PW) version with its smaller footprint and reduction in height fits in places where other P-channel MOSFETs cannot. The size advantage is especially important where board real estate is at a premium and height restrictions do not allow for a small-outline integrated circuit (SOIC) package.

schematic



NOTE A. For all applications, all source pins should be connected and all drain pins should be connected.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		CHIP FORM (Y)
	SMALL OUTLINE (D)	PLASTIC DIP (P)	
−40°C to 85°C	TPS1100D	TPS1100PWLE	TPS1100Y

The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS1100DR). The PW package is available only left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TPS1100PWLE). The chip form is tested at 25°C.

Caution. This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.

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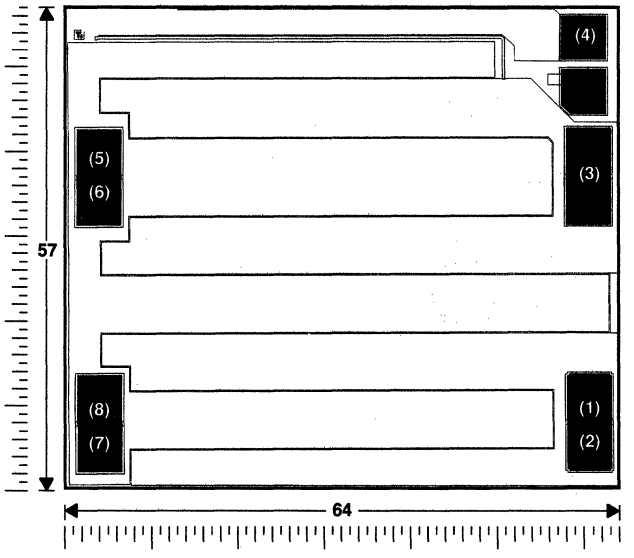
description (continued)

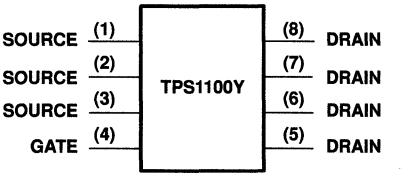
Such applications include notebook computers, personal digital assistants (PDAs), cellular telephones, and PCMCIA cards. For existing designs, the D-packaged version has a pinout common with other p-channel MOSFETs in SOIC packages.

TPS1100Y chip information

This chip, when properly assembled, displays characteristics similar to the TPS1100. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

					UNIT
Drain-to-source voltage, V_{DS}				–15	V
Gate-to-source voltage, V_{GS}				2 or –15	V
Continuous drain current (T_J = 150°C), I_D‡	V_{GS} = –2.7 V	D package	T_A = 25°C	±0.41	A
			T_A = 125°C	±0.28	
		PW package	T_A = 25°C	±0.4	
			T_A = 125°C	±0.23	
	V_{GS} = –3 V	D package	T_A = 25°C	±0.6	
			T_A = 125°C	±0.33	
		PW package	T_A = 25°C	±0.53	
			T_A = 125°C	±0.27	
	V_{GS} = –4.5 V	D package	T_A = 25°C	±1	
			T_A = 125°C	±0.47	
		PW package	T_A = 25°C	±0.81	
			T_A = 125°C	±0.37	
	V_{GS} = –10 V	D package	T_A = 25°C	±1.6	
			T_A = 125°C	±0.72	
		PW package	T_A = 25°C	±1.27	
			T_A = 125°C	±0.58	
Pulsed drain current, I_D‡			T_A = 25°C	±7	A
Continuous source current (diode conduction), I_S			T_A = 25°C	–1	A
Storage temperature range, T_{stg}				–55 to 150	°C
Operating junction temperature range, T_J				–40 to 150	°C
Operating free-air temperature range, T_A				–40 to 125	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds				260	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Maximum values are calculated using a derating factor based on $R_{\theta JA}$ = 158°C/W for the D package and $R_{\theta JA}$ = 248°C/W for the PW package. These devices are mounted on a FR4 board with no special thermal considerations.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	791 mW	6.33 mW/°C	506 mW	411 mW	158 mW
PW	504 mW	4.03 mW/°C	323 mW	262 mW	101 mW

‡ Maximum values are calculated using a derating factor based on $R_{\theta JA}$ = 158°C/W for the D package and $R_{\theta JA}$ = 248°C/W for the PW package. These devices are mounted on an FR4 board with no special thermal considerations when tested.

electrical characteristics at T_J = 25°C (unless otherwise noted)

static

PARAMETER		TEST CONDITIONS			TPS1100			TPS1100Y			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS},	I_D = −250 µA		−1	−1.25	−1.50		−1.25		V
V_{SD}	Source-to-drain voltage (diode-forward voltage)†	I_S = −1 A,	V_{GS} = 0 V			−0.9			−0.9		V
I_{GSS}	Reverse gate current, drain short circuited to source	V_{DS} = 0 V,	V_{GS} = −12 V				±100				nA
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = −12 V,	V_{GS} = 0 V	T_J = 25°C			−0.5				µA
				T_J = 125°C			−10				
$r_{DS(on)}$	Static drain-to-source on-state resistance†	V_{GS} = −10 V	I_D = −1.5 A			180			180		mΩ
		V_{GS} = −4.5 V	I_D = −0.5 A			291	400		291		
		V_{GS} = −3 V	I_D = −0.2 A			476	700		476		
		V_{GS} = −2.7 V				606	850		606		
g_{fs}	Forward transconductance†	V_{DS} = −10 V,	I_D = −2 A			2.5			2.5		S

† Pulse test: pulse duration ≤ 300 µs, duty cycle ≤ 2%

dynamic

PARAMETER		TEST CONDITIONS			TPS1100, TPS1100Y			UNIT
					MIN	TYP	MAX	
Q_g	Total gate charge	V_{DS} = −10 V,	V_{GS} = −10 V,	I_D = −1 A		5.45		nC
Q_{gs}	Gate-to-source charge					0.87		
Q_{gd}	Gate-to-drain charge					1.4		
$t_{d(on)}$	Turn-on delay time	V_{DD} = −10 V, R_G = 6 Ω,	R_L = 10 Ω, See Figures 1 and 2	I_D = −1 A,		4.5		ns
$t_{d(off)}$	Turn-off delay time					13		ns
t_r	Rise time					10		ns
t_f	Fall time					2		
$t_{rr(SD)}$	Source-to-drain reverse recovery time	I_F = 5.3 A,	di/dt = 100 A/µs			16		

PARAMETER MEASUREMENT INFORMATION

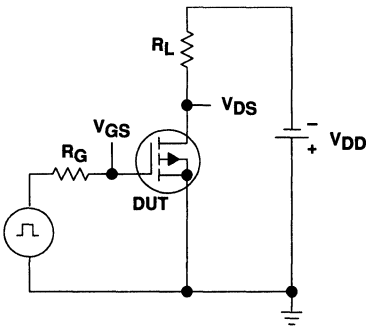


Figure 1. Switching-Time Test Circuit

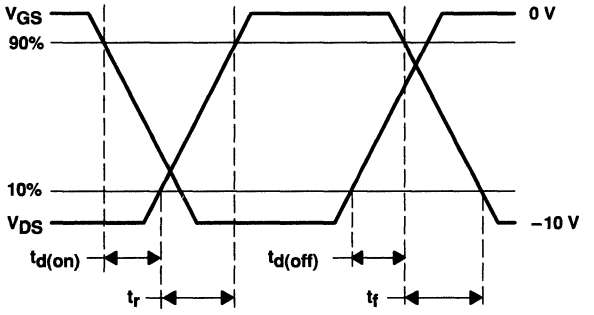


Figure 2. Switching-Time Waveforms

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Drain current	vs Drain-to-source voltage	3
Drain current	vs Gate-to-source voltage	4
Static drain-to-source on-state resistance	vs Drain current	5
Capacitance	vs Drain-to-source voltage	6
Static drain-to-source on-state resistance (normalized)	vs Junction temperature	7
Source-to-drain diode current	vs Source-to-drain voltage	8
Static drain-to-source on-state resistance	vs Gate-to-source voltage	9
Gate-to-source threshold voltage	vs Junction temperature	10
Gate-to-source voltage	vs Gate charge	11

TYPICAL CHARACTERISTICS

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

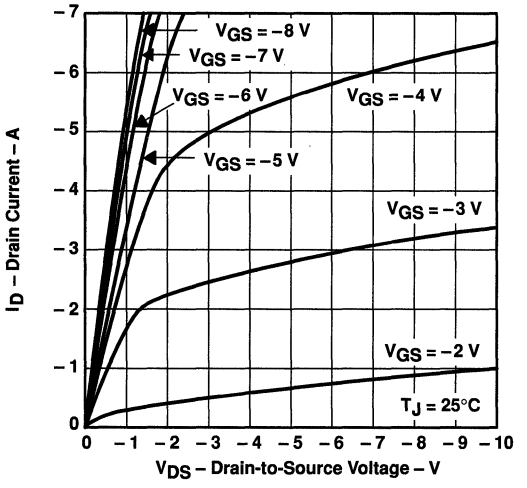


Figure 3

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

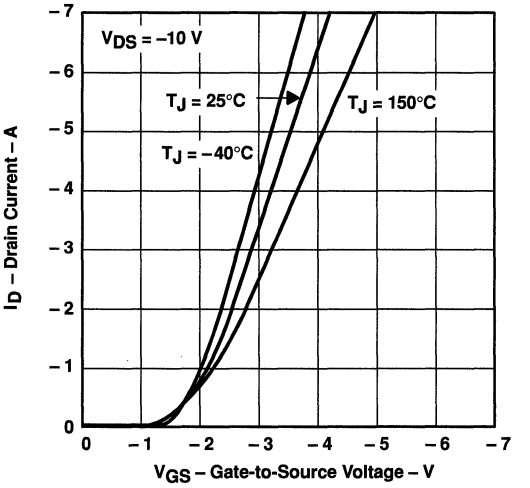


Figure 4

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

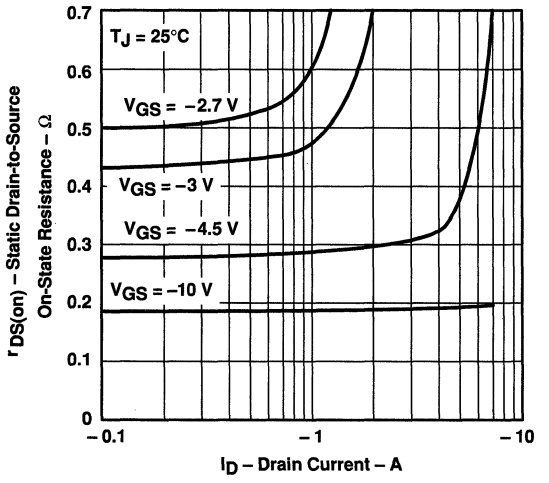
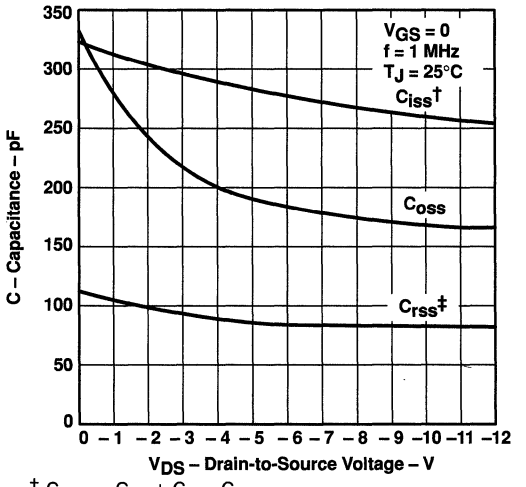


Figure 5

CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE



† $C_{iss} = C_{gs} + C_{gd}$, $C_{ds(shorted)}$

‡ $C_{rss} = C_{gd}$, $C_{oss} = C_{ds} + \frac{C_{gs}\,C_{gd}}{C_{gs} + C_{gd}} \approx C_{ds} + C_{gd}$

Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE
ON-STATE RESISTANCE (NORMALIZED)
vs
JUNCTION TEMPERATURE

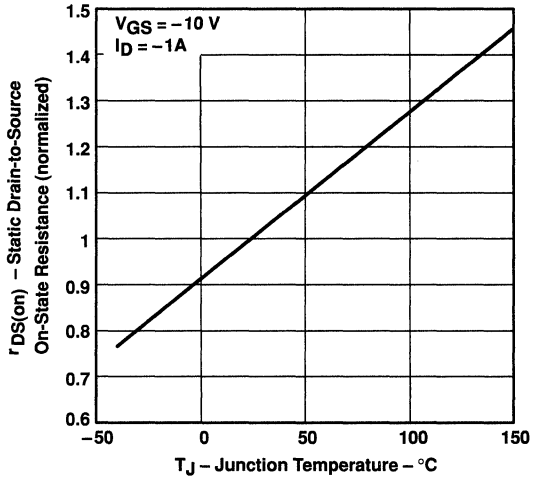


Figure 7

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

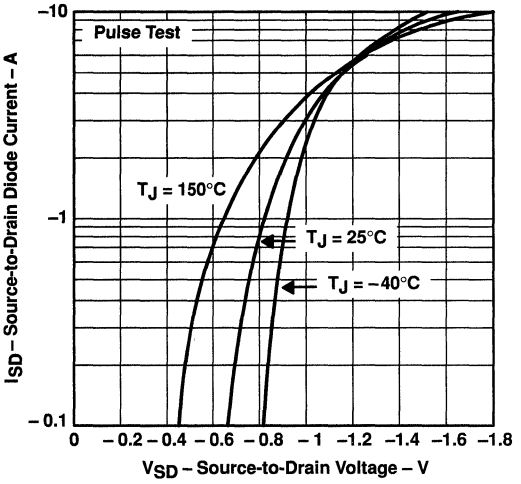


Figure 8

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
GATE-TO-SOURCE VOLTAGE

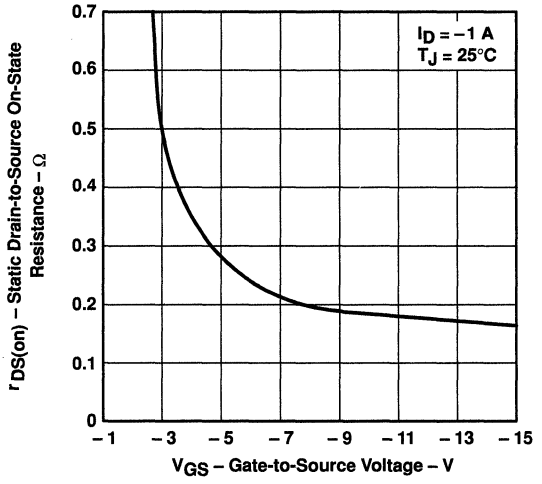


Figure 9

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

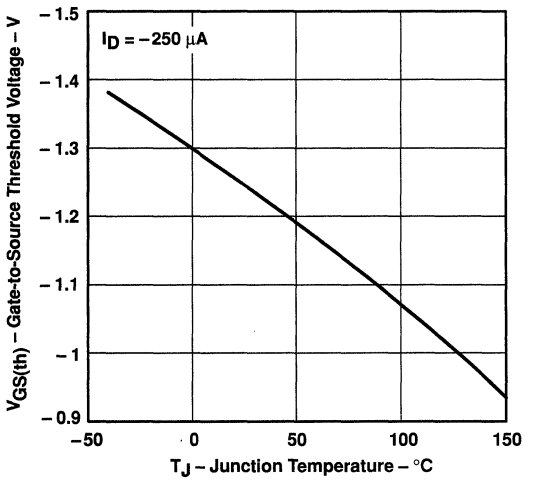


Figure 10

TYPICAL CHARACTERISTICS

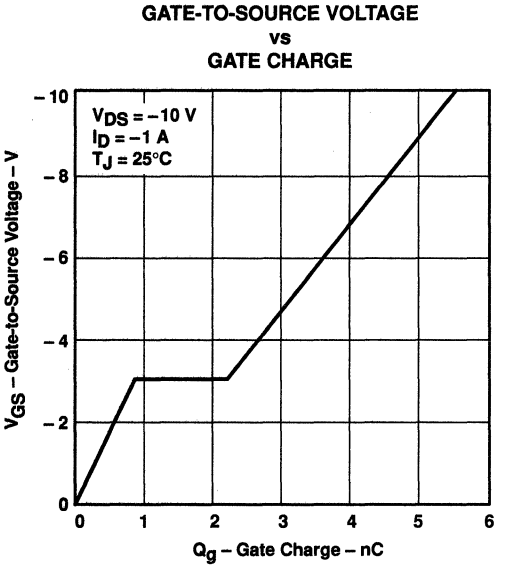


Figure 11

THERMAL INFORMATION

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

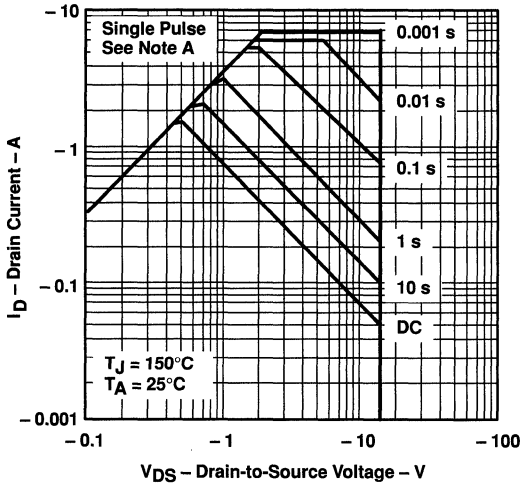


Figure 12

TRANSIENT JUNCTION-TO-AMBIENT
THERMAL IMPEDANCE
vs
PULSE DURATION

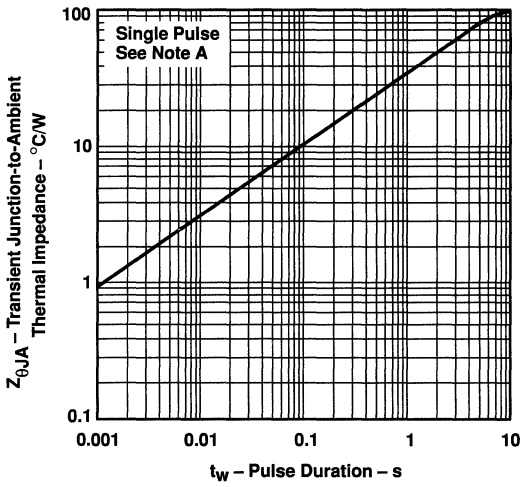


Figure 13

NOTE A. Values are for the D package and are FR4-board mounted only.

APPLICATION INFORMATION

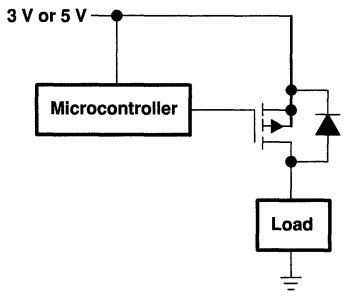


Figure 14. Notebook Load Management

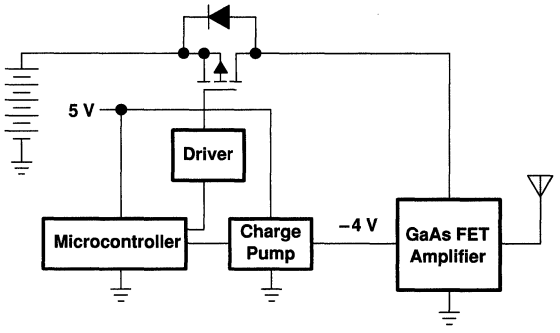
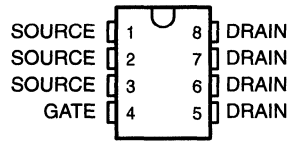


Figure 15. Cellular Phone Output Drive

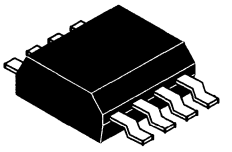
SLVS079C – DECEMBER 1993 – REVISED AUGUST 1995

- **Low $r_{DS(on)}$ . . . 0.09 Ω Typ at V_{GS} = −10 V**
- **3 V Compatible**
- **Requires No External V_{CC}**
- **TTL and CMOS Compatible Inputs**
- **$V_{GS(th)}$ = −1.5 V Max**
- **Available in Ultrathin TSSOP Package (PW)**
- **ESD Protection Up to 2 kV per MIL-STD-883C, Method 3015**

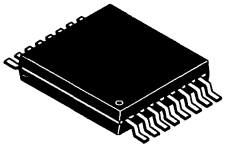
D PACKAGE
(TOP VIEW)



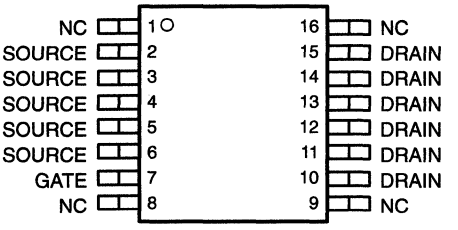
D PACKAGE



PW PACKAGE



PW PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TPS1101 is a single, low-$r_{DS(on)}$, P-channel, enhancement-mode MOSFET. The device has been optimized for 3-V or 5-V power distribution in battery-powered systems by means of the Texas Instruments LinBiCMOS™ process. With a maximum $V_{GS(th)}$ of −1.5 V and an I_{DSS} of only 0.5 µA, the TPS1101 is the ideal high-side switch for low-voltage, portable battery-management systems where maximizing battery life is a primary concern. The low $r_{DS(on)}$ and excellent ac characteristics (rise time 5.5 ns typical) of the TPS1101 make it the logical choice for low-voltage switching applications such as power switches for pulse-width-modulated (PWM) controllers or motor/bridge drivers.

The ultrathin thin shrink small-outline package or TSSOP (PW) version fits in height-restricted places where other P-channel MOSFETs cannot. The size advantage is especially important where board height restrictions do not allow for an small-outline integrated circuit (SOIC) package. Such applications include notebook computers, personal digital assistants (PDAs), cellular telephones, and PCMCIA cards. For existing designs, the D-packaged version has a pinout common with other P-channel MOSFETs in SOIC packages.

AVAILABLE OPTIONS

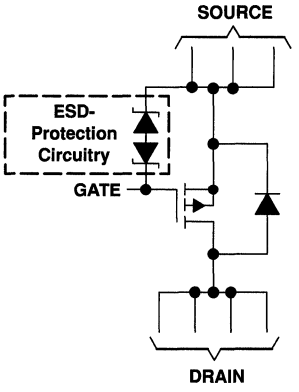
T_J	PACKAGED DEVICES†		CHIP FORM (Y)
	SMALL OUTLINE (D)	TSSOP (PW)	
−40°C to 150°C	TPS1101D	TPS1101PWLE	TPS1101Y

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS1101DR). The PW package is only available left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TPS1101PWLE). The chip form is tested at 25°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LinBiCMOS is a trademark of Texas Instruments Incorporated.

schematic

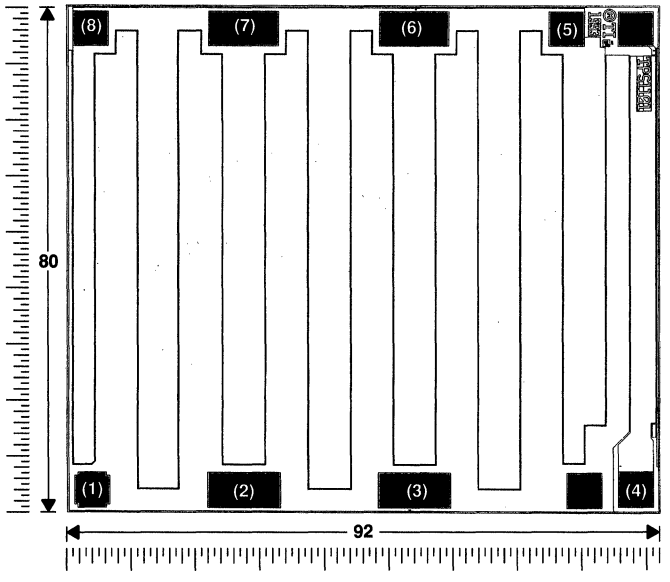


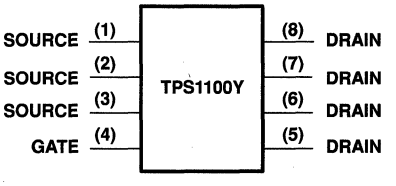
NOTE B. For all applications, all source terminals should be connected and all drain terminals should be connected.

TPS1101Y chip information

This chip, when properly assembled, displays characteristics similar to the TPS1101. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

					UNIT
Drain-to-source voltage, V_{DS}				−15	V
Gate-to-source voltage, V_{GS}				2 or −15	V
Continuous drain current (T_J = 150°C), I_D‡	V_{GS} = −2.7 V	D package	T_A = 25°C	±0.62	A
			T_A = 125°C	±0.39	
		PW package	T_A = 25°C	±0.61	
			T_A = 125°C	±0.38	
	V_{GS} = −3 V	D package	T_A = 25°C	±0.88	
			T_A = 125°C	±0.47	
		PW package	T_A = 25°C	±0.86	
			T_A = 125°C	±0.45	
	V_{GS} = −4.5 V	D package	T_A = 25°C	±1.52	
			T_A = 125°C	±0.71	
		PW package	T_A = 25°C	±1.44	
			T_A = 125°C	±0.67	
	V_{GS} = −10 V	D package	T_A = 25°C	±2.30	
			T_A = 125°C	±1.04	
		PW package	T_A = 25°C	±2.18	
			T_A = 125°C	±0.98	
Pulsed drain current, I_D‡			T_A = 25°C	±10	A
Continuous source current (diode conduction), I_S			T_A = 25°C	−1.1	A
Storage temperature range, T_{stg}				−55 to 150	°C
Operating junction temperature range, T_J				−40 to 150	°C
Operating free-air temperature range, T_A				−40 to 125	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds				260	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Maximum values are calculated using a derating factor based on $R_{\theta JA}$ = 158°C/W for the D package and $R_{\theta JA}$ = 176°C/W for the PW package. These devices are mounted on an FR4 board with no special thermal considerations.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	791 mW	6.33 mW/°C	506 mW	411 mW	158 mW
PW	710 mW	5.68 mW/°C	454 mW	369 mW	142 mW

‡ Maximum values are calculated using a derating factor based on $R_{\theta JA}$ = 158°C/W for the D package and $R_{\theta JA}$ = 176°C/W for the PW package. These devices are mounted on an FR4 board with no special thermal considerations.

electrical characteristics at T_J = 25°C (unless otherwise noted)

static

PARAMETER		TEST CONDITIONS			TPS1101 MIN	TPS1101 TYP	TPS1101 MAX	TPS1101Y MIN	TPS1101Y TYP	TPS1101Y MAX	UNIT
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS},	I_D = −250 µA		−1	−1.25	−1.5		−1.25		V
V_{SD}	Source-to-drain voltage (diode-forward voltage)†	I_S = −1 A,	V_{GS} = 0 V			−1.04			−1.04		V
I_{GSS}	Reverse gate current, drain short circuited to source	V_{DS} = 0 V,	V_{GS} = −12 V				±100				nA
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = −12 V,	V_{GS} = 0 V	T_J = 25°C			−0.5				µA
				T_J = 125°C			−10				
$r_{DS(on)}$	Static drain-to-source on-state resistance†	V_{GS} = −10 V	I_D = −2.5 A			90			90		mΩ
		V_{GS} = −4.5 V	I_D = −1.5 A			134	190		134		
		V_{GS} = −3 V	I_D = −0.5 A			198	310		198		
		V_{GS} = −2.7 V				232	400		232		
g_{fs}	Forward transconductance†	V_{DS} = −10 V,	I_D = −2 A			4.3			4.3		S

† Pulse test: pulse duration ≤ 300 µs, duty cycle ≤ 2%

dynamic

PARAMETER		TEST CONDITIONS			TPS1101, TPS1101Y MIN	TPS1101, TPS1101Y TYP	TPS1101, TPS1101Y MAX	UNIT
Q_g	Total gate charge	V_{DS} = −10 V,	V_{GS} = −10 V,	I_D = −1 A		11.25		nC
Q_{gs}	Gate-to-source charge					1.5		
Q_{gd}	Gate-to-drain charge					2.6		
$t_{d(on)}$	Turn-on delay time	V_{DD} = −10 V,	R_L = 10 Ω,	I_D = −1 A,		6.5		ns
$t_{d(off)}$	Turn-off delay time	R_G = 6 Ω,	See Figures 1 and 2			19		ns
t_r	Rise time					5.5		ns
t_f	Fall time					13		
$t_{rr(SD)}$	Source-to-drain reverse recovery time	I_F = 5.3 A,	di/dt = 100 A/µs			16		

PARAMETER MEASUREMENT INFORMATION

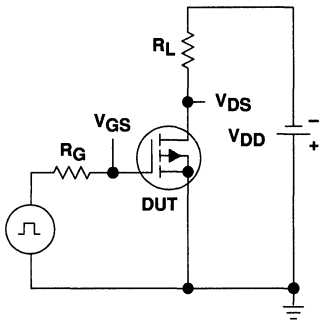


Figure 1. Switching-Time Test Circuit

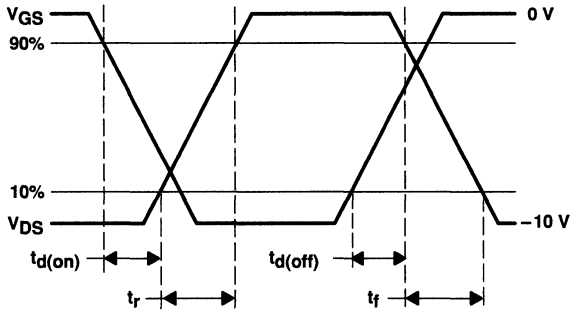


Figure 2. Switching-Time Waveforms

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Drain current	vs Drain-to-source voltage	3
Drain current	vs Gate-to-source voltage	4
Static drain-to-source on-state resistance	vs Drain current	5
Capacitance	vs Drain-to-source voltage	6
Static drain-to-source on-state resistance (normalized)	vs Junction temperature	7
Source-to-drain diode current	vs Source-to-drain voltage	8
Static drain-to-source on-state resistance	vs Gate-to-source voltage	9
Gate-to-source threshold voltage	vs Junction temperature	10
Gate-to-source voltage	vs Gate charge	11

TYPICAL CHARACTERISTICS

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

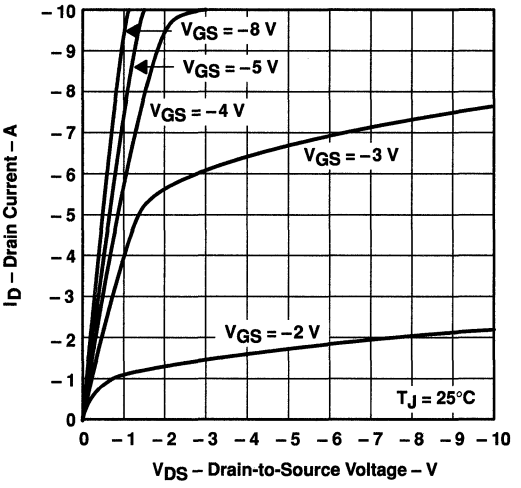


Figure 3

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

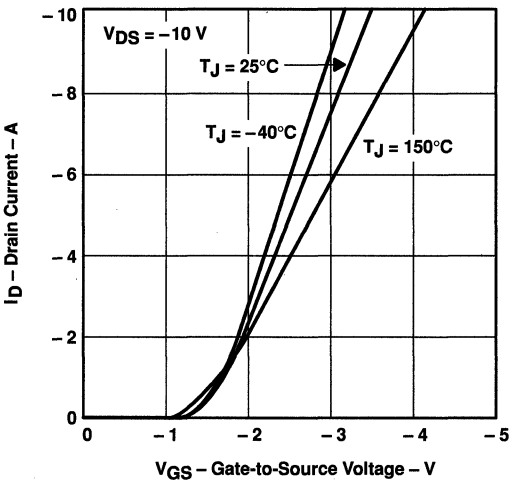


Figure 4

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

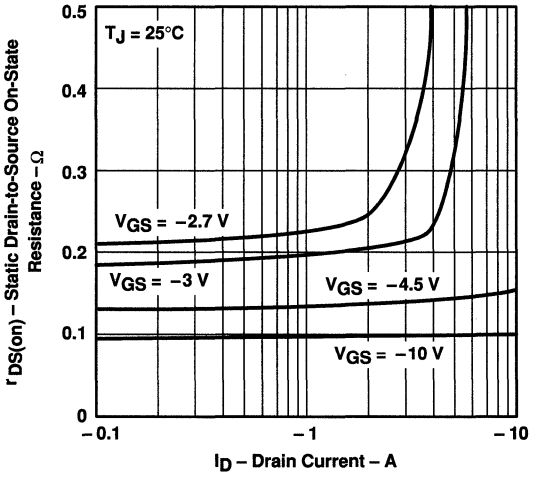
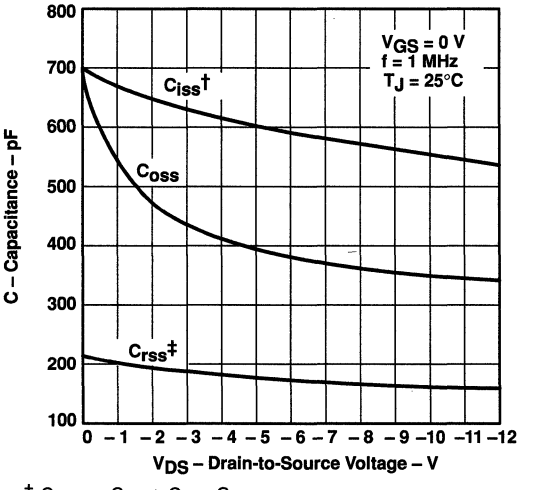


Figure 5

CAPACITANCE†
vs
DRAIN-TO-SOURCE VOLTAGE



† $C_{iss} = C_{gs} + C_{gd}$, $C_{ds(shorted)}$

‡ $C_{rss} = C_{gd}$, $C_{oss} = C_{ds} + \dfrac{C_{gs}\,C_{gd}}{C_{gs} + C_{gd}} \approx C_{ds} + C_{gd}$

Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE
ON-STATE RESISTANCE (NORMALIZED)
vs
JUNCTION TEMPERATURE

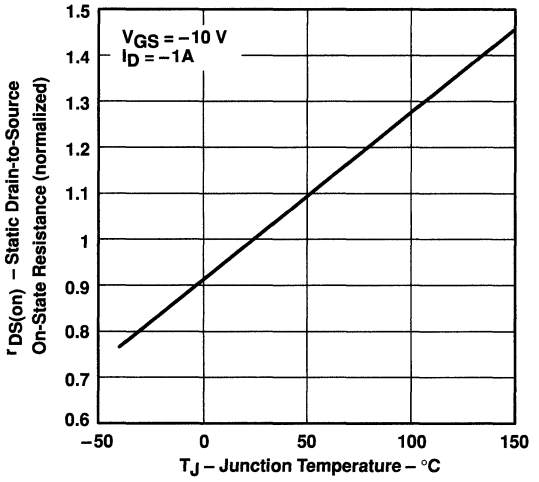


Figure 7

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

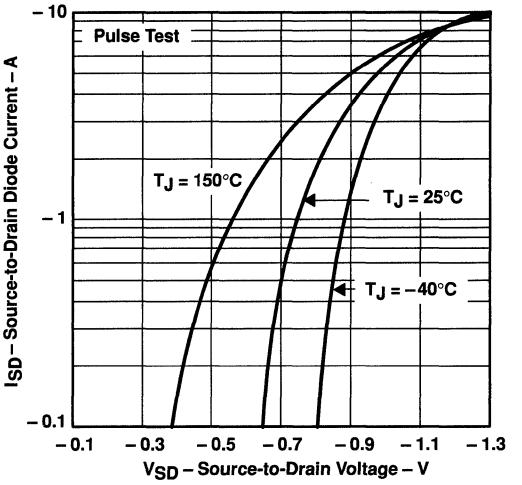


Figure 8

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
GATE-TO-SOURCE VOLTAGE

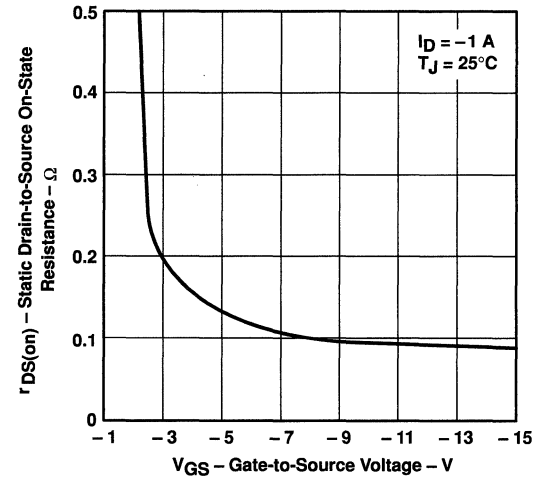


Figure 9

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

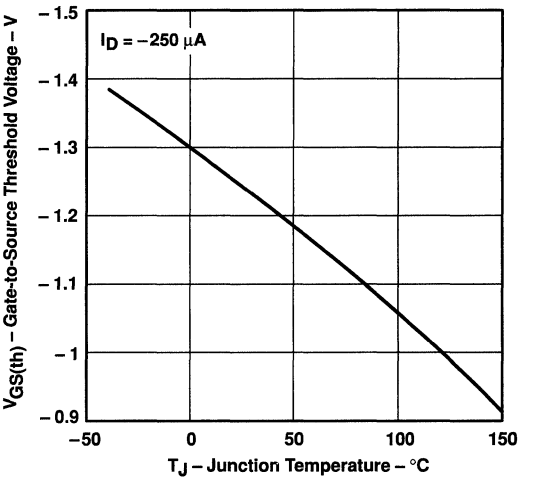


Figure 10

TYPICAL CHARACTERISTICS

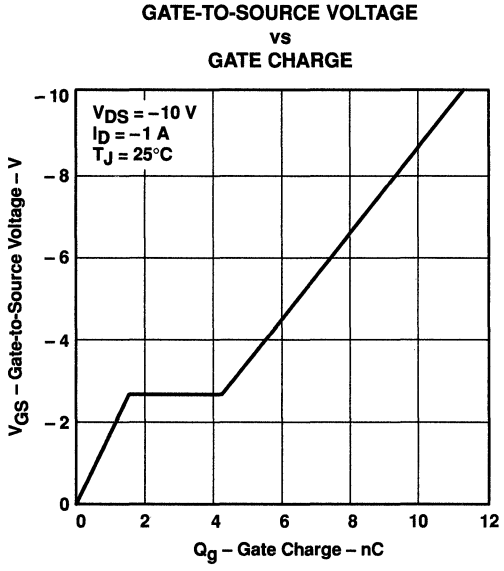
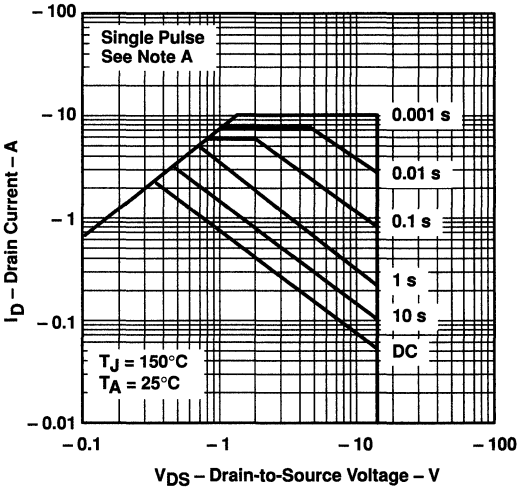


Figure 11

THERMAL INFORMATION

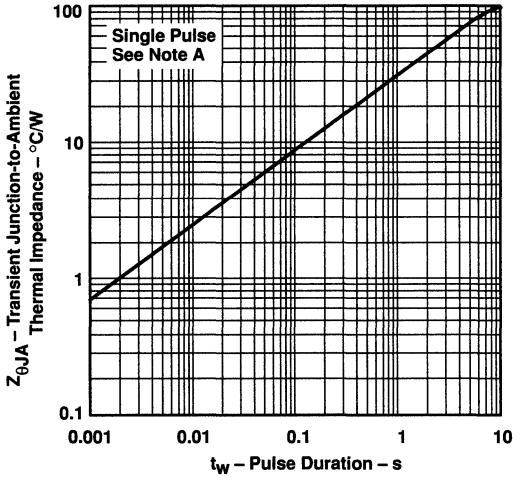
DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE



NOTE A. Values are for the D package and are FR4-board-mounted only.

Figure 12

TRANSIENT JUNCTION-TO-AMBIENT
THERMAL IMPEDANCE
vs
PULSE DURATION



NOTE A. Values are for the D package and are FR4-board-mounted only.

Figure 13

APPLICATION INFORMATION

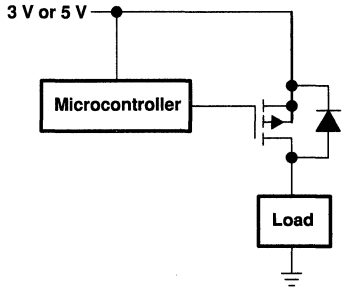


Figure 14. Notebook Load Management

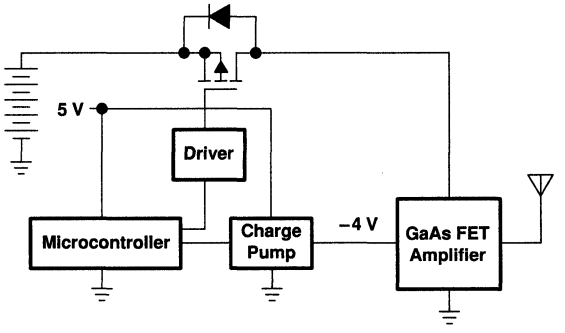


Figure 15. Cellular Phone Output Drive

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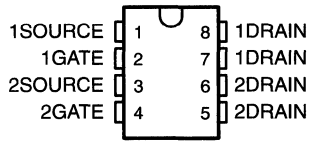
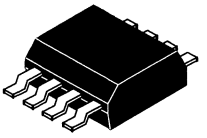
- **Low $r_{DS(on)}$ . . . 0.18 Ω at V_{GS} = –10 V**
- **3-V Compatible**
- **Requires No External V_{CC}**
- **TTL and CMOS Compatible Inputs**
- **$V_{GS(th)}$ = –1.5 V Max**
- **ESD Protection Up to 2 kV per MIL-STD-883C, Method 3015**

D PACKAGE
(TOP VIEW)





description

The TPS1120 incorporates two independent p-channel enhancement-mode MOSFETs that have been optimized, by means of the Texas Instruments LinBiCMOS™ process, for 3-V or 5-V power distribution in battery-powered systems. With a maximum $V_{GS(th)}$ of –1.5 V and an I_{DSS} of only 0.5 µA, the TPS1120 is the ideal high-side switch for low-voltage portable battery-management systems, where maximizing battery life is a primary concern. Because portable equipment is potentially subject to electrostatic discharge (ESD), the MOSFETs have built-in circuitry for 2-kV ESD protection. End equipment for the TPS1120 includes notebook computers, personal digital assistants (PDAs), cellular telephones, bar-code scanners, and PCMCIA cards. For existing designs, the TPS1120D has a pinout common with other p-channel MOSFETs in small-outline integrated circuit SOIC packages.

The TPS1120 is characterized for an operating junction temperature range, T_J, from –40°C to 150°C.

AVAILABLE OPTIONS

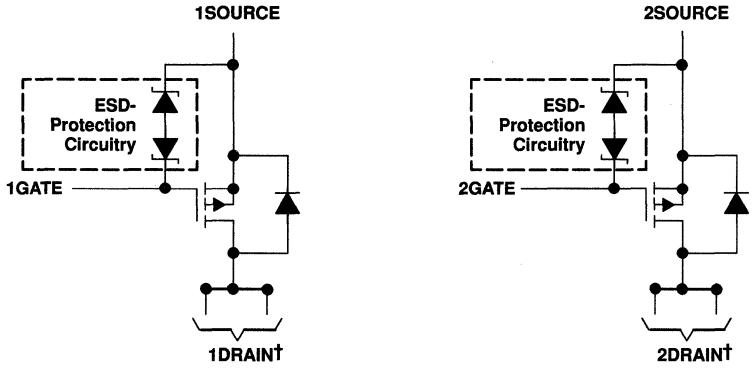
T_J	PACKAGED DEVICES†	CHIP FORM (Y)
	SMALL OUTLINE (D)	
–40°C to 150°C	TPS1120D	TPS1120Y

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS1120DR). The chip form is tested at 25°C.

Caution. This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.

LinBiCMS is a trademark of Texas Instruments Incorporated.

schematic

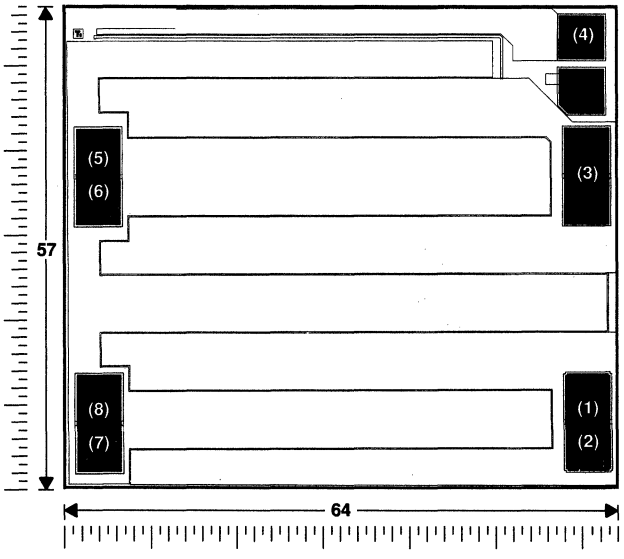


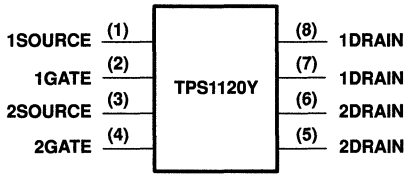
† For all applications, both drain pins for each device should be connected.

TPS1120Y chip information

This chip, when properly assembled, displays characteristics similar to the TPS1120C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

				UNIT
Drain-to-source voltage, V_{DS}			–15	V
Gate-to-source voltage, V_{GS}			2 or –15	V
Continuous drain current, each device (T_J = 150°C), I_D	V_{GS} = –2.7 V	T_A = 25°C	±0.39	A
		T_A = 125°C	±0.21	
	V_{GS} = –3 V	T_A = 25°C	±0.5	
		T_A = 125°C	±0.25	
	V_{GS} = –4.5 V	T_A = 25°C	±0.74	
		T_A = 125°C	±0.34	
	V_{GS} = –10 V	T_A = 25°C	±1.17	
		T_A = 125°C	±0.53	
Pulse drain current, I_D		T_A = 25°C	±7	A
Continuous source current (diode conduction), I_S		T_A = 25°C	–1	A
Continuous total power dissipation		See Dissipation Rating Table		
Storage temperature range, T_{stg}			–55 to 150	°C
Operating junction temperature range, T_J			–40 to 150	°C
Operating free-air temperature range, T_A			–40 to 125	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	840 mW	6.71 mW/°C	538 mW	437 mW	169 mW

‡ Maximum values are calculated using a derating factor based on $R_{\theta JA}$ = 149°C/W for the package. These devices are mounted on an FR4 board with no special thermal considerations.

electrical characteristics at T_J = 25°C (unless otherwise noted)

static

PARAMETER		TEST CONDITIONS		TPS1120 MIN	TPS1120 TYP	TPS1120 MAX	UNIT
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS},	I_D = −250 µA	−1	−1.25	−1.50	V
V_{SD}	Source-to-drain voltage (diode forward voltage)†	I_S = −1 A,	V_{GS} = 0 V		−0.9		V
I_{GSS}	Reverse gate current, drain short circuited to source	V_{DS} = 0 V,	V_{GS} = −12 V			±100	nA
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = −12 V, V_{GS} = 0 V	T_J = 25°C			−0.5	µA
			T_J = 125°C			−10	
$r_{DS(on)}$	Static drain-to-source on-state resistance†	V_{GS} = −10 V	I_D = −1.5 A		180		mΩ
		V_{GS} = −4.5 V	I_D = −0.5 A		291	400	
		V_{GS} = −3 V	I_D = −0.2 A		476	700	
		V_{GS} = −2.7 V			606	850	
g_{fs}	Forward transconductance†	V_{DS} = −10 V,	I_D = −2 A		2.5		S

† Pulse test: pulse width ≤ 300 µs, duty cycle ≤ 2%

static

PARAMETER		TEST CONDITIONS		TPS1120Y MIN	TPS1120Y TYP	TPS1120Y MAX	UNIT
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS},	I_D = −250 µA		−1.25		V
V_{SD}	Source-to-drain voltage (diode forward voltage)†	I_S = −1 A,	V_{GS} = 0 V		−0.9		V
$r_{DS(on)}$	Static drain-to-source on-state resistance†	V_{GS} = −10 V	I_D = −1.5 A		180		mΩ
		V_{GS} = −4.5 V	I_D = −0.5 A		291		
		V_{GS} = −3 V	I_D = −0.2 A		476		
		V_{GS} = −2.7 V			606		
g_{fs}	Forward transconductance†	V_{DS} = −10 V,	I_D = −2 A		2.5		S

† Pulse test: pulse width ≤ 300 µs, duty cycle ≤ 2%

dynamic

PARAMETER		TEST CONDITIONS			TPS1120, TPS1120Y MIN	TPS1120, TPS1120Y TYP	TPS1120, TPS1120Y MAX	UNIT
Q_g	Total gate charge	V_{DS} = −10 V,	V_{GS} = −10 V,	I_D = −1 A		5.45		nC
Q_{gs}	Gate-to-source charge					0.87		
Q_{gd}	Gate-to-drain charge					1.4		
$t_{d(on)}$	Turn-on delay time	V_{DD} = −10 V, R_G = 6 Ω,	R_L = 10 Ω, See Figures 1 and 2	I_D = −1 A,		4.5		ns
$t_{d(off)}$	Turn-off delay time					13		ns
t_r	Rise time					10		ns
t_f	Fall time					2		
$t_{rr(SD)}$	Source-to-drain reverse recovery time	I_F = 5.3 A,	di/dt = 100 A/µs			16		

PARAMETER MEASUREMENT INFORMATION

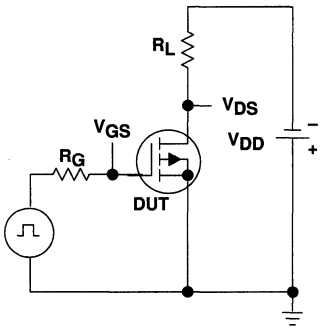


Figure 1. Switching-Time Test Circuit

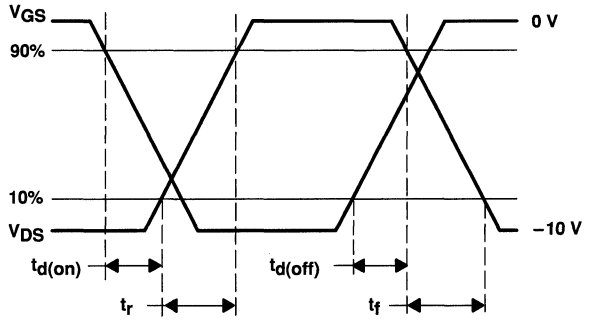


Figure 2. Switching-Time Waveforms

TYPICAL CHARACTERISTICS†

Table of Graphs

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

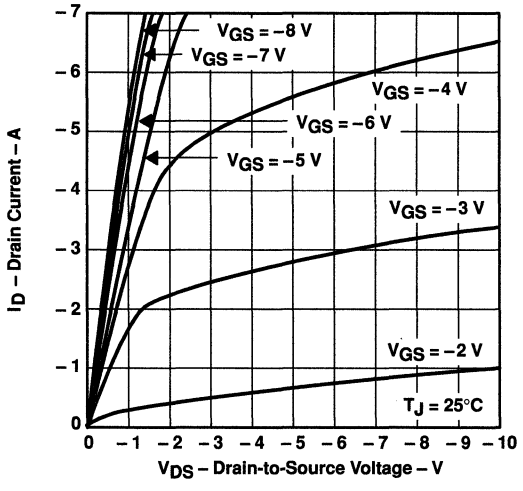


Figure 3

DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

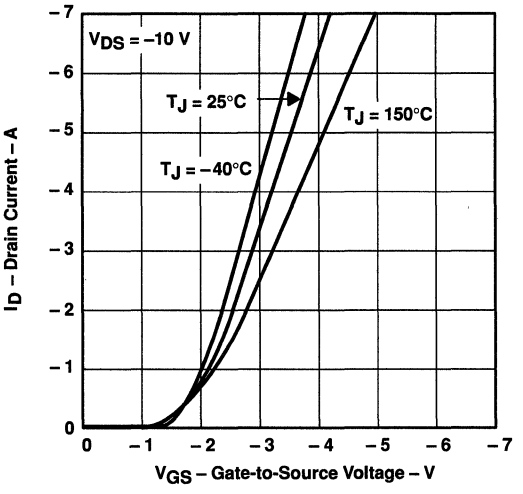


Figure 4

† All characteristics data applies for each independent MOSFET incorporated on the TPS1120.

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

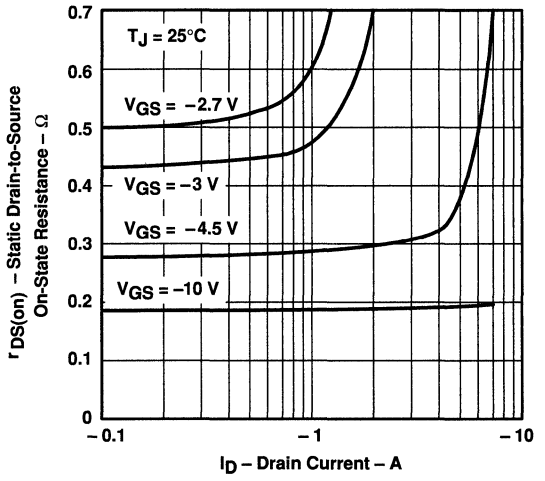
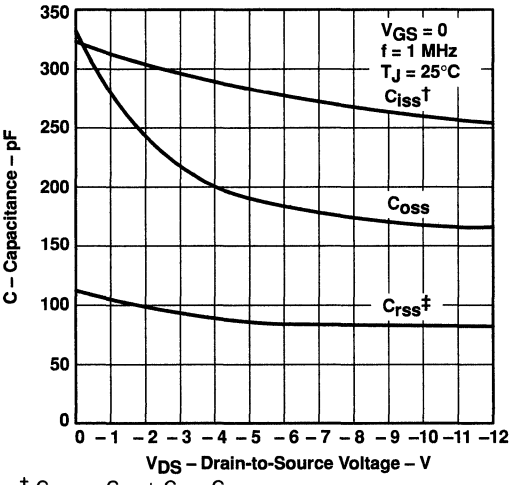


Figure 5

CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE



† $C_{iss} = C_{gs} + C_{gd}$, $C_{ds(shorted)}$

‡ $C_{rss} = C_{gd}$, $C_{oss} = C_{ds} + \frac{C_{gs}\,C_{gd}}{C_{gs} + C_{gd}} \approx C_{ds} + C_{gd}$

Figure 6

STATIC DRAIN-TO-SOURCE
ON-STATE RESISTANCE (NORMALIZED)
vs
JUNCTION TEMPERATURE

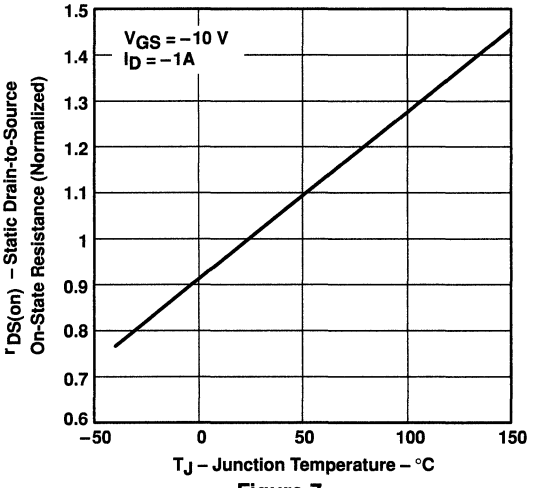


Figure 7

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE

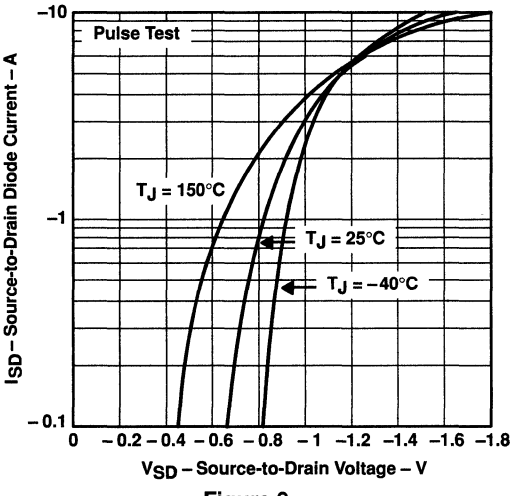


Figure 8

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
GATE-TO-SOURCE VOLTAGE

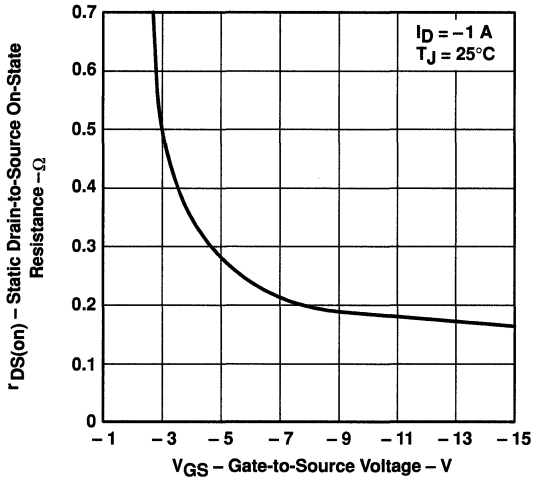


Figure 9

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

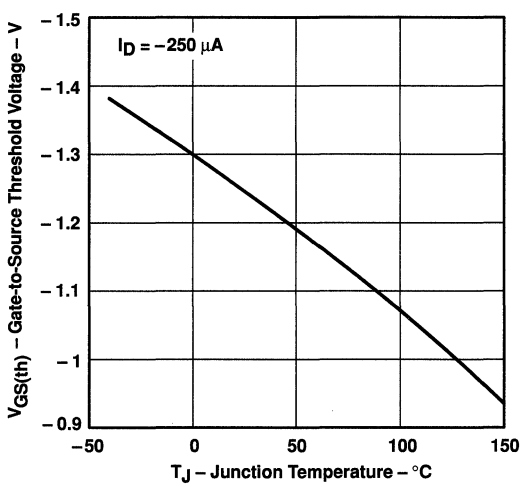


Figure 10

GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

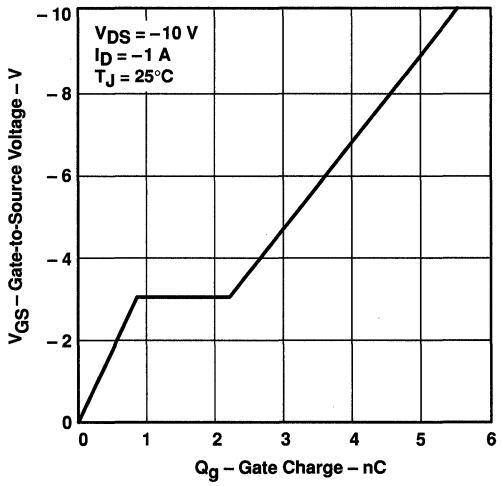
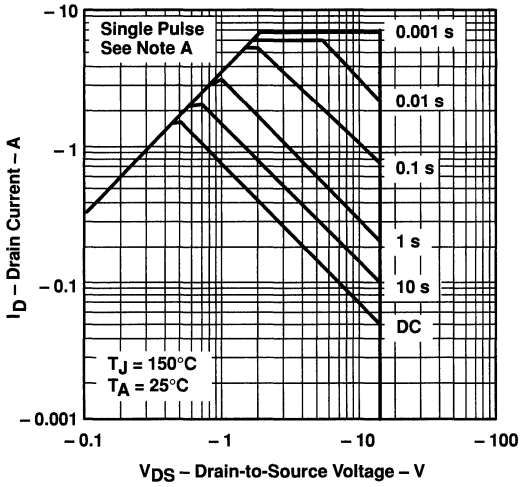


Figure 11

THERMAL INFORMATION

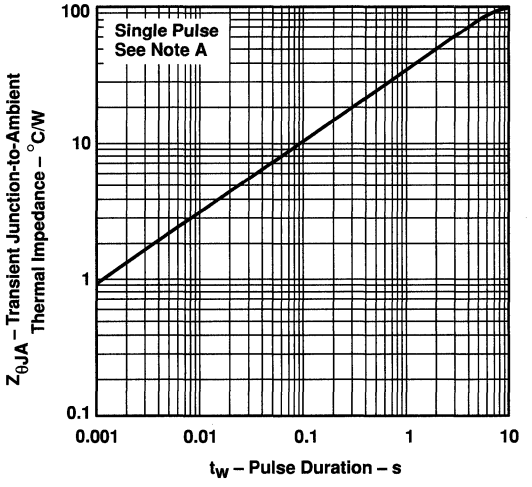
**DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE**



NOTE A: FR4-board-mounted only

Figure 12

**TRANSIENT JUNCTION-TO-AMBIENT
THERMAL IMPEDANCE
vs
PULSE DURATION**



NOTE A: FR4-board-mounted only

Figure 13

THERMAL INFORMATION

The profile of the heat sinks used for thermal measurements is shown in Figure 14. Board type is FR4 with 1-oz copper and 1-oz tin/lead (63/37) plate. Use of vias or through-holes to enhance thermal conduction was avoided.

Figure 15 shows a family of $R_{\theta JA}$ curves. The $R_{\theta JA}$ was obtained for various areas of heat sinks while subject to air flow. Power remained fixed at 0.25 W per device or 0.50 W per package. This testing was done at 25°C.

As Figure 14 illustrates, there are two separated heat sinks for each package. Each heat sink is coupled to the lead that is internally tied to a single MOSFET source and is half the total area, as shown in Figure 15. For example, if the total area shown in Figure 15 is 4 cm^2, each heat sink is 2 cm^2.

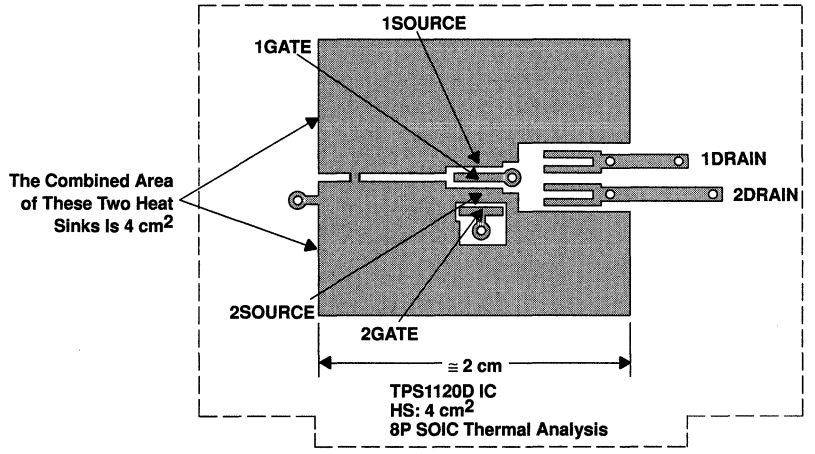


Figure 14. Profile of Heat Sinks

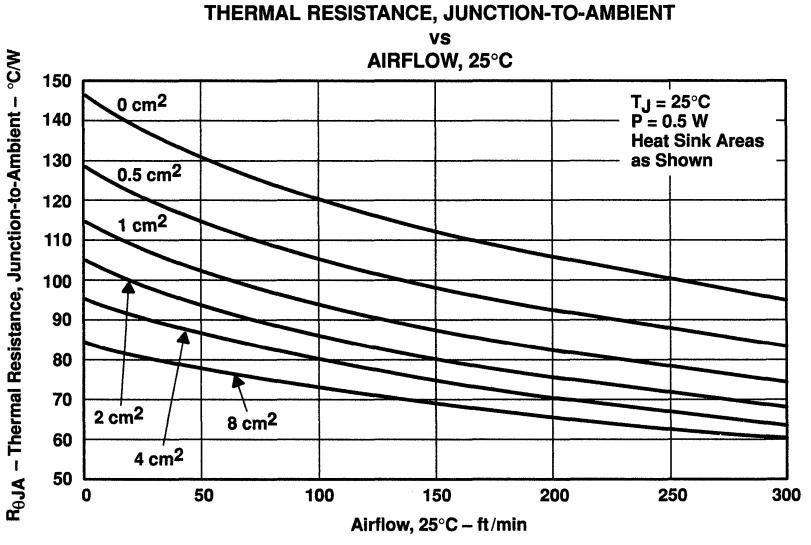


Figure 15

THERMAL INFORMATION

Figure 16 illustrates the thermally enhanced (SO) lead frame. Attaching the two MOSFET dies directly to the source terminals allows maximum heat transfer into a power plane.

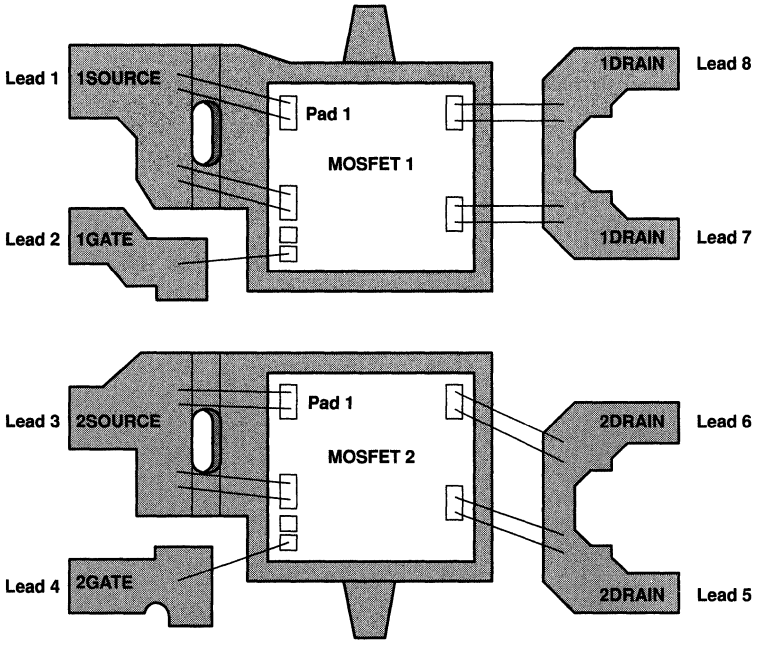


Figure 16. TPS1120 Dual MOSFET SO-8 Lead Frame

APPLICATION INFORMATION

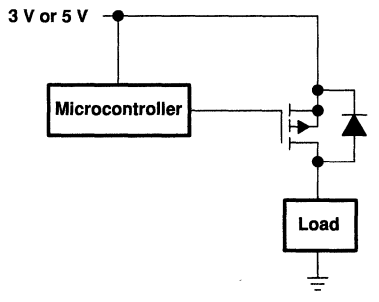


Figure 17. Notebook Load Management

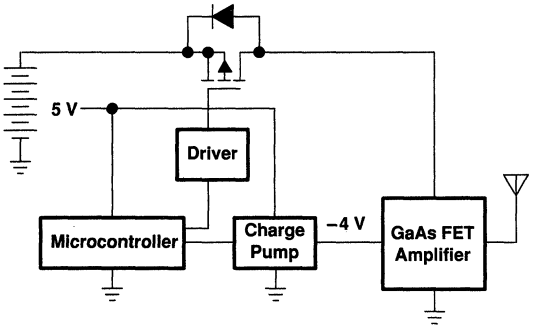
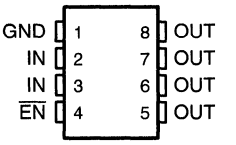


Figure 18. Cellular Phone Output Drive

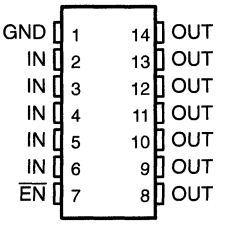
SLVS097A – DECEMBER 1994 – REVISED AUGUST 1995

- 95-mΩ Max (5.5-V Input) High-Side MOSFET Switch With Logic Compatible Enable Input
- Short-Circuit and Thermal Protection
- Typical Short-Circuit Current Limits: 0.4 A, TPS2010; 1.2 A, TPS2011; 2 A, TPS2012; 2.6 A, TPS2013
- Electrostatic-Discharge Protection, 12-kV Output, 6-kV All Other Terminals
- Controlled Rise and Fall Times to Limit Current Surges and Minimize EMI
- SOIC-8 Package Pin Compatible With the Popular Littlefoot™ Series When GND Is Connected
- 2.7-V to 5.5-V Operating Range
- 10-μA Maximum Standby Current
- Surface-Mount SOIC-8 and TSSOP-14 Packages
- –40°C to 125°C Operating Junction Temperature Range

D PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



description

The TPS201x family of power-distribution switches is intended for applications where heavy capacitive loads and short circuits are likely to be encountered. The high-side switch is a 95-mΩ N-channel MOSFET. Gate drive is provided by an internal driver and charge pump designed to control the power switch rise times and fall times to minimize current surges during switching. The charge pump operates at 100 kHz, requires no external components, and allows operation from supplies as low as 2.7 V. When the output load exceeds the current-limit threshold or a short circuit is present, the TPS201x limits the output current to a safe level by switching into a constant-current mode. Continuous heavy overloads and short circuits increase power dissipation in the switch and cause the junction temperature to rise. If the junction temperature reaches approximately 180°C, a thermal protection circuit shuts the switch off to prevent damage. Recovery from thermal shutdown is automatic once the device has cooled sufficiently.

The members of the TPS201x family differ only in short-circuit current threshold. The TPS2010 is designed to limit at 0.4-A load; the other members of the family limit at 1.2 A, 2 A, and 2.6 A (see the available options table). The TPS201x family is available in 8-pin small-outline integrated circuit (SOIC) and 14-pin thin shink small-outline (TSSOP) packages and operates over a junction temperature range of –40°C to 125°C. Versions in the 8-pin SOIC package are drop-in replacements for Siliconix's Littlefoot™ power PMOS switches, except that GND must be connected.

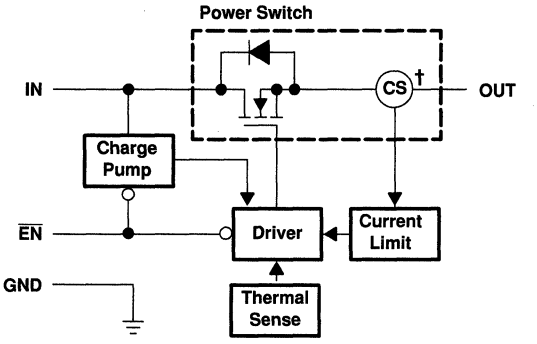
AVAILABLE OPTIONS

T_J	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A)	TYPICAL SHORT-CIRCUIT OUTPUT CURRENT LIMIT AT 25°C (A)	PACKAGED DEVICES		CHIP FORM (Y)
			SOIC (D)†	TSSOP (PW)‡	
–40°C to 125°C	0.2	0.4	TPS2010D	TPS2010PWLE	TPS2010Y
	0.6	1.2	TPS2011D	TPS2011PWLE	TPS2011Y
	1	2	TPS2012D	TPS2012PWLE	TPS2012Y
	1.5	2.6	TPS2013D	TPS2013PWLE	TPS2013Y

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2010DR).
‡ The PW package is only available left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TPS2010PWLE).

Littlefoot is a trademark of Siliconix.

functional block diagram



† Current sense

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	D	PW		
$\overline{EN}$	4	7	I	Enable input. Logic low turns power switch on.
GND	1	1	I	Ground
IN	2, 3	2–6	I	Input voltage
OUT	5–8	8–14	O	Power-switch output

detailed description

power switch

The power switch is an N-channel MOSFET with a maximum on-state resistance of 95 mΩ ($V_{I(IN)}$ = 5.5 V), configured as a high-side switch.

charge pump

An internal 100-kHz charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 4-ms range instead of the microsecond or nanosecond range for a standard FET.

enable ($\overline{EN}$)

A logic high on the $\overline{EN}$ input turns off the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10 μA. A logic zero input restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

current sense

A sense FET monitors the current supplied to the load. The sense FET is a much more efficient way to measure current than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its linear region, which switches the output into a constant current mode and simply holds the current constant while varying the voltage on the load.

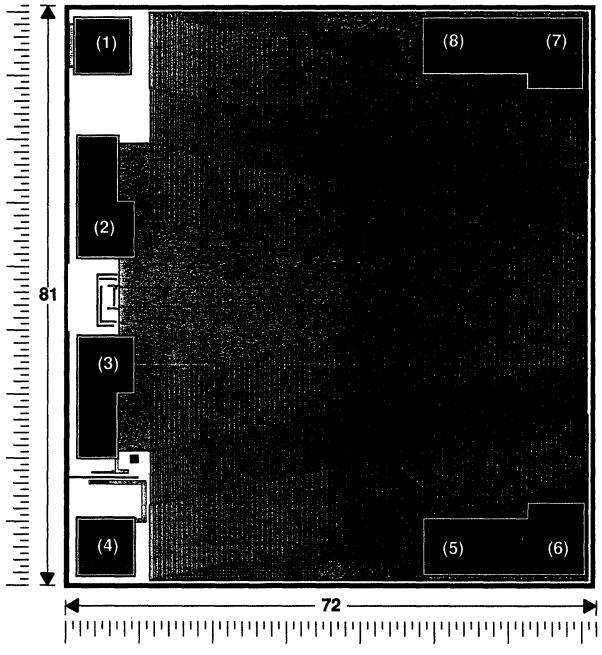
thermal sense

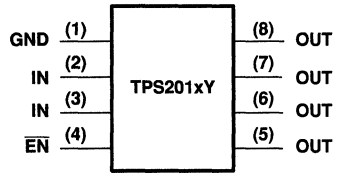
An internal thermal-sense circuit shuts the power switch off when the junction temperature rises to approximately 180°C. Hysteresis is built into the thermal sense, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed.

TPS201xY chip information

This chip, when properly assembled, displays characteristics similar to the TPS201xC. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, $V_{I(IN)}$ (see Note 1) ..... −0.3 V to 7 V
Output voltage range, V_O (see Note 1) ..... −0.3 V to $V_{I(IN)}$ +0.3 V
Input voltage range, V_I at $\overline{EN}$ ..... −0.3 V to 7 V
Continuous output current, I_O ..... internally limited
Continuous total power dissipation ..... See Dissipation Rating Table
Operating virtual junction temperature range, T_J ..... −40°C to 125°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	145 mW
PW	700 mW	5.6 mW/°C	448 mW	140 mW

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, $V_{I(IN)}$		2.7	5.5	V
Input voltage, V_I at $\overline{EN}$		0	5.5	V
Continuous output current, I_O	TPS2010	0	0.2	A
	TPS2011	0	0.6	
	TPS2012	0	1	
	TPS2013	0	1.5	
Operating virtual junction temperature, T_J		−40	125	°C

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = rated current, $\overline{EN}$ = 0 V (unless otherwise noted)

power switch

PARAMETER		TEST CONDITIONS†		TPS2010, TPS2011 TPS2012, TPS2013			UNIT
				MIN	TYP	MAX	
	On-state resistance	$V_{I(IN)}$ = 5.5 V,	T_J = 25°C		75	95	mΩ
		$V_{I(IN)}$ = 4.5 V,	T_J = 25°C		80	110	
		$V_{I(IN)}$ = 3 V,	T_J = 25°C		120	175	
		$V_{I(IN)}$ = 2.7 V,	T_J = 25°C		140	215	
	Output leakage current	$\overline{EN}$ = $V_{I(IN)}$	T_J = 25°C		0.001	1	μA
			−40°C ≤ T_J ≤ 125°C			10	
t_r	Output rise time	$V_{I(IN)}$ = 5.5 V,	T_J = 25°C, C_L = 1 μF		4		ms
		$V_{I(IN)}$ = 2.7 V,	T_J = 25°C, C_L = 1 μF		3.8		
t_f	Output fall time	$V_{I(IN)}$ = 5.5 V,	T_J = 25°C, C_L = 1 μF		3.9		ms
		$V_{I(IN)}$ = 2.7 V,	T_J = 25°C, C_L = 1 μF		3.5		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

enable input ($\overline{EN}$)

PARAMETER		TEST CONDITIONS	TPS2010, TPS2011 TPS2012, TPS2013			UNIT
			MIN	TYP	MAX	
	High-level input voltage	2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V	2			V
	Low-level input voltage	4.5 V ≤ $V_{I(IN)}$ ≤ 5.5 V			0.8	V
		2.7 V ≤ $V_{I(IN)}$ < 4.5 V			0.4	
	Input current	$\overline{EN}$ = 0 V or $\overline{EN}$ = $V_{I(IN)}$	−0.5		0.5	μA
t_{PLH}	Propagation (delay) time, low-to-high-level output	C_L = 1 μF			20	ms
t_{PHL}	Propagation (delay) time, high-to-low-level output	C_L = 1 μF			40	

current limit

PARAMETER	TEST CONDITIONS†		TPS2010, TPS2011 TPS2012, TPS2013			UNIT
			MIN	TYP	MAX	
Short-circuit current	T_J = 25°C, $V_{I(IN)}$ = 5.5 V, OUT connected to GND, device enabled into short circuit	TPS2010	0.22	0.4	0.6	A
		TPS2011	0.66	1.2	1.8	
		TPS2012	1.1	2	3	
		TPS2013	1.65	2.6	4.5	

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

supply current

PARAMETER	TEST CONDITIONS		TPS2010, TPS2011 TPS2012, TPS2013			UNIT
			MIN	TYP	MAX	
Supply current, low-level output	$\overline{EN}$ = $V_{I(IN)}$	T_J = 25°C		0.015	1	μA
		−40°C ≤ T_J ≤ 125°C			10	
Supply current, high-level output	$\overline{EN}$ = 0 V	T_J = 25°C		73	100	μA
		−40°C ≤ T_J ≤ 125°C			100	

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = rated current, $\overline{EN}$ = 0 V, T_J = 25°C (unless otherwise noted)

power switch

PARAMETER	TEST CONDITIONS†	TPS2010Y, TPS2011Y TPS2012Y, TPS2013Y			UNIT
		MIN	TYP	MAX	
On-state resistance	$V_{I(IN)}$ = 5.5 V,		75		mΩ
	$V_{I(IN)}$ = 4.5 V,		80		
	$V_{I(IN)}$ = 3 V,		120		
	$V_{I(IN)}$ = 2.7 V,		140		
Output leakage current	$\overline{EN}$ = $V_{I(IN)}$		0.001		μA
Output rise time	$V_{I(IN)}$ = 5.5 V, C_L = 1 μF		4		ms
	$V_{I(IN)}$ = 2.7 V, C_L = 1 μF		3.8		
Output fall time	$V_{I(IN)}$ = 5.5 V, C_L = 1 μF		3.9		ms
	$V_{I(IN)}$ = 2.7 V, C_L = 1 μF		3.5		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

current limit

PARAMETER	TEST CONDITIONS†	TPS2010Y, TPS2011Y TPS2012Y, TPS2013Y			UNIT
		MIN	TYP	MAX	
Short-circuit current	$V_{I(IN)}$ = 5.5 V, OUT connected to GND, Device enabled into short circuit		0.4		A

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

supply current

PARAMETER	TEST CONDITIONS	TPS2010Y, TPS2011Y TPS2012Y, TPS2013Y			UNIT
		MIN	TYP	MAX	
Supply current, low-level output	$\overline{EN}$ = $V_{I(IN)}$		0.015		μA
Supply current, high-level output	$\overline{EN}$ = 0 V		73		μA

PARAMETER MEASUREMENT INFORMATION

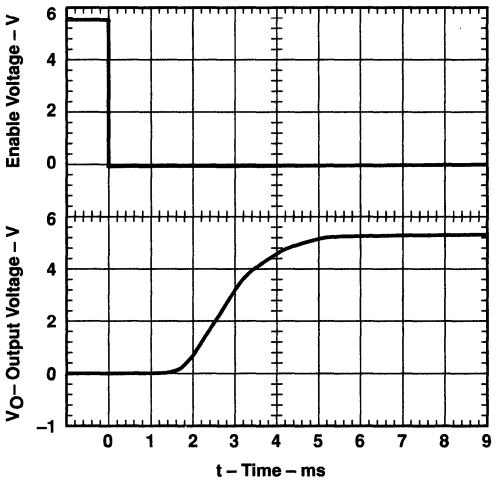


Figure 1. Propagation Delay and Rise Time With 1-μF Load, $V_{I(IN)}$ = 5.5 V

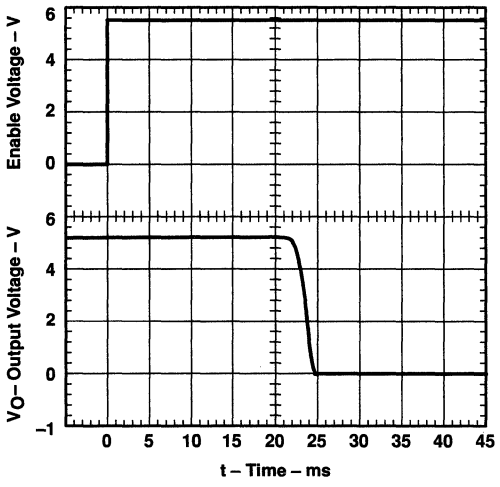


Figure 2. Propagation Delay and Fall Time With 1-μF Load, $V_{I(IN)}$ = 5.5 V

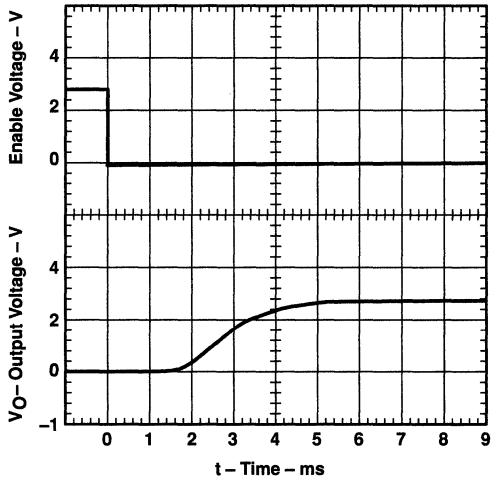


Figure 3. Propagation Delay and Rise Time With 1-μF Load, $V_{I(IN)}$ = 2.7 V

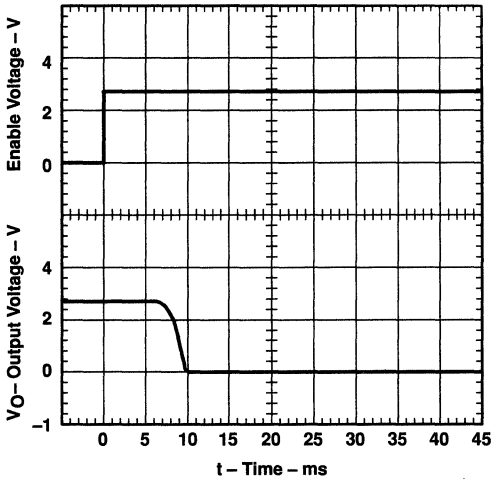


Figure 4. Propagation Delay and Fall Time With 1-μF Load, $V_{I(IN)}$ = 2.7 V

PARAMETER MEASUREMENT INFORMATION

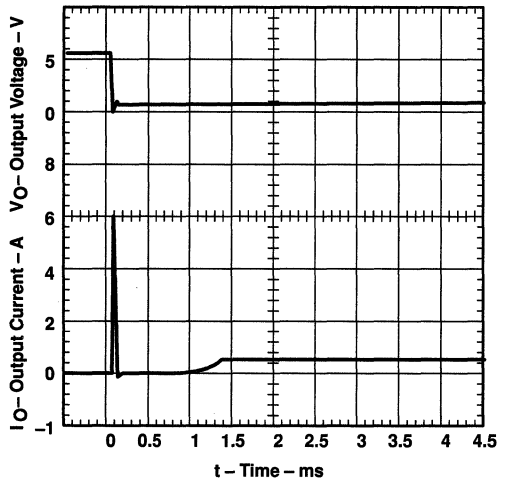


Figure 5. TPS2010, Short-Circuit Current. Short is Applied to Enabled Device, $V_{I(IN)}$ = 5.5 V

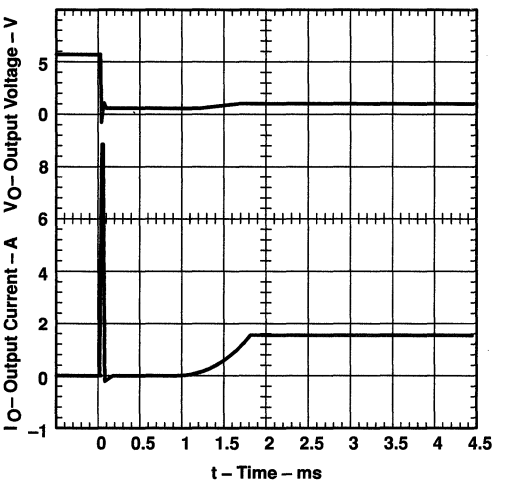


Figure 6. TPS2011, Short-Circuit Current. Short is Applied to Enabled Device, $V_{I(IN)}$ = 5.5 V

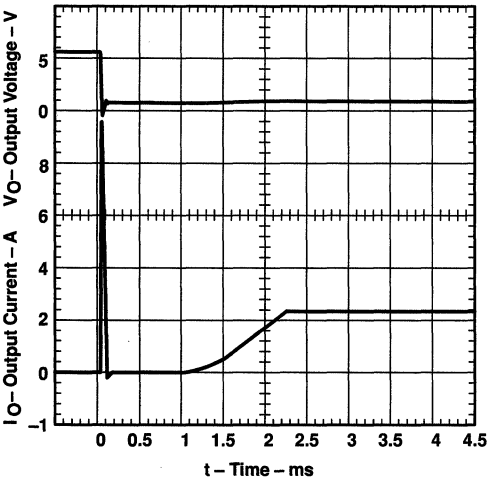


Figure 7. TPS2012, Short-Circuit Current. Short is Applied to Enabled Device, $V_{I(IN)}$ = 5.5 V

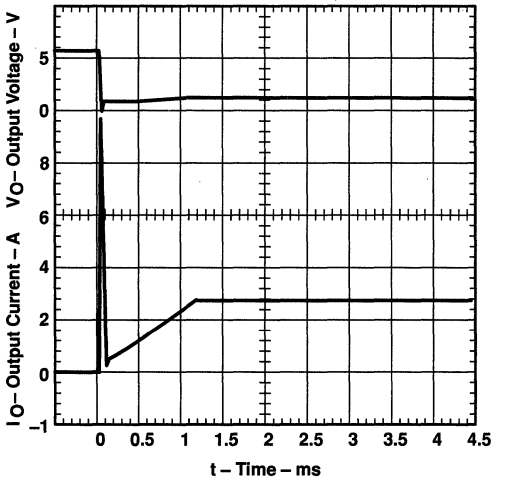


Figure 8. TPS2013 – Short-Circuit Current. Short is Applied to Enabled Device, $V_{I(IN)}$ = 5.5 V

PARAMETER MEASUREMENT INFORMATION

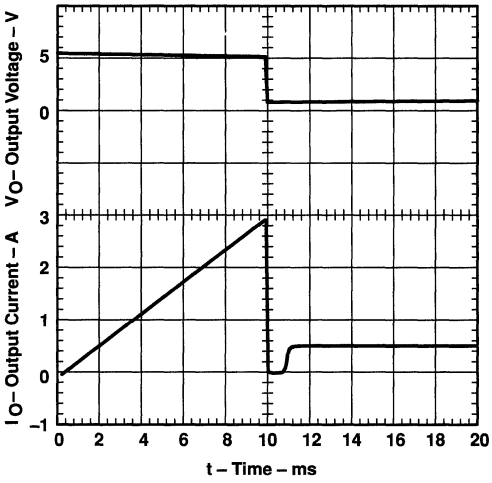


Figure 9. TPS2010 – Threshold Current, $V_{I(IN)}$ = 5.5 V

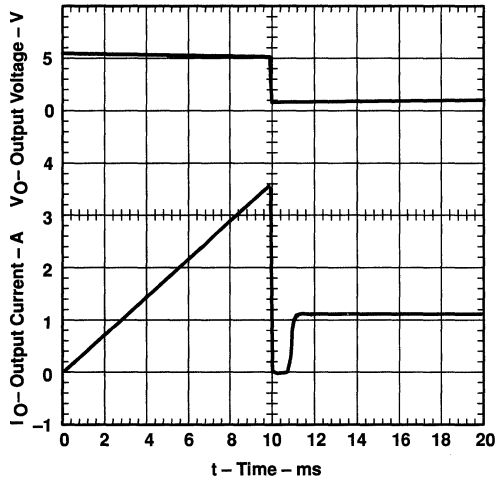


Figure 10. TPS2011 – Threshold Current, $V_{I(IN)}$ = 5.5 V

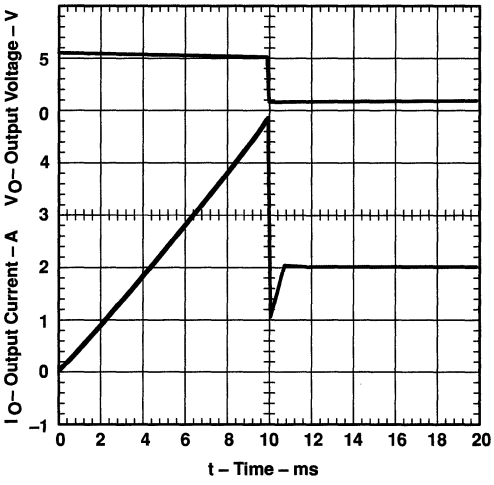


Figure 11. TPS2012 – Threshold Current, $V_{I(IN)}$ = 5.5 V

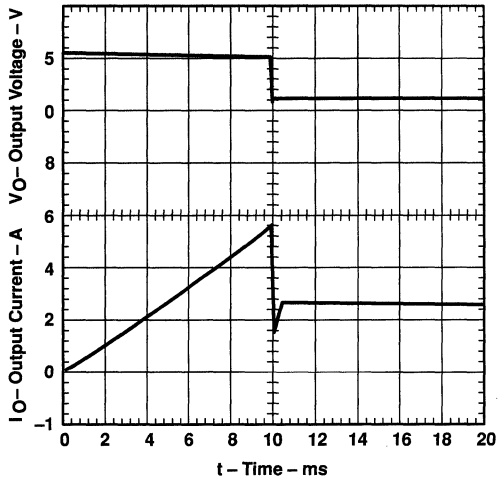


Figure 12. TPS2013 – Threshold Current, $V_{I(IN)}$ = 5.5 V

PARAMETER MEASUREMENT INFORMATION

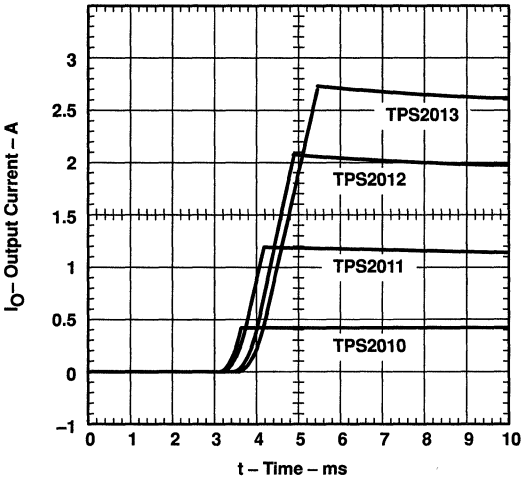
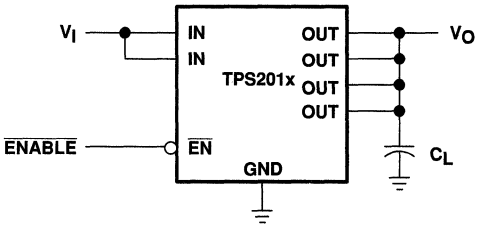
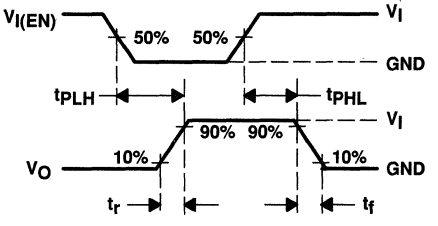


Figure 13. Turned-On (Enabled) Into Short Circuit, $V_{I(IN)}$ = 5.5 V



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 14. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

TURN-ON DELAY TIME vs INPUT VOLTAGE

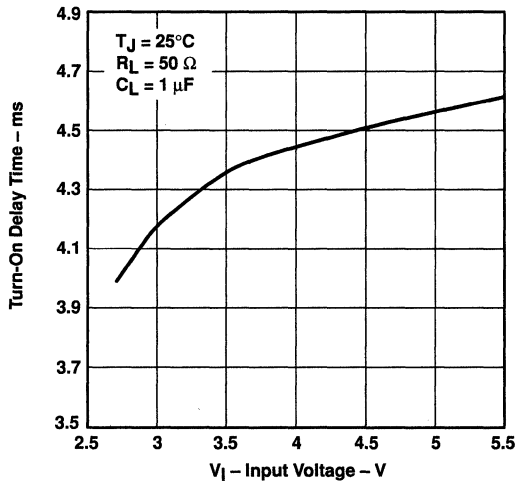


Figure 15

TURN-OFF DELAY TIME vs INPUT VOLTAGE

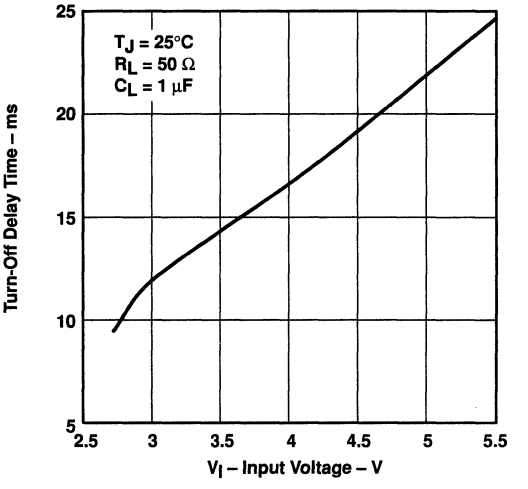


Figure 16

RISE TIME vs OUTPUT CURRENT

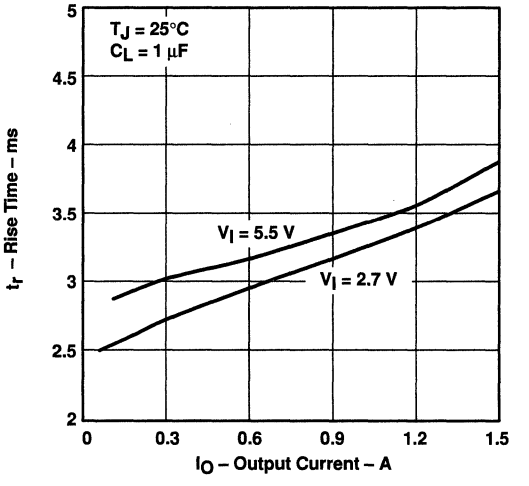


Figure 17

FALL TIME vs OUTPUT CURRENT

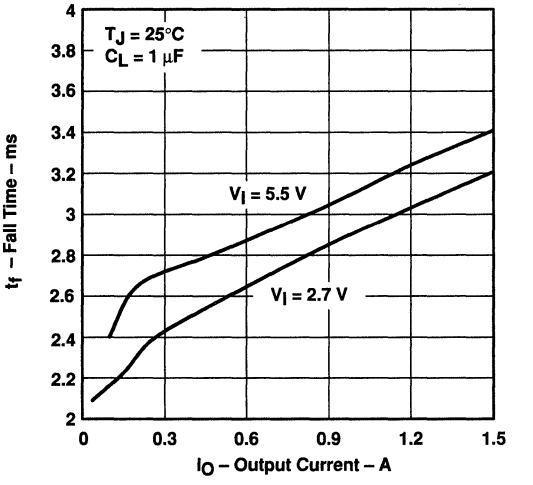


Figure 18

TYPICAL CHARACTERISTICS

SUPPLY CURRENT (OUTPUT ENABLED)
vs
JUNCTION TEMPERATURE

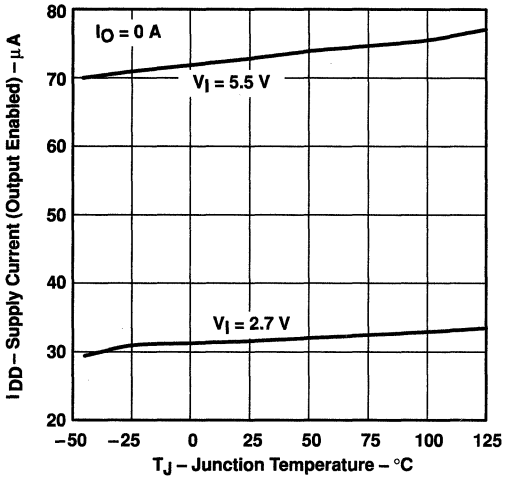


Figure 19

SUPPLY CURRENT (OUTPUT DISABLED)
vs
JUNCTION TEMPERATURE

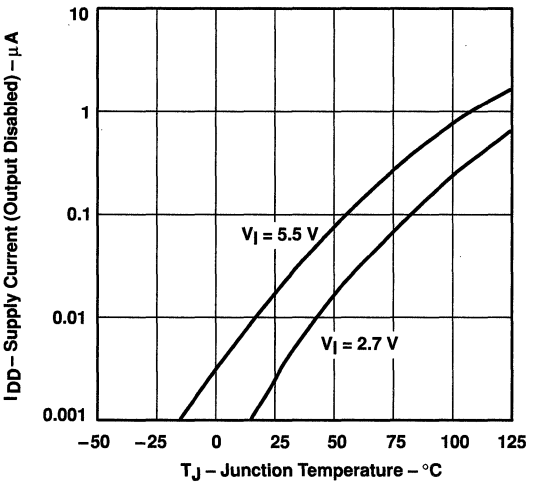


Figure 20

SUPPLY CURRENT (OUTPUT ENABLED)
vs
INPUT VOLTAGE

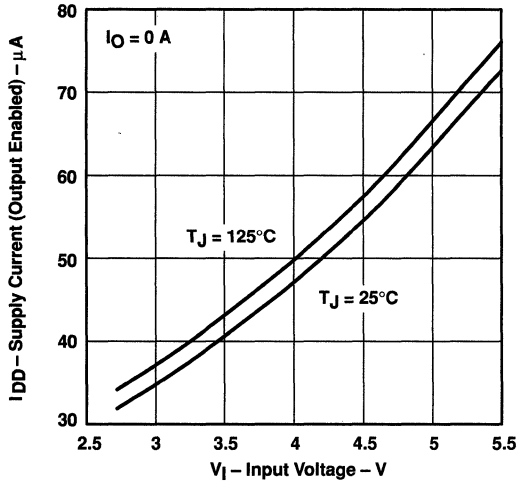


Figure 21

SUPPLY CURRENT (OUTPUT DISABLED)
vs
INPUT VOLTAGE

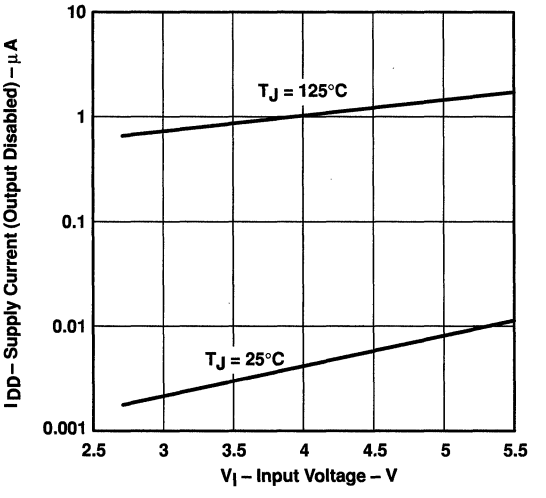


Figure 22

TYPICAL CHARACTERISTICS

ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

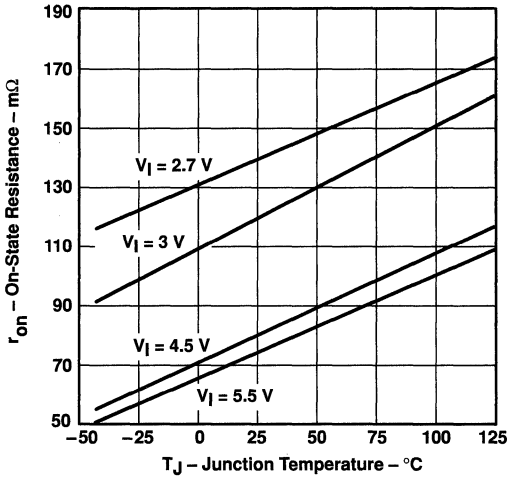


Figure 23

ON-STATE RESISTANCE
vs
INPUT VOLTAGE

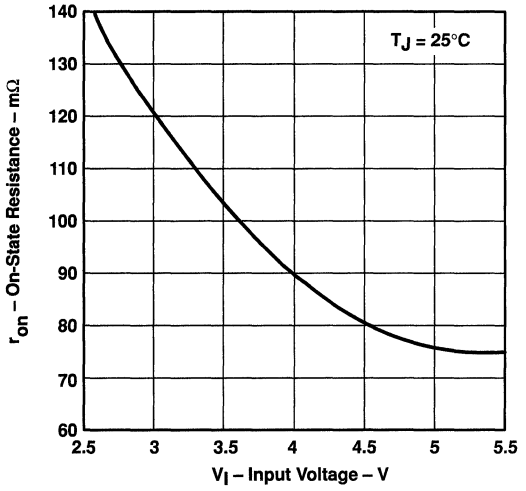


Figure 24

INPUT VOLTAGE TO OUTPUT VOLTAGE
vs
INPUT VOLTAGE

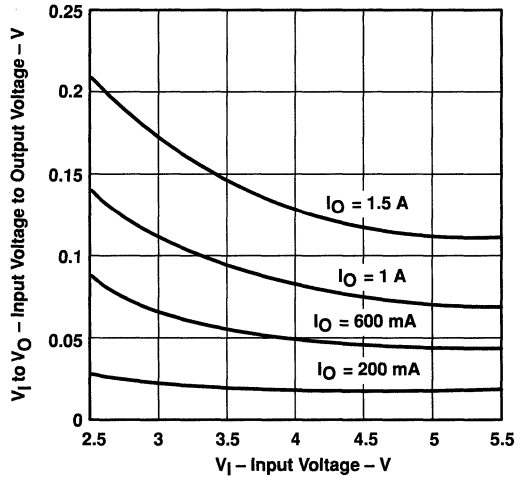


Figure 25

SHORT-CIRCUIT CURRENT
vs
INPUT VOLTAGE

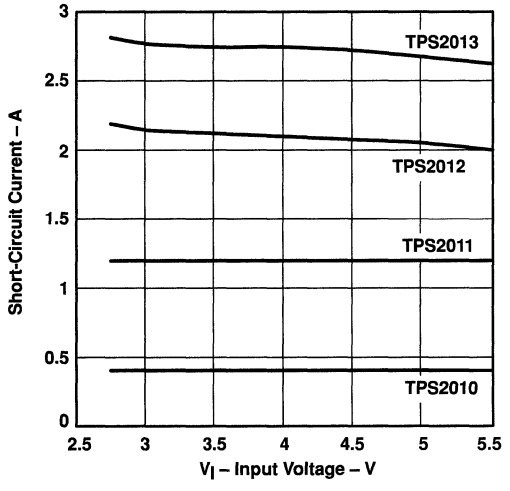


Figure 26

TYPICAL CHARACTERISTICS

THRESHOLD TRIP CURRENT
vs
INPUT VOLTAGE

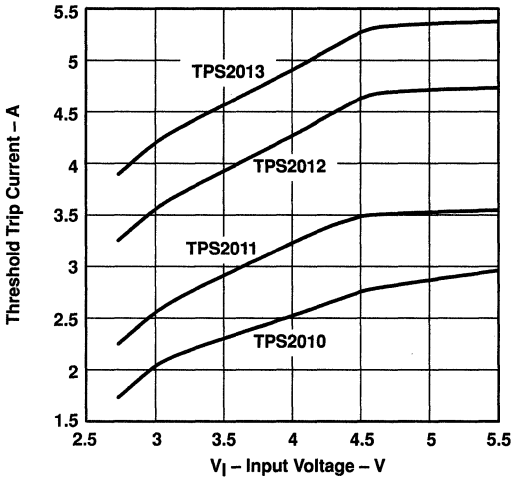


Figure 27

SHORT-CIRCUIT CURRENT
vs
JUNCTION TEMPERATURE

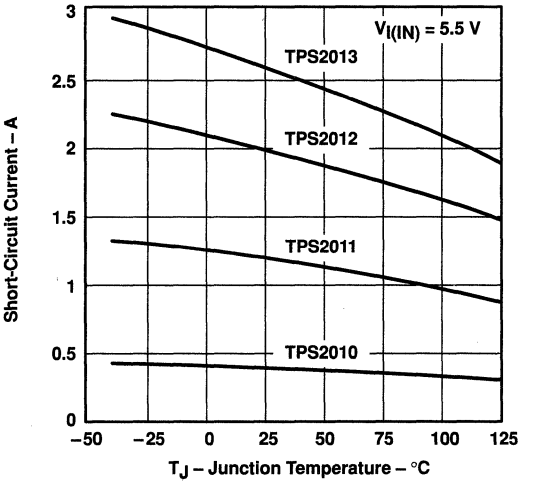


Figure 28

APPLICATION INFORMATION

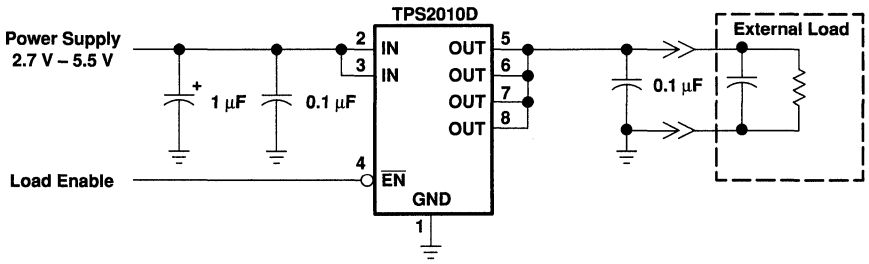


Figure 29. Typical Application

power supply considerations

The TPS201x family has multiple inputs and outputs, which must be connected in parallel to minimize voltage drop and prevent unnecessary power dissipation.

A 0.047-µF to 0.1-µF ceramic bypass capacitor between IN and GND, close to the device, is recommended. A high-value electrolytic capacitor is also desirable when the output load is heavy or has large paralleled capacitors. Bypassing the output with a 0.1-µF ceramic capacitor improves the immunity of the device to electrostatic discharge (ESD).

overcurrent

A sense FET is employed to check for overcurrent conditions. Unlike sense resistors and polyfuses, sense FETs do not increase series resistance to the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Shutdown only occurs if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 30). The TPS201x senses the short and immediately switches into a constant-current output.

Under the second condition, the short occurs while the device is enabled. At the instant the short occurs, very high currents flow for a short time before the current-limit circuit can react (see Figures 5, 6, 7, and 8). After the current-limit circuit has tripped, the device limits normally.

Under the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached (see Figures 9, 10, 11, and 12). The TPS201x family is capable of delivering currents up to the current-limit threshold without damage. Once the threshold has been reached, the device switches into its constant-current mode.

APPLICATION INFORMATION

overcurrent (continued)

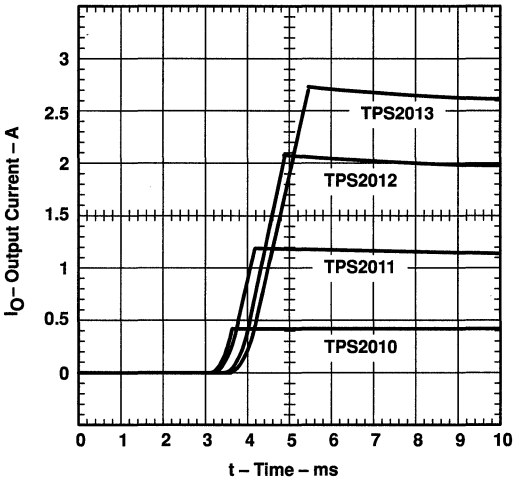


Figure 30. Turned-On (Enabled) Into Short Circuit, $V_{I(IN)}$ = 5.5 V

power dissipation and junction temperature

The low on resistance of the N-channel MOSFET allows small surface-mount packages, such as SOIC or TSSOP to pass large currents. The thermal resistances of these packages are high compared to that of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find r_{on} at the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read r_{on} from Figure 23. Next calculate the power dissipation using:

$$P_D = r_{on} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient temperature
$R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W, TSSOP = 179°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

APPLICATION INFORMATION

thermal protection

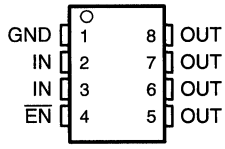
Thermal protection is provided to prevent damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS201x into its constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to dangerously high levels. The protection circuit senses the junction temperature of the switch and shuts it off. The switch remains off until the junction has dropped approximately 20°C. The switch continues to cycle in this manner until the load fault or input power is removed.

ESD protection

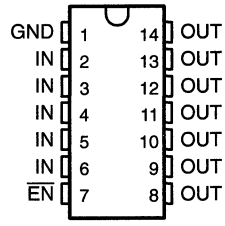
All TPS201x terminals incorporate ESD-protection circuitry designed to withstand a 6-kV human-body-model discharge as defined in MIL-STD-883C. Additionally, the output is protected from discharges up to 12 kV.

- 50-mΩ -Maximum (5-V Input) High-Side MOSFET Switch
- Short-Circuit and Thermal Protection
- Operating Range . . . 2.7 V to 5.5 V
- Logic-Level Enable Input
- Typical Rise Time . . . 6.1 ms
- Undervoltage Lockout
- Maximum Standby Supply Current . . . 10 μA
- No Drain-Source Back-Gate Diode
- Available in 8-pin SOIC and 14-Pin TSSOP Packages
- Ambient Temperature Range, –40°C to 85°C
- 2-kV Human-Body-Model, 200-V Machine-Model ESD Protection

D PACKAGE
(TOP VIEW)



PWP PACKAGE
(TOP VIEW)



description

The TPS201xA family of power distribution switches is intended for applications where heavy capacitive loads and short circuits are likely to be encountered. These devices are 50-mΩ N-channel MOSFET high-side power switches. The switch is controlled by a logic enable compatible with 5-V logic and 3-V logic. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the TPS201xA limits the output current to a safe level by switching into a constant-current mode. When continuous heavy overloads and short circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until valid input voltage is present.

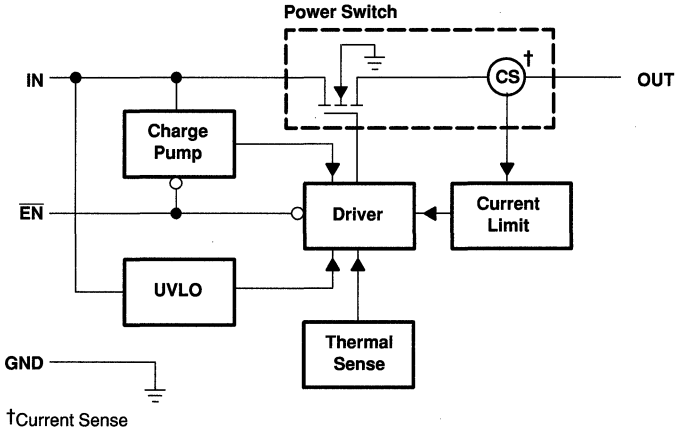
The TPS201xA devices differ only in short-circuit current threshold. The TPS2010A limits at 0.3-A load, the TPS2011 at 0.9-A load, the TPS2012A at 1.5-A load, and the TPS2013A at 2.2-A load (see Available Options). The TPS201xA is available in an 8-pin small-outline integrated-circuit (SOIC) package and in a 14-pin thin-shrink small-outline package (TSSOP) and operates over a junction temperature range of –40°C to 125°C.

AVAILABLE OPTIONS

T_A	ENABLE	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A)	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (A)	PACKAGED DEVICES	
				SMALL OUTLINE (D)†	TSSOP (PWP)‡
–40°C to 85°C	Active low	0.2	0.3	TPS2010AD	TPS2010APWPR
		0.6	0.9	TPS2011AD	TPS2011APWPR
		1	1.5	TPS2012AD	TPS2012APWPR
		1.5	2.2	TPS2013AD	TPS2013APWPR

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2010DR)
‡ The PWP package is only available left-end taped-and-reeled.

TPS201xA functional block diagram



Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO. D	NO. PWP		
$\overline{EN}$	4	7	I	Enable input. Logic low turns on power switch.
GND	1	1	I	Ground
IN	2, 3	2–6	I	Input voltage
OUT	5, 6, 7, 8	8–14	O	Power-switch output

detailed description

power switch

The power switch is an N-channel MOSFET with a maximum on-state resistance of 50 mΩ ($V_{I(IN)}$ = 5 V). Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled.

charge pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 9-ms range.

enable ($\overline{EN}$)

The logic enable disables the power switch, the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10 μA when a logic high is present on $\overline{EN}$. A logic zero input on $\overline{EN}$ restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

current sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant current mode and holds the current constant while varying the voltage on the load.

thermal sense

An internal thermal-sense circuit shuts off the power switch when the junction temperature rises to approximately 140°C. Hysteresis is built into the thermal sense circuit. After the device has cooled approximately 20°C, the switch turns back on. The switch continues to cycle off and on until the fault is removed.

undervoltage lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, $V_{I(IN)}$ (see Note 1) ..... −0.3 V to 6 V
Output voltage range, $V_{O(OUT)}$ (see Note 1) ..... −0.3 V to $V_{I(IN)}$ + 0.3 V
Input voltage range, $V_{I(\overline{EN})}$ ..... −0.3 V to 6 V
Continuous output current, $I_{O(OUT)}$ ..... internally limited
Continuous total power dissipation ..... See Dissipation Rating Table
Operating virtual junction temperature range, T_J ..... −40°C to 125°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
PWP	700 mW	5.6 mW/°C	448 mW	364 mW

recommended operating conditions

		MIN	MAX	UNIT
Input voltage	$V_{I(IN)}$	2.7	5.5	V
	$V_{I(\overline{EN})}$	0	5.5	V
Continuous output current, I_O	TPS2010A	0	0.2	A
	TPS2011A	0	0.6	
	TPS2012A	0	1	
	TPS2013A	0	1.5	
Operating virtual junction temperature, T_J		−40	125	°C

electro static discharge (ESD) protection

	MIN	MAX	UNIT
Human Body Model MIL-STD-883C		2	kV
Machine model		0.2	kV

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $\overline{EN}$ = 0 V (unless otherwise noted)

power switch

PARAMETER		TEST CONDITIONS†			MIN	TYP	MAX	UNIT
$r_{DS(on)}$	Static drain-source on-state resistance	$V_{I(IN)}$ = 5 V,	T_J = 25°C,	I_O = 1.5 A		33	36	mΩ
		$V_{I(IN)}$ = 5 V,	T_J = 85°C,	I_O = 1.5 A		38	46	
		$V_{I(IN)}$ = 5 V,	T_J = 125°C,	I_O = 1.5 A		44	50	
		$V_{I(IN)}$ = 3.3 V,	T_J = 25°C,	I_O = 1.5 A		37	41	
		$V_{I(IN)}$ = 3.3 V,	T_J = 85°C,	I_O = 1.5 A		43	52	
		$V_{I(IN)}$ = 3.3 V,	T_J = 125°C,	I_O = 1.5 A		51	61	
		$V_{I(IN)}$ = 5 V,	T_J = 25°C,	I_O = 0.18 A		30	34	
		$V_{I(IN)}$ = 5 V,	T_J = 85°C,	I_O = 0.18 A		35	41	
		$V_{I(IN)}$ = 5 V,	T_J = 125°C,	I_O = 0.18 A		39	47	
		$V_{I(IN)}$ = 3.3 V,	T_J = 25°C,	I_O = 0.18 A		33	37	
		$V_{I(IN)}$ = 3.3 V,	T_J = 85°C,	I_O = 0.18 A		39	46	
		$V_{I(IN)}$ = 3.3 V,	T_J = 125°C,	I_O = 0.18 A		44	56	
t_r	Rise time, output	$V_{I(IN)}$ = 5.5 V, C_L = 1 µF,	T_J = 25°C, R_L = 10 Ω			6.1		ms
		$V_{I(IN)}$ = 2.7 V, C_L = 1 µF,	T_J = 25°C, R_L = 10 Ω			8.6		
t_f	Fall time, output	$V_{I(IN)}$ = 5.5 V, C_L = 1 µF,	T_J = 25°C, R_L = 10 Ω			3.4		ms
		$V_{I(IN)}$ = 2.7 V, C_L = 1 µF,	T_J = 25°C, R_L = 10 Ω			3		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

enable input ($\overline{EN}$)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V	2			V
V_{IL}	Low-level input voltage	4.5 V ≤ $V_{I(IN)}$ ≤ 5.5 V			0.8	V
		2.7 V ≤ $V_{I(IN)}$ ≤ 4.5 V			0.5	
I_I	Input current	$\overline{EN}$ = 0 V or $\overline{EN}$ = $V_{I(IN)}$	−0.5		0.5	µA
t_{on}	Turn-on time	C_L = 100 µF, R_L = 10 Ω			20	ms
t_{off}	Turn-off time	C_L = 100 µF, R_L = 10 Ω			40	

current limit

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
I_{OS}	Short-circuit output current	T_J = 25°C, V_I = 5.5 V, OUT connected to GND, Device enable into short circuit	TPS2010A	0.22	0.3	0.4	A
			TPS2011A	0.66	0.9	1.1	
			TPS2012A	1.1	1.5	1.8	
			TPS2013A	1.65	2.2	2.7	

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $\overline{EN}$ = 0 V (unless otherwise noted) (continued)

supply current

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Supply current, low-level output	No Load on OUT	$\overline{EN}$ = $V_{I(IN)}$	T_J = 25°C		0.3	1	µA
			−40°C ≤ T_J ≤ 125°C			10	
Supply current, high-level output	No Load on OUT	$\overline{EN}$ = 0 V	T_J = 25°C		58	75	µA
			−40°C ≤ T_J ≤ 125°C		75	100	
Leakage current	OUT connected to ground	$\overline{EN}$ = $V_{I(IN)}$	−40°C ≤ T_J ≤ 125°C		10		µA

undervoltage lockout

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low-level input voltage		2		2.5	V
Hysteresis	T_J = 25°C		100		mV

PARAMETER MEASUREMENT INFORMATION

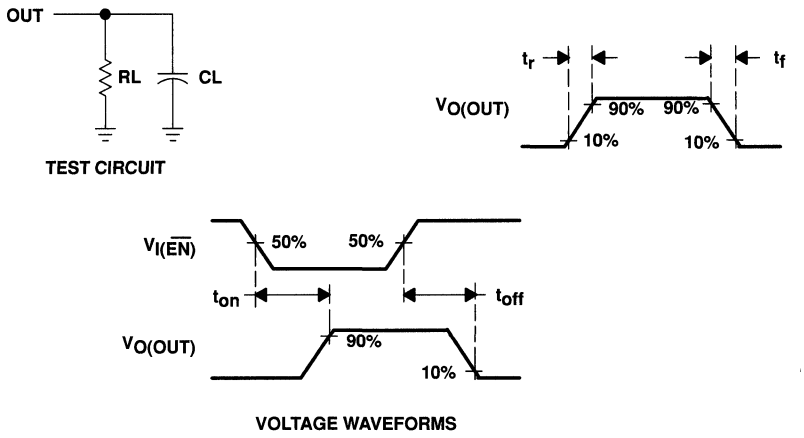


Figure 1. Test Circuit and Voltage Waveforms

Table of Timing Diagrams

	FIGURE
Turn-on Delay and Rise TIme	2
Turn-off Delay and Fall Time	3
Turn-on Delay and Rise TIme with 1-μF Load	4
Turn-off Delay and Rise TIme with 1-μF Load	5
Device Enabled into Short	6
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TPS2013A, Inrush Current	15
7.9-Ω Load Connected to an Enabled TPS2010A Device	16
3.7-Ω Load Connected to an Enabled TPS2010A Device	17
3.7-Ω Load Connected to an Enabled TPS2011A Device	18
2.6-Ω Load Connected to an Enabled TPS2011A Device	19
2.6-Ω Load Connected to an Enabled TPS2012A Device	20
1.2-Ω Load Connected to an Enabled TPS2012A Device	21
1.2-Ω Load Connected to an Enabled TPS2013A Device	22
0.9-Ω Load Connected to an Enabled TPS2013A Device	23

PARAMETER MEASUREMENT INFORMATION

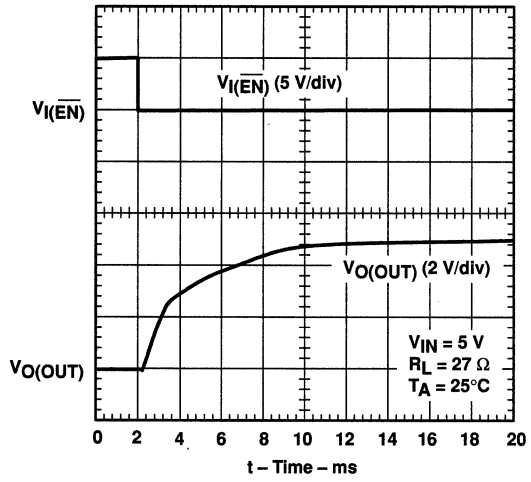

Figure 2. Turn-on Delay and Rise Time

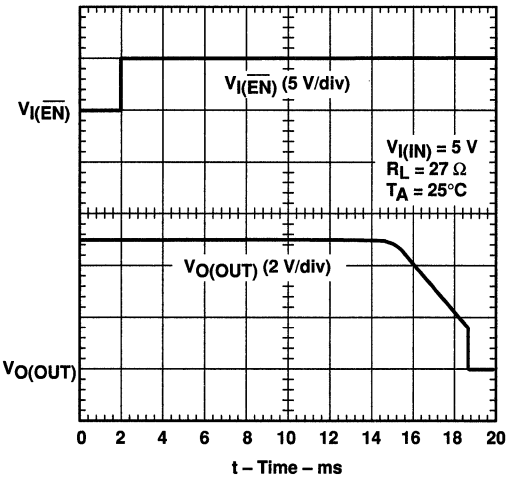

Figure 3. Turn-off Delay and Fall Time

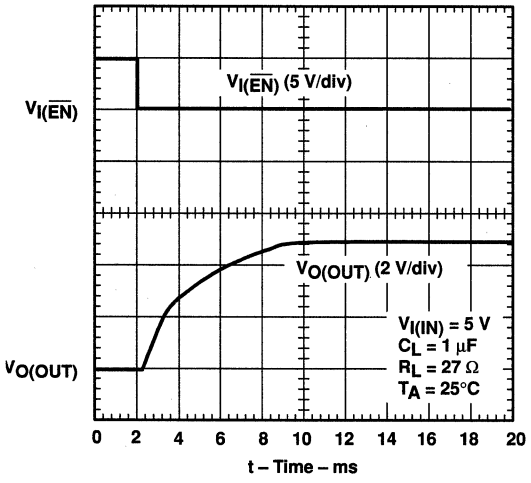

Figure 4. Turn-on Delay and Rise Time With 1-μF Load

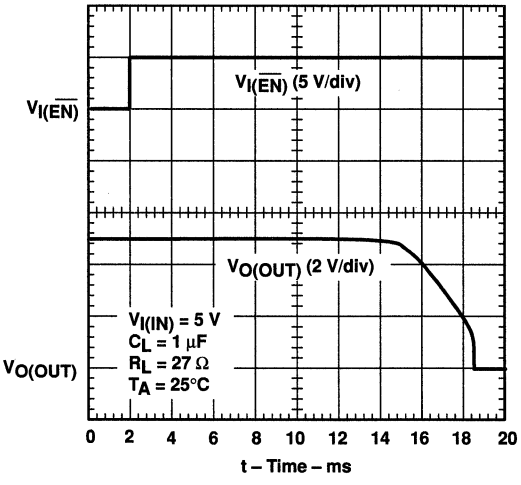

Figure 5. Turn-off Delay and Fall Time with 1-μF Load

PARAMETER MEASUREMENT INFORMATION

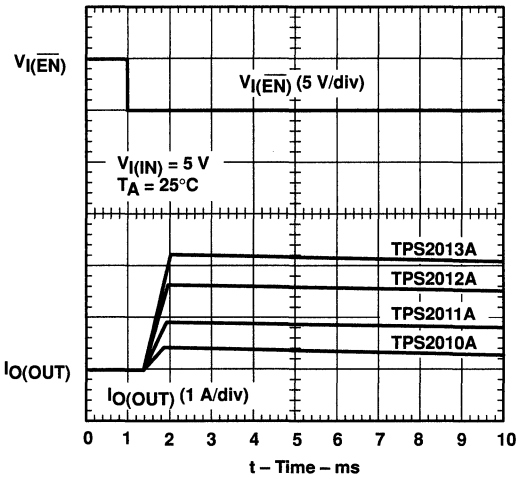

Figure 6. Device Enabled into Short

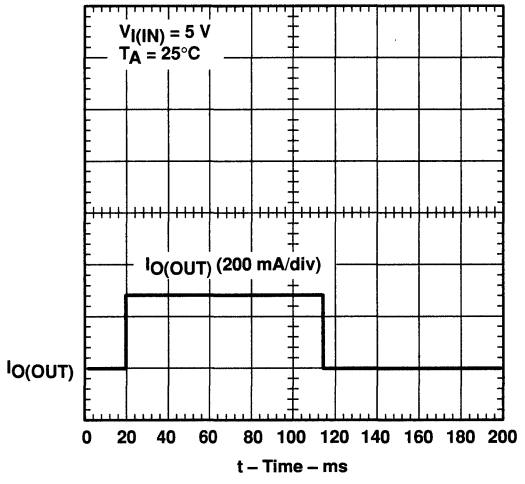

Figure 7. TPS2010A, Short Applied to an Enabled Device

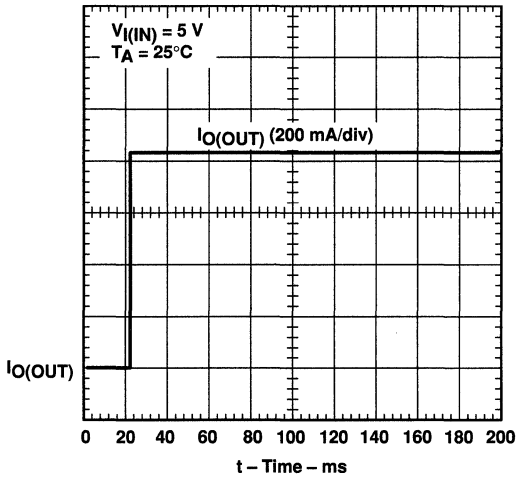

Figure 8. TPS2011A, Short Applied to an Enabled Device

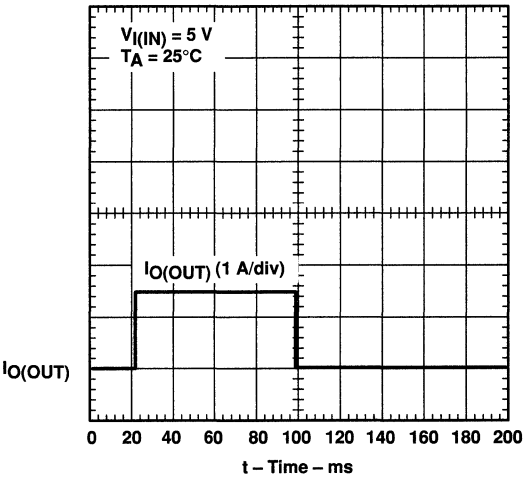

Figure 9. TPS2012A, Short Applied to an Enabled Device

PARAMETER MEASUREMENT INFORMATION

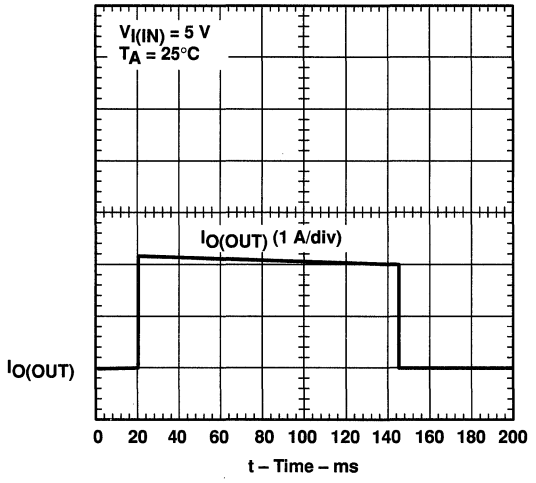

Figure 10. TPS2013A, Short Applied to an Enabled Device

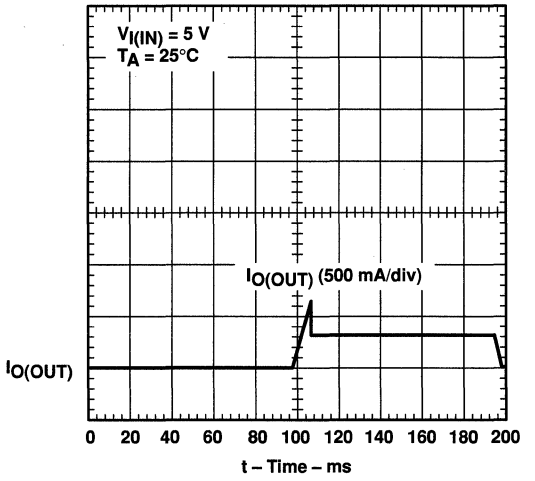

Figure 11. TPS2010A, Ramped Load on Enabled Device

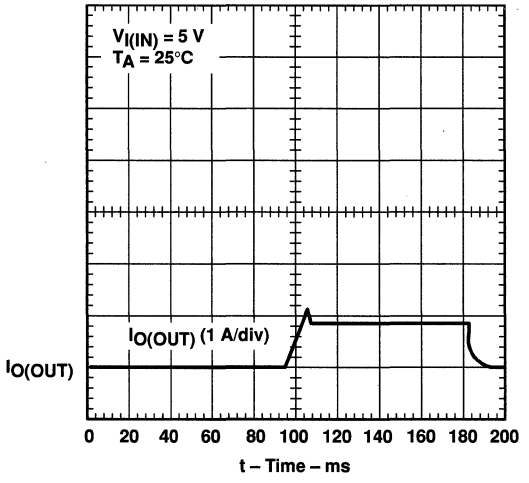

Figure 12. TPS2011A, Ramped Load on Enabled Device

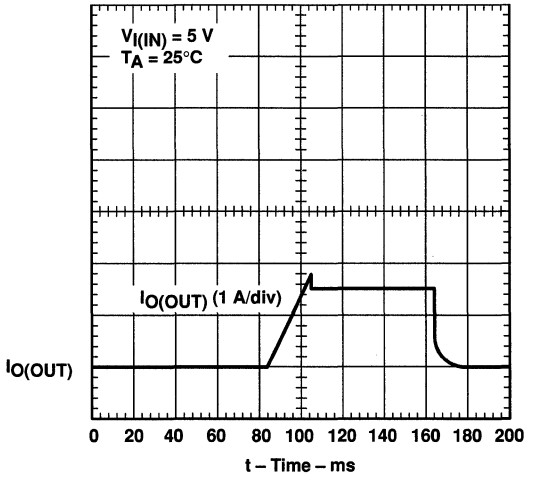

Figure 13. TPS2012A, Ramped Load on Enabled Device

PARAMETER MEASUREMENT INFORMATION

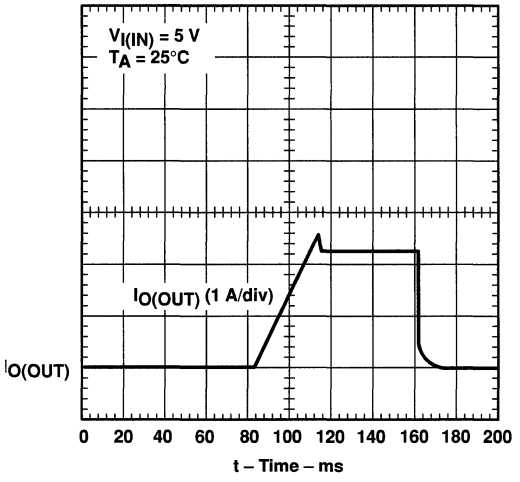

Figure 14. TPS2013A, Ramped Load on Enabled Device

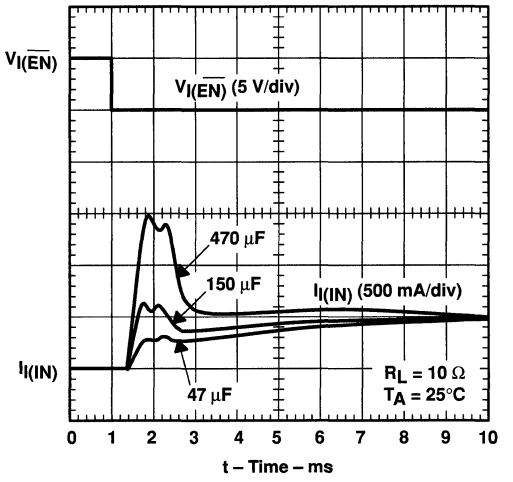

Figure 15. TPS2013A, Inrush Current

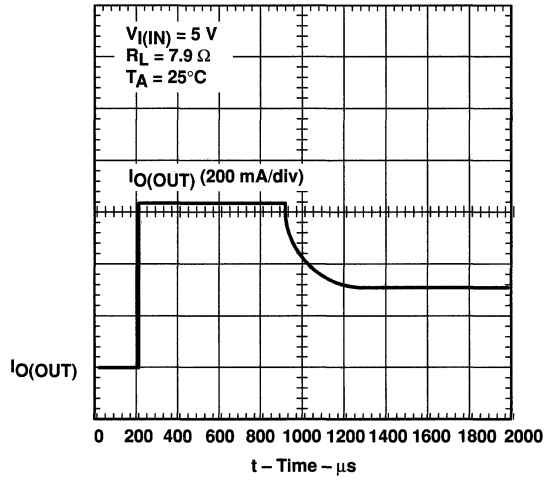

Figure 16. 7.9-Ω Load Connected to an Enabled TPS2010A Device

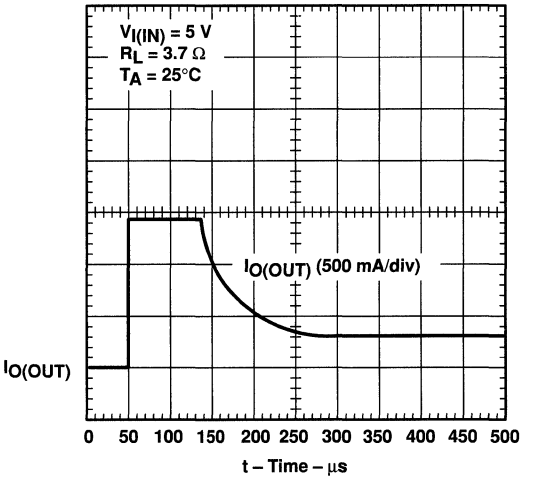

Figure 17. 3.7-Ω Load Connected to an Enabled TPS2010A Device

PARAMETER MEASUREMENT INFORMATION

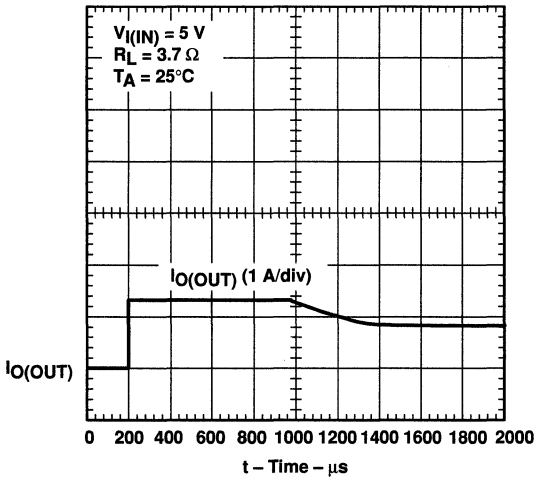

Figure 18. 3.7-Ω Load Connected to an Enabled TPS2011A Device

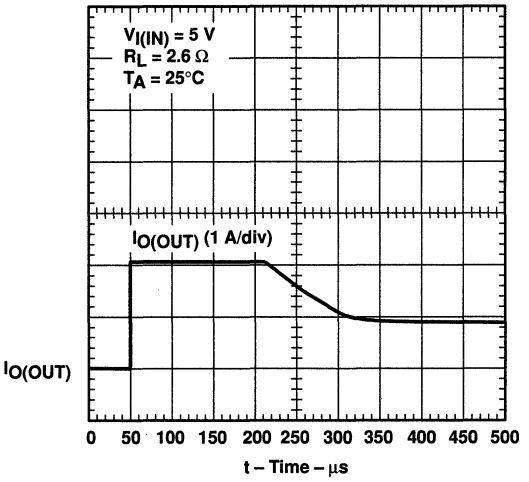

Figure 19. 2.6-Ω Load Connected to an Enabled TPS2011A Device

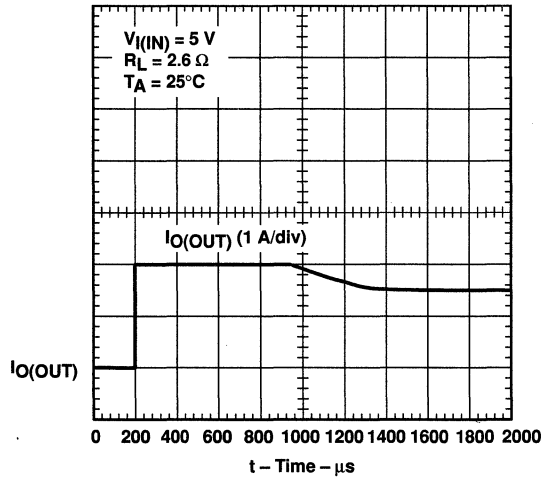

Figure 20. 2.6-Ω Load Connected to an Enabled TPS2012A Device

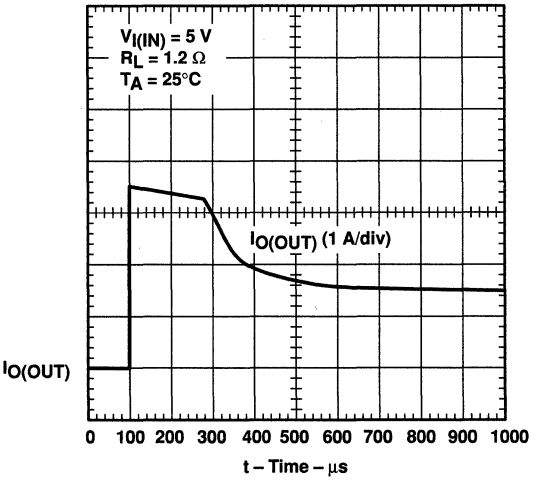

Figure 21. 1.2-Ω Load Connected to an Enabled TPS2012A Device

PARAMETER MEASUREMENT INFORMATION

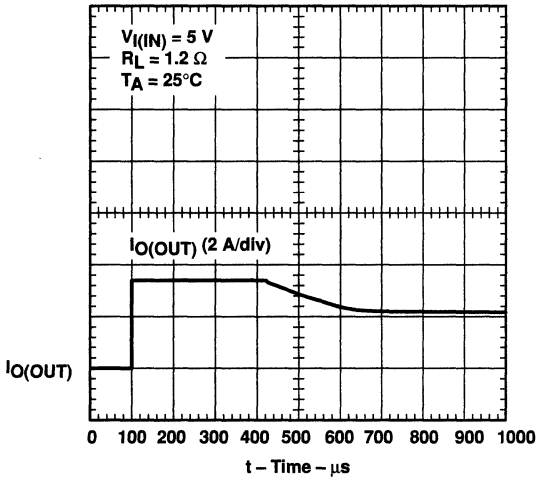

Figure 22. 1.2-Ω Load Connected to an Enabled TPS2013A Device

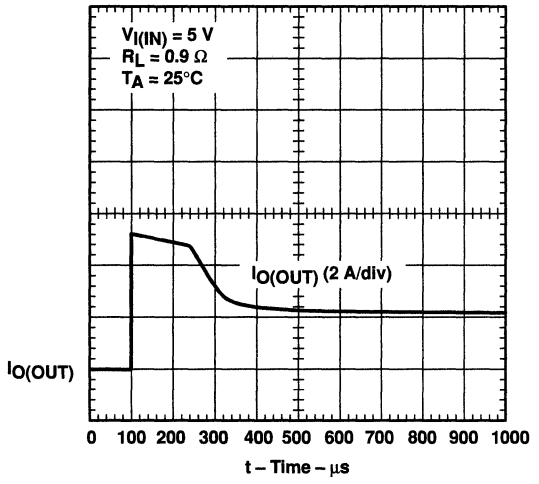

Figure 23. 0.9-Ω Load Connected to an Enabled TPS2013A Device

TYPICAL CHARACTERISTICS

Table of Graphs

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$t_{d(on)}$	Turn-on delay time	vs Output voltage	24
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t_f	Fall time	vs Load current	27
	Supply current (enabled)	vs Junction temperature	28
	Supply current (disabled)	vs Junction temperature	29
	Supply current (enabled)	vs Input voltage	30
	Supply current (disabled)	vs Input voltage	31
I_{OS}	Short-circuit current limit	vs Input voltage	32
		vs Junction temperature	33
$r_{DS(on)}$	Static drain-source on-state resistance	vs Input voltage	34
		vs Junction temperature	35
		vs Input voltage	36
		vs Junction temperature	37
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TURN-ON DELAY TIME vs OUTPUT VOLTAGE

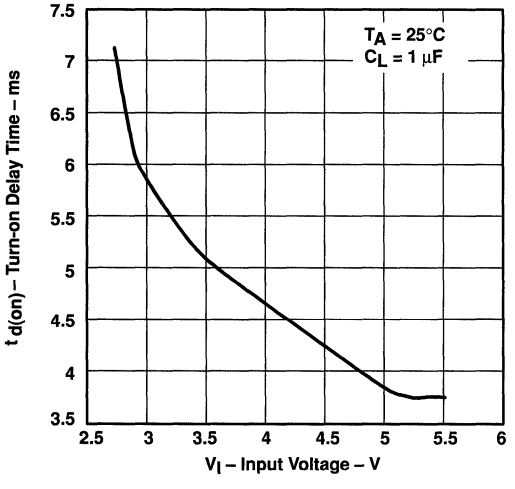


Figure 24

TURN-OFF DELAY TIME vs INPUT VOLTAGE

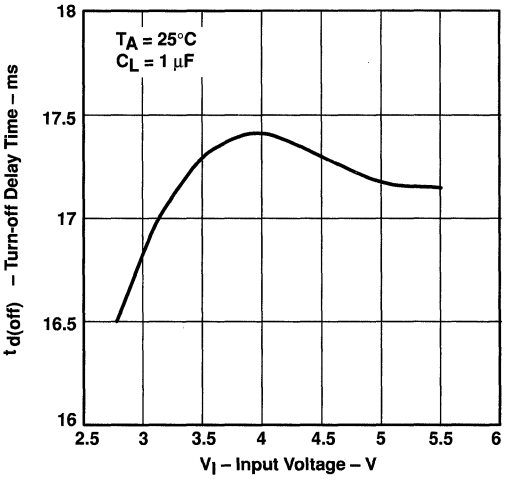


Figure 25

TYPICAL CHARACTERISTICS

RISE TIME
vs
LOAD CURRENT

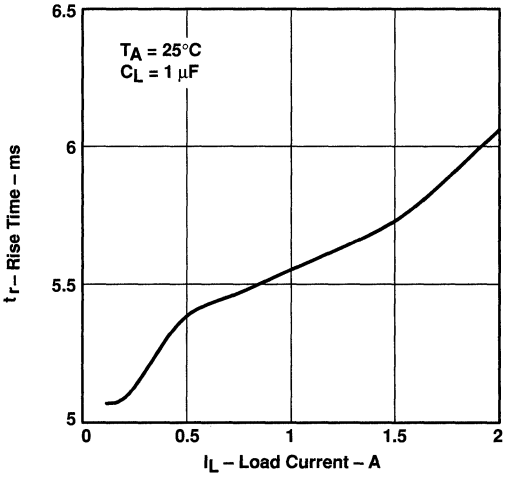


Figure 26

FALL TIME
vs
LOAD CURRENT

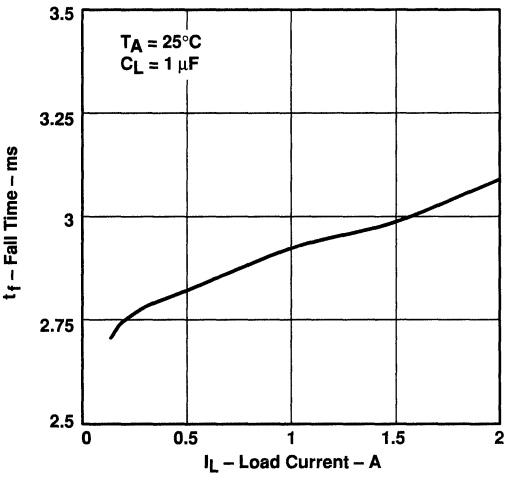


Figure 27

SUPPLY CURRENT (ENABLED)
vs
JUNCTION TEMPERATURE

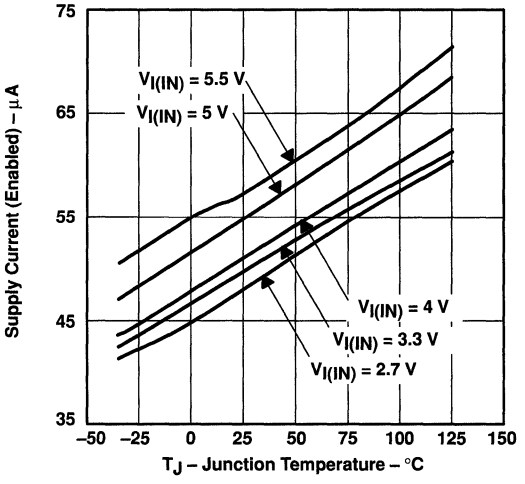


Figure 28

SUPPLY CURRENT (DISABLED)
vs
JUNCTION TEMPERATURE

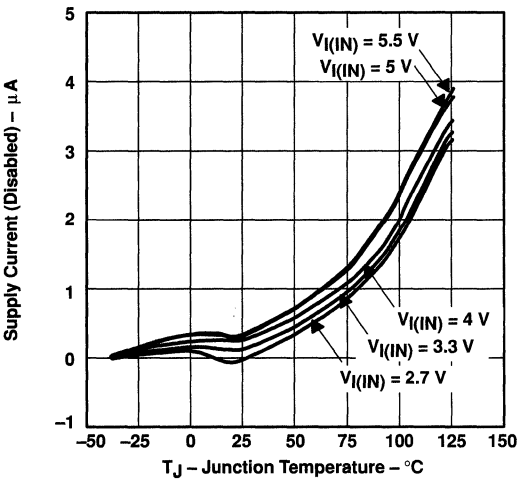


Figure 29

TYPICAL CHARACTERISTICS

SUPPLY CURRENT (ENABLED)
vs
INPUT VOLTAGE

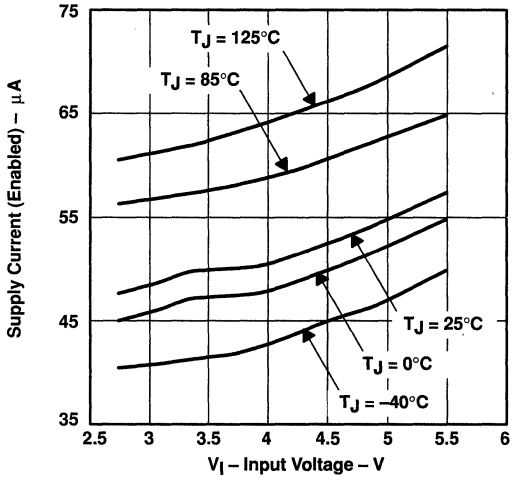


Figure 30

SUPPLY CURRENT (DISABLED)
vs
INPUT VOLTAGE

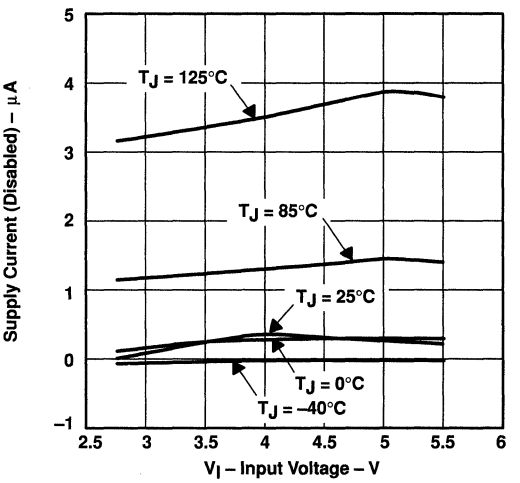


Figure 31

SHORT-CIRCUIT CURRENT LIMIT
vs
INPUT VOLTAGE

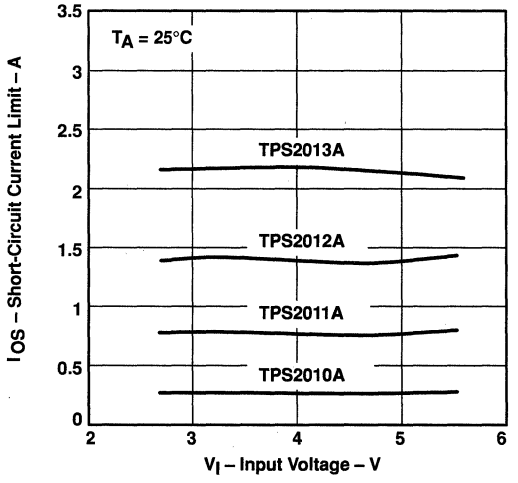


Figure 32

SHORT-CIRCUIT CURRENT LIMIT
vs
JUNCTION TEMPERATURE

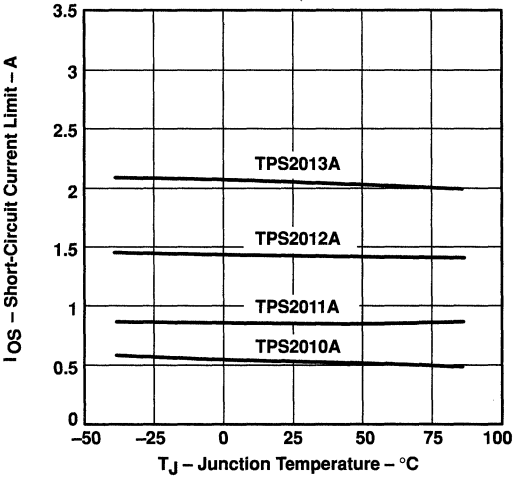


Figure 33

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
INPUT VOLTAGE

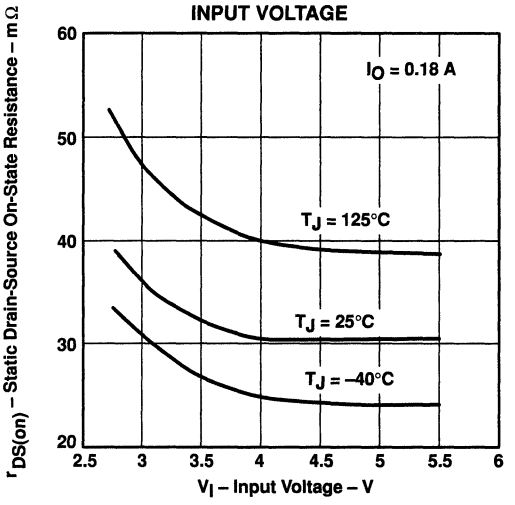


Figure 34

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

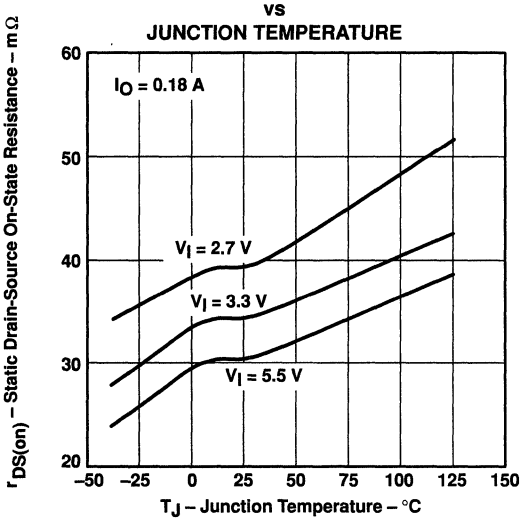


Figure 35

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
INPUT VOLTAGE

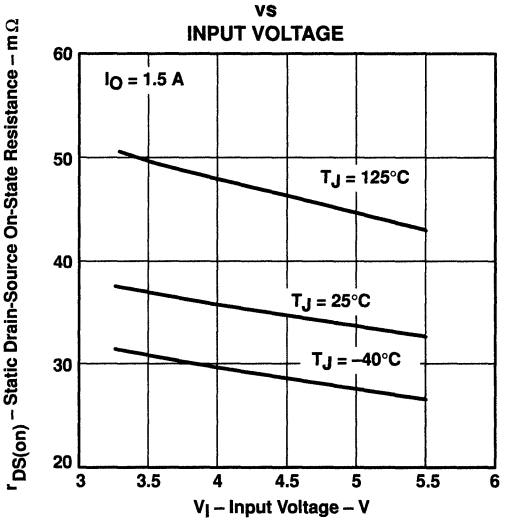


Figure 36

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

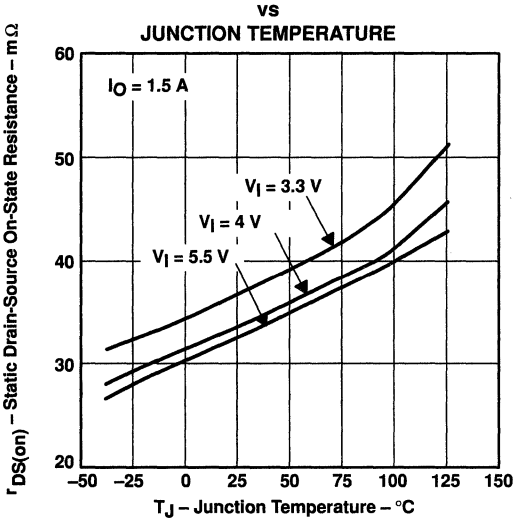


Figure 37

TYPICAL CHARACTERISTICS

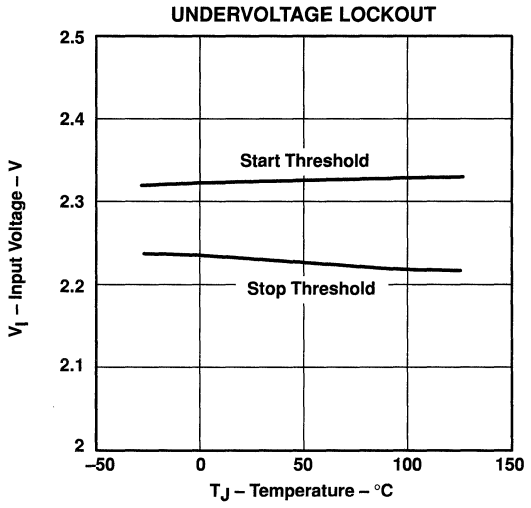


Figure 38

APPLICATION INFORMATION

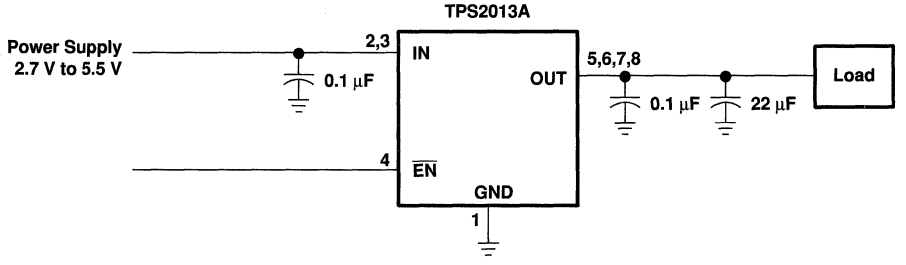


Figure 39. Typical Application

power supply considerations

A 0.01-μF to 0.1-μF ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output and input pins is recommended when the output load is heavy. This reduces power supply transients that may cause ringing on the input. Also, bypassing the output with a 0.01-μF to 0.1-μF ceramic capacitor improves the immunity of the device to short-circuit transients.

overcurrent

A sense FET checks for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

APPLICATION INFORMATION

overcurrent (continued)

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 6). The TPS201xA senses the short and immediately switches into a constant-current output.

In the second condition, the excessive load occurs while the device is enabled. At the instant the excessive load occurs, very high currents may flow for a short time before the current-limit circuit can react (see Figures 16–23). After the current-limit circuit has tripped (reached the overcurrent trip threshhold) the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figures 11–14). The TPS201xA is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

power dissipation and junction temperature

The low on-resistance on the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find $r_{DS(on)}$ at the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figures 34–37. Next, calculate the power dissipation using:

$$P_D = r_{DS(on)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient Temperature °C
$R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get an acceptable answer.

thermal protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS201xA into constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels. The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

APPLICATION INFORMATION

undervoltage lock-out (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch will be quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO will also keep the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. Upon reinsertion, the power switch will be turned on, with a controlled rise time to reduce EMI and voltage overshoots.

generic hot-plug applications (see Figure 40)

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Because of the controlled rise times and fall times of the TPS201xA series, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS201xA also ensures the switch will be off after the card has been removed, and the switch will be off during the next insertion. The UVLO feature guarantees a soft start with a controlled rise time for every insertion of the card or module.

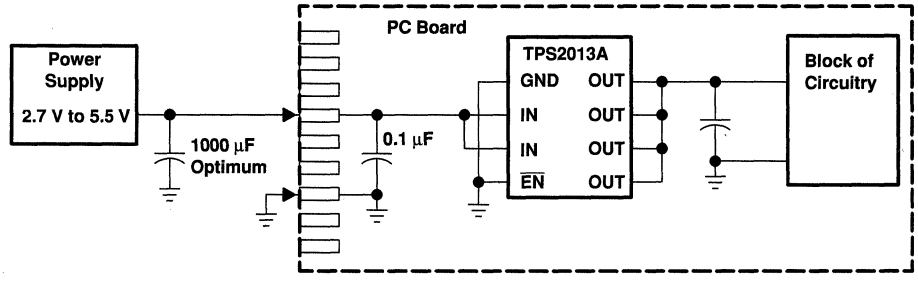


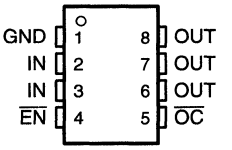
Figure 40. Typical Hot-Plug Implementation

By placing the TPS201xA between the V_{CC} input and the rest of the circuitry, the input power will reach this device first after insertion. The typical rise time of the switch is approximately 9 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

SLVS159B – DECEMBER 1996 – REVISED AUGUST 1997

- 95-mΩ Maximum (5-V Input) High-Side MOSFET Switch
- Short-Circuit Protection and Thermal Protection
- Logic Overcurrent Output
- 4-V to 7-V Operating Range
- Enable Input Compatible With 3-V and 5-V Logic
- Controlled Rise and Fall Times Limit Current Surges and Minimize EMI
- Undervoltage Lockout Ensures That Switch is Off at Start-Up
- 10-μA Maximum Standby Current
- Available in Space-Saving 8-Pin SOIC and 8-Pin PDIP
- 0°C to 125°C Operating Junction Temperature Range
- 12-kV Output, 6-kV Input Electrostatic-Discharge Protection

D OR P PACKAGE
(TOP VIEW)



description

The TPS2014 and TPS2015 power distribution switches are intended for applications where heavy capacitive loads and short circuits are likely to be encountered. The high-side switch is a 95-mΩ n-channel MOSFET. The switch is controlled by a logic enable that is compatible with 3-V and 5-V logic. Gate drive is provided by an internal charge pump designed to control the power switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 4 V.

When the output load exceeds the current-limit threshold or a short is present, the TPS20xx limits the output current to a safe level by switching into a constant-current mode, and the overcurrent logic output is set to low. Continuous heavy overloads and short circuits will increase the power dissipation in the switch and cause the junction temperature to rise. A thermal protection circuit is implemented, which shuts the switch off to prevent damage when the junction temperature exceeds its thermal limit. An undervoltage lockout is provided to ensure the switch is in the off state at start-up.

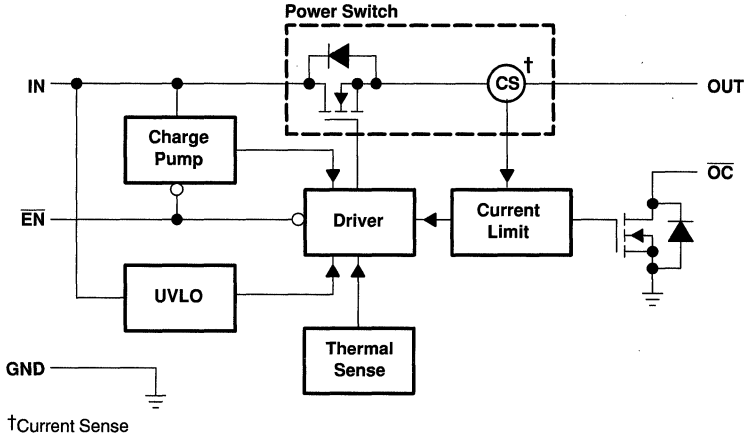
The TPS2014 and TPS2015 differ only in short-circuit current limits. The TPS2014 is designed to limit at 1.2 A load and the TPS2015 limits at 2 A (see the available options table). The TPS20xx is available in 8-pin small-outline integrated circuit (SOIC) and 8-pin PDIP packages, and operates over a junction temperature range of 0°C to 125°C.

AVAILABLE OPTIONS

T_A	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C	PACKAGED DEVICES		CHIP FORM (Y)
			SOIC (D)†	PDIP (P)	
0°C TO 85°C	0.6 A	1.2 A	TPS2014D	TPS2014P	TPS2014Y
	1 A	2 A	TPS2015D	TPS2015P	TPS2015Y

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2014DR).

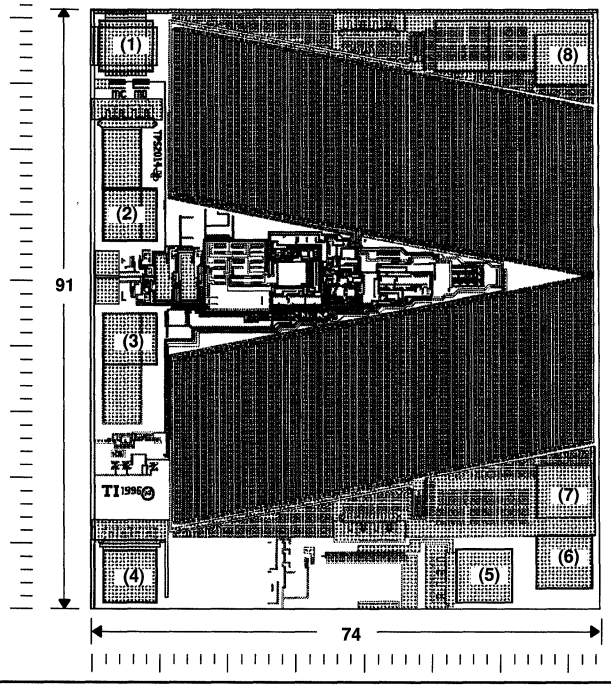
functional block diagram

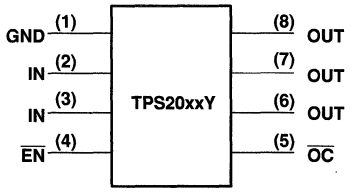


TPS20xxY chip information

This chip, when properly assembled, displays characteristics similar to those of the TPS20xx. Ultrasonic bonding may be used on the doped aluminium bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAl

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{EN}$	4	I	Enable input. Logic low at $\overline{EN}$ turns the power switch on.
GND	1	I	Ground
$\overline{IN}$	2, 3	I	Input voltage
$\overline{OC}$	5	O	$\overline{OC}$ is asserted active low during a fault condition.
OUT	6–8	O	Power switch output

detailed description

power switch

The power switch is an n-channel MOSFET with a maximum on-state resistance of 95 mΩ ($V_{I(IN)}$ = 5 V), configured as a high-side switch.

charge pump

An internal 100-kHz charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 4 V and requires very little supply current.

driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 4-ms range instead of the microsecond or nanosecond range for a standard FET.

enable ($\overline{EN}$)

A logic high on $\overline{EN}$ turns off the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10 μA. A logic zero input restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

overcurrent ($\overline{OC}$)

$\overline{OC}$ is an open-drain logic output that is asserted (active low) when an overload or short circuit is encountered. The output remains asserted until the overload or short-circuit condition is removed.

current sense

A sense FET monitors the current supplied to the load. The sense FET provides a much more efficient way to measure current than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its linear region, which switches the output into a constant current mode and simply holds the current constant while varying the voltage on the load.

thermal sense

An internal thermal-sense circuit shuts off the power switch when the junction temperature rises to approximately to 180°C. Hysteresis is built into the thermal sense circuit. After the device has cooled approximately 20°C, the switch turns back on. The switch continues to cycle off and on until the fault is removed.

undervoltage lockout

An internal voltage sense monitors the input voltage. When the input voltage is below 3.2 V nominal, a control signal turns off the power switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, V_I (see Note1) ..... –0.3 V to 7 V
Output voltage range, V_O (see Note1) ..... –0.3 V to $V_{I(IN)}$ + 0.3 V
Input voltage range, V_I at $\overline{EN}$ ..... –0.3 V to 7 V
Continuous output current, I_O ..... internally limited
Continuous total power dissipation ..... See Dissipation Rating Table
Operating virtual junction temperature range, T_J ..... 0°C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
P	1175 mW	9.4 mW/°C	752 mW	235 mW
D	725 mW	5.8 mW/°C	464 mW	145 mW

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I		4	5.5	V
Input voltage, V_I at $\overline{EN}$		0	5.5	V
Continuous output current, I_O	TPS2014	0	0.6	A
	TPS2015	0	1	
Operating virtual junction temperature, T_J		0	125	°C

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $\overline{EN}$ = 0 V (unless otherwise noted)

power switch

PARAMETER		TEST CONDITIONS†			MIN	TYP	MAX	UNIT
r_{on}	On-state resistance	V_I = 5.5 V,	T_J = 25°C			75	95	mΩ
		V_I = 5 V,	T_J = 25°C			80	95	
		V_I = 4.5V,	T_J = 25°C			90	110	
		V_I = 4 V,	T_J = 25°C			96	110	
I_{lkg}	Leakage current, output	$\overline{EN}$ = V_I,	T_J = 25°C			0.001	1	µA
		$\overline{EN}$ = V_I,	0°C ≤ T_J ≤ 125°C				10	
t_r	Rise time, output	V_I = 5.5 V,	T_J = 25°C	C_L = 1 µF		4		ms
		V_I = 4 V,	T_J = 25°C	C_L = 1 µF		3.8		
t_f	Fall time, output	V_I = 5.5 V,	T_J = 25°C	C_L = 1 µF		3.9		ms
		V_I = 4 V,	T_J = 25°C	C_L = 1 µF		3.5		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $\overline{EN}$ = 0 V (unless otherwise noted) (continued)

enable input ($\overline{EN}$)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{IH}	High-level input voltage	4 V ≤ V_I ≤ 5.5 V	2		V
V_{IL}	Low-level input voltage	4 V ≤ V_I ≤ 5.5 V		0.8	V
I_I	Input current	$\overline{EN}$ = 0 V or $\overline{EN}$ = V_I	–0.5	0.5	μA
t_{PLH}	Propagation (delay) time, low to high output	C_L = 1 μF		20	ms
t_{PHL}	Propagation (delay) time, high to low output	C_L = 1 μF		40	

current limit

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
I_{OS}	Short-circuit output current	T_J = 25°C, V_I = 5.5 V	TPS2014	0.66	1.2	1.8	A
			TPS2015	1.1	2	3	

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

supply current

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DDL}	Supply current, low-level output	$\overline{EN}$ = V_I	T_J = 25°C		0.015	10	μA
			0°C ≤ T_J ≤ 125°C			10	
I_{DDH}	Supply current, high-level output	$\overline{EN}$ = 0 V	T_J = 25°C		73	100	μA
			0°C ≤ T_J ≤ 125°C			100	

undervoltage lockout

PARAMETER		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage	2	3.2	4	V

$\overline{OC}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OS}	Short-circuit output current	0°C ≤ T_J ≤ 125°C			5	mA
V_{OL}	Low-level output voltage	0°C ≤ T_J ≤ 125°C			0.3	

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $\overline{EN}$ = 0 V (unless otherwise noted)

power switch

PARAMETER		TEST CONDITIONS†			TPS2014Y, TPS2015Y MIN	TPS2014Y, TPS2015Y TYP	TPS2014Y, TPS2015Y MAX	UNIT
r_{on}	On-state resistance	V_I = 5.5 V,	T_J = 25°C			75		mΩ
		V_I = 5 V,	T_J = 25°C			80		
		V_I = 4.5V,	T_J = 25°C			90		
		V_I = 4 V,	T_J = 25°C			96		
I_{lkg}	Leakage current, output	$\overline{EN}$ = V_I,	T_J = 25°C			0.001		µA
		$\overline{EN}$ = V_I,	0°C ≤ T_J ≤ 125°C			10		
t_r	Rise time, output	V_I = 5.5 V,	T_J = 25°C	C_L = 1 µF		4		ms
		V_I = 4 V,	T_J = 25°C	C_L = 1 µF		3.8		
t_f	Fall time, output	V_I = 5.5 V,	T_J = 25°C	C_L = 1 µF		3.9		ms
		V_I = 4 V,	T_J = 25°C	C_L = 1 µF		3.5		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

enable input ($\overline{EN}$)

PARAMETER		TEST CONDITIONS	TPS2014Y, TPS2015Y MIN	TPS2014Y, TPS2015Y TYP	TPS2014Y, TPS2015Y MAX	UNIT
V_{IH}	High-level input voltage	4 V ≤ V_I ≤ 5.5 V		2		V
V_{IL}	Low-level input voltage	4 V ≤ V_I ≤ 5.5 V		0.8		V
I_I	Input current	$\overline{EN}$ = 0 V or $\overline{EN}$ = V_I		0.5		µA
t_{PLH}	Propagation (delay) time, low to high output	C_L = 1 µF		20		ms
t_{PHL}	Propagation (delay) time, high to low output	C_L = 1 µF		40		

current limit

PARAMETER		TEST CONDITIONS†		TPS2014Y, TPS2015Y MIN	TPS2014Y, TPS2015Y TYP	TPS2014Y, TPS2015Y MAX	UNIT
I_{OS}	Short-circuit output current	T_J = 25°C, V_I = 5.5 V	TPS2014		1.2		A
			TPS2015		2		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

supply current

PARAMETER		TEST CONDITIONS		TPS2014Y, TPS2015Y MIN	TPS2014Y, TPS2015Y TYP	TPS2014Y, TPS2015Y MAX	UNIT
I_{DDL}	Supply current, low-level output	$\overline{EN}$ = V_I	T_J = 25°C		0.015		µA
			0°C ≤ T_J ≤ 125°C		10		
I_{DDH}	Supply current, high-level output	$\overline{EN}$ = 0 V	T_J = 25°C		73		µA
			0°C ≤ T_J ≤ 125°C		100		

undervoltage lockout

PARAMETER		TPS2014Y, TPS2015Y MIN	TPS2014Y, TPS2015Y TYP	TPS2014Y, TPS2015Y MAX	UNIT
V_{IL}	Low-level input voltage		3.2		V

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $\overline{EN}$ = 0 V (unless otherwise noted) (continued)

$\overline{OC}$

PARAMETER		TEST CONDITIONS	TPS2014Y, TPS2015Y			UNIT
			MIN	TYP	MAX	
I_{OS}	Short-circuit output current	$0°C \le T_J \le 125°C$		5		mA
V_{OL}	Low-level output voltage	$0°C \le T_J \le 125°C$		0.3		

PARAMETER MEASUREMENT INFORMATION

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Propagation Delay and Rise Time With 1-μF Load, $V_{I(IN)}$ = 5 V	1
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TPS2015 Short-Circuit Current. Short is Applied to Enabled Device, $V_{I(IN)}$ = 5 V	4
TPS2014 Threshold Current, $V_{I(IN)}$ = 5 V	5
TPS2015 Threshold Current, $V_{I(IN)}$ = 5 V	6
TPS2014 (Enabled) into Short Circuit, $V_{I(IN)}$ = 5 V	7
TPS2015 (Enabled) into Short Circuit, $V_{I(IN)}$ = 5 V	8

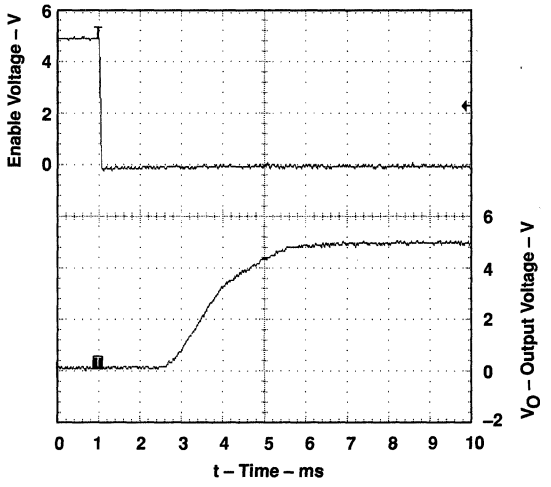

Figure 1. Propagation Delay and Rise Time With 1-μF Load, $V_{I(IN)}$ = 5 V

PARAMETER MEASUREMENT INFORMATION

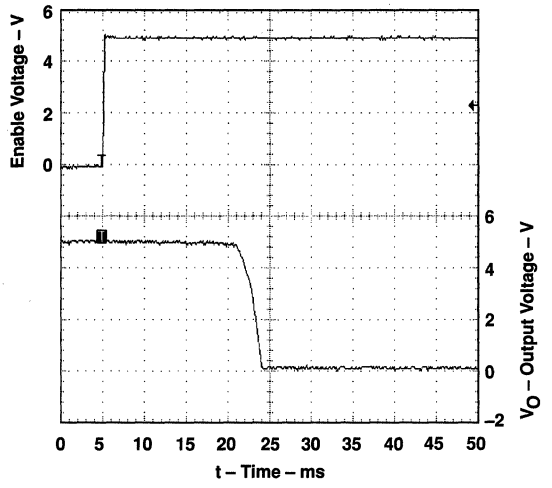

Figure 2. Propagation Delay and Fall Time With 1-μF Load, $V_{I(IN)}$ = 5 V

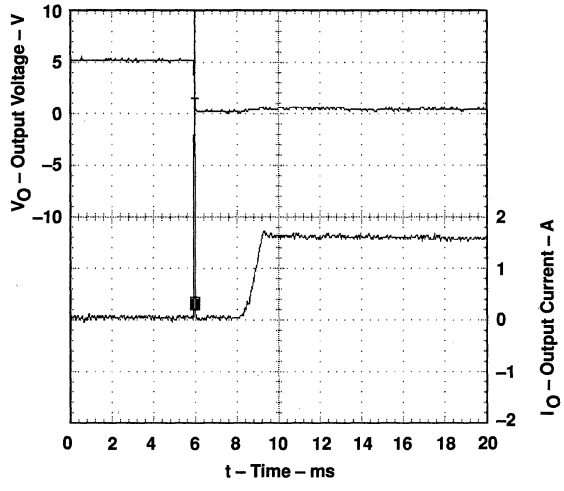

Figure 3. TPS2014 Short-Circuit Current. Short is Applied to Enabled Device, $V_{I(IN)}$ = 5 V

PARAMETER MEASUREMENT INFORMATION

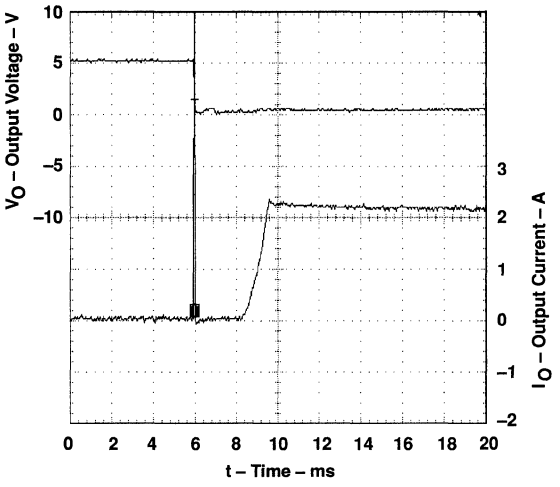

Figure 4. TPS2015 Short-Circuit Current. Short is Applied to Enabled Device, $V_{I(IN)}$ = 5 V

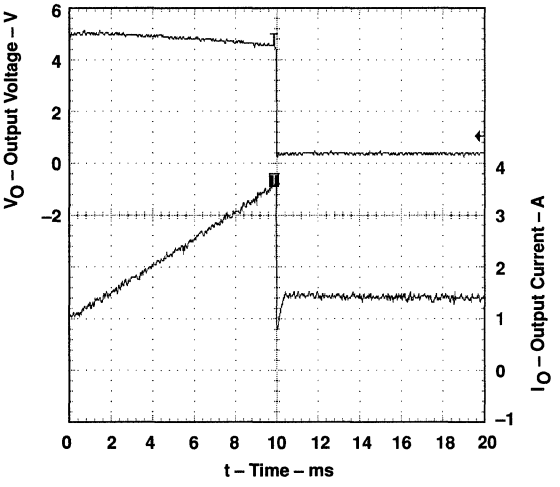

Figure 5. TPS2014 Threshold Current, $V_{I(IN)}$ = 5 V

PARAMETER MEASUREMENT INFORMATION

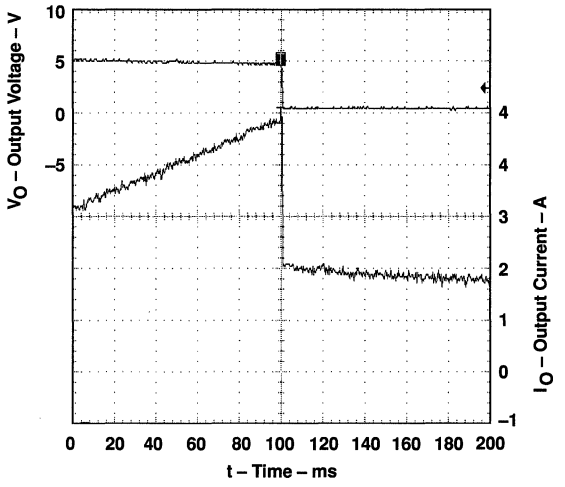

Figure 6. TPS2015 Threshold Current, $V_{I(IN)}$ = 5 V

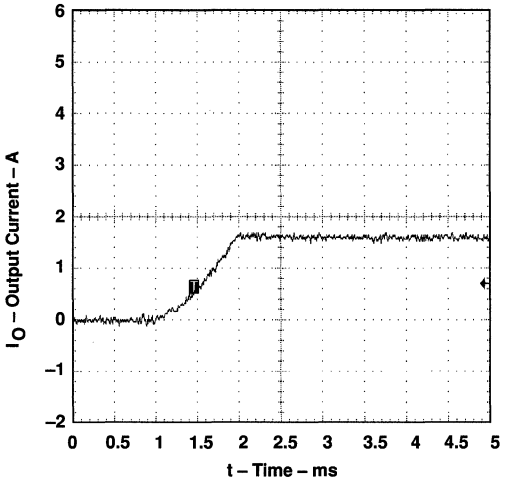

Figure 7. TPS2014 (Enabled) into Short Circuit, $V_{I(IN)}$ = 5 V

PARAMETER MEASUREMENT INFORMATION

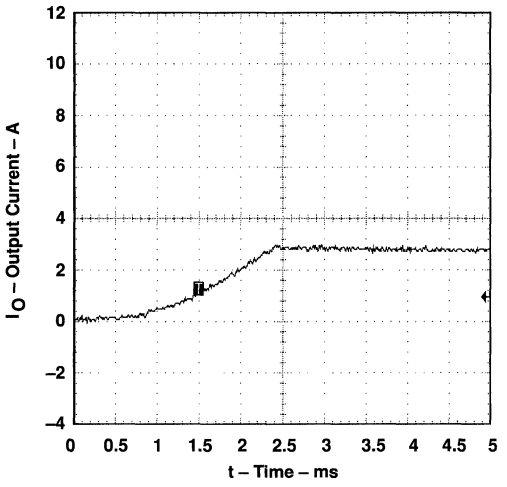

Figure 8. TPS2015 (Enabled) into Short Circuit, $V_{I(IN)}$ = 5 V

TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS

TURN-ON DELAY TIME
vs
INPUT VOLTAGE

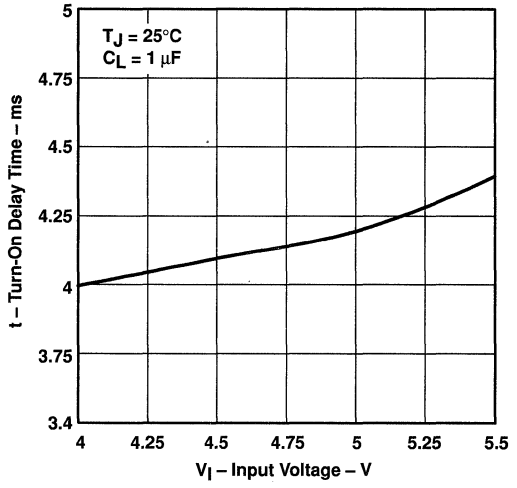


Figure 9

TURN-OFF DELAY TIME
vs
INPUT VOLTAGE

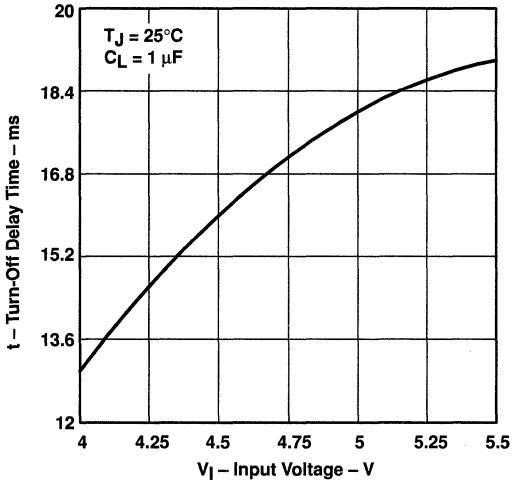


Figure 10

RISE TIME
vs
OUTPUT CURRENT

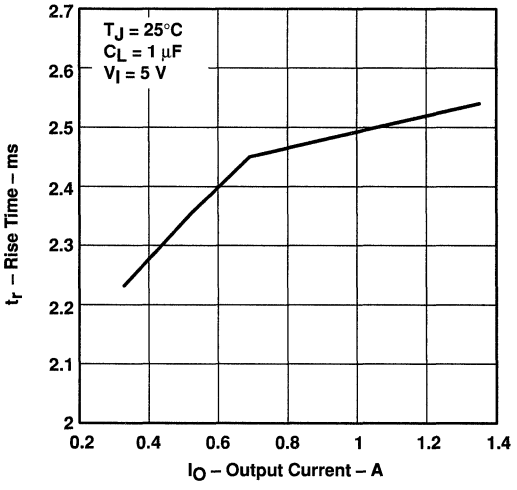


Figure 11

FALL TIME
vs
OUTPUT CURRENT

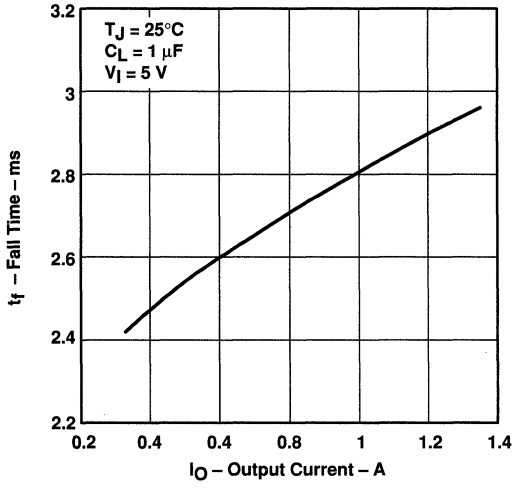


Figure 12

TYPICAL CHARACTERISTICS

SUPPLY CURRENT, OUTPUT ENABLED
vs
JUNCTION TEMPERATURE

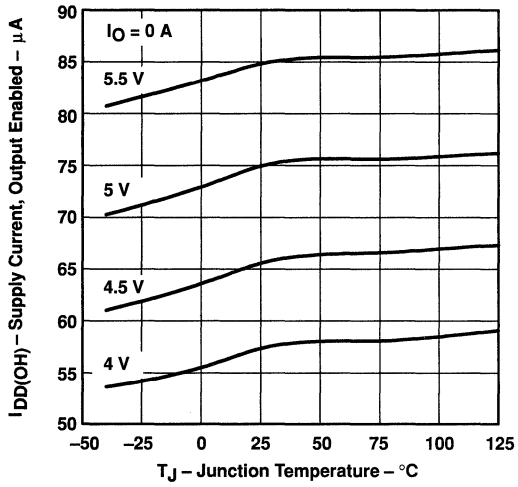


Figure 13

SUPPLY CURRENT, OUTPUT DISABLED
vs
JUNCTION TEMPERATURE

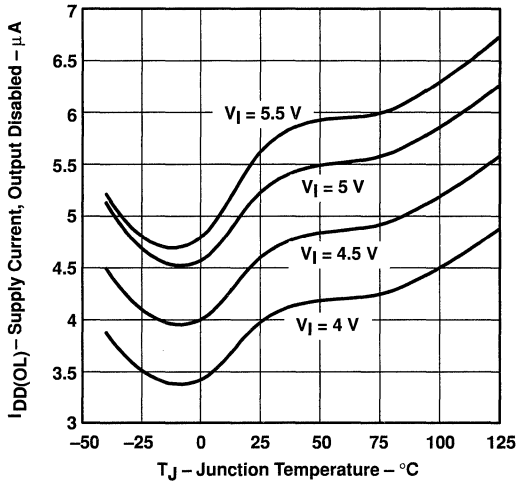


Figure 14

SUPPLY CURRENT, OUTPUT ENABLED
vs
INPUT VOLTAGE

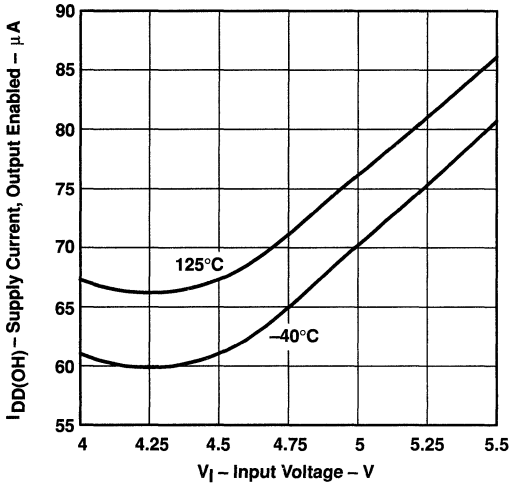


Figure 15

SUPPLY CURRENT, OUTPUT DISABLED
vs
INPUT VOLTAGE

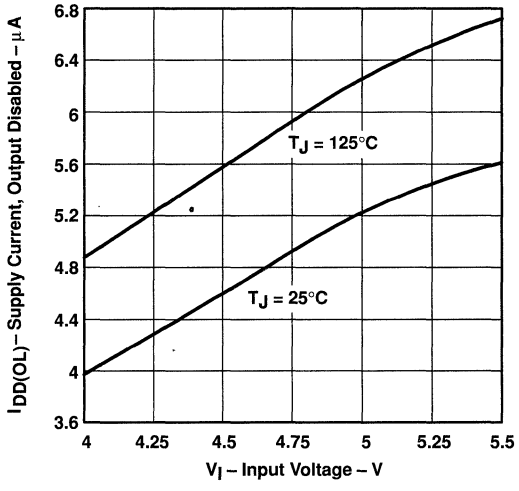


Figure 16

TYPICAL CHARACTERISTICS

ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

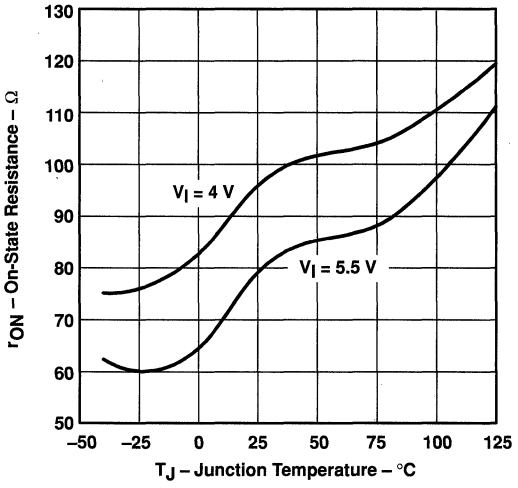


Figure 17

ON-STATE RESISTANCE
vs
INPUT VOLTAGE

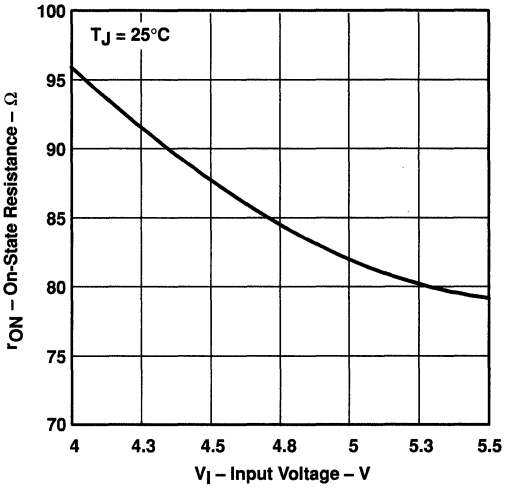


Figure 18

INPUT VOLTAGE TO OUTPUT VOLTAGE
vs
INPUT VOLTAGE

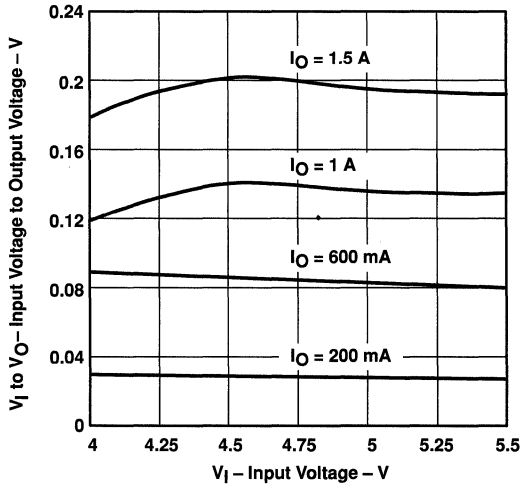


Figure 19

SHORT-CIRCUIT OUTPUT CURRENT
vs
INPUT VOLTAGE

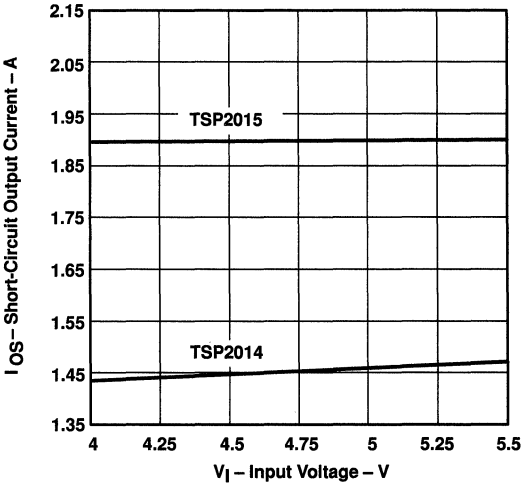


Figure 20

TYPICAL CHARACTERISTICS

THRESHOLD TRIP CURRENT
vs
INPUT VOLTAGE

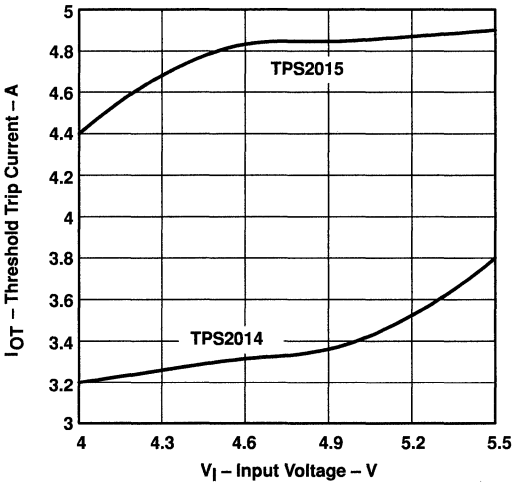


Figure 21

SHORT-CIRCUIT OUTPUT CURRENT
vs
JUNCTION TEMPERATURE

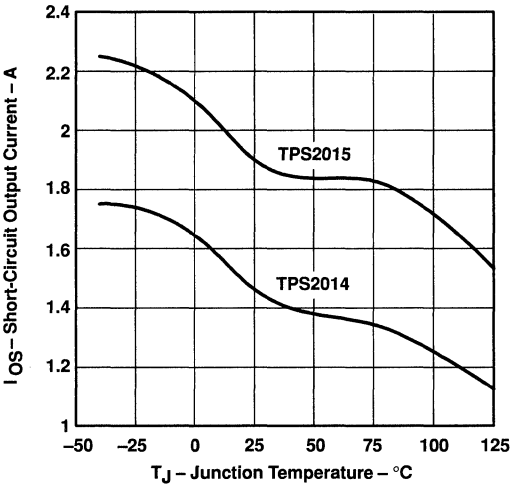


Figure 22

UVLO TRIP VOLTAGE
vs
JUNCTION TEMPERATURE

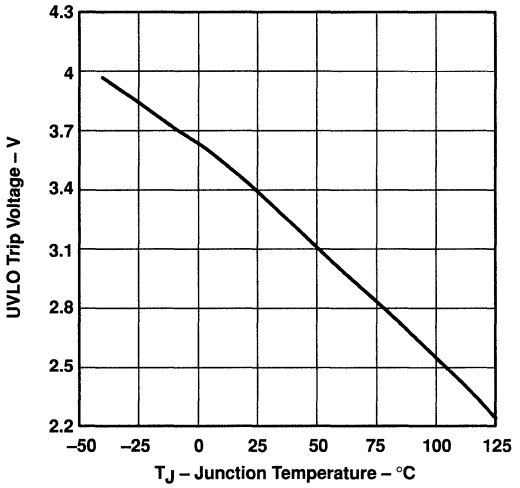


Figure 23

APPLICATION INFORMATION

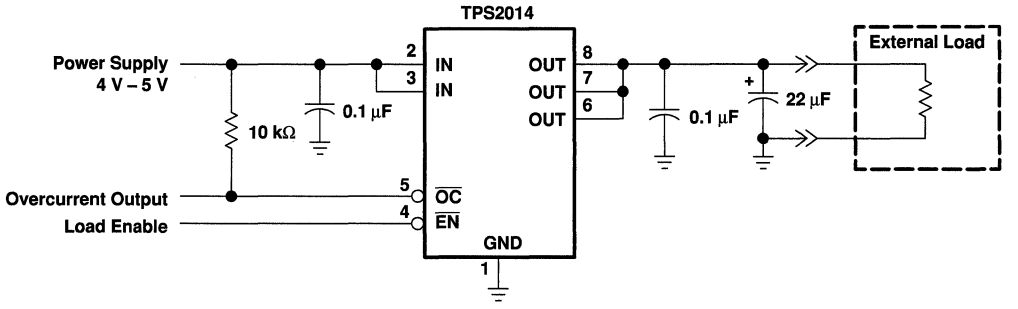


Figure 24. Typical Application

power supply considerations

The TPS20xx has multiple inputs and outputs that must be connected in parallel to minimize voltage drop and prevent unnecessary power dissipation.

A 0.1-µF ceramic bypass capacitor between IN and GND, close to the device, is recommended. A high-value electrolytic capacitor is also desirable when the output load is heavy or has large paralleled capacitors. Bypassing the output with a 0.1-µF ceramic capacitor improves the immunity of the device to electrostatic discharge (ESD).

overcurrent

A sense FET is employed to check for overcurrent conditions. Unlike sense resistors and polyfuses, sense FETs do not increase series resistance to the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Shutdown only occurs when the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figures 7 and 8). The TPS20xx senses the short and immediately switches into a constant-current output.

Under the second condition, the short occurs while the device is enabled. At the instant the short occurs, very high currents flow for a short time before the current-limit circuit can react (see Figures 3 and 4). After the current-limit circuit has tripped, the device limits normally.

Under the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached (see Figures 5 and 6). The TPS20xx is capable of delivering current up to the current-limit threshold without damage. When the threshold has been reached, the device switches into its constant-current mode.

APPLICATION INFORMATION

power dissipation and junction temperature

The low on-resistance of the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistance of these packages is high compared to that of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find r_{on} at the input voltage and at the operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read r_{on} from Figure 17. Next calculate the power dissipation using:

$$P_D = r_{on} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient temperature

$R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W, P = 106°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

thermal protection

Thermal protection is provided to prevent damage to the IC when heavy-overload or a short-circuit fault is present for an extended period of time. The fault forces the TPS20xx into constant current mode, which causes the voltage across the high-side switch to increase. Under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to dangerously high levels. The protection circuit senses the junction temperature of the switch and shuts it off. The switch remains off until the junction temperature has dropped approximately 20°C. The switch continues to cycle in this manner until the load fault or the input power is removed.

undervoltage lockout

An undervoltage lockout is provided to ensure that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 3.2 V, the power switch quickly turns off. This facilitates the design of hot-insertion systems that may not have the ability to turn off the power switch before input power is removed. Upon reapplication of the input voltage (if enabled), the power switch turns on with a controlled rise time to reduce inrush current, EMI, and voltage overshoots.

For proper operation of the UVLO, the TPS20xx requires the voltage decay from 3 V to 2 V to take at least 200 µs. Capacitance is added to the input or output of the TPS20xx to increase this decay rate. Capacitance is generally added to the output to lower inrush current due to input capacitance.

Universal Serial Bus (USB) applications

The USB specification provides for five different classes of devices based on their power sourcing and sinking requirements. These classes of devices are: bus-powered hub, self-powered hub, lower power bus-powered function, high power bus-powered function, and self-powered functions. The TPS20xx can provide power distribution solutions for many of these devices.

APPLICATION INFORMATION

bus-powered and self-power hubs

Hubs provide data and power for downstream functions through output ports. Self-power hubs have internal power supplies that furnish power to downstream functions. Each port is required to supply 500 mA continuous to a downstream function. Each port must have overcurrent protection to meet the requlatory safety limit that no single port can deliver more than 5 A. The self-power hub must also have a method to detect and report an overcurrent condition to the USB host. The TPS20xx provides the required current-limiting function and has an overcurrent logic output to inform the hub controller of the fault condition. The on-state resistance of the TPS20xx is low enough to meet all USB voltage regulation requirements. The switch also provides the capability to remove power from a faulted port.

Bus-powered hubs distribute power and data from an input port to downstream ports. Each output port is required to supply 100 mA continuous. A bus-powered hub is not required to provide overcurrent protection because it is provided by the upstream port. In order to power up in a low power state, the self-powered hub must be able to switch power to its output ports. The TPS20xx can also provide this function.

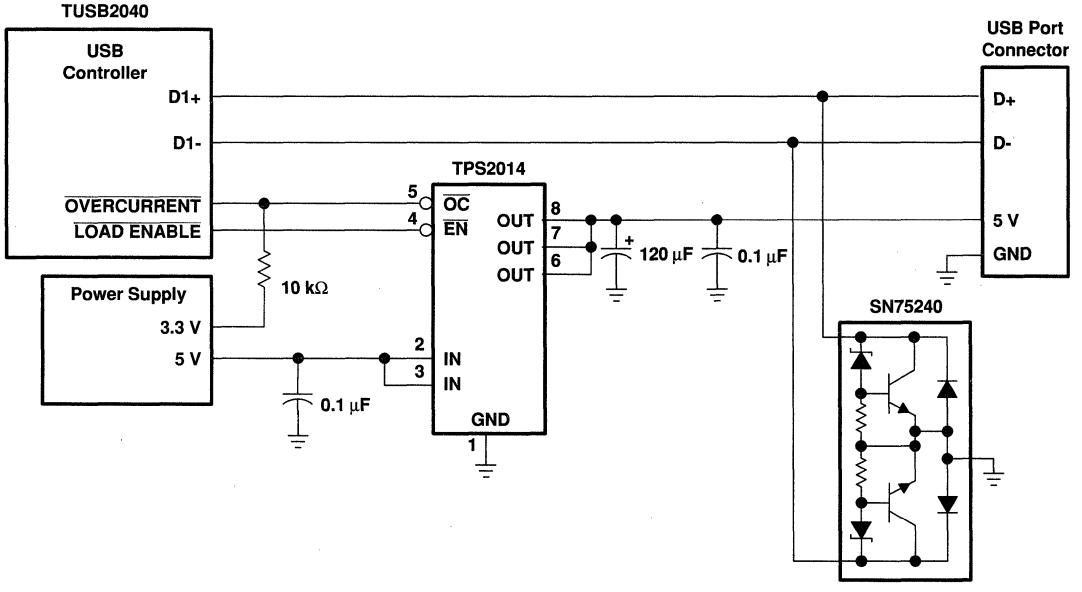


Figure 25. Typical USB Self-Powered Hub Application

low power bus-powered functions and high power bus-powered functions

Low-power and high-power bus-powered functions are powered by their input ports. If the load of the function is more than the parallel combination of 44 Ω and 10 µF, it must implement inrush current limiting. The TPS20xx provides this function with its controlled rise time during turn on.

APPLICATION INFORMATION

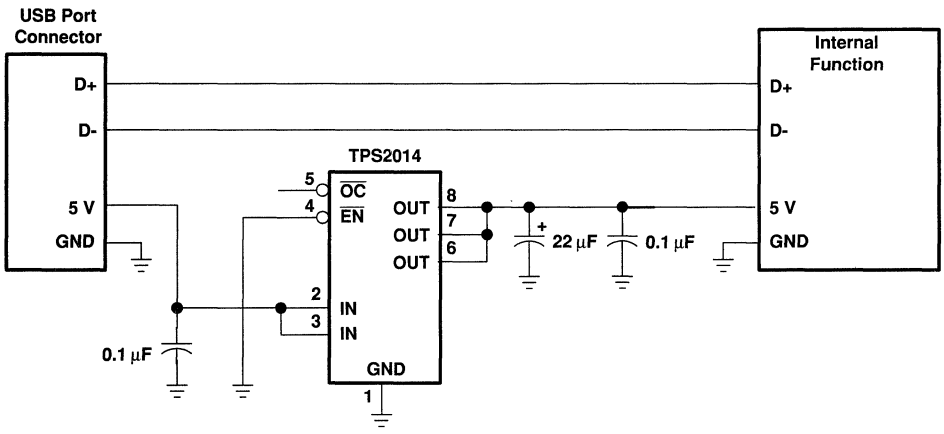


Figure 26. Typical USB Bus-Powered Function Application

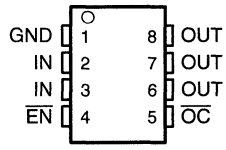
ESD protection

All TPS20xx terminals incorporate ESD-protection circuitry designed to withstand a 6-kV human-body-model discharge as defined in MIL-STD-883C. Additionally, the output is protected from discharges up to 12 kV.

SLVS175 – DECEMBER 1998

- 50-mΩ -Maximum (5-V Input) High-Side MOSFET Switch
- Short-Circuit and Thermal Protection
- Overcurrent Logic Output
- Operating Range . . . 2.7 V to 5.5 V
- Logic-Level Enable Input
- Typical Rise Time . . . 6.1 ms
- Undervoltage Lockout
- Maximum Standby Supply Current . . . 10 μA
- No Drain-Source Back-Gate Diode
- Available in 8-pin SOIC and PDIP Packages
- Ambient Temperature Range, –40°C to 85°C
- 2-kV Human-Body-Model, 200-V Machine-Model ESD Protection

D OR P PACKAGE
(TOP VIEW)



description

The TPS202x family of power distribution switches is intended for applications where heavy capacitive loads and short circuits are likely to be encountered. These devices are 50-mΩ N-channel MOSFET high-side power switches. The switch is controlled by a logic enable compatible with 5-V logic and 3-V logic. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the TPS202x limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{OC}$) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until valid input voltage is present.

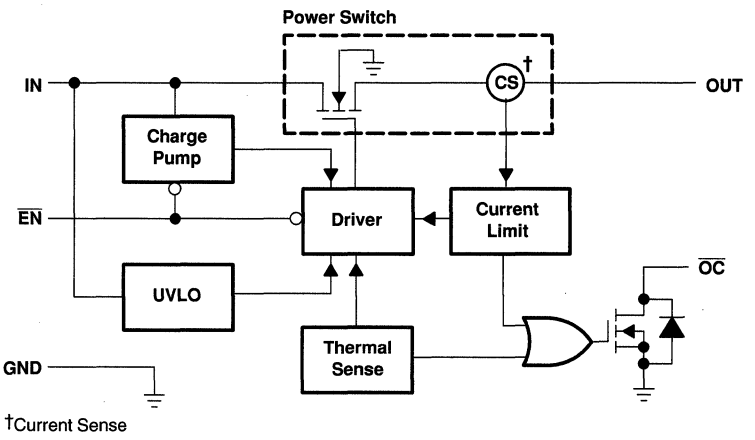
The TPS202x devices differ only in short-circuit current threshold. The TPS2020 limits at 0.3-A load, the TPS2021 at 0.9-A load, the TPS2022 at 1.5-A load, the TPS2023 at 2.2-A load, and the TPS2024 at 3-A load (see Available Options). The TPS202x is available in an 8-pin small-outline integrated-circuit (SOIC) package and in an 8-pin dual-in-line (DIP) package and operates over a junction temperature range of –40°C to 125°C.

AVAILABLE OPTIONS

T_A	ENABLE	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A)	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (A)	PACKAGED DEVICES	
				SMALL OUTLINE (D)†	PLASTIC DIP (P)
–40°C to 85°C	Active low	0.2	0.3	TPS2020D	TPS2020P
		0.6	0.9	TPS2021D	TPS2021P
		1	1.5	TPS2022D	TPS2022P
		1.5	2.2	TPS2023D	TPS2023P
		2	3	TPS2024D	TPS2024P

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2020DR)

TPS2020 functional block diagram



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO. D OR P		
$\overline{EN}$	4	I	Enable input. Logic low turns on power switch.
GND	1	I	Ground
IN	2, 3	I	Input voltage
$\overline{OC}$	5	O	Overcurrent. Logic output active low
OUT	6, 7, 8	O	Power-switch output

detailed description

power switch

The power switch is an N-channel MOSFET with a maximum on-state resistance of 50 mΩ ($V_{I(IN)}$ = 5 V). Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled.

charge pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 9-ms range.

enable ($\overline{EN}$)

The logic enable disables the power switch, the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10 μA when a logic high is present on $\overline{EN}$. A logic zero input on $\overline{EN}$ restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

overcurrent ($\overline{OC}$)

The $\overline{OC}$ open drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed.

current sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant current mode and holds the current constant while varying the voltage on the load.

thermal sense

An internal thermal-sense circuit shuts off the power switch when the junction temperature rises to approximately 140°C. Hysteresis is built into the thermal sense circuit. After the device has cooled approximately 20°C, the switch turns back on. The switch continues to cycle off and on until the fault is removed.

undervoltage lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, $V_{I(IN)}$ (see Note 1) ..... −0.3 V to 6 V
Output voltage range, $V_{O(OUT)}$ (see Note 1) ..... −0.3 V to $V_{I(IN)}$ + 0.3 V
Input voltage range, $V_{I(\overline{EN})}$ ..... −0.3 V to 6 V
Continuous output current, $I_{O(OUT)}$ ..... internally limited
Continuous total power dissipation ..... See Dissipation Rating Table
Operating virtual junction temperature range, T_J ..... −40°C to 125°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1175 mW	9.4 mW/°C	752 mW	611 mW

recommended operating conditions

		MIN	MAX	UNIT
Input voltage	$V_{I(IN)}$	2.7	5.5	V
	$V_{I(\overline{EN})}$	0	5.5	V
Continuous output current, I_O	TPS2020	0	0.2	A
	TPS2021	0	0.6	
	TPS2022	0	1	
	TPS2023	0	1.5	
	TPS2024	0	2	
Operating virtual junction temperature, T_J		−40	125	°C

electro static discharge (ESD) protection

	MIN	MAX	UNIT
Human Body Model MIL-STD-883C		2	kV
Machine model		0.2	kV

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $\overline{EN}$ = 0 V (unless otherwise noted)

power switch

PARAMETER		TEST CONDITIONS†			MIN	TYP	MAX	UNIT
$r_{DS(on)}$	Static drain-source on-state resistance	$V_{I(IN)}$ = 5 V,	T_J = 25°C,	I_O = 1.8 A		33	36	mΩ
		$V_{I(IN)}$ = 5 V,	T_J = 85°C,	I_O = 1.8 A		38	46	
		$V_{I(IN)}$ = 5 V,	T_J = 125°C,	I_O = 1.8 A		44	50	
		$V_{I(IN)}$ = 3.3 V,	T_J = 25°C,	I_O = 1.8 A		37	41	
		$V_{I(IN)}$ = 3.3 V,	T_J = 85°C,	I_O = 1.8 A		43	52	
		$V_{I(IN)}$ = 3.3 V,	T_J = 125°C,	I_O = 1.8 A		51	61	
		$V_{I(IN)}$ = 5 V,	T_J = 25°C,	I_O = 0.18 A		30	34	
		$V_{I(IN)}$ = 5 V,	T_J = 85°C,	I_O = 0.18 A		35	41	
		$V_{I(IN)}$ = 5 V,	T_J = 125°C,	I_O = 0.18 A		39	47	
		$V_{I(IN)}$ = 3.3 V,	T_J = 25°C,	I_O = 0.18 A		33	37	
		$V_{I(IN)}$ = 3.3 V,	T_J = 85°C,	I_O = 0.18 A		39	46	
		$V_{I(IN)}$ = 3.3 V,	T_J = 125°C,	I_O = 0.18 A		44	56	
t_r	Rise time, output	$V_{I(IN)}$ = 5.5 V, C_L = 1 µF,	T_J = 25°C, R_L = 10 Ω			6.1		ms
		$V_{I(IN)}$ = 2.7 V, C_L = 1 µF,	T_J = 25°C, R_L = 10 Ω			8.6		
t_f	Fall time, output	$V_{I(IN)}$ = 5.5 V, C_L = 1 µF,	T_J = 25°C, R_L = 10 Ω			3.4		ms
		$V_{I(IN)}$ = 2.7 V, C_L = 1 µF,	T_J = 25°C, R_L = 10 Ω			3		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

enable input ($\overline{EN}$)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V	2			V
V_{IL}	Low-level input voltage	4.5 V ≤ $V_{I(IN)}$ ≤ 5.5 V			0.8	V
		2.7 V ≤ $V_{I(IN)}$ ≤ 4.5 V			0.5	
I_I	Input current	$\overline{EN}$= 0 V or $\overline{EN}$ = $V_{I(IN)}$	−0.5		0.5	µA
t_{on}	Turn-on time	C_L = 100 µF, R_L = 10 Ω			20	ms
t_{off}	Turn-off time	C_L = 100 µF, R_L = 10 Ω			40	

current limit

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
I_{OS}	Short-circuit output current	T_J = 25°C, V_I = 5.5 V, OUT connected to GND, Device enable into short circuit	TPS2020	0.22	0.3	0.4	A
			TPS2021	0.66	0.9	1.1	
			TPS2022	1.1	1.5	1.8	
			TPS2023	1.65	2.2	2.7	
			TPS2024	2.2	3	3.8	

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $\overline{EN}$ = 0 V (unless otherwise noted) (continued)

supply current

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Supply current, low-level output	No Load on OUT	$\overline{EN}$ = $V_{I(IN)}$	T_J = 25°C		0.3	1	µA
			−40°C ≤ T_J ≤ 125°C			10	
Supply current, high-level output	No Load on OUT	$\overline{EN}$ = 0 V	T_J = 25°C		58	75	µA
			−40°C ≤ T_J ≤ 125°C		75	100	
Leakage current	OUT connected to ground	$\overline{EN}$ = $V_{I(IN)}$	−40°C ≤ T_J ≤ 125°C		10		µA

undervoltage lockout

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low-level input voltage		2		2.5	V
Hysteresis	T_J = 25°C		100		mV

overcurrent ($\overline{OC}$)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output low voltage	I_O = 10 mA, $V_{OL(\overline{OC})}$			0.4	V
Off-state current†	V_O = 5 V, V_O = 3.3 V			1	µA

† Specified by design, not production tested.

PARAMETER MEASUREMENT INFORMATION

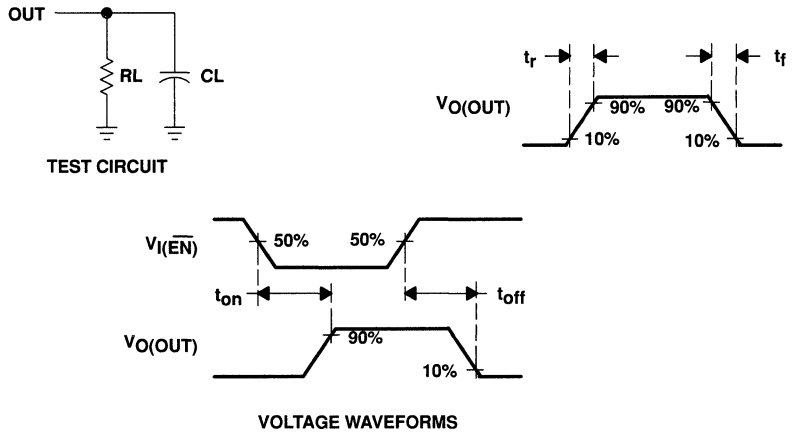


Figure 1. Test Circuit and Voltage Waveforms

Table of Timing Diagrams

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Turn-on Delay and Rise TIme	2
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TPS2020, TPS2021, TPS2022, TPS2023, and TPS2024, Ramped Load on Enabled Device	12, 13, 14, 15,16
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1.2-Ω Load Connected to an Enabled TPS2023 Device	24
0.9-Ω Load Connected to an Enabled TPS2023 Device	25
0.9-Ω Load Connected to an Enabled TPS2024 Device	26
0.5-Ω Load Connected to an Enabled TPS2024 Device	27

PARAMETER MEASUREMENT INFORMATION

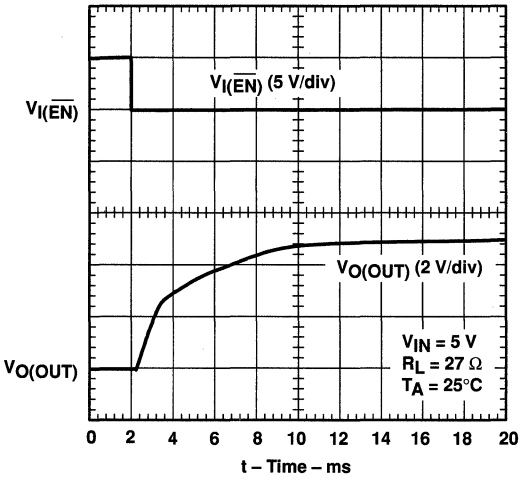

Figure 2. Turn-on Delay and Rise Time

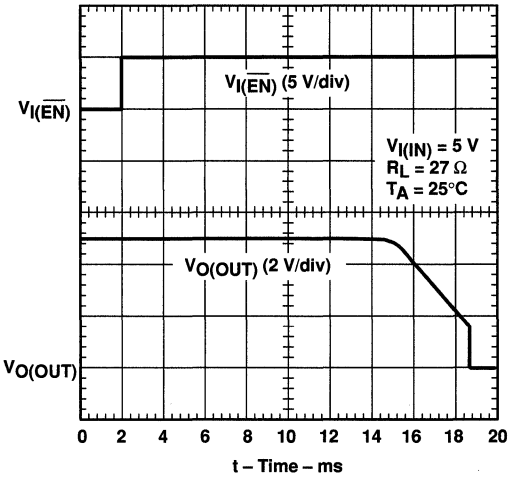

Figure 3. Turn-off Delay and Fall Time

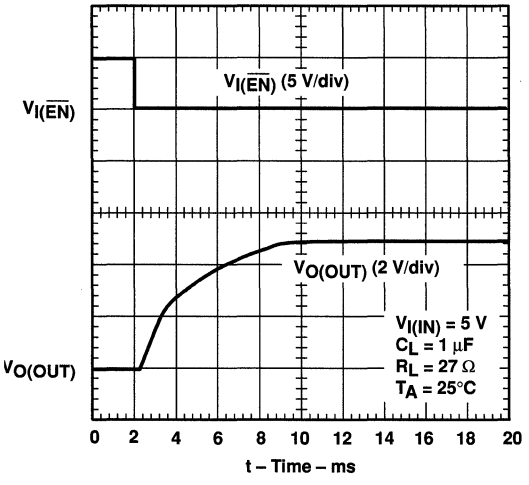

Figure 4. Turn-on Delay and Rise Time With 1-μF Load

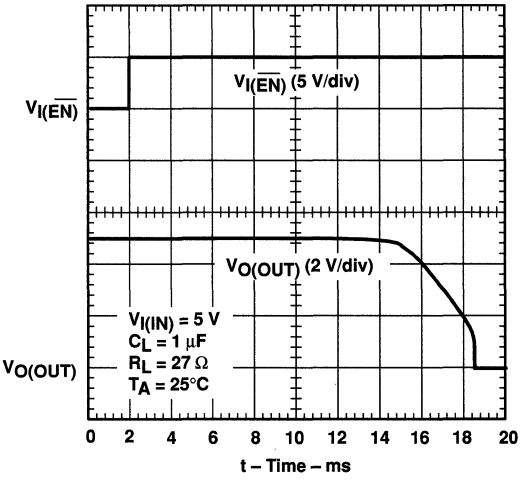

Figure 5. Turn-off Delay and Fall Time with 1-μF Load

PARAMETER MEASUREMENT INFORMATION

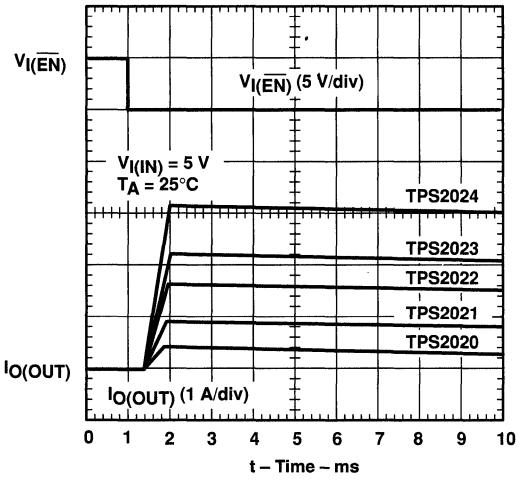

Figure 6. Device Enabled into Short

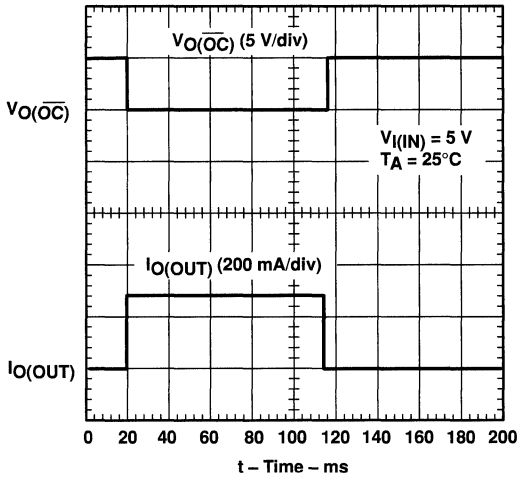

Figure 7. TPS2020, Short Applied to an Enabled Device

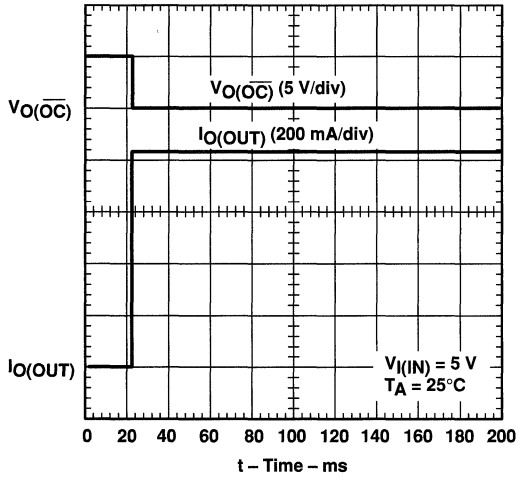

Figure 8. TPS2021, Short Applied to an Enabled Device

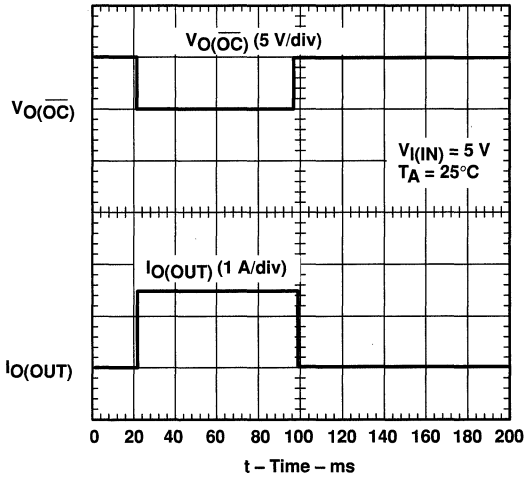

Figure 9. TPS2022, Short Applied to an Enabled Device

PARAMETER MEASUREMENT INFORMATION

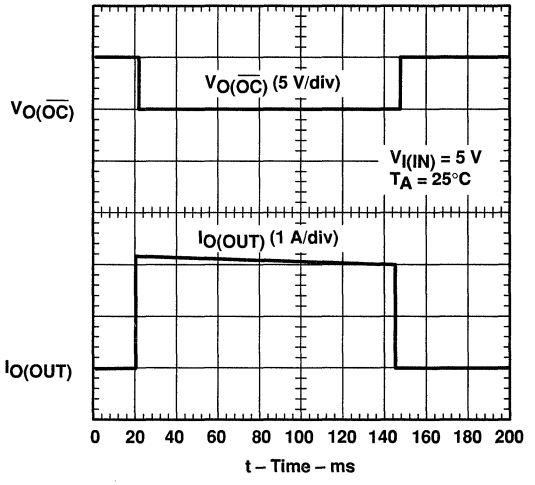

Figure 10. TPS2023, Short Applied to an Enabled Device

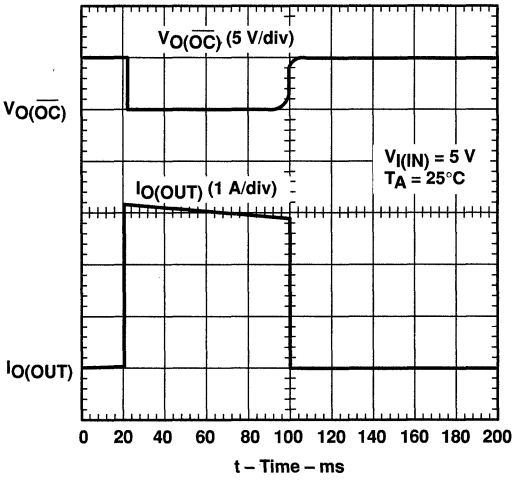

Figure 11. TPS2024, Short Applied to an Enabled Device

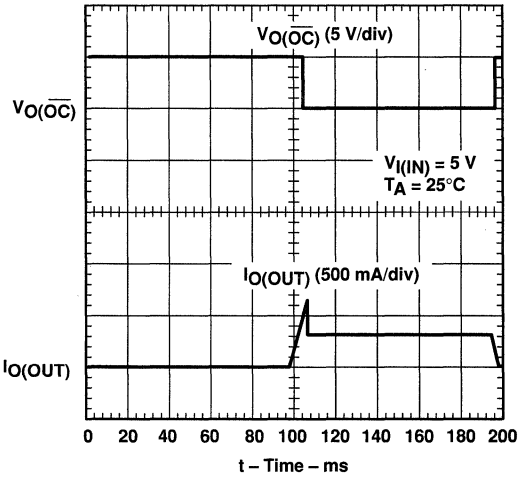

Figure 12. TPS2020, Ramped Load on Enabled Device

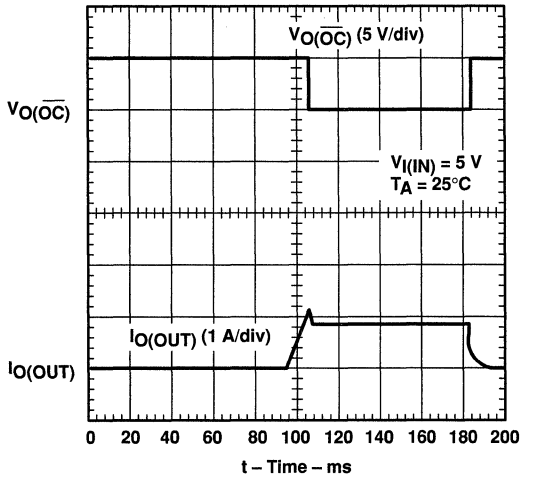

Figure 13. TPS2021, Ramped Load on Enabled Device

PARAMETER MEASUREMENT INFORMATION

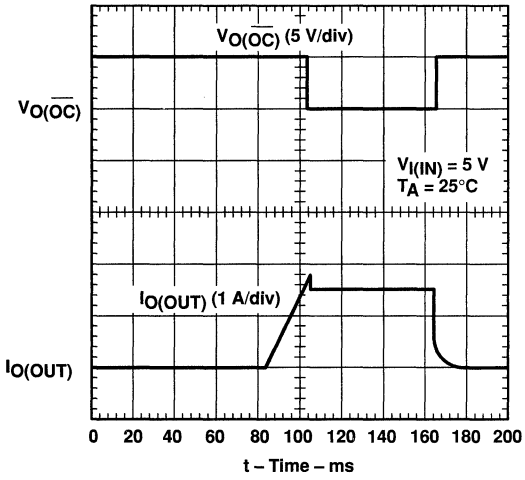

Figure 14. TPS2022, Ramped Load on Enabled Device

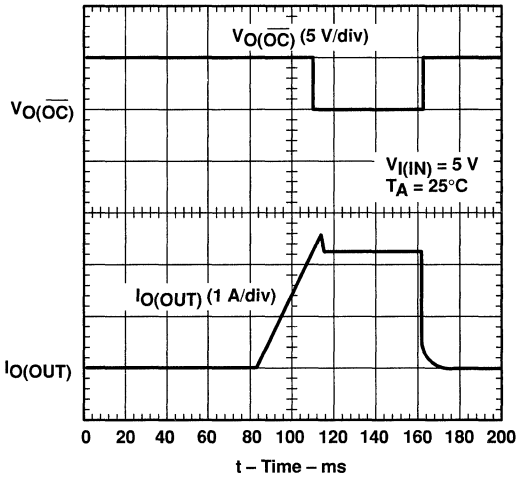

Figure 15. TPS2023, Ramped Load on Enabled Device

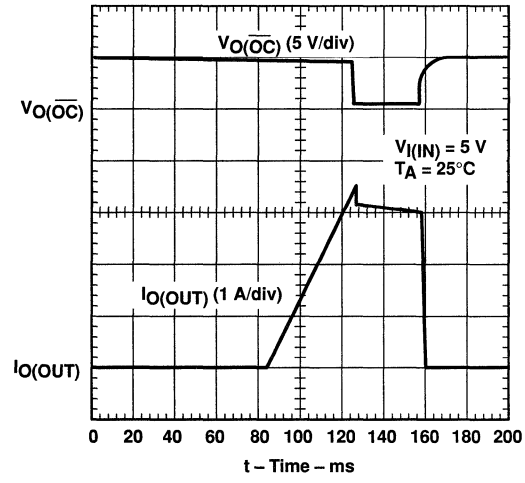

Figure 16. TPS2024, Ramped Load on Enabled Device

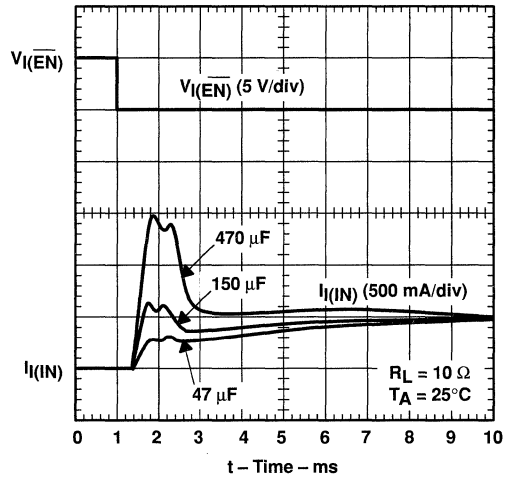

Figure 17. TPS2024, Inrush Current

PARAMETER MEASUREMENT INFORMATION

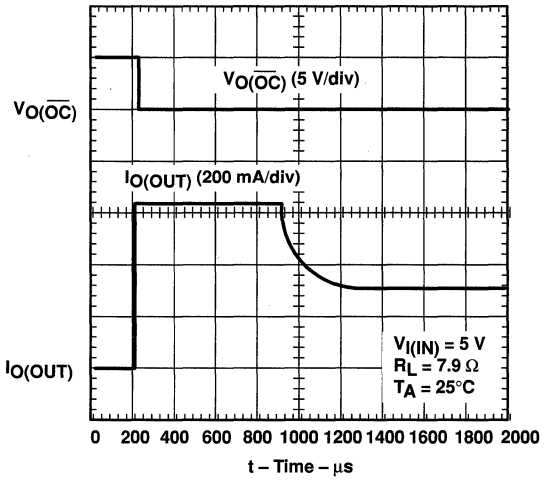

Figure 18. 7.9-Ω Load Connected to an Enabled TPS2020 Device

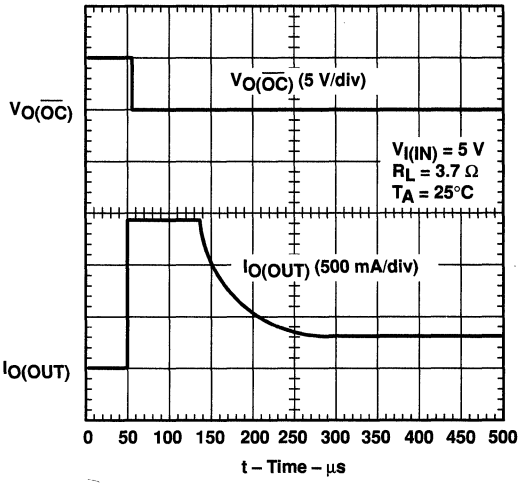

Figure 19. 3.7-Ω Load Connected to an Enabled TPS2020 Device

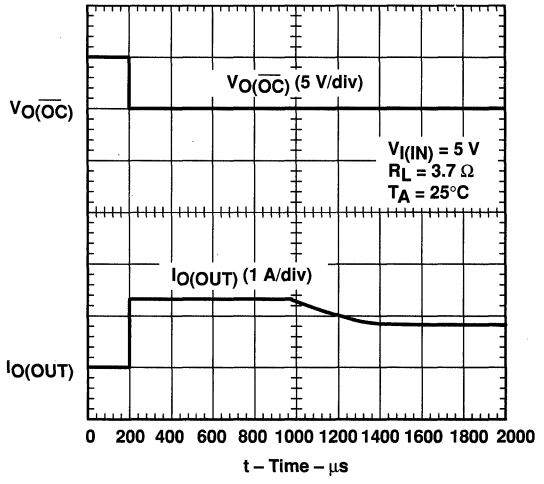

Figure 20. 3.7-Ω Load Connected to an Enabled TPS2021 Device

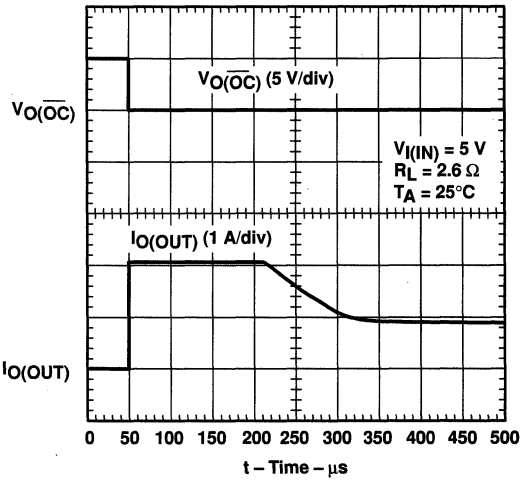

Figure 21. 2.6-Ω Load Connected to an Enabled TPS2021 Device

PARAMETER MEASUREMENT INFORMATION

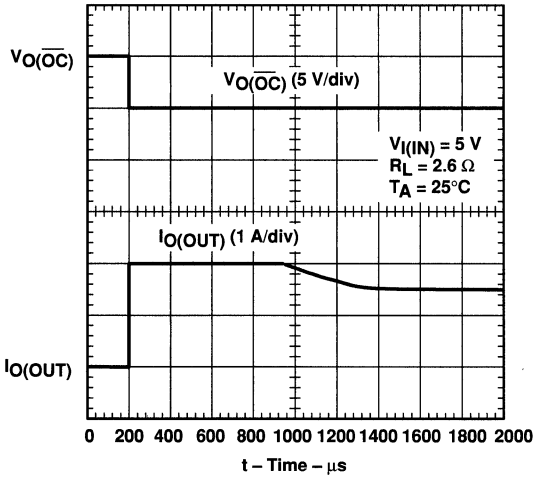

Figure 22. 2.6-Ω Load Connected to an Enabled TPS2022 Device

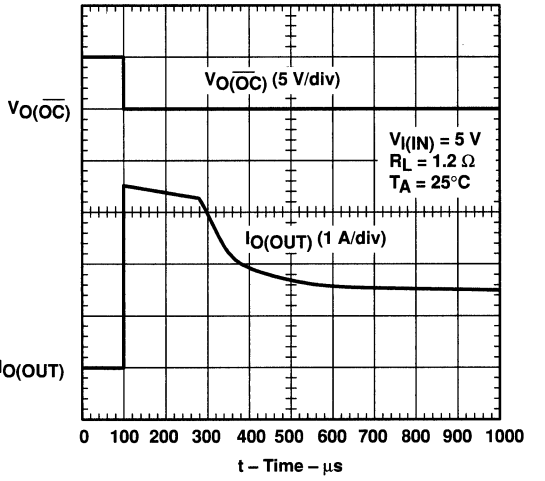

Figure 23. 1.2-Ω Load Connected to an Enabled TPS2022 Device

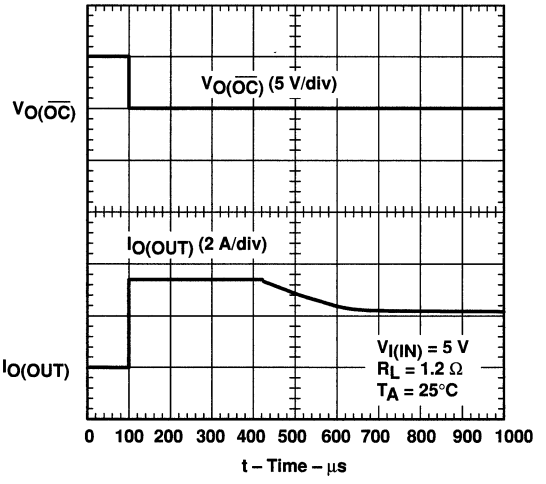

Figure 24. 1.2-Ω Load Connected to an Enabled TPS2023 Device

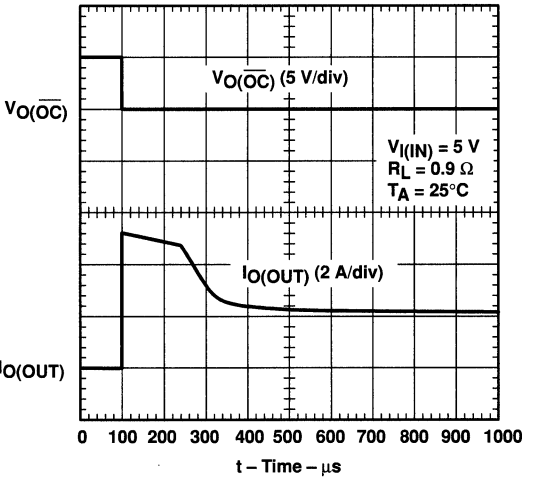

Figure 25. 0.9-Ω Load Connected to an Enabled TPS2023 Device

PARAMETER MEASUREMENT INFORMATION

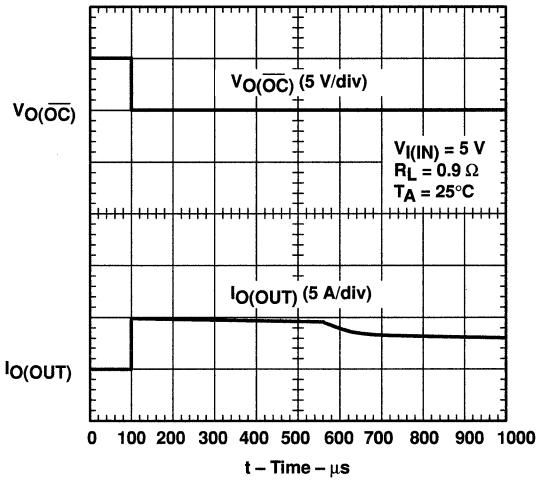

Figure 26. 0.9-Ω Load Connected to an Enabled TPS2024 Device

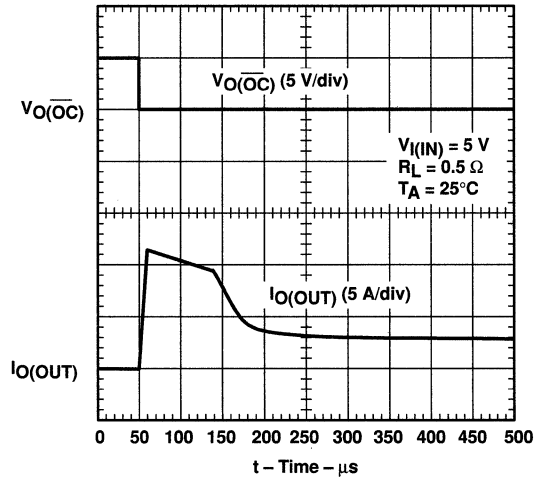

Figure 27. 0.5-Ω Load Connected to an Enabled TPS2024 Device

TYPICAL CHARACTERISTICS

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TURN-ON DELAY TIME vs OUTPUT VOLTAGE

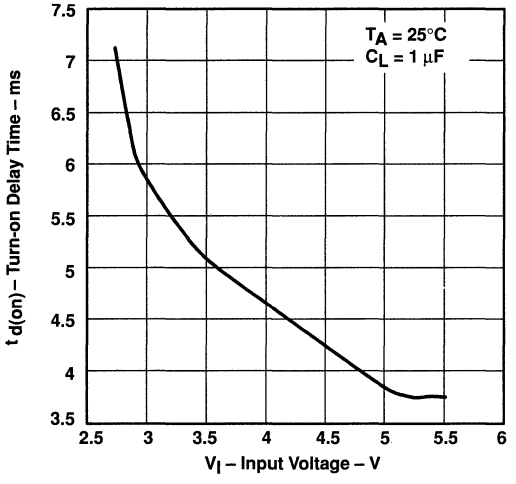

Figure 28

TURN-OFF DELAY TIME vs INPUT VOLTAGE

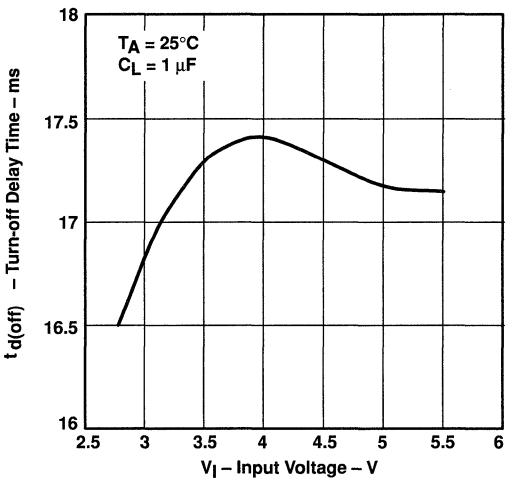

Figure 29

TYPICAL CHARACTERISTICS

RISE TIME
vs
LOAD CURRENT

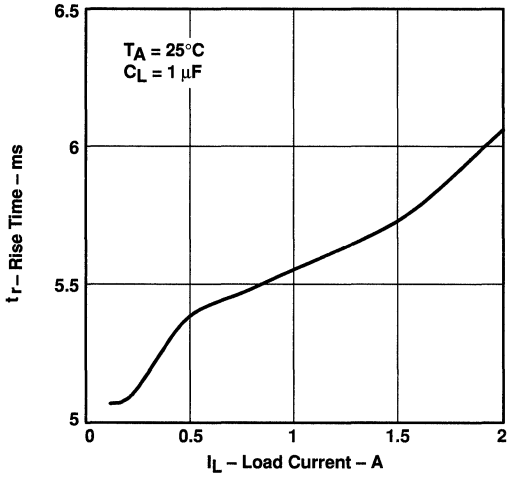

Figure 30

FALL TIME
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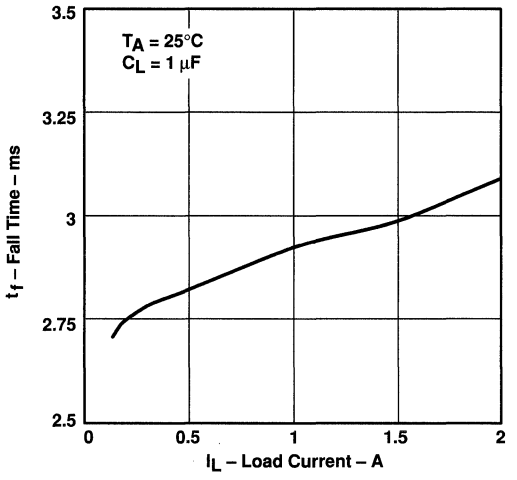

Figure 31

SUPPLY CURRENT (ENABLED)
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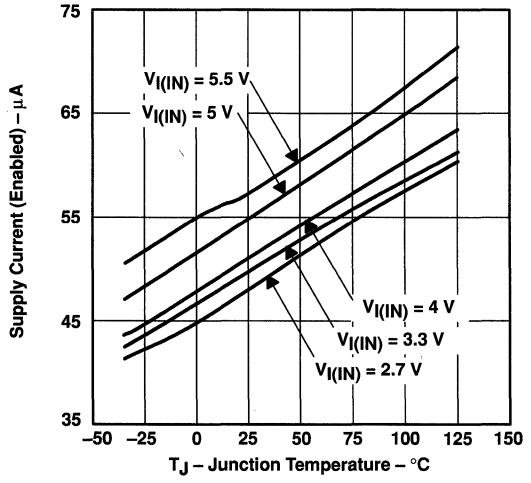

Figure 32

SUPPLY CURRENT (DISABLED)
vs
JUNCTION TEMPERATURE

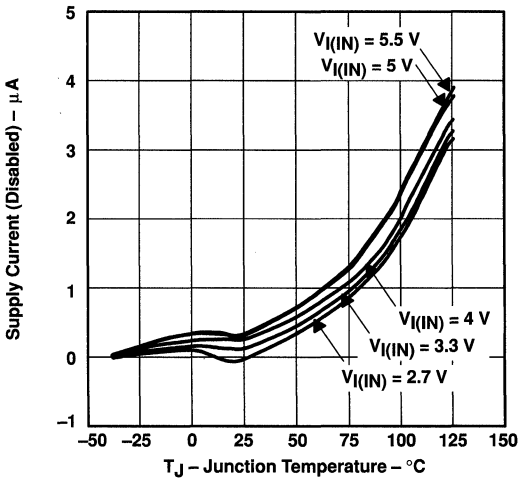

Figure 33

TYPICAL CHARACTERISTICS

SUPPLY CURRENT (ENABLED)
vs
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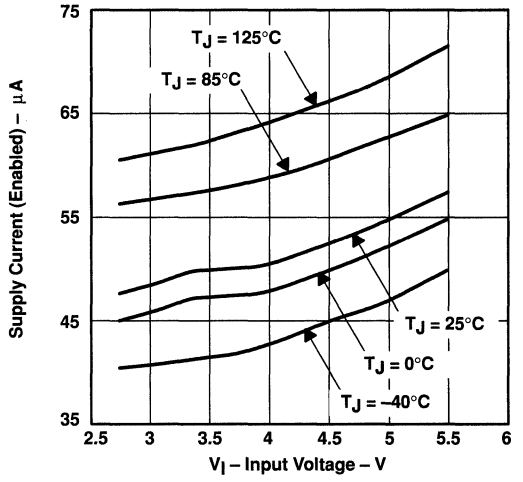

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SUPPLY CURRENT (DISABLED)
vs
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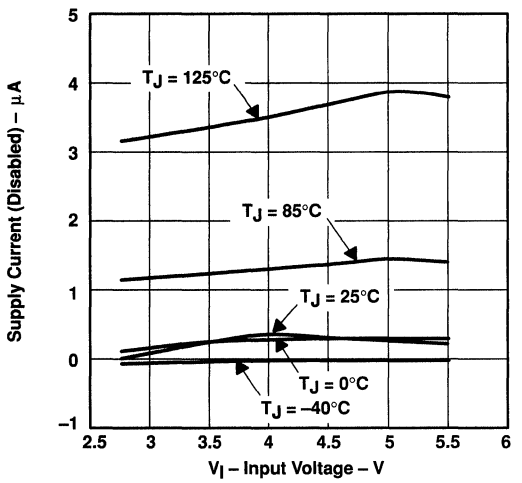

Figure 35

SHORT-CIRCUIT CURRENT LIMIT
vs
INPUT VOLTAGE

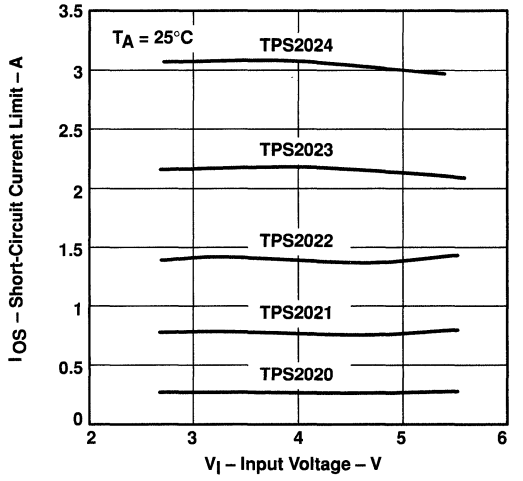

Figure 36

SHORT-CIRCUIT CURRENT LIMIT
vs
JUNCTION TEMPERATURE

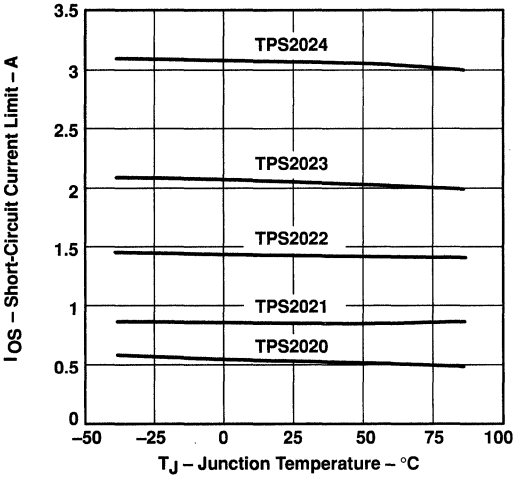

Figure 37

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
INPUT VOLTAGE

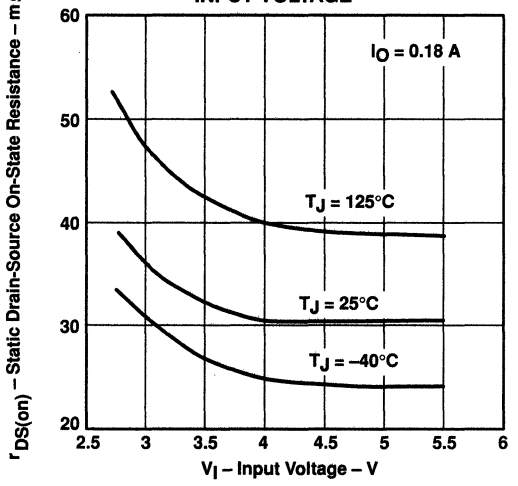

Figure 38

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

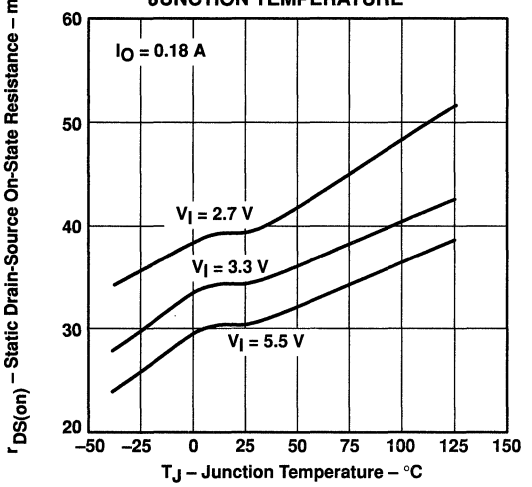

Figure 39

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
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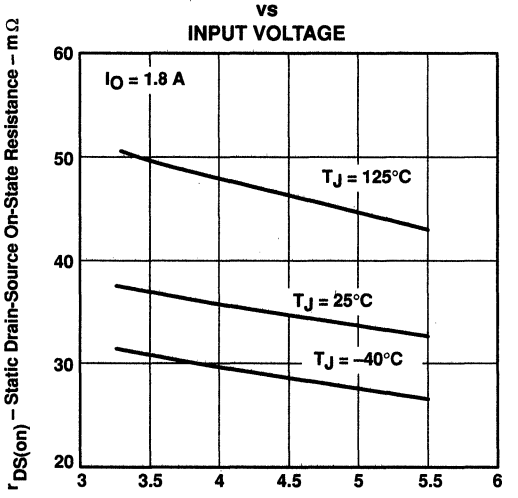

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STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
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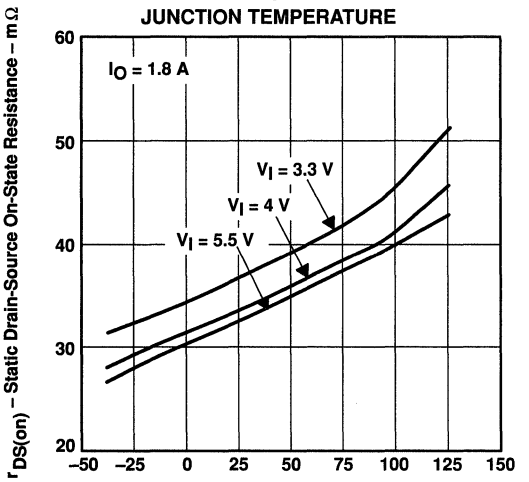

Figure 41

TYPICAL CHARACTERISTICS

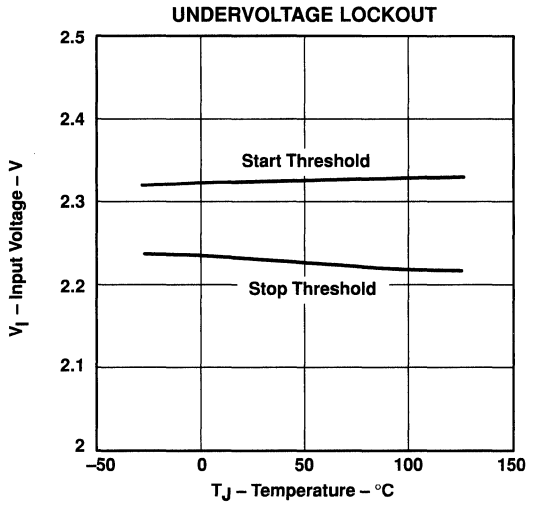

Figure 42

APPLICATION INFORMATION

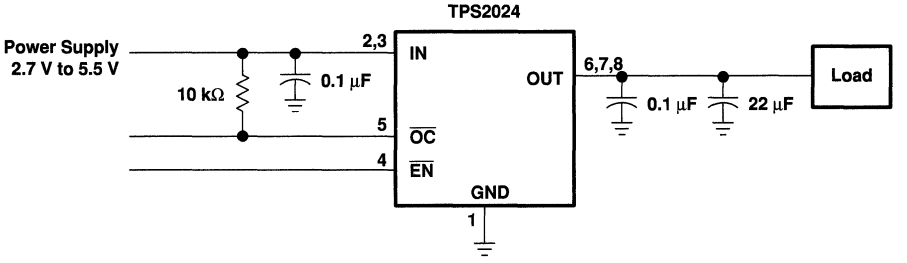

Figure 43. Typical Application

power supply considerations

A 0.01-µF to 0.1-µF ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output and input pins is recommended when the output load is heavy. This reduces power supply transients that may cause ringing on the input. Also, bypassing the output with a 0.01-µF to 0.1-µF ceramic capacitor improves the immunity of the device to short-circuit transients.

overcurrent

A sense FET checks for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

APPLICATION INFORMATION

overcurrent (continued)

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 6). The TPS202x senses the short and immediately switches into a constant-current output.

In the second condition, the excessive load occurs while the device is enabled. At the instant the excessive load occurs, very high currents may flow for a short time before the current-limit circuit can react (see Figures 18–27). After the current-limit circuit has tripped (reached the overcurrent trip threshhold) the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figures 12–16). The TPS202x is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

$\overline{OC}$ response

The $\overline{OC}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false overcurrent reporting from the inrush current flowing through the device, charging the downstream capacitor. An RC filter can be connected to the $\overline{OC}$ pin to reduce false overcurrent reporting. Using low-ESR electrolytic capacitors on the output lowers the inrush current flow through the device during hot-plug events by providing a low impedance energy source, thereby reducing erroneous overcurrent reporting.

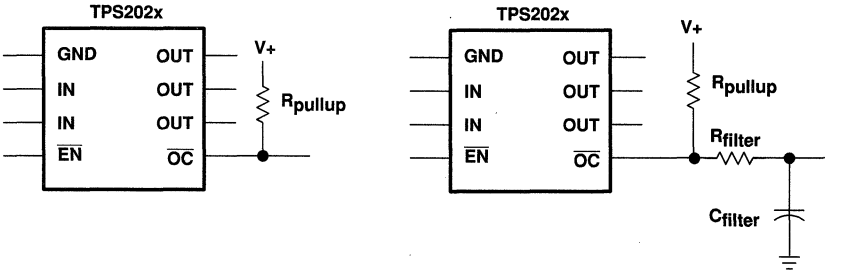

Figure 44. Typical Circuit for $\overline{OC}$ Pin and RC Filter for Damping Inrush $\overline{OC}$ Responses

APPLICATION INFORMATION

power dissipation and junction temperature

The low on-resistance on the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find $r_{DS(on)}$ at the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figures 38–41. Next, calculate the power dissipation using:

$$P_D = r_{DS(on)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient Temperature °C
$R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W, PDIP = 106°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get an acceptable answer.

thermal protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS202x into constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels. The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

undervoltage lock-out (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch will be quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO will also keep the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. Upon reinsertion, the power switch will be turned on, with a controlled rise time to reduce EMI and voltage overshoots.

APPLICATION INFORMATION

generic hot-plug applications (see Figure 45)

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Because of the controlled rise times and fall times of the TPS202x series, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS202x also ensures the switch will be off after the card has been removed, and the switch will be off during the next insertion. The UVLO feature guarantees a soft start with a controlled rise time for every insertion of the card or module.

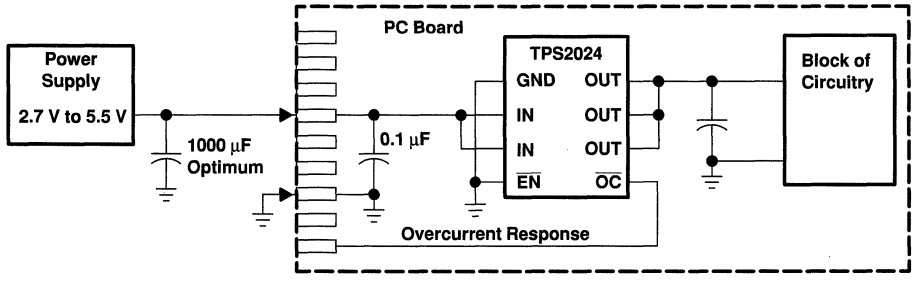

Figure 45. Typical Hot-Plug Implementation

By placing the TPS202x between the V_{CC} input and the rest of the circuitry, the input power will reach this device first after insertion. The typical rise time of the switch is approximately 9 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

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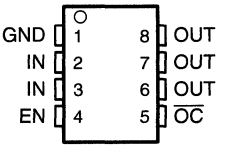
- **50-mΩ -Maximum (5-V Input) High-Side MOSFET Switch**
- **Short-Circuit and Thermal Protection**
- **Overcurrent Logic Output**
- **Operating Range . . . 2.7 V to 5.5 V**
- **Logic-Level Enable Input**
- **Typical Rise Time . . . 6.1 ms**
- **Undervoltage Lockout**
- **Maximum Standby Supply Current . . . 10 μA**
- **No Drain-Source Back-Gate Diode**
- **Available in 8-pin SOIC and PDIP Packages**
- **Ambient Temperature Range, –40°C to 85°C**
- **2-kV Human-Body-Model, 200-V Machine-Model ESD Protection**

D OR P PACKAGE
(TOP VIEW)



description

The TPS203x family of power distribution switches is intended for applications where heavy capacitive loads and short circuits are likely to be encountered. These devices are 50-mΩ N-channel MOSFET high-side power switches. The switch is controlled by a logic enable compatible with 5-V logic and 3-V logic. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the TPS203x limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{OC}$) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until valid input voltage is present.

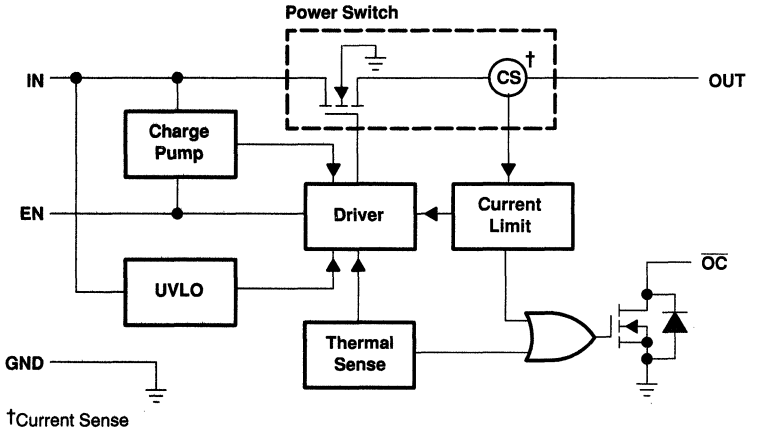
The TPS203x devices differ only in short-circuit current threshold. The TPS2030 limits at 0.3-A load, the TPS2031 at 0.9-A load, the TPS2032 at 1.5-A load, the TPS2033 at 2.2-A load, and the TPS2034 at 3-A load (see Available Options). The TPS203x is available in an 8-pin small-outline integrated-circuit (SOIC) package and in an 8-pin dual-in-line (DIP) package and operates over a junction temperature range of –40°C to 125°C.

AVAILABLE OPTIONS

T_A	ENABLE	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A)	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (A)	PACKAGED DEVICES	
				SMALL OUTLINE (D)†	PLASTIC DIP (P)
–40°C to 85°C	Active high	0.2	0.3	TPS2030D	TPS2030P
		0.6	0.9	TPS2031D	TPS2031P
		1	1.5	TPS2032D	TPS2032P
		1.5	2.2	TPS2033D	TPS2033P
		2	3	TPS2034D	TPS2034P

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2030DR)

TPS2030 functional block diagram



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO. D OR P		
EN	4	I	Enable input. Logic high turns on power switch.
GND	1	I	Ground
IN	2, 3	I	Input voltage
$\overline{OC}$	5	O	Overcurrent. Logic output active low
OUT	6, 7, 8	O	Power-switch output

detailed description

power switch

The power switch is an N-channel MOSFET with a maximum on-state resistance of 50 mΩ ($V_{I(IN)}$ = 5 V). Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled.

charge pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 9-ms range.

enable (EN)

The logic enable disables the power switch, the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10 μA when a logic low is present on EN . A logic high input on EN restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

overcurrent ($\overline{OC}$)

The $\overline{OC}$ open drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed.

current sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant current mode and holds the current constant while varying the voltage on the load.

thermal sense

An internal thermal-sense circuit shuts off the power switch when the junction temperature rises to approximately 140°C. Hysteresis is built into the thermal sense circuit. After the device has cooled approximately 20°C, the switch turns back on. The switch continues to cycle off and on until the fault is removed.

undervoltage lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, $V_{I(IN)}$ (see Note 1) ..... −0.3 V to 6 V
Output voltage range, $V_{O(OUT)}$ (see Note 1) ..... −0.3 V to $V_{I(IN)}$ + 0.3 V
Input voltage range, $V_{I(EN)}$ ..... −0.3 V to 6 V
Continuous output current, $I_{O(OUT)}$ ..... internally limited
Continuous total power dissipation ..... See Dissipation Rating Table
Operating virtual junction temperature range, T_J ..... −40°C to 125°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1175 mW	9.4 mW/°C	752 mW	611 mW

recommended operating conditions

		MIN	MAX	UNIT
Input voltage	$V_{I(IN)}$	2.7	5.5	V
	$V_{I(EN)}$	0	5.5	V
Continuous output current, I_O	TPS2030	0	0.2	A
	TPS2031	0	0.6	
	TPS2032	0	1	
	TPS2033	0	1.5	
	TPS2034	0	2	
Operating virtual junction temperature, T_J		−40	125	°C

electro static discharge (ESD) protection

	MIN	MAX	UNIT
Human Body Model MIL-STD-883C		2	kV
Machine model		0.2	kV

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, EN = 5 V (unless otherwise noted)

power switch

PARAMETER		TEST CONDITIONS†			MIN	TYP	MAX	UNIT
$r_{DS(on)}$	Static drain-source on-state resistance	$V_{I(IN)}$ = 5 V,	T_J = 25°C,	I_O = 1.8 A		33	36	mΩ
		$V_{I(IN)}$ = 5 V,	T_J = 85°C,	I_O = 1.8 A		38	46	
		$V_{I(IN)}$ = 5 V,	T_J = 125°C,	I_O = 1.8 A		44	50	
		$V_{I(IN)}$ = 3.3 V,	T_J = 25°C,	I_O = 1.8 A		37	41	
		$V_{I(IN)}$ = 3.3 V,	T_J = 85°C,	I_O = 1.8 A		43	52	
		$V_{I(IN)}$ = 3.3 V,	T_J = 125°C,	I_O = 1.8 A		51	61	
		$V_{I(IN)}$ = 5 V,	T_J = 25°C,	I_O = 0.18 A		30	34	
		$V_{I(IN)}$ = 5 V,	T_J = 85°C,	I_O = 0.18 A		35	41	
		$V_{I(IN)}$ = 5 V,	T_J = 125°C,	I_O = 0.18 A		39	47	
		$V_{I(IN)}$ = 3.3 V,	T_J = 25°C,	I_O = 0.18 A		33	37	
		$V_{I(IN)}$ = 3.3 V,	T_J = 85°C,	I_O = 0.18 A		39	46	
		$V_{I(IN)}$ = 3.3 V,	T_J = 125°C,	I_O = 0.18 A		44	56	
t_r	Rise time, output	$V_{I(IN)}$ = 5.5 V, C_L = 1 µF,	T_J = 25°C, R_L = 10 Ω			6.1		ms
		$V_{I(IN)}$ = 2.7 V, C_L = 1 µF,	T_J = 25°C, R_L = 10 Ω			8.6		
t_f	Fall time, output	$V_{I(IN)}$ = 5.5 V, C_L = 1 µF,	T_J = 25°C, R_L = 10 Ω			3.4		ms
		$V_{I(IN)}$ = 2.7 V, C_L = 1 µF,	T_J = 25°C, R_L = 10 Ω			3		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

enable input (EN)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V	2			V
V_{IL}	Low-level input voltage	4.5 V ≤ $V_{I(IN)}$ ≤ 5.5 V			0.8	V
		2.7 V ≤ $V_{I(IN)}$ ≤ 4.5 V			0.5	
I_I	Input current	EN = 0 V or EN = $V_{I(IN)}$	−0.5		0.5	µA
t_{on}	Turn-on time	C_L = 100 µF, R_L = 10 Ω			20	ms
t_{off}	Turn-off time	C_L = 100 µF, R_L = 10 Ω			40	

current limit

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
I_{OS}	Short-circuit output current	T_J = 25°C, V_I = 5.5 V, OUT connected to GND, Device enable into short circuit	TPS2030	0.22	0.3	0.4	A
			TPS2031	0.66	0.9	1.1	
			TPS2032	1.1	1.5	1.8	
			TPS2033	1.65	2.2	2.7	
			TPS2034	2.2	3	3.8	

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, EN = 5 V (unless otherwise noted) (continued)

supply current

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Supply current, low-level output	No Load on OUT	EN = 0	T_J = 25°C		0.3	1	µA
			−40°C ≤ T_J ≤ 125°C			10	
Supply current, high-level output	No Load on OUT	EN = $V_{I(IN)}$	T_J = 25°C		58	75	µA
			−40°C ≤ T_J ≤ 125°C		75	100	
Leakage current	OUT connected to ground	EN = 0	−40°C ≤ T_J ≤ 125°C		10		µA

undervoltage lockout

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low-level input voltage		2		2.5	V
Hysteresis	T_J = 25°C		100		mV

overcurrent ($\overline{OC}$)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output low voltage	I_O = 10 mA, $V_{OL(\overline{OC})}$			0.4	V
Off-state current†	V_O = 5 V, V_O = 3.3 V			1	µA

† Specified by design, not production tested.

PARAMETER MEASUREMENT INFORMATION

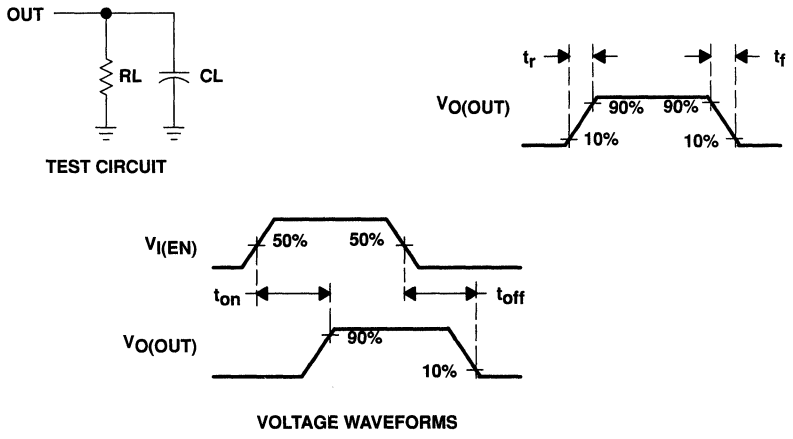


Figure 1. Test Circuit and Voltage Waveforms

Table of Timing Diagrams

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1.2-Ω Load Connected to an Enabled TPS2033 Device	24
0.9-Ω Load Connected to an Enabled TPS2033 Device	25
0.9-Ω Load Connected to an Enabled TPS2034 Device	26
0.5-Ω Load Connected to an Enabled TPS2034 Device	27

PARAMETER MEASUREMENT INFORMATION

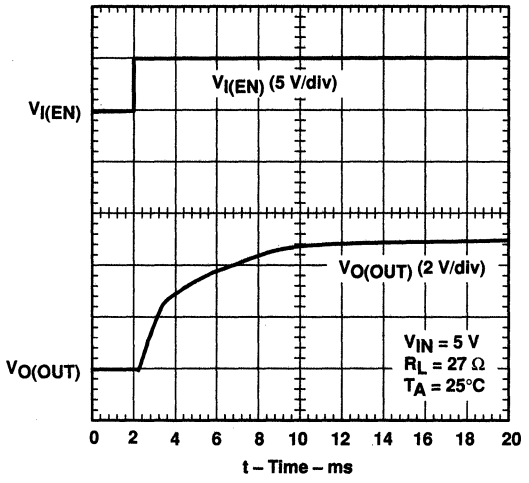

Figure 2. Turn-on Delay and Rise Time

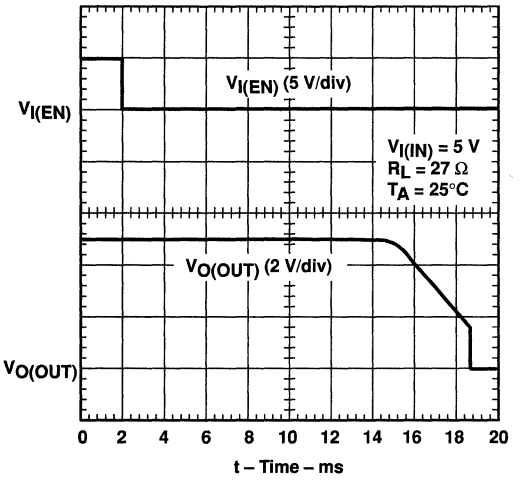

Figure 3. Turn-off Delay and Fall Time

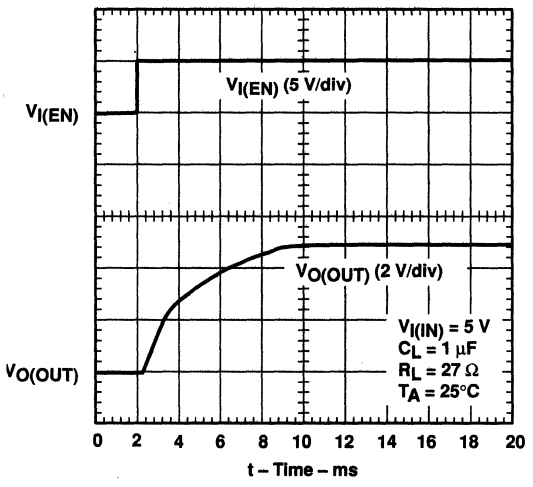

Figure 4. Turn-on Delay and Rise Time With 1-μF Load

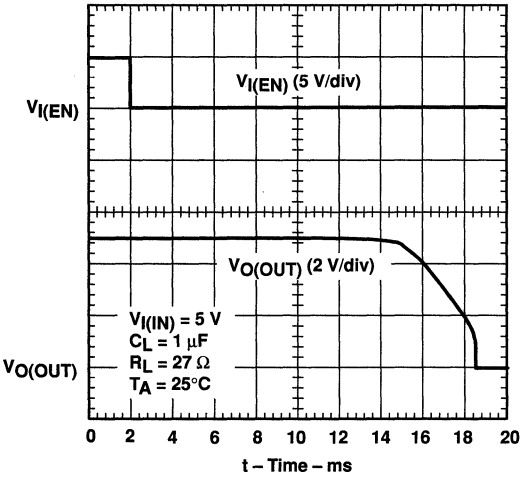

Figure 5. Turn-off Delay and Fall Time with 1-μF Load

PARAMETER MEASUREMENT INFORMATION

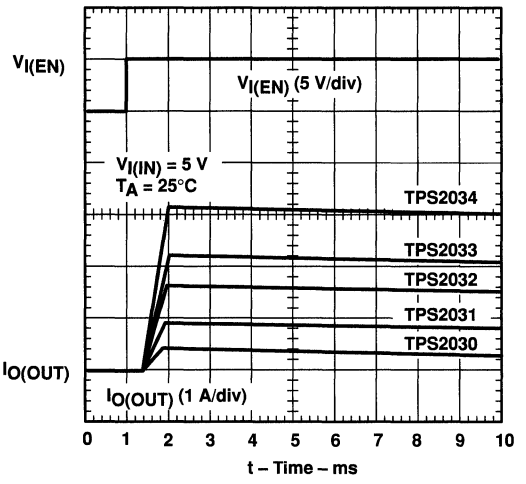

Figure 6. Device Enabled into Short

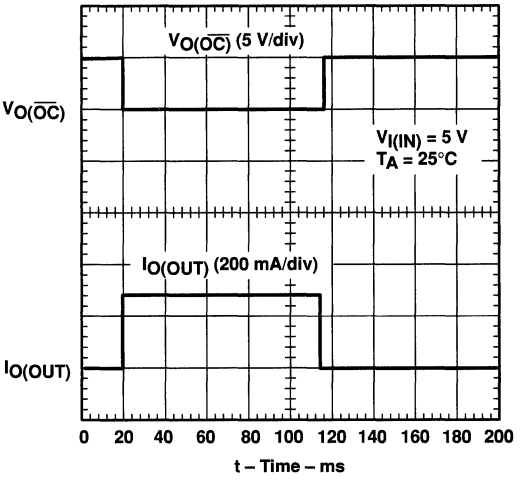

Figure 7. TPS2030, Short Applied to an Enabled Device

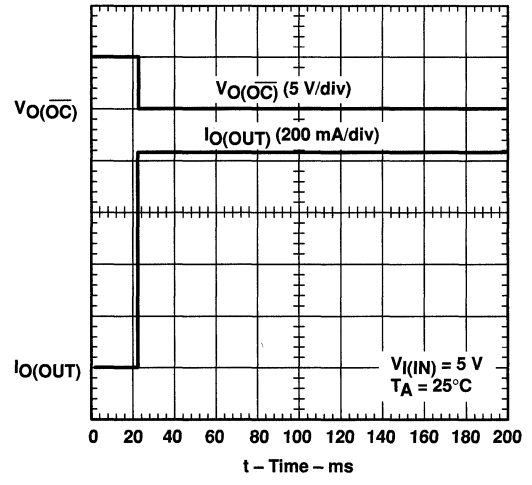

Figure 8. TPS2031, Short Applied to an Enabled Device

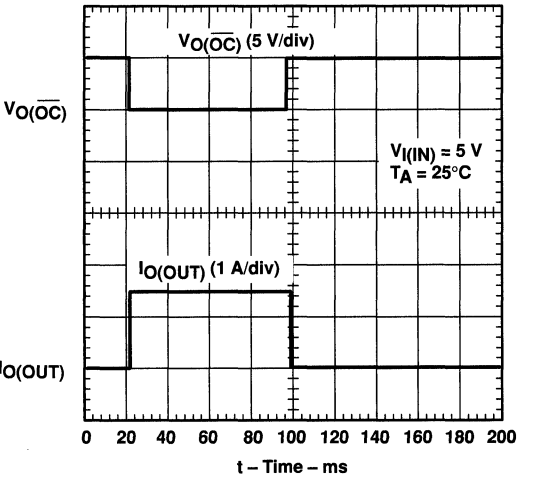

Figure 9. TPS2032, Short Applied to an Enabled Device

PARAMETER MEASUREMENT INFORMATION

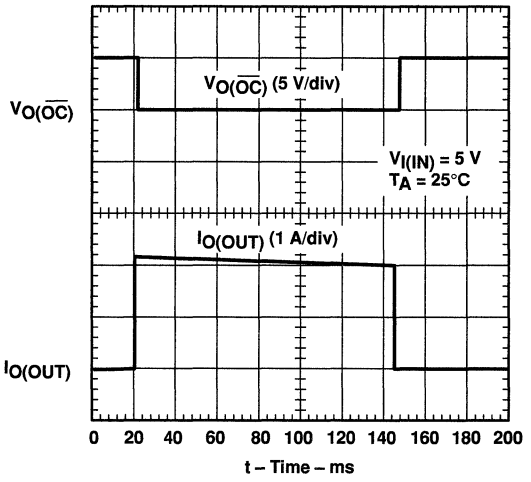

Figure 10. TPS2033, Short Applied to an Enabled Device

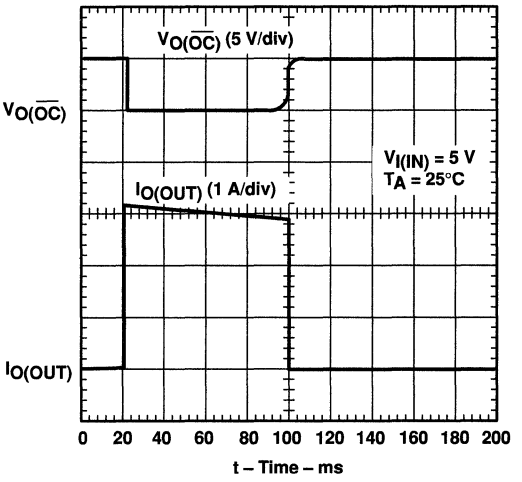

Figure 11. TPS2034, Short Applied to an Enabled Device

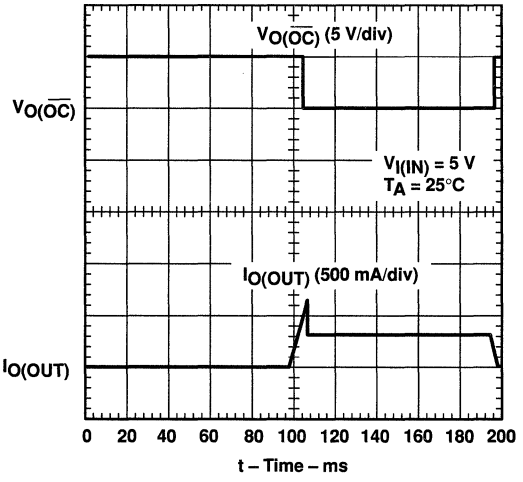

Figure 12. TPS2030, Ramped Load on Enabled Device

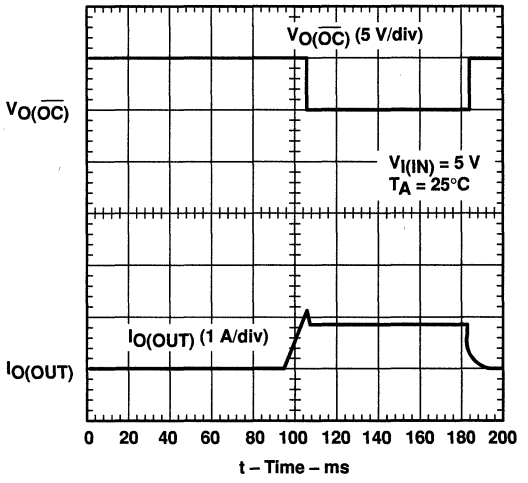

Figure 13. TPS2031, Ramped Load on Enabled Device

PARAMETER MEASUREMENT INFORMATION

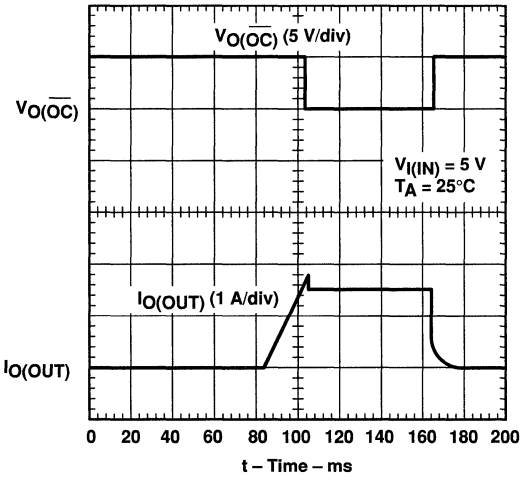

Figure 14. TPS2032, Ramped Load on Enabled Device

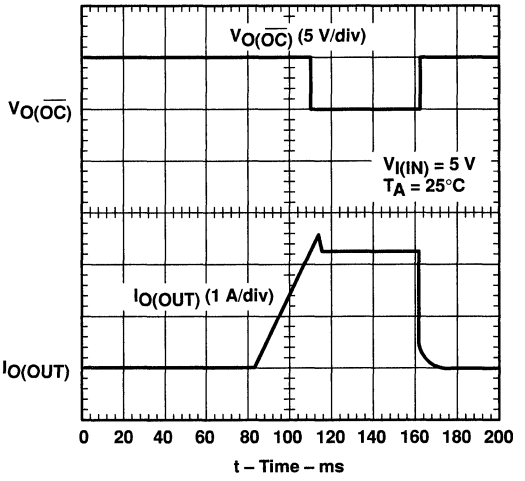

Figure 15. TPS2033, Ramped Load on Enabled Device

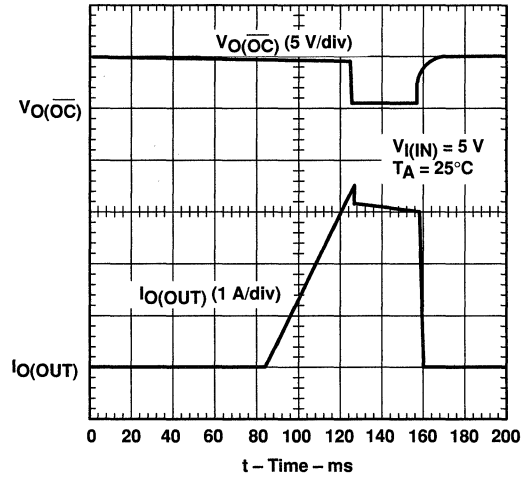

Figure 16. TPS2034, Ramped Load on Enabled Device

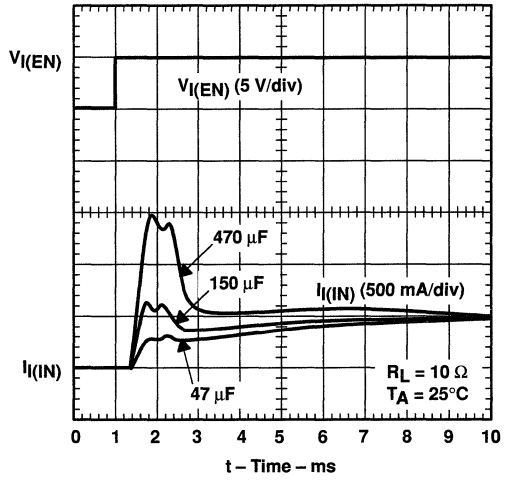

Figure 17. TPS2034, Inrush Current

PARAMETER MEASUREMENT INFORMATION

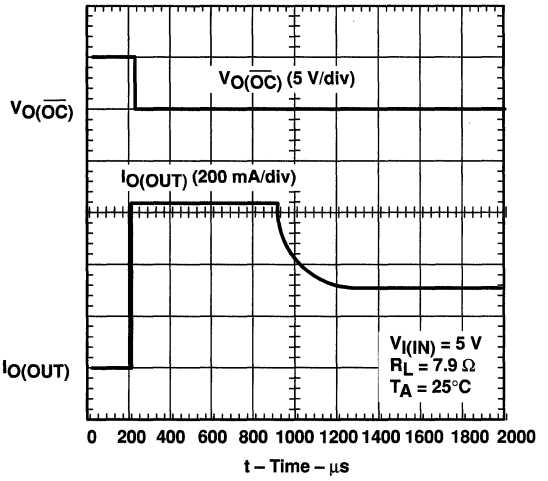

Figure 18. 7.9-Ω Load Connected to an Enabled TPS2030 Device

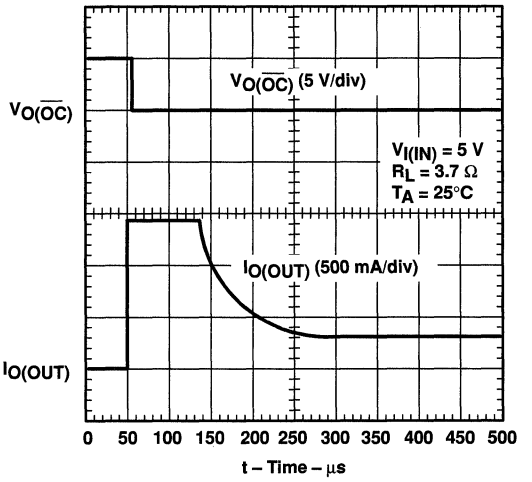

Figure 19. 3.7-Ω Load Connected to an Enabled TPS2030 Device

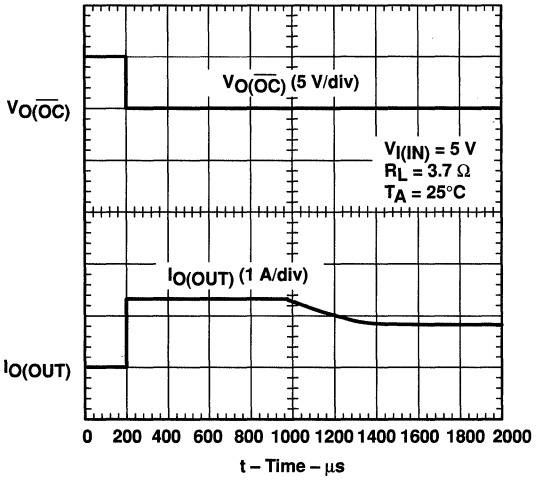

Figure 20. 3.7-Ω Load Connected to an Enabled TPS2031 Device

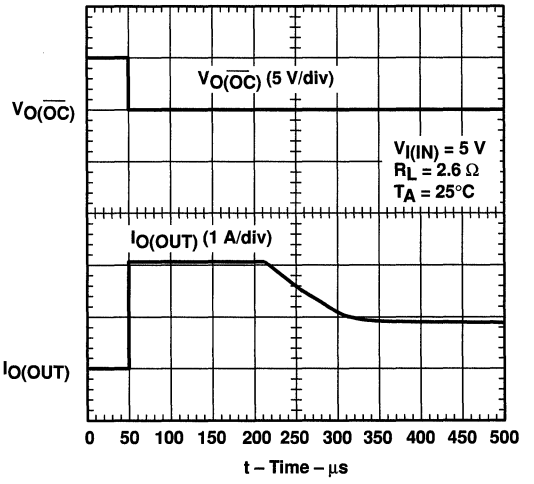

Figure 21. 2.6-Ω Load Connected to an Enabled TPS2031 Device

PARAMETER MEASUREMENT INFORMATION

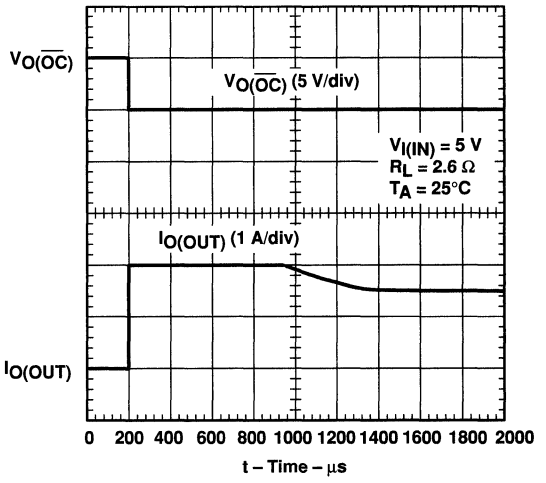

Figure 22. 2.6-Ω Load Connected to an Enabled TPS2032 Device

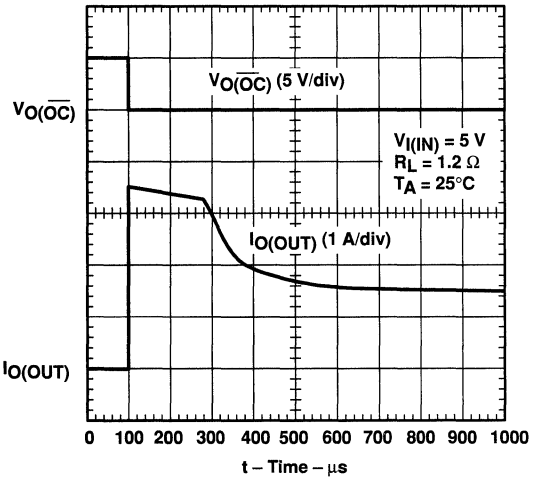

Figure 23. 1.2-Ω Load Connected to an Enabled TPS2032 Device

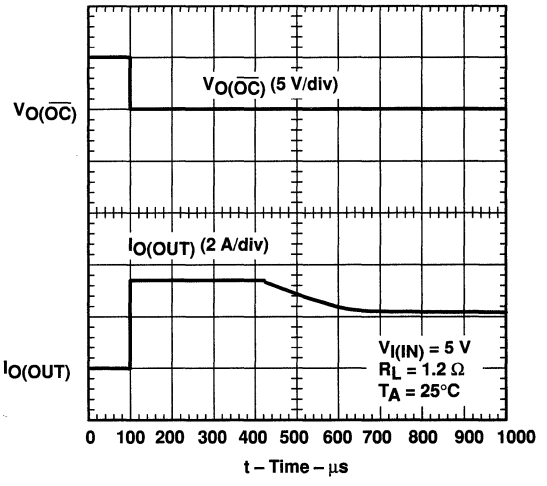

Figure 24. 1.2-Ω Load Connected to an Enabled TPS2033 Device

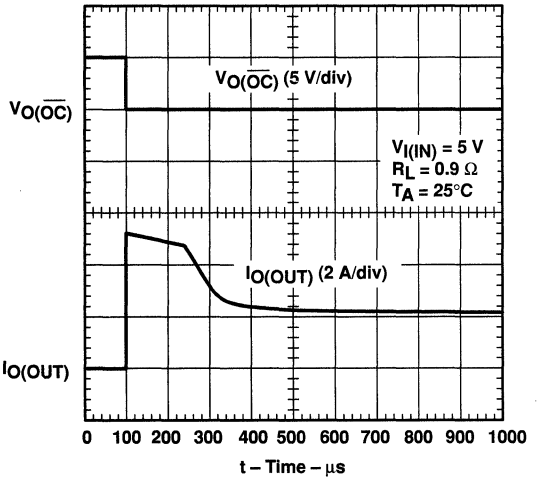

Figure 25. 0.9-Ω Load Connected to an Enabled TPS2033 Device

PARAMETER MEASUREMENT INFORMATION

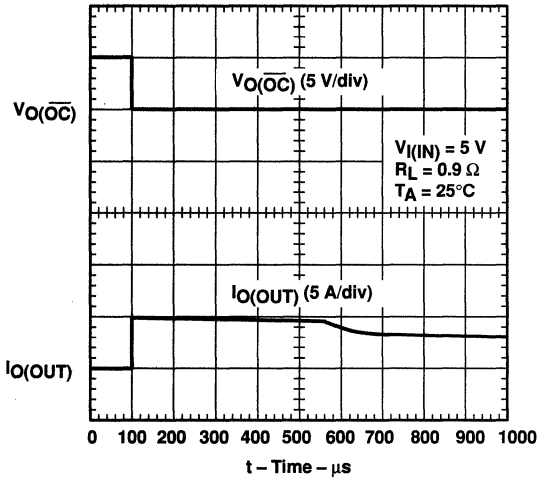

Figure 26. 0.9-Ω Load Connected to an Enabled TPS2034 Device

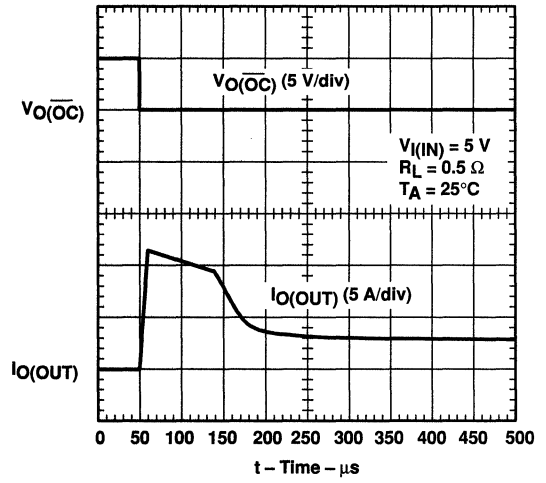

Figure 27. 0.5-Ω Load Connected to an Enabled TPS2034 Device

TYPICAL CHARACTERISTICS

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TURN-ON DELAY TIME vs OUTPUT VOLTAGE

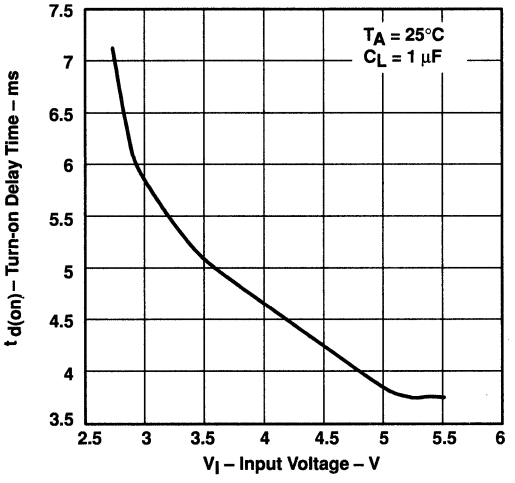


Figure 28

TURN-OFF DELAY TIME vs INPUT VOLTAGE

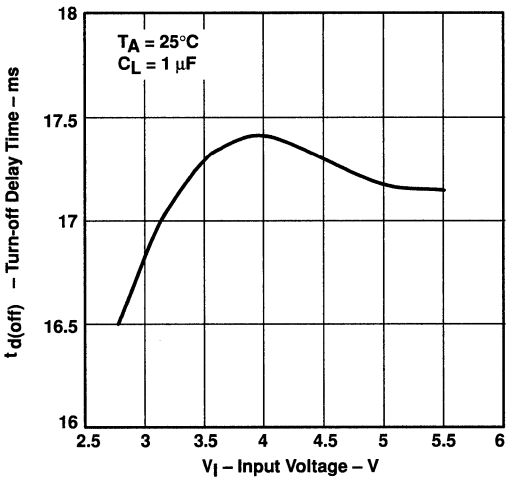


Figure 29

TYPICAL CHARACTERISTICS

RISE TIME
vs
LOAD CURRENT

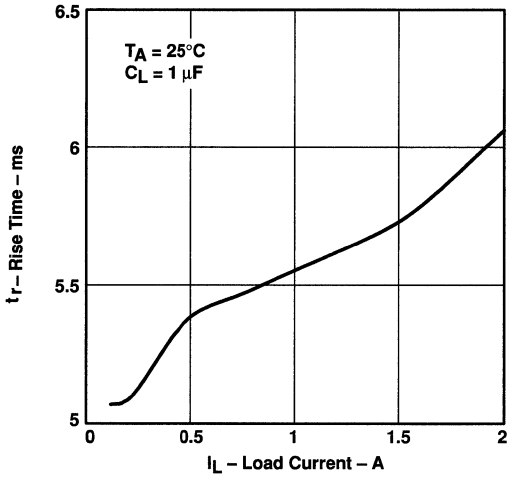


Figure 30

FALL TIME
vs
LOAD CURRENT

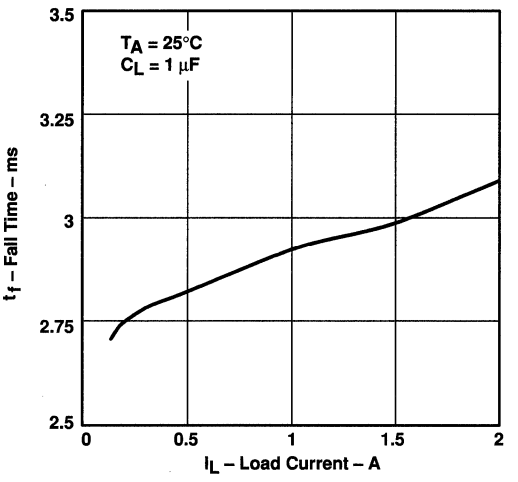


Figure 31

SUPPLY CURRENT (ENABLED)
vs
JUNCTION TEMPERATURE

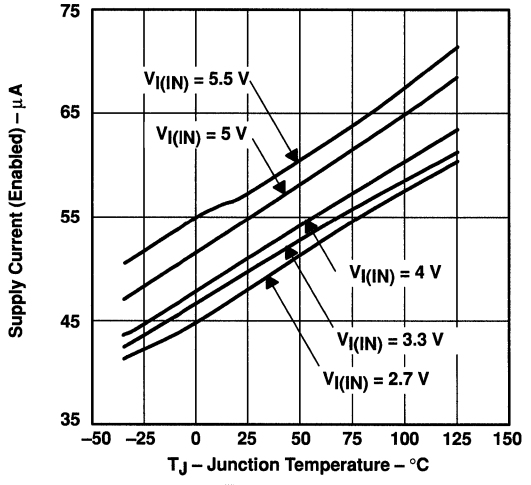


Figure 32

SUPPLY CURRENT (DISABLED)
vs
JUNCTION TEMPERATURE

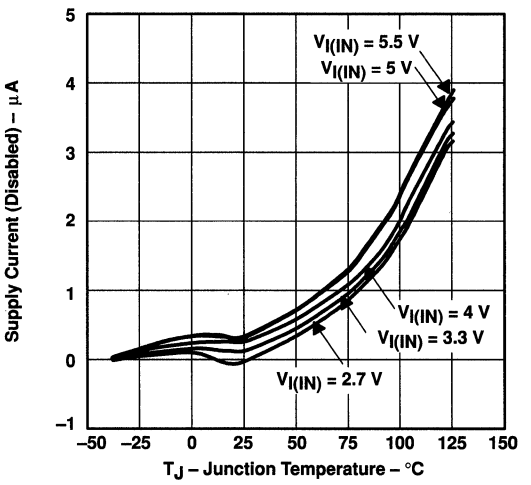


Figure 33

TYPICAL CHARACTERISTICS

SUPPLY CURRENT (ENABLED)
vs
INPUT VOLTAGE

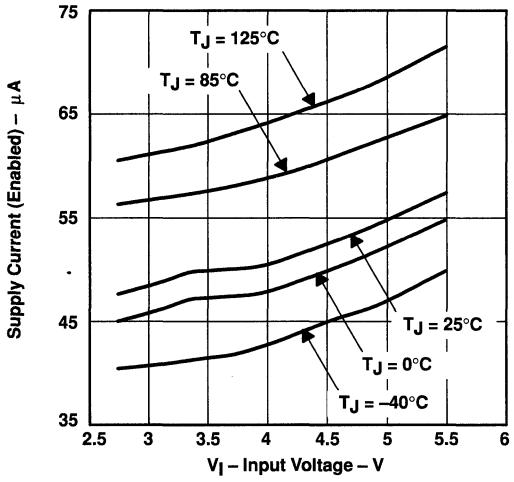


Figure 34

SUPPLY CURRENT (DISABLED)
vs
INPUT VOLTAGE

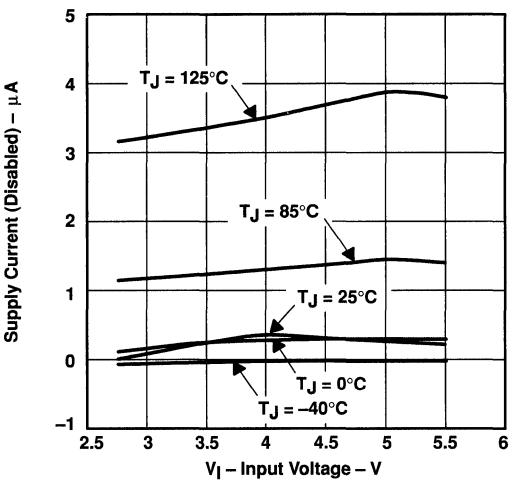


Figure 35

SHORT-CIRCUIT CURRENT LIMIT
vs
INPUT VOLTAGE

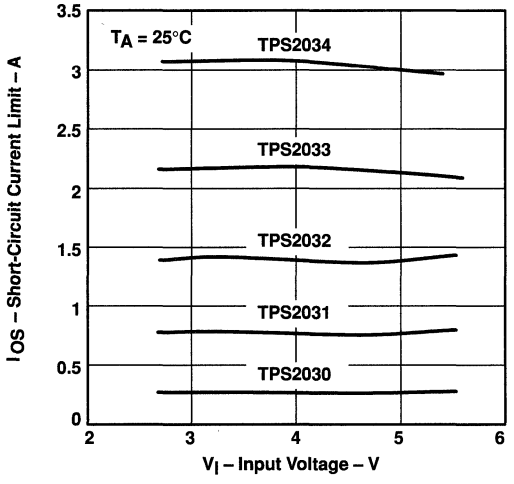


Figure 36

SHORT-CIRCUIT CURRENT LIMIT
vs
JUNCTION TEMPERATURE

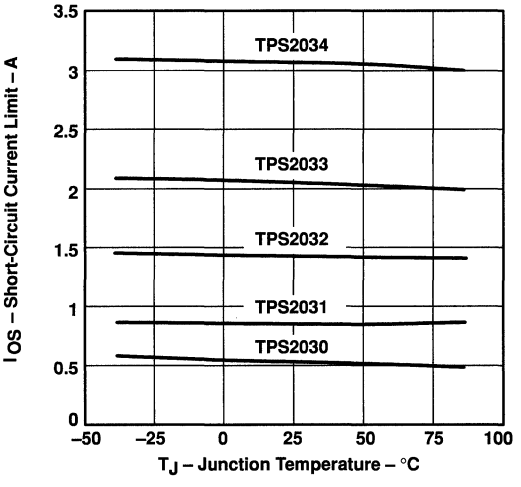


Figure 37

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
INPUT VOLTAGE

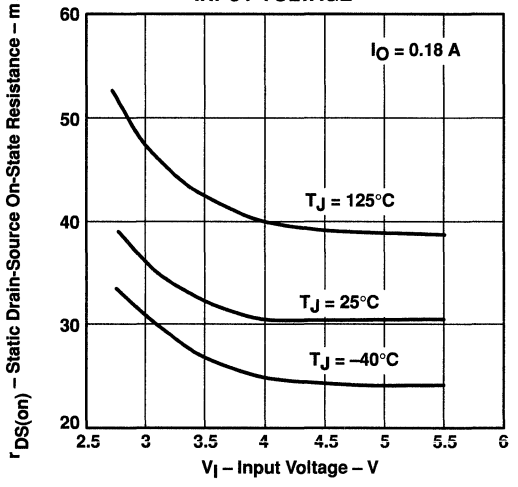


Figure 38

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

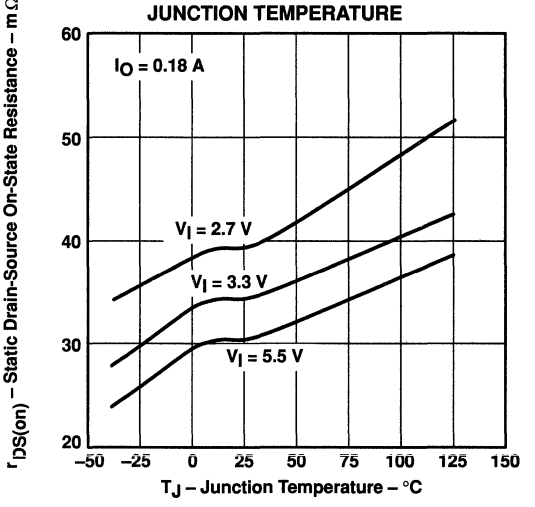


Figure 39

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
INPUT VOLTAGE

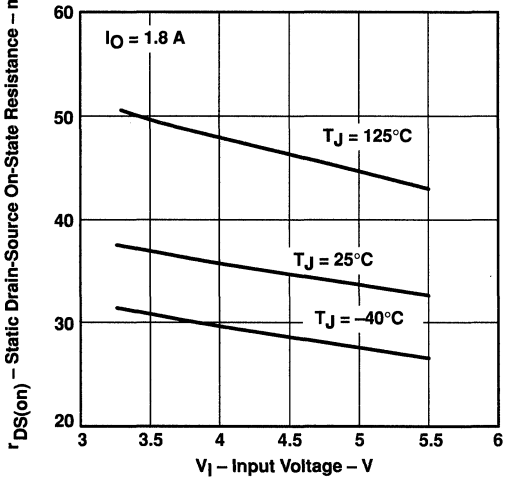


Figure 40

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

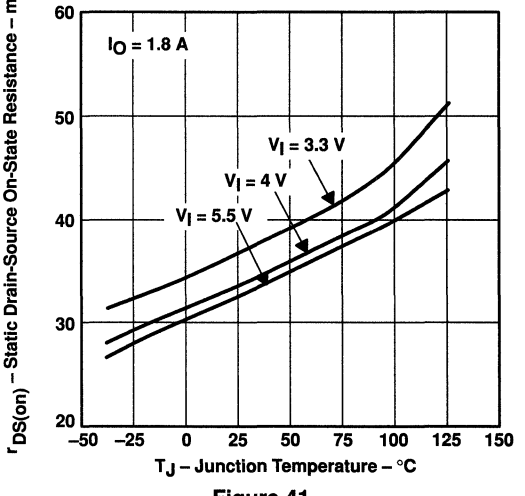


Figure 41

TYPICAL CHARACTERISTICS

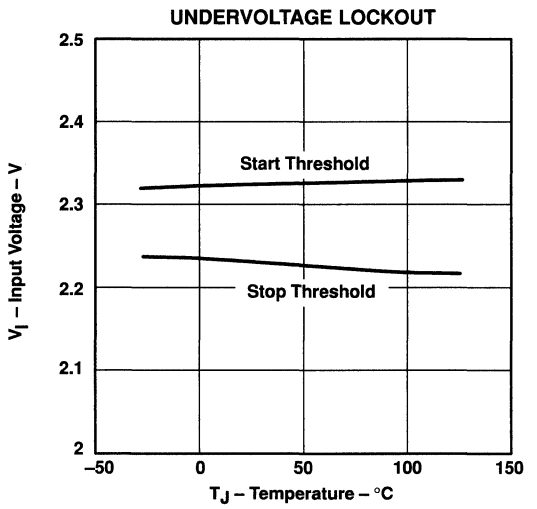


Figure 42

APPLICATION INFORMATION

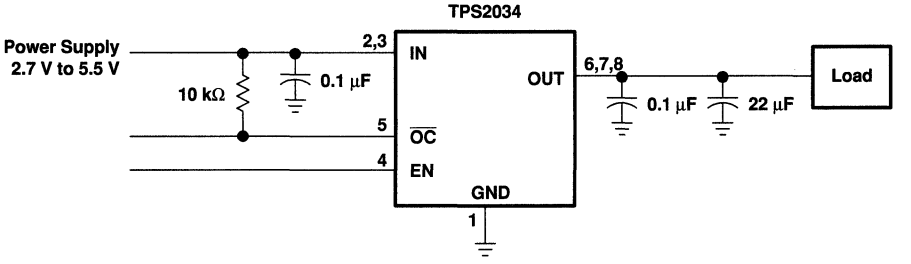


Figure 43. Typical Application

power supply considerations

A 0.01-μF to 0.1-μF ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output and input pins is recommended when the output load is heavy. This reduces power supply transients that may cause ringing on the input. Also, bypassing the output with a 0.01-μF to 0.1-μF ceramic capacitor improves the immunity of the device to short-circuit transients.

overcurrent

A sense FET checks for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

APPLICATION INFORMATION

overcurrent (continued)

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 6). The TPS203x senses the short and immediately switches into a constant-current output.

In the second condition, the excessive load occurs while the device is enabled. At the instant the excessive load occurs, very high currents may flow for a short time before the current-limit circuit can react (see Figures 18–27). After the current-limit circuit has tripped (reached the overcurrent trip threshhold) the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figures 12–16). The TPS203x is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

$\overline{OC}$ response

The $\overline{OC}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false overcurrent reporting from the inrush current flowing through the device, charging the downstream capacitor. An RC filter can be connected to the $\overline{OC}$ pin to reduce false overcurrent reporting. Using low-ESR electrolytic capacitors on the output lowers the inrush current flow through the device during hot-plug events by providing a low impedance energy source, thereby reducing erroneous overcurrent reporting.

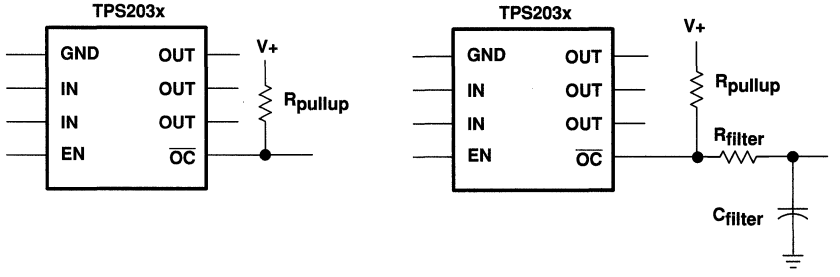


Figure 44. Typical Circuit for $\overline{OC}$ Pin and RC Filter for Damping Inrush $\overline{OC}$ Responses

APPLICATION INFORMATION

power dissipation and junction temperature

The low on-resistance on the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find $r_{DS(on)}$ at the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figures 38–41. Next, calculate the power dissipation using:

$$P_D = r_{DS(on)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient Temperature °C
$R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W, PDIP = 106°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get an acceptable answer.

thermal protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS203x into constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels. The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

undervoltage lock-out (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch will be quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO will also keep the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. Upon reinsertion, the power switch will be turned on, with a controlled rise time to reduce EMI and voltage overshoots.

APPLICATION INFORMATION

generic hot-plug applications (see Figure 45)

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Because of the controlled rise times and fall times of the TPS203x series, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS203x also ensures the switch will be off after the card has been removed, and the switch will be off during the next insertion. The UVLO feature guarantees a soft start with a controlled rise time for every insertion of the card or module.

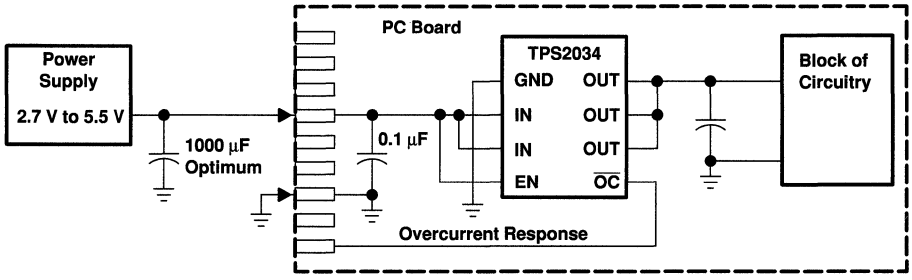


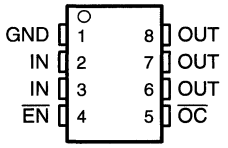
Figure 45. Typical Hot-Plug Implementation

By placing the TPS203x between the V_{CC} input and the rest of the circuitry, the input power will reach this device first after insertion. The typical rise time of the switch is approximately 9 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

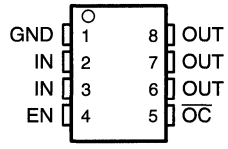
SLVS172A –AUGUST 1998 – REVISED APRIL 1999

- 135-mΩ -Maximum (5-V Input) High-Side MOSFET Switch
- 500 mA Continuous Current
- Short-Circuit and Thermal Protection With Overcurrent Logic Output
- Operating Range . . . 2.7 V to 5.5 V
- Logic-Level Enable Input
- 2.5-ms Typical Rise Time
- Undervoltage Lockout
- 10 μA Maximum Standby Supply Current
- Bidirectional Switch
- Available in 8-pin SOIC and PDIP Packages
- Ambient Temperature Range, –40°C to 85°C
- 2-kV Human-Body-Model, 200-V Machine-Model ESD Protection
- UL Listed – File No. E169910

TPS2041
D OR P PACKAGE
(TOP VIEW)



TPS2051
D OR P PACKAGE
(TOP VIEW)



description

The TPS2041 and TPS2051 power distribution switches are intended for applications where heavy capacitive loads and short circuits are likely to be encountered. The TPS2041 and the TPS2051 are 135-mΩ N-channel MOSFET high-side power switches. Each switch is controlled by a logic enable compatible with 5-V and 3-V logic. Gate drive is provided by an internal charge pump that controls the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the TPS2041 and TPS2051 limit the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{OC}$) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch in overcurrent to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until valid input voltage is present.

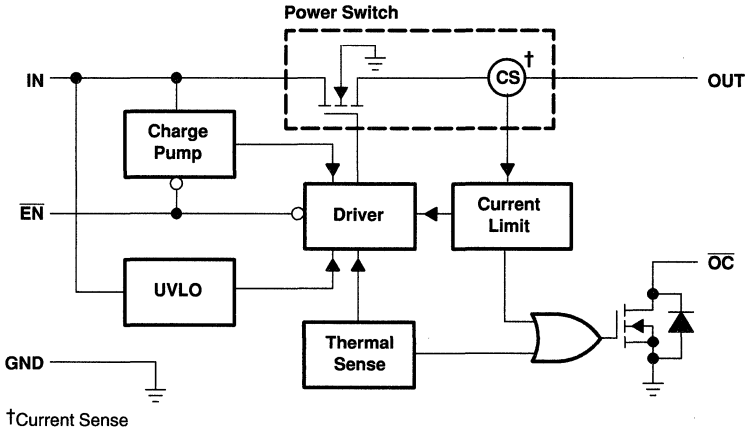
The TPS2041 and TPS2051 are designed to limit at 0.9-A load. These power distribution switches are available in 8-pin small-outline integrated circuit (SOIC) and 8-pin plastic dual-in-line packages (PDIP) and operate over an ambient temperature range of –40°C to 85°C.

AVAILABLE OPTIONS

T_A	ENABLE	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A)	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (A)	PACKAGED DEVICES	
				SOIC (D)†	PDIP (P)
–40°C to 85°C	Active low	0.5	0.9	TPS2041D	TPS2041P
–40°C to 85°C	Active high	0.5	0.9	TPS2051D	TPS2051P

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2041DR)

TPS2041 functional block diagram



Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO. D OR P			
	TPS2041	TPS2051		
$\overline{EN}$	4	–	I	Enable input. Logic low turns on power switch.
EN	–	4	I	Enable input. Logic high turns on power switch.
GND	1	1	I	Ground
IN	2, 3	2, 3	I	Input voltage
$\overline{OC}$	5	5	O	Over current. Logic output active low
OUT	6, 7, 8	6, 7, 8	O	Power-switch output

detailed description

power switch

The power switch is an N-channel MOSFET with a maximum on-state resistance of 135 mΩ ($V_{I(IN)}$ = 5 V). Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled. The power switch supplies a minimum of 500 mA per switch.

charge pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 4-ms range.

enable ($\overline{EN}$ or EN)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10 µA when a logic high is present on $\overline{EN}$ (TPS2041) or a logic low is present on EN (TPS2051). A logic zero input on $\overline{EN}$ or a logic high on EN restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

overcurrent ($\overline{OC}$)

The $\overline{OC}$ open drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed.

current sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant current mode and holds the current constant while varying the voltage on the load.

thermal sense

An internal thermal-sense circuit shuts off the power switch when the junction temperature rises to approximately 140°C. Hysteresis is built into the thermal sense circuit. After the device has cooled approximately 20°C, the switch turns back on. The switch continues to cycle off and on until the fault is removed.

undervoltage lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, $V_{I(IN)}$ (see Note 1) ..... –0.3 V to 6 V
Output voltage range, $V_{O(OUT)}$ (see Note 1) ..... –0.3 V to $V_{I(IN)}$ + 0.3 V
Input voltage range, $V_{I(\overline{ENx})}$ or $V_{I(ENx)}$ ..... –0.3 V to 6 V
Continuous output current, $I_{O(OUT)}$ ..... internally limited
Continuous total power dissipation ..... See Dissipation Rating Table
Operating virtual junction temperature range, T_J ..... –40°C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C
Electrostatic discharge (ESD) protection: Human body model MIL-STD-883C ..... 2 kV
Machine model ..... 0.2 kV

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1175 mW	9.4 mW/°C	752 mW	611 mW

recommended operating conditions

	TPS2041		TPS2051		UNIT
	MIN	MAX	MIN	MAX	
Input voltage, $V_{I(IN)}$	2.7	5.5	2.7	5.5	V
Input voltage, $V_{I(\overline{EN})}$ or $V_{I(EN)}$	0	5.5	0	5.5	V
Continuous output current, $I_{O(OUT)}$	0	500	0	500	mA
Operating virtual junction temperature, T_J	–40	125	–40	125	°C

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $V_{I(\overline{EN})}$ = 0 V, $V_{I(EN)}$ = Hi (unless otherwise noted)

power switch

PARAMETER		TEST CONDITIONS†	TPS2041			TPS2051			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$r_{DS(on)}$	Static drain-source on-state resistance, 5-V operation	$V_{I(IN)}$ = 5 V, T_J = 25°C		80	95		80	95	mΩ
		$V_{I(IN)}$ = 5 V, T_J = 85°C		90	120		90	120	
		$V_{I(IN)}$ = 5 V, T_J = 125°C		100	135		100	135	
	Static drain-source on-state resistance, 3.3-V operation	$V_{I(IN)}$ = 3.3 V, T_J = 25°C		85	105		85	105	
		$V_{I(IN)}$ = 3.3 V, T_J = 85°C		100	135		100	135	
		$V_{I(IN)}$ = 3.3 V, T_J = 125°C		115	150		115	150	
t_r	Rise time, output	$V_{I(IN)}$ = 5.5 V, T_J = 25°C, C_L = 1 µF, R_L = 10 Ω		2.5			2.5		ms
		$V_{I(IN)}$ = 2.7 V, T_J = 25°C, C_L = 1 µF, R_L = 10 Ω		3			3		
t_f	Fall time, output	$V_{I(IN)}$ = 5.5 V, T_J = 25°C, C_L = 1 µF, R_L = 10 Ω		4.4			4.4		ms
		$V_{I(IN)}$ = 2.7 V, T_J = 25°C, C_L = 1 µF, R_L = 10 Ω		2.5			2.5		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

enable input $\overline{EN}$ or EN

PARAMETER			TEST CONDITIONS	TPS2041			TPS2051			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High-level input voltage		2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V	2			2			V
V_{IL}	Low-level input voltage		4.5 V ≤ $V_{I(IN)}$ ≤ 5.5 V			0.8			0.8	V
			2.7 V ≤ $V_{I(IN)}$ ≤ 4.5 V			0.4			0.4	
I_I	Input current	TPS2041	$V_{I(\overline{EN})}$ = 0 V or $V_{I(\overline{EN})}$ = $V_{I(IN)}$	–0.5		0.5				µA
		TPS2051	$V_{I(EN)}$ = $V_{I(IN)}$ or $V_{I(EN)}$ = 0 V				–0.5		0.5	
t_{on}	Turnon time		C_L = 100 µF, R_L = 10 Ω			20			20	ms
t_{off}	Turnoff time		C_L = 100 µF, R_L = 10 Ω			40			40	

current limit

PARAMETER		TEST CONDITIONS†	TPS2041			TPS2051			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{OS}	Short-circuit output current	$V_{I(IN)}$ = 5 V, OUT connected to GND, Device enabled into short circuit	0.7	0.9	1.1	0.7	0.9	1.1	A

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $V_{I(\overline{EN})}$ = 0 V, $V_{I(EN)}$ = Hi (unless otherwise noted) (continued)

supply current

PARAMETER	TEST CONDITIONS				TPS2041			TPS2051			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
Supply current, low-level output	No Load on OUT	$\overline{EN}$ = $V_{I(IN)}$	T_J = 25°C	TPS2041		0.015	1				µA
			–40°C ≤ T_J ≤ 125°C				10				
		EN = 0 V	T_J = 25°C	TPS2051					0.015	1	
			–40°C ≤ T_J ≤ 125°C							10	
Supply current, high-level output	No Load on OUT	$\overline{EN}$ = 0 V	T_J = 25°C	TPS2041		80	100				µA
			–40°C ≤ T_J ≤ 125°C			100					
		EN = $V_{I(IN)}$	T_J = 25°C	TPS2051					80	100	
			–40°C ≤ T_J ≤ 125°C						100		
Leakage current	OUT connected to ground	$\overline{EN}$ = $V_{I(IN)}$	–40°C ≤ T_J ≤ 125°C	TPS2041		100					µA
		EN= 0 V	–40°C ≤ T_J ≤ 125°C	TPS2051					100		
Reverse leakage current	IN = High impedance	$V_{I(\overline{EN})}$ = 0 V	T_J = 25°C	TPS2041		0.3					µA
		$V_{I(EN)}$ = Hi		TPS2051					0.3		

undervoltage lockout

PARAMETER	TEST CONDITIONS	TPS2041			TPS2051			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Low-level input voltage		2		2.5	2		2.5	V
Hysteresis	T_J = 25°C		100			100		mV

overcurrent $\overline{OC}$

PARAMETER	TEST CONDITIONS	TPS2041			TPS2051			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Sink current†	V_O = 5 V			10			10	mA
Output low voltage	I_O = 5 V, $V_{OL(\overline{OC})}$			0.5			0.5	V
Off-state current†	V_O = 5 V, V_O = 3.3 V			1			1	µA

† Specified by design, not production tested.

PARAMETER MEASUREMENT INFORMATION

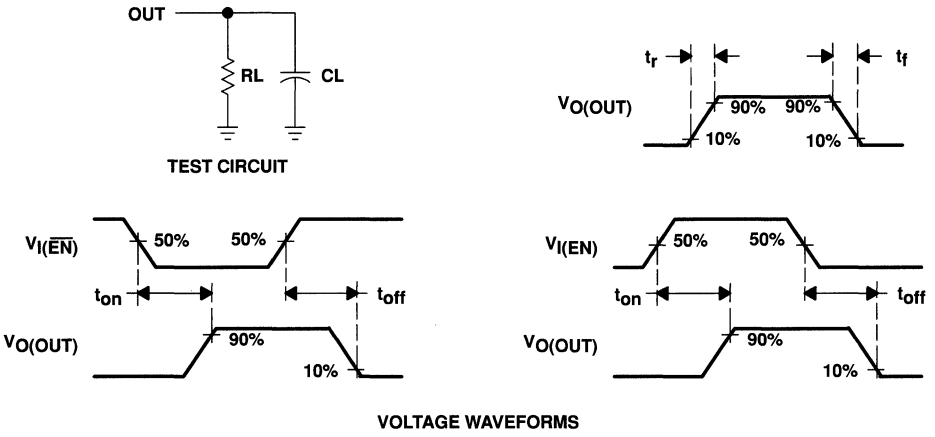


Figure 1. Test Circuit and Voltage Waveforms

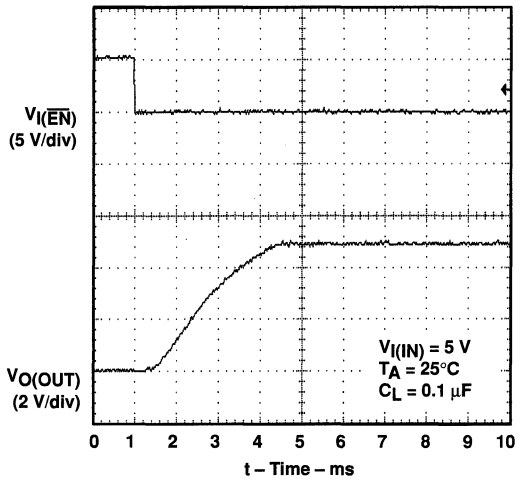


Figure 2. Turnon Delay and Rise Time with 0.1-μF Load

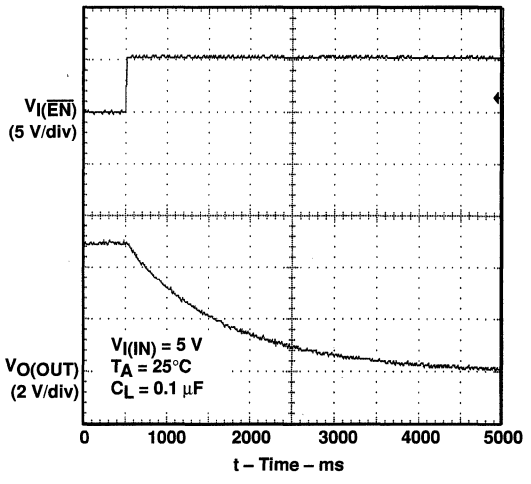


Figure 3. Turnoff Delay and Fall Time with 0.1-μF Load

PARAMETER MEASUREMENT INFORMATION

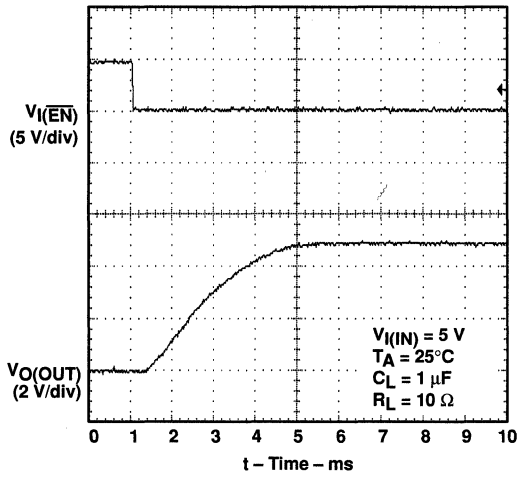


Figure 4. Turnon Delay and Rise Time with 1-μF Load

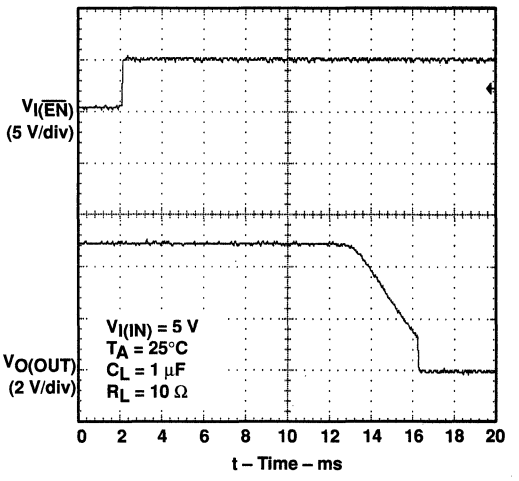


Figure 5. Turnoff Delay and Fall Time with 1-μF Load

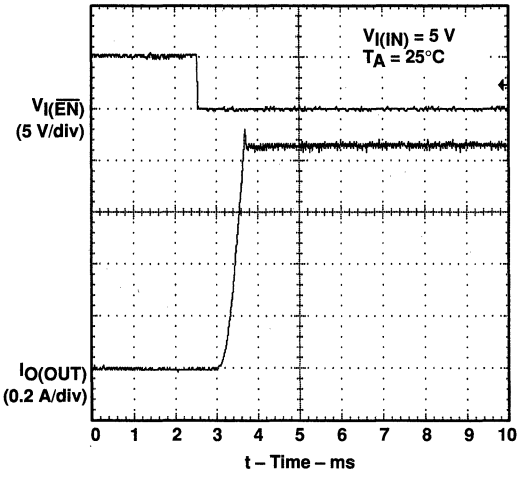


Figure 6. TPS2041, Short-Circuit Current, Device Enabled into Short

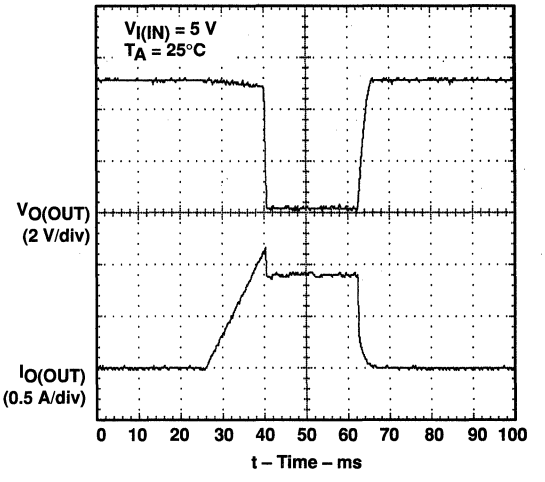


Figure 7. TPS2041, Threshold Trip Current with Ramped Load on Enabled Device

PARAMETER MEASUREMENT INFORMATION

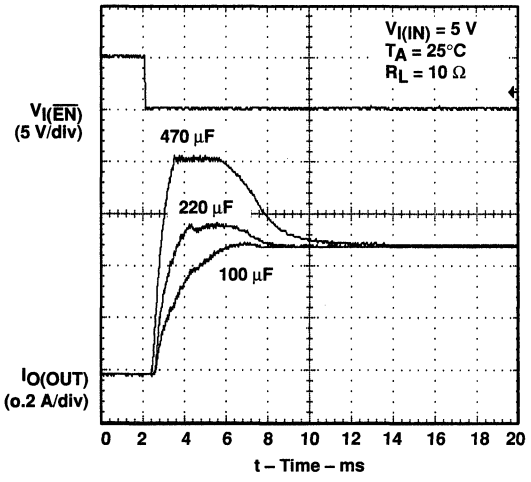


Figure 8. Inrush Current with 100-µF, 220-µF and 470-µF Load Capacitance

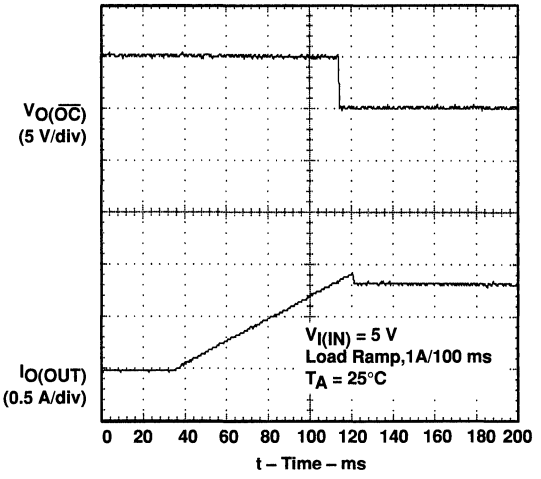


Figure 9. Ramped Load on Enabled Device

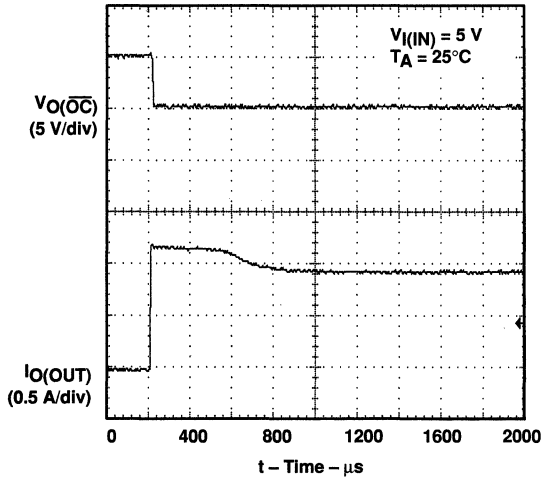


Figure 10. 4-Ω Load Connected to Enabled Device

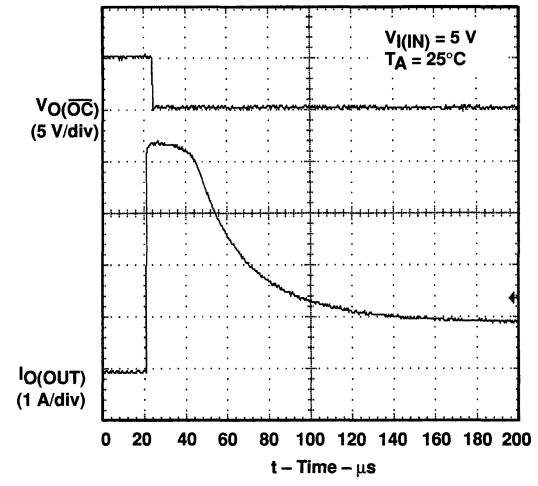


Figure 11. 1-Ω Load Connected to Enabled Device

TYPICAL CHARACTERISTICS

TURNON DELAY
vs
INPUT VOLTAGE

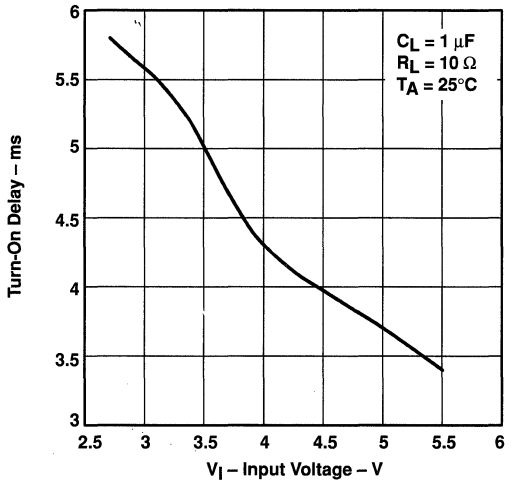


Figure 12

TURNOFF DELAY
vs
INPUT VOLTAGE

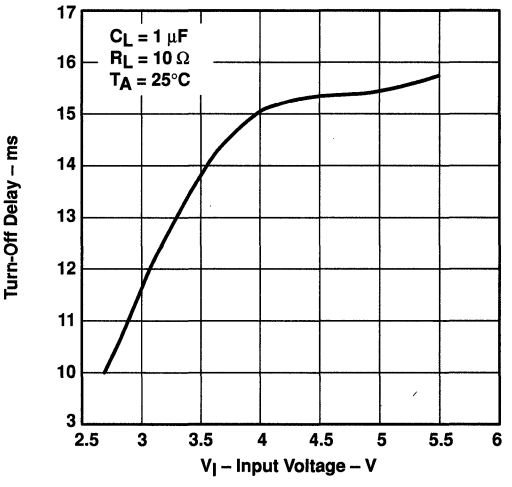


Figure 13

RISE TIME
vs
LOAD CURRENT

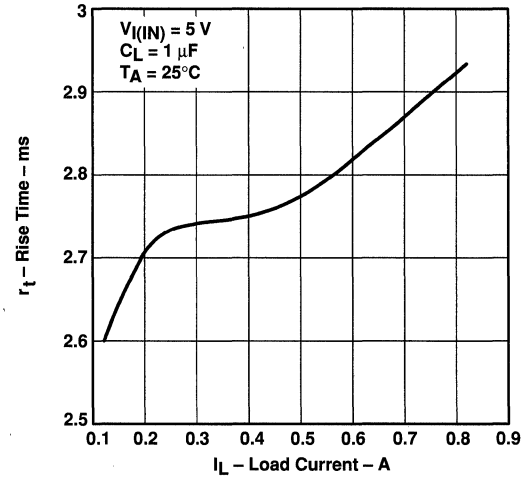


Figure 14

FALL TIME
vs
LOAD CURRENT

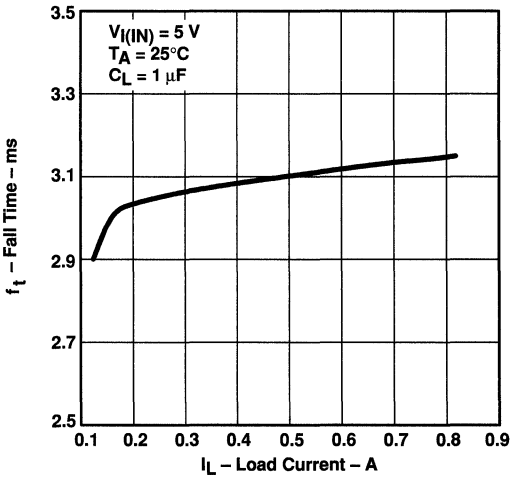


Figure 15

TYPICAL CHARACTERISTICS

SUPPLY CURRENT, OUTPUT ENABLED
vs
JUNCTION TEMPERATURE

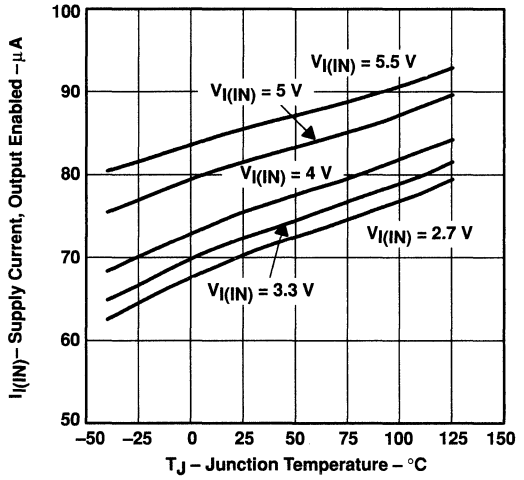


Figure 16

SUPPLY CURRENT, OUTPUT DISABLED
vs
JUNCTION TEMPERATURE

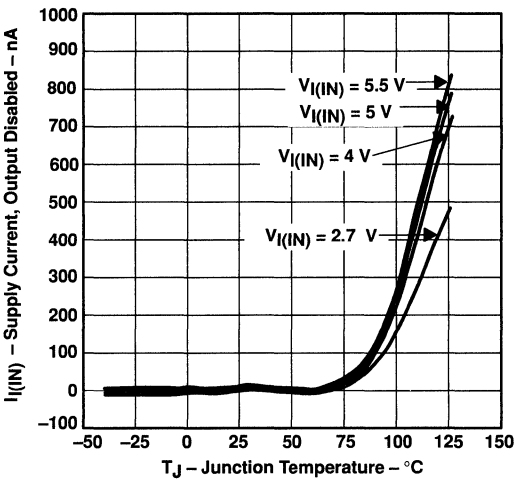


Figure 17

SUPPLY CURRENT, OUTPUT ENABLED
vs
INPUT VOLTAGE

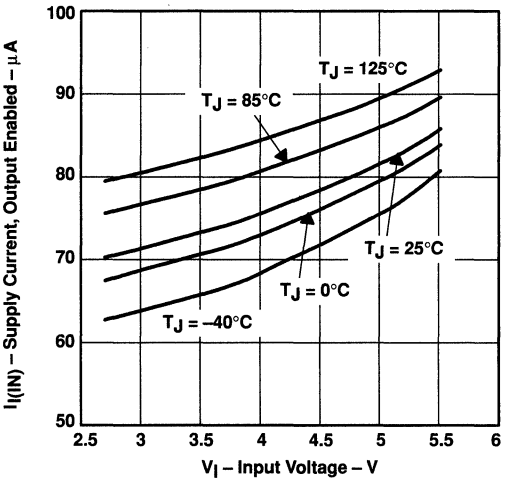


Figure 18

SUPPLY CURRENT, OUTPUT DISABLED
vs
INPUT VOLTAGE

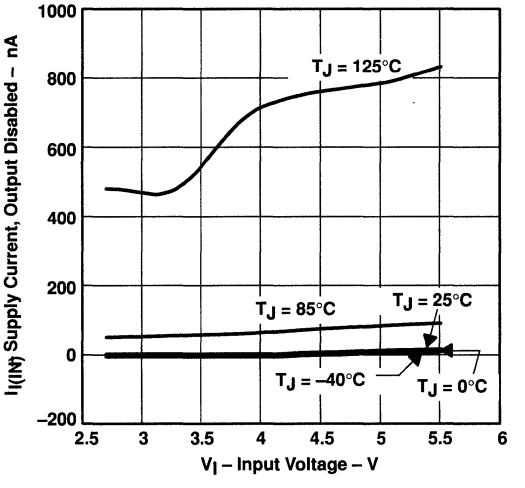


Figure 19

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

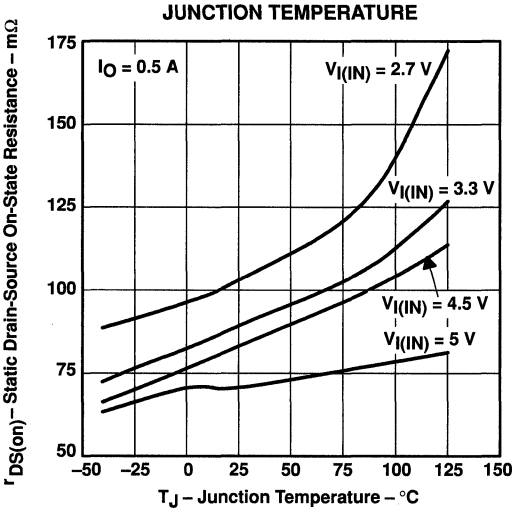


Figure 20

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
INPUT VOLTAGE

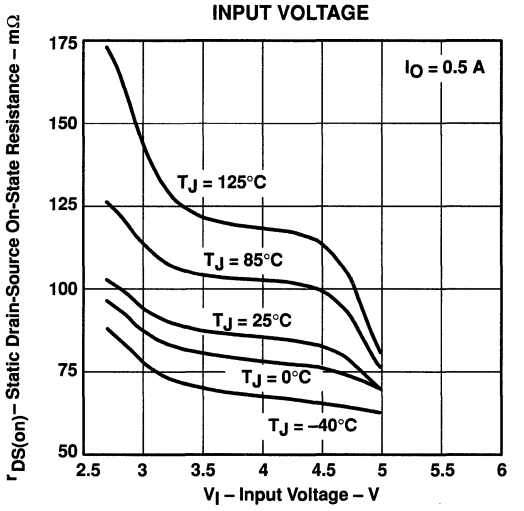


Figure 21

INPUT-TO-OUTPUT VOLTAGE
vs
LOAD CURRENT

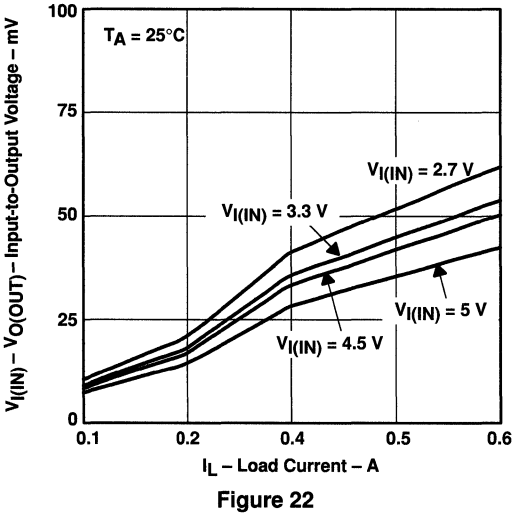


Figure 22

SHORT-CURCUIT OUTPUT CURRENT
vs
INPUT VOLTAGE

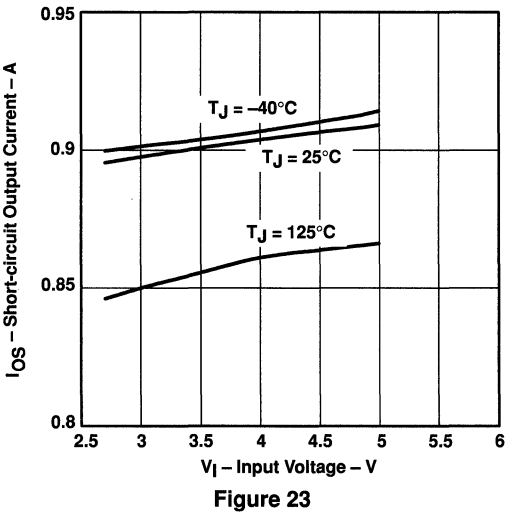


Figure 23

TYPICAL CHARACTERISTICS

THRESHOLD TRIP CURRENT
vs
INPUT VOLTAGE

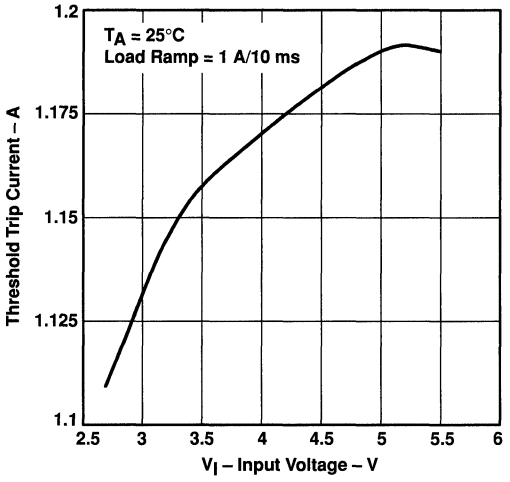


Figure 24

SHORT CIRCUIT OUTPUT CURRENT
vs
JUNCTION TEMPERATURE

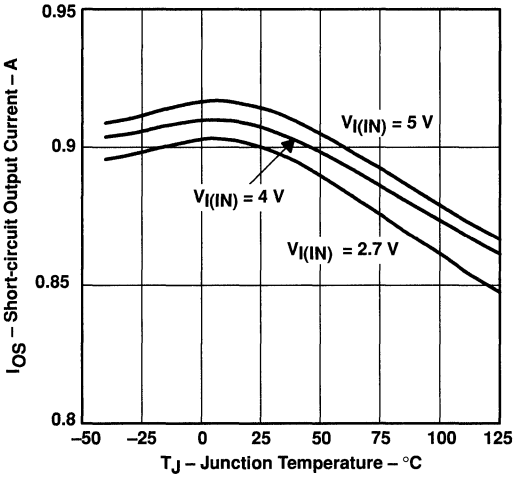


Figure 25

UNDERVOLTAGE LOCKOUT
vs
JUNCTION TEMPERATURE

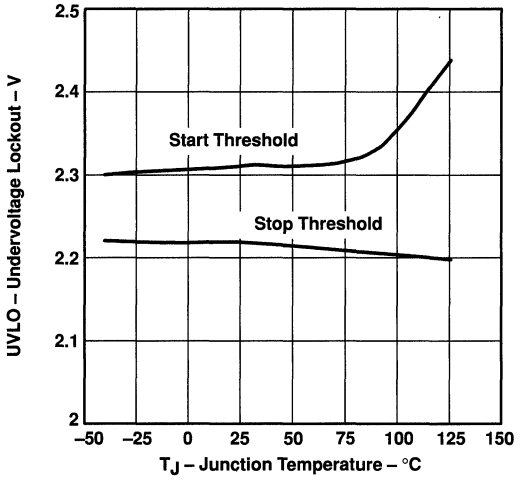


Figure 26

CURRENT LIMIT RESPONSE
vs
PEAK CURRENT

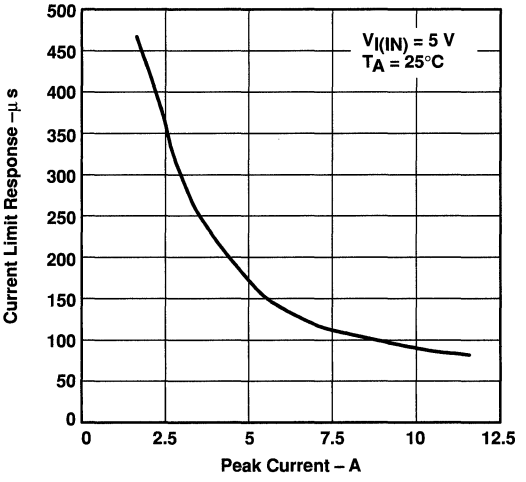


Figure 27

TYPICAL CHARACTERISTICS

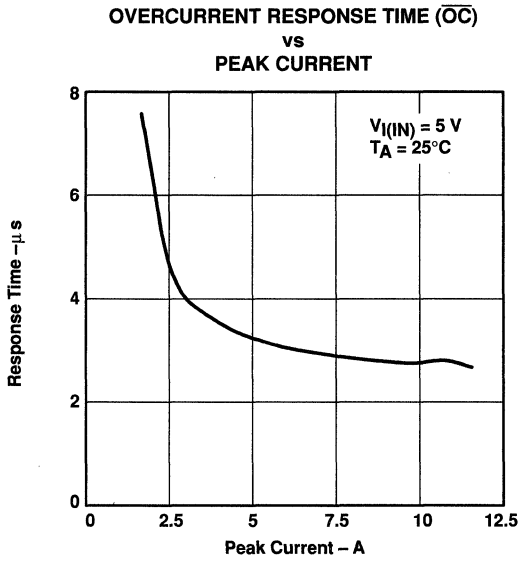


Figure 28

APPLICATION INFORMATION

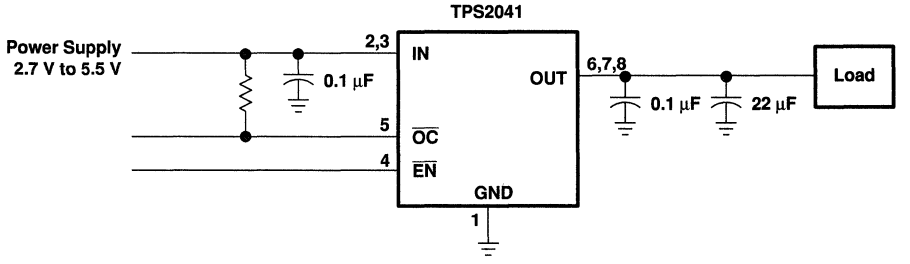


Figure 29. Typical Application

power-supply considerations

A 0.01-µF to 0.1-µF ceramic bypass capacitor between INx and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-µF to 0.1-µF ceramic capacitor improves the immunity of the device to short-circuit transients.

APPLICATION INFORMATION

overcurrent

A sense FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 6). The TPS2041 and TPS2051 sense the short and immediately switch into a constant-current output.

In the second condition, the short occurs while the device is enabled. At the instant the short occurs, very high currents may flow for a short time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshhold) the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figure 7). The TPS2041 and TPS2051 are capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

$\overline{OC}$ response

The $\overline{OC}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false overcurrent reporting from the inrush current flowing through the device, charging the downstream capacitor. An RC filter of 500 µs (see Figure 30) can be connected to the $\overline{OC}$ pin to reduce false overcurrent reporting. Using low-ESR electrolytic capacitors on the output lowers the inrush current flow through the device during hot-plug events by providing a low-impedance energy source, thereby reducing erroneous overcurrent reporting.

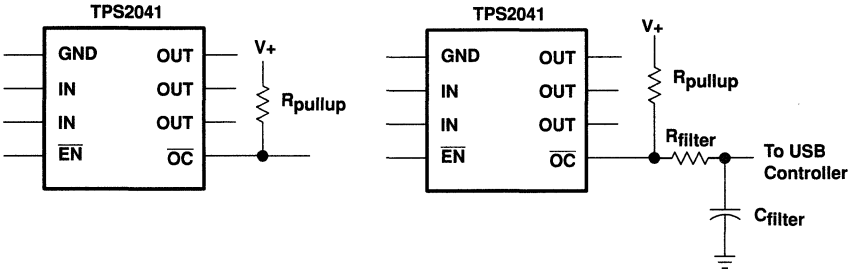


Figure 30. Typical Circuit for $\overline{OC}$ Pin and RC Filter for Damping Inrush $\overline{OC}$ Responses

APPLICATION INFORMATION

power dissipation and junction temperature

The low on-resistance on the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find $r_{DS(on)}$ at the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figure 21. Next, calculate the power dissipation using:

$$P_D = r_{DS(on)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient Temperature °C
$R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W, PDIP = 106°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

thermal protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS2041 and TPS2051 into constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels. The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

undervoltage lockout (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at powerup. Whenever the input voltage falls below approximately 2 V, the power switch will be quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO will also keep the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. Upon reinsertion, the power switch will be turned on, with a controlled rise time to reduce EMI and voltage overshoots.

universal serial bus (USB) applications

The universal serial bus (USB) interface is a 12-Mb/s, or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

APPLICATION INFORMATION

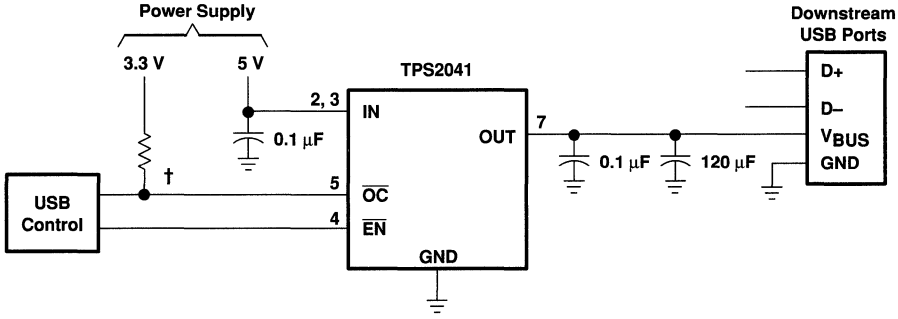
The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

Self-powered and bus-powered hubs distribute data and power to downstream functions. The TPS2041 and TPS2051 can provide power-distribution solutions for many of these classes of devices.

host/self-powered and bus-powered hubs

Hosts and self-powered hubs have a local power supply that powers the embedded functions and the downstream ports (see Figure 31). This power supply must provide from 5.25 V to 4.75 V to the board side of the downstream connection under full-load and no-load conditions. Hosts and SPHs are required to have current limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.



† May need RC Filter (see Figure 34)

Figure 31. One-Port Solution

Bus-powered hubs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on powerup, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

APPLICATION INFORMATION

low-power bus-powered functions and high-power bus-powered functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at powerup and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 µF at powerup, the device must implement inrush current limiting (see Figure 32).

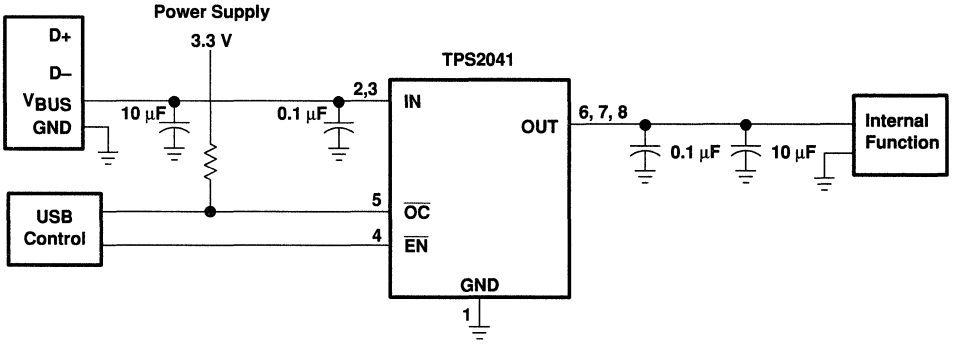


Figure 32. High-Power Bus-Powered Function

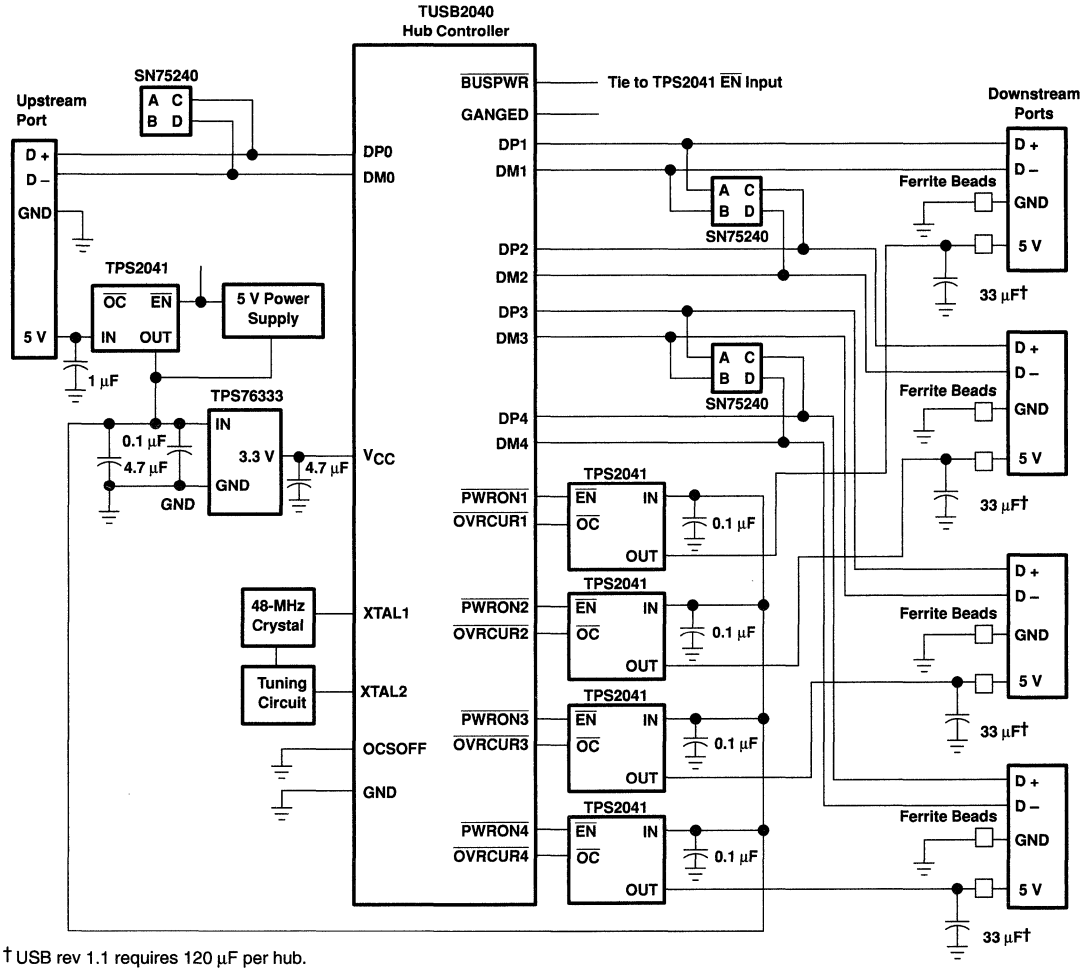
USB power-distribution requirements

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several powe- distribution features must be implemented.

- Hosts/self-powered hubs must:
  - Current-limit downstream ports
  - Report overcurrent conditions on USB V_{BUS}
- Bus-powered hubs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 µF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

The feature set of the TPS2041 and TPS2051 allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-power hubs, as well as the input ports for bus-power functions (see Figure 33).

APPLICATION INFORMATION



† USB rev 1.1 requires 120 µF per hub.

Figure 33. Hybrid Self/Bus-Powered Hub Implementation

APPLICATION INFORMATION

generic hot-plug applications (see Figure 34)

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS2041 and TPS2051, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS2041 and TPS2051 also ensures the switch will be off after the card has been removed, and the switch will be off during the next insertion. The UVLO feature guarantees a soft start with a controlled rise time for every insertion of the card or module.

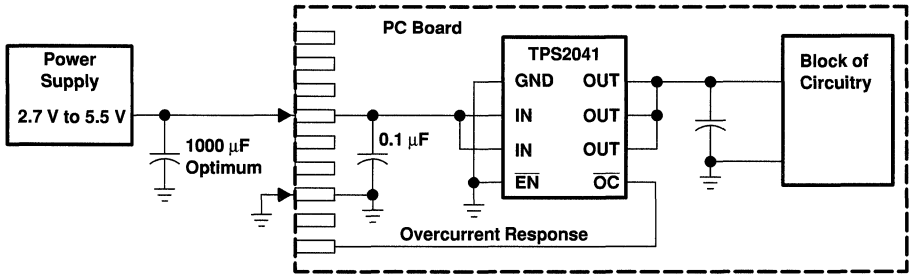


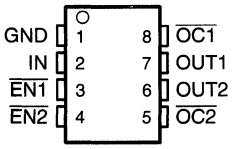
Figure 34. Typical Hot-Plug Implementation

By placing the TPS2041 and TPS2051 between the V_{CC} input and the rest of the circuitry, the input power will reach these devices first after insertion. The typical rise time of the switch is approximately 2.5 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

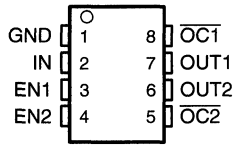
SLVS173A – AUGUST 1998 – REVISED APRIL 1999

- **135-mΩ -Maximum (5-V Input) High-Side MOSFET Switch**
- **500 mA Continuous Current per Channel**
- **Short-Circuit and Thermal Protection With Overcurrent Logic Output**
- **Operating Range . . . 2.7-V to 5.5-V**
- **Logic-Level Enable Input**
- **2.5-ms Typical Rise Time**
- **Undervoltage Lockout**
- **10 μA Maximum Standby Supply Current**
- **Bidirectional Switch**
- **Available in 8-pin SOIC and PDIP Packages**
- **Ambient Temperature Range, –40°C to 85°C**
- **2-kV Human-Body-Model, 200-V Machine-Model ESD Protection**
- **UL Listed – File No. E169910**

TPS2042
D OR P PACKAGE
(TOP VIEW)



TPS2052
D OR P PACKAGE
(TOP VIEW)



description

The TPS2042 and TPS2052 dual power distribution switches are intended for applications where heavy capacitive loads and short circuits are likely to be encountered. The TPS2042 and the TPS2052 incorporate in single packages two 135-mΩ N-channel MOSFET high-side power switches for power distribution systems that require multiple power switches. Each switch is controlled by a logic enable that is compatible with 5-V logic and 3-V logic. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the TPS2042 and TPS2052 limit the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{OCx}$) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until valid input voltage is present.

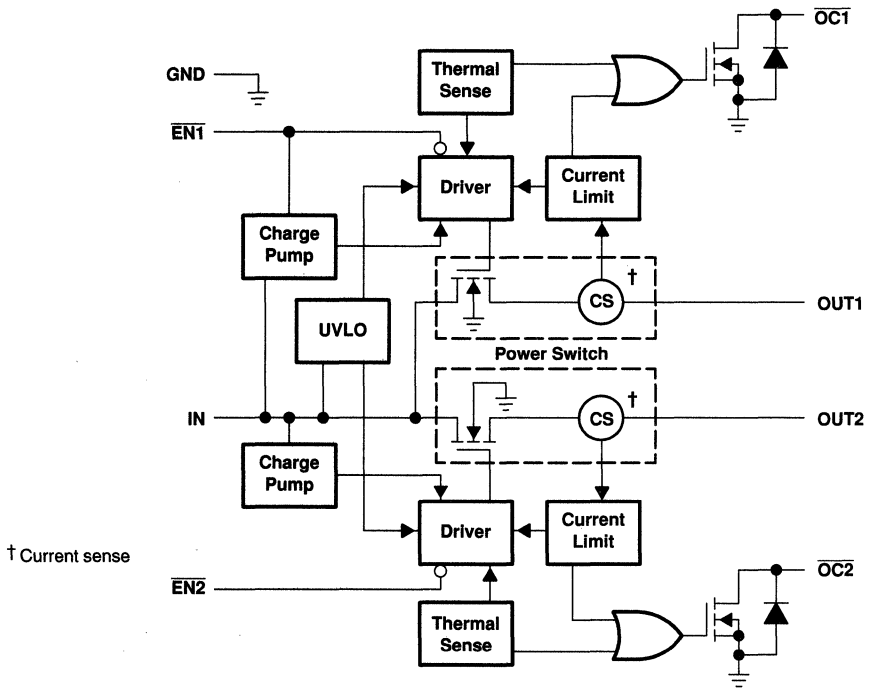
The TPS2042 and TPS2052 are designed to limit at 0.9-A load. These power distribution switches are available in 8-pin small-outline integrated circuit (SOIC) and 8-pin plastic dual-in-line packages (PDIP) and operate over an ambient temperature range of –40°C to 85°C.

AVAILABLE OPTIONS

T_A	ENABLE	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A)	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (A)	PACKAGED DEVICES	
				SOIC (D)†	PDIP (P)
–40°C to 85°C	Active low	0.5	0.9	TPS2042D	TPS2042P
–40°C to 85°C	Active high	0.5	0.9	TPS2052D	TPS2052P

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2042DR)

TPS2042 functional block diagram



Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO. D OR P			
	TPS2042	TPS2052		
$\overline{EN1}$	3	–	I	Enable input. Logic low turns on power switch, IN-OUT1.
$\overline{EN2}$	4	–	I	Enable input. Logic low turns on power switch, IN-OUT2.
EN1	–	3	I	Enable input. Logic high turns on power switch, IN-OUT1.
EN2	–	4	I	Enable input. Logic high turns on power switch, IN-OUT2.
GND	1	1	I	Ground
IN	2	2	I	Input voltage
$\overline{OC1}$	8	8	O	Over current. Logic output active low, for power switch, IN-OUT1
$\overline{OC2}$	5	5	O	Over current. Logic output active low, for power switch, IN-OUT2
OUT1	7	7	O	Power-switch output
OUT2	6	6	O	Power-switch output

detailed description

power switch

The power switch is an N-channel MOSFET with a maximum on-state resistance of 135 mΩ ($V_{I(IN)}$ = 5 V). Configured as a high-side switch, the power switch prevents current flow from OUTx to IN and IN to OUTx when disabled. The power switch supplies a minimum of 500 mA per switch.

charge pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 4-ms range.

enable ($\overline{\text{ENx}}$ or ENx)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10 μA when a logic high is present on $\overline{\text{ENx}}$ (TPS2042) or a logic low is present on ENx (TPS2052). A logic zero input on $\overline{\text{ENx}}$ or logic high on ENx restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

overcurrent ($\overline{\text{OCx}}$)

The $\overline{\text{OCx}}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed.

current sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant current mode and holds the current constant while varying the voltage on the load.

thermal sense

The TPS2042 and TPS2052 implement a dual-threshold thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition the junction temperature rises. When the die temperature rises to approximately 140°C, the internal thermal sense circuitry checks to determine which power switch is in an overcurrent condition and turns off that switch, thus isolating the fault without interrupting operation of the adjacent power switch. Hysteresis is built into the thermal sense, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed. The ($\overline{\text{OCx}}$) open-drain output is asserted (active low) when overtemperature or overcurrent occurs.

undervoltage lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, $V_{I(IN)}$ (see Note1) ..... –0.3 V to 6 V
Output voltage range, $V_{O(OUTx)}$ (see Note1) ..... –0.3 V to $V_{I(IN)}$ + 0.3 V
Input voltage range, $V_{I(\overline{ENx})}$ or $V_{I(ENx)}$ ..... –0.3 V to 6 V
Continuous output current, $I_{O(OUTx)}$ ..... internally limited
Continuous total power dissipation ..... See Dissipation Rating Table
Operating virtual junction temperature range, T_J ..... –40°C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C
Electrostatic discharge (ESD) protection: Human body model MIL-STD-883C ..... 2 kV
Machine model ..... 0.2 kV

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1175 mW	9.4 mW/°C	752 mW	611 mW

recommended operating conditions

	TPS2042		TPS2052		UNIT
	MIN	MAX	MIN	MAX	
Input voltage, $V_{I(IN)}$	2.7	5.5	2.7	5.5	V
Input voltage, $V_{I(\overline{ENx})}$ or $V_{I(ENx)}$	0	5.5	0	5.5	V
Continuous output current, $I_{O(OUTx)}$	0	500	0	500	mA
Operating virtual junction temperature, T_J	–40	125	–40	125	°C

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $V_{I(\overline{ENx})}$ = 0 V, $V_{I(ENx)}$ = Hi (unless otherwise noted)

power switch

PARAMETER		TEST CONDITIONS†	TPS2042			TPS2052			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$r_{DS(on)}$	Static drain-source on-state resistance, 5-V operation	$V_{I(IN)}$ = 5 V, T_J = 25°C, I_O = 0.5 A		80	95		80	95	mΩ
		$V_{I(IN)}$ = 5 V, T_J = 85°C, I_O = 0.5 A		90	120		90	120	
		$V_{I(IN)}$ = 5 V, T_J = 125°C, I_O = 0.5 A		100	135		100	135	
	Static drain-source on-state resistance, 3.3-V operation	$V_{I(IN)}$ = 3.3 V, T_J = 25°C, I_O = 0.5 A		85	105		85	105	
		$V_{I(IN)}$ = 3.3 V, T_J = 85°C, I_O = 0.5 A		100	135		100	135	
		$V_{I(IN)}$ = 3.3 V, T_J = 125°C, I_O = 0.5 A		115	150		115	150	
t_r	Rise time, output	$V_{I(IN)}$ = 5.5 V, T_J = 25°C, C_L = 1 µF, R_L=10 Ω		2.5			2.5		ms
		$V_{I(IN)}$ = 2.7 V, T_J = 25°C, C_L = 1 µF, R_L=10 Ω		3			3		
t_f	Fall time, output	$V_{I(IN)}$ = 5.5 V, T_J = 25°C, C_L = 1 µF, R_L=10 Ω		4.4			4.4		ms
		$V_{I(IN)}$ = 2.7 V, T_J = 25°C, C_L = 1 µF, R_L=10 Ω		2.5			2.5		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

enable input $\overline{ENx}$ or ENx

PARAMETER			TEST CONDITIONS	TPS2042			TPS2052			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High-level input voltage		2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V	2			2			V
V_{IL}	Low-level input voltage		4.5 V ≤ $V_{I(IN)}$ ≤ 5.5 V			0.8			0.8	V
			2.7 V≤ $V_{I(IN)}$ ≤ 4.5 V			0.4			0.4	
I_I	Input current	TPS2042	$V_{I(\overline{ENx})}$ = 0 V or $V_{I(\overline{ENx})}$ = $V_{I(IN)}$	–0.5		0.5				µA
		TPS2052	$V_{I(ENx)}$ = $V_{I(IN)}$ or $V_{I(ENx)}$ = 0 V				–0.5		0.5	
t_{on}	Turnon time		C_L = 100 µF, R_L=10 Ω			20			20	ms
t_{off}	Turnoff time		C_L = 100 µF, R_L=10 Ω			40			40	

current limit

PARAMETER		TEST CONDITIONS†	TPS2042			TPS2052			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{OS}	Short-circuit output current	$V_{I(IN)}$ = 5 V, OUT connected to GND, Device enable into short circuit	0.7	0.9	1.1	0.7	0.9	1.1	A

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $V_{I(\overline{ENx})}$ = 0 V, $V_{I(ENx)}$ = Hi (unless otherwise noted) (continued)

supply current

PARAMETER	TEST CONDITIONS				TPS2042			TPS2052			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
Supply current, low-level output	No Load on OUT	$V_{I(\overline{ENx})} = V_{I(IN)}$	T_J = 25°C	TPS2042		0.015	1				µA
			–40°C ≤ T_J ≤ 125°C				10				
		$V_{I(ENx)}$ = 0 V	T_J = 25°C	TPS2052					0.015	1	
			–40°C ≤ T_J ≤ 125°C							10	
Supply current, high-level output	No Load on OUT	$V_{I(\overline{ENx})}$ = 0 V	T_J = 25°C	TPS2042		80	100				µA
			–40°C ≤ T_J ≤ 125°C			100					
		$V_{I(ENx)} = V_{I(IN)}$	T_J = 25°C	TPS2052					80	100	
			–40°C ≤ T_J ≤ 125°C						100		
Leakage current	OUT connected to ground	$V_{I(\overline{ENx})} = V_{I(IN)}$	–40°C ≤ T_J ≤ 125°C	TPS2042		100					µA
		$V_{I(ENx)}$ = 0 V	–40°C ≤ T_J ≤ 125°C	TPS2052					100		
Reverse leakage current	IN = high impedance	$V_{I(\overline{EN})}$ = 0 V	T_J = 25°C	TPS2042		0.3					µA
		$V_{I(EN)}$ = Hi		TPS2052					0.3		

undervoltage lockout

PARAMETER	TEST CONDITIONS	TPS2042			TPS2052			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Low-level input voltage		2		2.5	2		2.5	V
Hysteresis	T_J = 25°C		100			100		mV

overcurrent $\overline{OCx}$

PARAMETER	TEST CONDITIONS	TPS2042			TPS2052			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Sink current†	V_O = 5 V			10			10	mA
Output low voltage	I_O = 5 mA, $V_{OL(\overline{OCx})}$			0.5			0.5	V
Off-state current†	V_O = 5 V, V_O = 3.3 V			1			1	µA

† Specified by design, not production tested.

PARAMETER MEASUREMENT INFORMATION

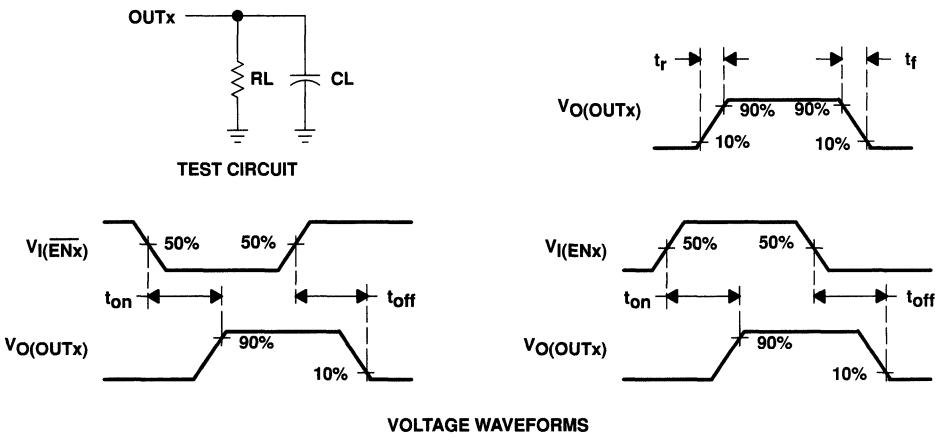


Figure 1. Test Circuit and Voltage Waveforms

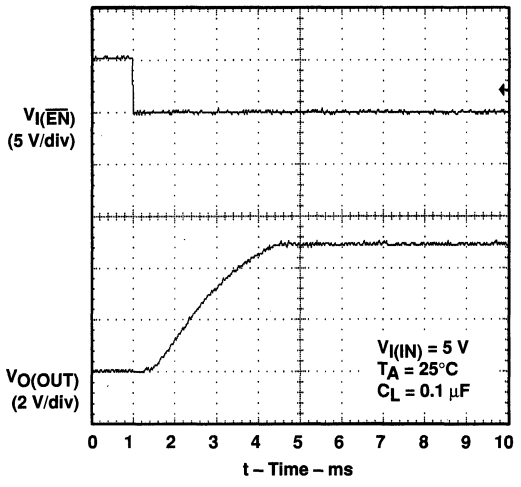


Figure 2. Turnon Delay and Rise Time with 0.1-μF Load

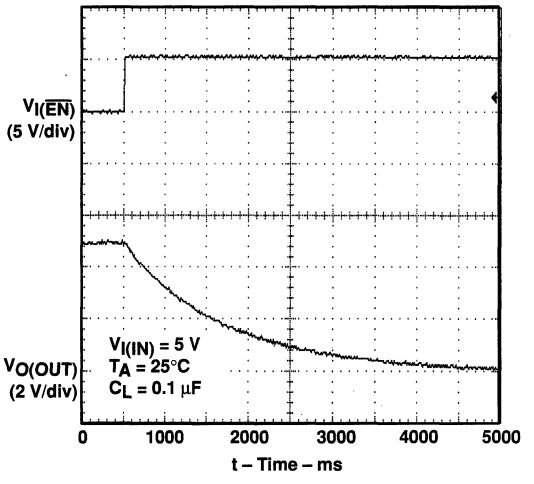


Figure 3. Turnoff Delay and Fall Time with 0.1-μF Load

PARAMETER MEASUREMENT INFORMATION

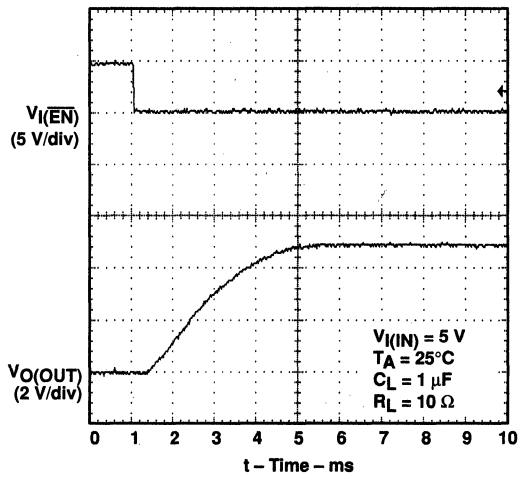


Figure 4. Turnon Delay and Rise Time with 1-μF Load

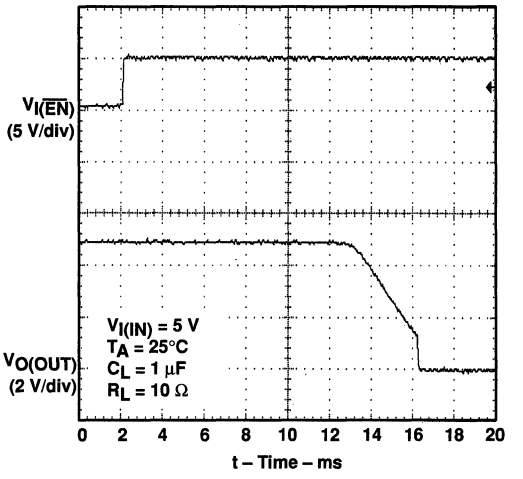


Figure 5. Turnoff Delay and Fall Time with 1-μF Load

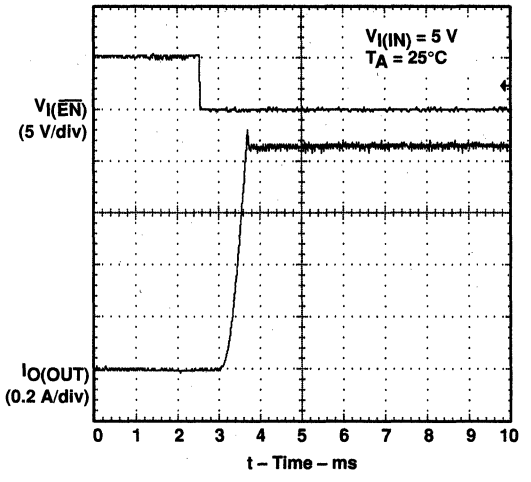


Figure 6. TPS2042, Short-Circuit Current, Device Enabled into Short

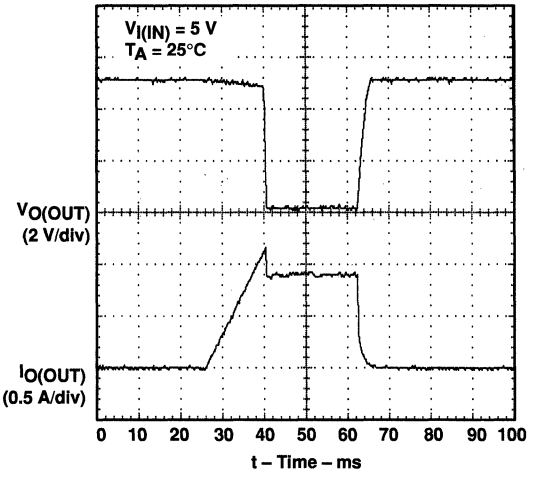


Figure 7. TPS2042, Threshold Trip Current with Ramped Load on Enabled Device

PARAMETER MEASUREMENT INFORMATION

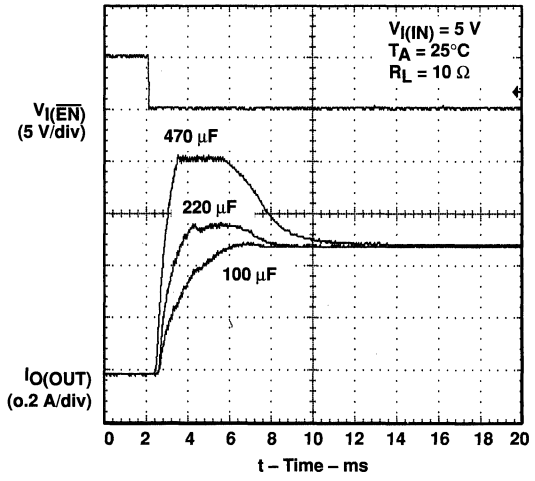


Figure 8. Inrush Current with 100-µF, 220-µF and 470-µF Load Capacitance

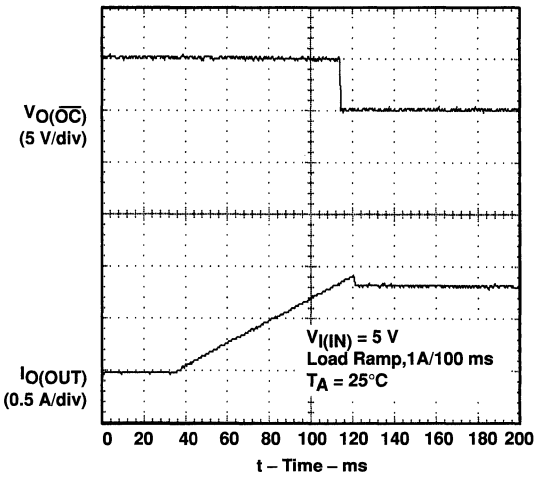


Figure 9. Ramped Load on Enabled Device

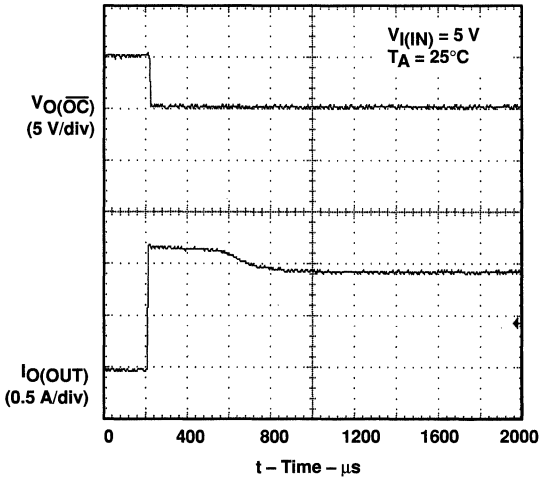


Figure 10. 4-Ω Load Connected to Enabled Device

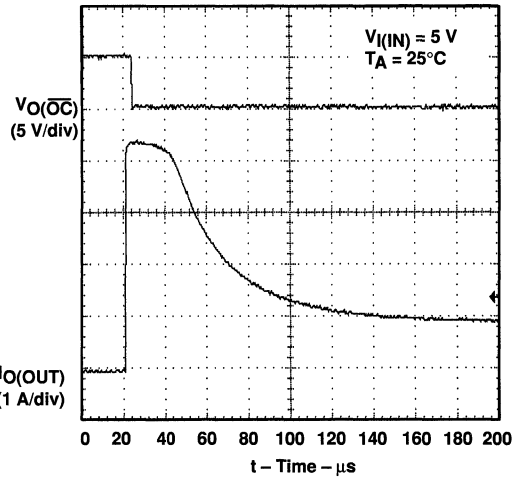


Figure 11. 1-Ω Load Connected to Enabled Device

TYPICAL CHARACTERISTICS

TURNON DELAY
vs
INPUT VOLTAGE

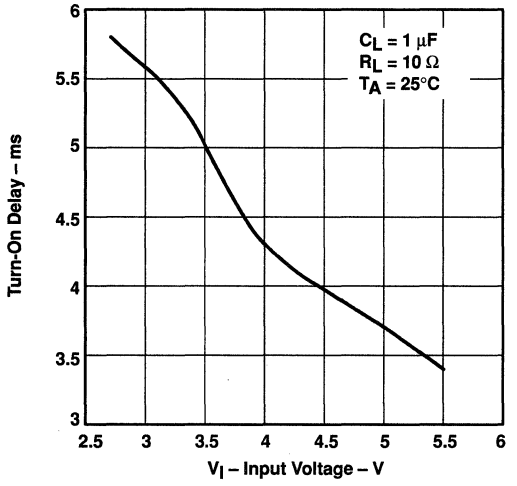


Figure 12

TURNOFF DELAY
vs
INPUT VOLTAGE

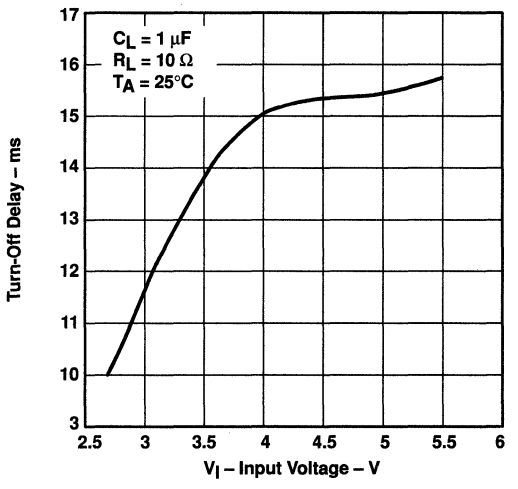


Figure 13

RISE TIME
vs
LOAD CURRENT

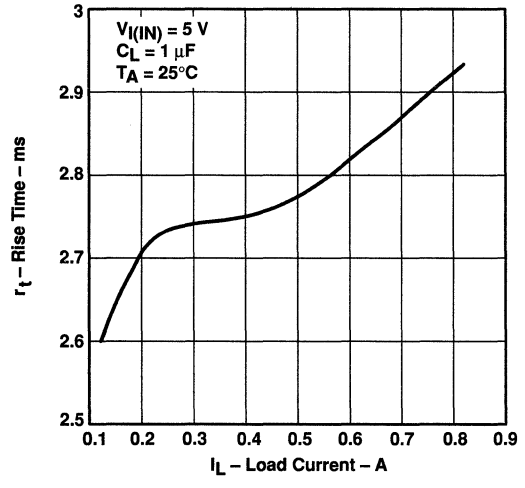


Figure 14

FALL TIME
vs
LOAD CURRENT

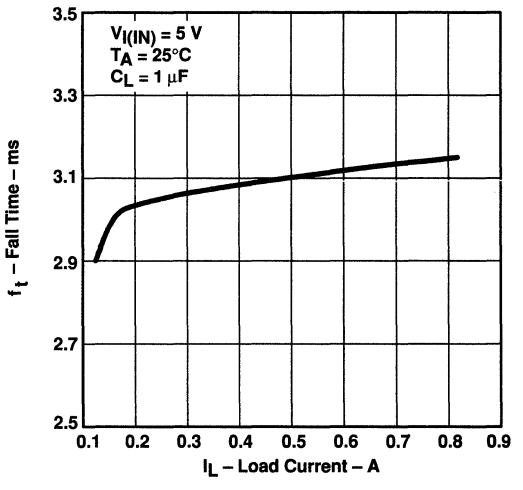


Figure 15

TYPICAL CHARACTERISTICS

SUPPLY CURRENT, OUTPUT ENABLED
vs
JUNCTION TEMPERATURE

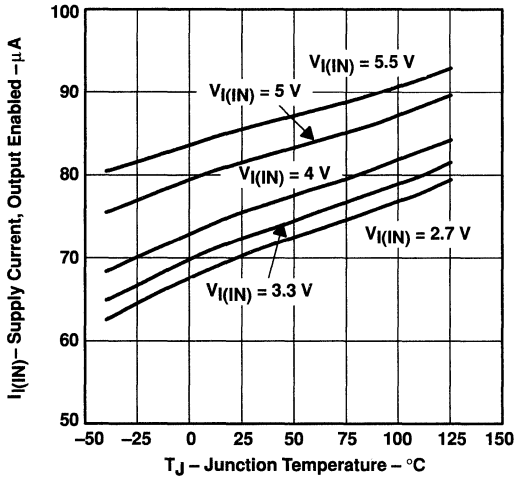


Figure 16

SUPPLY CURRENT, OUTPUT DISABLED
vs
JUNCTION TEMPERATURE

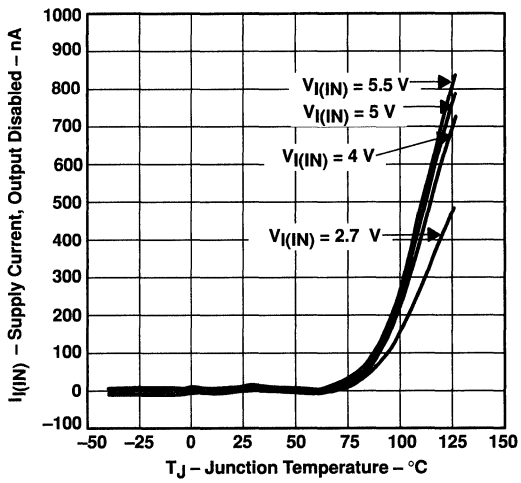


Figure 17

SUPPLY CURRENT, OUTPUT ENABLED
vs
INPUT VOLTAGE

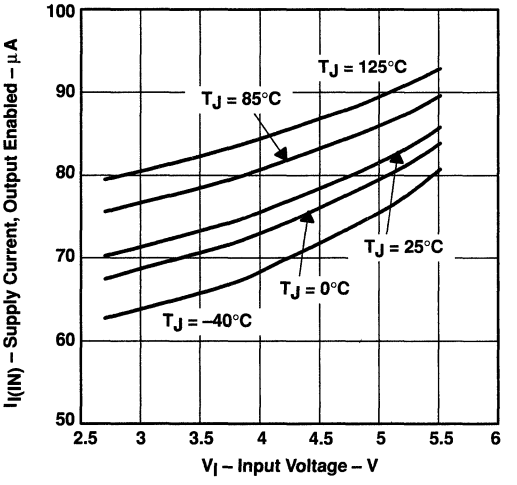


Figure 18

SUPPLY CURRENT, OUTPUT DISABLED
vs
INPUT VOLTAGE

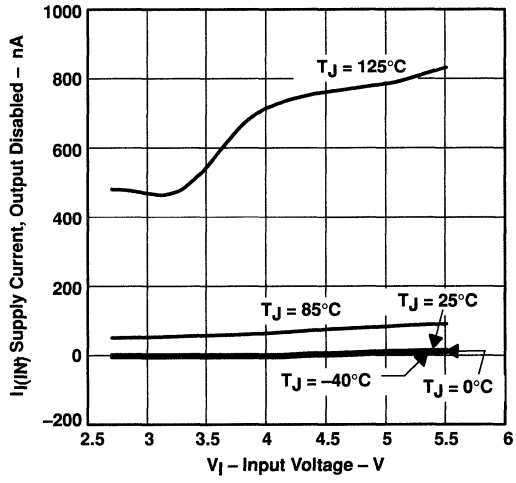


Figure 19

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

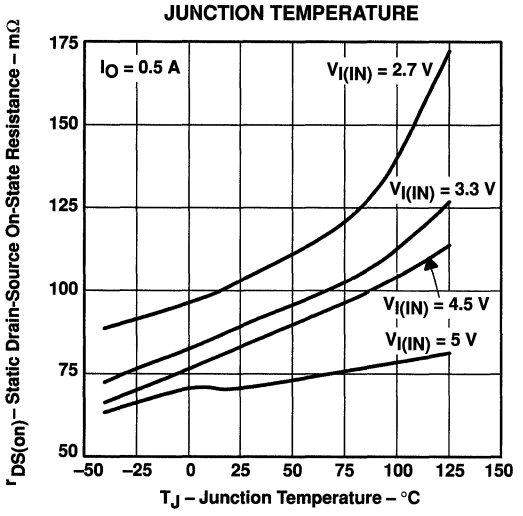


Figure 20

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
INPUT VOLTAGE

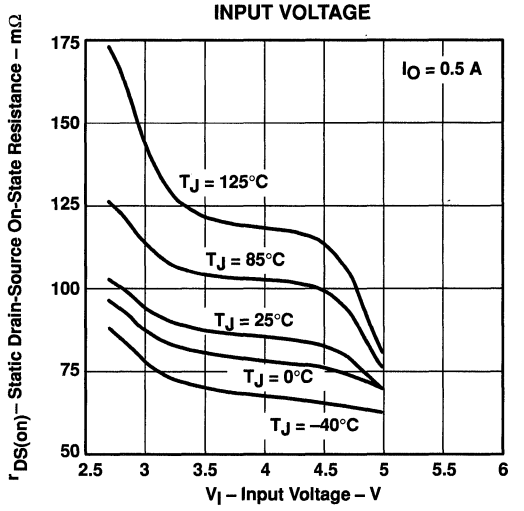


Figure 21

INPUT-TO-OUTPUT VOLTAGE
vs
LOAD CURRENT

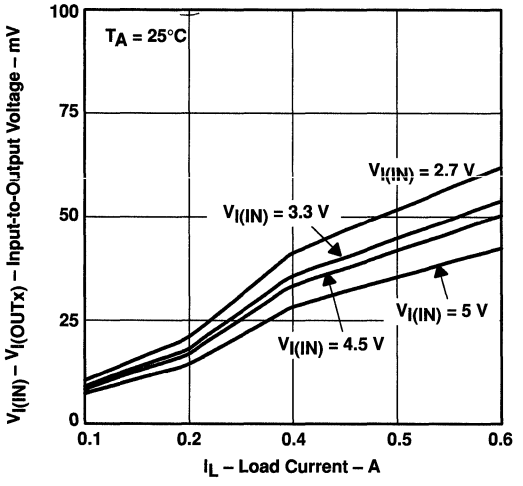


Figure 22

SHORT-CURCUIT OUTPUT CURRENT
vs
INPUT VOLTAGE

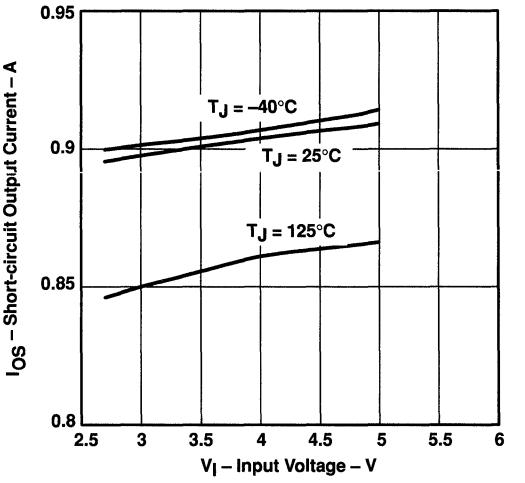


Figure 23

TYPICAL CHARACTERISTICS

THRESHOLD TRIP CURRENT
vs
INPUT VOLTAGE

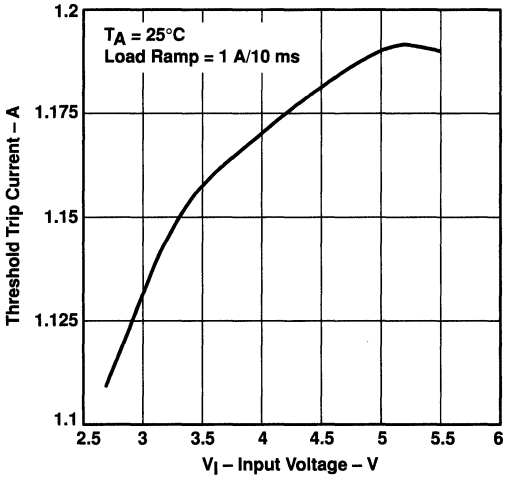


Figure 24

SHORT CIRCUIT OUTPUT CURRENT
vs
JUNCTION TEMPERATURE

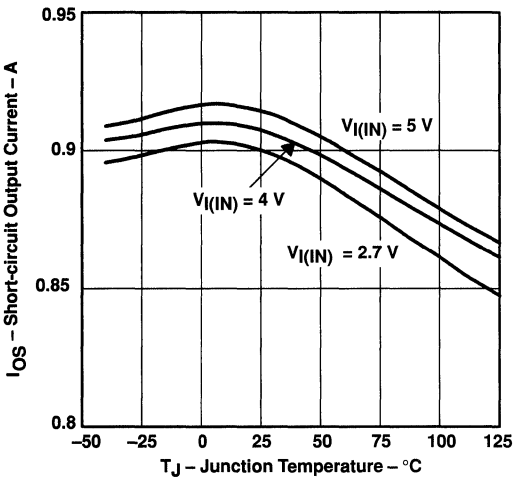


Figure 25

UNDERVOLTAGE LOCKOUT
vs
JUNCTION TEMPERATURE

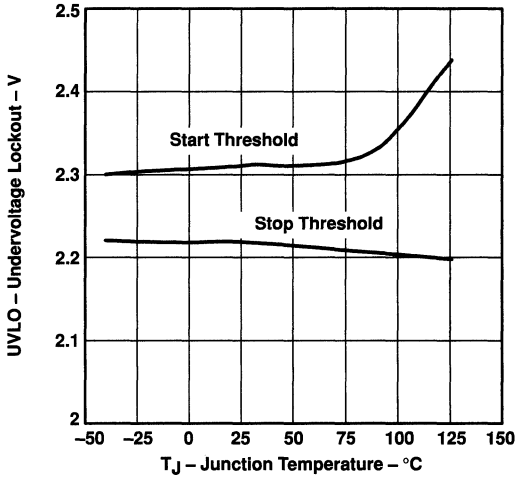


Figure 26

CURRENT-LIMIT RESPONSE
vs
PEAK CURRENT

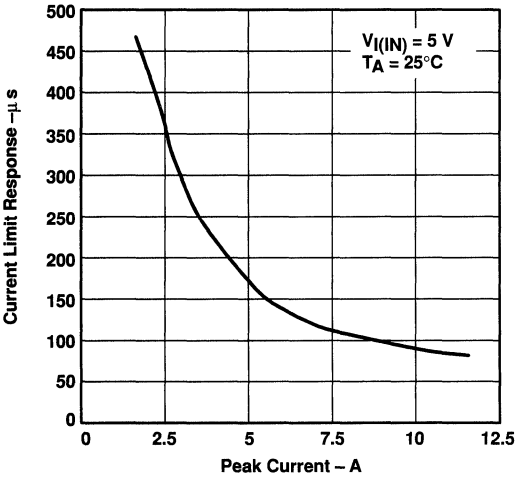


Figure 27

TYPICAL CHARACTERISTICS

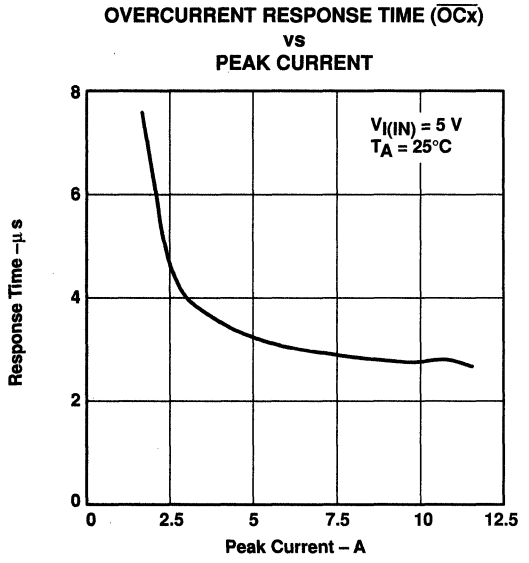


Figure 28

APPLICATION INFORMATION

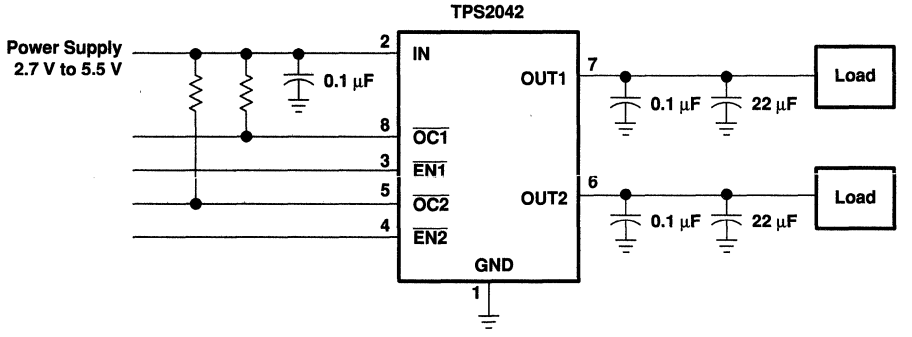


Figure 29. Typical Application

power-supply considerations

A 0.01-µF to 0.1-µF ceramic bypass capacitor between INx and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-µF to 0.1-µF ceramic capacitor improves the immunity of the device to short-circuit transients.

APPLICATION INFORMATION

overcurrent

A sense FET checks for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 6). The TPS2042 and TPS2052 sense the short and immediately switch into a constant-current output.

In the second condition, the short occurs while the device is enabled. At the instant the short occurs, very high currents may flow for a short time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshhold) the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figure 7). The TPS2042 and TPS2052 are capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

$\overline{OC}$ response

The $\overline{OC}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false overcurrent reporting from the inrush current flowing through the device, charging the downstream capacitor. An RC filter of 500 µs (see Figure 30) can be connected to the $\overline{OC}$ pin to reduce false overcurrent reporting. Using low-ESR electrolytic capacitors on the output lowers the inrush current flow through the device during hot-plug events by providing a low impedance energy source, thereby reducing erroneous overcurrent reporting.

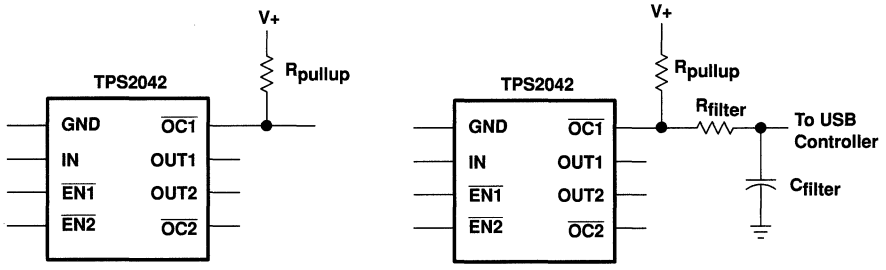


Figure 30. Typical Circuit for $\overline{OC}$ Pin and RC Filter for Damping Inrush $\overline{OC}$ Responses

APPLICATION INFORMATION

power dissipation and junction temperature

The low on-resistance on the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistances of these packages are high compared to that of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find $r_{DS(on)}$ at the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figure 21. Next, calculate the power dissipation using:

$$P_D = r_{DS(on)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient Temperature °C
$R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W, PDIP = 106°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

thermal protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS2042 and TPS2052 into constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels. The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

The TPS2042 and TPS2052 implement a dual thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition the junction temperature will rise. Once the die temperature rises to approximately 140°C, the internal thermal sense circuitry checks which power switch is in an overcurrent condition and turns that power switch off, thus isolating the fault without interrupting operation of the adjacent power switch. Should the die temperature exceed the first thermal trip point of 140°C and reach 160°C, both switches turn off. The $\overline{OC}$ open-drain output is asserted (active low) when overtemperature or overcurrent occurs.

undervoltage lockout (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch will be quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO will also keep the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. Upon reinsertion, the power switch will be turned on with a controlled rise time to reduce EMI and voltage overshoots.

APPLICATION INFORMATION

universal serial bus (USB) applications

The universal serial bus (USB) interface is a 12-Mb/s, or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

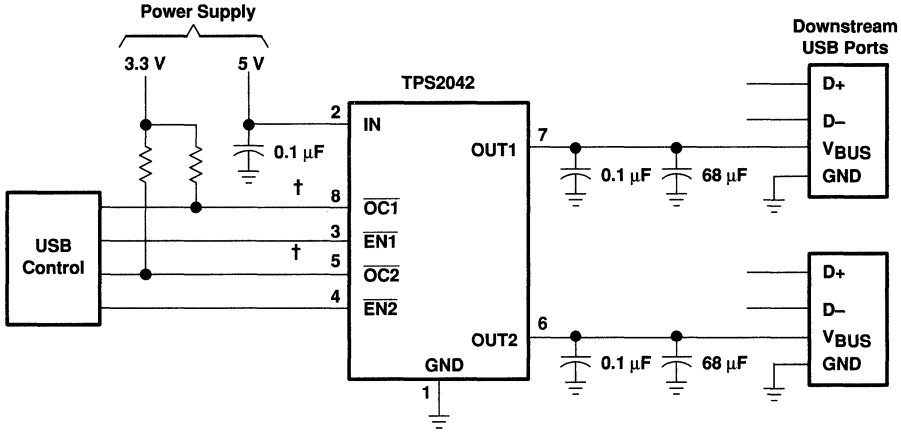
The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

Self-powered and bus-powered hubs distribute data and power to downstream functions. The TPS2042 and TPS2052 can provide power-distribution solutions for many of these classes of devices.

host/self-powered and bus-powered hubs

Hosts and self-powered hubs have a local power supply that powers the embedded functions and the downstream ports (see Figure 31). This power supply must provide from 5.25 V to 4.75 V to the board side of the downstream connection under full-load and no-load conditions. Hosts and SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.



† May need RC filter (see Figure 36)

Figure 31. Typical Two-Port USB Host/Self-Powered Hub

APPLICATION INFORMATION

host/self-powered and bus-powered hubs (continued)

Bus-powered hubs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

low-power bus-powered functions and high-power bus-powered functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA, and high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 μF at power up, the device must implement inrush current limiting (see Figure 32).

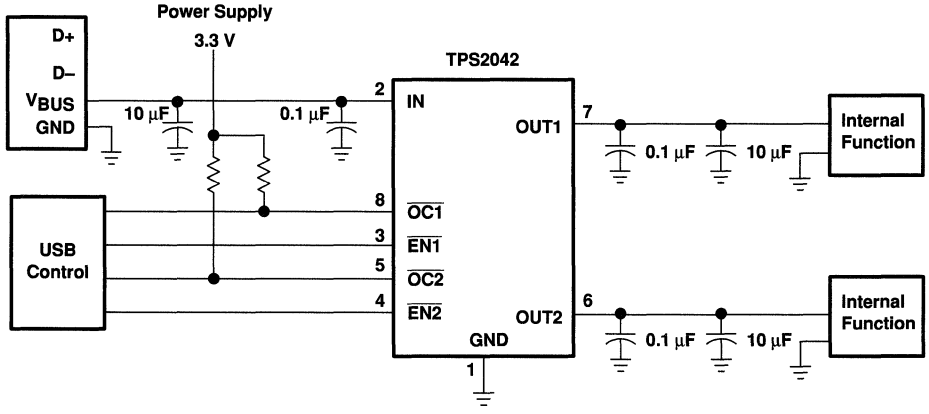


Figure 32. High-Power Bus-Powered Function

APPLICATION INFORMATION

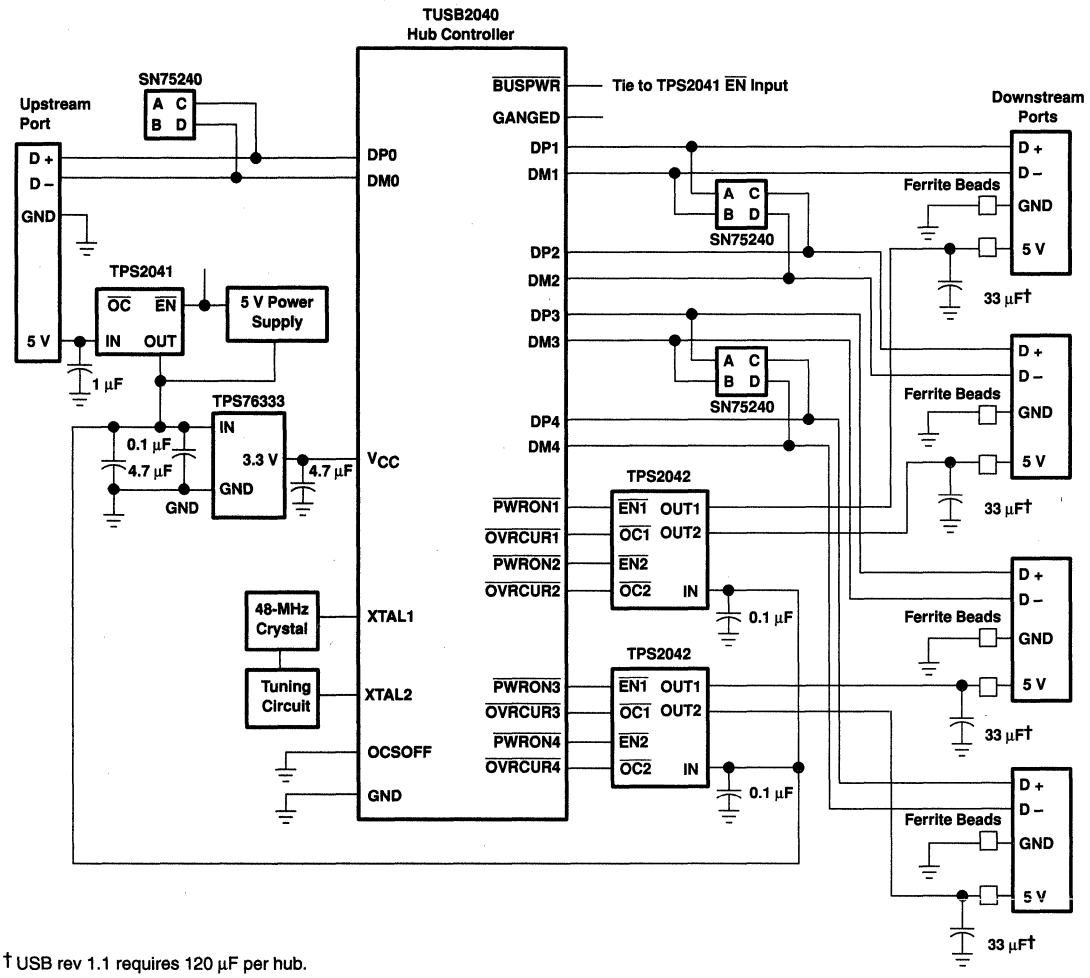
USB power-distribution requirements

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power-distribution features must be implemented.

- Hosts/self-powered hubs must:
  - Current-limit downstream ports
  - Report overcurrent conditions on USB V_{BUS}
- Bus-powered hubs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 μF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

The feature set of the TPS2042 and TPS2052 allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-power hubs, as well as the input ports for bus-power functions (see Figure 33).

APPLICATION INFORMATION



† USB rev 1.1 requires 120 µF per hub.

Figure 33. Hybrid Self/Bus-Powered Hub Implementation

APPLICATION INFORMATION

generic hot-plug applications (see Figure 34)

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS2042 and TPS2052, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS2042 and TPS2052 also ensures the switch will be off after the card has been removed, and the switch will be off during the next insertion. The UVLO feature guarantees a soft start with a controlled rise time for every insertion of the card or module.

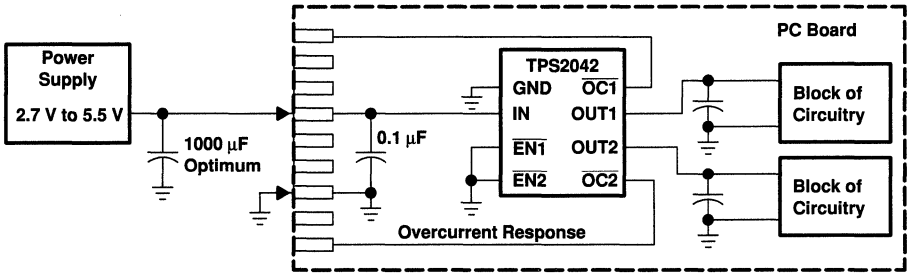


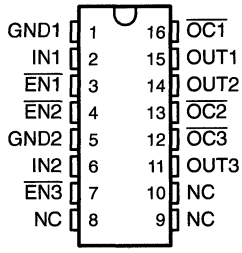
Figure 34. Typical Hot-Plug Implementation

By placing the TPS2042 and TPS2052 between the V_{CC} input and the rest of the circuitry, the input power will reach these devices first after insertion. The typical rise time of the switch is approximately 2.5 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

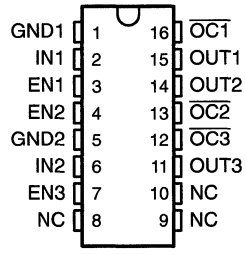
SLVS191 – JANUARY 1999

- 135-mΩ -Maximum (5-V Input) High-Side MOSFET Switch
- 500 mA Continuous Current per Channel
- Short-Circuit and Thermal Protection With Overcurrent Logic Output
- Operating Range . . . 2.7 V to 5.5 V
- Logic-Level Enable Input
- 2.5-ms Typical Rise Time
- Undervoltage Lockout
- 20 μA Maximum Standby Supply Current
- Bidirectional Switch
- Available in 16-pin SOIC Package
- Ambient Temperature Range, –40°C to 85°C
- 2-kV Human-Body-Model, 200-V Machine-Model ESD Protection
- UL Listed – File No. E169910

TPS2043
D PACKAGE
(TOP VIEW)



TPS2053
D PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TPS2043 and TPS2053 triple power distribution switches are intended for applications where heavy capacitive loads and short circuits are likely to be encountered. The TPS2043 and the TPS2053 incorporate in single packages three 135-mΩ N-channel MOSFET high-side power switches for power-distribution systems that require multiple power switches. Each switch is controlled by a logic enable that is compatible with 5-V logic and 3-V logic. Gate drive is provided by an internal charge pump that controls the power-switch rise times and fall times to minimize current surges during switching. The charge pump, requiring no external components, allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the TPS2043 and TPS2053 limit the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{OCx}$) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until valid input voltage is present.

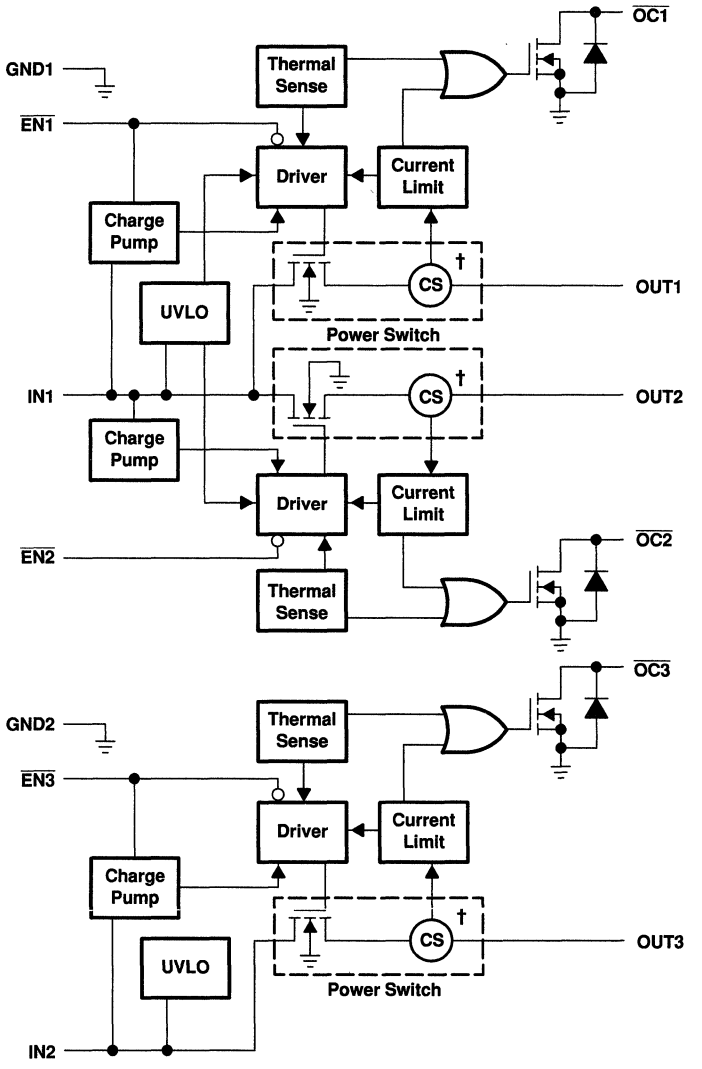
The TPS2043 and TPS2053 are designed to limit at 0.9-A load. These power distribution switches are available in a 16-pin small-outline integrated circuit (SOIC) package and operate over an ambient temperature range of –40°C to 85°C.

AVAILABLE OPTIONS

T_A	ENABLE	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A)	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (A)	PACKAGED DEVICES
				SOIC (D)†
–40°C to 85°C	Active low	0.5	0.9	TPS2043D
–40°C to 85°C	Active high	0.5	0.9	TPS2053D

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2043DR)

TPS2043 functional block diagram



† Current sense

Terminal Functions

TERMINAL NAME	TERMINAL NO. TPS2043	TERMINAL NO. TPS2053	I/O	DESCRIPTION
$\overline{EN1}$	3	–	I	Enable input, logic low turns on power switch, IN1-OUT1.
$\overline{EN2}$	4	–	I	Enable input, logic low turns on power switch, IN1-OUT2.
$\overline{EN3}$	7	–	I	Enable input, logic low turns on power switch, IN2-OUT3.
EN1	–	3	I	Enable input, logic high turns on power switch, IN1-OUT1.
EN2	–	4	I	Enable input, logic high turns on power switch, IN1-OUT2.
EN3	–	7	I	Enable input, logic high turns on power switch, IN2-OUT3.
GND1	1	1		Ground
GND2	5	5		Ground
IN1	2	2	I	Input voltage
IN2	6	6	I	Input voltage
$\overline{NC}$	8, 9, 10	8, 9, 10		No connection
$\overline{OC1}$	16	16	O	Overcurrent, logic output active low, IN1-OUT1
$\overline{OC2}$	13	13	O	Overcurrent, logic output active low, IN1-OUT2
$\overline{OC3}$	12	12	O	Overcurrent, logic output active low, IN2-OUT3
OUT1	15	15	O	Power-switch output, IN1-OUT1
OUT2	14	14	O	Power-switch output, IN1-OUT2
OUT3	11	11	O	Power-switch output, IN2-OUT3

detailed description

power switch

The power switch is an N-channel MOSFET with a maximum on-state resistance of 135 mΩ ($V_{I(INx)}$ = 5 V). Configured as a high-side switch, the power switch prevents current flow from OUTx to INx and INx to OUTx when disabled. The power switch supplies a minimum of 500 mA per switch.

charge pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 4-ms range.

enable ($\overline{\text{ENx}}$ or ENx)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 20 μA when a logic high is present on $\overline{\text{ENx}}$ (TPS2043) or a logic low is present on ENx (TPS2053). A logic zero input on $\overline{\text{ENx}}$ or logic high on ENx restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

overcurrent ($\overline{\text{OCx}}$)

The $\overline{\text{OCx}}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed.

current sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant current mode and holds the current constant while varying the voltage on the load.

thermal sense

The TPS2043 and TPS2053 implement a dual-threshold thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition the junction temperature rises. When the die temperature rises to approximately 140°C, the internal thermal sense circuitry checks to determine which power switch is in an overcurrent condition and turns off that switch, thus isolating the fault without interrupting operation of the adjacent power switch. Hysteresis is built into the thermal sense, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed. The ($\overline{\text{OCx}}$) open-drain output is asserted (active low) when overtemperature or overcurrent occurs.

undervoltage lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, $V_{I(INx)}$ (see Note1) ..... –0.3 V to 6 V
Output voltage range, $V_{O(OUTx)}$ (see Note1) ..... –0.3 V to $V_{I(INx)}$ + 0.3 V
Input voltage range, $V_{I(\overline{ENx})}$ or $V_{I(ENx)}$ ..... –0.3 V to 6 V
Continuous output current, $I_{O(OUTx)}$ ..... Internally limited
Continuous total power dissipation ..... See Dissipation Rating Table
Operating virtual junction temperature range, T_J ..... –40°C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C
Electrostatic discharge (ESD) protection: Human body model MIL-STD-883C ..... 2 kV
Machine model ..... 0.2 kV

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW

recommended operating conditions

	TPS2043		TPS2053		UNIT
	MIN	MAX	MIN	MAX	
Input voltage, $V_{I(INx)}$	2.7	5.5	2.7	5.5	V
Input voltage, $V_{I(\overline{ENx})}$ or $V_{I(ENx)}$	0	5.5	0	5.5	V
Continuous output current, $I_{O(OUTx)}$	0	500	0	500	mA
Operating virtual junction temperature, T_J	–40	125	–40	125	°C

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $V_{I(\overline{ENx})}$ = 0 V, $V_{I(ENx)}$ = Hi (unless otherwise noted)

power switch

PARAMETER		TEST CONDITIONS†	TPS2043			TPS2053			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$r_{DS(on)}$	Static drain-source on-state resistance, 5-V operation	$V_{I(INx)}$ = 5 V, T_J = 25°C, I_O = 0.5 A		80	95		80	95	mΩ
		$V_{I(INx)}$ = 5 V, T_J = 85°C, I_O = 0.5 A		90	120		90	120	
		$V_{I(INx)}$ = 5 V, T_J = 125°C, I_O = 0.5 A		100	135		100	135	
	Static drain-source on-state resistance, 3.3-V operation	$V_{I(INx)}$ = 3.3 V, T_J = 25°C, I_O = 0.5 A		85	105		85	105	
		$V_{I(INx)}$ = 3.3 V, T_J = 85°C, I_O = 0.5 A		100	135		100	135	
		$V_{I(INx)}$ = 3.3 V, T_J = 125°C, I_O = 0.5 A		115	150		115	150	
t_r	Rise time, output	$V_{I(INx)}$ = 5.5 V, T_J = 25°C, C_L = 1 µF, R_L = 10 Ω		2.5			2.5		ms
		$V_{I(INx)}$ = 2.7 V, T_J = 25°C, C_L = 1 µF, R_L = 10 Ω		3			3		
t_f	Fall time, output	$V_{I(INx)}$ = 5.5 V, T_J = 25°C, C_L = 1 µF, R_L = 10 Ω		4.4			4.4		ms
		$V_{I(INx)}$ = 2.7 V, T_J = 25°C, C_L = 1 µF, R_L = 10 Ω		2.5			2.5		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

enable input $\overline{ENx}$ or ENx

PARAMETER			TEST CONDITIONS	TPS2043			TPS2053			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High-level input voltage		2.7 V ≤ $V_{I(INx)}$ ≤ 5.5 V	2			2			V
V_{IL}	Low-level input voltage		4.5 V ≤ $V_{I(INx)}$ ≤ 5.5 V			0.8			0.8	V
			2.7 V≤ $V_{I(INx)}$ ≤ 4.5 V			0.4			0.4	
I_I	Input current	TPS2043	$V_{I(\overline{ENx})}$ = 0 V or $V_{I(\overline{ENx})}$ = $V_{I(IN)}$	–0.5		0.5				µA
		TPS2053	$V_{I(ENx)}$ = $V_{I(INx)}$ or $V_{I(ENx)}$ = 0 V				–0.5		0.5	
t_{on}	Turnon time		C_L = 100 µF, R_L=10 Ω			20			20	ms
t_{off}	Turnoff time		C_L = 100 µF, R_L=10 Ω			40			40	

current limit

PARAMETER		TEST CONDITIONS†	TPS2043			TPS2053			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{OS}	Short-circuit output current	$V_{I(INx)}$ = 5 V, OUT connected to GND, Device enable into short circuit	0.7	0.9	1.1	0.7	0.9	1.1	A

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $V_{I(\overline{ENx})}$ = 0 V, $V_{I(ENx)}$ = Hi (unless otherwise noted) (continued)

supply current

PARAMETER	TEST CONDITIONS				TPS2043			TPS2053			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
Supply current, low-level output	No Load on OUTx	$V_{I(\overline{ENx})} = V_{I(INx)}$	T_J = 25°C	TPS2043		0.03	2				µA
			–40°C ≤ T_J ≤ 125°C				20				
		$V_{I(ENx)}$ = 0 V	T_J = 25°C	TPS2053					0.03	2	
			–40°C ≤ T_J ≤ 125°C							20	
Supply current, high-level output	No Load on OUTx	$V_{I(\overline{ENx})}$ = 0 V	T_J = 25°C	TPS2043		160	200				µA
			–40°C ≤ T_J ≤ 125°C			200					
		$V_{I(ENx)} = V_{I(INx)}$	T_J = 25°C	TPS2053					160	200	
			–40°C ≤ T_J ≤ 125°C						200		
Leakage current	OUTx connected to ground	$V_{I(\overline{ENx})} = V_{I(INx)}$	–40°C ≤ T_J ≤ 125°C	TPS2043		200					µA
		$V_{I(ENx)}$ = 0 V	–40°C ≤ T_J ≤ 125°C	TPS2053					200		
Reverse leakage current	IN = high impedance	$V_{I(\overline{ENx})}$ = 0 V	T_J = 25°C	TPS2043		0.3					µA
		$V_{I(ENx)}$ = Hi		TPS2053					0.3		

undervoltage lockout

PARAMETER	TEST CONDITIONS	TPS2043			TPS2053			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Low-level input voltage		2		2.5	2		2.5	V
Hysteresis	T_J = 25°C		100			100		mV

overcurrent $\overline{OCx}$

PARAMETER	TEST CONDITIONS	TPS2043			TPS2053			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Sink current†	V_O = 5 V			10			10	mA
Output low voltage	I_O = 5 mA, $V_{OL(\overline{OCx})}$			0.5			0.5	V
Off-state current†	V_O = 5 V, V_O = 3.3 V			1			1	µA

† Specified by design, not production tested.

PARAMETER MEASUREMENT INFORMATION

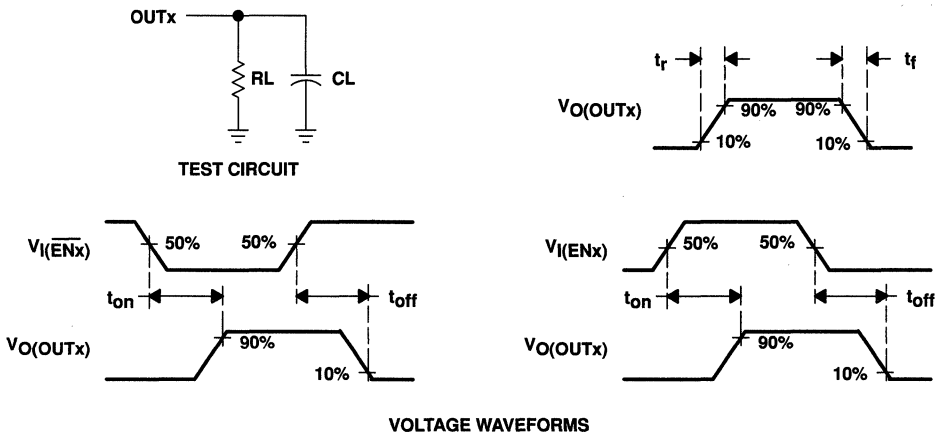


Figure 1. Test Circuit and Voltage Waveforms

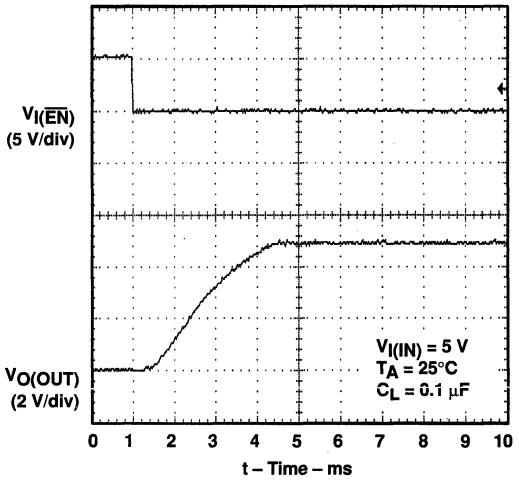


Figure 2. Turnon Delay and Rise Time with 0.1-µF Load

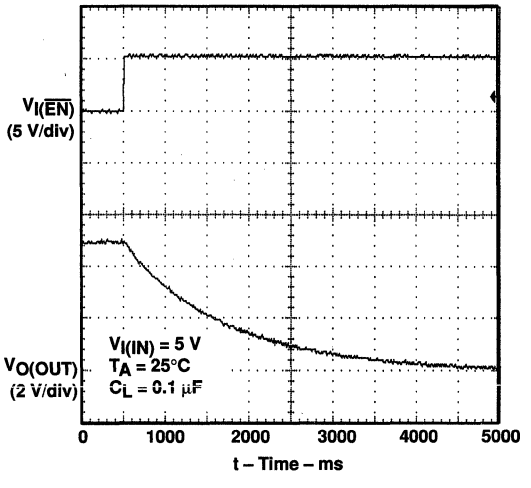


Figure 3. Turnoff Delay and Fall Time with 0.1-µF Load

PARAMETER MEASUREMENT INFORMATION

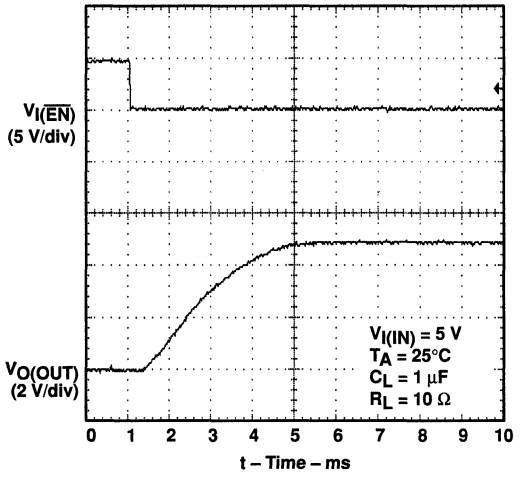


Figure 4. Turnon Delay and Rise Time with 1-μF Load

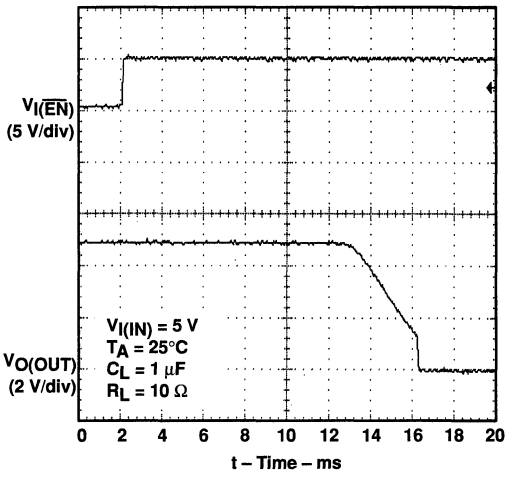


Figure 5. Turnoff Delay and Fall Time with 1-μF Load

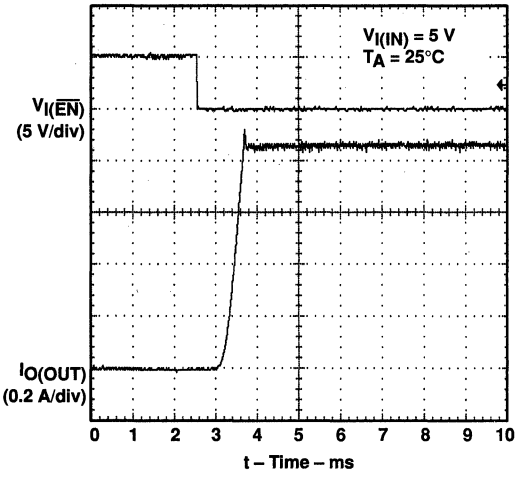


Figure 6. TPS2043, Short-Circuit Current, Device Enabled into Short

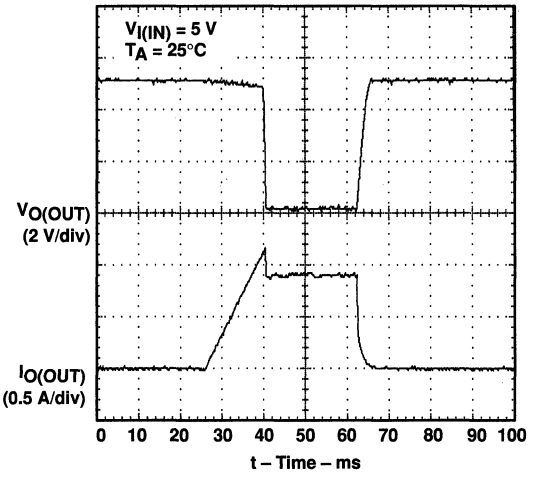


Figure 7. TPS2043, Threshold Trip Current with Ramped Load on Enabled Device

PARAMETER MEASUREMENT INFORMATION

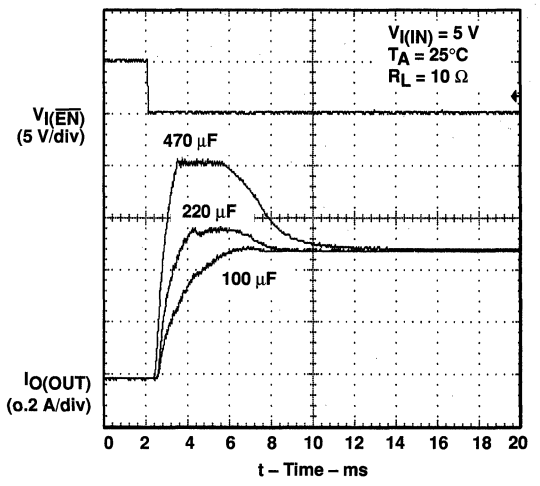


Figure 8. Inrush Current with 100-µF, 220-µF and 470-µF Load Capacitance

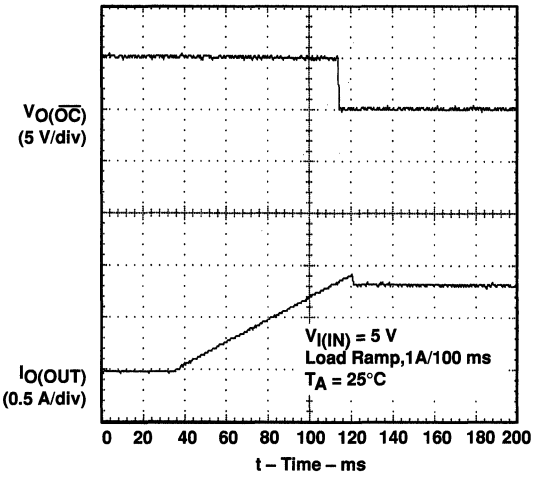


Figure 9. Ramped Load on Enabled Device

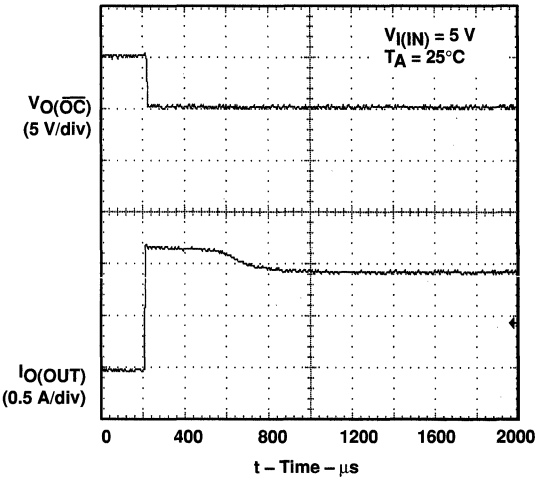


Figure 10. 4-Ω Load Connected to Enabled Device

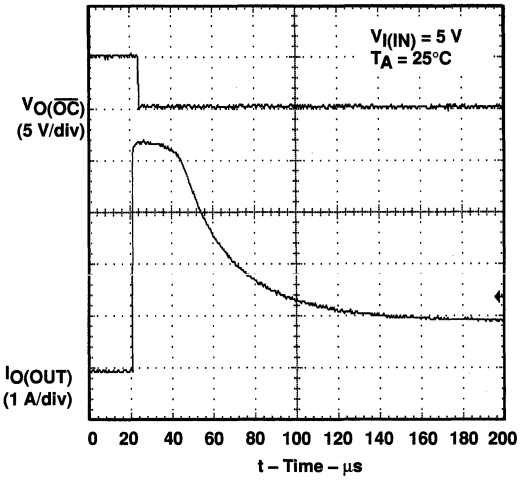


Figure 11. 1-Ω Load Connected to Enabled Device

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TYPICAL CHARACTERISTICS

TURNON DELAY vs INPUT VOLTAGE

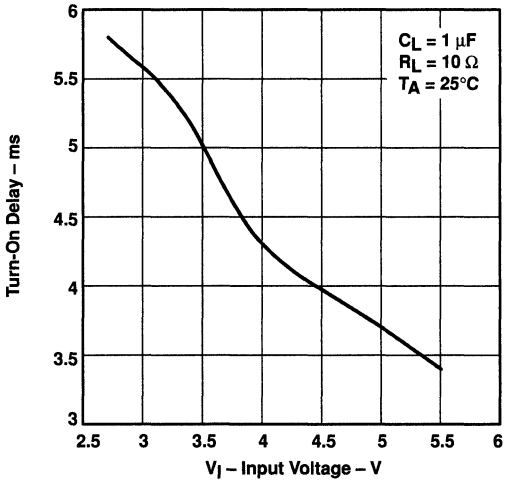


Figure 12

TURNOFF DELAY vs INPUT VOLTAGE

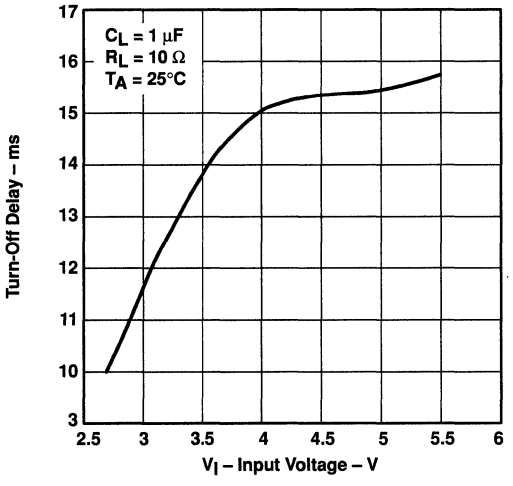


Figure 13

RISE TIME vs LOAD CURRENT

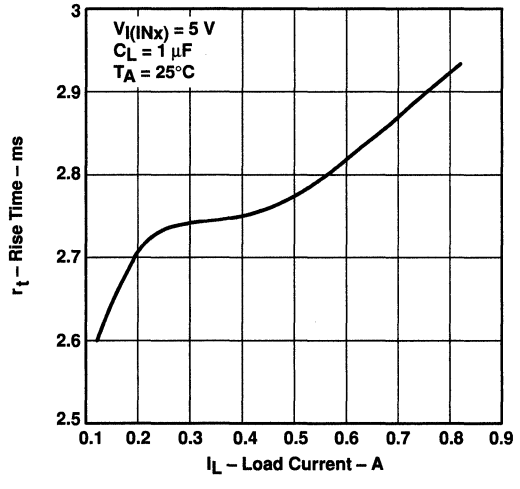


Figure 14

FALL TIME vs LOAD CURRENT

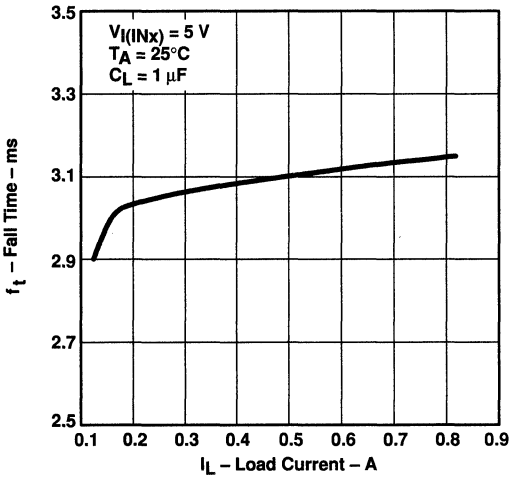


Figure 15

TYPICAL CHARACTERISTICS

SUPPLY CURRENT, OUTPUT ENABLED
vs
JUNCTION TEMPERATURE

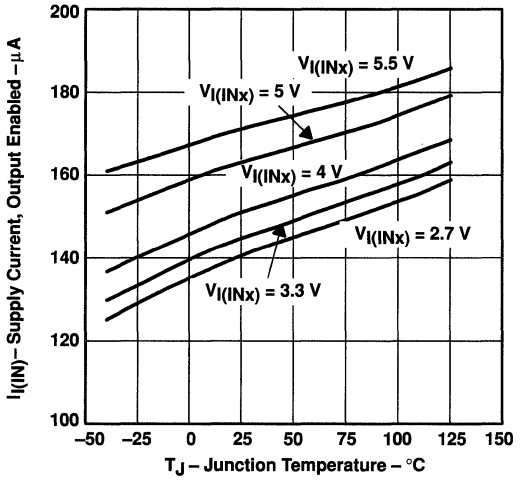


Figure 16

SUPPLY CURRENT, OUTPUT DISABLED
vs
JUNCTION TEMPERATURE

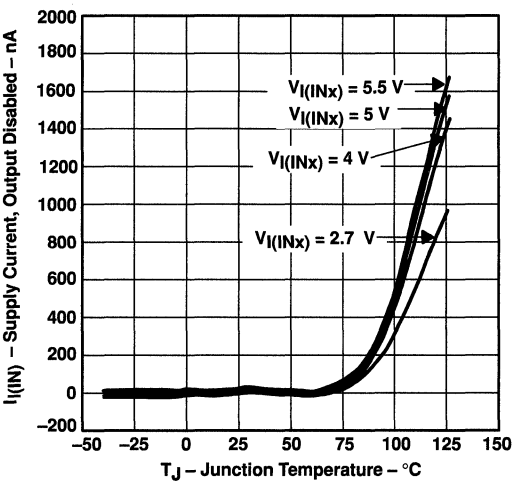


Figure 17

SUPPLY CURRENT, OUTPUT ENABLED
vs
INPUT VOLTAGE

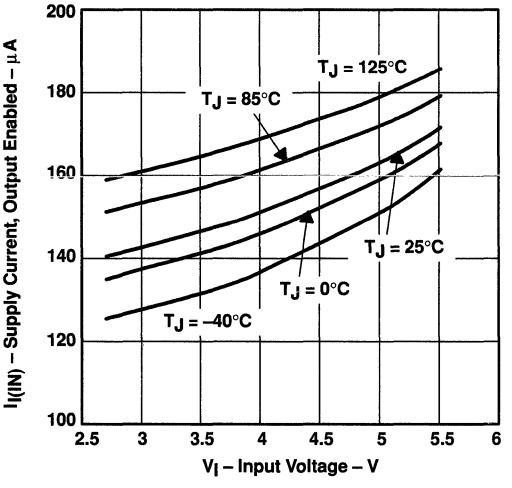


Figure 18

SUPPLY CURRENT, OUTPUT DISABLED
vs
INPUT VOLTAGE

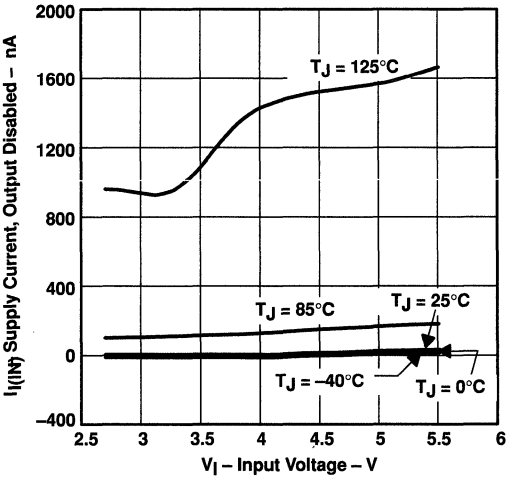


Figure 19

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

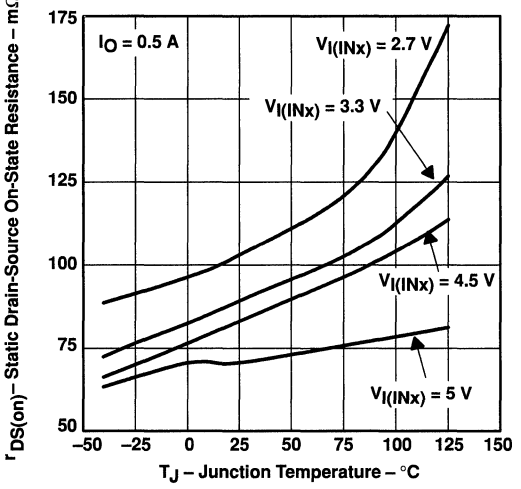


Figure 20

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
INPUT VOLTAGE

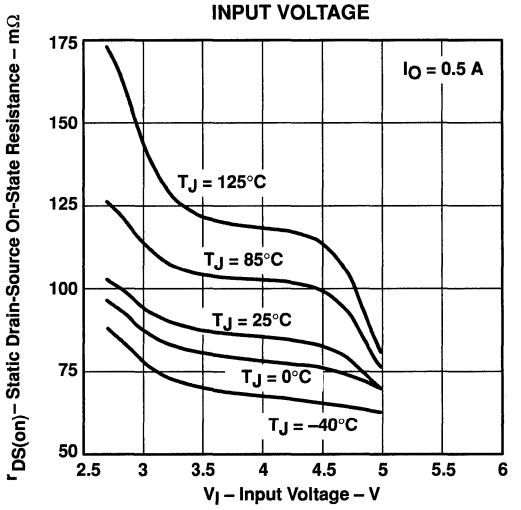


Figure 21

INPUT-TO-OUTPUT VOLTAGE
vs
LOAD CURRENT

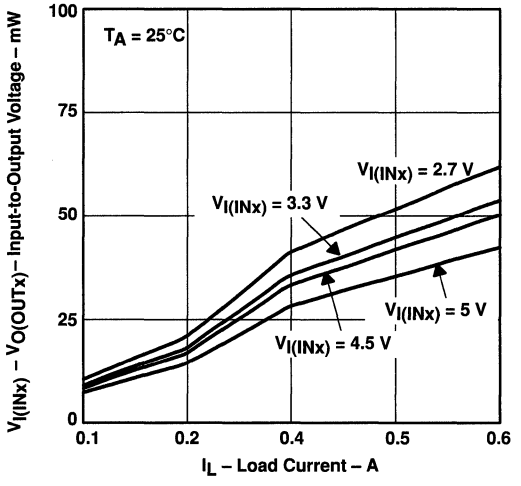


Figure 22

SHORT-CURCUIT OUTPUT CURRENT
vs
INPUT VOLTAGE

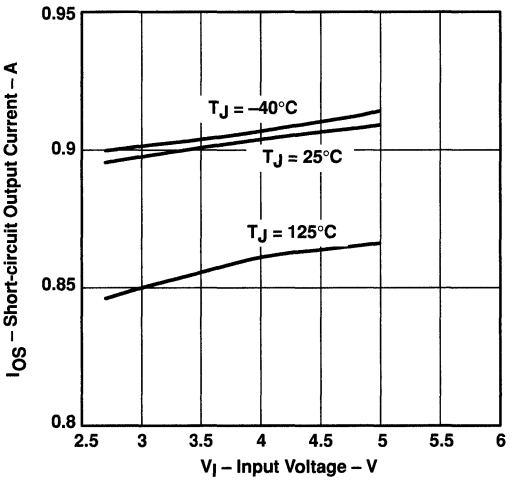


Figure 23

TYPICAL CHARACTERISTICS

THRESHOLD TRIP CURRENT
vs
INPUT VOLTAGE

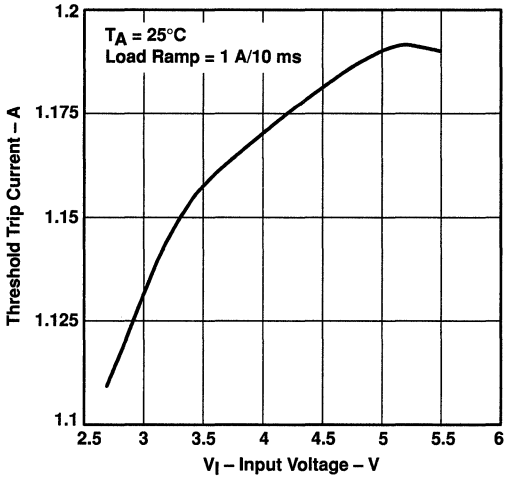


Figure 24

SHORT CIRCUIT OUTPUT CURRENT
vs
JUNCTION TEMPERATURE

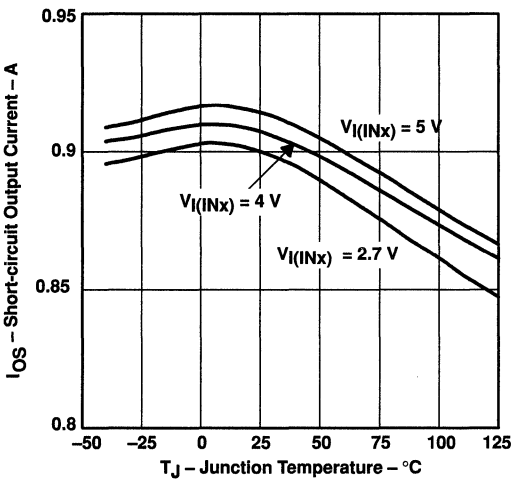


Figure 25

UNDERVOLTAGE LOCKOUT
vs
JUNCTION TEMPERATURE

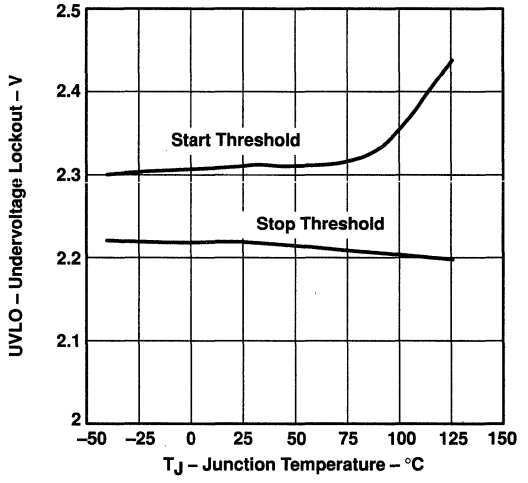


Figure 26

CURRENT-LIMIT RESPONSE
vs
PEAK CURRENT

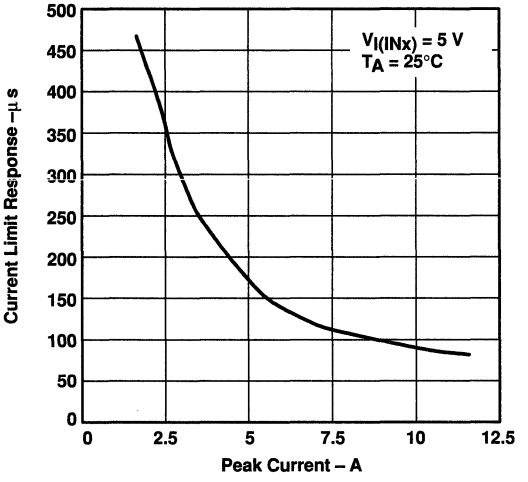


Figure 27

TYPICAL CHARACTERISTICS

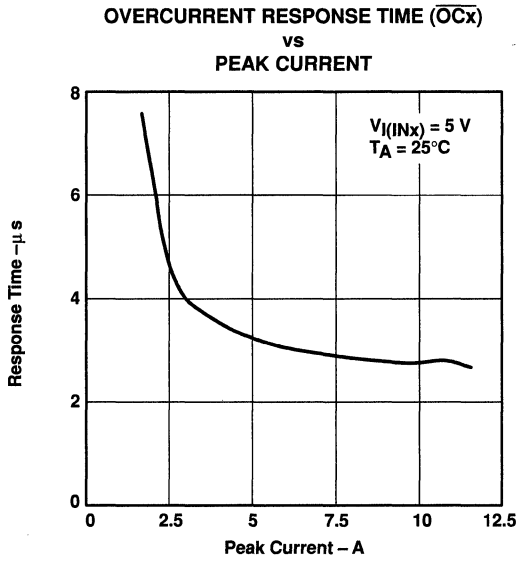


Figure 28

APPLICATION INFORMATION

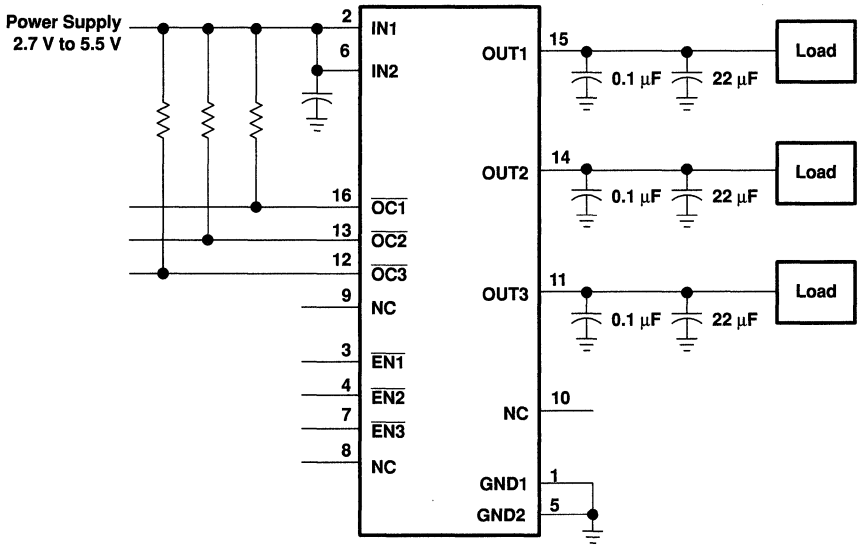


Figure 29. Typical Application

APPLICATION INFORMATION

power-supply considerations

A 0.01-μF to 0.1-μF ceramic bypass capacitor between INx and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-μF to 0.1-μF ceramic capacitor improves the immunity of the device to short-circuit transients.

overcurrent

A sense FET checks for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(INx)}$ has been applied (see Figure 6). The TPS2043 and TPS2053 sense the short and immediately switch into a constant-current output.

In the second condition, the excessive load occurs while the device is enabled. At the instant the excessive load occurs, very high currents may flow for a short time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshhold) the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figure 7). The TPS2043 and TPS2053 are capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

$\overline{OC}$ response

The $\overline{OC}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false overcurrent reporting from the inrush current flowing through the device, charging the downstream capacitor. An RC filter of 500 μs (see Figure 30) can be connected to the $\overline{OC}$ pin to reduce false overcurrent reporting. Using low-ESR electrolytic capacitors on the output lowers the inrush current flow through the device during hot-plug events by providing a low impedance energy source, thereby reducing erroneous overcurrent reporting.

APPLICATION INFORMATION

$\overline{OC}$ response (continued)

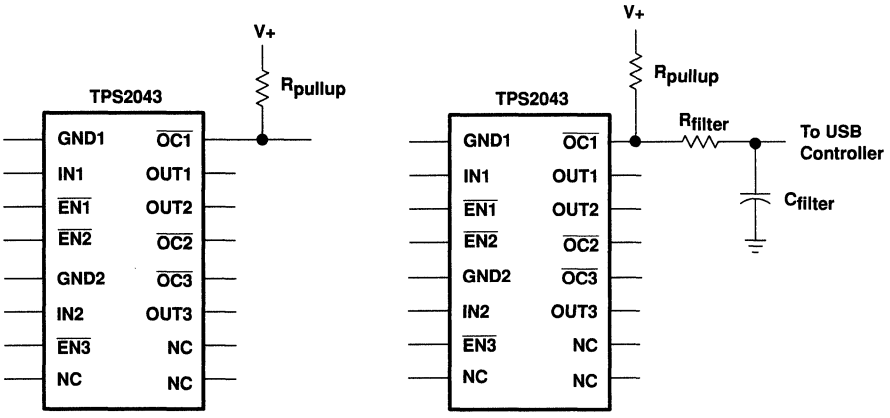


Figure 30. Typical Circuit for $\overline{OC}$ Pin and RC Filter for Damping Inrush $\overline{OC}$ Responses

power dissipation and junction temperature

The low on-resistance on the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find $r_{DS(on)}$ at the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figure 21. Next, calculate the power dissipation using:

$$P_D = r_{DS(on)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient Temperature °C
$R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get an acceptable answer.

APPLICATION INFORMATION

thermal protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS2043 and TPS2053 into constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels. The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

The TPS2043 and TPS2053 implement a dual thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition the junction temperature will rise. Once the die temperature rises to approximately 140°C, the internal thermal sense circuitry checks which power switch is in an overcurrent condition and turns that power switch off, thus isolating the fault without interrupting operation of the adjacent power switch. Should the die temperature exceed the first thermal trip point of 140°C and reach 160°C, both switches turn off. The $\overline{OC}$ open-drain output is asserted (active low) when overtemperature or overcurrent occurs.

undervoltage lockout (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch will be quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO will also keep the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. Upon reinsertion, the power switch will be turned on with a controlled rise time to reduce EMI and voltage overshoots.

universal serial bus (USB) applications

The universal serial bus (USB) interface is a 12-Mb/s, or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

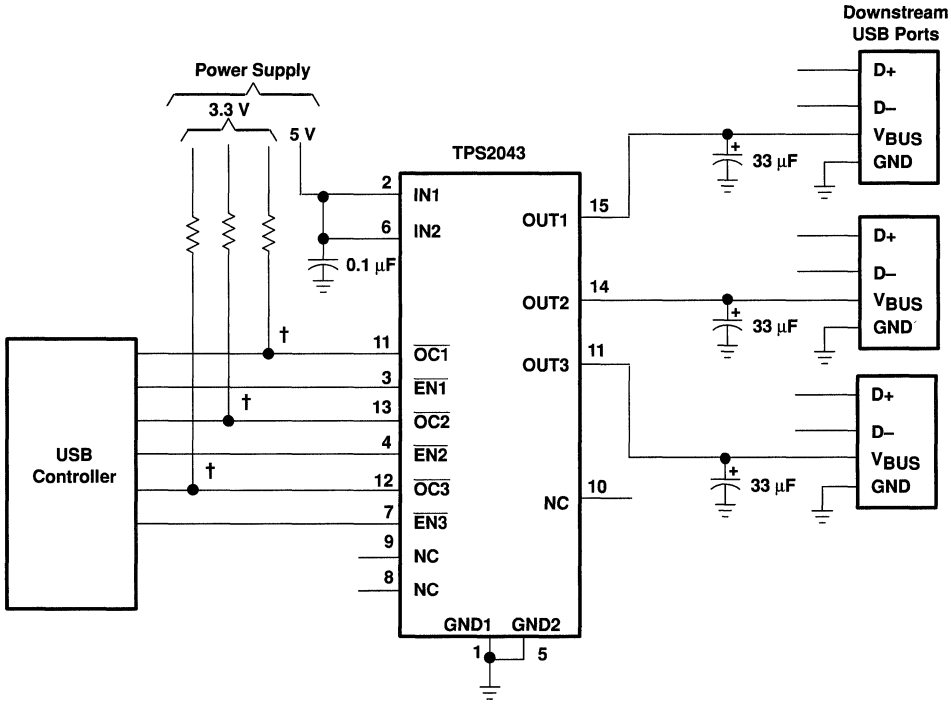
- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

Self-powered and bus-powered hubs distribute data and power to downstream functions. The TPS2043 and TPS2053 can provide power-distribution solutions for many of these classes of devices.

APPLICATION INFORMATION

host/self-powered and bus-powered hubs

Hosts and self-powered hubs have a local power supply that powers the embedded functions and the downstream ports (see Figure 31). This power supply must provide from 5.25 V to 4.75 V to the board side of the downstream connection under full-load and no-load conditions. Hosts and SPHs must have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.



† An RC filter may be needed, see Figure 36

Figure 31. Typical Three-Port USB Host/Self-Powered Hub

Bus-powered hubs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

APPLICATION INFORMATION

low-power bus-powered functions and high-power bus-powered functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA, and high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 µF at power up, the device must implement inrush current limiting (see Figure 32).

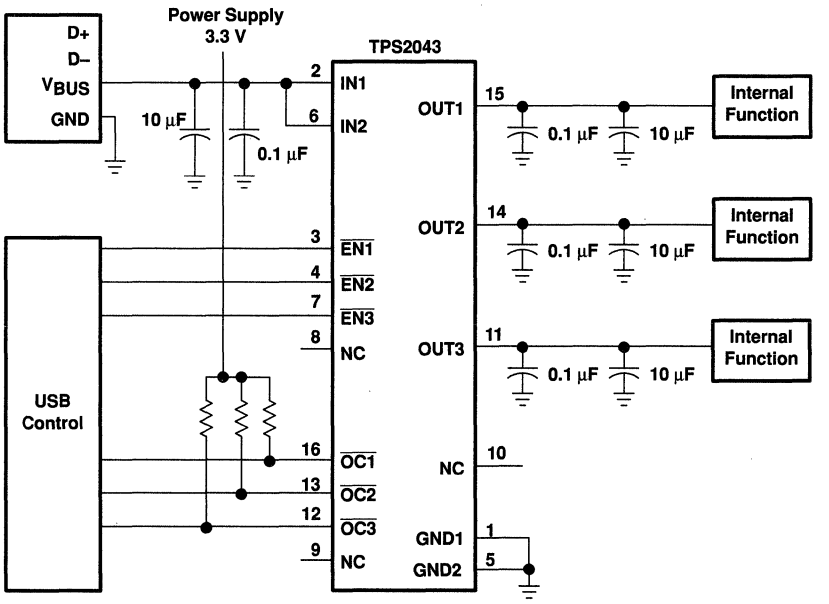


Figure 32. High-Power Bus-Powered Function

APPLICATION INFORMATION

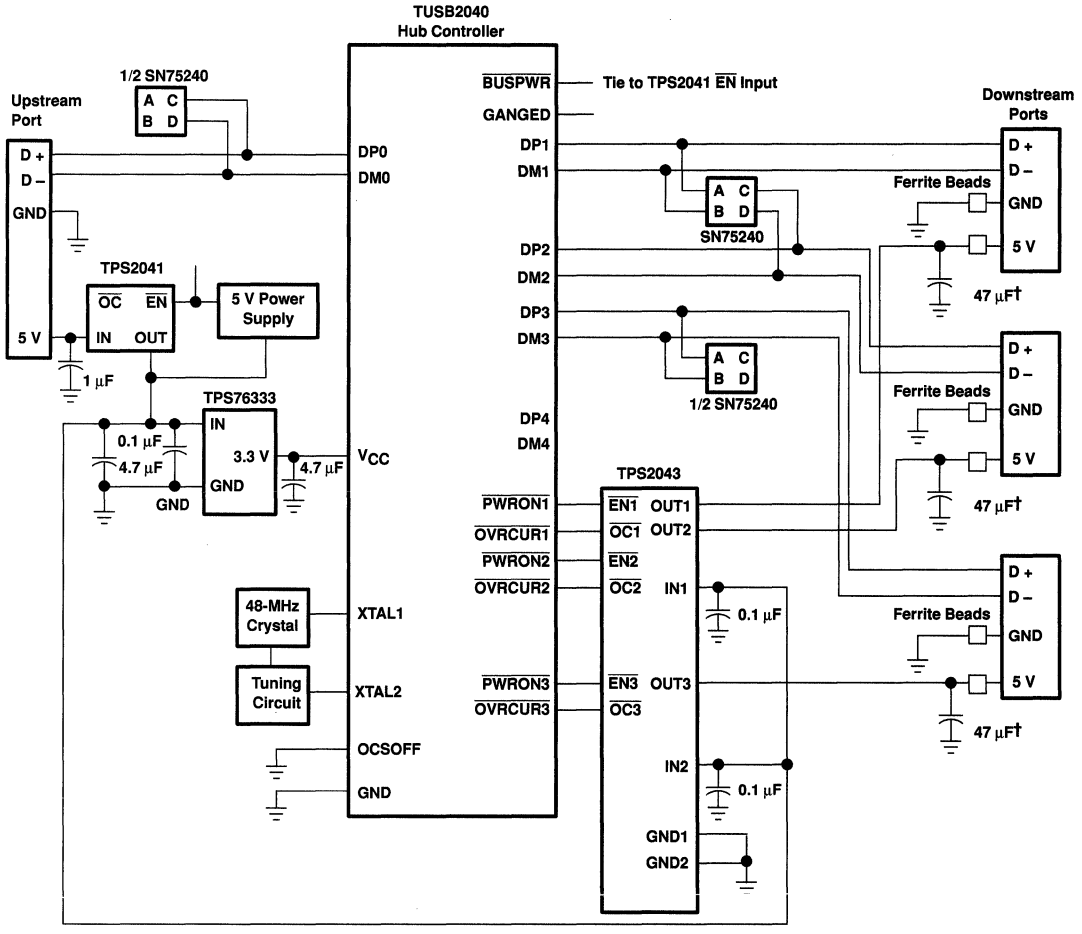
USB power-distribution requirements

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power distribution features must be implemented.

- Hosts/self-powered hubs must:
  - Current-limit downstream ports
  - Report overcurrent conditions on USB V_{BUS}
- Bus-powered hubs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 μF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

The feature set of the TPS2043 and TPS2053 allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-power hubs, as well as the input ports for bus-power functions (see Figure 39).

APPLICATION INFORMATION



† USB rev 1.1 requires 120 µF per hub.

Figure 33. Hybrid Self/Bus-Powered Hub Implementation

APPLICATION INFORMATION

generic hot-plug applications (see Figure 34)

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS2043 and TPS2053, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS2043 and TPS2053 also ensures the switch will be off after the card has been removed, and the switch will be off during the next insertion. The UVLO feature guarantees a soft start with a controlled rise time for every insertion of the card or module.

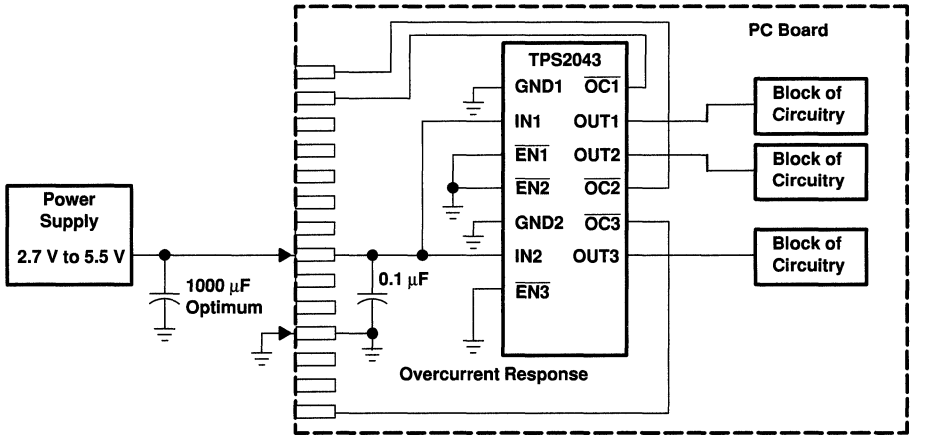


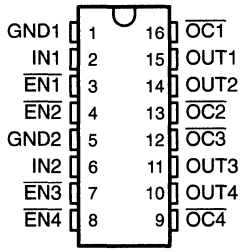
Figure 34. Typical Hot-Plug Implementation

By placing the TPS2043 and TPS2053 between the V_{CC} input and the rest of the circuitry, the input power will reach these devices first after insertion. The typical rise time of the switch is approximately 2.5 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

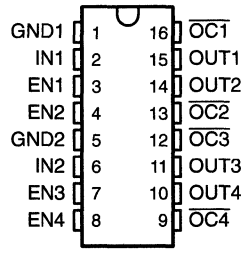
SLVS174B – JULY 1998 – REVISED FEBRUARY 1999

- **135-mΩ -Maximum (5-V Input) High-Side MOSFET Switch**
- **500 mA Continuous Current per Channel**
- **Short-Circuit and Thermal Protection With Overcurrent Logic Output**
- **Operating Range . . . 2.7-V to 5.5-V**
- **Logic-Level Enable Input**
- **2.5-ms Typical Rise Time**
- **Undervoltage Lockout**
- **20-μA-Maximum Standby Supply Current**
- **Bidirectional Switch**
- **16-pin SOIC Package**
- **Ambient Temperature Range, –40°C to 85°C**
- **2-kV Human-Body-Model, 200-V Machine-Model ESD Protection**
- **UL Listed – File No. E169910**

TPS2044
D PACKAGE
(TOP VIEW)



TPS2054
D PACKAGE
(TOP VIEW)



description

The TPS2044 and TPS2054 quad power-distribution switches are intended for applications where heavy capacitive loads and short circuits are likely to be encountered. The TPS2044 and the TPS2054 incorporate in single packages four 135-mΩ N-channel MOSFET high-side power switches for power-distribution systems that require multiple power switches. Each switch is controlled by a logic enable that is compatible with 5-V logic and 3-V logic. Gate drive is provided by an internal charge pump that controls the power-switch rise times and fall times to minimize current surges during switching. The charge pump, requiring no external components, allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the TPS2044 and TPS2054 limit the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{OCx}$) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until valid input voltage is present.

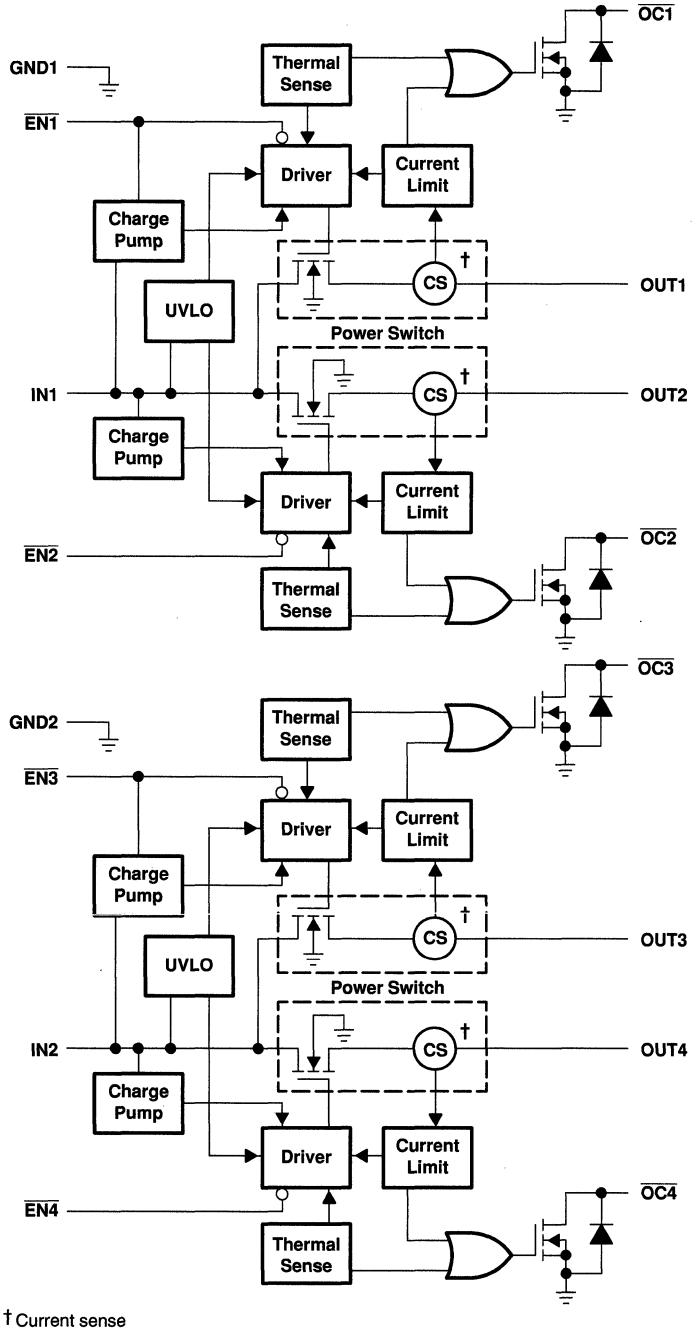
The TPS2044 and TPS2054 are designed to limit at 0.9-A load. These power-distribution switches are available in 16-pin small-outline integrated-circuit (SOIC) packages and operate over an ambient temperature range of –40°C to 85°C.

AVAILABLE OPTIONS

T_A	ENABLE	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A)	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (A)	PACKAGED DEVICES
				SOIC (D)†
–40°C to 85°C	Active low	0.5	0.9	TPS2044D
–40°C to 85°C	Active high	0.5	0.9	TPS2054D

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2044DR)

TPS2044 functional block diagram



† Current sense

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	TPS2044	TPS2054		
$\overline{EN1}$	3	–	I	Enable input. logic low turns on power switch, IN1-OUT1.
$\overline{EN2}$	4	–	I	Enable input. Logic low turns on power switch, IN1-OUT2.
$\overline{EN3}$	7	–	I	Enable input. Logic low turns on power switch, IN2-OUT3.
$\overline{EN4}$	8	–	I	Enable input. Logic low turns on power switch, IN2-OUT4.
EN1	–	3	I	Enable input. Logic high turns on power switch, IN1-OUT1.
EN2	–	4	I	Enable input. Logic high turns on power switch, IN1-OUT2.
EN3	–	7	I	Enable input. Logic high turns on power switch, IN2-OUT3.
EN4	–	8	I	Enable input. Logic high turns on power switch, IN2-OUT4.
GND1	1	1		Ground.
GND2	5	5		Ground.
IN1	2	2	I	Input voltage.
IN2	6	6	I	Input voltage.
$\overline{OC1}$	16	16	O	Overcurrent. Logic output active low, IN1-OUT1
$\overline{OC2}$	13	13	O	Overcurrent. Logic output active low, IN1-OUT2
$\overline{OC3}$	12	12	O	Overcurrent. Logic output active low, IN2-OUT3
$\overline{OC4}$	9	9	O	Overcurrent. Logic output active low, IN2-OUT4
OUT1	15	15	O	Power-switch output, IN1-OUT1
OUT2	14	14	O	Power-switch output, IN1-OUT2
OUT3	11	11	O	Power-switch output, IN2-OUT3
OUT4	10	10	O	Power-switch output, IN2-OUT4

detailed description

power switch

The power switch is an N-channel MOSFET with a maximum on-state resistance of 135 mΩ ($V_{I(INx)}$ = 5 V). Configured as a high-side switch, the power switch prevents current flow from OUTx to INx and INx to OUTx when disabled. The power switch supplies a minimum of 500 mA per switch.

charge pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 4-ms range.

enable ($\overline{\text{ENx}}$ or ENx)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 20 µA when a logic high is present on $\overline{\text{ENx}}$ (TPS2044) or a logic low is present on ENx (TPS2054). A logic zero input on $\overline{\text{ENx}}$ or logic high on ENx restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

overcurrent ($\overline{\text{OCx}}$)

The $\overline{\text{OCx}}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed.

current sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant current mode and holds the current constant while varying the voltage on the load.

thermal sense

The TPS2044 and TPS2054 implement a dual-threshold thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition the junction temperature rises. When the die temperature rises to approximately 140°C, the internal thermal sense circuitry checks to determine which power switch is in an overcurrent condition and turns off that switch, thus isolating the fault without interrupting operation of the adjacent power switch. Hysteresis is built into the thermal sense, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed. The ($\overline{\text{OCx}}$) open-drain output is asserted (active low) when overtemperature or overcurrent occurs.

undervoltage lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, $V_{I(INx)}$ (see Note1) ..... –0.3 V to 6 V
Output voltage range, $V_{O(OUTx)}$ (see Note1) ..... –0.3 V to $V_{I(INx)}$ + 0.3 V
Input voltage range, $V_{I(\overline{ENx})}$ or $V_{I(ENx)}$ ..... –0.3 V to 6 V
Continuous output current, $I_{O(OUTx)}$ ..... Internally limited
Continuous total power dissipation ..... See Dissipation Rating Table
Operating virtual junction temperature range, T_J ..... –40°C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C
Electrostatic discharge (ESD) protection: Human body model MIL-STD-883C ..... 2 kV
Machine model ..... 0.2 kV

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.6 mW/°C	464 mW	377 mW

recommended operating conditions

	TPS2044		TPS2054		UNIT
	MIN	MAX	MIN	MAX	
Input voltage, $V_{I(INx)}$	2.7	5.5	2.7	5.5	V
Input voltage, $V_{I(\overline{ENx})}$ or $V_{I(ENx)}$	0	5.5	0	5.5	V
Continuous output current, $I_{O(OUTx)}$	0	500	0	500	mA
Operating virtual junction temperature, T_J	–40	125	–40	125	°C

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $V_{I(\overline{ENx})}$ = 0 V, $V_{I(ENx)}$ = Hi (unless otherwise noted)

power switch

PARAMETER		TEST CONDITIONS†	TPS2044			TPS2054			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$r_{DS(on)}$	Static drain-source on-state resistance, 5-V operation	$V_{I(INx)}$ = 5 V, I_O = 0.5 A, T_J = 25°C		80	95		80	95	mΩ
		$V_{I(INx)}$ = 5 V, I_O = 0.5 A, T_J = 85°C		90	120		90	120	
		$V_{I(INx)}$ = 5 V, I_O = 0.5 A, T_J = 125°C		100	135		100	135	
	Static drain-source on-state resistance, 3.3-V operation	$V_{I(INx)}$ = 3.3 V, I_O = 0.5 A, T_J = 25°C		85	105		85	105	
		$V_{I(INx)}$ = 3.3 V, I_O = 0.5 A, T_J = 85°C		100	135		100	135	
		$V_{I(INx)}$ = 3.3 V, I_O = 0.5 A, T_J = 125°C		115	150		115	150	
t_r	Rise time, output	$V_{I(INx)}$ = 5.5 V, C_L = 1 µF, R_L = 10 Ω, T_J = 25°C		2.5			2.5		ms
		$V_{I(INx)}$ = 2.7 V, C_L = 1 µF, R_L = 10 Ω, T_J = 25°C		3			3		
t_f	Fall time, output	$V_{I(INx)}$ = 5.5 V, C_L = 1 µF, R_L = 10 Ω, T_J = 25°C		4.4			4.4		ms
		$V_{I(INx)}$ = 2.7 V, C_L = 1 µF, R_L = 10 Ω, T_J = 25°C		2.5			2.5		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

enable input $\overline{ENx}$ or ENx

PARAMETER			TEST CONDITIONS	TPS2044			TPS2054			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High-level input voltage		2.7 V ≤ $V_{I(INx)}$ ≤ 5.5 V	2			2			V
V_{IL}	Low-level input voltage		4.5 V ≤ $V_{I(INx)}$ ≤ 5.5 V			0.8			0.8	V
			2.7 V≤ $V_{I(INx)}$ ≤ 4.5 V			0.4			0.4	
I_I	Input current	TPS2044	$V_{I(\overline{ENx})}$ = 0 V or $V_{I(\overline{ENx})}$ = $V_{I(IN)}$	–0.5		0.5				µA
		TPS2054	$V_{I(ENx)}$ = $V_{I(INx)}$ or $V_{I(ENx)}$ = 0 V				–0.5		0.5	
t_{on}	Turnon time		C_L = 100 µF, R_L=10 Ω			20			20	ms
t_{off}	Turnoff time		C_L = 100 µF, R_L=10 Ω			40			40	

current limit

PARAMETER		TEST CONDITIONS†	TPS2044			TPS2054			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{OS}	Short-circuit output current	$V_{I(INx)}$ = 5 V, OUT connected to GND, Device enable into short circuit	0.7	0.9	1.1	0.7	0.9	1.1	A

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $V_{I(\overline{ENx})}$ = 0 V, $V_{I(ENx)}$ = Hi (unless otherwise noted) (continued)

supply current

PARAMETER	TEST CONDITIONS				TPS2044			TPS2054			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
Supply current, low-level output	No Load on OUTx	$V_{I(\overline{ENx})} = V_{I(INx)}$	T_J = 25°C	TPS2044		0.03	2				µA
			–40°C ≤ T_J ≤ 125°C				20				
		$V_{I(ENx)}$ = 0 V	T_J = 25°C	TPS2054					0.03	2	
			–40°C ≤ T_J ≤ 125°C							20	
Supply current, high-level output	No Load on OUTx	$V_{I(\overline{ENx})}$ = 0 V	T_J = 25°C	TPS2044		160	200				µA
			–40°C ≤ T_J ≤ 125°C			200					
		$V_{I(ENx)} = V_{I(INx)}$	T_J = 25°C	TPS2054					160	200	
			–40°C ≤ T_J ≤ 125°C						200		
Leakage current	OUTx connected to ground	$V_{I(\overline{ENx})} = V_{I(INx)}$	–40°C ≤ T_J ≤ 125°C	TPS2044		200					µA
		$V_{I(ENx)}$ = 0 V	–40°C ≤ T_J ≤ 125°C	TPS2054					200		
Reverse leakage current	IN = high impedance	$V_{I(\overline{EN})}$ = 0 V	T_J = 25°C	TPS2044		0.3					µA
		$V_{I(EN)}$ = Hi		TPS2054					0.3		

undervoltage lockout

PARAMETER	TEST CONDITIONS	TPS2044			TPS2054			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Low-level input voltage		2		2.5	2		2.5	V
Hysteresis	T_J = 25°C		100			100		mV

overcurrent $\overline{OCx}$

PARAMETER	TEST CONDITIONS	TPS2044			TPS2054			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Sink current†	V_O = 5 V			10			10	mA
Output low voltage	I_O = 5 mA, $V_{OL(\overline{OCx})}$			0.5			0.5	V
Off-state current†	V_O = 5 V, V_O = 3.3 V			1			1	µA

† Specified by design, not production tested.

PARAMETER MEASUREMENT INFORMATION

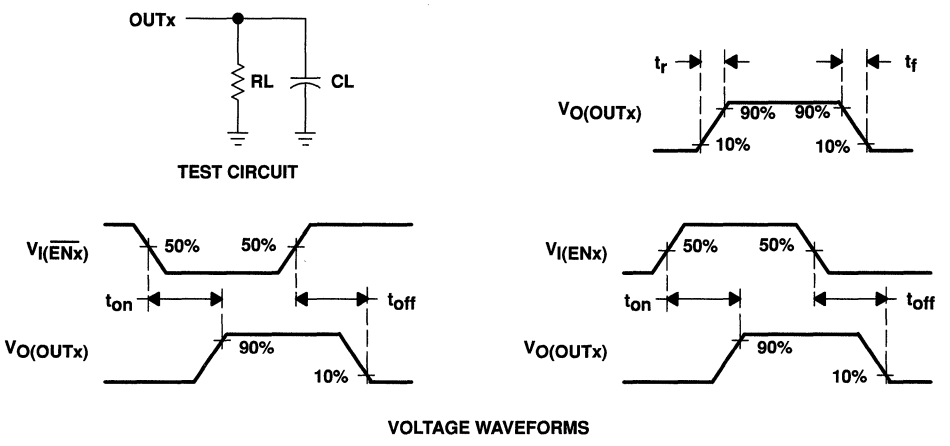


Figure 1. Test Circuit and Voltage Waveforms

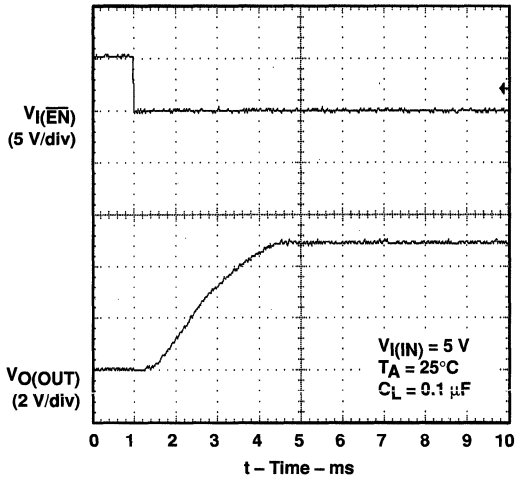


Figure 2. Turnon Delay and Rise Time with 0.1-μF Load

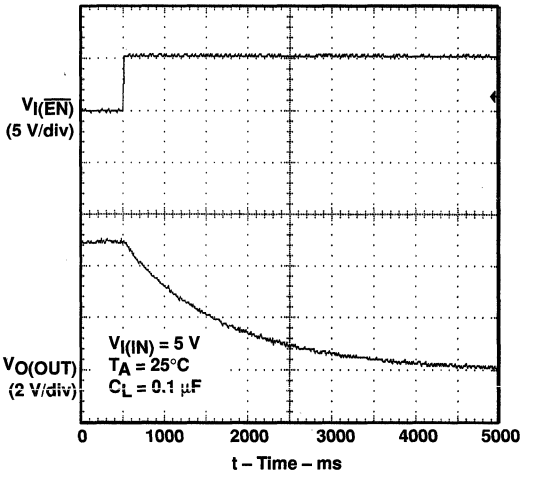


Figure 3. Turnoff Delay and Fall Time with 0.1-μF Load

PARAMETER MEASUREMENT INFORMATION

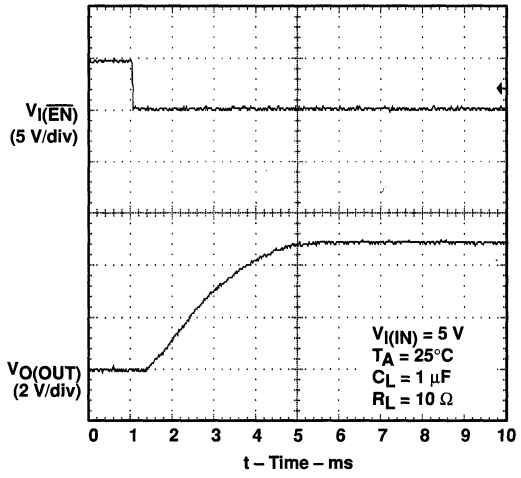


Figure 4. Turnon Delay and Rise Time with 1-μF Load

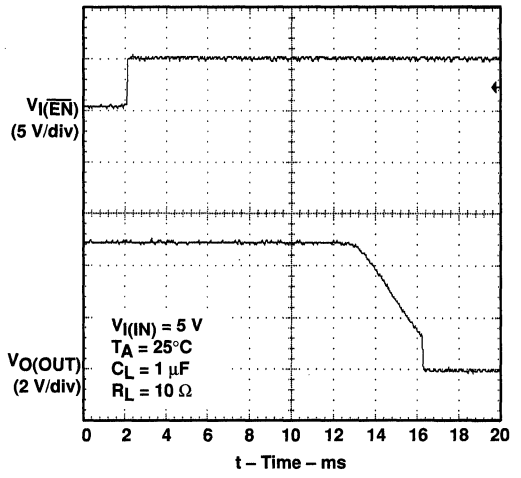


Figure 5. Turnoff Delay and Fall Time with 1-μF Load

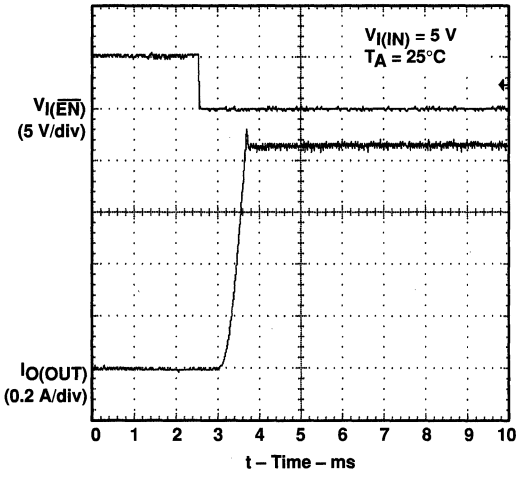


Figure 6. TPS2044, Short-Circuit Current, Device Enabled into Short

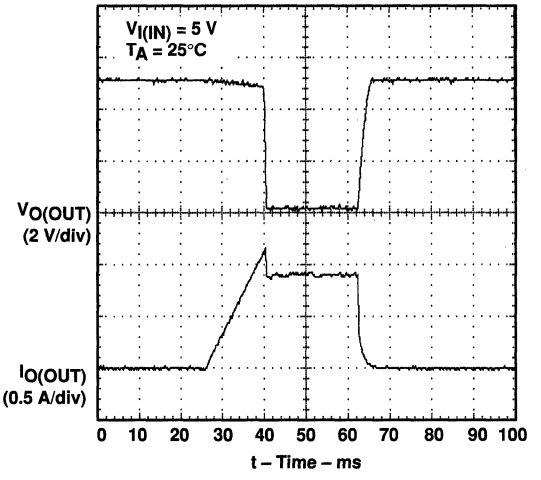


Figure 7. TPS2044, Threshold Trip Current with Ramped Load on Enabled Device

PARAMETER MEASUREMENT INFORMATION

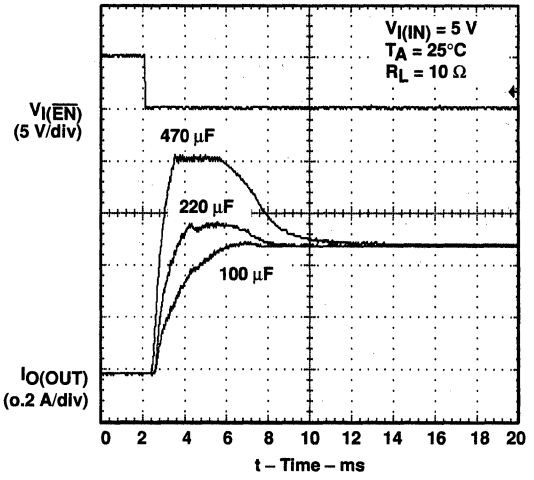


Figure 8. Inrush Current with 100-µF, 220-µF and 470-µF Load Capacitance

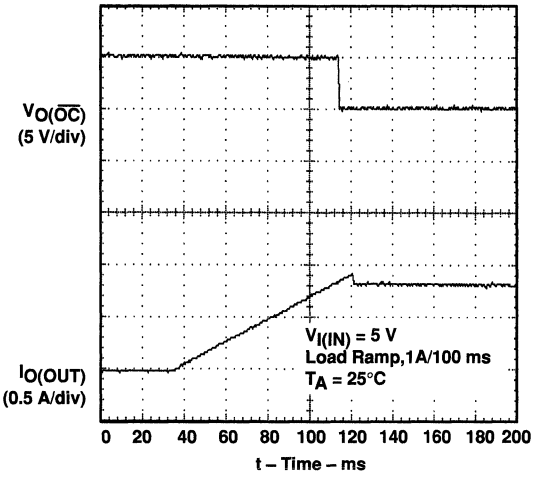


Figure 9. Ramped Load on Enabled Device

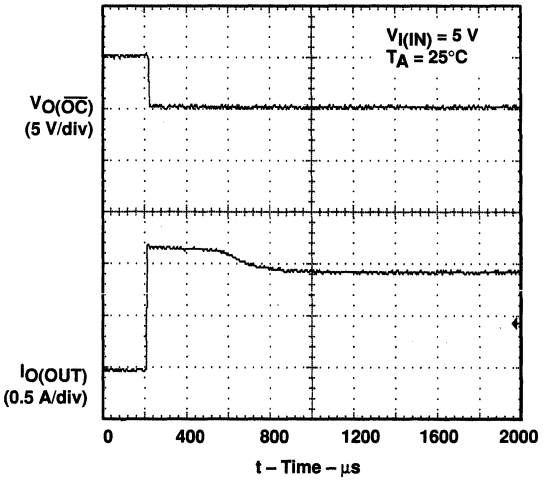


Figure 10. 4-Ω Load Connected to Enabled Device

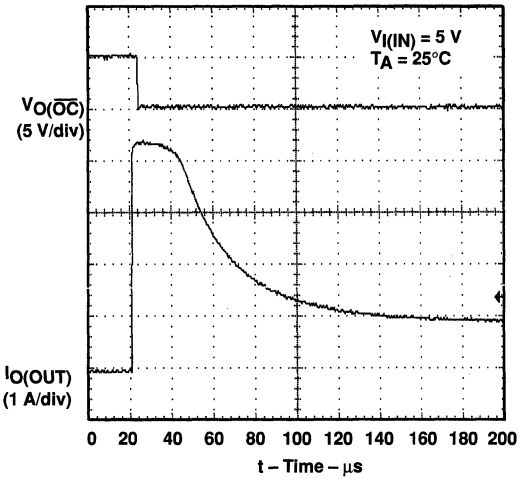


Figure 11. 1-Ω Load Connected to Enabled Device

TYPICAL CHARACTERISTICS

TURNON DELAY vs INPUT VOLTAGE

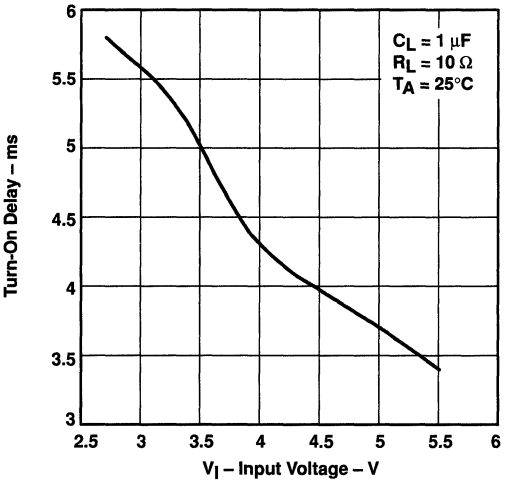


Figure 12

TURNOFF DELAY vs INPUT VOLTAGE

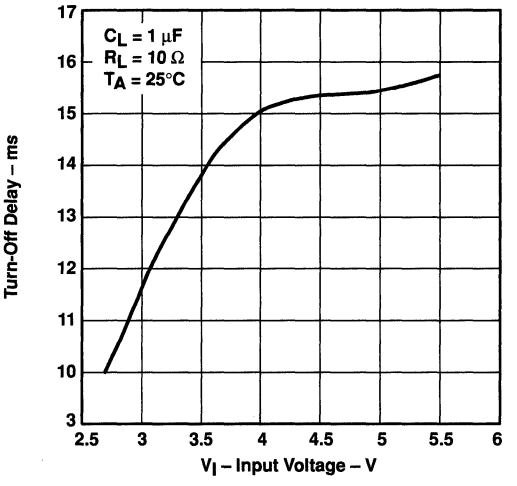


Figure 13

RISE TIME vs LOAD CURRENT

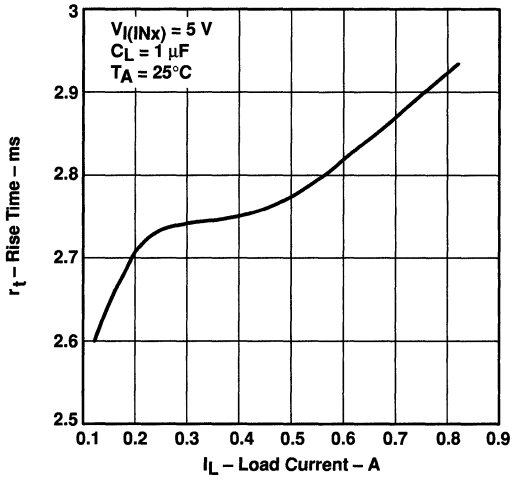


Figure 14

FALL TIME vs LOAD CURRENT

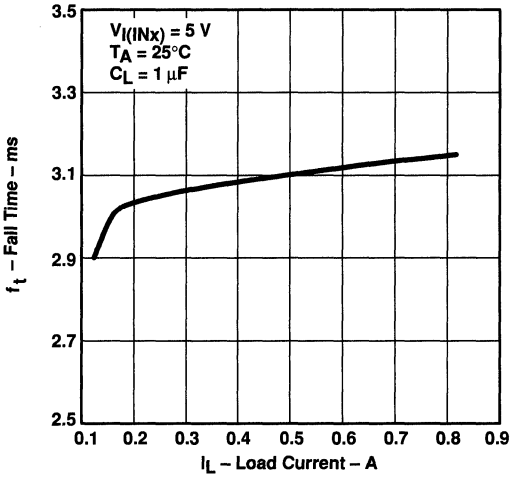


Figure 15

TYPICAL CHARACTERISTICS

SUPPLY CURRENT, OUTPUT ENABLED
vs
JUNCTION TEMPERATURE

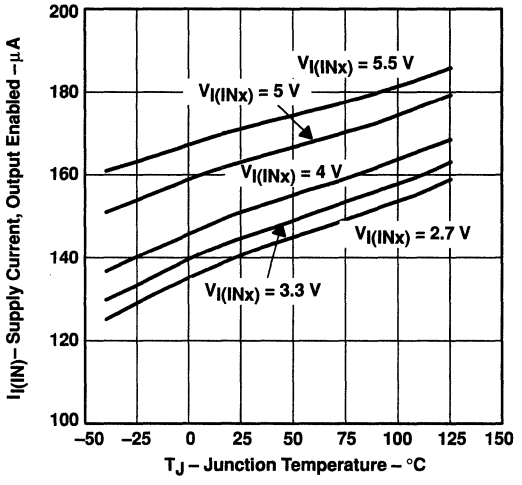


Figure 16

SUPPLY CURRENT, OUTPUT DISABLED
vs
JUNCTION TEMPERATURE

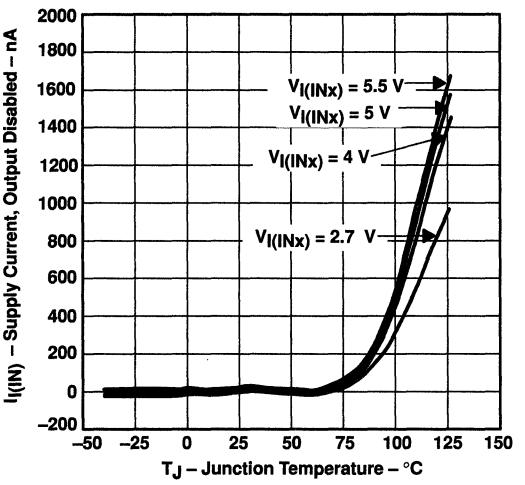


Figure 17

SUPPLY CURRENT, OUTPUT ENABLED
vs
INPUT VOLTAGE

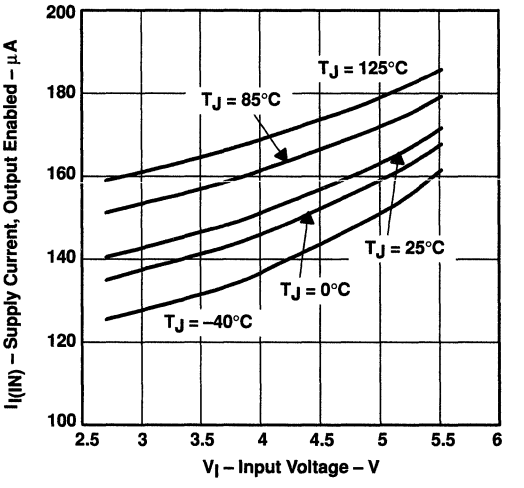


Figure 18

SUPPLY CURRENT, OUTPUT DISABLED
vs
INPUT VOLTAGE

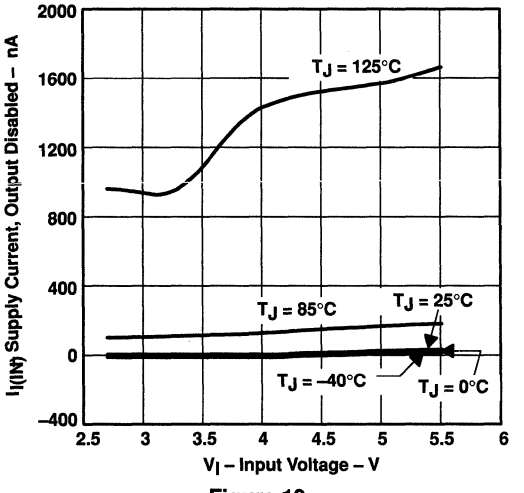


Figure 19

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

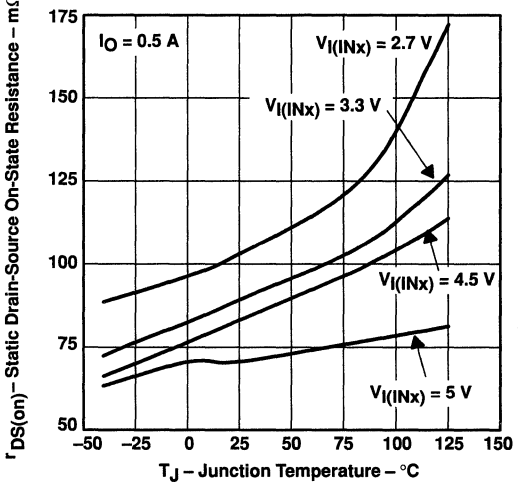


Figure 20

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
INPUT VOLTAGE

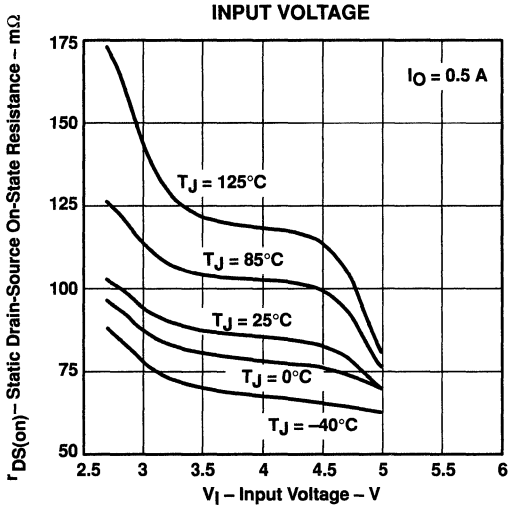


Figure 21

INPUT-TO-OUTPUT VOLTAGE
vs
LOAD CURRENT

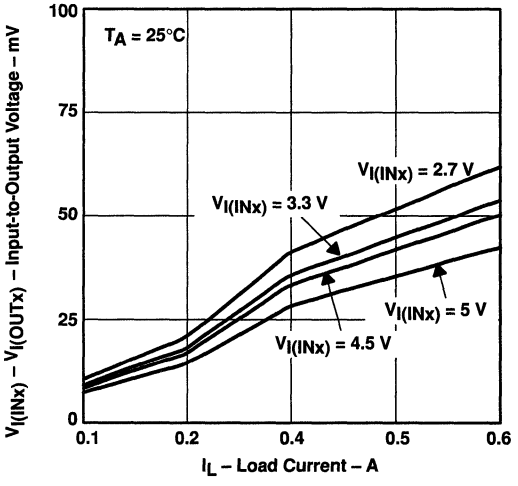


Figure 22

SHORT-CURCUIT OUTPUT CURRENT
vs
INPUT VOLTAGE

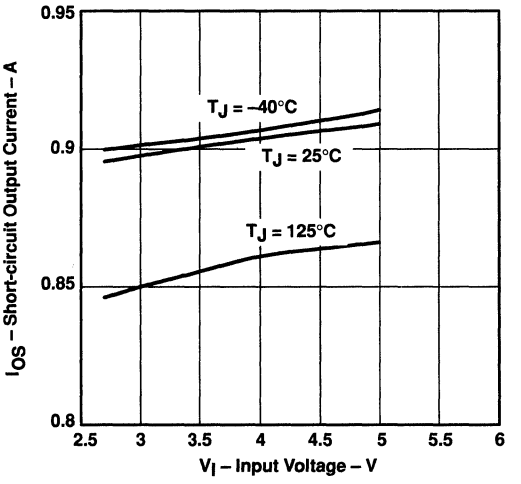


Figure 23

TYPICAL CHARACTERISTICS

THRESHOLD TRIP CURRENT
vs
INPUT VOLTAGE

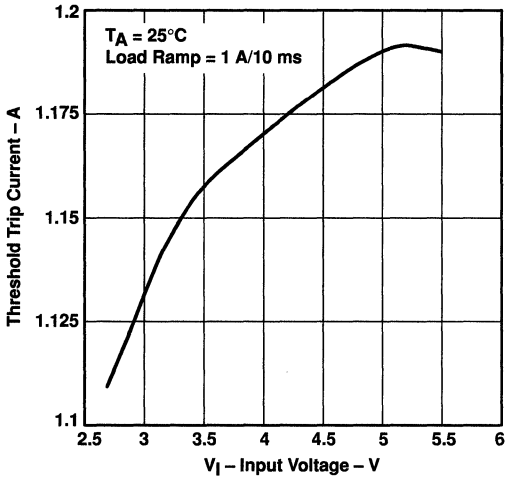


Figure 24

SHORT-CIRCUIT OUTPUT CURRENT
vs
JUNCTION TEMPERATURE

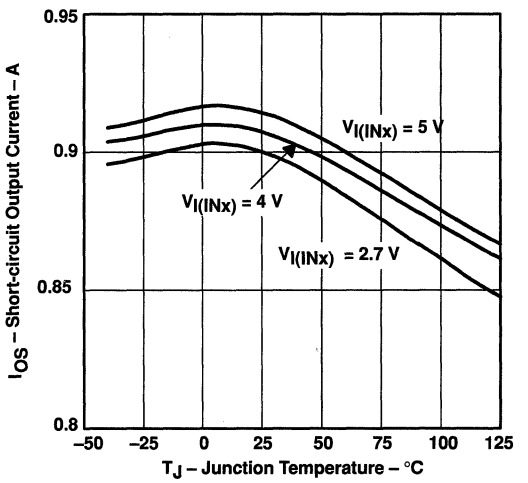


Figure 25

UNDERVOLTAGE LOCKOUT
vs
JUNCTION TEMPERATURE

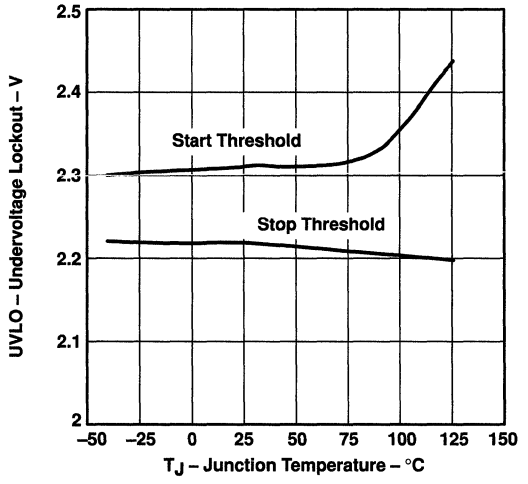


Figure 26

CURRENT LIMIT RESPONSE
vs
PEAK CURRENT

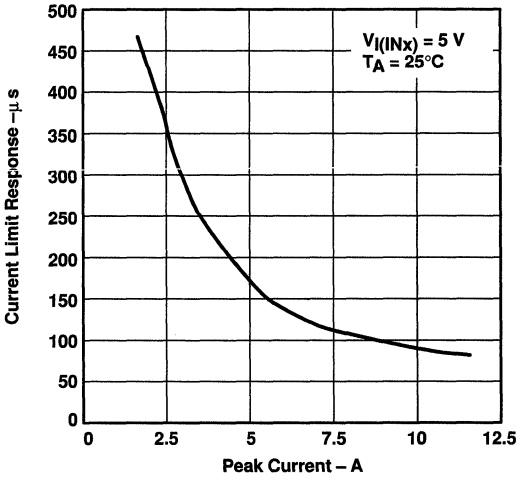


Figure 27

TYPICAL CHARACTERISTICS

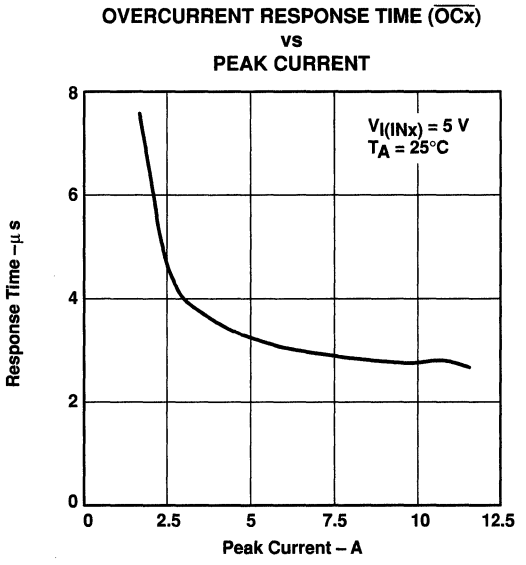


Figure 28

APPLICATION INFORMATION

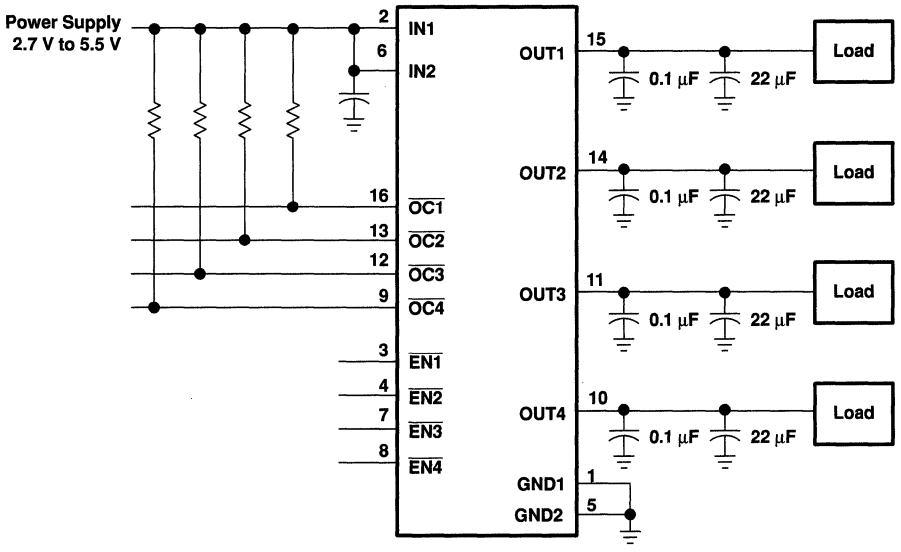


Figure 29. Typical Application

APPLICATION INFORMATION

power-supply considerations

A 0.01-μF to 0.1-μF ceramic bypass capacitor between INx and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-μF to 0.1-μF ceramic capacitor improves the immunity of the device to short-circuit transients.

overcurrent

A sense FET checks for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(INx)}$ has been applied (see Figure 6). The TPS2044 and TPS2054 sense the short and immediately switch into a constant-current output.

In the second condition, the short occurs while the device is enabled. At the instant the short occurs, very high currents may flow for a short time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshhold) the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figure 7). The TPS2044 and TPS2054 are capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

APPLICATION INFORMATION

$\overline{OC}$ response

The $\overline{OC}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false overcurrent reporting from the inrush current flowing through the device, charging the downstream capacitor. An RC filter of 500 µs (see Figure 30) can be connected to the $\overline{OC}$ pin to reduce false overcurrent reporting. Using low-ESR electrolytic capacitors on the output lowers the inrush current flow through the device during hot-plug events by providing a low impedance energy source, thereby reducing erroneous overcurrent reporting.

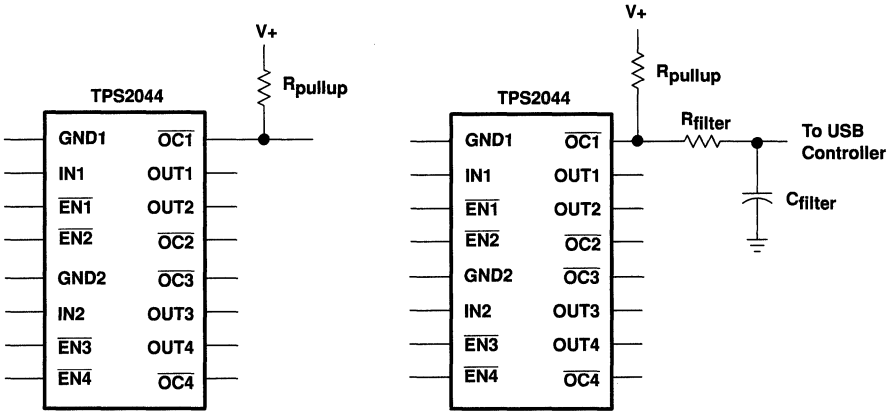


Figure 30. Typical Circuit for $\overline{OC}$ Pin and RC Filter for Damping Inrush $\overline{OC}$ Responses

power dissipation and junction temperature

The low on-resistance on the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find $r_{DS(on)}$ at the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figure 21. Next, calculate the power dissipation using:

$$P_D = r_{DS(on)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient Temperature °C
$R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

APPLICATION INFORMATION

thermal protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS2044 and TPS2054 into constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels. The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

The TPS2044 and TPS2054 implement a dual thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition the junction temperature will rise. Once the die temperature rises to approximately 140°C, the internal thermal sense circuitry checks which power switch is in an overcurrent condition and turns that power switch off, thus isolating the fault without interrupting operation of the adjacent power switch. Should the die temperature exceed the first thermal trip point of 140°C and reach 160°C, both switches turn off. The $\overline{OC}$ open-drain output is asserted (active low) when overtemperature or overcurrent occurs.

undervoltage lockout (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch will be quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO will also keep the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. Upon reinsertion, the power switch will be turned on with a controlled rise time to reduce EMI and voltage overshoots.

universal serial bus (USB) applications

The universal serial bus (USB) interface is a 12-Mb/s, or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

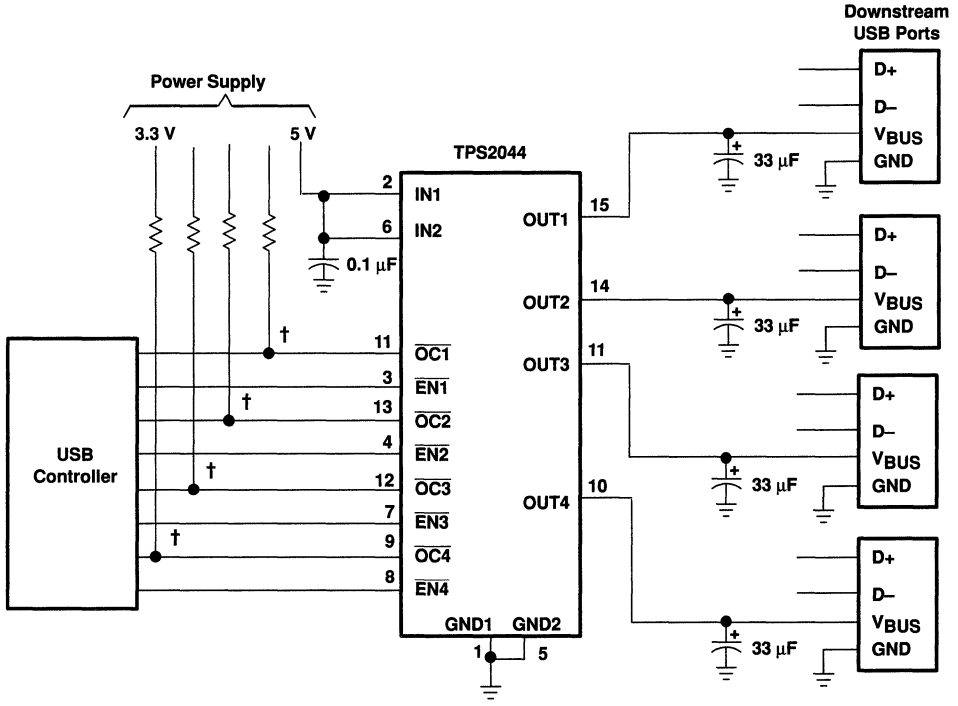
- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

Self-powered and bus-powered hubs distribute data and power to downstream functions. The TPS2044 and TPS2054 can provide power-distribution solutions for many of these classes of devices.

APPLICATION INFORMATION

host/self-powered and bus-powered hubs

Hosts and self-powered hubs have a local power supply that powers the embedded functions and the downstream ports (see Figure 31). This power supply must provide from 5.25 V to 4.75 V to the board side of the downstream connection under full-load and no-load conditions. Hosts and SPHs must have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.



† An RC filter may be needed, see Figure 36

Figure 31. Typical Four-Port USB Host/Self-Powered Hub

Bus-powered hubs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

APPLICATION INFORMATION

low-power bus-powered functions and high-power bus-powered functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA, and high-power functions must draw less than 100 mA at powerup and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 µF at power up, the device must implement inrush current limiting (see Figure 32).

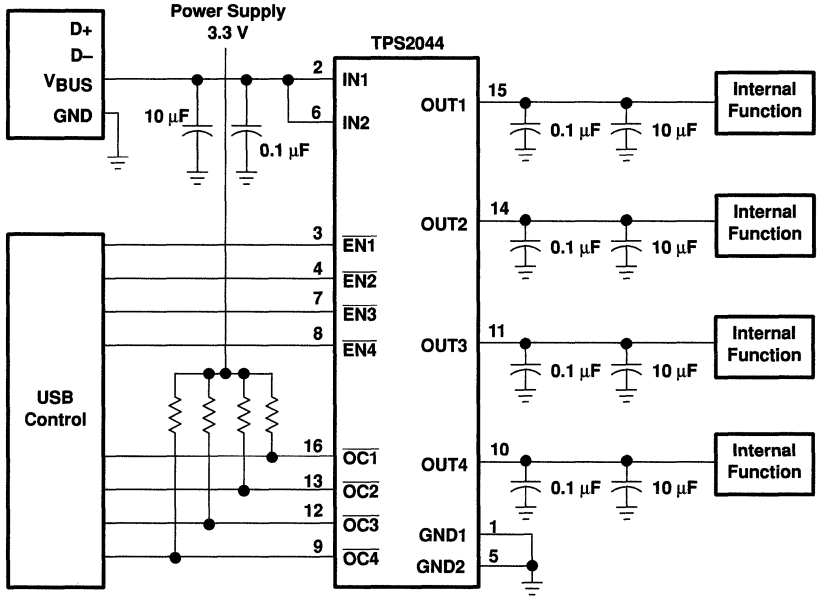


Figure 32. High-Power Bus-Powered Function

APPLICATION INFORMATION

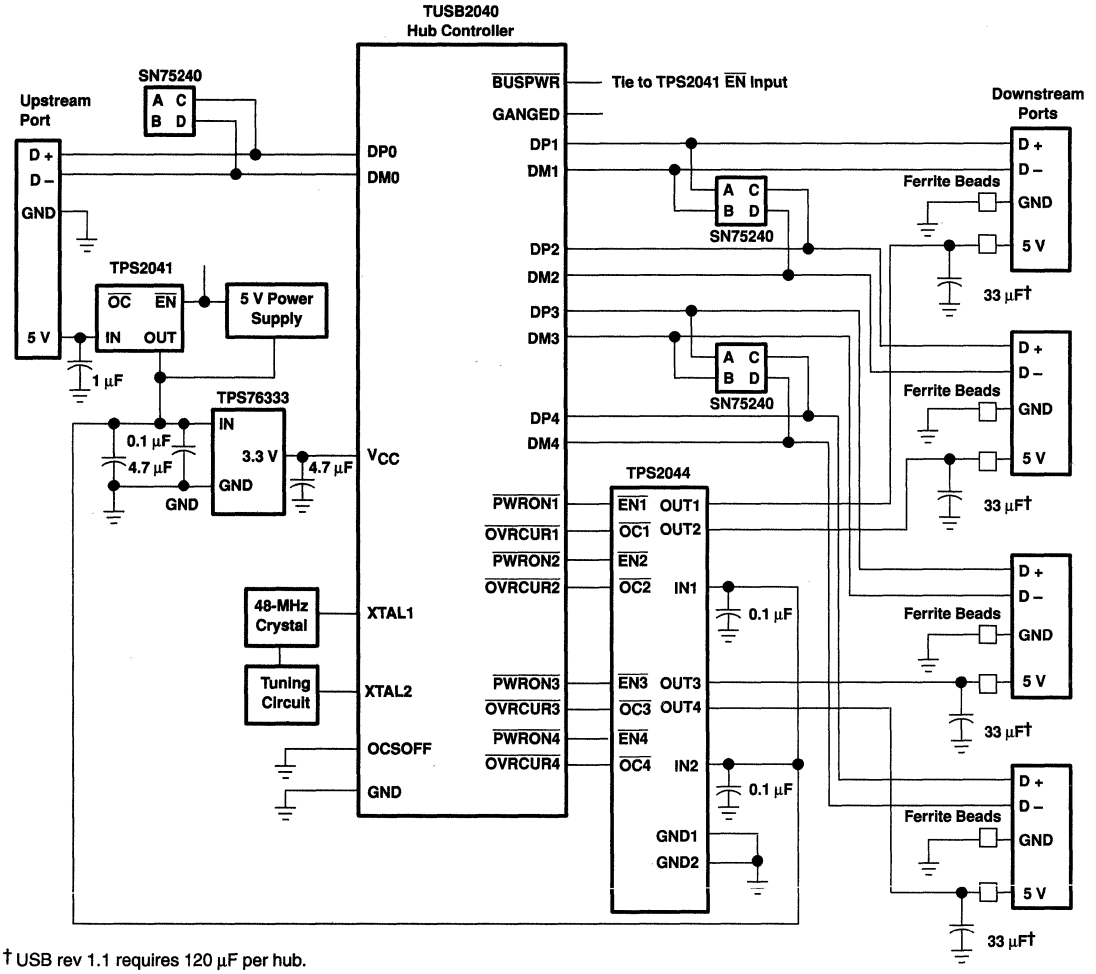
USB power-distribution requirements

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power-distribution features must be implemented.

- Hosts/self-powered hubs must:
  - Current-limit downstream ports
  - Report overcurrent conditions on USB V_{BUS}
- Bus-powered hubs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 μF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

The feature set of the TPS2044 and TPS2054 allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-power hubs, as well as the input ports for bus-power functions (see Figure 33).

APPLICATION INFORMATION



† USB rev 1.1 requires 120 µF per hub.

Figure 33. Hybrid Self/Bus-Powered Hub Implementation

APPLICATION INFORMATION

generic hot-plug applications (see Figure 34)

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS2044 and TPS2054, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS2044 and TPS2054 also ensures the switch will be off after the card has been removed, and the switch will be off during the next insertion. The UVLO feature guarantees a soft start with a controlled rise time for every insertion of the card or module.

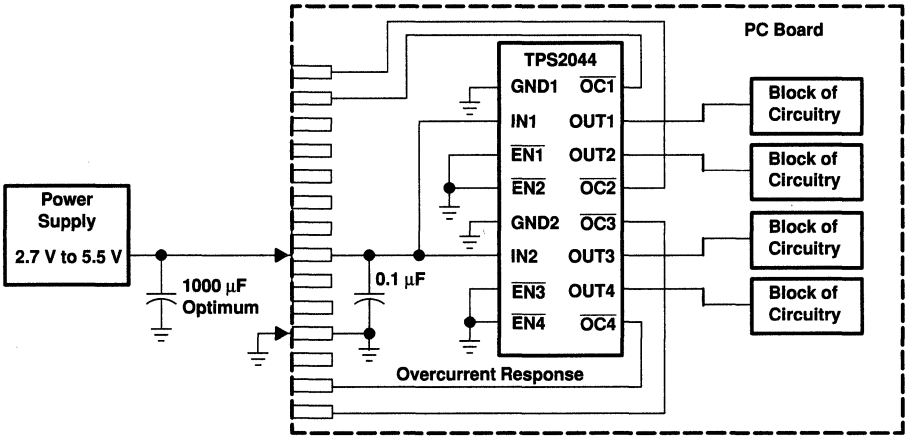


Figure 34. Typical Hot-Plug Implementation

By placing the TPS2044 and TPS2054 between the V_{CC} input and the rest of the circuitry, the input power will reach these devices first after insertion. The typical rise time of the switch is approximately 2.5 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

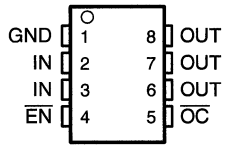
features

- 135-mΩ -Maximum (5-V Input) High-Side MOSFET Switch
- 250 mA Continuous Current
- Short-Circuit and Thermal Protection With Overcurrent Logic Output
- Operating Range . . . 2.7-V to 5.5-V
- Logic-Level Enable Input
- 2.5-ms Typical Rise Time
- Undervoltage Lockout
- 10 μA Maximum Standby Supply Current
- Bidirectional Switch
- Available in 8-pin SOIC and PDIP Packages
- Ambient Temperature Range, –40°C to 85°C
- 2-kV Human-Body-Model, 200-V Machine-Model ESD Protection

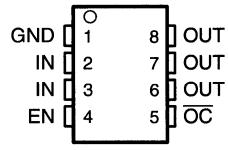
typical applications

- Notebook, Desktop and Palmtop PCs
- Monitors, Keyboards, Scanners, and Printers
- Digital Cameras, Phones, and PBXs
- Hot-Insertion Applications

TPS2045
D OR P PACKAGE
(TOP VIEW)



TPS2055
D OR P PACKAGE
(TOP VIEW)



description

The TPS2045 and TPS2055 power-distribution switches are intended for applications where heavy capacitive loads and short circuits are likely. Each of these 135-mΩ N-channel MOSFET high-side power switches is controlled by a logic enable compatible with 5-V and 3-V logic. Gate drive is provided by an internal charge pump that controls the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the TPS2045 and TPS2055 limit the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{OC}$) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch in overcurrent to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until valid input voltage is present.

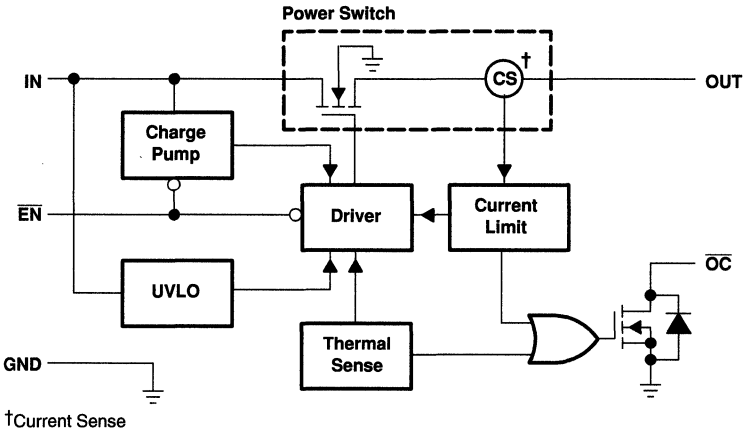
The TPS2045 and TPS2055 are designed to limit at 0.44-A load. These power-distribution switches, available in 8-pin small-outline integrated circuit (SOIC) and 8-pin plastic dual-in-line packages (PDIP), operate over an ambient temperature range of –40°C to 85°C.

AVAILABLE OPTIONS

T_A	ENABLE	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A)	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (A)	PACKAGED DEVICES	
				SOIC (D)†	PDIP (P)
–40°C to 85°C	Active low	0.25	0.44	TPS2045D	TPS2045P
–40°C to 85°C	Active high	0.25	0.44	TPS2055D	TPS2055P

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2045DR)

TPS2045 functional block diagram



Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO. D OR P			
	TPS2045	TPS2055		
$\overline{EN}$	4	–	I	Enable input. Logic low turns on power switch.
EN	–	4	I	Enable input. Logic high turns on power switch.
GND	1	1	I	Ground
IN	2, 3	2, 3	I	Input voltage
$\overline{OC}$	5	5	O	Over current. Logic output active low
OUT	6, 7, 8	6, 7, 8	O	Power-switch output

detailed description

power switch

The power switch is an N-channel MOSFET with a maximum on-state resistance of 135 mΩ ($V_{I(IN)}$ = 5 V). Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled. The power switch can supply a minimum of 250 mA per switch.

charge pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 4-ms range.

enable ($\overline{EN}$ or EN)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10 μA when a logic high is present on $\overline{EN}$ (TPS2045) or a logic low is present on EN (TPS2055). A logic zero input on $\overline{EN}$ or a logic high on EN restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

overcurrent ($\overline{OC}$)

The $\overline{OC}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed.

current sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant current mode and holds the current constant while varying the voltage on the load.

thermal sense

An internal thermal-sense circuit shuts off the power switch when the junction temperature rises to approximately 140°C. Hysteresis is built into the thermal sense circuit. After the device has cooled approximately 20°C, the switch turns back on. The switch continues to cycle off and on until the fault is removed.

undervoltage lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, $V_{I(IN)}$ (see Note 1) ..... –0.3 V to 6 V
Output voltage range, $V_{O(OUT)}$ (see Note 1) ..... –0.3 V to $V_{I(IN)}$ + 0.3 V
Input voltage range, $V_{I(\overline{EN})}$ or $V_{I(EN)}$ ..... –0.3 V to 6 V
Continuous output current, $I_{O(OUT)}$ ..... internally limited
Continuous total power dissipation ..... See Dissipation Rating Table
Operating virtual junction temperature range, T_J ..... –40°C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C
Electrostatic discharge (ESD) protection: Human body model MIL-STD-883C ..... 2 kV
Machine model ..... 0.2 kV

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1175 mW	9.4 mW/°C	752 mW	611 mW

recommended operating conditions

	TPS2045		TPS2055		UNIT
	MIN	MAX	MIN	MAX	
Input voltage, $V_{I(IN)}$	2.7	5.5	2.7	5.5	V
Input voltage, $V_{I(\overline{EN})}$ or $V_{I(EN)}$	0	5.5	0	5.5	V
Continuous output current, $I_{O(OUT)}$	0	250	0	250	mA
Operating virtual junction temperature, T_J	–40	125	–40	125	°C

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $V_{I(\overline{EN})}$= 0 V, $V_{I(EN)}$ = Hi (unless otherwise noted)

power switch

PARAMETER		TEST CONDITIONS†	TPS2045			TPS2055			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$r_{DS(on)}$	Static drain-source on-state resistance, 5-V operation	$V_{I(IN)}$ = 5 V, T_J = 25°C, I_O = 0.25 A		80	95		80	95	mΩ
		$V_{I(IN)}$ = 5 V, T_J = 85°C, I_O = 0.25 A		90	120		90	120	
		$V_{I(IN)}$ = 5 V, T_J = 125°C, I_O = 0.25 A		100	135		100	135	
	Static drain-source on-state resistance, 3.3-V operation	$V_{I(IN)}$ = 3.3 V, T_J = 25°C, I_O = 0.25 A		85	105		85	105	
		$V_{I(IN)}$ = 3.3 V, T_J = 85°C, I_O = 0.25 A		100	135		100	135	
		$V_{I(IN)}$ = 3.3 V, T_J = 125°C, I_O = 0.25 A		115	150		115	150	
t_r	Rise time, output	$V_{I(IN)}$ = 5.5 V, T_J = 25°C, C_L = 1 µF, R_L = 20 Ω		2.5			2.5		ms
		$V_{I(IN)}$ = 2.7 V, T_J = 25°C, C_L = 1 µF, R_L = 20 Ω		3			3		
t_f	Fall time, output	$V_{I(IN)}$ = 5.5 V, T_J = 25°C, C_L = 1 µF, R_L = 20 Ω		4.4			4.4		ms
		$V_{I(IN)}$ = 2.7 V, T_J = 25°C, C_L = 1 µF, R_L = 20 Ω		2.5			2.5		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

enable input $\overline{EN}$ or EN

PARAMETER			TEST CONDITIONS	TPS2045			TPS2055			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High-level input voltage		2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V	2			2			V
V_{IL}	Low-level input voltage		4.5 V ≤ $V_{I(IN)}$ ≤ 5.5 V			0.8			0.8	V
			2.7 V ≤ $V_{I(IN)}$ ≤ 4.5 V			0.4			0.4	
I_I	Input current	TPS2045	$V_{I(\overline{EN})}$ = 0 V or $V_{I(EN)}$ = $V_{I(IN)}$	–0.5		0.5				µA
		TPS2055	$V_{I(\overline{EN})}$ = $V_{I(IN)}$ or $V_{I(EN)}$ = 0 V				–0.5		0.5	
t_{on}	Turnon time		C_L = 100 µF, R_L = 20 Ω			20			20	ms
t_{off}	Turnoff time		C_L = 100 µF, R_L = 20 Ω			40			40	

current limit

PARAMETER		TEST CONDITIONS†	TPS2045			TPS2055			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{OS}	Short-circuit output current	$V_{I(IN)}$ = 5 V, OUT connected to GND, Device enabled into short circuit	0.345	0.44	0.525	0.345	0.44	0.525	A

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $V_{I(\overline{EN})}$ = 0 V, $V_{I(EN)}$ = Hi (unless otherwise noted) (continued)

supply current

PARAMETER	TEST CONDITIONS				TPS2045			TPS2055			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
Supply current, low-level output	No Load on OUT	$V_{I(\overline{EN})} = V_{I(IN)}$	T_J = 25°C	TPS2045		0.015	1				µA
			–40°C ≤ T_J ≤ 125°C				10				
		$V_{I(EN)}$ = 0 V	T_J = 25°C	TPS2055					0.015	1	
			–40°C ≤ T_J ≤ 125°C							10	
Supply current, high-level output	No Load on OUT	$V_{I(\overline{EN})}$ = 0 V	T_J = 25°C	TPS2045		80	100				µA
			–40°C ≤ T_J ≤ 125°C			100					
		$V_{I(EN)} = V_{I(IN)}$	T_J = 25°C	TPS2055					80	100	
			–40°C ≤ T_J ≤ 125°C						100		
Leakage current	OUT connected to ground	$V_{I(\overline{EN})} = V_{I(IN)}$	–40°C ≤ T_J ≤ 125°C	TPS2045		100					µA
		$V_{I(EN)}$ = 0 V	–40°C ≤ T_J ≤ 125°C	TPS2055					100		
Reverse leakage current	IN = high impedance	$V_{I(\overline{EN})}$ = 0 V	T_J = 25°C	TPS2045		0.3					µA
		$V_{I(EN)}$ = Hi		TPS2055					0.3		

undervoltage lockout

PARAMETER	TEST CONDITIONS	TPS2045			TPS2055			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Low-level input voltage		2		2.5	2		2.5	V
Hysteresis	T_J = 25°C		100			100		mV

overcurrent $\overline{OC}$

PARAMETER	TEST CONDITIONS	TPS2045			TPS2055			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Sink current†	V_O = 5 V			10			10	mA
Output low voltage	I_O = 5 V, $V_{OL(\overline{OC})}$			0.5			0.5	V
Off-state current†	V_O = 5 V, V_O = 3.3 V			1			1	µA

† Specified by design, not production tested.

PARAMETER MEASUREMENT INFORMATION

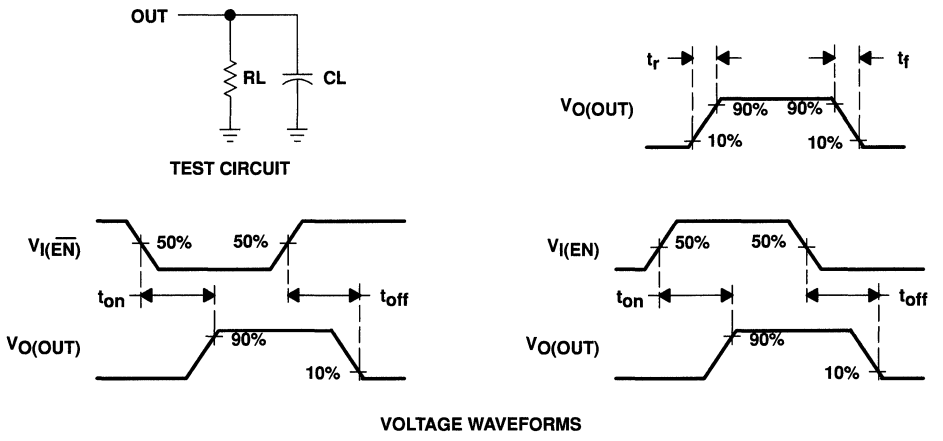


Figure 1. Test Circuit and Voltage Waveforms

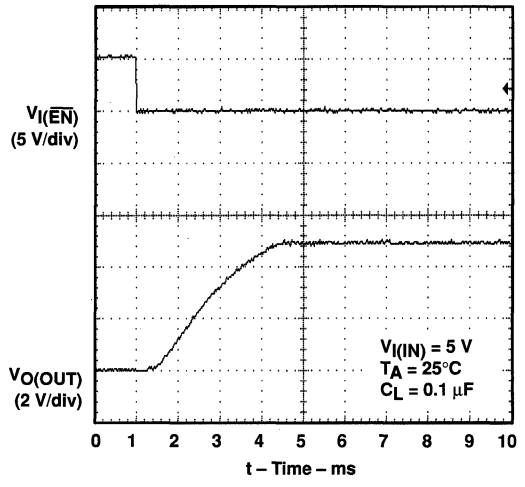


Figure 2. Turnon Delay and Rise Time with 0.1-μF Load

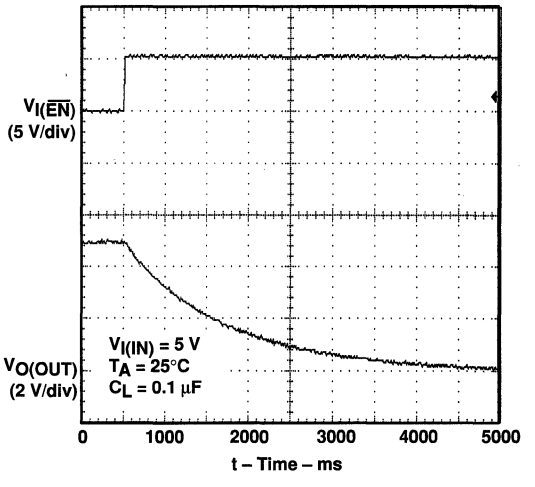


Figure 3. Turnoff Delay and Fall Time with 0.1-μF Load

PARAMETER MEASUREMENT INFORMATION

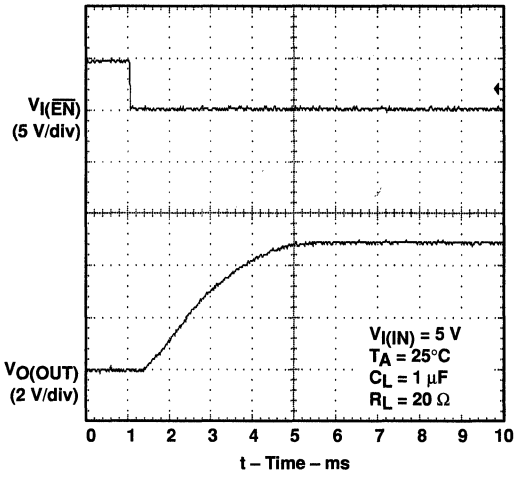


Figure 4. Turnon Delay and Rise Time with 1-μF Load

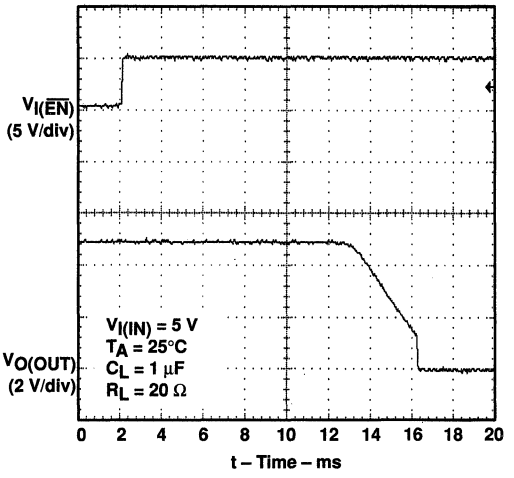


Figure 5. Turnoff Delay and Fall Time with 1-μF Load

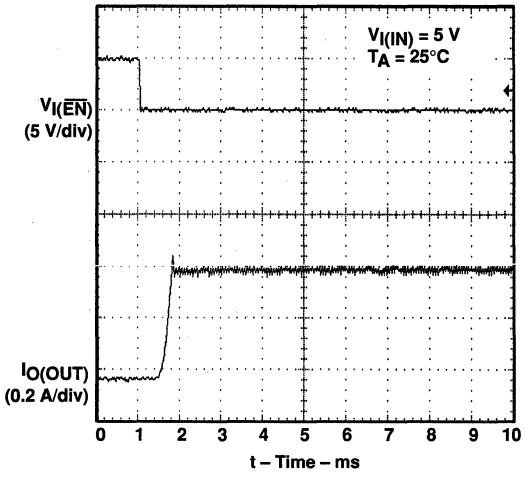


Figure 6. TPS2045, Short-Circuit Current, Device Enabled into Short

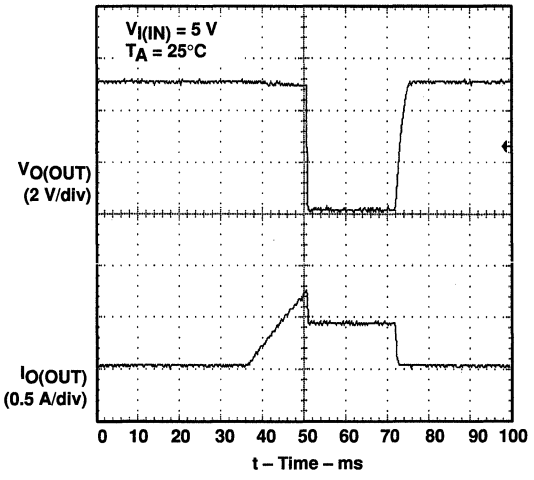


Figure 7. TPS2045, Threshold Trip Current with Ramped Load on Enabled Device

PARAMETER MEASUREMENT INFORMATION

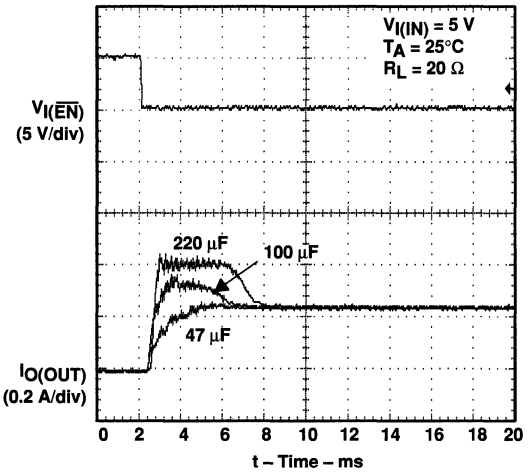


Figure 8. Inrush Current with 220-µF, 100-µF and 47-µF Load Capacitance

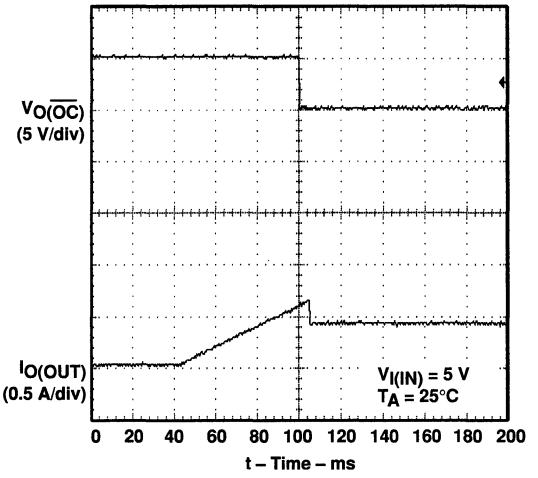


Figure 9. Ramped Load on Enabled Device

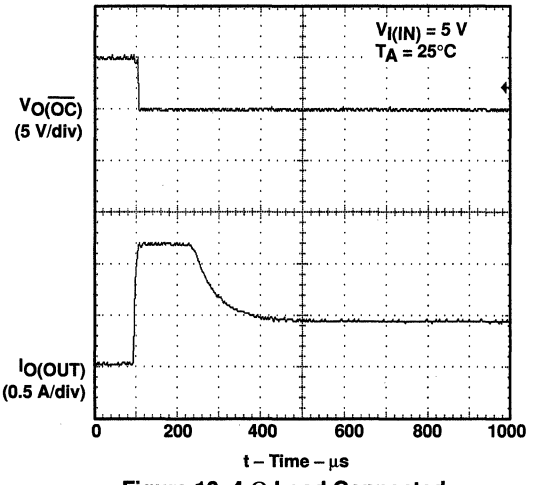


Figure 10. 4-Ω Load Connected to Enabled Device

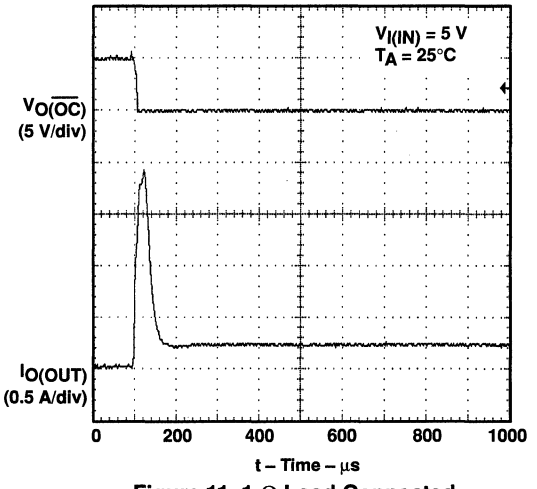


Figure 11. 1-Ω Load Connected to Enabled Device

TYPICAL CHARACTERISTICS

TURNON DELAY
vs
INPUT VOLTAGE

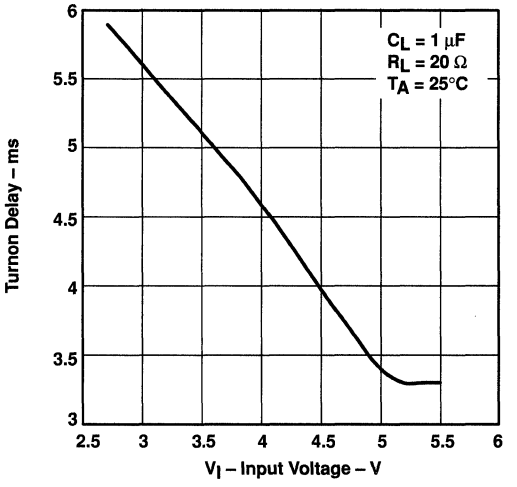


Figure 12

TURNOFF DELAY
vs
INPUT VOLTAGE

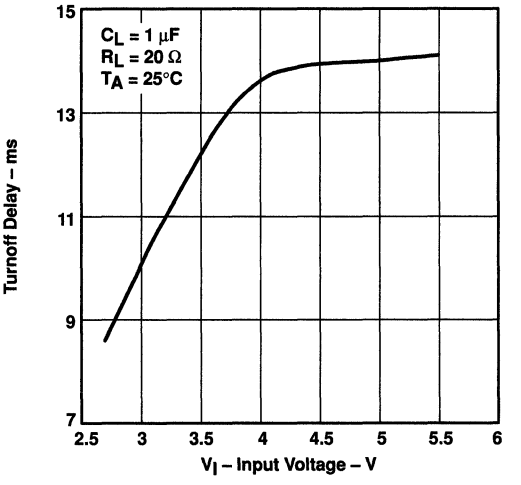


Figure 13

RISE TIME
vs
LOAD CURRENT

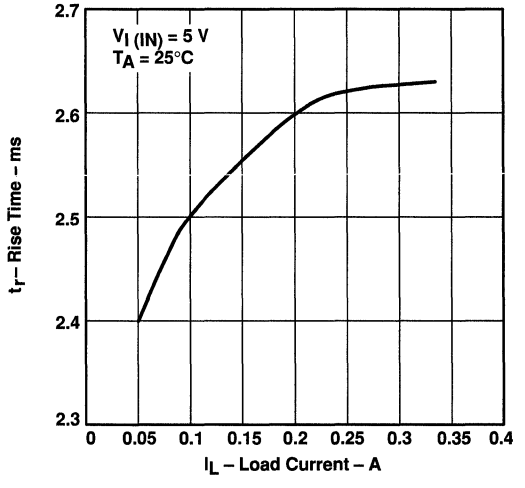


Figure 14

FALL TIME
vs
LOAD CURRENT

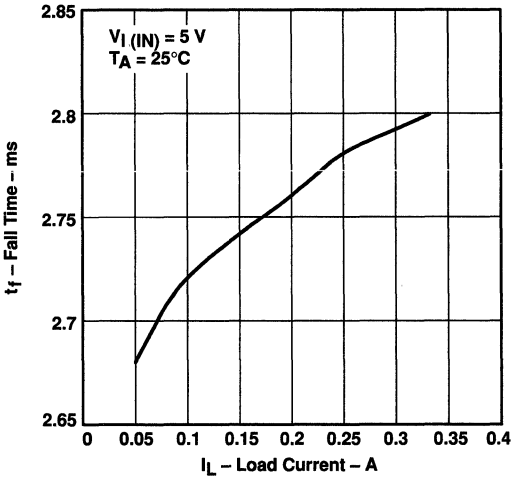


Figure 15

TYPICAL CHARACTERISTICS

SUPPLY CURRENT, OUTPUT ENABLED
vs
JUNCTION TEMPERATURE

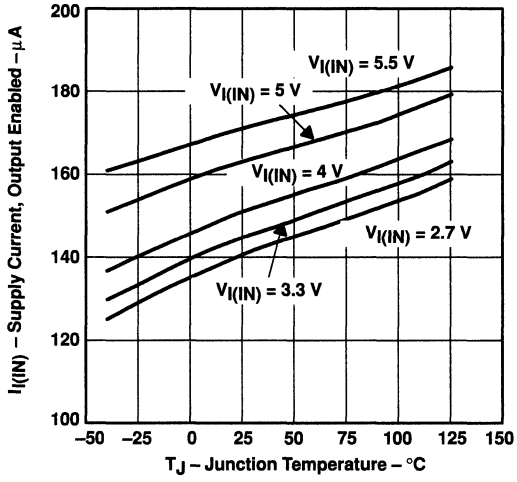


Figure 16

SUPPLY CURRENT, OUTPUT DISABLED
vs
JUNCTION TEMPERATURE

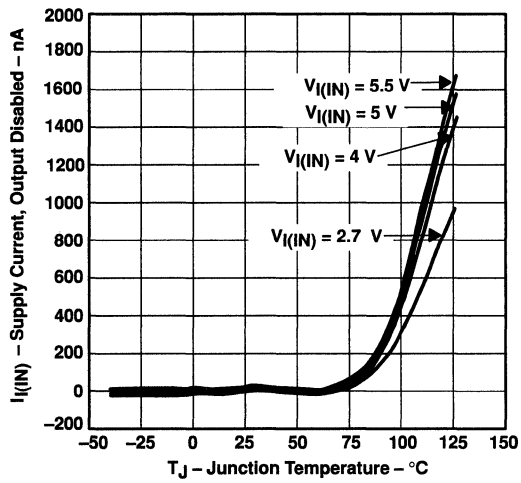


Figure 17

SUPPLY CURRENT, OUTPUT ENABLED
vs
INPUT VOLTAGE

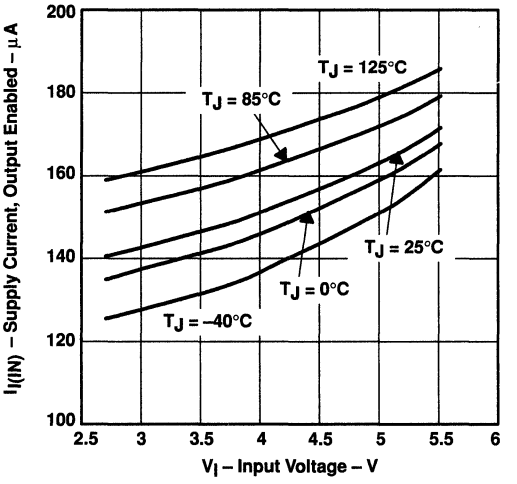


Figure 18

SUPPLY CURRENT, OUTPUT DISABLED
vs
INPUT VOLTAGE

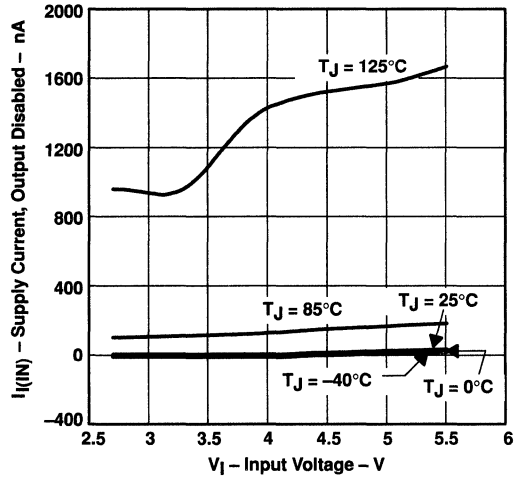


Figure 19

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

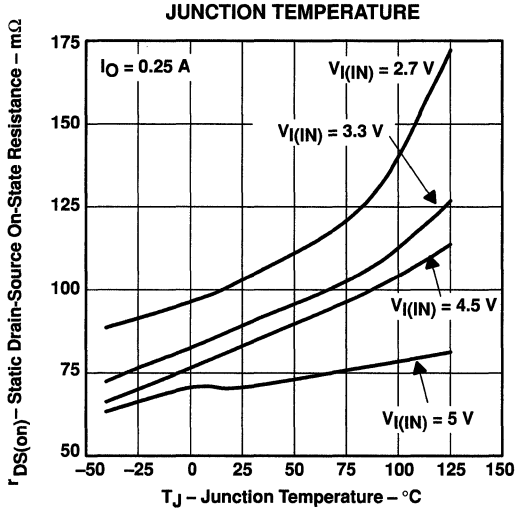


Figure 20

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
INPUT VOLTAGE

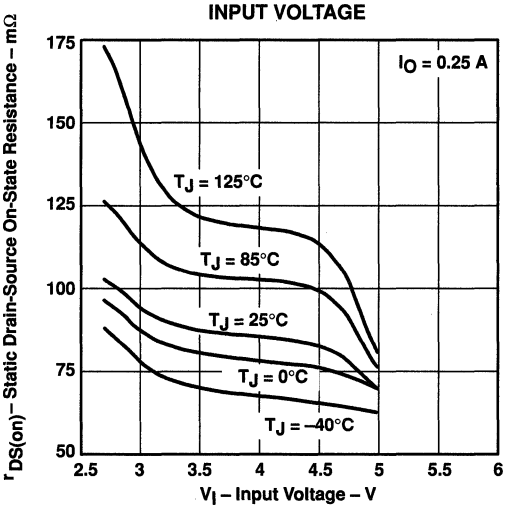


Figure 21

INPUT-TO-OUTPUT VOLTAGE
vs
LOAD CURRENT

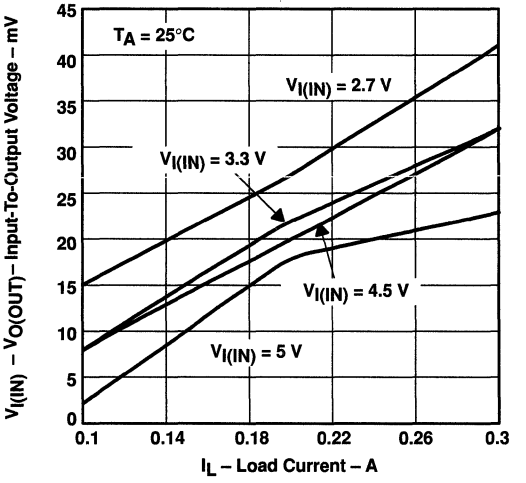


Figure 22

SHORT-CURCUIT OUTPUT CURRENT
vs
INPUT VOLTAGE

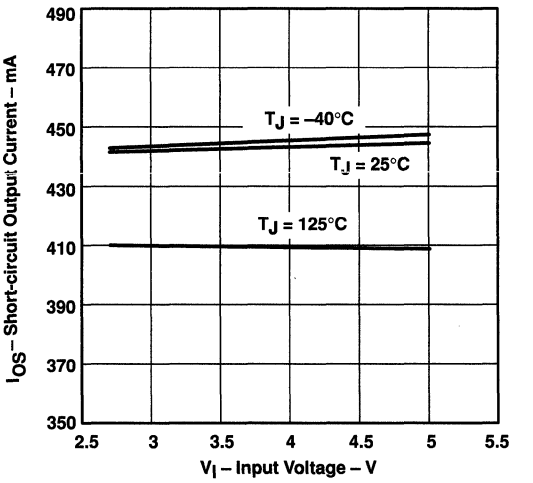


Figure 23

TYPICAL CHARACTERISTICS

THRESHOLD TRIP CURRENT
vs
INPUT VOLTAGE

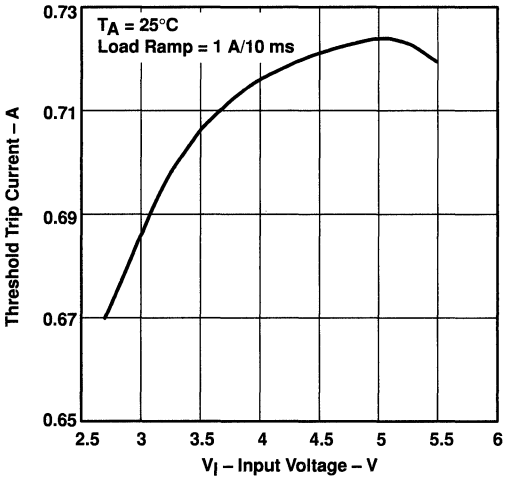


Figure 24

SHORTCIRCUIT OUTPUT CURRENT
vs
JUNCTION TEMPERATURE

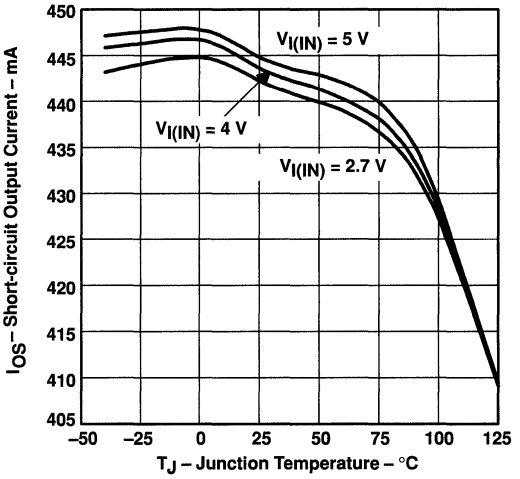


Figure 25

UNDERVOLTAGE LOCKOUT
vs
JUNCTION TEMPERATURE

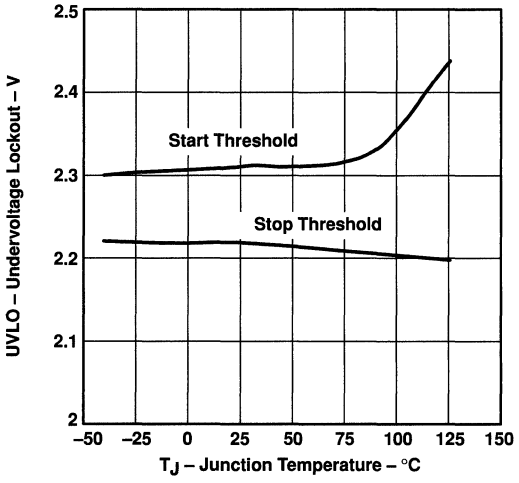


Figure 26

CURRENT-LIMIT RESPONSE
vs
PEAK CURRENT

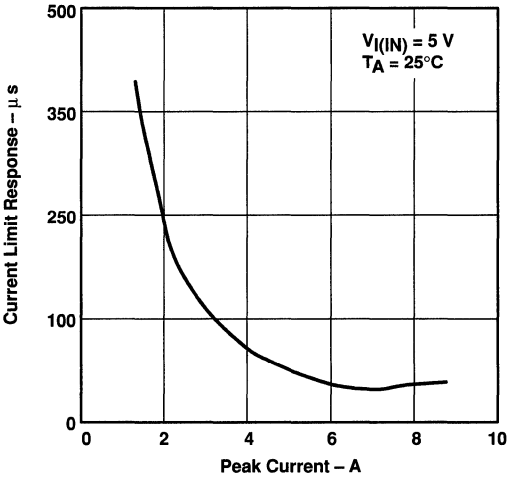


Figure 27

TYPICAL CHARACTERISTICS

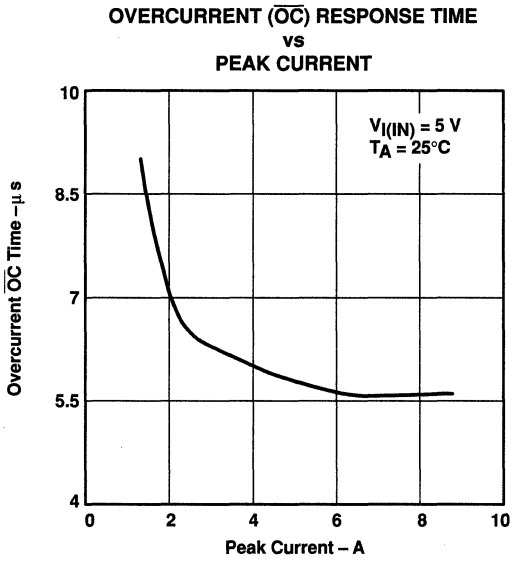


Figure 28

APPLICATION INFORMATION

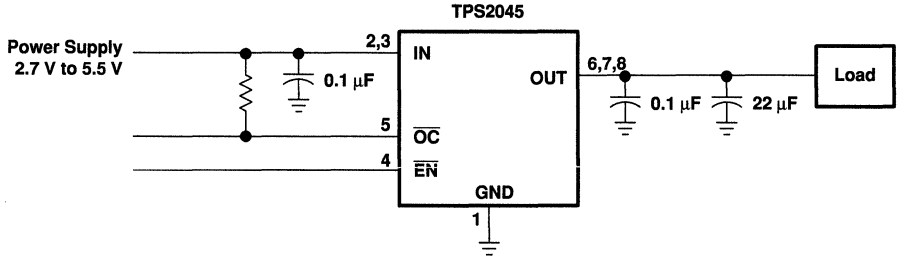


Figure 29. Typical Application

power-supply considerations

A 0.01-µF to 0.1-µF ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-µF to 0.1-µF ceramic capacitor improves the immunity of the device to short-circuit transients.

APPLICATION INFORMATION

overcurrent

A sense FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 6). The TPS2045 and TPS2055 sense the short and immediately switch into a constant-current output.

In the second condition, the short occurs while the device is enabled. At the instant the short occurs, very high currents may flow for a short time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshhold) the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figure 7). The TPS2045 and TPS2055 are capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

$\overline{OC}$ response

The $\overline{OC}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false overcurrent reporting from the inrush current flowing through the device, charging the downstream capacitor. An RC filter of 500 µs (see Figure 30) can be connected to the $\overline{OC}$ pin to reduce false overcurrent reporting caused by hot-plug switching events or extremely high capacitive loads. Using low-ESR electrolytic capacitors on the output lowers the inrush current flow through the device during hot-plug events by providing a low impedance energy source, thereby reducing erroneous overcurrent reporting.

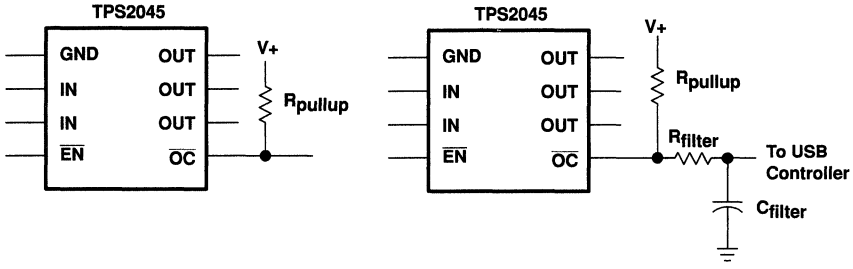


Figure 30. Typical Circuit for $\overline{OC}$ Pin and RC Filter for Damping Inrush $\overline{OC}$ Responses

APPLICATION INFORMATION

power dissipation and junction temperature

The low on-resistance on the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find $r_{DS(on)}$ at the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figure 21. Next, calculate the power dissipation using:

$$P_D = r_{DS(on)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient Temperature °C
$R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W, PDIP = 106°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

thermal protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS2045 and TPS2055 into constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels. The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

undervoltage lockout (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch will be quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO will also keep the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. Upon reinsertion, the power switch will be turned on, with a controlled rise time to reduce EMI and voltage overshoots.

APPLICATION INFORMATION

Universal Serial Bus (USB) applications

The Universal Serial Bus (USB) interface is a 12-Mb/s, or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

Self-powered and bus-powered hubs distribute data and power to downstream functions. The TPS2045 and TPS2055 can provide power-distribution solutions for many of these classes of devices.

Bus-powered hubs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

low-power bus-powered functions and high-power bus-powered functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 µF at power up, the device must implement inrush current limiting (see Figure 31).

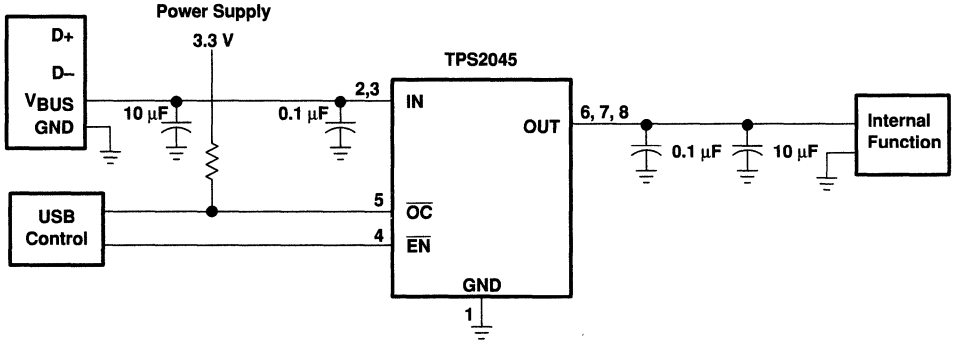


Figure 31. High-Power Bus-Powered Function

APPLICATION INFORMATION

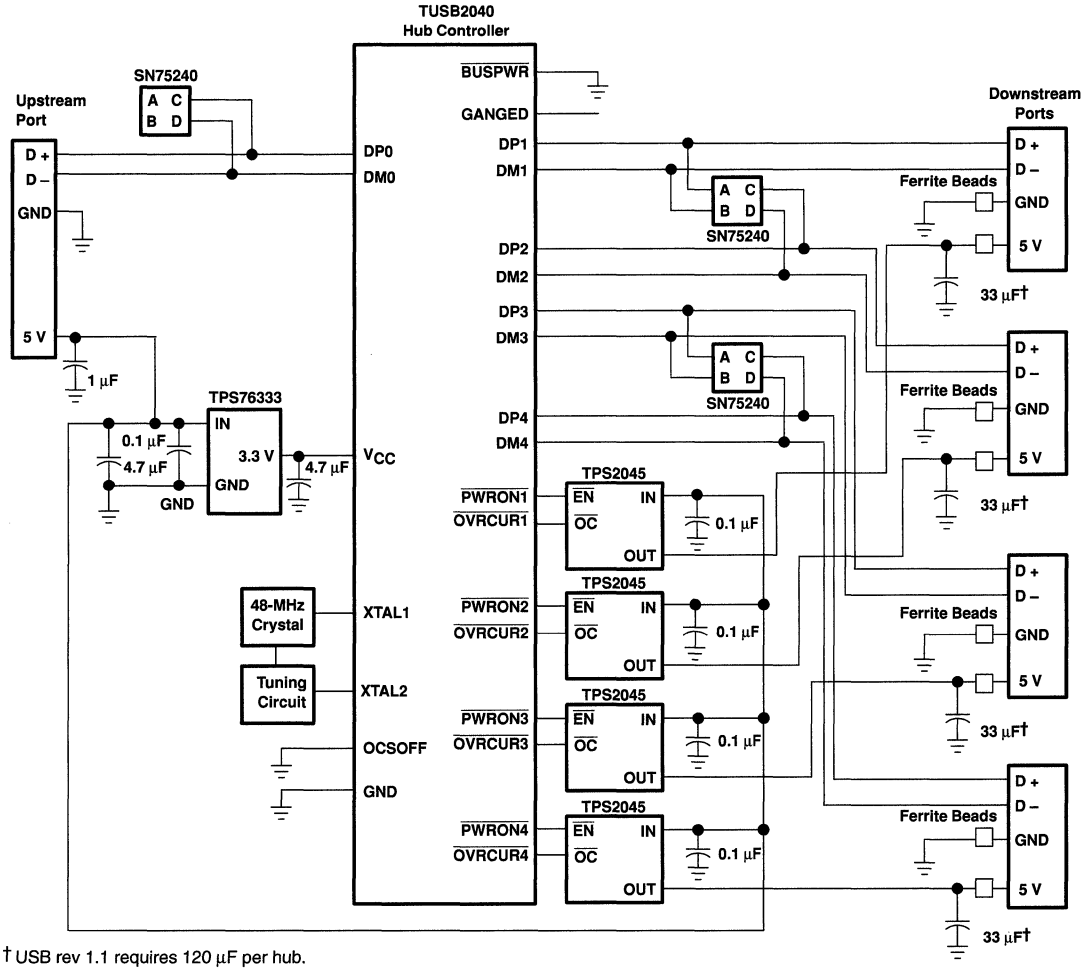
USB power-distribution requirements

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power distribution features must be implemented.

- Bus-Powered Hubs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 μF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

The feature set of the TPS2045 and TPS2055 allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-power hubs, as well as the input ports for bus-power functions (see Figure 32).

APPLICATION INFORMATION



† USB rev 1.1 requires 120 µF per hub.

Figure 32. Bus-Powered Hub Implementation

APPLICATION INFORMATION

generic hot-plug applications (see Figure 33)

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS2045 and TPS2055, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS2045 and TPS2055 also ensures the switch will be off after the card has been removed, and the switch will be off during the next insertion. The UVLO feature guarantees a soft start with a controlled rise time for every insertion of the card or module.

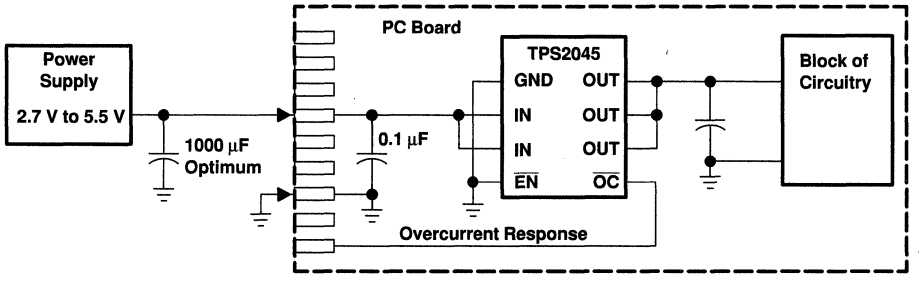


Figure 33. Typical Hot-Plug Implementation

By placing the TPS2045 and TPS2055 between the V_{CC} input and the rest of the circuitry, the input power will reach these devices first after insertion. The typical rise time of the switch is approximately 2.5 ms, providng a slow voltage ramp at the output of the device. This implementaion controls system surge currents and provides a hot-plugging mechanism for any device.

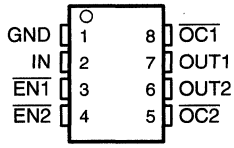
features

- 135-mΩ -Maximum (5-V Input) High-Side MOSFET Switch
- 250 mA Continuous Current per Channel
- Independent Short-Circuit and Thermal Protection With Overcurrent Logic Output
- Operating Range . . . 2.7-V to 5.5-V
- Logic-Level Enable Input
- 2.5-ms Typical Rise Time
- Undervoltage Lockout
- 10 μA Maximum Standby Supply Current
- Bidirectional Switch
- Available in 8-pin SOIC and PDIP Packages
- Ambient Temperature Range, –40°C to 85°C
- 2-kV Human-Body-Model, 200-V Machine-Model ESD Protection

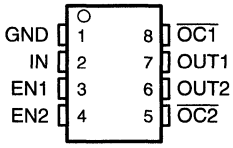
typical applications

- Notebook, Desktop and Palmtop PCs
- Monitors, Keyboards, Scanners, and Printers
- Digital Cameras, Phones, and PBXs
- Hot-Insertion Applications

TPS2046
D OR P PACKAGE
(TOP VIEW)



TPS2056
D OR P PACKAGE
(TOP VIEW)



description

The TPS2046 and TPS2056 dual power-distribution switches are intended for applications where heavy capacitive loads and short circuits are likely. These devices incorporate in single packages two 135-mΩ N-channel MOSFET high-side power switches for power-distribution systems that require multiple power switches. Each switch is controlled by a logic enable compatible with 5-V and 3-V logic. Gate drive is provided by an internal charge pump that controls the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the TPS2046 and TPS2056 limit the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{OCx}$) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch causing the junction temperature to rise, a thermal protection circuit shuts off the switch in overcurrent to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until valid input voltage is present.

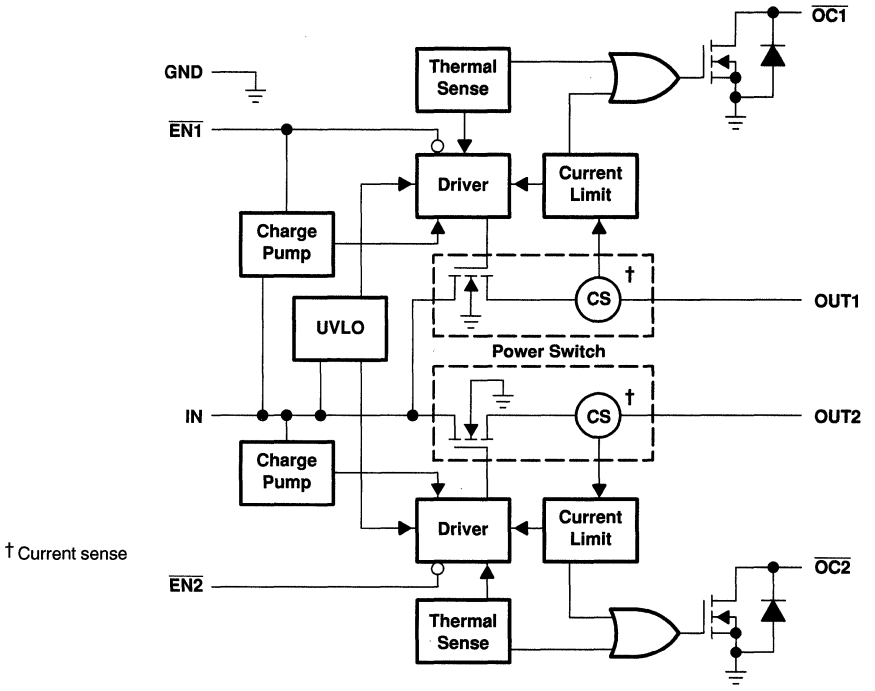
The TPS2046 and TPS2056 are designed to limit at 0.44-A load. These power distribution switches, available in 8-pin small-outline integrated circuit (SOIC) and 8-pin plastic dual-in-line packages (PDIP), operate over an ambient temperature range of –40°C to 85°C.

AVAILABLE OPTIONS

T_A	ENABLE	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A)	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (A)	PACKAGED DEVICES	
				SOIC (D)†	PDIP (P)
–40°C to 85°C	Active low	0.25	0.44	TPS2046D	TPS2046P
–40°C to 85°C	Active high	0.25	0.44	TPS2056D	TPS2056P

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2046DR)

TPS2046 functional block diagram



Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO. D OR P			
	TPS2046	TPS2056		
$\overline{EN1}$	3	–	I	Enable input. Logic low turns on power switch, IN-OUT1.
EN2	4	–	I	Enable input. Logic low turns on power switch, IN-OUT2.
EN1	–	3	I	Enable input. Logic high turns on power switch, IN-OUT1.
EN2	–	4	I	Enable input. Logic high turns on power switch, IN-OUT2.
GND	1	1	I	Ground
IN	2	2	I	Input voltage
$\overline{OC1}$	8	8	O	Overcurrent. Logic output active low, for power switch, IN-OUT1
$\overline{OC2}$	5	5	O	Overcurrent. Logic output active low, for power switch, IN-OUT2
OUT1	7	7	O	Power-switch output
OUT2	6	6	O	Power-switch output

detailed description

power switch

The power switch is an N-channel MOSFET with a maximum on-state resistance of 135 mΩ ($V_{I(IN)}$ = 5 V). Configured as a high-side switch, the power switch prevents current flow from OUTx to IN and IN to OUTx when disabled. The power switch can supply a minimum of 250 mA per switch.

charge pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 4-ms range.

enable ($\overline{\text{ENx}}$ or ENx)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10 μA when a logic high is present on $\overline{\text{ENx}}$ (TPS2046) or a logic low is present on ENx (TPS2056). A logic zero input on $\overline{\text{ENx}}$ or logic high on ENx restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

overcurrent ($\overline{\text{OCx}}$)

The $\overline{\text{OCx}}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed.

current sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant current mode and holds the current constant while varying the voltage on the load.

thermal sense

The TPS2046 and TPS2056 implement a dual-threshold thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition the junction temperature rises. When the die temperature rises to approximately 140°C, the internal thermal sense circuitry checks to determine which power switch is in an overcurrent condition and turns off that switch, thus isolating the fault without interrupting operation of the adjacent power switches. Hysteresis is built into the thermal sense, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed. The ($\overline{\text{OCx}}$) open-drain output is asserted (active low) when overtemperature or overcurrent occurs.

undervoltage lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, $V_{I(IN)}$ (see Note1) ..... –0.3 V to 6 V
Output voltage range, $V_{O(OUTx)}$ (see Note1) ..... –0.3 V to $V_{I(IN)}$ + 0.3 V
Input voltage range, $V_{I(\overline{ENx})}$ or $V_{I(ENx)}$ ..... –0.3 V to 6 V
Continuous output current, $I_{O(OUTx)}$ ..... internally limited
Continuous total power dissipation ..... See Dissipation Rating Table
Operating virtual junction temperature range, T_J ..... –40°C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C
Electrostatic discharge (ESD) protection: Human body model MIL-STD-883C ..... 2 kV
Machine model ..... 0.2 kV

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1175 mW	9.4 mW/°C	752 mW	611 mW

recommended operating conditions

	TPS2046		TPS2056		UNIT
	MIN	MAX	MIN	MAX	
Input voltage, $V_{I(IN)}$	2.7	5.5	2.7	5.5	V
Input voltage, $V_{I(\overline{ENx})}$ or $V_{I(ENx)}$	0	5.5	0	5.5	V
Continuous output current, $I_{O(OUTx)}$	0	250	0	250	mA
Operating virtual junction temperature, T_J	–40	125	–40	125	°C

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $V_{I(\overline{ENx})}$ = 0 V, $V_{I(ENx)}$ = Hi (unless otherwise noted)

power switch

PARAMETER		TEST CONDITIONS†	TPS2046			TPS2056			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$r_{DS(on)}$	Static drain-source on-state resistance, 5-V operation	$V_{I(IN)}$ = 5 V, I_O = 0.1 A, T_J = 25°C		80	95		80	95	mΩ
		$V_{I(IN)}$ = 5 V, I_O = 0.1 A, T_J = 85°C		90	120		90	120	
		$V_{I(IN)}$ = 5 V, I_O = 0.1 A, T_J = 125°C		100	135		100	135	
	Static drain-source on-state resistance, 3.3-V operation	$V_{I(IN)}$ = 3.3 V, I_O = 0.1 A, T_J = 25°C		85	105		85	105	
		$V_{I(IN)}$ = 3.3 V, I_O = 0.1 A, T_J = 85°C		100	135		100	135	
		$V_{I(IN)}$ = 3.3 V, I_O = 0.1 A, T_J = 125°C		115	150		115	150	
t_r	Rise time, output	$V_{I(IN)}$ = 5.5 V, C_L = 1 µF, R_L = 20 Ω, T_J = 25°C		2.5			2.5		ms
		$V_{I(IN)}$ = 2.7 V, C_L = 1 µF, R_L = 20 Ω, T_J = 25°C		3			3		
t_f	Fall time, output	$V_{I(IN)}$ = 5.5 V, C_L = 1 µF, R_L = 20 Ω, T_J = 25°C		4.4			4.4		ms
		$V_{I(IN)}$ = 2.7 V, C_L = 1 µF, R_L = 20 Ω, T_J = 25°C		2.5			2.5		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

enable input $\overline{ENx}$ or ENx

PARAMETER			TEST CONDITIONS	TPS2046			TPS2056			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High-level input voltage		2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V	2			2			V
V_{IL}	Low-level input voltage		4.5 V ≤ $V_{I(IN)}$ ≤ 5.5 V			0.8			0.8	V
			2.7 V≤ $V_{I(IN)}$ ≤ 4.5 V			0.4			0.4	
I_I	Input current	TPS2046	$V_{I(\overline{ENx})}$ = 0 V or $V_{I(\overline{ENx})}$ = $V_{I(IN)}$	–0.5		0.5				µA
		TPS2056	$V_{I(ENx)}$ = $V_{I(IN)}$ or $V_{I(ENx)}$ = 0 V				–0.5		0.5	
t_{on}	Turn-on time		C_L = 100 µF, R_L = 20 Ω			20			20	ms
t_{off}	Turn-off time		C_L = 100 µF, R_L = 20 Ω			40			40	

current limit

PARAMETER		TEST CONDITIONS†	TPS2046			TPS2056			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{OS}	Short-circuit output current	$V_{I(IN)}$ = 5 V, OUT connected to GND, Device enable into short circuit.	0.345	0.44	0.525	0.345	0.44	0.525	A

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $V_{I(\overline{ENx})}$ = 0 V, $V_{I(ENx)}$ = Hi (unless otherwise noted) (continued)

supply current

PARAMETER	TEST CONDITIONS				TPS2046			TPS2056			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
Supply current, low-level output	No Load on OUTx	$V_{I(\overline{ENx})} = V_{I(IN)}$	T_J = 25°C	TPS2046		0.015	1				µA
			–40°C ≤ T_J ≤ 125°C				10				
		$V_{I(ENx)}$ = 0 V	T_J = 25°C	TPS2056					0.015	1	
			–40°C ≤ T_J ≤ 125°C							10	
Supply current, high-level output	No Load on OUTx	$V_{I(\overline{ENx})}$ = 0 V	T_J = 25°C	TPS2046		80	100				µA
			–40°C ≤ T_J ≤ 125°C			100					
		$V_{I(ENx)} = V_{I(IN)}$	T_J = 25°C	TPS2056					80	100	
			–40°C ≤ T_J ≤ 125°C						100		
Leakage current	OUTx connected to ground	$V_{I(\overline{ENx})} = V_{I(IN)}$	–40°C ≤ T_J ≤ 125°C	TPS2046		100					µA
		$V_{I(ENx)}$ = 0 V	–40°C ≤ T_J ≤ 125°C	TPS2056					100		
Reverse leakage current	IN = high impedance	$V_{I(\overline{ENx})}$ = 0 V	T_J = 25°C	TPS2046		0.3					µA
		$V_{I(ENx)}$ = Hi		TPS2056					0.3		

undervoltage lockout

PARAMETER	TEST CONDITIONS	TPS2046			TPS2056			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Low-level input voltage		2		2.5	2		2.5	V
Hysteresis	T_J = 25°C		100			100		mV

overcurrent $\overline{OCx}$

PARAMETER	TEST CONDITIONS	TPS2046			TPS2056			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Sink current†	V_O = 5 V			10			10	mA
Output low voltage	I_O = 5 mA, $V_{OL(\overline{OCx})}$			0.5			0.5	V
Off-state current†	V_O = 5 V, V_O = 3.3 V			1			1	µA

† Specified by design, not production tested.

PARAMETER MEASUREMENT INFORMATION

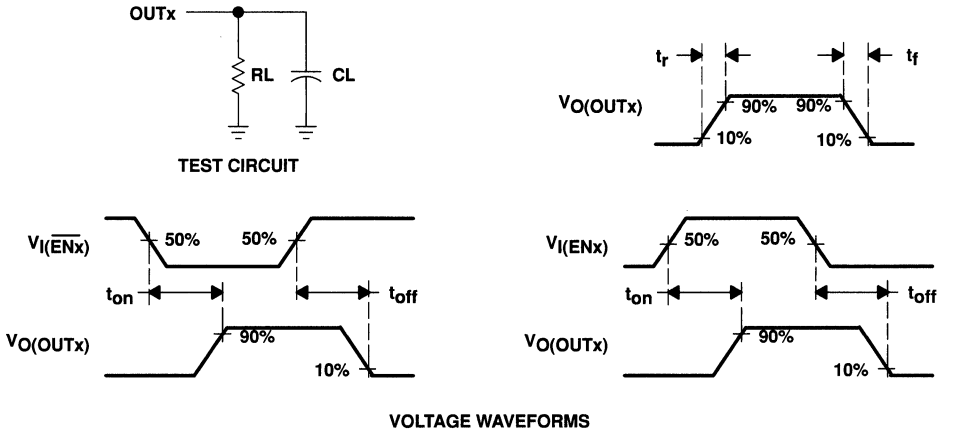


Figure 1. Test Circuit and Voltage Waveforms

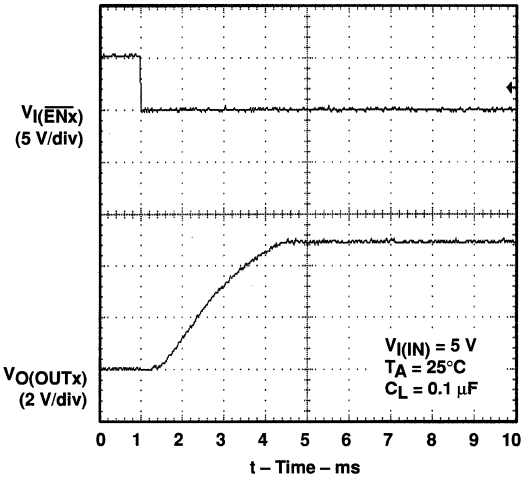


Figure 2. Turnon Delay and Rise Time with 0.1-μF Load

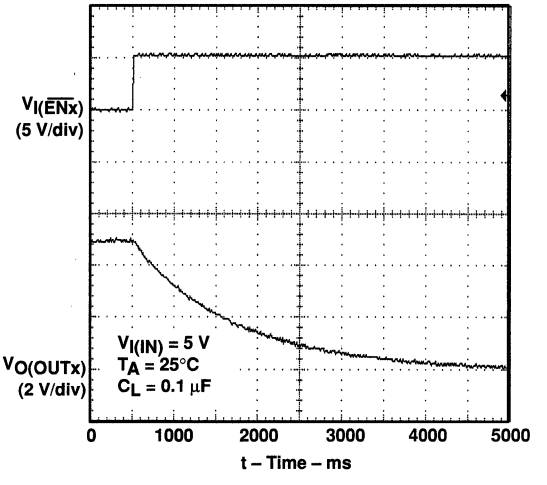


Figure 3. Turnoff Delay and Fall Time with 0.1-μF Load

PARAMETER MEASUREMENT INFORMATION

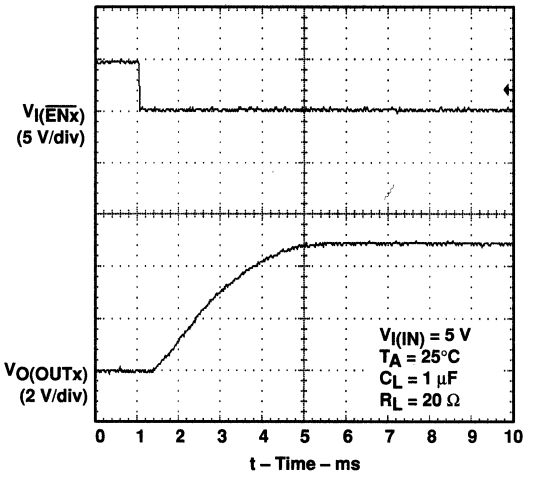


Figure 4. Turnon Delay and Rise Time with 1-μF Load

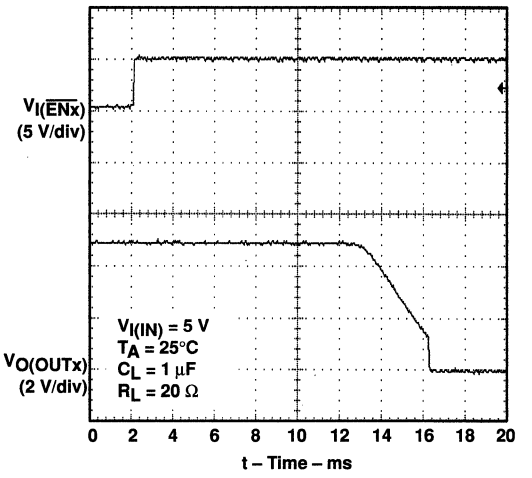


Figure 5. Turnoff Delay and Fall Time with 1-μF Load

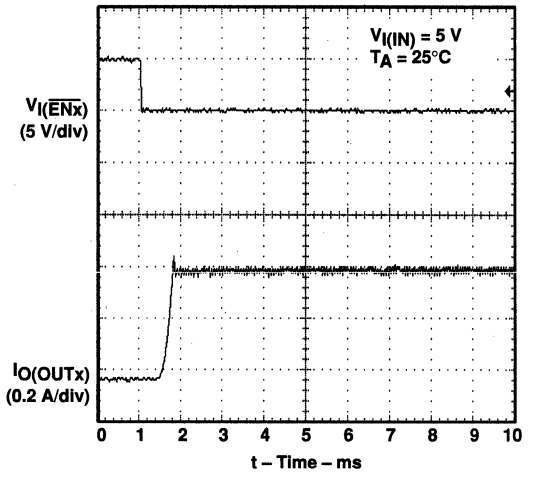


Figure 6. TPS2046, Short-Circuit Current, Device Enabled into Short

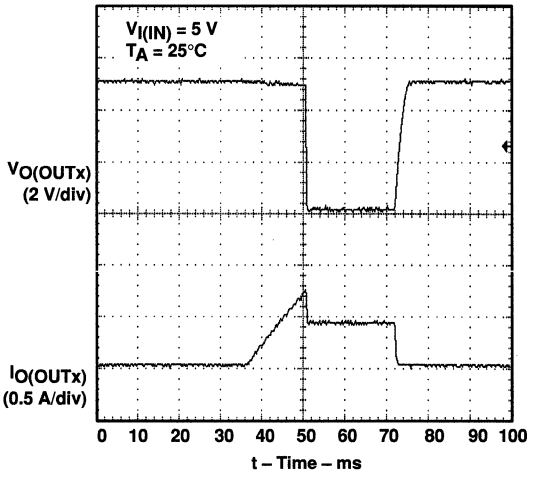


Figure 7. TPS2046, Threshold Trip Current with Ramped Load on Enabled Device

PARAMETER MEASUREMENT INFORMATION

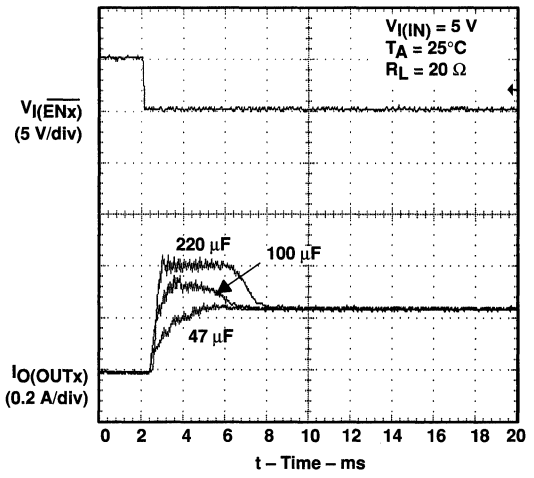


Figure 8. Inrush Current with 220-µF, 100-µF and 47-µF Load Capacitance

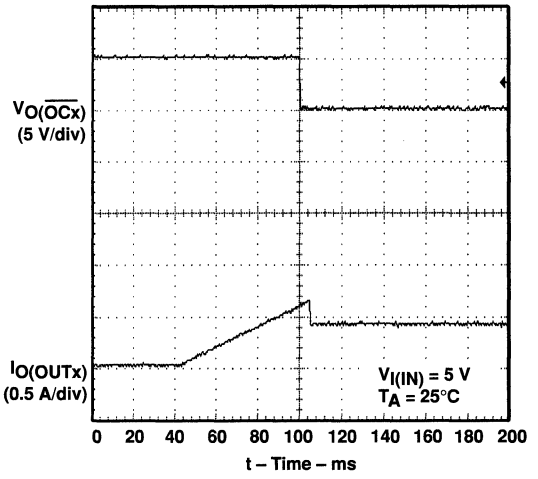


Figure 9. Ramped Load on Enabled Device

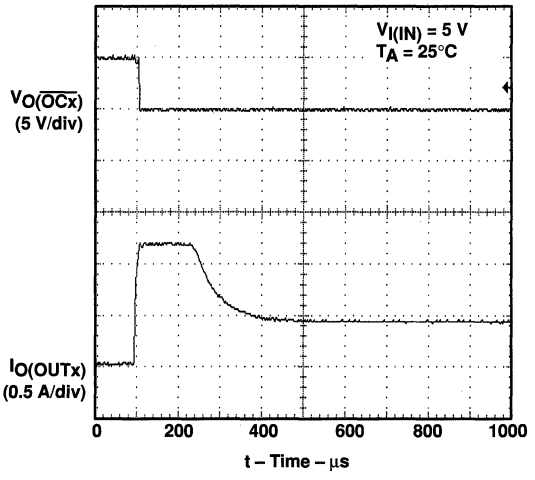


Figure 10. 4-Ω Load Connected to Enabled Device

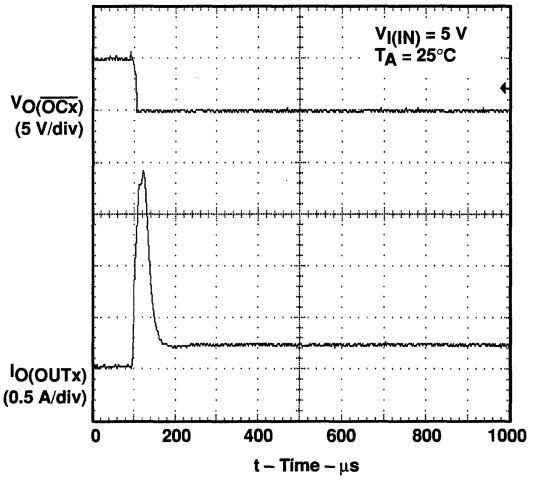


Figure 11. 1-Ω Load Connected to Enabled Device

TYPICAL CHARACTERISTICS

TURNON DELAY
vs
INPUT VOLTAGE

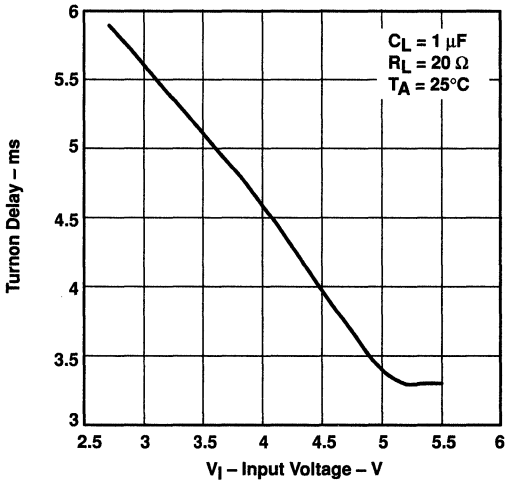


Figure 12

TURNOFF DELAY
vs
INPUT VOLTAGE

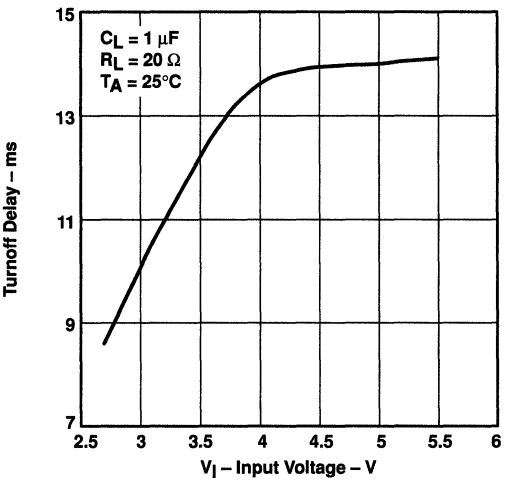


Figure 13

RISE TIME
vs
LOAD CURRENT

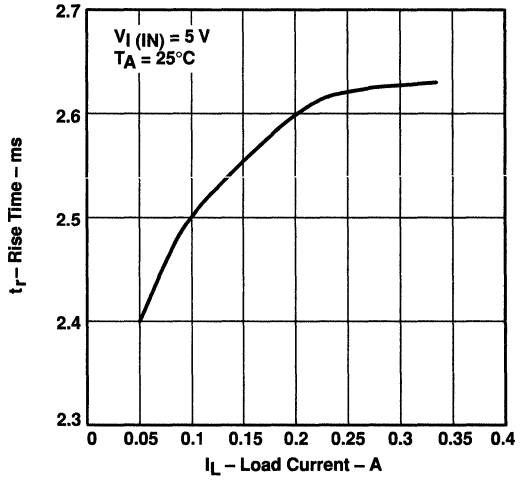


Figure 14

FALL TIME
vs
LOAD CURRENT

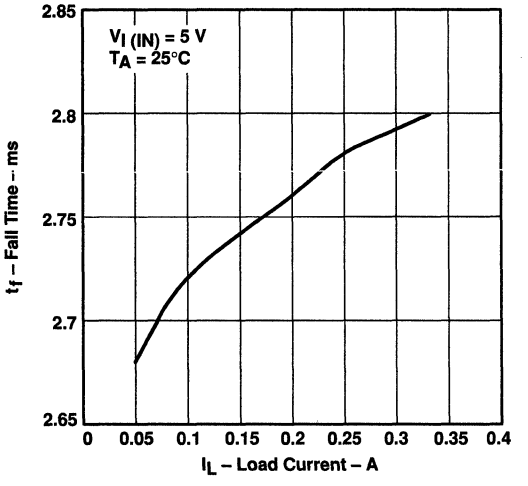


Figure 15

TYPICAL CHARACTERISTICS

SUPPLY CURRENT, OUTPUT ENABLED
vs
JUNCTION TEMPERATURE

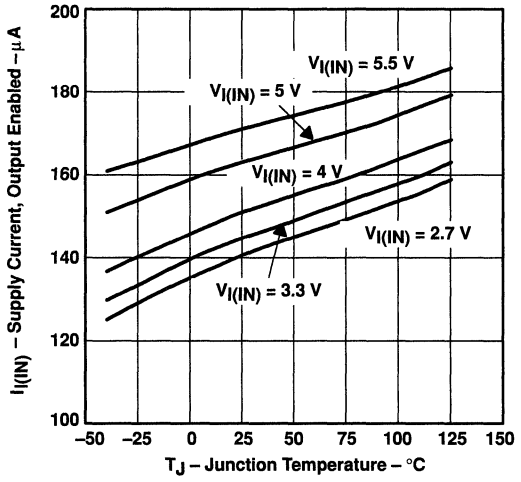


Figure 16

SUPPLY CURRENT, OUTPUT DISABLED
vs
JUNCTION TEMPERATURE

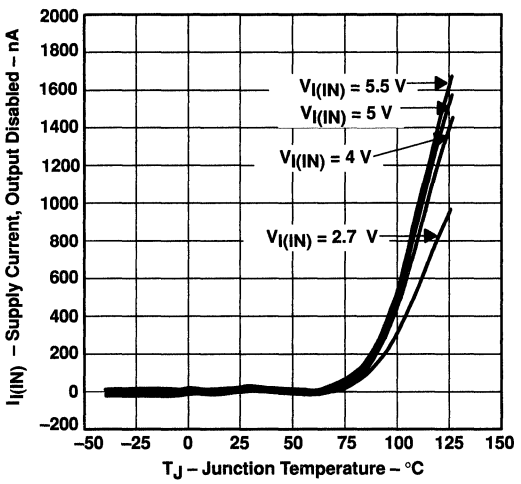


Figure 17

SUPPLY CURRENT, OUTPUT ENABLED
vs
INPUT VOLTAGE

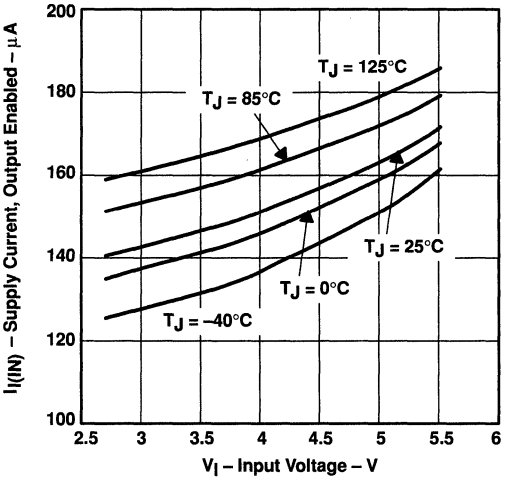


Figure 18

SUPPLY CURRENT, OUTPUT DISABLED
vs
INPUT VOLTAGE

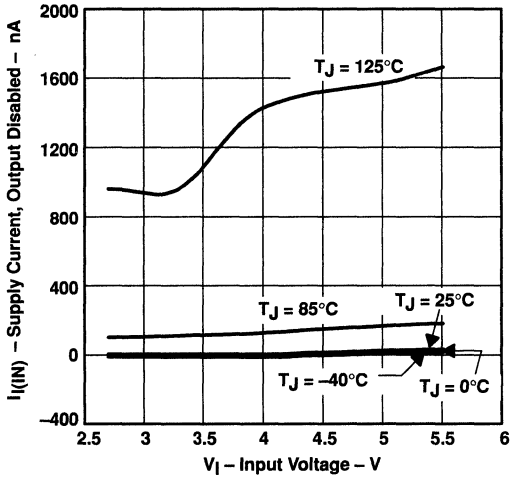


Figure 19

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

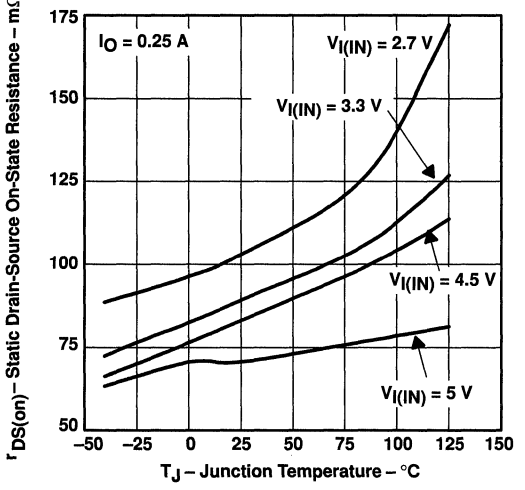


Figure 20

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
INPUT VOLTAGE

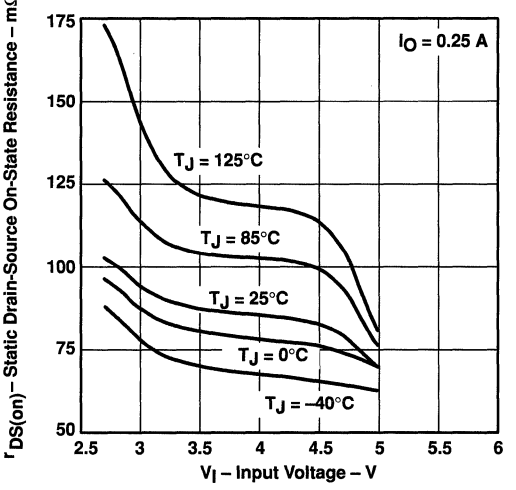


Figure 21

INPUT-TO-OUTPUT VOLTAGE
vs
LOAD CURRENT

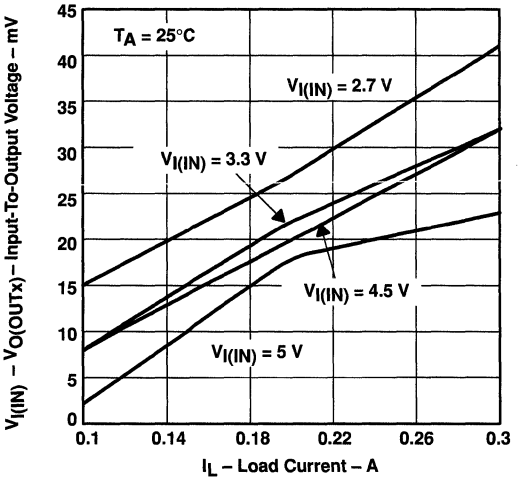


Figure 22

SHORT-CURCUIT OUTPUT CURRENT
vs
INPUT VOLTAGE

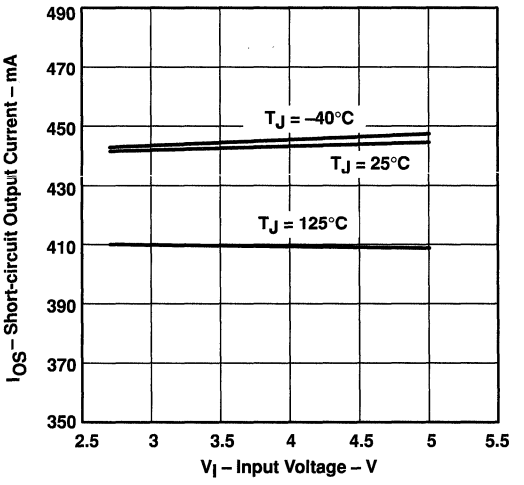


Figure 23

TYPICAL CHARACTERISTICS

THRESHOLD TRIP CURRENT
vs
INPUT VOLTAGE

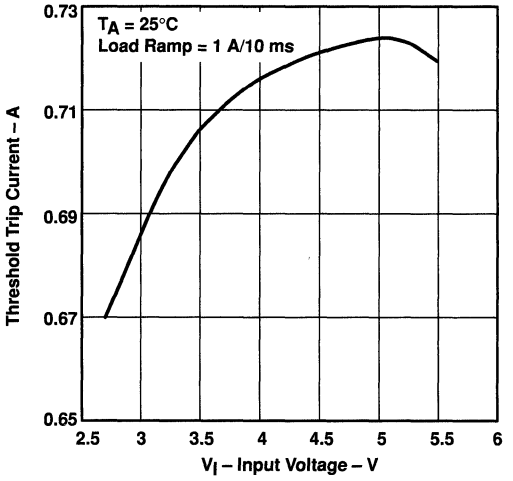


Figure 24

SHORTCIRCUIT OUTPUT CURRENT
vs
JUNCTION TEMPERATURE

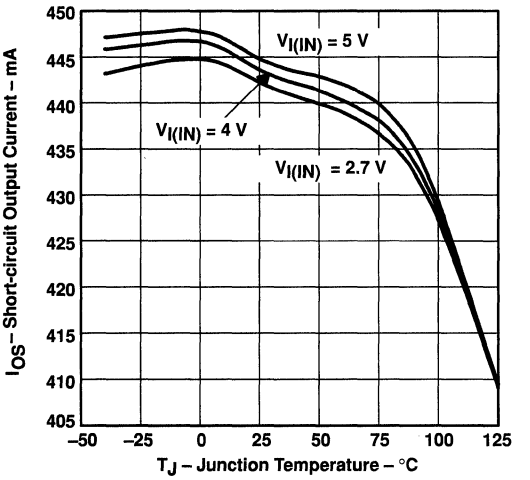


Figure 25

UNDERVOLTAGE LOCKOUT
vs
JUNCTION TEMPERATURE

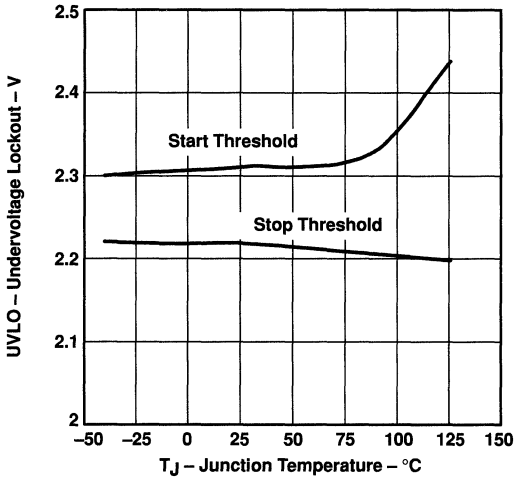


Figure 26

CURRENT-LIMIT RESPONSE
vs
PEAK CURRENT

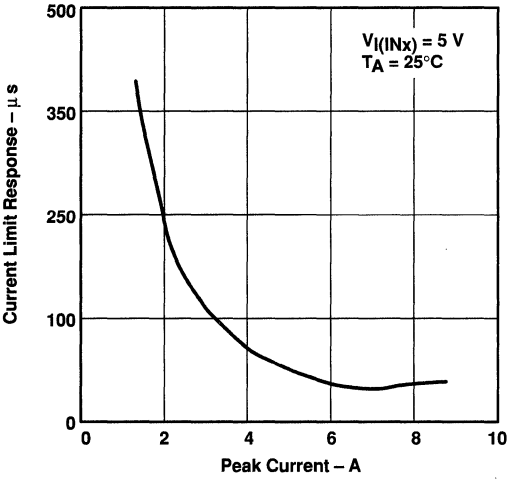


Figure 27

TYPICAL CHARACTERISTICS

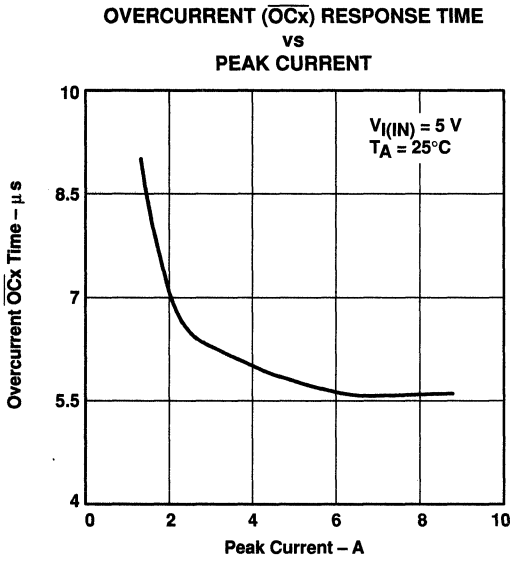


Figure 28

APPLICATION INFORMATION

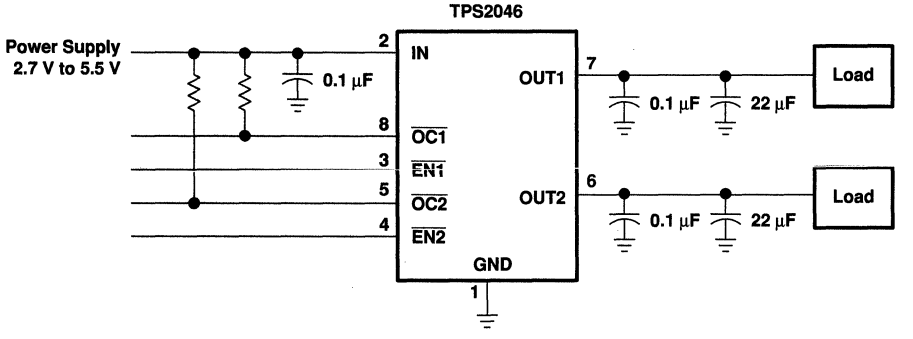


Figure 29. Typical Application

power-supply considerations

A 0.01-µF to 0.1-µF ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-µF to 0.1-µF ceramic capacitor improves the immunity of the device to short-circuit transients.

APPLICATION INFORMATION

overcurrent

A sense FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 6). The TPS2046 and TPS2056 sense the short and immediately switch into a constant-current output.

In the second condition, the short occurs while the device is enabled. At the instant the short occurs, very high currents may flow for a short time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshhold) the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figure 7). The TPS2046 and TPS2056 are capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

$\overline{\text{OCx}}$ response

The $\overline{\text{OCx}}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false overcurrent reporting from the inrush current flowing through the device, charging the downstream capacitor. An RC filter (see Figure 30) can be connected to the $\overline{\text{OCx}}$ pin to reduce false overcurrent reporting caused by hot-plug switching events or extremely high capacitive loads. Using low-ESR electrolytic capacitors on the output lowers the inrush current flow through the device during hot-plug events by providing a low impedance energy source, thereby reducing erroneous overcurrent reporting.

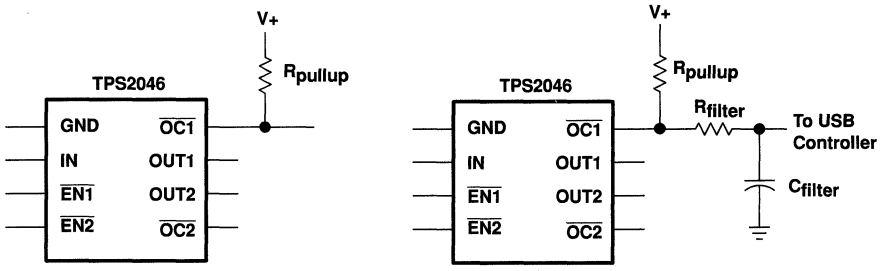


Figure 30. Typical Circuits for $\overline{\text{OC}}$ Pin and RC Filter for Damping Inrush $\overline{\text{OC}}$ Responses

APPLICATION INFORMATION

power dissipation and junction temperature

The low on-resistance on the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistances of these packages are high compared to that of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find $r_{DS(on)}$ at the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figure 21. Next, calculate the power dissipation using:

$$P_D = r_{DS(on)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient Temperature °C
$R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W, PDIP = 106°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

thermal protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS2046 and TPS2056 into constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels. The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

The TPS2046 and TPS2056 implement a dual thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition the junction temperature will rise. Once the die temperature rises to approximately 140°C, the internal thermal sense circuitry checks which power switch is in an overcurrent condition and turns that power switch off, thus isolating the fault without interrupting operation of the adjacent power switch. Should the die temperature exceed the first thermal trip point of 140°C and reach 160°C, both switches turn off. The $\overline{OC}$ open-drain output is asserted (active low) when overtemperature or overcurrent occurs.

undervoltage lockout (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch will be quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO will also keep the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. Upon reinsertion, the power switch will be turned on with a controlled rise time to reduce EMI and voltage overshoots.

APPLICATION INFORMATION

Universal Serial Bus (USB) applications

The Universal Serial Bus (USB) interface is a 12-Mb/s, or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

Self-powered and bus-powered hubs distribute data and power to downstream functions. The TPS2046 and TPS2056 can provide power-distribution solutions for many of these classes of devices.

bus-powered hubs

Bus-powered hubs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

low-power bus-powered functions and high-power bus-powered functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA, and high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 μF at power up, the device must implement inrush current limiting (see Figure 31).

APPLICATION INFORMATION

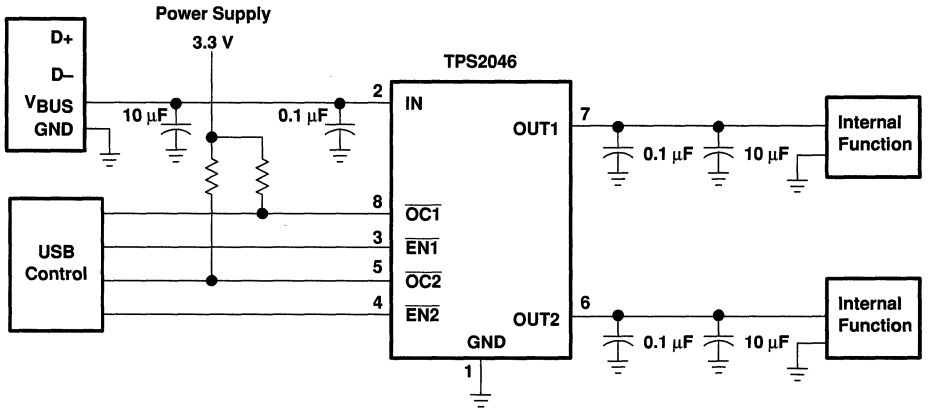


Figure 31. High-Power Bus-Powered Function

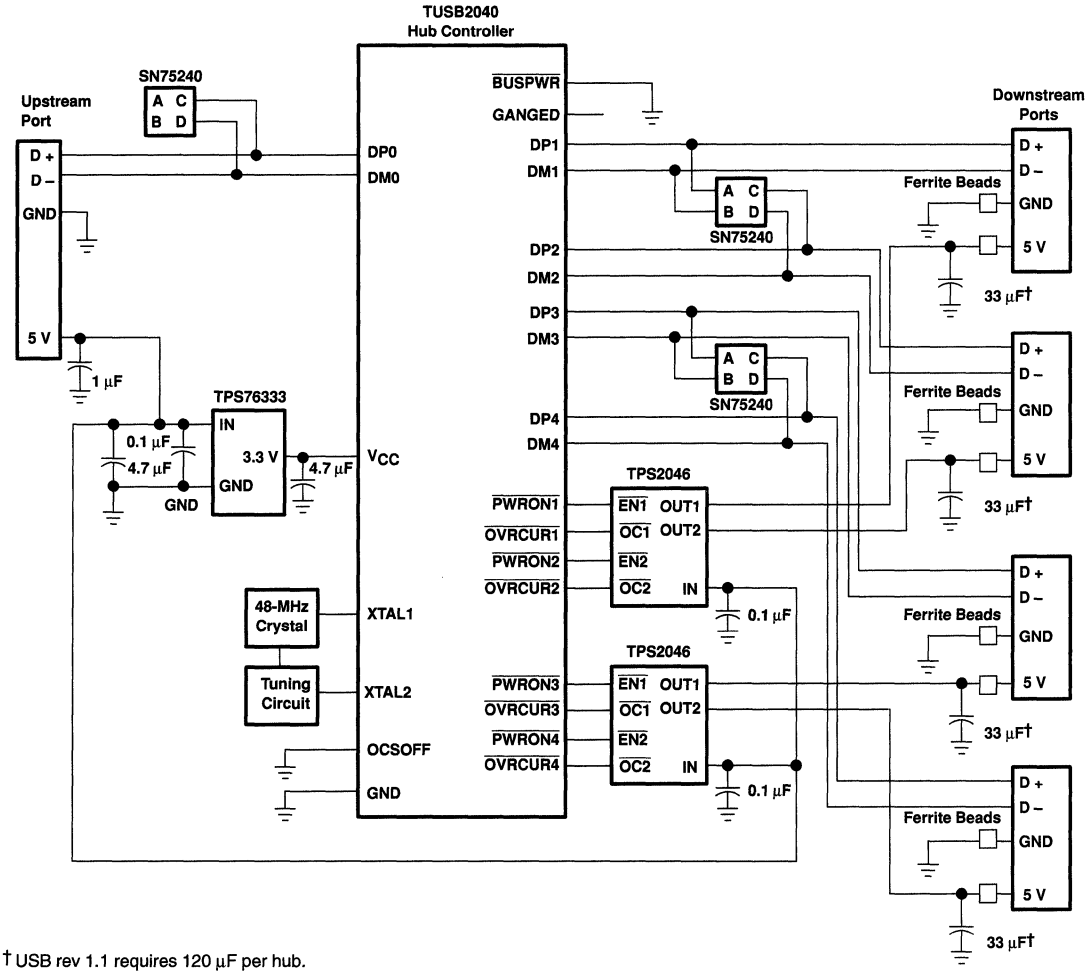
USB power-distribution requirements

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power distribution features must be implemented.

- Bus-Powered Hubs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 µF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

The feature set of the TPS2046 and TPS2056 allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-power hubs, as well as the input ports for bus-power functions (see Figure 32).

APPLICATION INFORMATION



† USB rev 1.1 requires 120 µF per hub.

Figure 32. Bus-Powered Hub Implementation

APPLICATION INFORMATION

generic hot-plug applications (see Figure 33)

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS2046 and TPS2056, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS2046 and TPS2056 also ensures the switch will be off after the card has been removed, and the switch will be off during the next insertion. The UVLO feature guarantees a soft start with a controlled rise time for every insertion of the card or module.

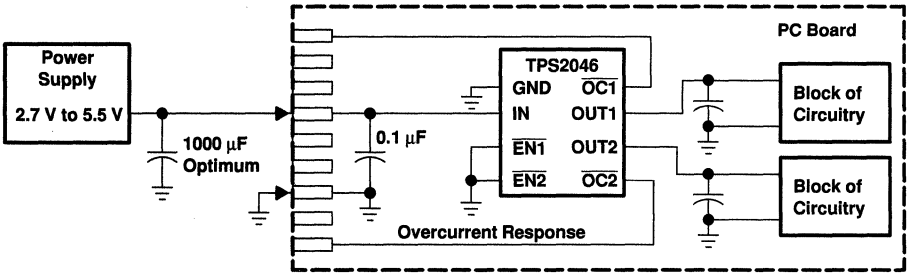


Figure 33. Typical Hot-Plug Implementation

By placing the TPS2046 and TPS2056 between the V_{CC} input and the rest of the circuitry, the input power will reach these devices first after insertion. The typical rise time of the switch is approximately 2.5 ms, providng a slow voltage ramp at the output of the device. This implementaion controls system surge currents and provides a hot-plugging mechanism for any device.

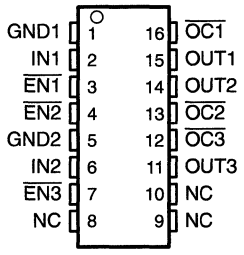
features

- 135-mΩ -Maximum (5-V Input) High-Side MOSFET Switch
- 250 mA Continuous Current per Channel
- Independent Short-Circuit and Thermal Protection With Overcurrent Logic Output
- Operating Range . . . 2.7-V to 5.5-V
- Logic-Level Enable Input
- 2.5-ms Typical Rise Time
- Undervoltage Lockout
- 20 μA Maximum Standby Supply Current
- Bidirectional Switch
- Available in 16-pin SOIC Package
- Ambient Temperature Range, –40°C to 85°C
- 2-kV Human-Body-Model, 200-V Machine-Model ESD Protection

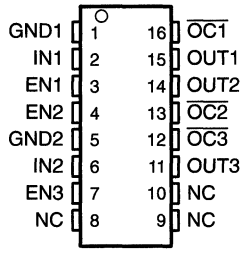
typical applications

- Notebook, Desktop and Palmtop PCs
- Monitors, Keyboards, Scanners, and Printers
- Digital Cameras, Phones, and PBXs
- Hot-Insertion Applications

TPS2047
D PACKAGE
(TOP VIEW)



TPS2057
D PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TPS2047 and TPS2057 triple power-distribution switches are intended for applications where heavy capacitive loads and short circuits are likely. These devices incorporate in single packages three 135-mΩ N-channel MOSFET high-side power switches for power-distribution systems that require multiple power switches. Each switch is controlled by a logic enable compatible with 5-V and 3-V logic. Gate drive is provided by an internal charge pump that controls the power-switch rise times and fall times to minimize current surges during switching. The charge pump, requiring no external components, allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the TPS2047 and TPS2057 limit the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{OCx}$) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch causing the junction temperature to rise, a thermal protection circuit shuts off the switch in overcurrent to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until valid input voltage is present.

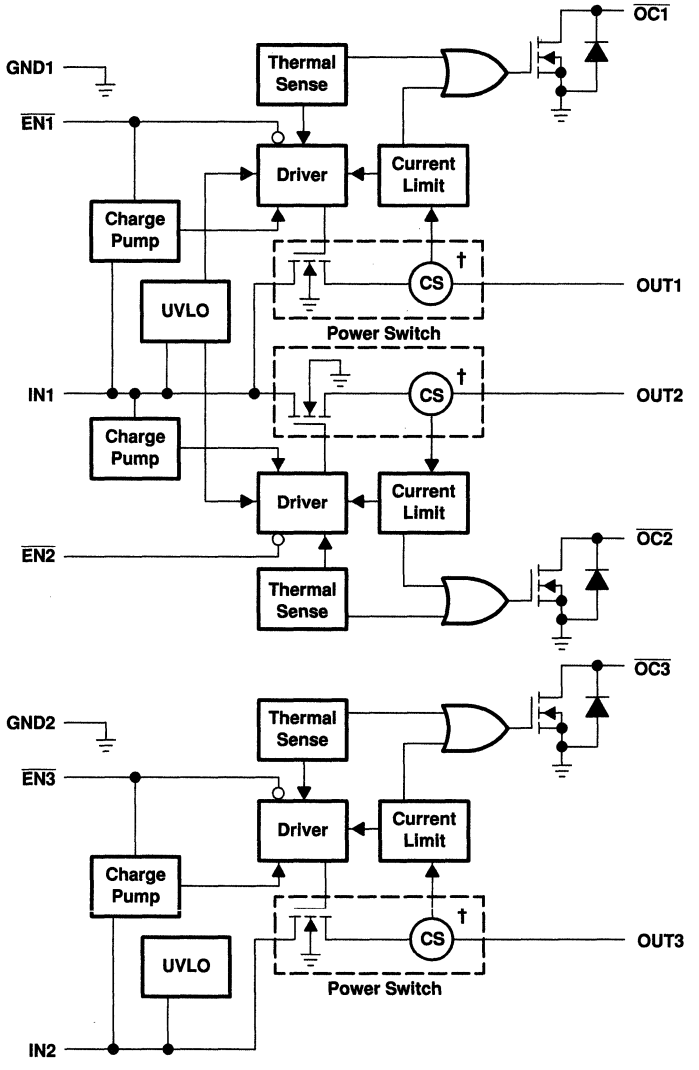
The TPS2047 and TPS2057 are designed to limit at 0.44-A load. These power-distribution switches are available in 16-pin small-outline integrated circuit (SOIC) packages and operate over an ambient temperature range of –40°C to 85°C.

AVAILABLE OPTIONS

T_A	ENABLE	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A)	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (A)	PACKAGED DEVICES SOIC (D)†
–40°C to 85°C	Active low	0.25	0.44	TPS2047D
–40°C to 85°C	Active high	0.25	0.44	TPS2057D

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2047DR)

TPS2047 functional block diagram



† Current sense

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	TPS2047	TPS2057		
$\overline{EN1}$	3	–	I	Enable input. Logic low turns on power switch, IN1-OUT1.
$\overline{EN2}$	4	–	I	Enable input. Logic low turns on power switch, IN1-OUT2.
$\overline{EN3}$	7	–	I	Enable input. Logic low turns on power switch, IN2-OUT3.
EN1	–	3	I	Enable input. Logic high turns on power switch, IN1-OUT1.
EN2	–	4	I	Enable input. Logic high turns on power switch, IN1-OUT2.
EN3	–	7	I	Enable input. Logic high turns on power switch, IN2-OUT3.
GND1	1	1		Ground
GND2	5	5		Ground
IN1	2	2	I	Input voltage
IN2	6	6	I	Input voltage
NC	8, 9, 10	8, 9, 10		No connection
$\overline{OC1}$	16	16	O	Overcurrent. Logic output active low, IN1-OUT1
$\overline{OC2}$	13	13	O	Overcurrent. Logic output active low, IN1-OUT2
$\overline{OC3}$	12	12	O	Overcurrent. Logic output active low, IN2-OUT3
OUT1	15	15	O	Power-switch output, IN1-OUT1
OUT2	14	14	O	Power-switch output, IN1-OUT2
OUT3	11	11	O	Power-switch output, IN2-OUT3

detailed description

power switch

The power switch is an N-channel MOSFET with a maximum on-state resistance of 135 mΩ ($V_{I(INx)}$ = 5 V). Configured as a high-side switch, the power switch prevents current flow from OUTx to INx and INx to OUTx when disabled. The power switch can supply a minimum of 250 mA per switch.

charge pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 4-ms range.

enable ($\overline{\text{ENx}}$ or ENx)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 20 µA when a logic high is present on $\overline{\text{ENx}}$ (TPS2047) or a logic low is present on ENx (TPS2057). A logic zero input on $\overline{\text{ENx}}$ or logic high on ENx restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

overcurrent ($\overline{\text{OCx}}$)

The $\overline{\text{OCx}}$ open drain output is asserted (active low) when an overcurrent or over temperature condition is encountered. The output will remain asserted until the overcurrent or over temperature condition is removed.

current sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant current mode and holds the current constant while varying the voltage on the load.

thermal sense

The TPS2047 and TPS2057 implement a dual-threshold thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition the junction temperature rises. When the die temperature rises to approximately 140°C, the internal thermal sense circuitry checks to determine which power switch is in an overcurrent condition and turns off that switch, thus, isolating the fault without interrupting operation of the adjacent power switches. Hysteresis is built into the thermal sense, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed. The ($\overline{\text{OCx}}$) open-drain output is asserted (active low) when overtemperature or overcurrent occurs.

undervoltage lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, $V_{I(INx)}$ (see Note1) ..... –0.3 V to 6 V
Output voltage range, $V_{O(OUTx)}$ (see Note1) ..... –0.3 V to $V_{I(INx)}$ + 0.3 V
Input voltage range, $V_{I(\overline{ENx})}$ or $V_{I(ENx)}$ ..... –0.3 V to 6 V
Continuous output current, $I_{O(OUTx)}$ ..... Internally limited
Continuous total power dissipation ..... See Dissipation Rating Table
Operating virtual junction temperature range, T_J ..... –40°C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C
Electrostatic discharge (ESD) protection: Human body model MIL-STD-883C ..... 2 kV
Machine model ..... 0.2 kV

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW

recommended operating conditions

	TPS2047		TPS2057		UNIT
	MIN	MAX	MIN	MAX	
Input voltage, $V_{I(INx)}$	2.7	5.5	2.7	5.5	V
Input voltage, $V_{I(\overline{ENx})}$ or $V_{I(ENx)}$	0	5.5	0	5.5	V
Continuous output current, $I_{O(OUTx)}$	0	250	0	250	mA
Operating virtual junction temperature, T_J	–40	125	–40	125	°C

electrical characteristics over recommended operating junction temperature range, $V_{I(INx)}$= 5.5 V, I_O = rated current, $V_{I(\overline{ENx})}$ = 0 V, $V_{I(ENx)}$ = Hi (unless otherwise noted)

power switch

PARAMETER		TEST CONDITIONS†	TPS2047			TPS2057			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$r_{DS(on)}$	Static drain-source on-state resistance, 5-V operation	$V_{I(INx)}$ = 5 V, T_J = 25°C, I_O = 0.25 A		80	95		80	95	mΩ
		$V_{I(INx)}$ = 5 V, T_J = 85°C, I_O = 0.25 A		90	120		90	120	
		$V_{I(INx)}$ = 5 V, T_J = 125°C, I_O = 0.25 A		100	135		100	135	
	Static drain-source on-state resistance, 3.3-V operation	$V_{I(INx)}$ = 3.3 V, T_J = 25°C, I_O = 0.25 A		85	105		85	105	
		$V_{I(INx)}$ = 3.3 V, T_J = 85°C, I_O = 0.25 A		100	135		100	135	
		$V_{I(INx)}$ = 3.3 V, T_J = 125°C, I_O = 0.25 A		115	150		115	150	
t_r	Rise time, output	$V_{I(INx)}$ = 5.5 V, T_J = 25°C, C_L = 1 µF, R_L = 20 Ω		2.5			2.5		ms
		$V_{I(INx)}$ = 2.7 V, T_J = 25°C, C_L = 1 µF, R_L = 20 Ω		3			3		
t_f	Fall time, output	$V_{I(INx)}$ = 5.5 V, T_J = 25°C, C_L = 1 µF, R_L = 20 Ω		4.4			4.4		ms
		$V_{I(INx)}$ = 2.7 V, T_J = 25°C, C_L = 1 µF, R_L = 20 Ω		2.5			2.5		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

enable input $\overline{ENx}$ or ENx

PARAMETER			TEST CONDITIONS	TPS2047			TPS2057			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High–level input voltage		2.7 V ≤ $V_{I(INx)}$ ≤ 5.5 V	2			2			V
V_{IL}	Low–level input voltage		4.5 V ≤ $V_{I(INx)}$ ≤ 5.5 V			0.8			0.8	V
			2.7 V≤ $V_{I(INx)}$ ≤ 4.5 V			0.4			0.4	
I_I	Input current	TPS2047	$V_{I(\overline{ENx})}$ = 0 V or $V_{I(\overline{ENx})}$ = $V_{I(INx)}$	–0.5		0.5				µA
		TPS2057	$V_{I(ENx)}$ = $V_{I(INx)}$ or $V_{I(ENx)}$ = 0 V				–0.5		0.5	
t_{on}	Turnon time		C_L = 100 µF, R_L = 20 Ω			20			20	ms
t_{off}	Turnoff time		C_L = 100 µF, R_L = 20 Ω			40			40	

current limit

PARAMETER		TEST CONDITIONS†	TPS2047			TPS2057			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{OS}	Short-circuit output current	$V_{I(INx)}$ = 5 V, OUT connected to GND, Device enable into short circuit	0.345	0.44	0.525	0.345	0.44	0.525	A

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics over recommended operating junction temperature range, $V_{I(INx)}$= 5.5 V, I_O = rated current, $V_{I(\overline{ENx})}$ = 0 V, $V_{I(ENx)}$ = Hi (unless otherwise noted) (continued)

supply current

PARAMETER	TEST CONDITIONS				TPS2047			TPS2057			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
Supply current, low-level output	No Load on OUTx	$V_{I(\overline{ENx})} = V_{I(INx)}$	T_J = 25°C	TPS2047		0.03	2				µA
			–40°C ≤ T_J ≤ 125°C				20				
		$V_{I(ENx)}$ = 0 V	T_J = 25°C	TPS2057					0.03	2	
			–40°C ≤ T_J ≤ 125°C							20	
Supply current, high-level output	No Load on OUTx	$V_{I(\overline{ENx})}$ = 0 V	T_J = 25°C	TPS2047		160	200				µA
			–40°C ≤ T_J ≤ 125°C			200					
		$V_{I(ENx)} = V_{I(INx)}$	T_J = 25°C	TPS2057					160	200	
			–40°C ≤ T_J ≤ 125°C						200		
Leakage current	OUTx connected to ground	$V_{I(\overline{ENx})} = V_{I(INx)}$	–40°C ≤ T_J ≤ 125°C	TPS2047		200					µA
		$V_{I(ENx)}$ = 0 V		TPS2057					200		
Reverse leakage current	INx = high impedance	$V_{I(\overline{ENx})}$ = 0 V	T_J = 25°C	TPS2047		0.3					µA
		$V_{I(ENx)}$ = Hi		TPS2057					0.3		

undervoltage lockout

PARAMETER	TEST CONDITIONS	TPS2047			TPS2057			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Low-level input voltage		2		2.5	2		2.5	V
Hysteresis	T_J = 25°C		100			100		mV

overcurrent $\overline{OCx}$

PARAMETER	TEST CONDITIONS	TPS2047			TPS2057			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Sink current†	V_O = 5 V			10			10	mA
Output low voltage	I_O = 5 mA, $V_{OL(\overline{OCx})}$			0.5			0.5	V
Off-state current†	V_O = 5 V, V_O = 3.3 V			1			1	µA

† Specified by design, not production tested.

PARAMETER MEASUREMENT INFORMATION

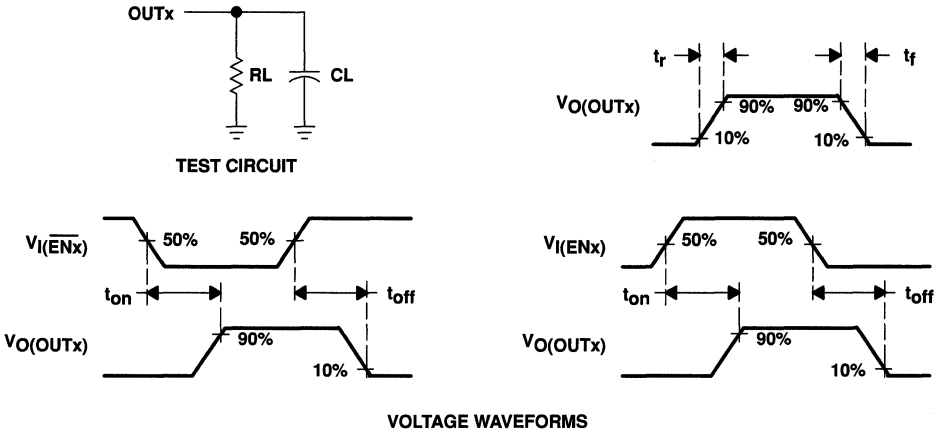


Figure 1. Test Circuit and Voltage Waveforms

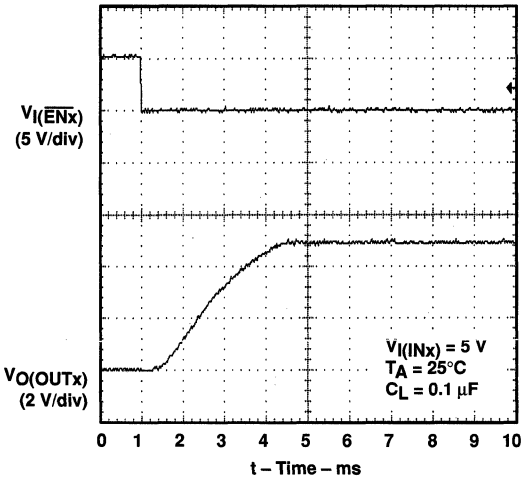


Figure 2. Turnon Delay and Rise Time with 0.1-μF Load

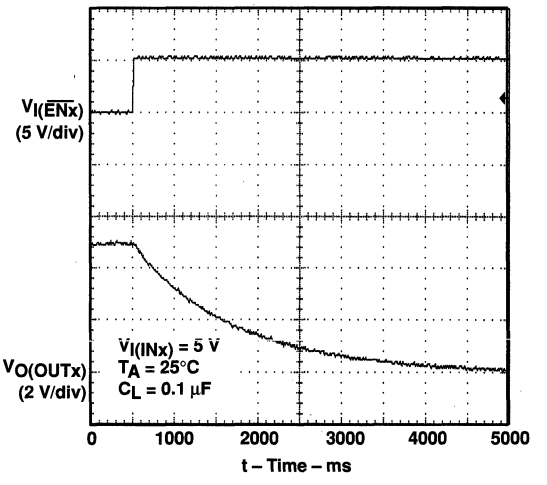


Figure 3. Turnoff Delay and Fall Time with 0.1-μF Load

PARAMETER MEASUREMENT INFORMATION

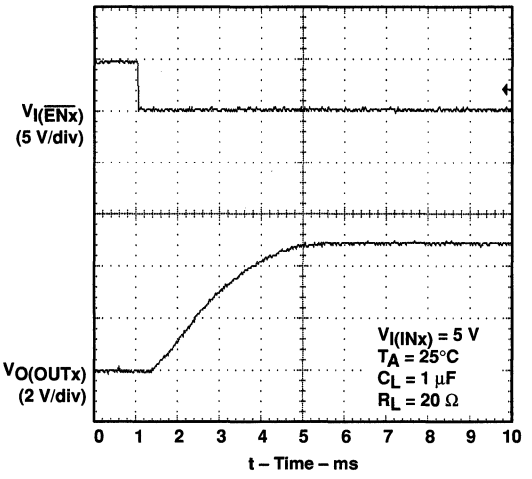


Figure 4. Turnon Delay and Rise Time with 1-μF Load

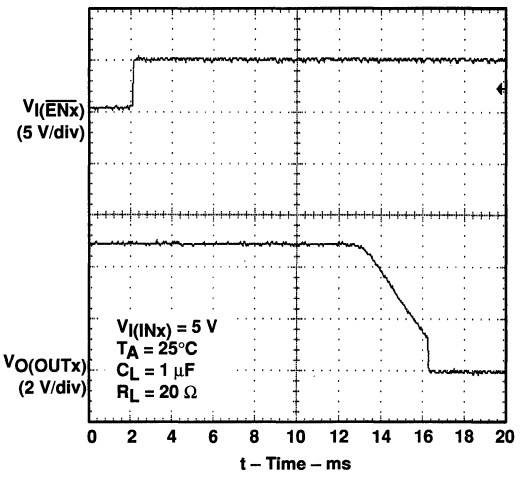


Figure 5. Turnoff Delay and Fall Time with 1-μF Load

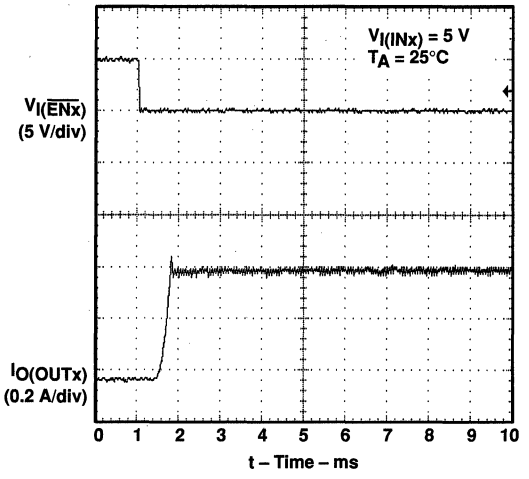


Figure 6. TPS2047, Short-Circuit Current, Device Enabled into Short

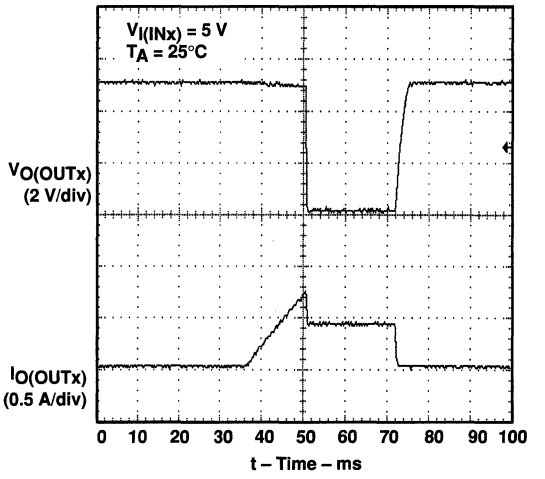


Figure 7. TPS2047, Threshold Trip Current with Ramped Load on Enabled Device

PARAMETER MEASUREMENT INFORMATION

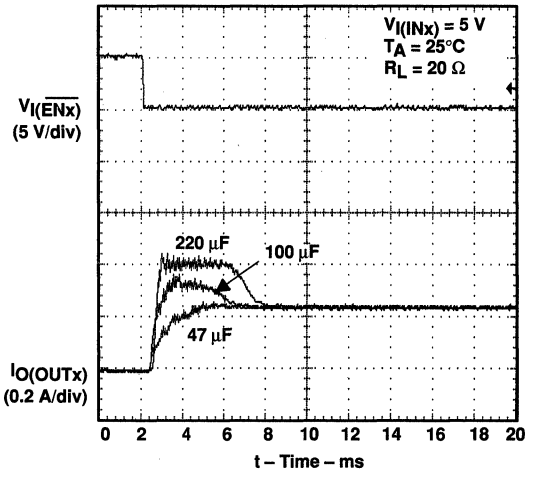


Figure 8. Inrush Current with 220-μF, 100-μF and 47-μF Load Capacitance

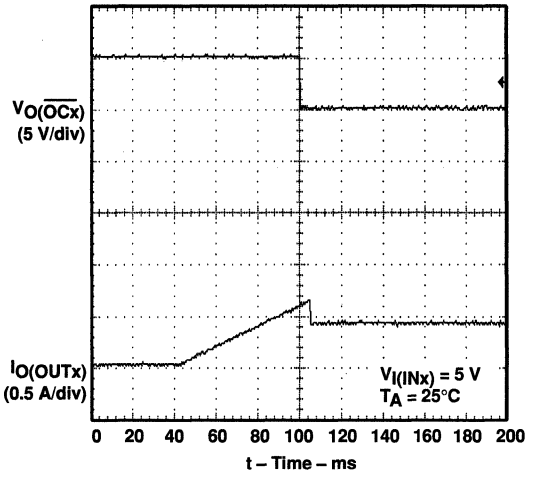


Figure 9. Ramped Load on Enabled Device

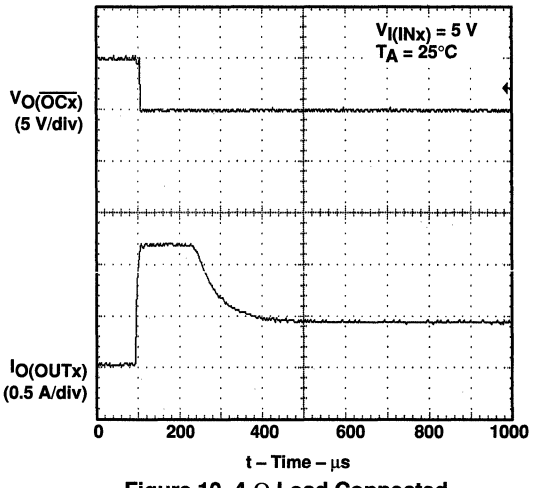


Figure 10. 4-Ω Load Connected to Enabled Device

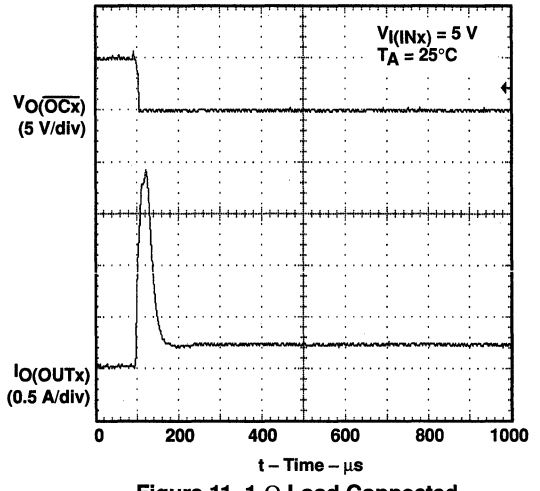


Figure 11. 1-Ω Load Connected to Enabled Device

TYPICAL CHARACTERISTICS

TURNON DELAY
vs
INPUT VOLTAGE

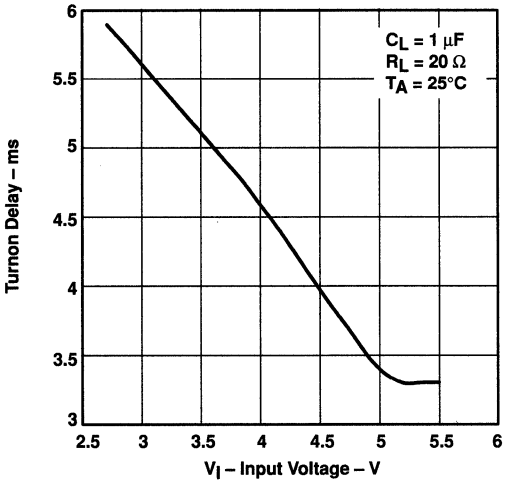


Figure 12

TURNOFF DELAY
vs
INPUT VOLTAGE

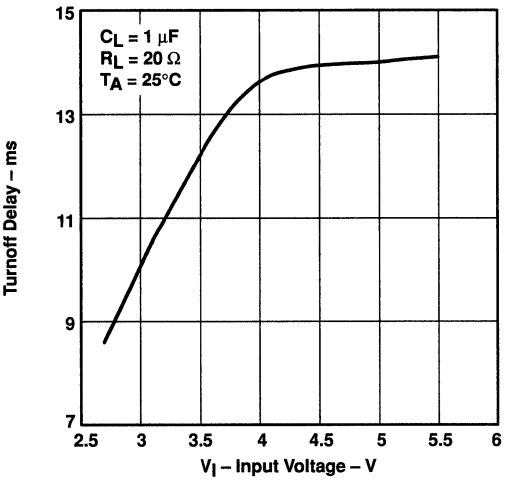


Figure 13

RISE TIME
vs
LOAD CURRENT

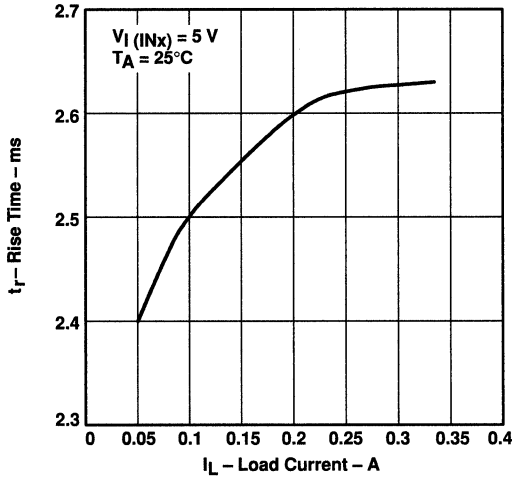


Figure 14

FALL TIME
vs
LOAD CURRENT

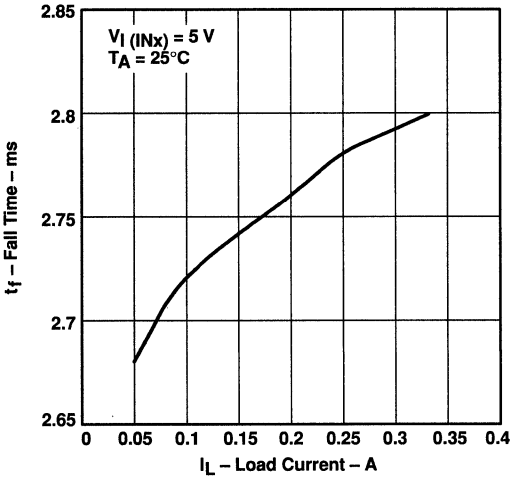


Figure 15

TYPICAL CHARACTERISTICS

SUPPLY CURRENT, OUTPUT ENABLED
vs
JUNCTION TEMPERATURE

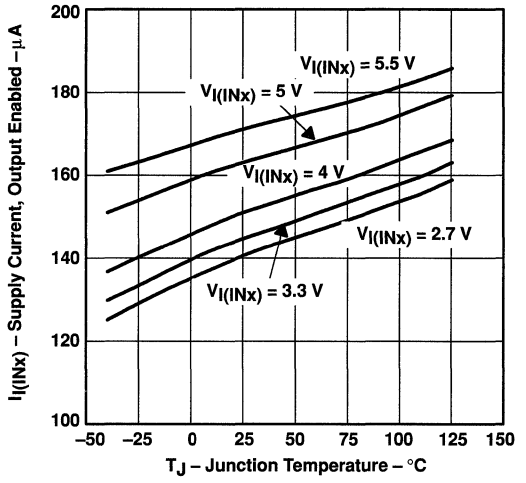


Figure 16

SUPPLY CURRENT, OUTPUT DISABLED
vs
JUNCTION TEMPERATURE

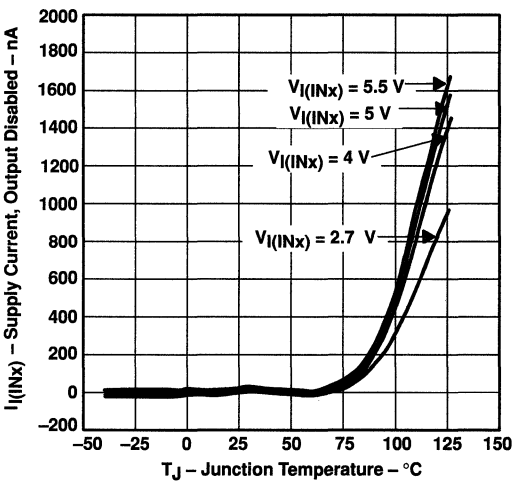


Figure 17

SUPPLY CURRENT, OUTPUT ENABLED
vs
INPUT VOLTAGE

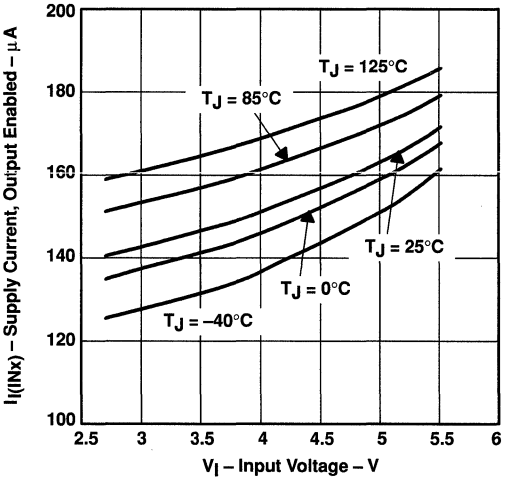


Figure 18

SUPPLY CURRENT, OUTPUT DISABLED
vs
INPUT VOLTAGE

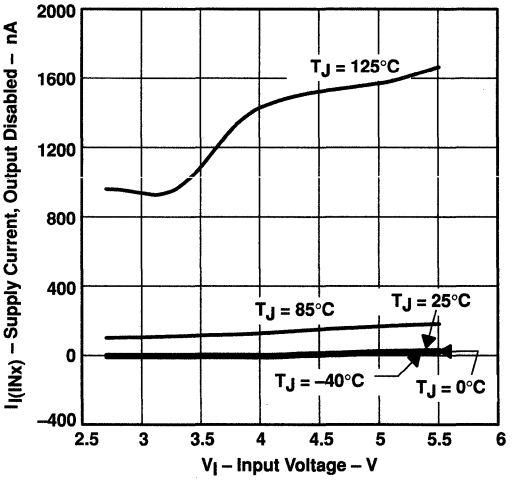


Figure 19

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

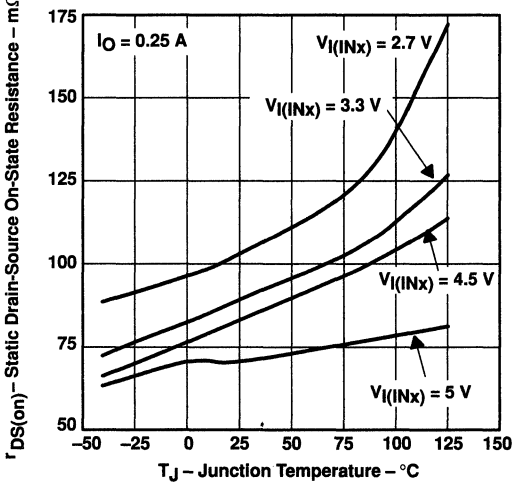


Figure 20

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
INPUT VOLTAGE

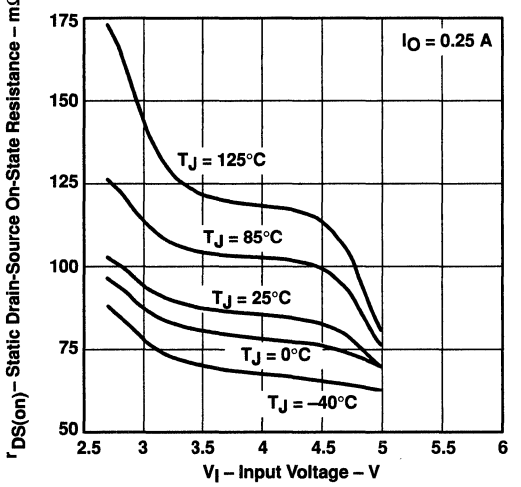


Figure 21

INPUT-TO-OUTPUT VOLTAGE
vs
LOAD CURRENT

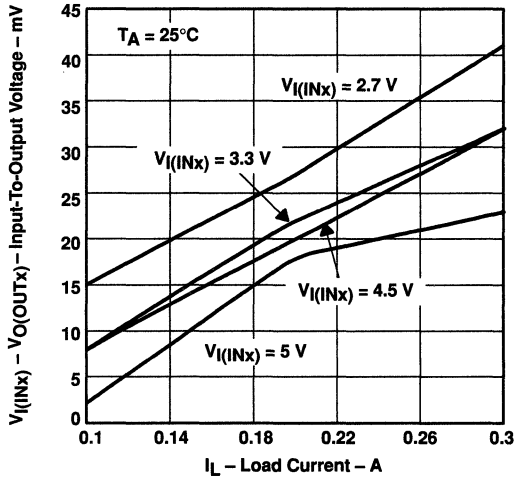


Figure 22

SHORT-CURCUIT OUTPUT CURRENT
vs
INPUT VOLTAGE

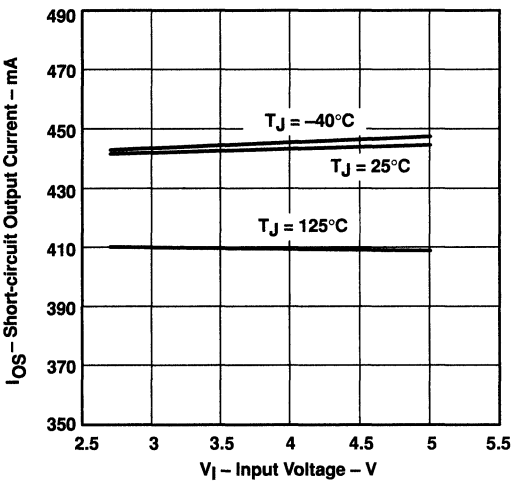


Figure 23

TYPICAL CHARACTERISTICS

THRESHOLD TRIP CURRENT
vs
INPUT VOLTAGE

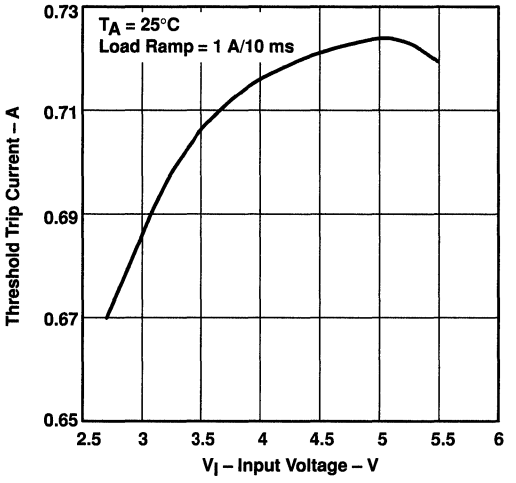


Figure 24

SHORTCIRCUIT OUTPUT CURRENT
vs
JUNCTION TEMPERATURE

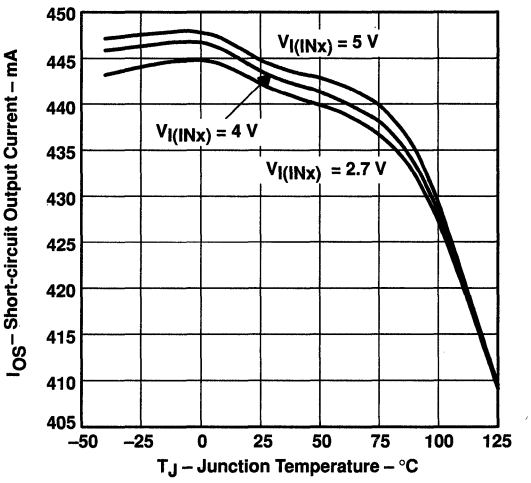


Figure 25

UNDERVOLTAGE LOCKOUT
vs
JUNCTION TEMPERATURE

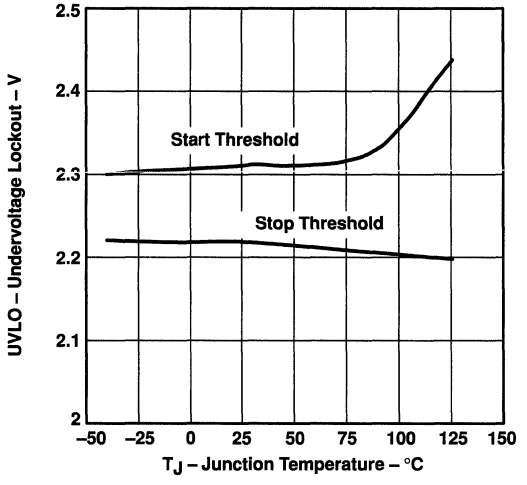


Figure 26

CURRENT-LIMIT RESPONSE
vs
PEAK CURRENT

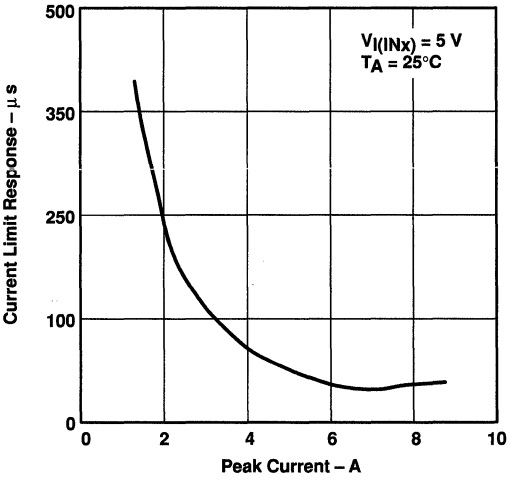


Figure 27

TYPICAL CHARACTERISTICS

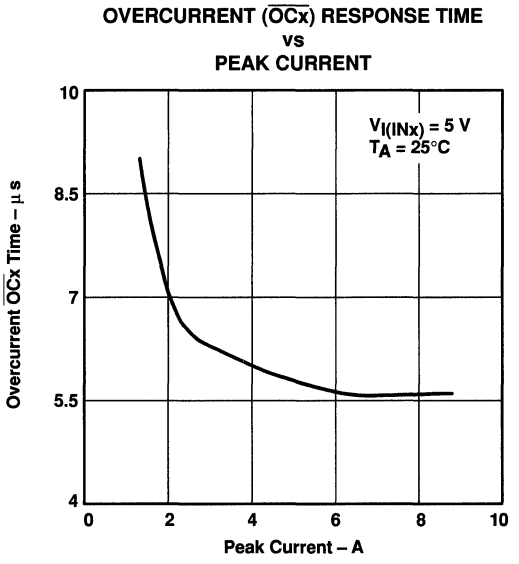


Figure 28

APPLICATION INFORMATION

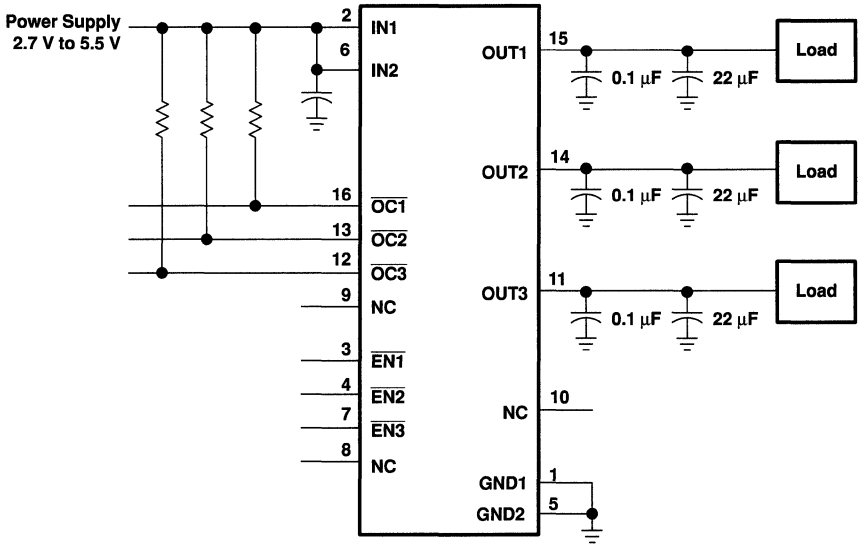


Figure 29. Typical Application

APPLICATION INFORMATION

power supply considerations

A 0.01-μF to 0.1-μF ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-μF to 0.1-μF ceramic capacitor improves the immunity of the device to short-circuit transients.

overcurrent

A sense FET checks for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(INx)}$ has been applied (see Figure 6). The TPS2047 and TPS2057 sense the short and immediately switch into a constant-current output.

In the second condition, the short occurs while the device is enabled. At the instant the short occurs, very high currents may flow for a short time before the current-limit circuit can react . After the current-limit circuit has tripped (reached the overcurrent trip threshhold) the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figure 7). The TPS2047 and TPS2057 are capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

$\overline{\text{OC}}$ response

The $\overline{\text{OC}}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false overcurrent reporting from the inrush current flowing through the device, charging the downstream capacitor. An RC filter of 500 μs (see Figure 30) can be connected to $\overline{\text{OCx}}$ to reduce false overcurrent reporting caused by hot-plug switching events or extremely high capacitive loads. Using low-ESR electrolytic capacitors on the output lowers the inrush current flow through the device during hot-plug events by providing a low impedance energy source, thereby reducing erroneous overcurrent reporting.

APPLICATION INFORMATION

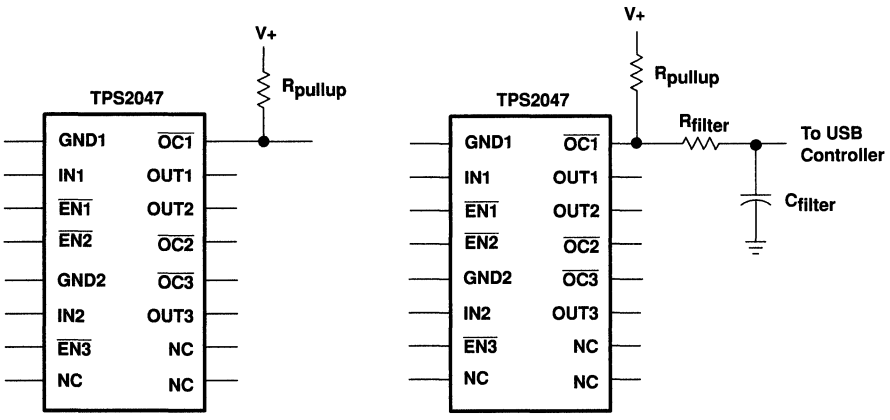


Figure 30. Typical Circuit for $\overline{OC}$ Pin and RC Filter for Damping Inrush $\overline{OC}$ Responses

power dissipation and junction temperature

The low on-resistance on the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find $r_{DS(on)}$ at the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figure 21. Next, calculate the power dissipation using:

$$P_D = r_{DS(on)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient Temperature °C
$R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

APPLICATION INFORMATION

thermal protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS2047 and TPS2057 into constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels. The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

The TPS2047 and TPS2057 implement a dual thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition the junction temperature will rise. Once the die temperature rises to approximately 140°C, the internal thermal sense circuitry checks which power switch is in an overcurrent condition and turns that power switch off, thus isolating the fault without interrupting operation of the adjacent power switch. Should the die temperature exceed the first thermal trip point of 140°C and reach 160°C, both switches turn off. The $\overline{OC}$ open-drain output is asserted (active low) when overtemperature or overcurrent occurs.

undervoltage lockout (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch will be quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO will also keep the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. Upon reinsertion, the power switch will be turned on with a controlled rise time to reduce EMI and voltage overshoots.

Universal Serial Bus (USB) applications

The universal serial bus (USB) interface is a 12-Mb/s, or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

Bus-powered hubs distribute data and power to downstream functions. The TPS2047 and TPS2057 can provide power-distribution solutions for many of these classes of devices.

APPLICATION INFORMATION

bus-powered hubs

Bus-powered hubs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

low-power bus-powered functions and high-power bus-powered functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA, and high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 µF at power up, the device must implement inrush current limiting (see Figure 31).

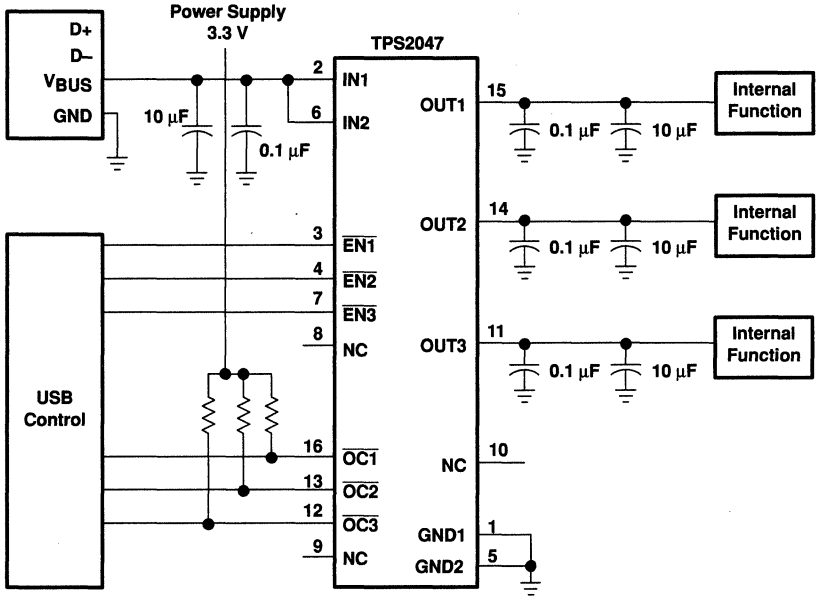


Figure 31. High-Power Bus-Powered Function

APPLICATION INFORMATION

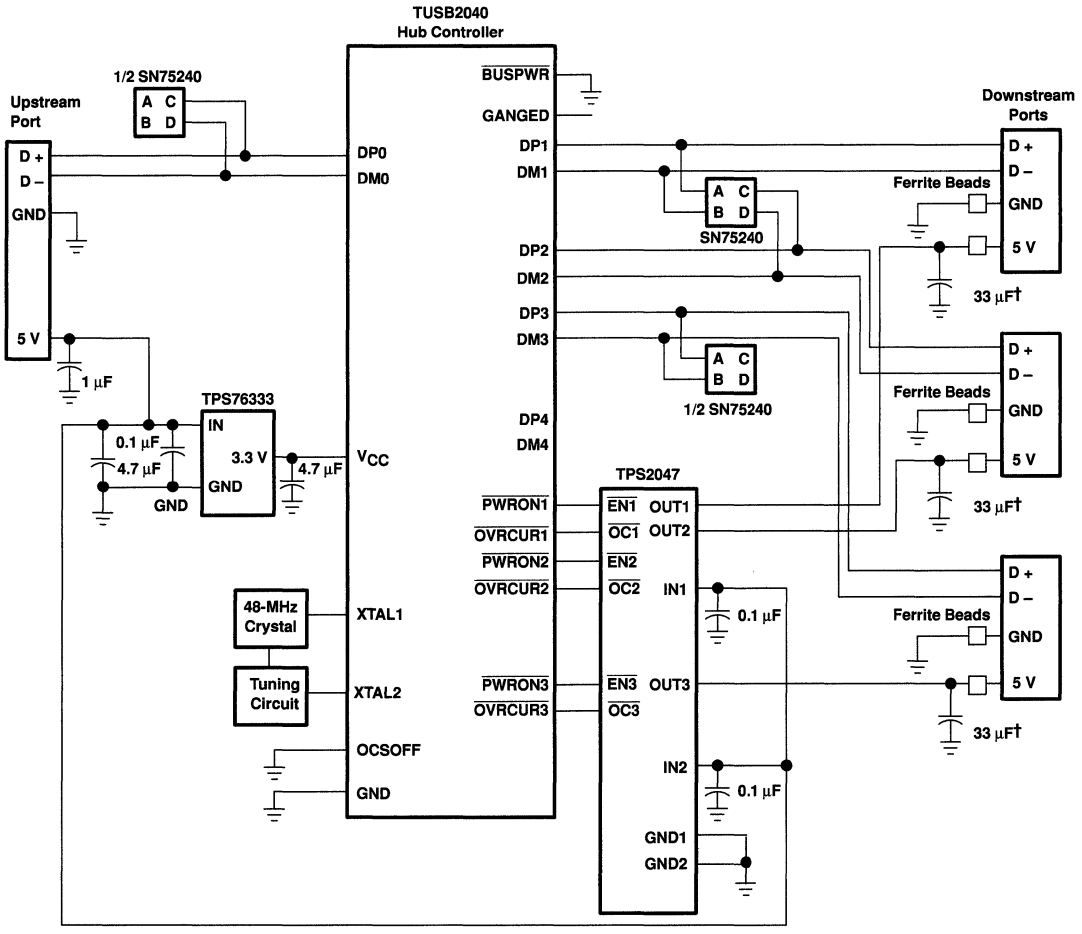
USB power-distribution requirements

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power distribution features must be implemented.

- Bus-Powered Hubs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 μF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

The feature set of the TPS2047 and TPS2057 allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-power hubs, as well as the input ports for bus-power functions (see Figure 32).

APPLICATION INFORMATION



† USB rev 1.1 requires 120 µF per hub.

Figure 32. Bus-Powered Hub Implementation

APPLICATION INFORMATION

generic hot-plug applications (see Figure 33)

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS2047 and TPS2057, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS2047 and TPS2057 also ensures the switch will be off after the card has been removed, and the switch will be off during the next insertion. The UVLO feature guarantees a soft start with a controlled rise time for every insertion of the card or module.

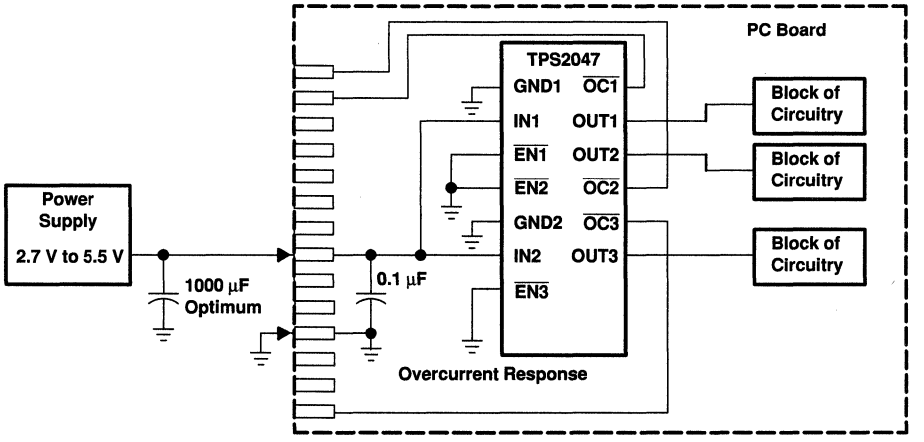


Figure 33. Typical Hot-Plug Implementation

By placing the TPS2047 or TPS2057 between the V_{CC} input and the rest of the circuitry, the input power will reach these devices first after insertion. The typical rise time of the switch is approximately 2.5 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

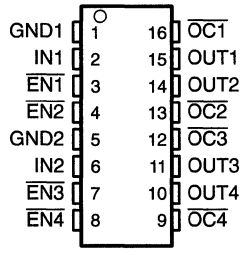
features

- 135-mΩ -Maximum (5-V Input) High-Side MOSFET Switch
- 250 mA Continuous Current per Channel
- Independent Short-Circuit and Thermal Protection With Overcurrent Logic Output
- Operating Range . . . 2.7-V to 5.5-V
- Logic-Level Enable Input
- 2.5-ms Typical Rise Time
- Undervoltage Lockout
- 20 μA Maximum Standby Supply Current
- Bidirectional Switch
- Available in 16-pin SOIC Package
- Ambient Temperature Range, –40°C to 85°C
- 2-kV Human-Body-Model, 200-V Machine-Model ESD Protection

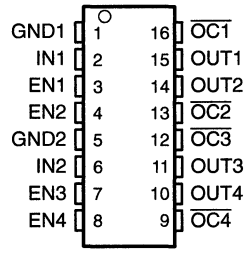
typical applications

- Notebook, Desktop and Palmtop PCs
- Monitors, Keyboards, Scanners, and Printers
- Digital Cameras, Phones, and PBXs
- Hot-Insertion Applications

TPS2048
D PACKAGE
(TOP VIEW)



TPS2058
D PACKAGE
(TOP VIEW)



description

The TPS2048 and TPS2058 quad power-distribution switches are intended for applications where heavy capacitive loads and short circuits are likely. These devices incorporate in single packages four 135-mΩ N-channel MOSFET high-side power switches for power-distribution systems that require multiple power switches. Each switch is controlled by a logic enable compatible with 5-V and 3-V logic. Gate drive is provided by an internal charge pump that controls the power-switch rise times and fall times to minimize current surges during switching. The charge pump, requiring no external components, allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the TPS2048 and TPS2058 limit the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{OCx}$) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch causing the junction temperature to rise, a thermal protection circuit shuts off the switch in overcurrent to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until valid input voltage is present.

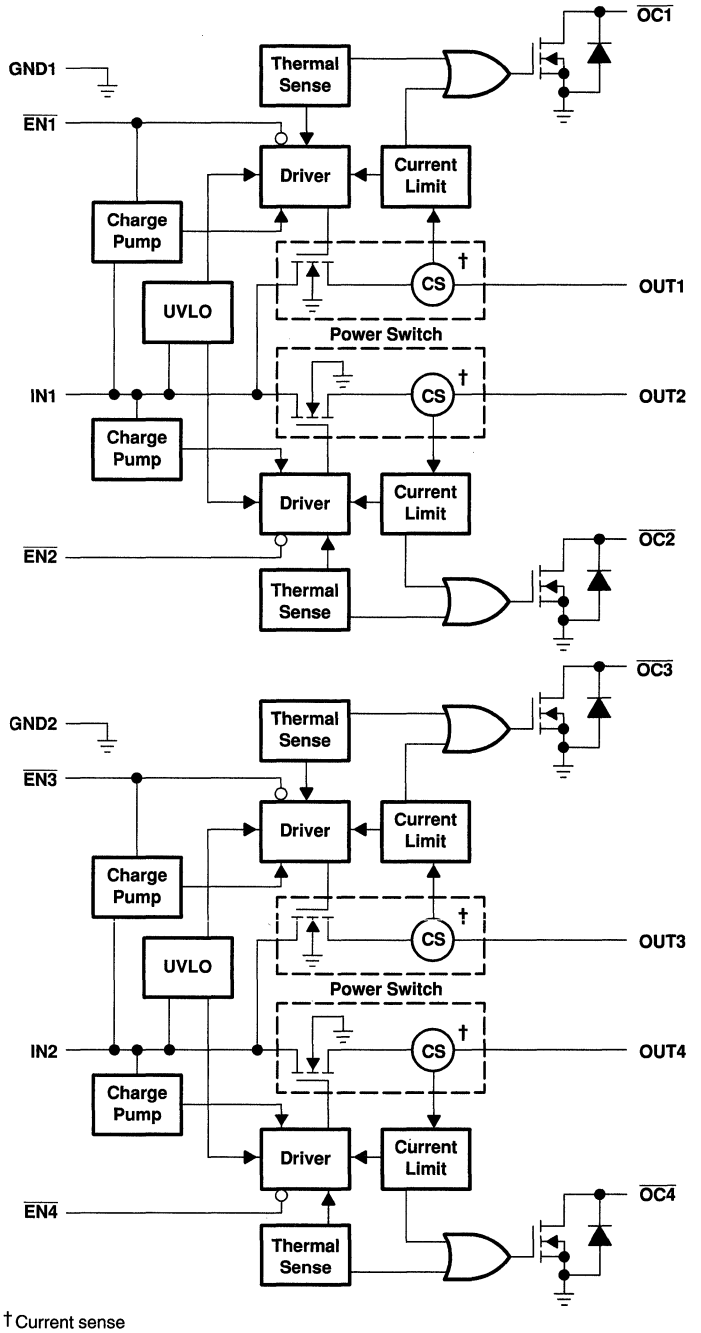
The TPS2048 and TPS2058 are designed to limit at 0.44-A load. These power-distribution switches are available in 16-pin small-outline integrated circuit (SOIC) packages and operate over an ambient temperature range of –40°C to 85°C.

AVAILABLE OPTIONS

T_A	ENABLE	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A)	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (A)	PACKAGED DEVICES SOIC (D)†
–40°C to 85°C	Active low	0.25	0.44	TPS2048D
–40°C to 85°C	Active high	0.25	0.44	TPS2058D

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2048DR)

TPS2048 functional block diagram



† Current sense

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	TPS2048	TPS2058		
$\overline{EN1}$	3	–	I	Enable input. Logic low turns on power switch, IN1-OUT1.
$\overline{EN2}$	4	–	I	Enable input. Logic low turns on power switch, IN1-OUT2.
$\overline{EN3}$	7	–	I	Enable input. Logic low turns on power switch, IN2-OUT3.
$\overline{EN4}$	8	–	I	Enable input. Logic low turns on power switch, IN2-OUT4.
EN1	–	3	I	Enable input. Logic high turns on power switch, IN1-OUT1.
EN2	–	4	I	Enable input. Logic high turns on power switch, IN1-OUT2.
EN3	–	7	I	Enable input. Logic high turns on power switch, IN2-OUT3.
EN4	–	8	I	Enable input. Logic high turns on power switch, IN2-OUT4.
GND1	1	1		Ground
GND2	5	5		Ground
IN1	2	2	I	Input voltage
IN2	6	6	I	Input voltage
$\overline{OC1}$	16	16	O	Overcurrent. Logic output active low, IN1-OUT1
$\overline{OC2}$	13	13	O	Overcurrent. Logic output active low, IN1-OUT2
$\overline{OC3}$	12	12	O	Overcurrent. Logic output active low, IN2-OUT3
$\overline{OC4}$	9	9	O	Overcurrent. Logic output active low, IN2-OUT4
OUT1	15	15	O	Power-switch output, IN1-OUT1
OUT2	14	14	O	Power-switch output, IN1-OUT2
OUT3	11	11	O	Power-switch output, IN2-OUT3
OUT4	10	10	O	Power-switch output, IN2-OUT4

detailed description

power switch

The power switch is an N-channel MOSFET with a maximum on-state resistance of 135 mΩ ($V_{I(INx)}$ = 5 V). Configured as a high-side switch, the power switch prevents current flow from OUTx to INx and INx to OUTx when disabled. The power switch can supply a minimum of 250 mA per switch.

charge pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 4-ms range.

enable ($\overline{ENx}$ or ENx)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 20 µA when a logic high is present on $\overline{ENx}$ (TPS2048) or a logic low is present on ENx (TPS2058). A logic zero input on $\overline{ENx}$ or logic high on ENx restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

overcurrent ($\overline{OCx}$)

The $\overline{OCx}$ open drain output is asserted (active low) when an overcurrent or over temperature condition is encountered. The output will remain asserted until the overcurrent or over temperature condition is removed.

current sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant current mode and holds the current constant while varying the voltage on the load.

thermal sense

The TPS2048 and TPS2058 implement a dual-threshold thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition the junction temperature rises. When the die temperature rises to approximately 140°C, the internal thermal sense circuitry checks to determine which power switch is in an overcurrent condition and turns off that switch, thus, isolating the fault without interrupting operation of the adjacent power switches. Hysteresis is built into the thermal sense, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed. The ($\overline{OCx}$) open-drain output is asserted (active low) when overtemperature or overcurrent occurs.

undervoltage lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, $V_{I(INx)}$ (see Note1) ..... –0.3 V to 6 V
Output voltage range, $V_{O(OUTx)}$ (see Note1) ..... –0.3 V to $V_{I(INx)}$ + 0.3 V
Input voltage range, $V_{I(\overline{ENx})}$ or $V_{I(ENx)}$ ..... –0.3 V to 6 V
Continuous output current, $I_{O(OUTx)}$ ..... Internally limited
Continuous total power dissipation ..... See Dissipation Rating Table
Operating virtual junction temperature range, T_J ..... –40°C to 125°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C
Electrostatic discharge (ESD) protection: Human body model MIL-STD-883C ..... 2 kV
Machine model ..... 0.2 kV

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW

recommended operating conditions

	TPS2048		TPS2058		UNIT
	MIN	MAX	MIN	MAX	
Input voltage, $V_{I(INx)}$	2.7	5.5	2.7	5.5	V
Input voltage, $V_{I(\overline{ENx})}$ or $V_{I(ENx)}$	0	5.5	0	5.5	V
Continuous output current, $I_{O(OUTx)}$	0	250	0	250	mA
Operating virtual junction temperature, T_J	–40	125	–40	125	°C

electrical characteristics over recommended operating junction temperature range, $V_{I(INx)}$= 5.5 V, I_O = rated current, $V_{I(\overline{ENx})}$ = 0 V, $V_{I(ENx)}$ = Hi (unless otherwise noted)

power switch

PARAMETER		TEST CONDITIONS†	TPS2048			TPS2058			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$r_{DS(on)}$	Static drain-source on-state resistance, 5-V operation	$V_{I(INx)}$ = 5 V, I_O = 0.25 A, T_J = 25°C		80	95		80	95	mΩ
		$V_{I(INx)}$ = 5 V, I_O = 0.25 A, T_J = 85°C		90	120		90	120	
		$V_{I(INx)}$ = 5 V, I_O = 0.25 A, T_J = 125°C		100	135		100	135	
	Static drain-source on-state resistance, 3.3-V operation	$V_{I(INx)}$ = 3.3 V, I_O = 0.25 A, T_J = 25°C		85	105		85	105	
		$V_{I(INx)}$ = 3.3 V, I_O = 0.25 A, T_J = 85°C		100	135		100	135	
		$V_{I(INx)}$ = 3.3 V, I_O = 0.25 A, T_J = 125°C		115	150		115	150	
t_r	Rise time, output	$V_{I(INx)}$ = 5.5 V, C_L = 1 µF, R_L = 20 Ω, T_J = 25°C		2.5			2.5		ms
		$V_{I(INx)}$ = 2.7 V, C_L = 1 µF, R_L = 20 Ω, T_J = 25°C		3			3		
t_f	Fall time, output	$V_{I(INx)}$ = 5.5 V, C_L = 1 µF, R_L = 20 Ω, T_J = 25°C		4.4			4.4		ms
		$V_{I(INx)}$ = 2.7 V, C_L = 1 µF, R_L = 20 Ω, T_J = 25°C		2.5			2.5		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

enable input $\overline{ENx}$ or ENx

PARAMETER			TEST CONDITIONS	TPS2048			TPS2058			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High–level input voltage		2.7 V ≤ $V_{I(INx)}$ ≤ 5.5 V	2			2			V
V_{IL}	Low–level input voltage		4.5 V ≤ $V_{I(INx)}$ ≤ 5.5 V			0.8			0.8	V
			2.7 V≤ $V_{I(INx)}$ ≤ 4.5 V			0.4			0.4	
I_I	Input current	TPS2048	$V_{I(\overline{ENx})}$ = 0 V or $V_{I(\overline{ENx})}$ = $V_{I(INx)}$	–0.5		0.5				µA
		TPS2058	$V_{I(ENx)}$ = $V_{I(INx)}$ or $V_{I(ENx)}$ = 0 V				–0.5		0.5	
t_{on}	Turnon time		C_L = 100 µF, R_L = 20 Ω			20			20	ms
t_{off}	Turnoff time		C_L = 100 µF, R_L = 20 Ω			40			40	

current limit

PARAMETER		TEST CONDITIONS†	TPS2048			TPS2058			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{OS}	Short-circuit output current	$V_{I(INx)}$ = 5 V, OUT connected to GND, Device enable into short circuit	0.345	0.44	0.525	0.345	0.44	0.525	A

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics over recommended operating junction temperature range, $V_{I(INx)}$= 5.5 V, I_O = rated current, $V_{I(\overline{ENx})}$ = 0 V, $V_{I(ENx)}$ = Hi (unless otherwise noted) (continued)

supply current

PARAMETER	TEST CONDITIONS				TPS2048			TPS2058			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
Supply current, low-level output	No Load on OUTx	$V_{I(\overline{ENx})} = V_{I(INx)}$	T_J = 25°C	TPS2048		0.03	2				µA
			–40°C ≤ T_J ≤ 125°C				20				
		$V_{I(ENx)}$ = 0 V	T_J = 25°C	TPS2058					0.03	2	
			–40°C ≤ T_J ≤ 125°C							20	
Supply current, high-level output	No Load on OUTx	$V_{I(\overline{ENx})}$ = 0 V	T_J = 25°C	TPS2048		160	200				µA
			–40°C ≤ T_J ≤ 125°C			200					
		$V_{I(ENx)} = V_{I(INx)}$	T_J = 25°C	TPS2058					160	200	
			–40°C ≤ T_J ≤ 125°C						200		
Leakage current	OUTx connected to ground	$V_{I(\overline{ENx})} = V_{I(INx)}$	–40°C ≤ T_J ≤ 125°C	TPS2048		200					µA
		$V_{I(ENx)}$ = 0 V		TPS2058					200		
Reverse leakage current	INx = high impedance	$V_{I(\overline{ENx})}$ = 0 V	T_J = 25°C	TPS2048		0.3					µA
		$V_{I(ENx)}$ = Hi		TPS2058					0.3		

undervoltage lockout

PARAMETER	TEST CONDITIONS	TPS2048			TPS2058			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Low-level input voltage		2		2.5	2		2.5	V
Hysteresis	T_J = 25°C		100			100		mV

overcurrent $\overline{OCx}$

PARAMETER	TEST CONDITIONS	TPS2048			TPS2058			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Sink current†	V_O = 5 V			10			10	mA
Output low voltage	I_O = 5 mA, $V_{OL(\overline{OCx})}$			0.5			0.5	V
Off-state current†	V_O = 5 V, V_O = 3.3 V			1			1	µA

† Specified by design, not production tested.

PARAMETER MEASUREMENT INFORMATION

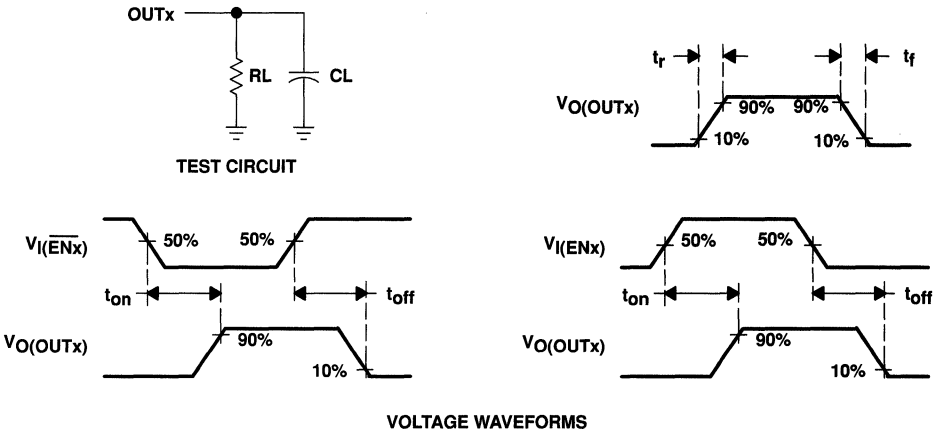


Figure 1. Test Circuit and Voltage Waveforms

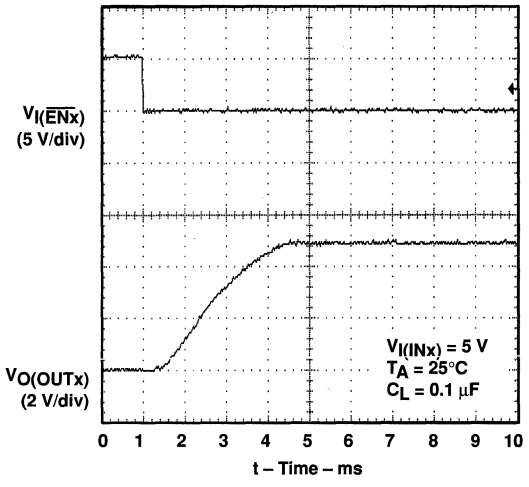


Figure 2. Turnon Delay and Rise Time with 0.1-μF Load

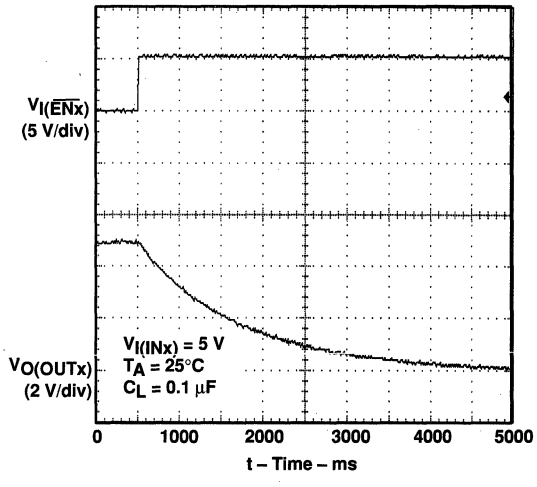


Figure 3. Turnoff Delay and Fall Time with 0.1-μF Load

PARAMETER MEASUREMENT INFORMATION

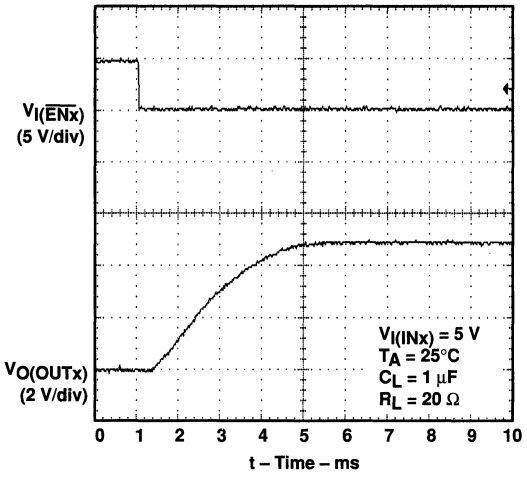


Figure 4. Turnon Delay and Rise Time with 1-μF Load

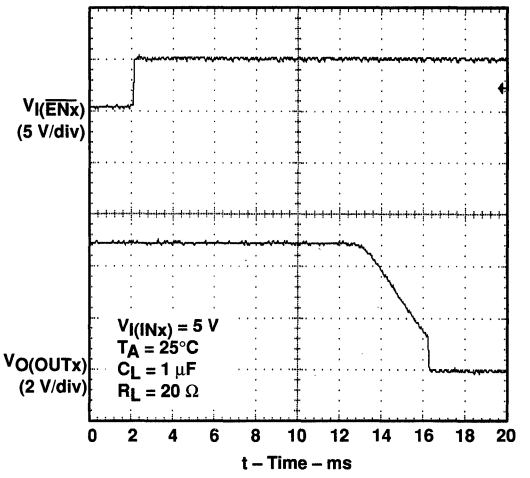


Figure 5. Turnoff Delay and Fall Time with 1-μF Load

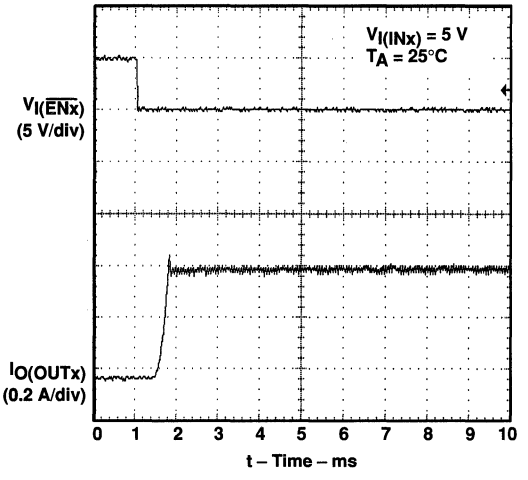


Figure 6. TPS2048, Short-Circuit Current, Device Enabled into Short

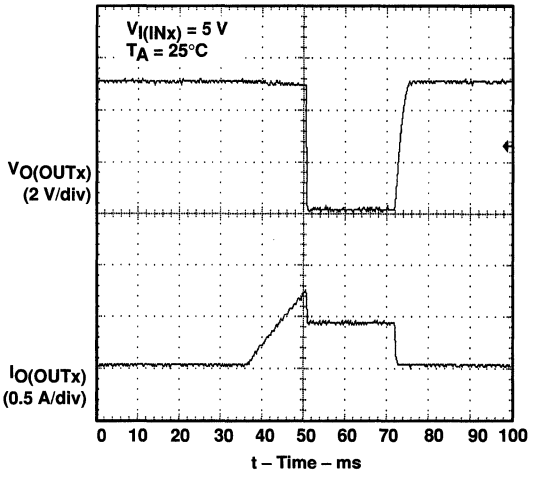


Figure 7. TPS2048, Threshold Trip Current with Ramped Load on Enabled Device

PARAMETER MEASUREMENT INFORMATION

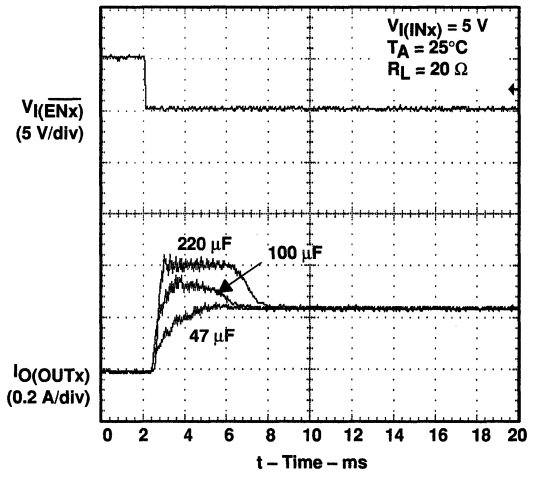


Figure 8. Inrush Current with 220-µF, 100-µF and 47-µF Load Capacitance

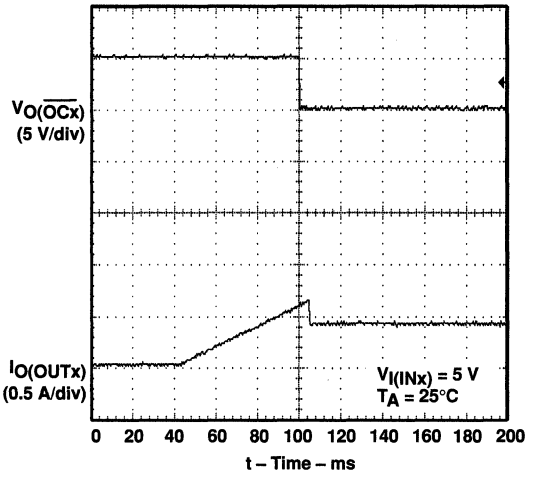


Figure 9. Ramped Load on Enabled Device

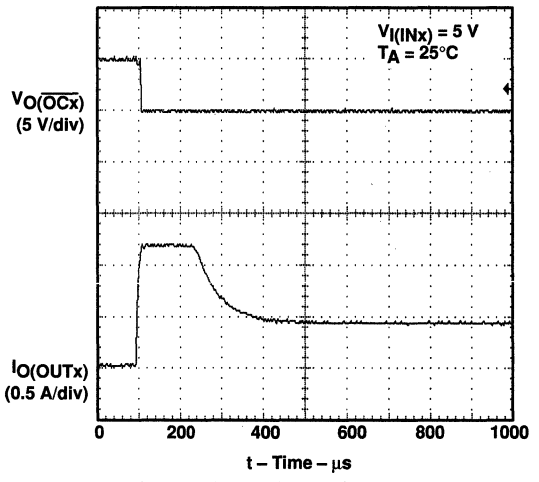


Figure 10. 4-Ω Load Connected to Enabled Device

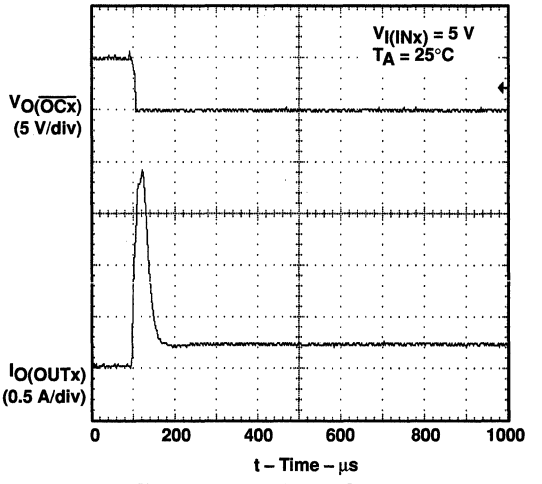


Figure 11. 1-Ω Load Connected to Enabled Device

TYPICAL CHARACTERISTICS

TURNON DELAY
vs
INPUT VOLTAGE

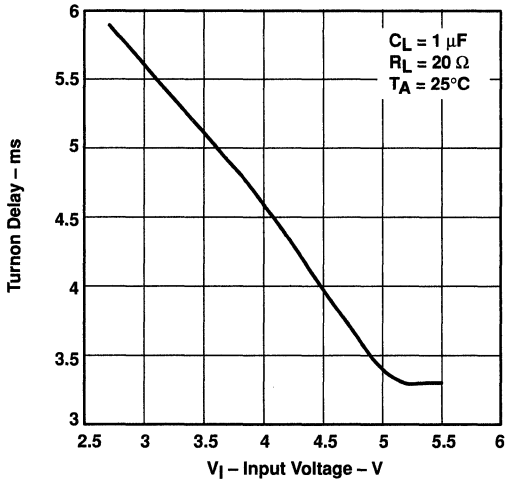


Figure 12

TURNOFF DELAY
vs
INPUT VOLTAGE

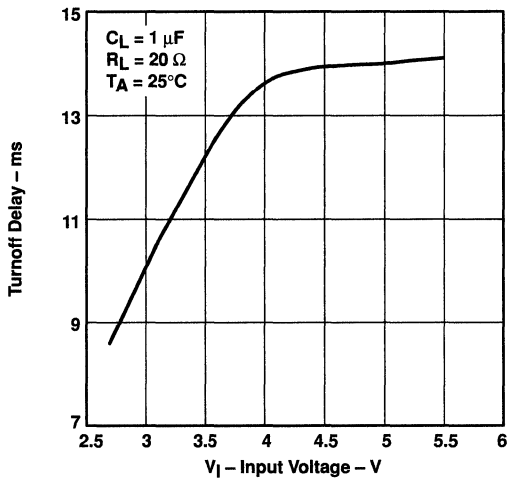


Figure 13

RISE TIME
vs
LOAD CURRENT

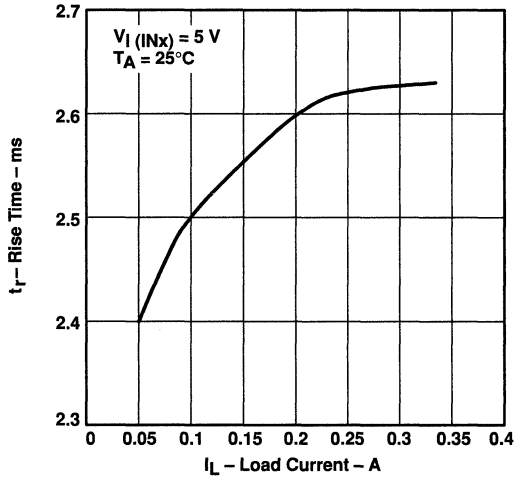


Figure 14

FALL TIME
vs
LOAD CURRENT

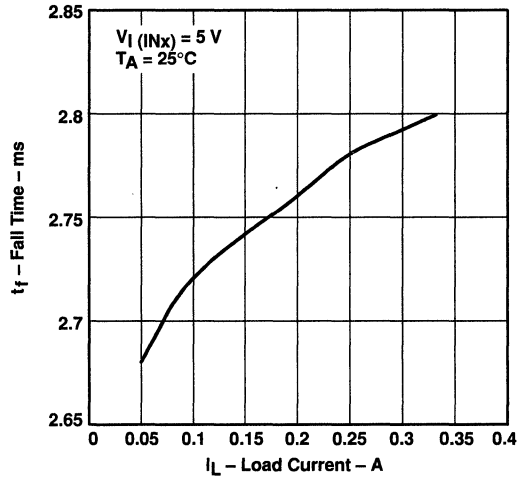


Figure 15

TYPICAL CHARACTERISTICS

SUPPLY CURRENT, OUTPUT ENABLED
vs
JUNCTION TEMPERATURE

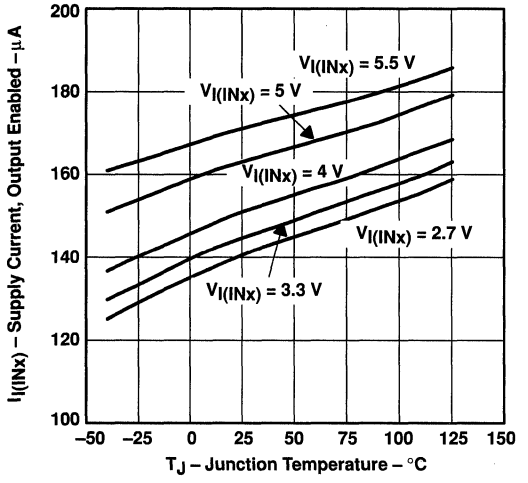


Figure 16

SUPPLY CURRENT, OUTPUT DISABLED
vs
JUNCTION TEMPERATURE

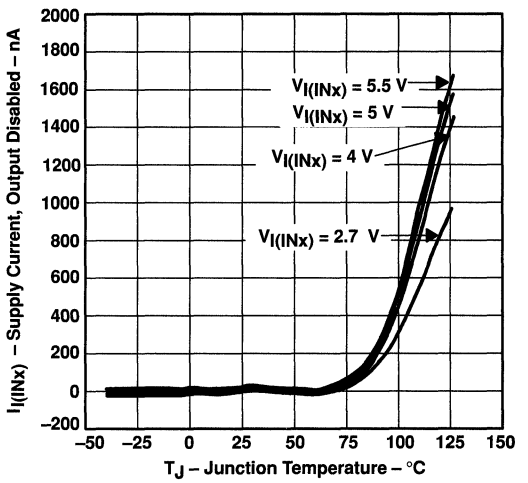


Figure 17

SUPPLY CURRENT, OUTPUT ENABLED
vs
INPUT VOLTAGE

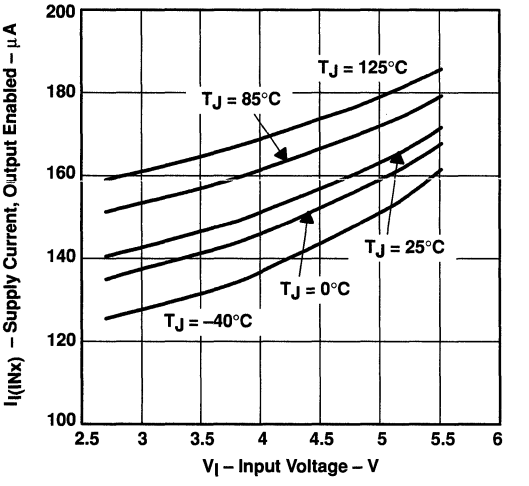


Figure 18

SUPPLY CURRENT, OUTPUT DISABLED
vs
INPUT VOLTAGE

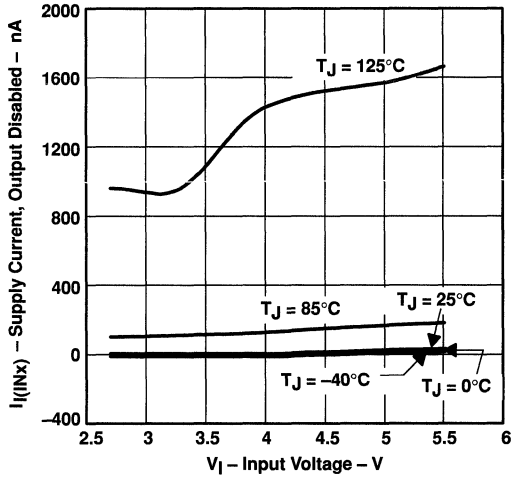


Figure 19

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

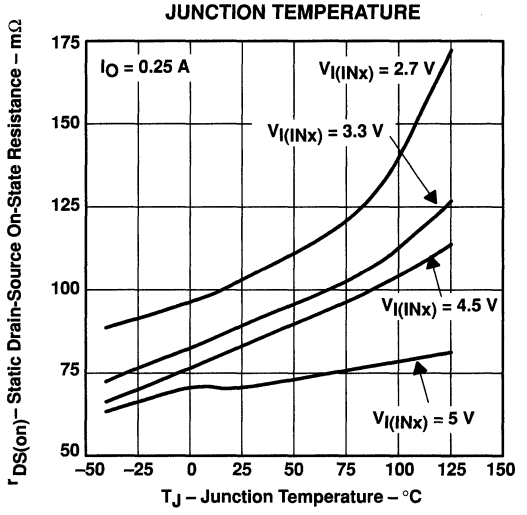


Figure 20

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
INPUT VOLTAGE

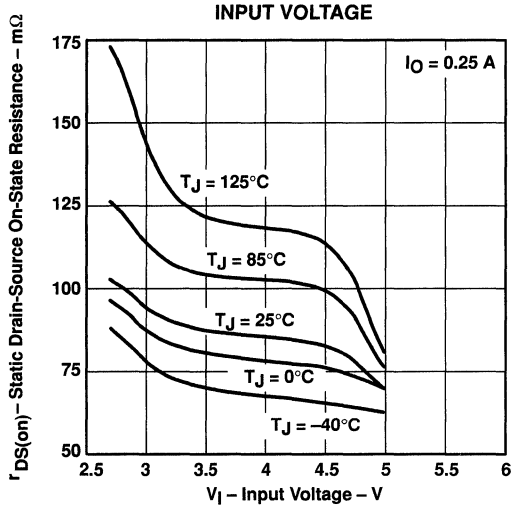


Figure 21

INPUT-TO-OUTPUT VOLTAGE
vs
LOAD CURRENT

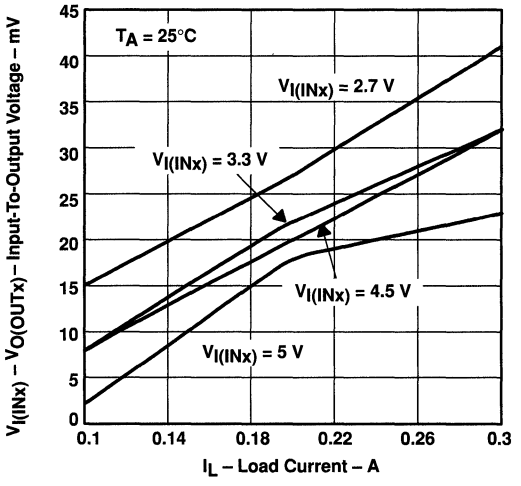


Figure 22

SHORT-CURCUIT OUTPUT CURRENT
vs
INPUT VOLTAGE

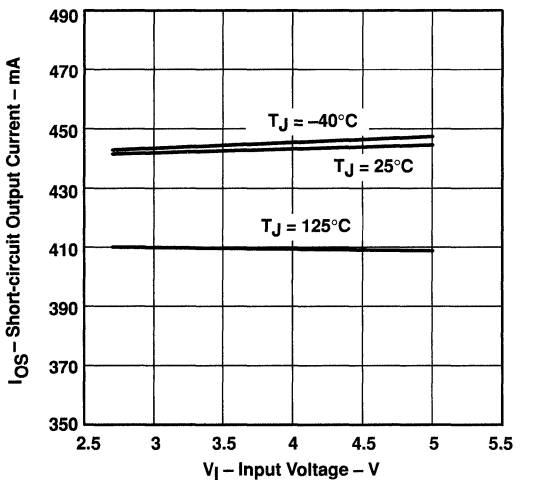


Figure 23

TYPICAL CHARACTERISTICS

THRESHOLD TRIP CURRENT
vs
INPUT VOLTAGE

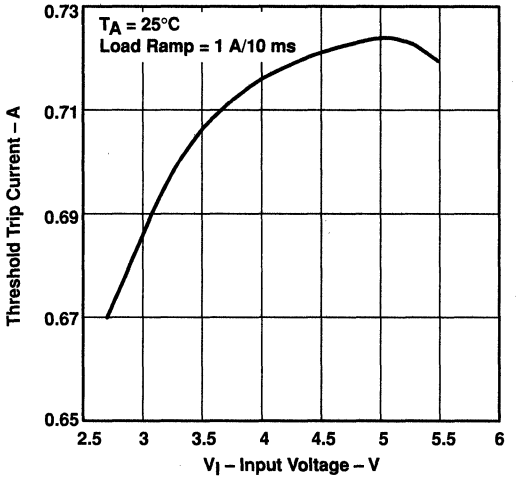


Figure 24

SHORTCIRCUIT OUTPUT CURRENT
vs
JUNCTION TEMPERATURE

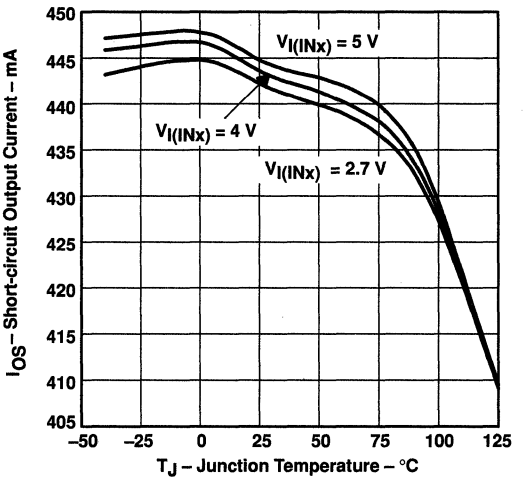


Figure 25

UNDERVOLTAGE LOCKOUT
vs
JUNCTION TEMPERATURE

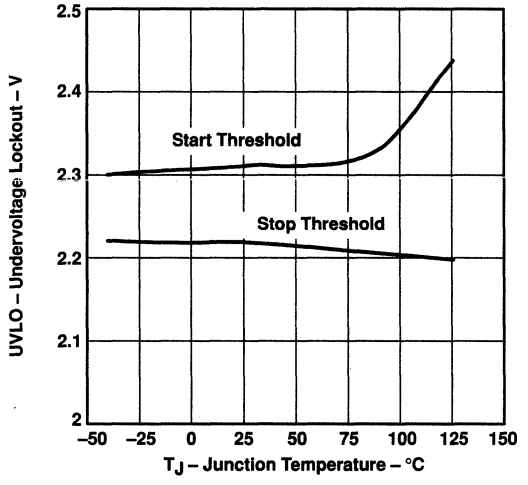


Figure 26

CURRENT-LIMIT RESPONSE
vs
PEAK CURRENT

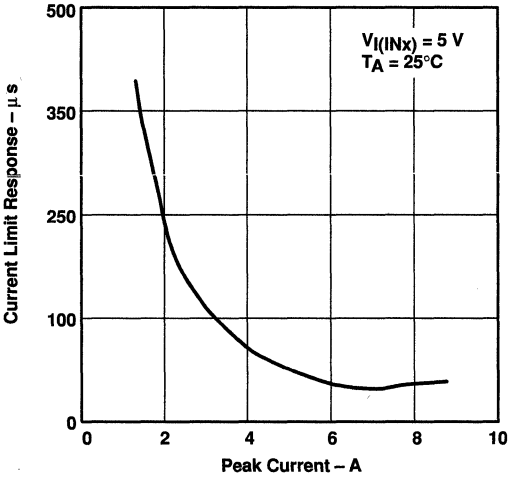


Figure 27

TYPICAL CHARACTERISTICS

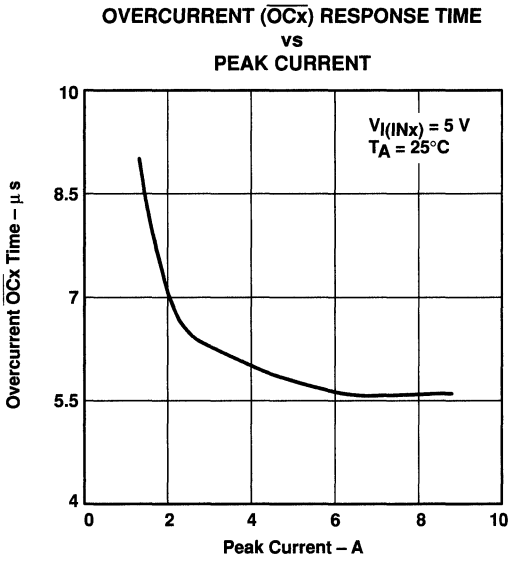


Figure 28

APPLICATION INFORMATION

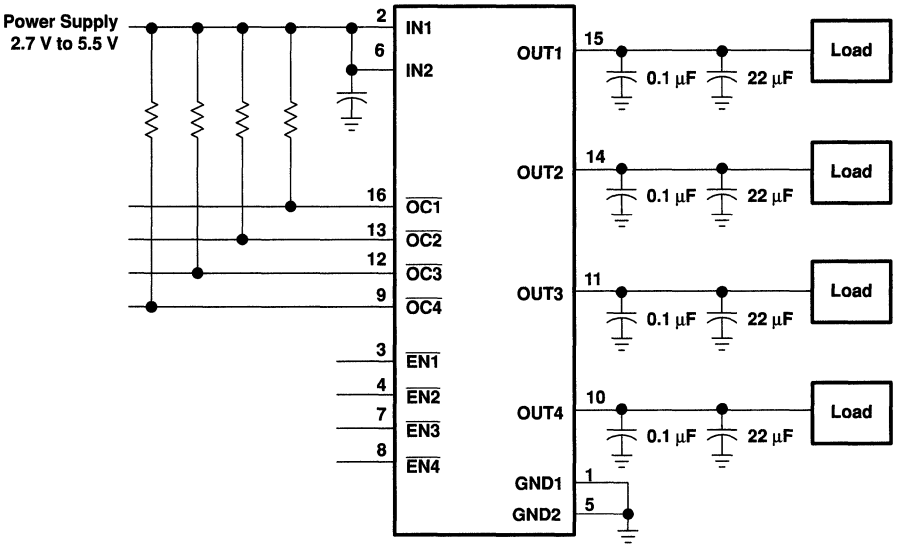


Figure 29. Typical Application

APPLICATION INFORMATION

power supply considerations

A 0.01-μF to 0.1-μF ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-μF to 0.1-μF ceramic capacitor improves the immunity of the device to short-circuit transients.

overcurrent

A sense FET checks for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(INx)}$ has been applied (see Figure 6). The TPS2048 and TPS2058 sense the short and immediately switch into a constant-current output.

In the second condition, the short occurs while the device is enabled. At the instant the short occurs, very high currents may flow for a short time before the current-limit circuit can react . After the current-limit circuit has tripped (reached the overcurrent trip threshhold) the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figure 7). The TPS2048 and TPS2058 are capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

$\overline{\text{OC}}$ response

The $\overline{\text{OC}}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false overcurrent reporting from the inrush current flowing through the device, charging the downstream capacitor. An RC filter of 500 μs (see Figure 30) can be connected to $\overline{\text{OCx}}$ to reduce false overcurrent reporting caused by hot-plug switching events or extremly high capacitive loads. Using low-ESR electrolytic capacitors on the output lowers the inrush current flow through the device during hot-plug events by providing a low impedance energy source, thereby reducing erroneous overcurrent reporting.

APPLICATION INFORMATION

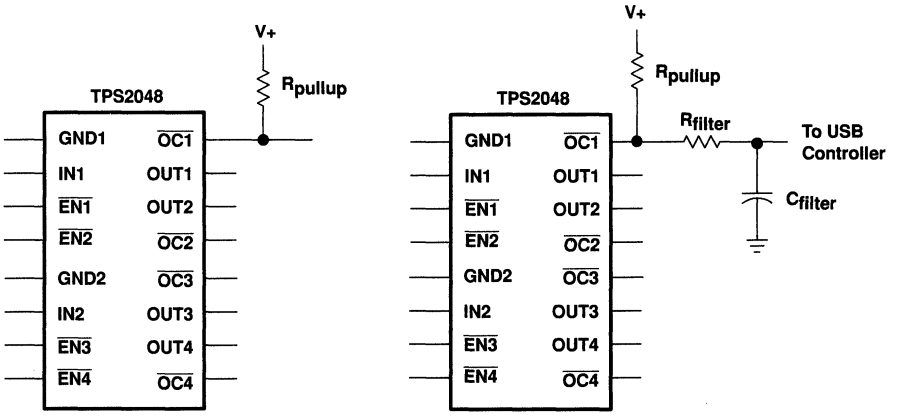


Figure 30. Typical Circuit for $\overline{OC}$ Pin and RC Filter for Damping Inrush $\overline{OC}$ Responses

power dissipation and junction temperature

The low on-resistance on the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find $r_{DS(on)}$ at the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figure 21. Next, calculate the power dissipation using:

$$P_D = r_{DS(on)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient Temperature °C
$R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

APPLICATION INFORMATION

thermal protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS2048 and TPS2058 into constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels. The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

The TPS2048 and TPS2058 implement a dual thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition the junction temperature will rise. Once the die temperature rises to approximately 140°C, the internal thermal sense circuitry checks which power switch is in an overcurrent condition and turns that power switch off, thus isolating the fault without interrupting operation of the adjacent power switch. Should the die temperature exceed the first thermal trip point of 140°C and reach 160°C, both switches turn off. The $\overline{OC}$ open-drain output is asserted (active low) when overtemperature or overcurrent occurs.

undervoltage lockout (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch will be quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO will also keep the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. Upon reinsertion, the power switch will be turned on with a controlled rise time to reduce EMI and voltage overshoots.

Universal Serial Bus (USB) applications

The universal serial bus (USB) interface is a 12-Mb/s, or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

Bus-powered hubs distribute data and power to downstream functions. The TPS2048 and TPS2058 can provide power-distribution solutions for many of these classes of devices.

APPLICATION INFORMATION

bus-powered hubs

Bus-powered hubs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

low-power bus-powered functions and high-power bus-powered functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA, and high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 µF at power up, the device must implement inrush current limiting (see Figure 31).

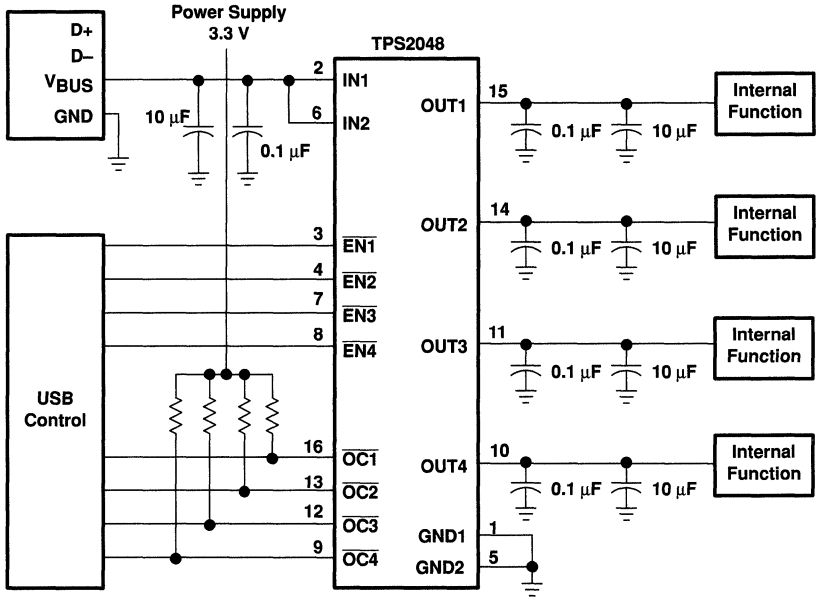


Figure 31. High-Power Bus-Powered Function

APPLICATION INFORMATION

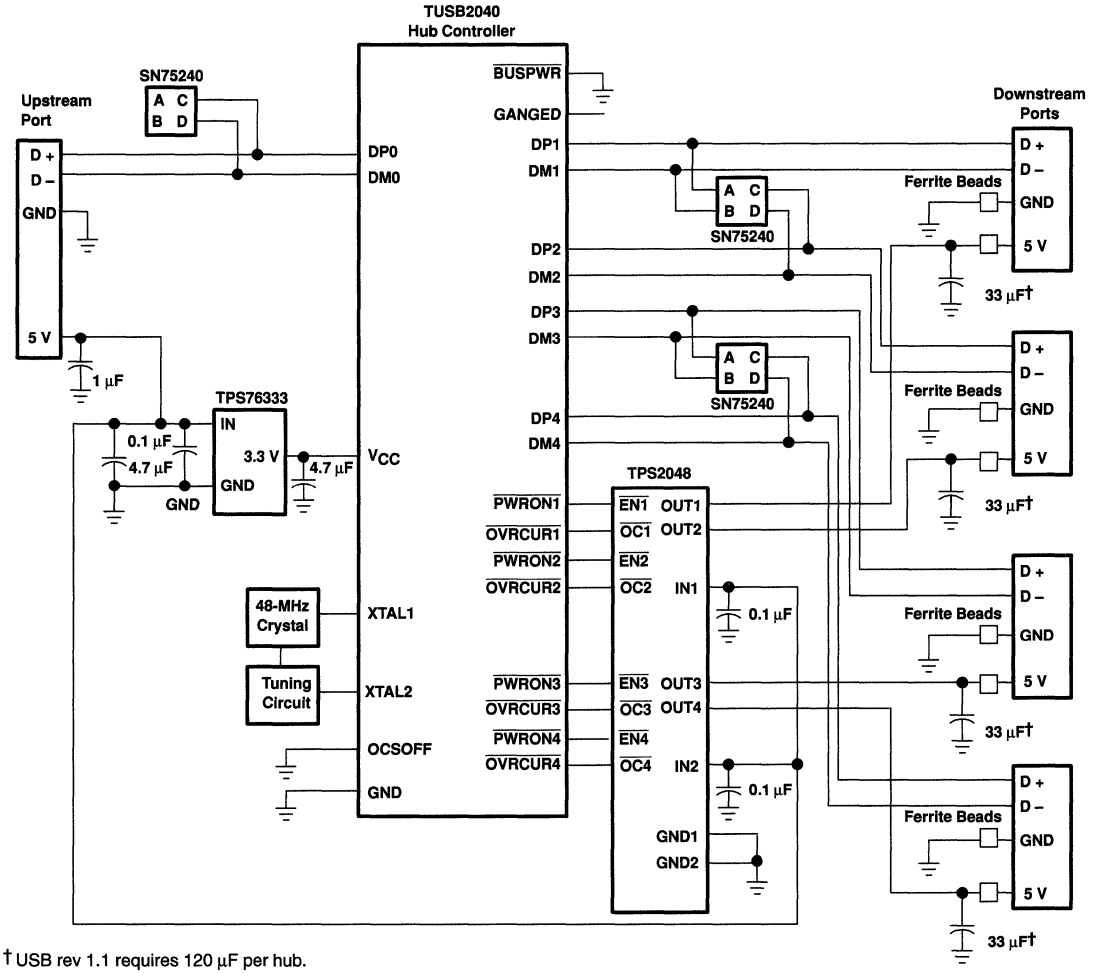
USB power-distribution requirements

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power distribution features must be implemented.

- Bus-Powered Hubs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 μF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

The feature set of the TPS2048 and TPS2058 allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-power hubs, as well as the input ports for bus-power functions (see Figure 32).

APPLICATION INFORMATION



† USB rev 1.1 requires 120 µF per hub.

Figure 32. Bus-Powered Hub Implementation

APPLICATION INFORMATION

generic hot-plug applications (see Figure 33)

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS2048 and TPS2058, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS2048 and TPS2058 also ensures the switch will be off after the card has been removed, and the switch will be off during the next insertion. The UVLO feature guarantees a soft start with a controlled rise time for every insertion of the card or module.

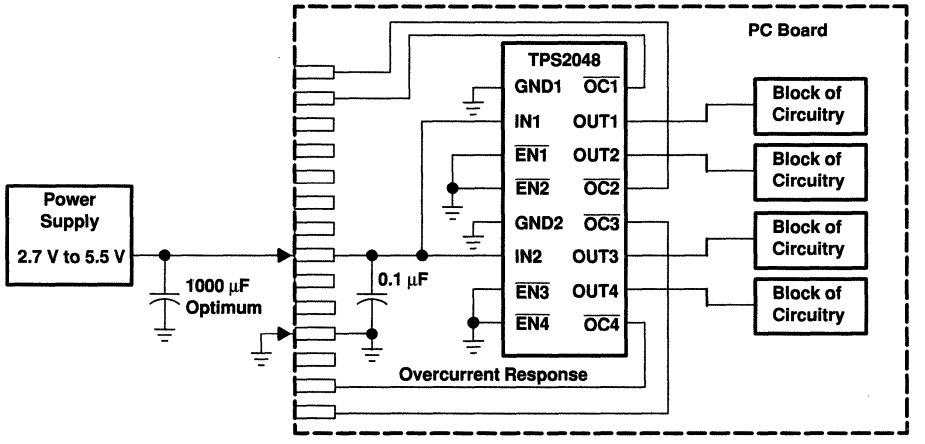


Figure 33. Typical Hot-Plug Implementation

By placing the TPS2048 or TPS2058 between the V_{CC} input and the rest of the circuitry, the input power will reach these devices first after insertion. The typical rise time of the switch is approximately 2.5 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

features

- Dual-Input, Single-Output MOSFET Switch With No Reverse Current Flow (No Parasitic Diodes)
- IN1 . . . 250-mΩ, 500-mA N-Channel; 16-μA Max Supply Current
- IN2 . . . 1.3-Ω, 10-mA P-Channel; 1.5-μA Max Supply Current (V_{AUX} Mode)
- Advanced Switch Control Logic
- CMOS- and TTL-Compatible Enable Input
- Controlled Rise, Fall, and Transition Times
- 2.7-V to 4 V Operating Range
- SOT-23-5 and SOIC-8 Package
- –40°C to 70°C Ambient Temperature Range
- 2-kV Human-Body-Model, 750-V CDM, 200-V Machine-Model Electrostatic-Discharge Protection

typical applications

- Notebook and Desktop PCs
- Palmtops and PDAs

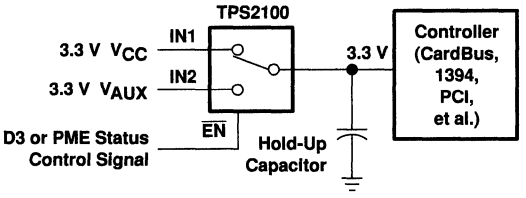


Figure 1. Typical Dual-Input Single-Output Application

description

The TPS2100 and TPS2101 are dual-input, single-output power switches designed to provide uninterrupted output voltage when transitioning between two independent power supplies. Both devices combine one n-channel (250 mΩ) and one p-channel (1.3 Ω) MOSFET with a single output. The p-channel MOSFET (IN2) is used with auxiliary power supplies that deliver lower current for standby modes. The n-channel MOSFET (IN1) is used with a main power supply that delivers higher current required for normal operation. Low on-resistance makes the n-channel the ideal path for higher main supply current when power-supply regulation and system voltage drops are critical. When using the p-channel MOSFET, quiescent current is reduced to 0.75 μA to decrease the demand on the standby power supply. The MOSFETs in the TPS2100 and TPS2101 do not have the parasitic diodes, found in discrete MOSFETs, which allow the devices to prevent back-flow current when the switch is off.

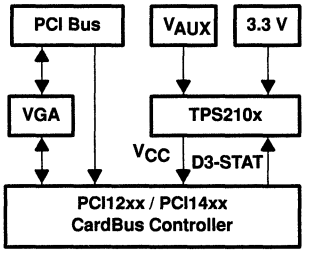
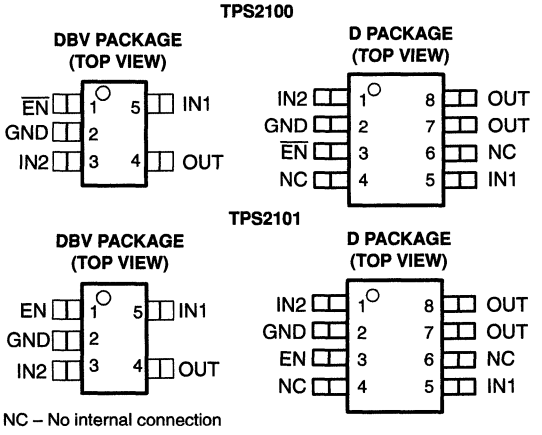


Figure 2. V_{AUX} CardBus Implementation



NC – No internal connection

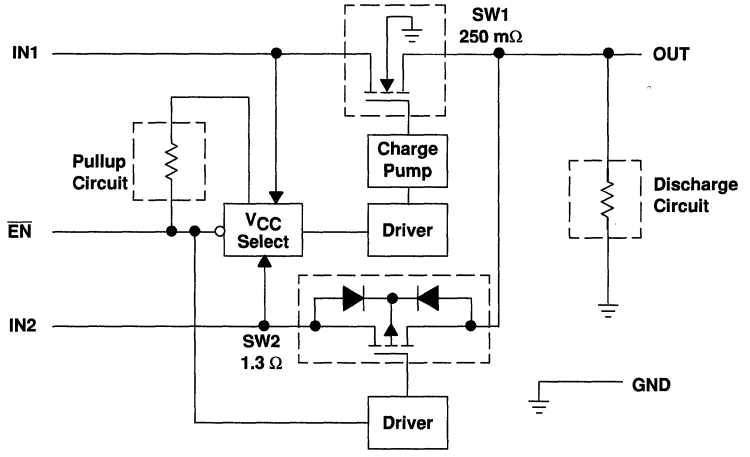
AVAILABLE OPTIONS

T_J	DEVICE	ENABLE	PACKAGED DEVICES	
			SOT-23-5 (DBV)†	SOIC-8 (D)
–40°C to 85°C	TPS2100	$\overline{EN}$	TSP2100DBV†	TPS2100D
	TPS2101	EN	TPS2101DBV†	TPS2101D

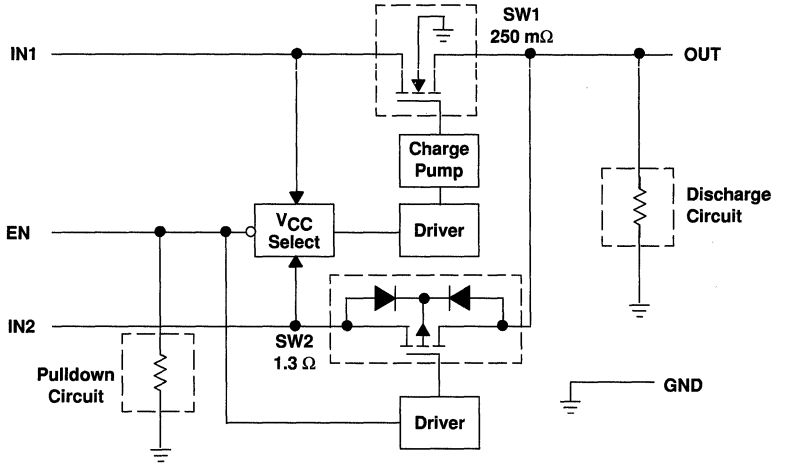
Both packages are available left-end taped and reeled. Add an R suffix to the D device type (e.g., TPS2101DR).

† Add T (e.g., TPS2100DBVT) to indicate tape and reel at order quantity of 250 parts.
Add R (e.g., TPS2100DBVR) to indicate tape and reel at order quantity of 3000 parts.

TPS2100 functional block diagram



TPS2101 functional block diagram



Function Tables

TPS2100			
VIN1	VIN2	$\overline{EN}$	OUT
0 V	0 V	XX	GND
0 V	3.3 V	L	GND
3.3 V	0 V	L	VIN1
3.3 V	3.3 V	L	VIN1
0 V	3.3 V	H	VIN2
3.3 V	0 V	H	VIN2
3.3 V	3.3 V	H	VIN2

XX = don't care

TPS2101			
VIN1	VIN2	EN	OUT
0 V	0 V	XX	GND
0 V	3.3 V	H	GND
3.3 V	0 V	H	VIN1
3.3 V	3.3 V	H	VIN1
0 V	3.3 V	L	VIN2
3.3 V	0 V	L	VIN2
3.3 V	3.3 V	L	VIN2

Terminal Functions

TERMINAL					I/O	DESCRIPTION
NAME	NO.					
	TPS2100		TPS2101			
	DBV	D	DBV	D		
EN			1	3		Active-high enable for IN1-OUT switch
$\overline{EN}$	1	3			I	Active-low enable for IN1-OUT switch
GND	2	2	2	2	I	Ground
IN1	5	5	5	5	I	Main Input voltage, NMOS drain (250 mΩ)
IN2	3	1	3	1	I	Auxilliary input voltage, PMOS drain (1.3 Ω)
OUT	4	7	4	7	O	Power switch output
NC		4, 6		4, 6		No connection

detailed description

power switches

n-channel MOSFET

The IN1-OUT n-channel MOSFET power switch has a typical on-resistance of 250 mΩ at 3.3-V input voltage, and is configured as a high-side switch.

p-channel MOSFET

The IN2-OUT p-channel MOSFET power switch with typical on-resistance of 1.3 Ω at 3.3-V input voltage and is configured as a high-side switch. When operating, the p-channel MOSFET quiescent current is reduced to less than 1.5 μA.

charge pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

driver

The driver controls the gate voltage of the IN1-OUT and IN2-OUT power switches. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the drivers incorporate circuitry that controls the rise times and fall times of the output voltage.

detailed description (continued)

enable

The logic enable will turn on the IN2-OUT power switch when a logic high is present on $\overline{EN}$ (TPS2100) or logic low is present on EN (TPS2101). A logic low input on $\overline{EN}$ (TPS2100) or logic high on EN (TPS2101) restores bias to the drive and control circuits and turns on the IN1-OUT power switch. The enable input is compatible with both TTL and CMOS logic levels.

the V_{AUX} application for CardBus controllers

The PC Card specification requires the support of V_{AUX} to the CardBus controller as well as to the PC Card sockets. Both are 3.3-V requirements; however the CardBus controller's current demand from the V_{AUX} supply is limited to 10 μA, whereas the PC Card may consume as much as 200 mA. In either implementation, if support of a wake-up event is required, the controller and the socket will transition from the 3.3-V V_{CC} rail to the 3.3-V V_{AUX} rail when the equipment moves into a low power mode such as D3. The transition from V_{CC} to V_{AUX} needs to be seamless in order to maintain all memory and register information in the system. If V_{AUX} is not supported, the system will lose all register information when it transitions to the D3 state.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Input voltage range, $V_{I(IN1)}$ (see Note1) ..... −0.3 V to 5 V
Input voltage range, $V_{I(IN2)}$ (see Note1) ..... −0.3 V to 5 V
Input voltage range, V_I at $\overline{EN}$ or EN ..... −0.3 V to 5 V
Output voltage range, V_O (see Note 1) ..... −0.3 V to 5 V
Continuous output current, $I_{O(IN1)}$ ..... 700 mA
Continuous output current, $I_{O(IN2)}$ ..... 70 mA
Continuous total power dissipation ..... See dissipation rating table
Operating virtual junction temperature range, T_J ..... −40°C to 85°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C
Electrostatic discharge (ESD) protection: Human body model ..... 2 kV
Machine model ..... 200 V
Charged device model (CDM) ..... 750 V

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DBV	309 mW	3.1 mW/°C	170 mW	123 mW
D	568 mW	5.7 mW/°C	313 mW	227 mW

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, $V_{I(INx)}$	2.7	4	V
Input voltage, V_I at $\overline{EN}$ and EN	0	4	V
Continuous output current, $I_{O(IN1)}$		500	mA
Continuous output current, $I_{O(IN2)}$		10	mA
Operating virtual junction temperature, T_J	−40	85	°C

electrical characteristics over recommended operating junction temperature range, $V_{I(IN1)} = V_{(IN2)} = 3.3$ V, I_O = rated current (unless otherwise noted)

power switch

PARAMETER			TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$r_{DS(on)}$ On-state resistance		IN1–OUT	T_J = 25°C		250		mΩ
			T_J = 85°C		300	375	
		IN2–OUT	T_J = 25°C		1.3		Ω
			T_J = 85°C		1.5	2.1	

† Pulse-testing techniques maintain junction temperature close to ambient termperature; thermal effects must be taken into account separately.

enable input ($\overline{EN}$ and EN)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	2.7 V ≤ $V_{I(INx)}$ ≤ 4 V		2			V
V_{IL}	Low-level input voltage	2.7 V ≤ $V_{I(INx)}$ ≤ 4 V				0.8	V
I_I	Input current	TPS2100	$\overline{EN}$ = 0 V or $\overline{EN}$ = $V_{I(INx)}$	–0.5		0.5	µA
		TPS2101	EN = 0 V or EN = $V_{I(INx)}$	–0.5		0.5	µA

supply current

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_I Supply current	TPS2100	$\overline{EN}$ = H, IN2 selected	T_J = 25°C		0.75		µA
			–40°C ≤ T_J ≤ 85°C			1.5	
		$\overline{EN}$ = L, IN1 selected	T_J = 25°C		10		µA
			–40°C ≤ T_J ≤ 85°C			16	
	TPS2101	EN = L, IN2 selected	T_J = 25°C		0.75		µA
			–40°C ≤ T_J ≤ 85°C			1.5	
		EN = H, IN1 selected	T_J = 25°C		10		µA
			–40°C ≤ T_J ≤ 85°C			16	

switching characteristics, T_J = 25°C, $V_{I(IN1)}$ = $V_{I(IN2)}$ = 3.3 V (unless otherwise noted)†

PARAMETER			TEST CONDITIONS†		MIN	TYP	MAX	UNIT
t_r	Output rise time	IN1-OUT	$V_{I(IN2)}$ = 0	C_L = 1 µF, I_L = 500 mA		830		µs
				C_L = 10 µF, I_L = 500 mA		840		
				C_L = 1 µF, I_L = 10 mA		640		
		IN2-OUT	$V_{I(IN1)}$ = 0	C_L = 1 µF, I_L = 10 mA		5.5		
				C_L = 10 µF, I_L = 10 mA		70		
				C_L = 1 µF, I_L = 1 mA		5.5		
t_f	Output fall time	IN1-OUT	$V_{I(IN2)}$ = 0	C_L = 1 µF, I_L = 500 mA		8		µs
				C_L = 10 µF, I_L = 500 mA		93		
				C_L = 1 µF, I_L = 10 mA		23		
		IN2-OUT	$V_{I(IN1)}$ = 0	C_L = 1 µF, I_L = 10 mA		690		
				C_L = 10 µF, I_L = 10 mA		6900		
				C_L = 1 µF, I_L = 1 mA		6900		
t_{PLH}	Propagation delay time, low-to-high output	IN1-OUT	$V_{I(IN2)}$ = 0	C_L = 10 µF, I_L = 10 mA		75		µs
		IN2-OUT	$V_{I(IN1)}$ = 0			2		
t_{PHL}	Propagation delay time, high-to-low output	IN1-OUT	$V_{I(IN2)}$ = 0	C_L = 10 µF, I_L = 10 mA		3		µs
		IN2-OUT	$V_{I(IN1)}$ = 0			370		

† All timing parameters refer to Figure 3.

PARAMETER MEASUREMENT INFORMATION

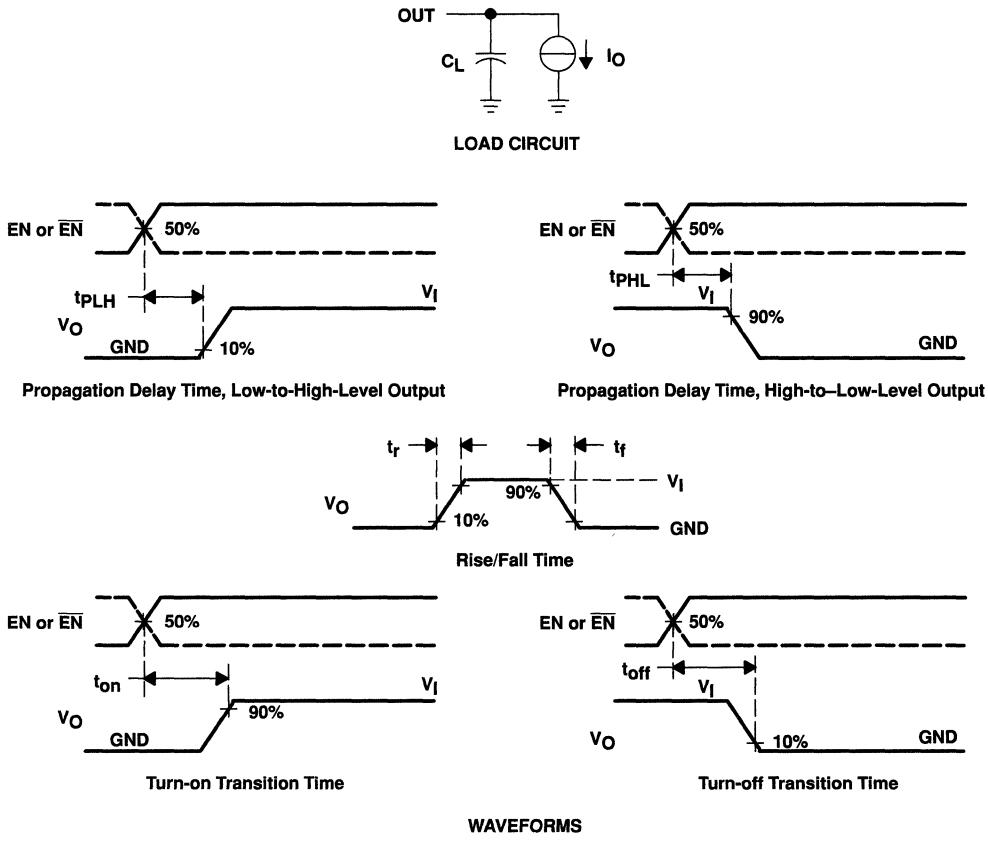


Figure 3. Test Circuit and Voltage Waveforms

Table of Timing Diagrams†

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Propagation Delay and Fall Time With 0.1-μF Load, IN2	7
Propagation Delay and Rise Time With 1-μF Load, IN1	8
Propagation Delay and Rise Time With 1-μF Load, IN2	9
Propagation Delay and Fall Time With 1-μF Load, IN1	10
Propagation Delay and Fall Time With 1-μF Load, IN2	11

† Waveforms shown in Figures 4–11 refer to TPS2100 at T_J = 25°C

PARAMETER MEASUREMENT INFORMATION

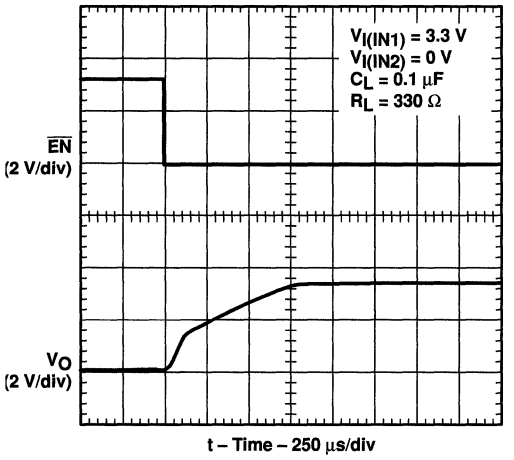

Figure 4. Propagation Delay and Rise Time With 0.1-μF Load, IN1

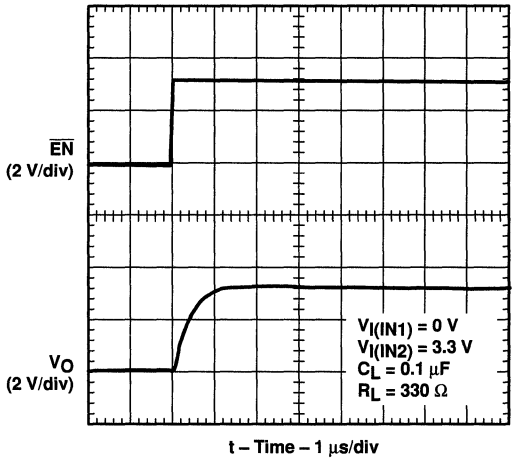

Figure 5. Propagation Delay and Fall Time With 0.1-μF Load, IN2

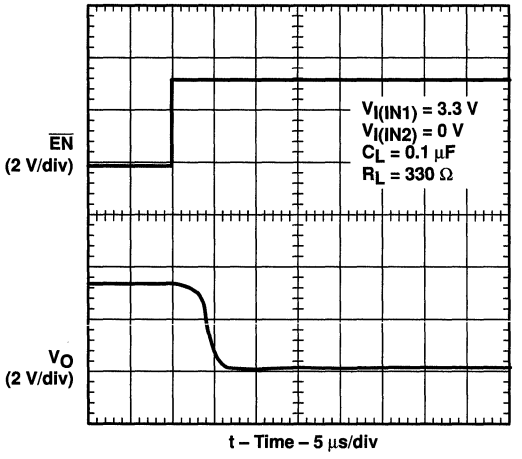

Figure 6. Propagation Delay and Fall Time With 0.1-μF Load, IN1

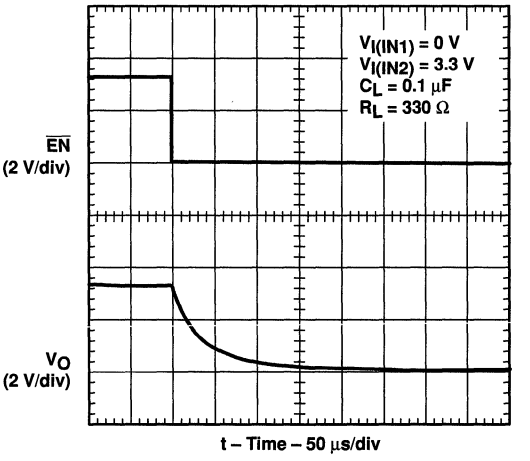

Figure 7. Propagation Delay and Fall Time With 0.1-μF Load, IN2

PARAMETER MEASUREMENT INFORMATION

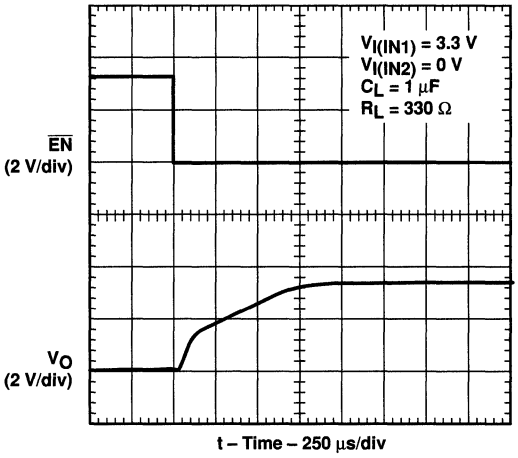

Figure 8. Propagation Delay and Rise Time With 1-μF Load, IN1

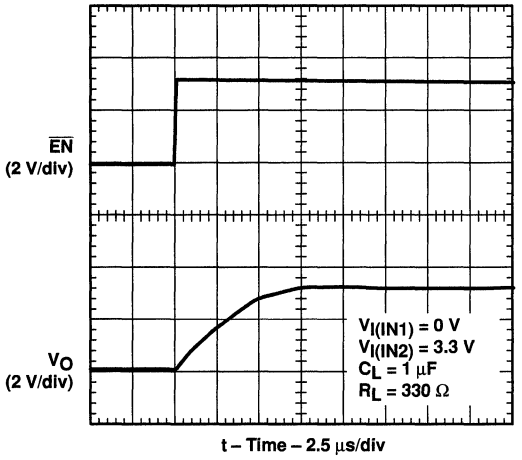

Figure 9. Propagation Delay and Rise Time With 1-μF Load, IN2

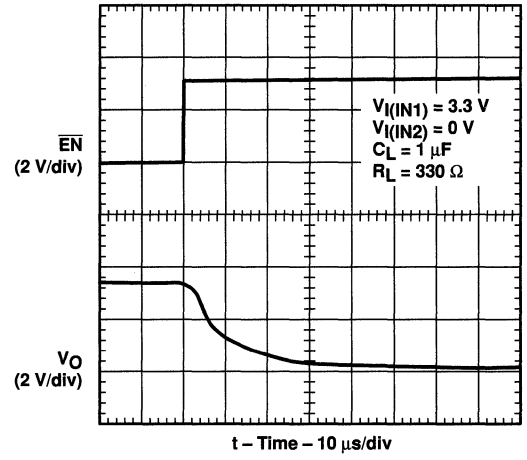

Figure 10. Propagation Delay and Fall Time With 1-μF Load, IN1

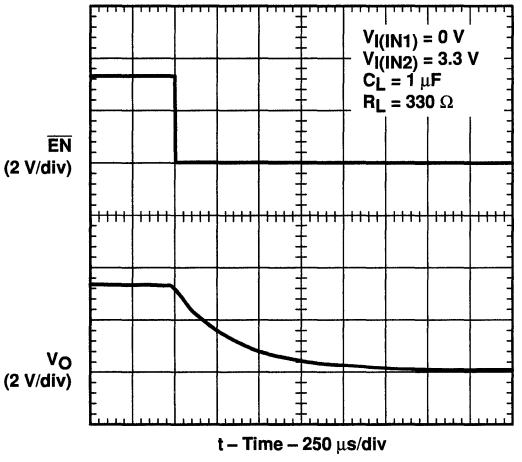

Figure 11. Propagation Delay and Fall Time With 1-μF Load, IN2

TYPICAL CHARACTERISTICS

Table of Graphs

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IN1 Switch Rise Time	vs Output Current	12
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IN1 Supply Current	vs Junction Temperature (IN1 Disabled)	19
IN2 Supply Current	vs Junction Temperature (IN2 Enabled)	20
IN2 Supply Current	vs Junction Temperature (IN2 Disabled)	21
IN1-OUT On-State Resistance	vs Junction Temperature	22
IN2-OUT On-State Resistance	vs Junction Temperature	23

IN1 SWTICH RISE TIME vs OUTPUT CURRENT

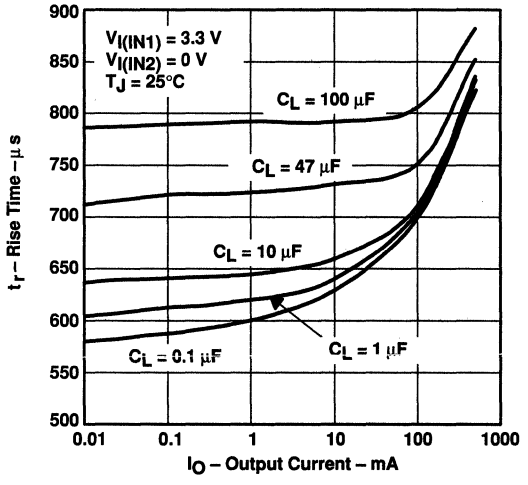


Figure 12

IN2 SWTICH RISE TIME vs OUTPUT CURRENT

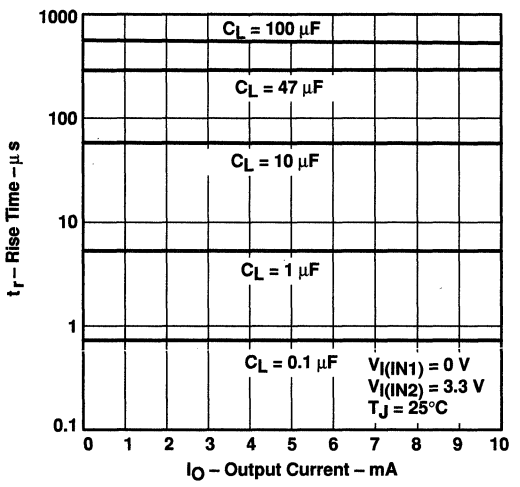


Figure 13

TYPICAL CHARACTERISTICS

IN1 SWITCH FALL TIME vs OUTPUT CURRENT

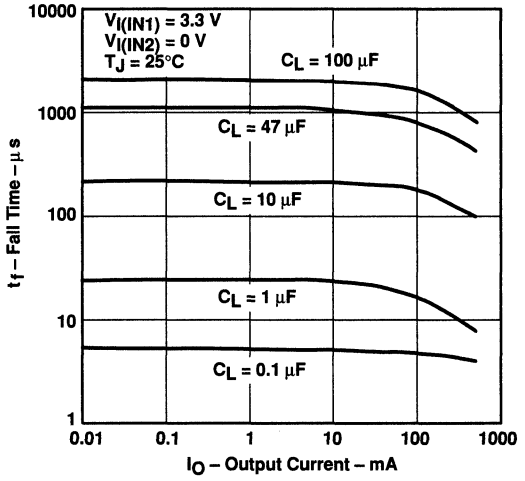


Figure 14

IN2 SWITCH FALL TIME vs OUTPUT CURRENT

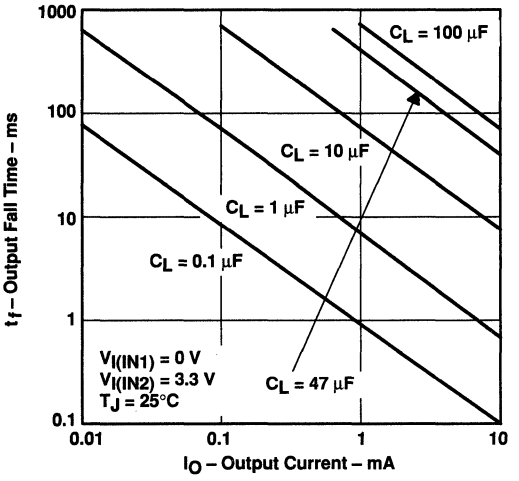


Figure 15

OUTPUT VOLTAGE DROOP vs OUTPUT CURRENT WHEN OUTPUT IS SWITCHED FROM IN2 TO IN1

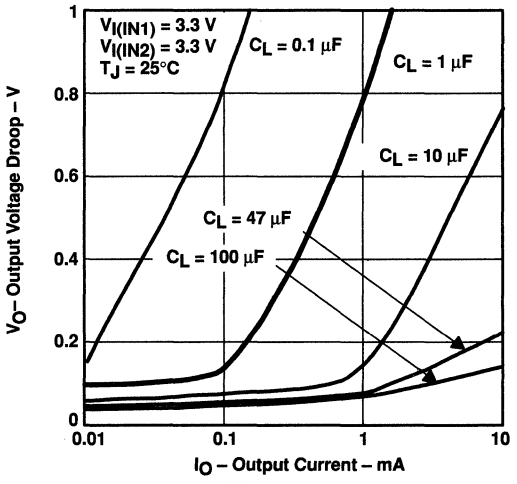


Figure 16

INRUSH CURRENT vs OUTPUT CAPACITANCE

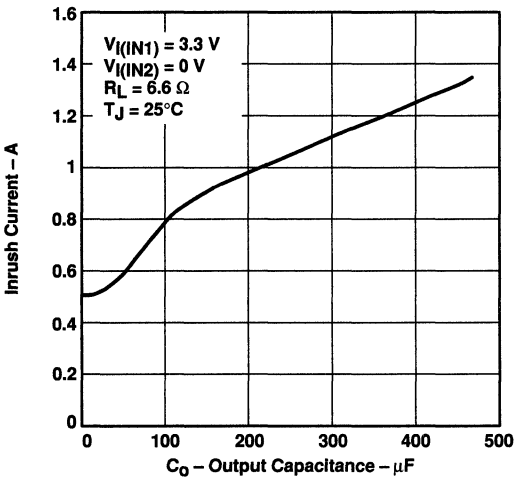


Figure 17

TYPICAL CHARACTERISTICS

IN1 SUPPLY CURRENT
vs
JUNCTION TEMPERATURE (IN1 ENABLED)

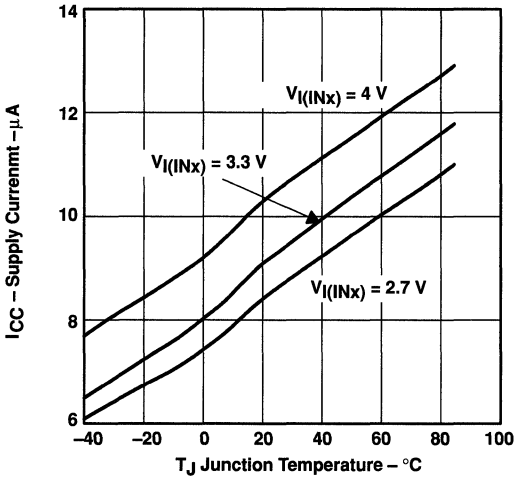


Figure 18

IN1 SUPPLY CURRENT
vs
JUNCTION TEMPERATURE (IN1 DISABLED)

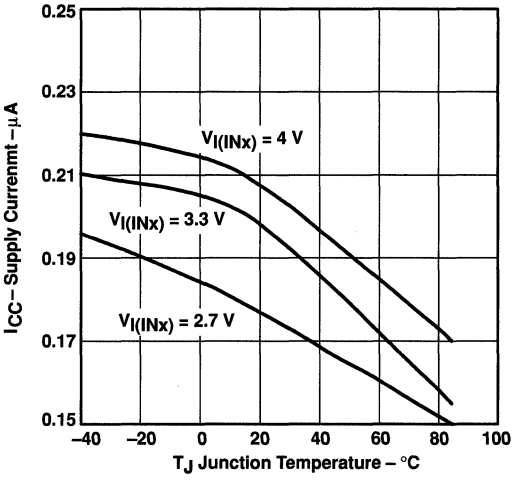


Figure 19

IN2 SUPPLY CURRENT
vs
JUNCTION TEMPERATURE (IN2 ENABLED)

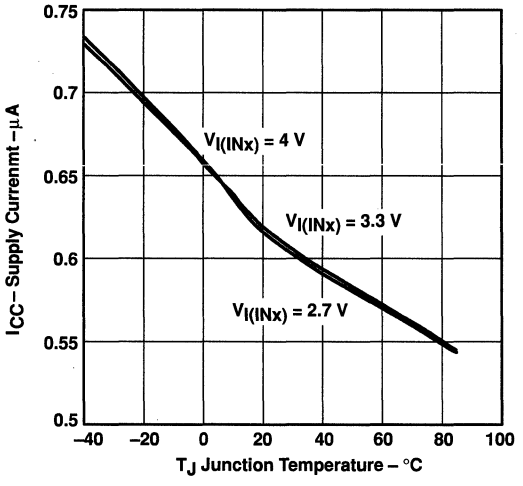


Figure 20

IN2 SUPPLY CURRENT
vs
JUNCTION TEMPERATURE (IN2 DISABLED)

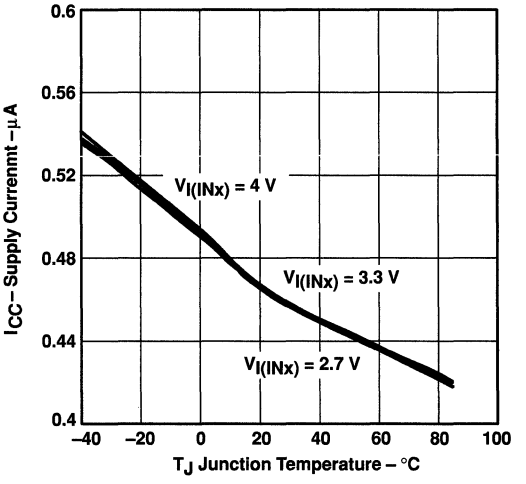


Figure 21

TYPICAL CHARACTERISTICS

IN1-OUT ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

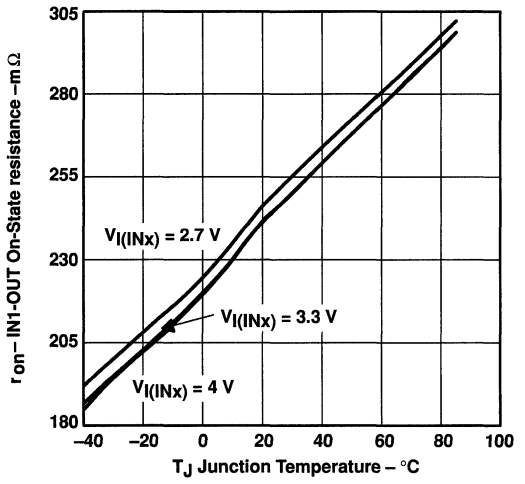


Figure 22

IN2-OUT ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

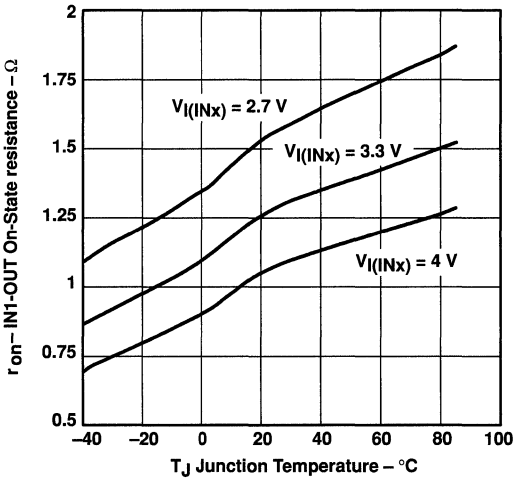


Figure 23

APPLICATION INFORMATION

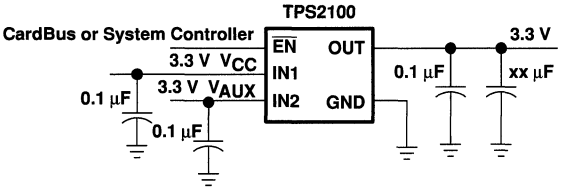


Figure 24. Typical Application

power supply considerations

A 0.01-µF to 0.1-µF ceramic bypass capacitor between IN and GND, close to the device is recommended. The output capacitor should be chosen based on the size of the load during the transition of the switch. A 47-µF capacitor is recommended for 10-mA loads. Typical output capacitors (xx µF, shown in Figure 24) required for a given load can be determined from Figure 16 which shows the output voltage droop when output is switched from IN2 to IN1. The output voltage droop is insignificant when output is switched from IN1 to IN2. Additionally, bypassing the output with a 0.01-µF to 0.1-µF ceramic capacitor improves the immunity of the device to short-circuit transients.

APPLICATION INFORMATION

power supply considerations (continued)

switch transition

The n-channel MOSFET on IN1 uses a charge-pump to create the gate-drive voltage, which gives the IN1 switch a rise time of approximately 1 ms. The p-channel MOSFET on IN2 has a simpler drive circuit that allows a rise time of approximately 8 µs. Because the device has two switches and a single enable pin, these rise times are seen as transition times, from IN1 to IN2, or IN2 to IN1, by the output. The controlled transition times help limit the surge currents seen by the power supply during switching.

thermal protection

Thermal protection provided on the IN1 switch prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The increased dissipation causes the junction temperature to rise to dangerously high levels. The protection circuit senses the junction temperature of the switch and shuts it off at approximately 125°C (T_J). The switch remains off until the junction temperature has dropped. The switch continues to cycle in this manner until the load fault or input power is removed.

undervoltage lockout

An undervoltage lockout function is provided to ensure that the power switch is in the off state at power-up. Whenever the input voltage falls below approximately 2 V, the power switch quickly turns off. This function facilitates the design of hot-insertion systems that may not have the capability to turn off the power switch before input power is removed. Upon reinsertion, the power switch will be turned on with a controlled rise time to reduce EMI and voltage overshoots.

power dissipation and junction temperature

The low on-resistance on the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistances of these packages are high compared to that of power packages; it is good design practice to check power dissipation and junction temperature. First, find r_{on} at the input voltage, and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read r_{on} from Figure 22 or Figure 23. Next calculate the power dissipation using:

$$P_D = r_{on} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where

T_A = Ambient temperature

$R_{\theta JA}$ = Thermal resistance

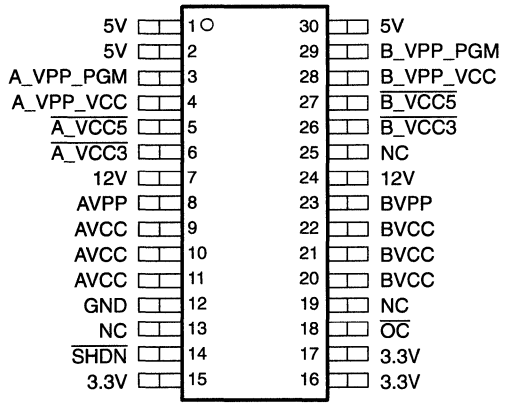
Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation using the calculated value as the new estimate. Two or three iterations are generally sufficient to obtain a reasonable answer.

ESD protection

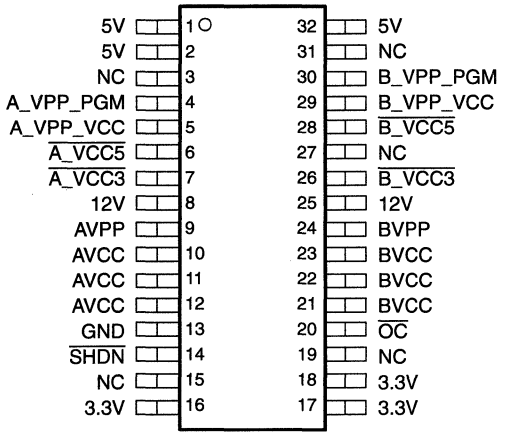
All TPS2100 and TPS2101 terminals incorporate ESD-protection circuitry designed to withstand a 2-kV human-body-model discharge as defined in MIL-STD-883C.

- **Fully Integrated V_{CC} and V_{pp} Switching for Dual-Slot PC Card™ Interface**
- **Compatible with Controllers From Cirrus, Ricoh, O_2Micro, Intel, and Texas Instruments**
- **3.3-V Low-Voltage Mode**
- **Meets PC Card Standards**
- **12-V Supply Can Be Disabled Except During 12-V Flash Programming**
- **Short Circuit and Thermal Protection**
- **30-Pin SSOP (DB) and 32-Pin TSSOP (DAP)**
- **Compatible With 3.3-V, 5-V and 12-V PC Cards**
- **Low $r_{DS(on)}$ (140-mΩ 5-V V_{CC} Switch; 110-mΩ 3.3-V V_{CC} Switch)**
- **Break-Before-Make Switching**

DB OR DF PACKAGE
(TOP VIEW)



DAP PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TPS2205 PC Card power-interface switch provides an integrated power-management solution for two PC Cards. All of the discrete power MOSFETs, a logic section, current limiting, and thermal protection for PC Card control are combined on a single integrated circuit (IC), using the Texas Instruments LinBiCMOS™ process. The circuit allows the distribution of 3.3-V, 5-V, and/or 12-V card power, and is compatible with many PCMCIA controllers. The current-limiting feature eliminates the need for fuses, which reduces component count and improves reliability.

The TPS2205 is backward compatible with the TPS2201, except that there is no V_{DD} connection. Bias current is derived from either the 3.3-V input pin or the 5-V input pin. The TPS2205 also eliminates the APWR_GOOD and BPWR_GOOD pins of the TPS2201.

The TPS2205 features a 3.3-V low-voltage mode that allows for 3.3-V switching without the need for 5 V. This facilitates low-power system designs such as sleep mode and pager mode where only 3.3 V is available.

End equipment for the TPS2205 includes notebook computers, desktop computers, personal digital assistants (PDAs), digital cameras, and bar-code scanners.

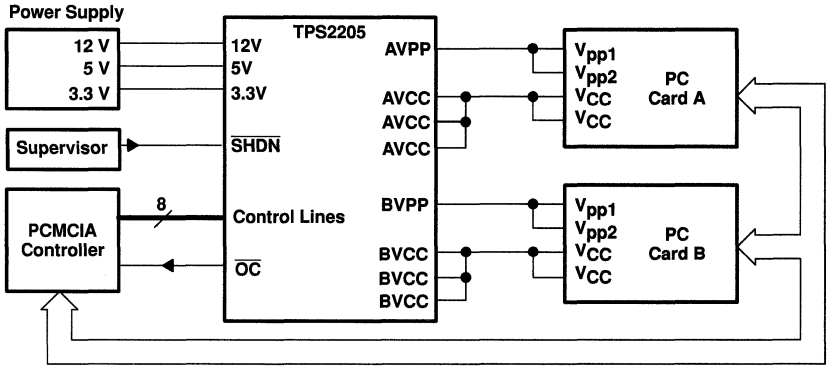
LinBiCMOS is a trademark of Texas Instruments Incorporated.
PC Card is a trademark of PCMCIA (Personal Computer Memory Card International Association).

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES			CHIP FORM (Y)
	PLASTIC SMALL OUTLINE (DB)	PLASTIC SMALL OUTLINE (DF)	TSSOP (DAP)	
–40°C to 85°C	TPS2205IDBLE	TPS2205IDFLE	TPS2205IDAPR	TPS2205Y

The DB package and the DF package are only available left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TPS2205IDBLE). The DAP package is only available taped and reeled (indicated by the R suffix on the device type; e.g., TPS2205IDAPR).

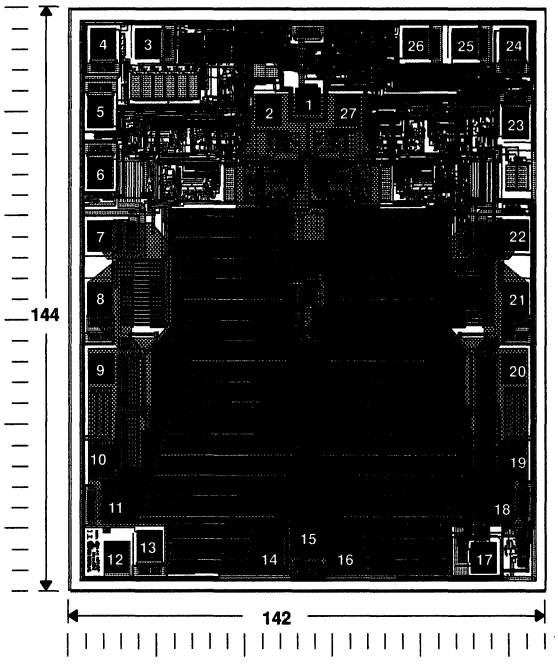
typical PC card power-distribution application

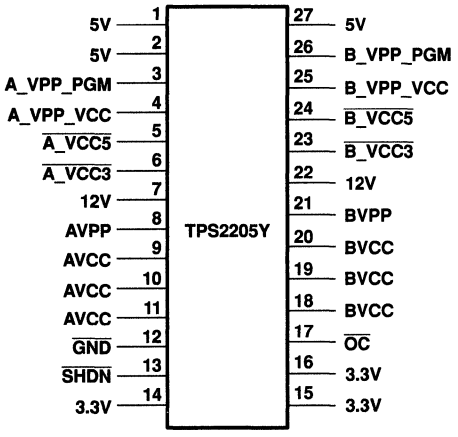


TPS2205Y chip information

This chip, when properly assembled, displays characteristics similar to those of the TPS2205. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	DB, DF	DAP		
$\overline{\text{A\_VCC3}}$	6	7	I	Logic input that controls voltage on AVCC (see TPS2205 Control-Logic table)
$\overline{\text{A\_VCC5}}$	5	6	I	Logic input that controls voltage on AVCC (see TPS2205 Control-Logic table)
A_VPP_PGM	3	4	I	Logic input that controls voltage on AVPP (see TPS2205 Control-Logic table)
A_VPP_VCC	4	5	I	Logic input that controls voltage on AVPP (see TPS2205 Control-Logic table)
AVCC	9, 10, 11	10, 11, 12	O	Switched output that delivers 0 V, 3.3 V, 5 V, or high impedance
AVPP	8	9	O	Switched output that delivers 0 V, 3.3 V, 5 V, 12 V, or high impedance
$\overline{\text{B\_VCC3}}$	26	26	I	Logic input that controls voltage on BVCC (see TPS2205 Control-Logic table)
$\overline{\text{B\_VCC5}}$	27	28	I	Logic input that controls voltage on BVCC (see TPS2205 Control-Logic table)
B_VPP_PGM	29	30	I	Logic input that controls voltage on BVPP (see TPS2205 Control-Logic table)
B_VPP_VCC	28	29	I	Logic input that controls voltage on BVPP (see TPS2205 Control-Logic table)
BVCC	20, 21, 22	21, 22, 23	O	Switched output that delivers 0 V, 3.3 V, 5 V, or high impedance
BVPP	23	24	O	Switched output that delivers 0 V, 3.3 V, 5 V, 12 V, or high impedance
$\overline{\text{SHDN}}$	14	14	I	Logic input that shuts down the TPS2205 and set all power outputs to high-impedance state
$\overline{\text{OC}}$	18	20	O	Logic-level overcurrent reporting output that goes low when an overcurrent condition exists
GND	12	13		Ground
3.3V	15, 16, 17	16, 17, 18	I	3.3-V V_{CC} in for card power
5V	1, 2, 30	1, 2, 32	I	5-V V_{CC} in for card power
12V	7, 24	8, 25	I	12-V VPP in for card power
NC	13, 19, 25	3, 15, 19, 27, 31	I	No internal connection

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Input voltage range for card power: $V_{I(5V)}$ . . . . . −0.3 V to 7 V
$V_{I(3.3V)}$ . . . . . −0.3 V to 7 V
$V_{I(12V)}$ . . . . . −0.3 V to 14 V
Logic input voltage . . . . . −0.3 V to 7 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Output current (each card): $I_{O(xVCC)}$ . . . . . Internally limited
$I_{O(xVPP)}$ . . . . . Internally limited
Operating virtual junction temperature range, T_J . . . . . −40°C to 150°C
Operating free-air temperature range, T_A . . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . . −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE		$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DB		1024 mW	8.2 mW/°C	655 mW	532 mW
DF		1158 mW	9.26 mW/°C	741 mW	602 mW
DAP	No backplane	1625 mW	13 mW/°C	1040 mW	845 mW
	Backplane§	6044 mW	48.36 mW/°C	3869 mW	3143 mW

‡ These devices are mounted on an FR4 board with no special thermal considerations.
§ 2-oz backplane with 2-oz traces; 5.2-mm × 11-mm thermal pad with 6-mil solder; 0.18-mm diameter vias in a 3×6 array.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage range, V_I	$V_{I(5V)}$	0	5.25	V
	$V_{I(3.3V)}$	0	5.25	V
	$V_{I(12V)}$	0	13.5	V
Output current	$I_{O(xVCC)}$ at 25°C		1	A
	$I_{O(xVPP)}$ at 25°C		150	mA
Operating virtual junction temperature, T_J		−40	125	°C

electrical characteristics, $T_A = 25°C$, $V_{I(5V)} = 5$ V (unless otherwise noted)

dc characteristics

PARAMETER			TEST CONDITIONS		TPS2205 MIN	TPS2205 TYP	TPS2205 MAX	UNIT
	Switch resistances†	5 V to xVCC				103	140	mΩ
		3.3 V to xVCC	$V_{I(5V)}$ = 5 V,	$V_{I(3.3\ V)}$ = 3.3 V		69	110	
		3.3 V to xVCC	$V_{I(5V)}$ = 0,	$V_{I(3.3V)}$ = 3.3 V		96	180	
		5 V to xVPP					6	Ω
		3.3 V to xVPP					6	
		12 V to xVPP					1	
$V_{O(xVPP)}$	Clamp low voltage		I_{pp} at 10 mA				0.8	V
$V_{O(xVCC)}$	Clamp low voltage		I_{CC} at 10 mA				0.8	V
I_{lkg}	Leakage current	I_{pp} high-impedance state	$T_A = 25°C$			1	10	µA
			$T_A = 85°C$				50	
		I_{CC} high-impedance state	$T_A = 25°C$			1	10	
			$T_A = 85°C$				50	
I_I	Input current	$V_{I(5V)}$ = 5 V	$V_{O(AVCC)} = V_{O(BVCC)}$ = 5 V, $V_{O(AVPP)} = V_{O(BVPP)}$ = 12 V			117	150	µA
		$V_{I(5V)}$ = 0, $V_{I(3.3V)}$ = 3.3 V	$V_{O(AVCC)} = V_{O(BVCC)}$ = 3.3 V, $V_{O(AVPP)} = V_{O(BVPP)}$ = 0			131	150	
		Shutdown mode	$V_{O(BVCC)} = V_{O(AVCC)} = V_{O(AVPP)} = V_{O(BVPP)}$ = Hi-Z				1	µA
I_{OS}	Short-circuit output-current limit	$I_{O(xVCC)}$	$T_J = 85°C$, Output powered up into a short to GND		1		2.2	A
		$I_{O(xVPP)}$			120		400	mA

† Pulse-testing techniques are used to maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics, T_A = 25°C, $V_{I(5V)}$ = 5 V (unless otherwise noted)

logic section

PARAMETER	TEST CONDITIONS	TPS2205 MIN	TPS2205 MAX	UNIT
Logic input current			1	μA
Logic input high level		2		V
Logic input low level			0.8	V
Logic output high level	$V_{I(5V)}$= 5 V, I_O = 1mA	$V_{I(5V)}$–0.4		V
	$V_{I(5V)}$= 0 V, I_O = 1mA, $V_{I(3.3V)}$ = 3.3 V	$V_{I(3.3V)}$–0.4		
Logic output low level	I_O = 1mA		0.4	V

switching characteristics†‡

PARAMETER		TEST CONDITIONS		TPS2205 MIN	TPS2205 TYP	TPS2205 MAX	UNIT
t_r	Output rise time	$V_{O(xVCC)}$			1.2		ms
		$V_{O(xVPP)}$			5		
t_f	Output fall time	$V_{O(xVCC)}$			10		
		$V_{O(xVPP)}$			14		
t_{pd}	Propagation delay (see Figure 1)	$V_{I(x\_VPP\_PGM)}$ to $V_{O(xVPP)}$	t_{on}		4.4		ms
			t_{off}		18		ms
		$V_{I(\overline{x\_VCC5})}$ to xVCC (3.3 V), $V_{I(5V)}$ = 5 V	t_{on}		6.5		ms
			t_{off}		20		ms
		$V_{I(\overline{x\_VCC5})}$ to xVCC (5 V)	t_{on}		5.7		ms
			t_{off}		25		ms
		$V_{I(\overline{x\_VCC5})}$ to xVCC (3.3 V), $V_{I(5V)}$ = 0	t_{on}		6.6		ms
			t_{off}		21		ms

† Refer to Parameter Measurement Information
‡ Switching Characteristics are with C_L = 150 μF.

electrical characteristics, T_A = 25°C, $V_{I(5V)}$ = 5 V (unless otherwise noted)

dc characteristics

PARAMETER			TEST CONDITIONS	TPS2205Y MIN	TPS2205Y TYP	TPS2205Y MAX	UNIT
	Switch resistances§	5 V to xVCC			103		mΩ
		3.3 V to xVCC	$V_{I(5V)}$ = 5 V, $V_{I(3.3\ V)}$ = 3.3 V		69		
		3.3 V to xVCC	$V_{I(5V)}$ = 0, $V_{I(3.3V)}$ = 3.3 V		96		
		5 V to xVPP			4.74		Ω
		3.3 V to xVPP			4.74		
		12 V to xVPP			0.724		
$V_{O(xVPP)}$	Clamp low voltage		I_{pp} at 10 mA		0.275		V
$V_{O(xVCC)}$	Clamp low voltage		I_{CC} at 10 mA		0.275		V
I_{lkg}	Leakage current	I_{pp} High-impedance state	T_A = 25°C		1		μA
		I_{CC} High-impedance state	T_A = 25°C		1		
I_I	Input current	$V_{I(5V)}$ = 5 V	$V_{O(AVCC)}$ = $V_{O(BVCC)}$ = 5 V, $V_{O(AVPP)}$ = $V_{O(BVPP)}$ = 12 V		117		μA
		$V_{I(5V)}$ = 0, $V_{I(3.3V)}$ = 3.3 V	$V_{O(AVCC)}$ = $V_{O(BVCC)}$ = 3.3 V, $V_{O(AVPP)}$ = $V_{O(BVPP)}$ = 0		131		

§ Pulse-testing techniques are used to maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

switching characteristics†‡

PARAMETER		TEST CONDITIONS		TPS2205Y MIN	TPS2205Y TYP	TPS2205Y MAX	UNIT
t_r	Output rise time	$V_{O(xVCC)}$			1.2		ms
		$V_{O(xVPP)}$			5		
t_f	Output fall time	$V_{O(xVCC)}$			10		
		$V_{O(xVPP)}$			14		
t_{pd}	Propagation delay (see Figure 1)	$V_{I(x\_VPP\_PGM)}$ to $V_{O(xVPP)}$	t_{on}		4.4		ms
			t_{off}		18		ms
		$V_{I(x\_VCC5)}$ to xVCC (3.3 V), $V_{I(5V)}$ = 5 V	t_{on}		6.5		ms
			t_{off}		20		ms
		$V_{I(x\_VCC5)}$ to xVCC (5 V)	t_{on}		5.7		ms
			t_{off}		25		ms
		$V_{I(x\_VCC5)}$ to xVCC (3.3 V), $V_{I(5V)}$ = 0	t_{on}		6.6		ms
			t_{off}		21		ms

† Refer to Parameter Measurement Information
‡ Switching Characteristics are with C_L = 150 μF.

PARAMETER MEASUREMENT INFORMATION

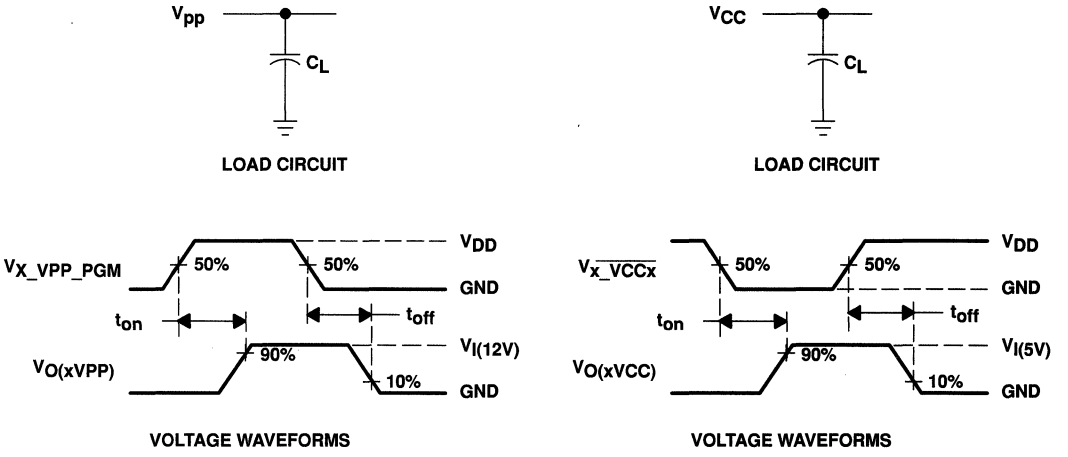


Figure 1. Test Circuits and Voltage Waveforms

Table of Timing Diagrams

	FIGURE
xVCC Propagation Delay and Rise Time With 1-µF Load, 3.3-V Switch, $V_{I(5V)}$ = 5 V	2
xVCC Propagation Delay and Fall Time With 1-µF Load, 3.3-V Switch, $V_{I(5V)}$ = 5 V	3
xVCC Propagation Delay and Rise Time With 150-µF Load, 3.3-V Switch, $V_{I(5V)}$ = 5 V	4
xVCC Propagation Delay and Fall Time With 150-µF Load, 3.3-V Switch, $V_{I(5V)}$ = 5 V	5
xVCC Propagation Delay and Rise Time With 1-µF Load, 3.3-V Switch, $V_{I(5V)}$ = 0	6
xVCC Propagation Delay and Fall Time With 1-µF Load, 3.3-V Switch, $V_{I(5V)}$ = 0	7
xVCC Propagation Delay and Rise Time With 150-µF Load, 3.3-V Switch, $V_{I(5V)}$ = 0	8
xVCC Propagation Delay and Fall Time With 150-µF Load, 3.3-V Switch, $V_{I(5V)}$ = 0	9
xVCC Propagation Delay and Rise Time With 1-µF Load, 5-V Switch	10
xVCC Propagation Delay and Fall Time With 1-µF Load, 5-V Switch	11
xVCC Propagation Delay and Rise Time With 150-µF Load, 5-V Switch	12
xVCC Propagation Delay and Fall Time With 150-µF Load, 5-V Switch	13
xVPP Propagation Delay and Rise Time With 1-µF Load, 12-V Switch	14
xVPP Propagation Delay and Fall Time With 1-µF Load, 12-V Switch	15
xVPP Propagation Delay and Rise Time With 150-µF Load, 12-V Switch	16
xVPP Propagation Delay and Fall Time With 150-µF Load, 12-V Switch	17

PARAMETER MEASUREMENT INFORMATION

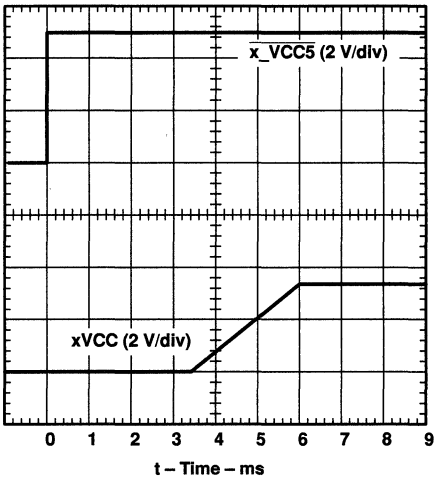


Figure 2. xVCC Propagation Delay and Rise Time With 1-μF Load, 3.3-V Switch, ($V_{I(5\ V)}$ = 5 V)

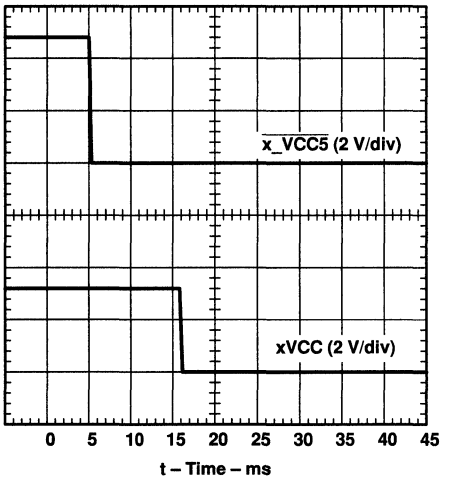


Figure 3. xVCC Propagation Delay and Fall Time With 1-μF Load, 3.3-V Switch, ($V_{I(5\ V)}$ = 5 V)

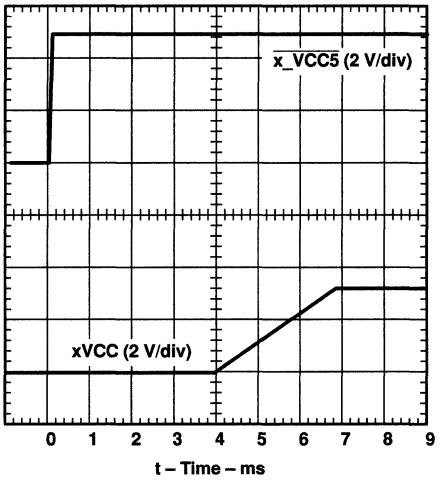


Figure 4. xVCC Propagation Delay and Rise Time With 150-μF Load, 3.3-V Switch, $V_{I(5\ V)}$ = 5 V

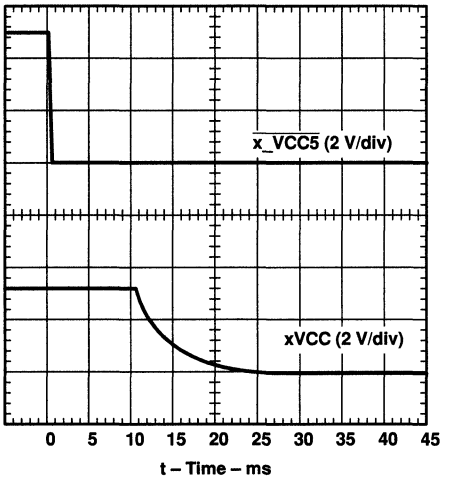


Figure 5. xVCC Propagation Delay and Fall Time With 150-μF Load, 3.3-V Switch, $V_{I(5\ V)}$ = 5 V

PARAMETER MEASUREMENT INFORMATION

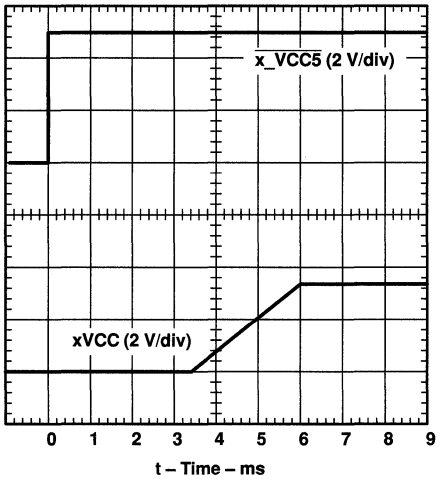


Figure 6. xVCC Propagation Delay and Rise Time With 1-μF Load, 3.3-V Switch, $V_{I(5\ V)}$ = 0

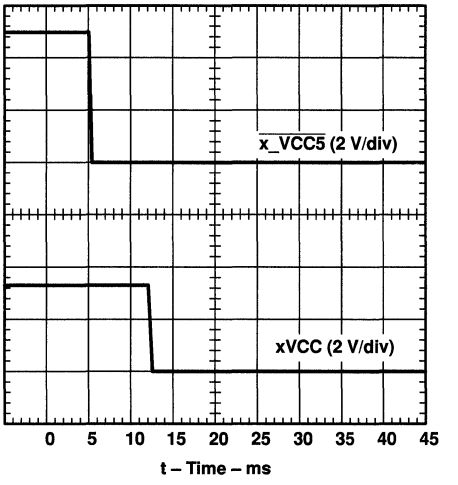


Figure 7. xVCC Propagation Delay and Fall Time With 1-μF Load, 3.3-V Switch, $V_{I(5\ V)}$ = 0

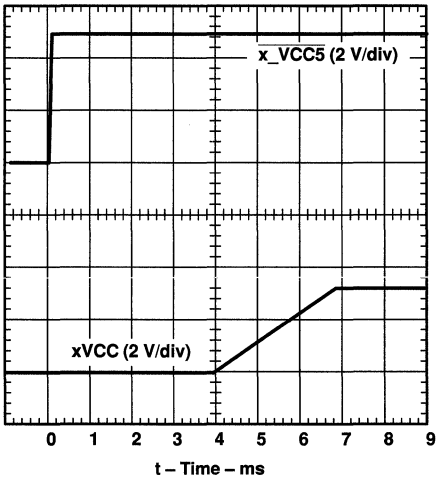


Figure 8. xVCC Propagation Delay and Rise Time With 150-μF Load, 3.3-V Switch, $V_{I(5\ V)}$ = 0

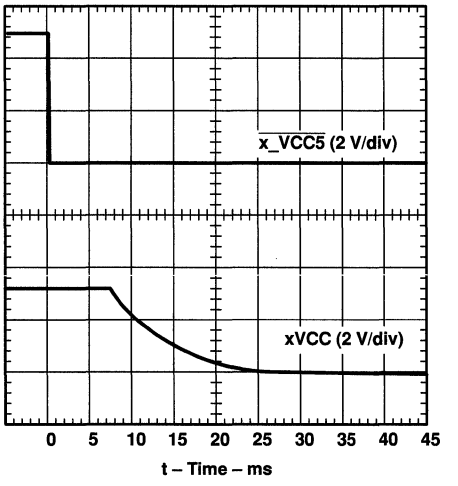


Figure 9. xVCC Propagation Delay and Fall Time With 150-μF Load, 3.3-V Switch, $V_{I(5\ V)}$ = 0

PARAMETER MEASUREMENT INFORMATION

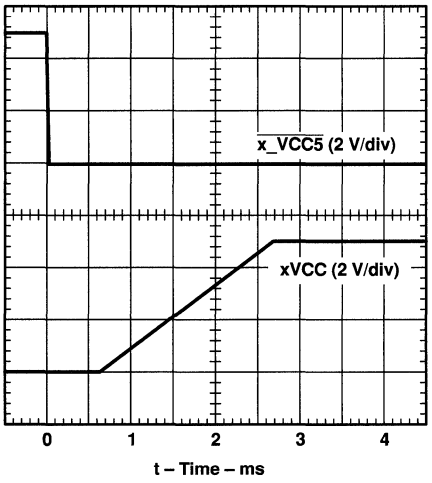


Figure 10. xVCC Propagation Delay and Rise Time With 1-μF Load, 5-V Switch

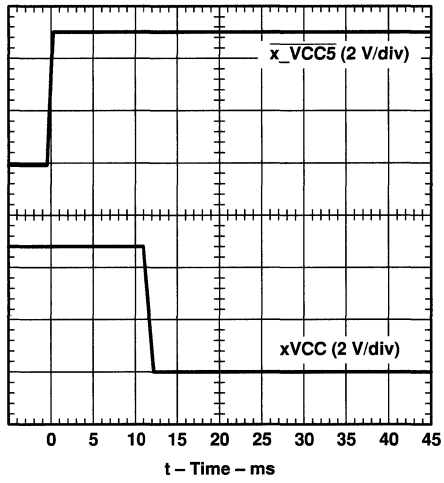


Figure 11. xVCC Propagation Delay and Fall Time With 1-μF Load, 5-V Switch

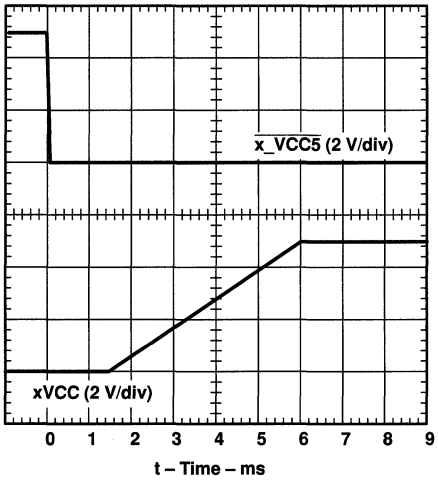


Figure 12. xVCC Propagation Delay and Rise Time With 150-μF Load, 5-V Switch

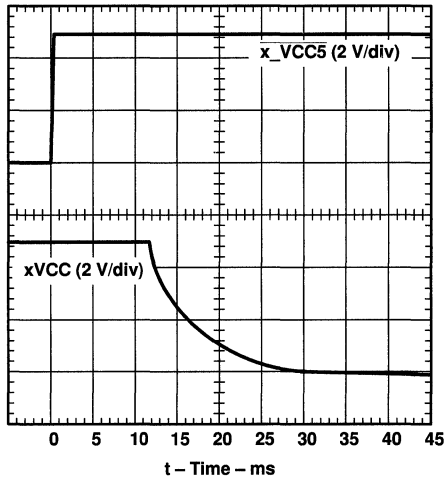


Figure 13. xVCC Propagation Delay and Fall Time With 150-μF Load, 5-V Switch

PARAMETER MEASUREMENT INFORMATION

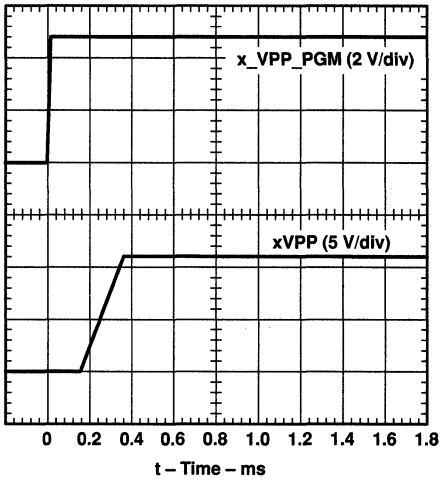


Figure 14. xVPP Propagation Delay and Rise Time With 1-μF Load, 12-V Switch

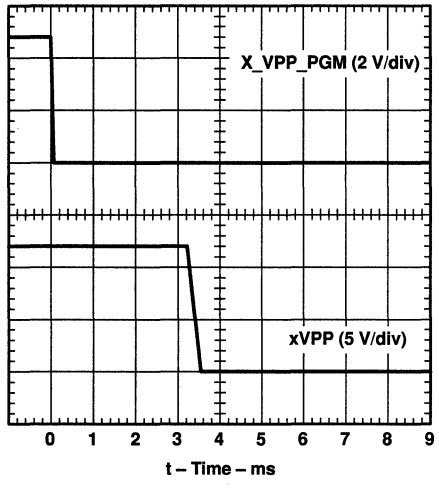


Figure 15. xVPP Propagation Delay and Fall Time With 1-μF Load, 12-V Switch

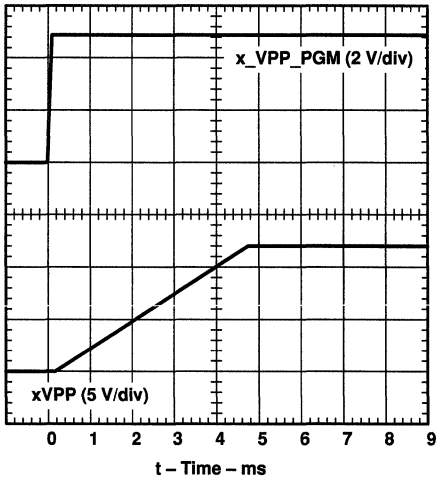
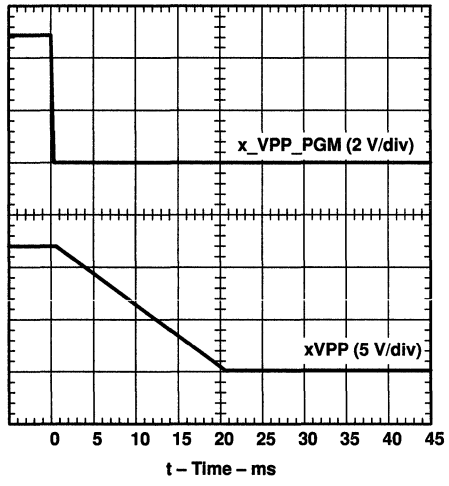


Figure 16. xVPP Propagation Delay and Rise Time With 150-μF Load, 12-V Switch



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TYPICAL CHARACTERISTICS

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$I_{OS(xVCC)}$	Short-circuit current, 3.3-V switch	vs Junction temperature	29
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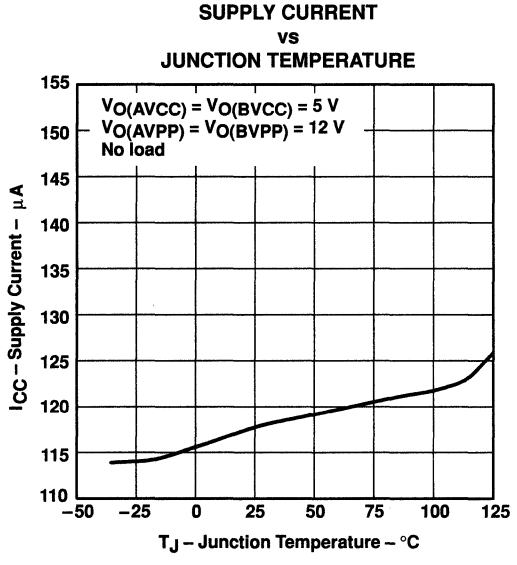


Figure 18

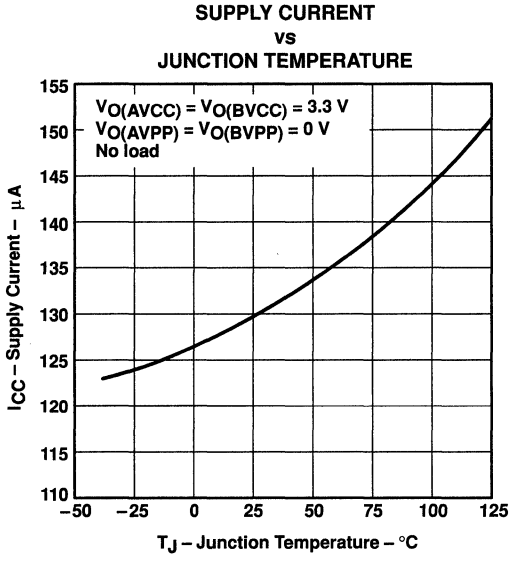


Figure 19

TYPICAL CHARACTERISTICS

3.3-V SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

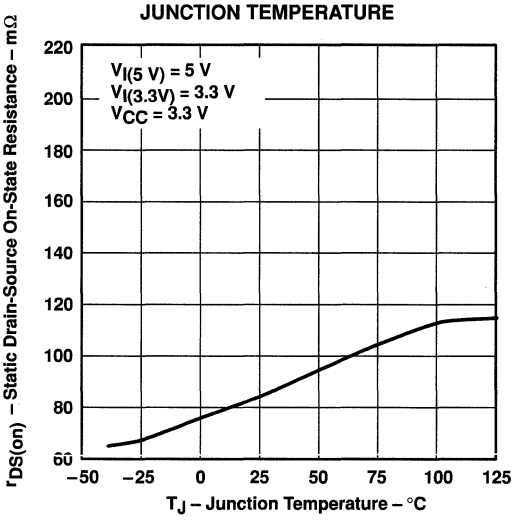


Figure 20

3.3-V SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

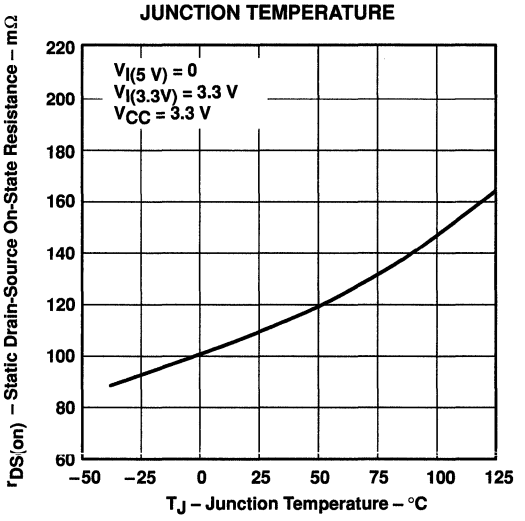


Figure 21

5-V SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

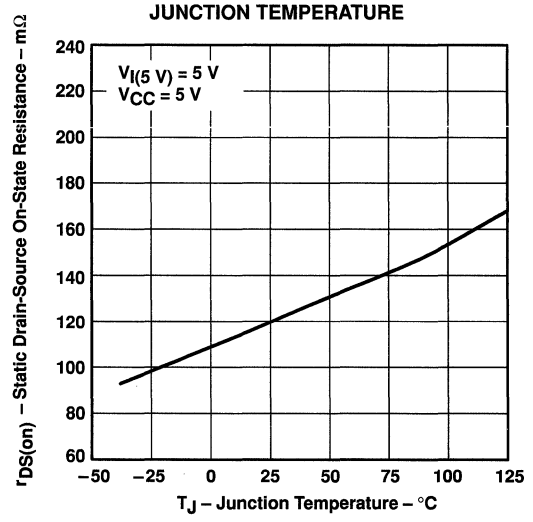


Figure 22

12-V SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

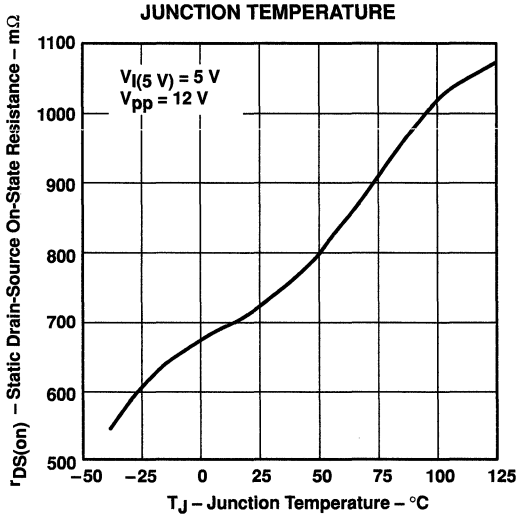


Figure 23

TYPICAL CHARACTERISTICS

5-V SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

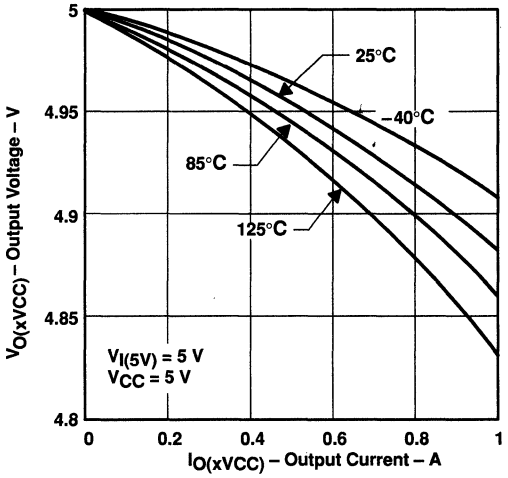


Figure 24

3.3-V SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

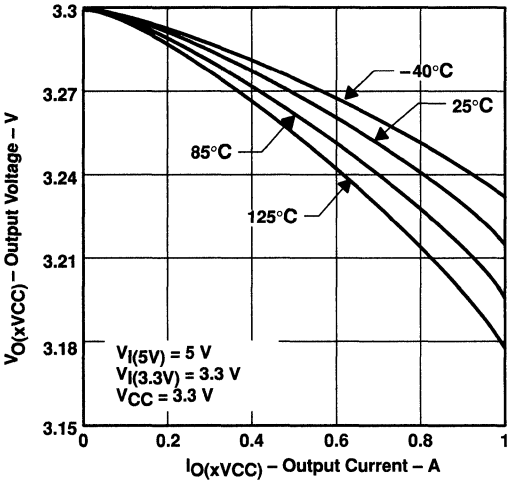


Figure 25

3.3-V SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

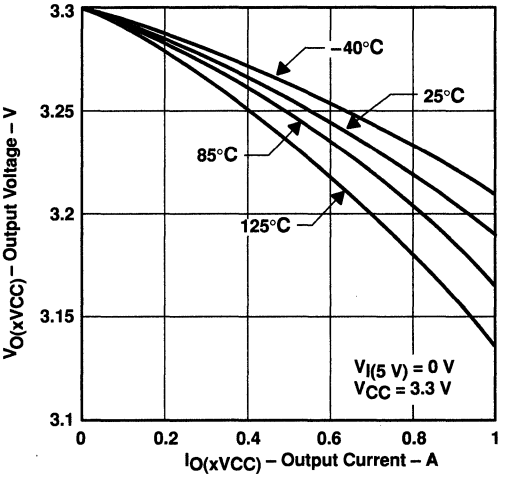


Figure 26

12-V SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

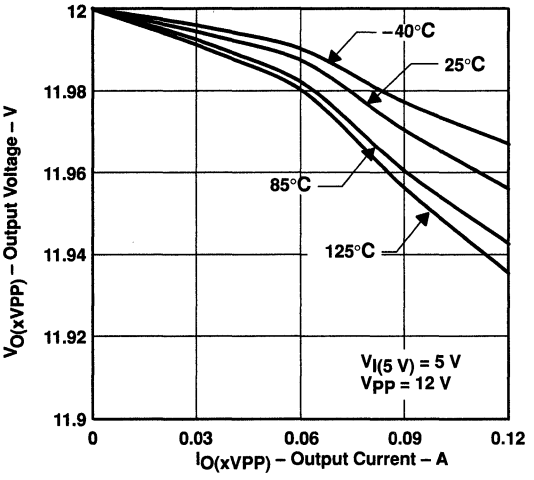


Figure 27

TYPICAL CHARACTERISTICS

5-V SWITCH
SHORT-CIRCUIT CURRENT
vs
JUNCTION TEMPERATURE

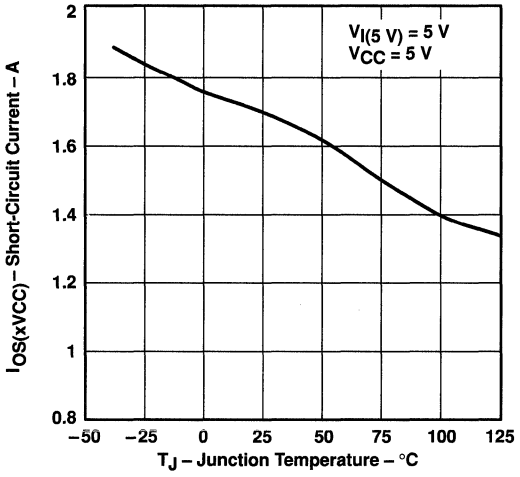


Figure 28

3.3-V SWITCH
SHORT-CIRCUIT CURRENT
vs
JUNCTION TEMPERATURE

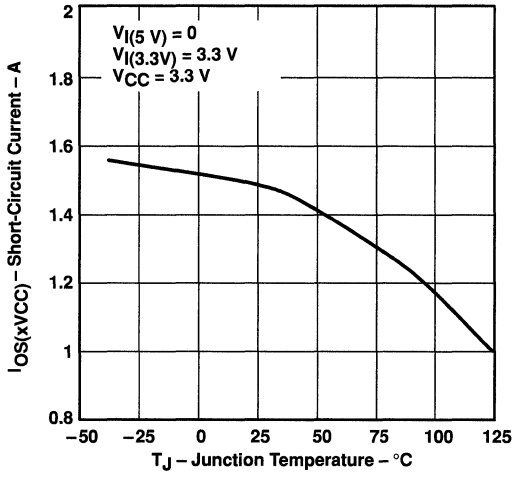


Figure 29

12-V SWITCH
SHORT-CIRCUIT CURRENT
vs
JUNCTION TEMPERATURE

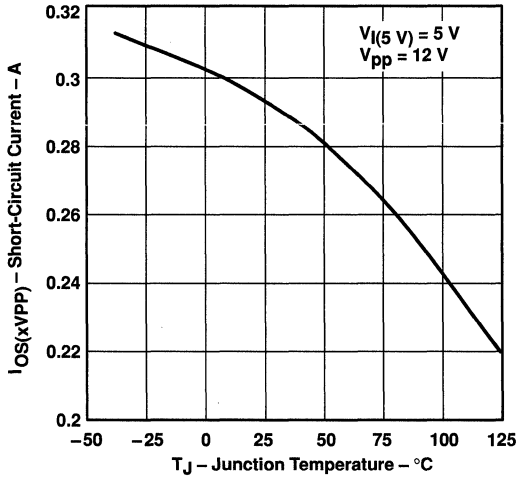


Figure 30

APPLICATION INFORMATION

overview

PC Cards were initially introduced as a means to add EEPROM (flash memory) to portable computers with limited on-board memory. The idea of add-in cards quickly took hold; modems, wireless LANs, global positioning satellite system (GPS), multimedia, and hard-disk versions were soon available. As the number of PC Card applications grew, the engineering community quickly recognized the need for a standard to ensure compatibility across platforms. To this end, the PCMCIA was established, comprised of members from leading computer, software, PC Card, and semiconductor manufacturers. One key goal was to realize the "plug-and-play" concept. Cards and hosts from different vendors should be compatible — able to communicate with one another transparently.

PC Card power specification

System compatibility also means power compatibility. The most current set of specifications (PC Card Standard) set forth by the PCMCIA committee states that power is to be transferred between the host and the card through eight of 68 terminals of the PC Card connector. This power interface consists of two V_{CC}, two V_{pp}, and four ground terminals. Multiple V_{CC} and ground terminals minimize connector-terminal and line resistance. The two V_{pp} terminals were originally specified as separate signals, but are commonly tied together in the host to form a single node to minimize voltage losses. Card primary power is supplied through the V_{CC} terminals; flash-memory programming and erase voltage is supplied through the V_{pp} terminals.

designing for voltage regulation

The current PCMCIA specification for output-voltage regulation ($V_{O(reg)}$) of the 5-V output is 5% (250 mV). In a typical PC power-system design, the power supply has an output-voltage regulation ($V_{PS(reg)}$) of 2% (100 mV). Also, a voltage drop from the power supply to the PC Card will result from resistive losses (V_{PCB}) in the PCB traces and the PCMCIA connector. A typical design would limit the total of these resistive losses to less than 1% (50 mV) of the output voltage. Therefore, the allowable voltage drop (V_{DS}) for the TPS2205 would be the PCMCIA voltage regulation less the power supply regulation and less the PCB and connector resistive drops:

$$V_{DS} = V_{O(reg)} - V_{PS(reg)} - V_{PCB}$$

Typically, this would leave 100 mV for the allowable voltage drop across the TPS2205. The voltage drop is the output current multiplied by the switch resistance of the TPS2205. Therefore, the maximum output current that can be delivered to the PC Card in regulation is the allowable voltage drop across the TPS2205 divided by the output switch resistance.

$$I_O max = \frac{V_{DS}}{r_{DS(on)}}$$

The xVCC outputs have been designed to deliver 700 mA at 5 V within regulation over the operating temperature range. Current proposals for the PCMCIA specifications are to limit the power dissipated in the PCMCIA slot to 3 W. With an input voltage of 5 V, 700 mA continous is the maximum current that can be delivered to the PC Card. The TPS2205 is capable of delivering up to 1 A continuously, but during worst-case conditions the output may not be within regulation. This is generally acceptable because the majority of PC Cards require less than 700 mA continuous. Some cards require higher peak currents (disk drives during initial platter spin-up), but it is generally acceptable for small voltage sags to occur during these peak currents.

The xVCC outputs have been designed to deliver 1 A continuously at 3.3 V within regulation over the operating temperature range. The PCMCIA specification for output voltage regulation of the 3.3-V output is 300 mV. Using the voltage drop percentages (2%) for power supply regulation and PCB resistive loss (1%), the allowable voltage drop for the 3.3 V switch is 200 mV.

The xVPP outputs have been designed to deliver 150 mA continuously at 12 V.

APPLICATION INFORMATION

overcurrent and over-temperature protection

PC Cards are inherently subject to damage that can result from mishandling. Host systems require protection against short-circuited cards that could lead to power supply or PCB-trace damage. Even systems sufficiently robust to withstand a short circuit would still undergo rapid battery discharge into the damaged PC Card, resulting in the rather sudden and unacceptable loss of system power. Most hosts include fuses for protection. The reliability of fused systems is poor, as blown fuses require troubleshooting and repair, usually by the manufacturer.

The TPS2205 takes a two-pronged approach to overcurrent protection. First, instead of fuses, sense FETs monitor each of the power outputs. Excessive current generates an error signal that linearly limits the output current, preventing host damage or failure. Sense FETs, unlike sense resistors or polyfuses, have an advantage in that they do not add to the series resistance of the switch and thus produce no additional voltage losses. Second, when an overcurrent condition is detected, the TPS2205 asserts a signal at $\overline{OC}$ that can be monitored by the microprocessor to initiate diagnostics and/or send the user a warning message. In the event that an overcurrent condition persists, causing the IC to exceed its maximum junction temperature, thermal-protection circuitry activates, shutting down all power outputs until the device cools to within a safe operating region.

12-V supply not required

Most PC Card switches use the externally supplied 12-V V_{pp} power for switch-gate drive and other chip functions, which requires that power be present at all times. The TPS2205 offers considerable power savings by using an internal charge pump to generate the required higher voltages from the 5-V or 3.3-V input; therefore, the external 12-V supply can be disabled except when needed for flash-memory functions, thereby extending battery lifetime. Do not ground the 12-V inputs when the 12-V input is not used. Additional power savings are realized by the TPS2205 during a software shutdown in which quiescent current drops to a maximum of 1 µA.

backward compatibility and 3.3-V low-voltage mode

The TPS2205 is backward compatible with the TPS2201, with the following considerations. Pin 25 (V_{DD} on TPS2201) is a no connect because bias current is derived from either the 3.3-V input pin or the 5-V input pin. Also, the TPS2205 does not have the APWR_GOOD or BPWR_GOOD VPP reporting outputs. These are left as no connects.

The TPS2205 operates in 3.3-V low-voltage mode when 3.3 V is the only available input voltage ($V_{I(5V)}$=0). This allows host and PC Cards to be operated in low-power 3.3-V-only modes such as sleep modes or pager modes. Note that in this operation mode, the TPS2205 derives its bias current from the 3.3-V input pin and only 3.3 V can be delivered to the PC Card. The 3.3-V switch resistance will be increased, but the added switch resistance should not be critical, because only a small amount of current is delivered in this mode. If 6% (198 mV) is allowed for the 3.3-V switch voltage drop, a 500 mΩ switch could deliver over 350 mA to the PC Card.

voltage transitioning requirement

PC Cards, like portables, are migrating from 5 V to 3.3 V to minimize power consumption, optimize board space, and increase logic speeds. The TPS2205 is designed to meet all combinations of power delivery as currently defined in the PCMCIA standard. The latest protocol accommodates mixed 3.3-V/5-V systems by first powering the card with 5 V, then polling it to determine its 3.3-V compatibility. The PCMCIA specification requires that the capacitors on 3.3-V-compatible cards be discharged to below 0.8 V before applying 3.3-V power. This ensures that sensitive 3.3-V circuitry is not subjected to any residual 5-V charge and functions as a power reset. The TPS2205 offers a selectable V_{CC} and V_{pp} ground state, in accordance with PCMCIA 3.3-V/5-V switching specifications, to fully discharge the card capacitors while switching between V_{CC} voltages.

APPLICATION INFORMATION

output ground switches

Several PCMCIA power-distribution switches on the market do not have an active-grounding FET switch. These devices do not meet the PC Card specification requiring a discharge of V_{CC} within 100 ms. PC Card resistance can not be relied on to provide a discharge path for voltages stored on PC Card capacitance because of possible high-impedance isolation by power-management schemes. A method commonly shown to alleviate this problem is to add to the switch output an external 100-kΩ resistor in parallel with the PC Card. Considering that this is the only discharge path to ground, a timing analysis shows that the RC time constant delays the required discharge time to more than 2 seconds. The only way to ensure timing compatibility with PC Card standards is to use a power-distribution switch that has an internal ground switch, like that of the TPS22xx family, or add an external ground FET to each of the output lines with the control logic necessary to select it.

In summary, the TPS2205 is a complete single-chip dual-slot PC Card power interface. It meets all currently defined PCMCIA specifications for power delivery in 5-V, 3.3-V, and mixed systems, and offers a serial control interface. The TPS2205 offers functionality, power savings, overcurrent and thermal protection, and fault reporting in one 30-pin SSOP surface-mount package, for maximum value added to new portable designs.

power supply considerations

The TPS2205 has multiple pins for each of its 3.3-V, 5-V, and 12-V power inputs and for the switched V_{CC} outputs. Any individual pin can conduct the rated input or output current. Unless all pins are connected in parallel, the series resistance is significantly higher than that specified, resulting in increased voltage drops and lost power. Both 12-V inputs must be connected for proper V_{pp} switching; it is recommended that all input and output power pins be paralleled for optimum operation.

Although the TPS2205 is fairly immune to power input fluctuations and noise, it is generally considered good design practice to bypass power supplies, typically with a 1-μF electrolytic or tantalum capacitor paralleled by a 0.047-μF to 0.1-μF ceramic capacitor. It is strongly recommended that the switched V_{CC} and V_{pp} outputs be bypassed with a 0.1-μF or larger capacitor; doing so improves the immunity of the TPS2205 to electrostatic discharge (ESD). Care should be taken to minimize the inductance of PCB traces between the TPS2205 and the load. High switching currents can produce large negative-voltage transients, which forward biases substrate diodes, resulting in unpredictable performance. Similary, no pin should be taken below −0.3 V.

overcurrent and thermal protection

The TPS2205 uses sense FETs to check for overcurrent conditions in each of the V_{CC} and V_{pp} outputs. Unlike sense resistors or polyfuses, these FETs do not add to the series resistance of the switch; therefore, voltage and power losses are reduced. Overcurrent sensing is applied to each output separately. When an overcurrent condition is detected, only the power output affected is limited; all other power outputs continue to function normally. The $\overline{OC}$ indicator, normally a logic high, is a logic low when any overcurrent condition is detected, providing for initiation of system diagnostics and/or sending a warning message to the user.

During power up, the TPS2205 controls the rise time of the V_{CC} and V_{pp} outputs and limits the current into a faulty card or connector. If a short circuit is applied after power is established (e.g., hot insertion of a bad card), current is initially limited only by the impedance between the short and the power supply. In extreme cases, as much as 10 A to 15 A may flow into the short before the current limiting of the TPS2205 engages. If the V_{CC} or V_{pp} outputs are driven below ground, the TPS2205 may latch nondestructively in an off state. Cycling power will reestablish normal operation.

Overcurrent limiting for the V_{CC} outputs is designed to activate if powered up into a short in the range of 1 A to 2.2 A, typically at about 1.6 A. The V_{pp} outputs limit from 120 mA to 400 mA, typically around 280 mA. The protection circuitry acts by linearly limiting the current passing through the switch rather than initiating a full shutdown of the supply. Shutdown occurs only during thermal limiting.

APPLICATION INFORMATION

overcurrent and thermal protection (continued)

Thermal limiting prevents destruction of the IC from overheating if the package power-dissipation ratings are exceeded. Thermal limiting disables all power outputs (both A and B slots) until the device has cooled.

calculating junction temperature

The switch resistance, $r_{DS(on)}$, is dependent on the junction temperature, T_J, of the die. The junction temperature is dependent on both $r_{DS(on)}$ and the current through the switch. To calculate T_J, first find $r_{DS(on)}$ from Figures 20, 21, 22, and 23 using an initial temperature estimate about 50°C above ambient. Then calculate the power dissipation for each switch, using the formula:

$$P_D = r_{DS(on)} \times I^2$$

Next, sum the power dissipation and calculate the junction temperature:

$$T_J = \left(\Sigma\, P_D \times R_{\theta JA}\right) + T_A,\ R_{\theta JA} = 108°C/W$$

Compare the calculated junction temperature with the initial temperature estimate. If the temperatures are not within a few degrees of each other, recalculate using the calculated temperature as the initial estimate.

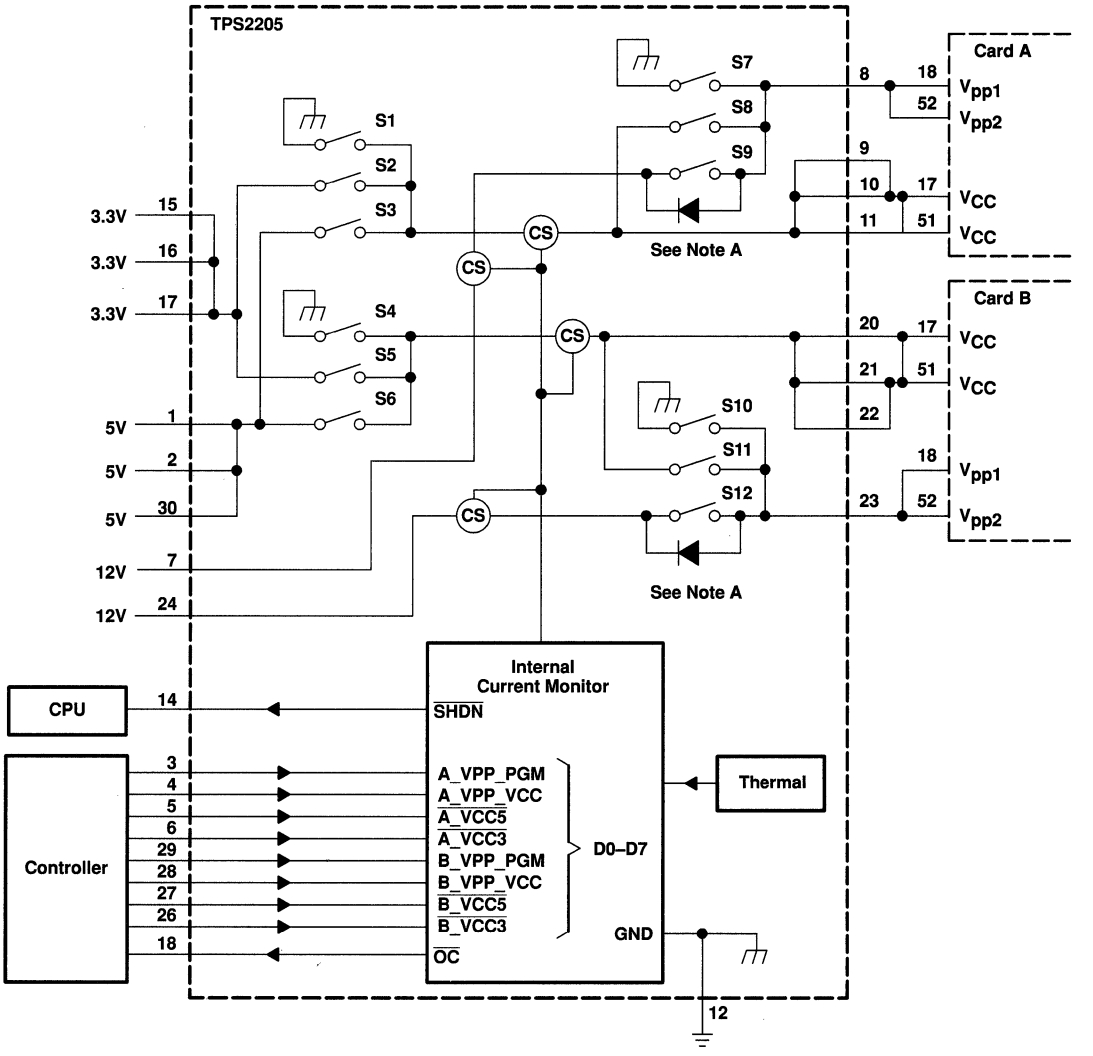
logic input and outputs

The TPS2205 was designed to be compatible with most popular PCMCIA controllers and current PCMCIA and JEIDA standards. However, some controllers require slightly counterintuitive connections to achieve desired output states. The TPS2205 control logic inputs $\overline{\text{A\_VCC3}}$, $\overline{\text{A\_VCC5}}$, $\overline{\text{B\_VCC3}}$ and $\overline{\text{B\_VCC5}}$ are defined active low (see Figure 31 and control-logic table). As such, they are directly compatible with the logic outputs of the Cirrus Logic CL-PD6720 controller.

The shutdown input ($\overline{\text{SHDN}}$) of the TPS2205, when held at a logic low, places all V_{CC} and V_{pp} outputs in a high-impedance state and reduces chip quiescent current to 1 μA to conserve battery power.

An overcurrent output ($\overline{\text{OC}}$) is provided to indicate an overcurrent condition in any of the V_{CC} or V_{pp} supplies (see discussion above).

APPLICATION INFORMATION



NOTE A. MOSFET switches S9 and S12 have a back-gate diode from the source to the drain. Unused switch inputs ;should never be grounded.

Figure 31. Internal Switching Matrix

APPLICATION INFORMATION

TPS2205 control logic

AVPP

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
D8 $\overline{SHDN}$	D0 A_VPP_PGM	D1 A_VPP_VCC	S7	S8	S9	VAVPP
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	VCC†
1	1	0	OPEN	OPEN	CLOSED	VPP(12 V)
1	1	1	OPEN	OPEN	OPEN	Hi-Z
0	X	X	OPEN	OPEN	OPEN	Hi-Z

BVPP

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
D8 $\overline{SHDN}$	D4 B_VPP_PGM	D5 B_VPP_VCC	S10	S11	S12	VBVPP
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	VCC‡
1	1	0	OPEN	OPEN	CLOSED	VPP(12 V)
1	1	1	OPEN	OPEN	OPEN	Hi-Z
0	X	X	OPEN	OPEN	OPEN	Hi-Z

AVCC

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
D8 $\overline{SHDN}$	D3 $\overline{A\_VCC3}$	D2 $\overline{A\_VCC5}$	S1	S2	S3	VAVCC
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	3.3 V
1	1	0	OPEN	OPEN	CLOSED	5 V
1	1	1	CLOSED	OPEN	OPEN	0 V
0	X	X	OPEN	OPEN	OPEN	Hi-Z

BVCC

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
D8 $\overline{SHDN}$	D6 $\overline{B\_VCC3}$	D7 $\overline{B\_VCC5}$	S4	S5	S6	VBVCC
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	3.3 V
1	1	0	OPEN	OPEN	CLOSED	5 V
1	1	1	CLOSED	OPEN	OPEN	0 V
0	X	X	OPEN	OPEN	OPEN	Hi-Z

† Output depends on AVCC
‡ Output depends on BVCC

ESD protection

All TPS2205 inputs and outputs incorporate ESD-protection circuitry designed to withstand a 2-kV human-body-model discharge as defined in MIL-STD-883C, Method 3015. The V_{CC} and V_{pp} outputs can be exposed to potentially higher discharges from the external environment through the PC Card connector. Bypassing the outputs with 0.1-µF capacitors protects the devices from discharges up to 10 kV.

APPLICATION INFORMATION

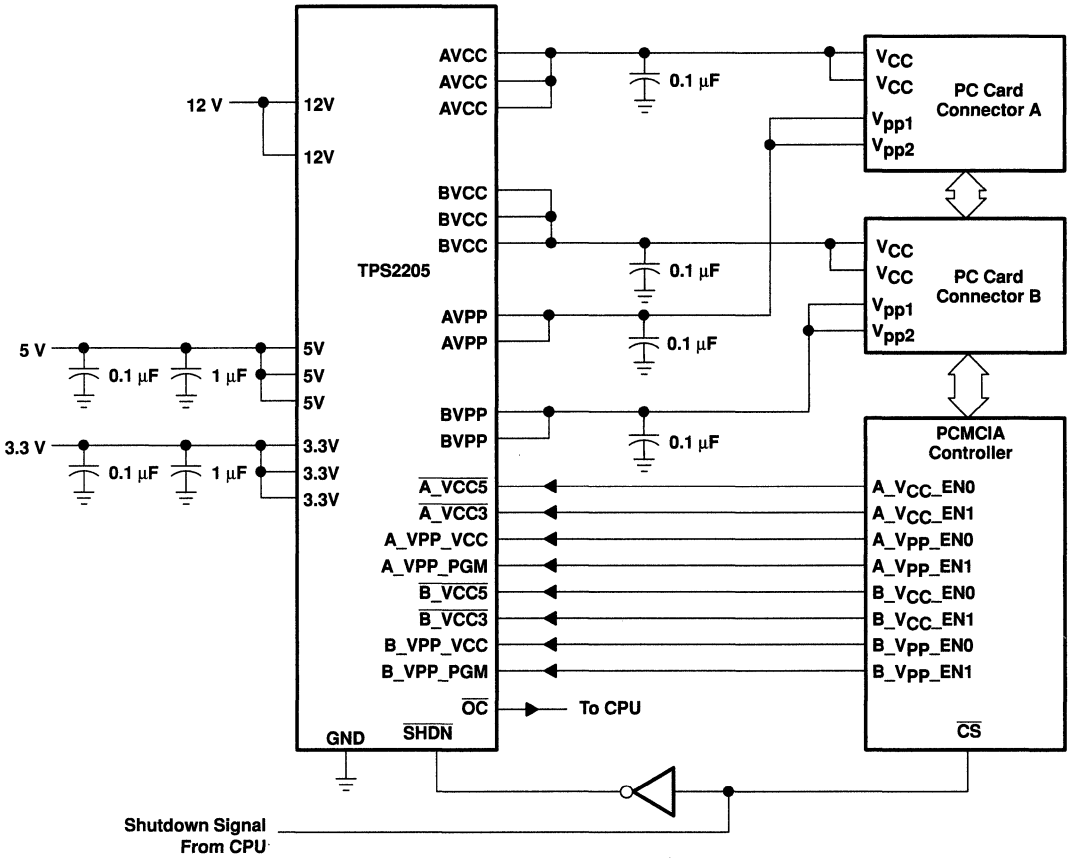


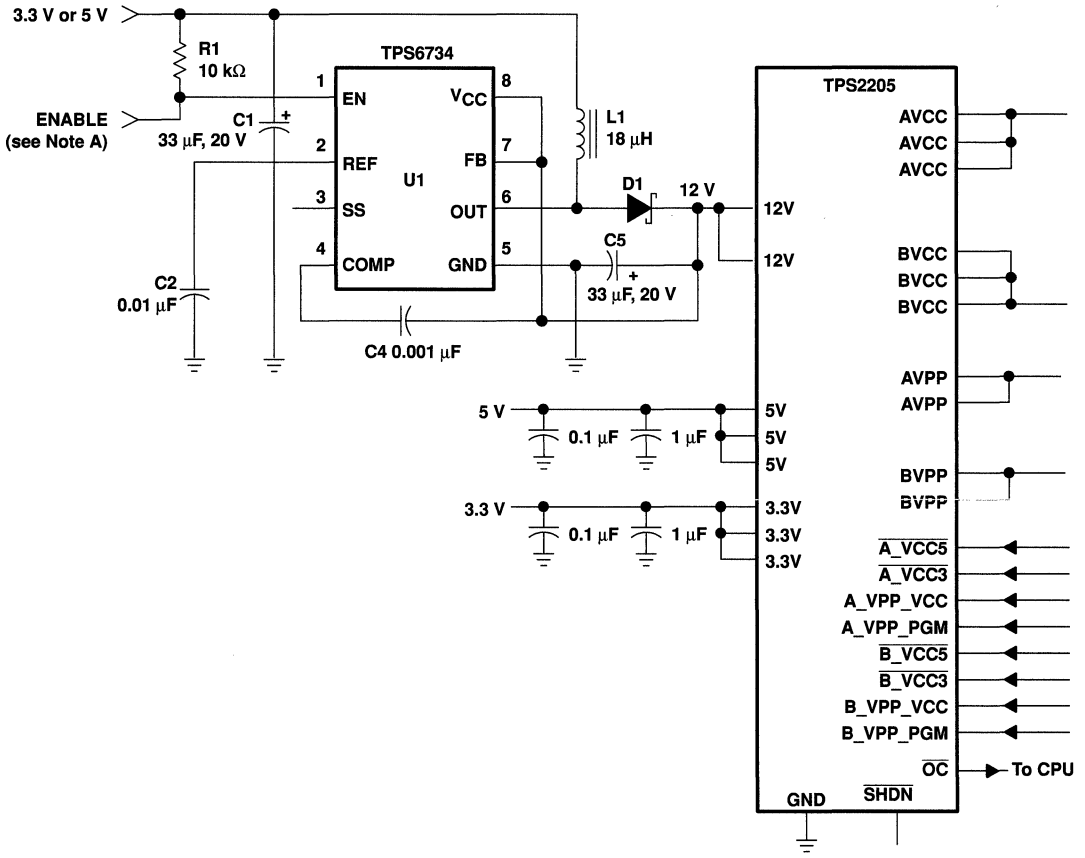
Figure 32. Detailed Interconnections and Capacitor Recommendations

APPLICATION INFORMATION

12-V flash memory supply

The TPS6734 is a fixed 12-V output boost converter capable of delivering 120 mA from inputs as low as 2.7 V. The device is pin-for-pin compatible with the MAX734 regulator and offers the following advantages: lower supply current, wider operating input-voltage range, and higher output currents. As shown in Figure 1, the only external components required are: an inductor, a Schottky rectifier, an output filter capacitor, an input filter capacitor, and a small capacitor for loop compensation. The entire converter occupies less than 0.7 in^2 of PCB space when implemented with surface-mount components. An enable input is provided to shut the converter down and reduce the supply current to 3 μA when 12 V is not needed.

The TPS6734 is a 170-kHz current-mode PWM (pulse-width modulation) controller with an n-channel MOSFET power switch. Gate drive for the switch is derived from the 12-V output after start-up to minimize the die area needed to realize the 0.7-Ω MOSFET and improve efficiency at input voltages below 5 V. Soft start is accomplished with the addition of one small capacitor. A 1.22-V reference (pin 2) is brought out for external use. For additional information, see the TPS6734 data sheet (SLVS127).

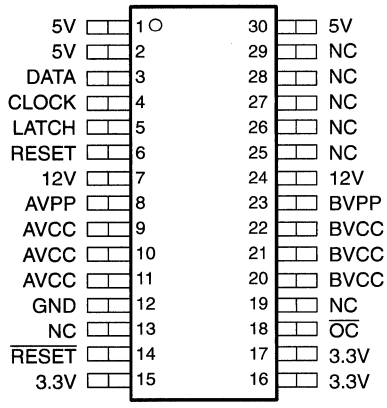


NOTE A. The enable terminal can be tied to a generall purpose I/O terminal on the PCMCIA controller or tied high.

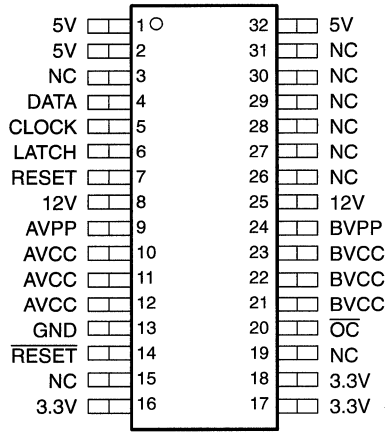
Figure 33. TPS2205 with TPS6734 12-V, 120-mA Supply

- **Fully Integrated V_{CC} and V_{pp} Switching for Dual-Slot PC Card™ Interface**
- **P²C™ 3-Lead Serial Interface Compatible With CardBus™ Controllers**
- **3.3 V Low-Voltage Mode**
- **Meets PC Card Standards**
- **RESET for System Initialization of PC Cards**
- **12-V Supply Can Be Disabled Except During 12-V Flash Programming**
- **Short Circuit and Thermal Protection**
- **30-Pin SSOP (DB) and 32-Pin TSSOP (DAP)**
- **Compatible With 3.3-V, 5-V and 12-V PC Cards**
- **Low $r_{DS(on)}$ (140-mΩ 5-V V_{CC} Switch; 110-mΩ 3.3-V V_{CC} Switch)**
- **Break-Before-Make Switching**

DB OR DF PACKAGE
(TOP VIEW)



DAP PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TPS2206 PC Card power-interface switch provides an integrated power-management solution for two PC Cards. All of the discrete power MOSFETs, a logic section, current limiting, and thermal protection for PC Card control are combined on a single integrated circuit (IC), using the Texas Instruments LinBiCMOS™ process. The circuit allows the distribution of 3.3-V, 5-V, and/or 12-V card power by means of the P²C (PCMCIA Peripheral-Control) Texas Instruments nonproprietary serial interface. The current-limiting feature eliminates the need for fuses, which reduces component count and improves reliability.

The TPS2206 is backward compatible with the TPS2202 and TPS2202A, except that there is no V_{DD} connection. Bias current is derived from either the 3.3-V input pin or the 5-V input pin. The TPS2206 also eliminates the APWR_GOOD and BPWR_GOOD pins of the TPS2202 and TPS2202A.

The TPS2206 features a 3.3-V low-voltage mode that allows for 3.3-V switching without the need for 5 V. This facilitates low-power system designs such as sleep mode and pager mode where only 3.3 V is available.

LinBiCMOS and P²C are trademarks of Texas Instruments Incorporated.
PC Card and CardBus are trademarks of PCMCIA (Personal Computer Memory Card International Association).

description (continued)

The TPS2206 incorporates a reset function, selectable by one of two inputs, to help alleviate system errors. The reset function enables PC Card initialization concurrent with host platform initialization, allowing a system reset. Reset is accomplished by grounding the V_{CC} and V_{pp} (flash-memory programming voltage) outputs, which discharges residual card voltage.

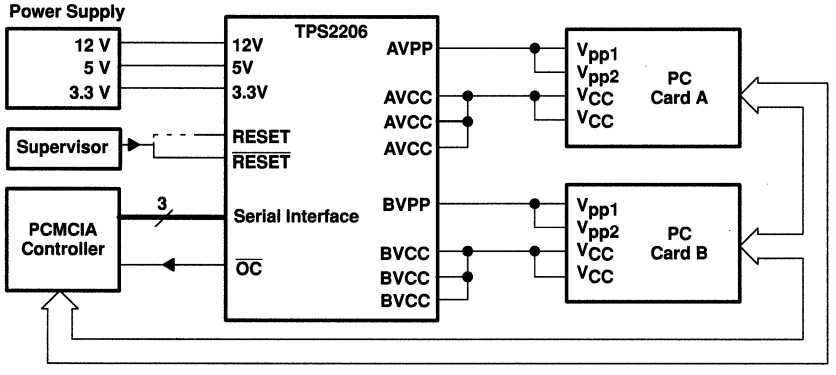
End equipment for the TPS2206 includes notebook computers, desktop computers, personal digital assistants (PDAs), digital cameras and bar-code scanners.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES			CHIP FORM (Y)
	PLASTIC SMALL OUTLINE (DB)	PLASTIC SMALL OUTLINE (DF)	TSSOP (DAP)	
–40°C to 85°C	TPS2206IDBLE	TPS2206IDFLE	TPS2206IDAPR	TPS2206Y

The DB package and the DF package are only available left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TPS2206IDBLE). The DAP package is only available taped and reeled (indicated by the R suffix on the device type; e.g., TPS2206IDAPR).

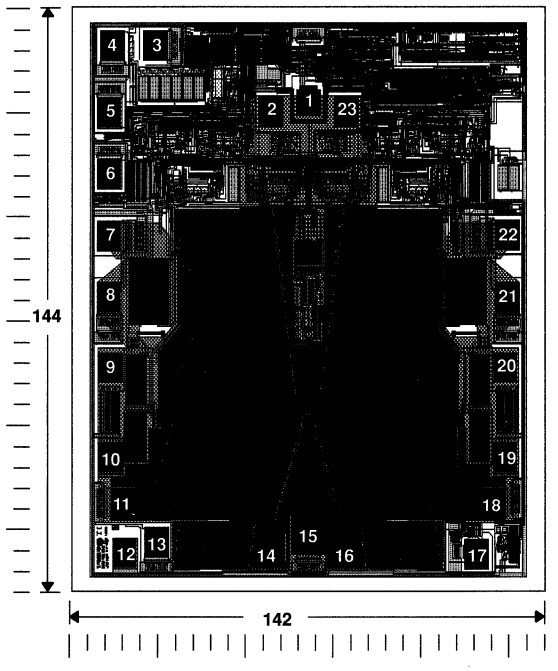
typical PC card power-distribution application

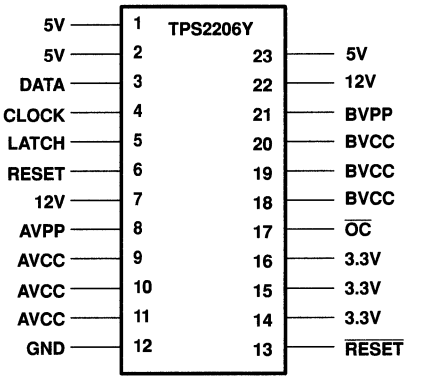


TPS2206Y chip information

This chip, when properly assembled, displays characteristics similar to those of the TPS2206. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

Terminal Functions

TERMINAL NAME	TERMINAL NO. DB, DF	TERMINAL NO. DAP	I/O	DESCRIPTION
3.3V	15, 16, 17	16, 17, 18	I	3.3-V V_{CC} input for card power
5V	1, 2, 30	1, 2, 32	I	5-V V_{CC} input for card power and/or chip power
12V	7, 24	8, 25	I	12-V V_{pp} input for card power
AVCC	9, 10, 11	10, 11, 12	O	Switched output that delivers 0 V, 3.3 V, 5 V, or high impedance to card
AVPP	8	9	O	Switched output that delivers 0 V, 3.3 V, 5 V, 12 V, or high impedance to card
BVCC	20, 21, 22	21, 22, 23	O	Switched output that delivers 0 V, 3.3 V, 5 V, or high impedance
BVPP	23	24	O	Switched output that delivers 0 V, 3.3 V, 5 V, 12 V, or high impedance
CLOCK	4	5	I	Logic-level clock for serial data word
DATA	3	4	I	Logic-level serial data word
GND	12	13		Ground
LATCH	5	6	I	Logic-level latch for serial data word
NC	13, 19, 25, 26, 27, 28, 29	3, 19, 26, 27, 28, 29, 30, 31		No internal connection
$\overline{OC}$	18	20	O	Logic-level overcurrent. $\overline{OC}$ reports output that goes low when an overcurrent condition exists
RESET	6	7	I	Logic-level RESET input active high. Do not connect if terminal 14 is used.
$\overline{RESET}$	14	14	I	Logic-level $\overline{RESET}$ input active low. Do not connect if terminal 6 is used.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Input voltage range for card power: $V_{I(5V)}$ ..... −0.3 V to 7 V
$V_{I(3.3V)}$ ..... −0.3 V to 7 V
$V_{I(12V)}$ ..... −0.3 V to 14 V
Logic input voltage ..... −0.3 V to 7 V
Continuous total power dissipation ..... See Dissipation Rating Table
Output current (each card): $I_{O(xVCC)}$ ..... internally limited
$I_{O(xVPP)}$ ..... internally limited
Operating virtual junction temperature range, T_J ..... −40°C to 150°C
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range, T_{stg} ..... −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE		$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DB		1024 mW	8.2 mW/°C	655 mW	532 mW
DF		1158 mW	9.26 mW/°C	741 mW	602 mW
DAP	No backplane	1625 mW	13 mW/°C	1040 mW	845 mW
	Backplane§	6044 mW	48.36 mW/°C	3869 mW	3143 mW

‡ These devices are mounted on an FR4 board with no special thermal considerations.
§ 2-oz backplane with 2-oz traces; 5.2-mm × 11-mm thermal pad with 6-mil solder; 0.18-mm diameter vias in a 3×6 array.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage range, V_I	$V_{I(5V)}$	0	5.25	V
	$V_{I(3.3V)}$	0	5.25	V
	$V_{I(12V)}$	0	13.5	V
Output current	$I_{O(xVCC)}$ at 25°C		1	A
	$I_{O(xVPP)}$ at 25°C		150	mA
Clock frequency		0	2.5	MHz
Operating virtual junction temperature, T_J		−40	125	°C

electrical characteristics, T_A = 25°C, $V_{I(5V)}$ = 5 V (unless otherwise noted)

dc characteristics

PARAMETER			TEST CONDITIONS	TPS2206 MIN	TPS2206 TYP	TPS2206 MAX	UNIT
	Switch resistances†	5 V to xVCC			103	140	mΩ
		3.3 V to xVCC	$V_{I(5V)}$ = 5 V, $V_{I(3.3\ V)}$ = 3.3 V		69	110	
		3.3 V to xVCC	$V_{I(5V)}$ = 0, $V_{I(3.3V)}$ = 3.3 V		96	180	
		5 V to xVPP				6	Ω
		3.3 V to xVPP				6	
		12 V to xVPP				1	
$V_{O(xVPP)}$	Clamp low voltage		I_{pp} at 10 mA			0.8	V
$V_{O(xVCC)}$	Clamp low voltage		I_{CC} at 10 mA			0.8	V
I_{lkg}	Leakage current	I_{pp} high-impedance state	T_A = 25°C		1	10	µA
			T_A = 85°C			50	
		I_{CC} high-impedance state	T_A = 25°C		1	10	
			T_A = 85°C			50	
I_I	Input current	$V_{I(5V)}$ = 5 V	$V_{O(AVCC)}$ = $V_{O(BVCC)}$ = 5 V, $V_{O(AVPP)}$ = $V_{O(BVPP)}$ = 12 V		117	150	µA
		$V_{I(5V)}$ = 0, $V_{I(3.3V)}$ = 3.3 V	$V_{O(AVCC)}$ = $V_{O(BVCC)}$ = 3.3 V, $V_{O(AVPP)}$ = $V_{O(BVPP)}$ = 0		131	150	
		Shutdown mode	$V_{O(BVCC)}$ = $V_{O(AVCC)}$ = $V_{O(AVPP)}$ = $V_{O(BVPP)}$ = Hi-Z			1	µA
I_{OS}	Short-circuit output-current limit	$I_{O(xVCC)}$	T_J = 85°C, Output powered up into a short to GND	1		2.2	A
		$I_{O(xVPP)}$		120		400	mA

† Pulse-testing techniques are used to maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

logic section

PARAMETER	TEST CONDITIONS	TPS2206 MIN	TPS2206 MAX	UNIT
Logic input current			1	µA
Logic input high level		2		V
Logic input low level			0.8	V
Logic output high level	$V_{I(5V)}$= 5 V, I_O = 1mA	$V_{I(5V)}$–0.4		V
	$V_{I(5V)}$= 0, $V_{I(3.3V)}$ = 3.3 V, I_O = 1mA,	$V_{I(3.3V)}$–0.4		
Logic output low level	I_O = 1mA		0.4	V

switching characteristics†‡

PARAMETER		TEST CONDITIONS		TPS2206 MIN	TPS2206 TYP	TPS2206 MAX	UNIT
t_r	Output rise time	$V_{O(xVCC)}$			1.2		ms
		$V_{O(xVPP)}$			5		
t_f	Output fall time	$V_{O(xVCC)}$			10		
		$V_{O(xVPP)}$			14		
t_{pd}	Propagation delay (see Figure 1)	LATCH↑ to $V_{O(xVPP)}$	t_{on}		4.4		ms
			t_{off}		18		ms
		LATCH↑ to $V_{O(xVCC)}$ (3.3 V), $V_{I(5V)}$ = 5 V	t_{on}		6.5		ms
			t_{off}		20		ms
		LATCH↑ to $V_{O(xVCC)}$ (5 V)	t_{on}		5.7		ms
			t_{off}		25		ms
		LATCH↑ to $V_{O(xVCC)}$ (3.3 V), $V_{I(5V)}$ = 0	t_{on}		6.6		ms
			t_{off}		21		ms

† Refer to Parameter Measurement Information
‡ Switching Characteristics are with C_L = 150 µF.

electrical characteristics, T_A = 25°C, $V_{I(5V)}$ = 5 V (unless otherwise noted)

dc characteristics

PARAMETER			TEST CONDITIONS	TPS2206Y MIN	TPS2206Y TYP	TPS2206Y MAX	UNIT
	Switch resistances§	5 V to xVCC			103		mΩ
		3.3 V to xVCC	$V_{I(5V)}$ = 5 V, $V_{I(3.3\ V)}$ = 3.3 V		69		
		3.3 V to xVCC	$V_{I(5V)}$ = 0, $V_{I(3.3V)}$ = 3.3 V		96		
		5 V to xVPP			4.74		Ω
		3.3 V to xVPP			4.74		
		12 V to xVPP			0.724		
$V_{O(xVPP)}$	Clamp low voltage		I_{pp} at 10 mA		0.275		V
$V_{O(xVCC)}$	Clamp low voltage		I_{CC} at 10 mA		0.275		V
I_{lkg}	Leakage current	I_{pp} High-impedance state	T_A = 25°C		1		µA
		I_{CC} High-impedance state	T_A = 25°C		1		
I_I	Input current	$V_{I(5V)}$ = 5 V	$V_{O(AVCC)}$ = $V_{O(BVCC)}$ = 5 V, $V_{O(AVPP)}$ = $V_{O(BVPP)}$ = 12 V		117		µA
		$V_{I(5V)}$ = 0, $V_{I(3.3V)}$ = 3.3 V	$V_{O(AVCC)}$ = $V_{O(BVCC)}$ = 3.3 V, $V_{O(AVPP)}$ = $V_{O(BVPP)}$ = 0		131		

§ Pulse-testing techniques are used to maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

switching characteristics†‡

PARAMETER		TEST CONDITIONS		TPS2206Y MIN	TPS2206Y TYP	TPS2206Y MAX	UNIT
t_r	Output rise time	$V_{O(xVCC)}$			1.2		ms
		$V_{O(xVPP)}$			5		
t_f	Output fall time	$V_{O(xVCC)}$			10		
		$V_{O(xVPP)}$			14		
t_{pd}	Propagation delay (see Figure 1)	LATCH↑ to $V_{O(xVPP)}$	t_{on}		4.4		ms
			t_{off}		18		ms
		LATCH↑ to $V_{O(xVCC)}$ (3.3 V), $V_{I(5V)}$ = 5 V	t_{on}		6.5		ms
			t_{off}		20		ms
		LATCH↑ to $V_{O(xVCC)}$ (5 V)	t_{on}		5.7		ms
			t_{off}		25		ms
		LATCH↑ to $V_{O(xVCC)}$ (3.3 V), $V_{I(5V)}$ = 0	t_{on}		6.6		ms
			t_{off}		21		ms

† Refer to Parameter Measurement Information
‡ Switching Characteristics are with C_L = 150 µF.

PARAMETER MEASUREMENT INFORMATION

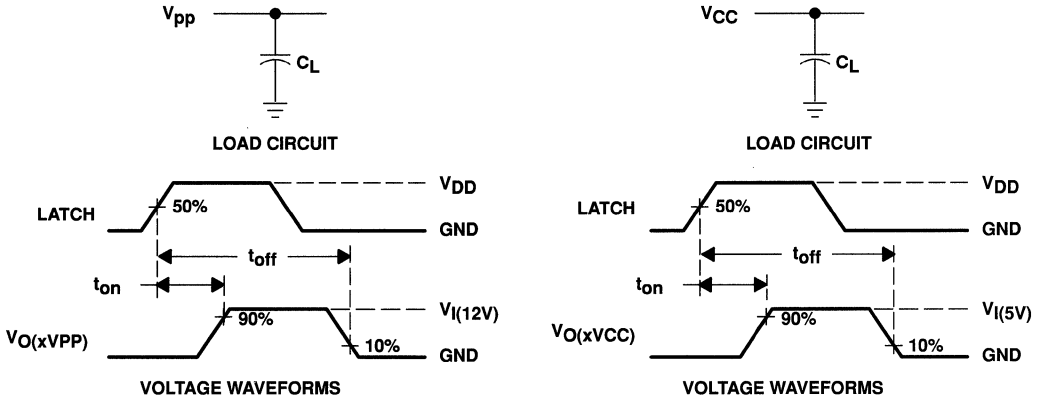
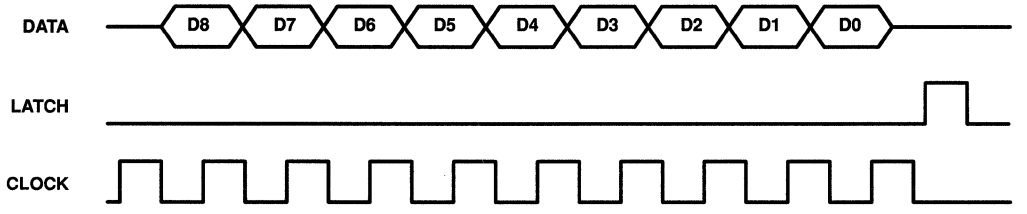


Figure 1. Test Circuits and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

Table of Timing Diagrams

	FIGURE
Serial-Interface Timing	2
xVCC Propagation Delay and Rise Time With 1-µF Load, 3.3-V Switch, $V_{I(5V)}$ = 5 V	3
xVCC Propagation Delay and Fall Time With 1-µF Load, 3.3-V Switch, $V_{I(5V)}$ = 5 V	4
xVCC Propagation Delay and Rise Time With 150-µF Load, 3.3-V Switch, $V_{I(5V)}$ = 5 V	5
xVCC Propagation Delay and Fall Time With 150-µF Load, 3.3-V Switch, $V_{I(5V)}$ = 5 V	6
xVCC Propagation Delay and Rise Time With 1-µF Load, 3.3-V Switch, $V_{I(5V)}$ = 0	7
xVCC Propagation Delay and Fall Time With 1-µF Load, 3.3-V Switch, $V_{I(5V)}$ = 0	8
xVCC Propagation Delay and Rise Time With 150-µF Load, 3.3-V Switch, $V_{I(5V)}$ = 0	9
xVCC Propagation Delay and Fall Time With 150-µF Load, 3.3-V Switch, $V_{I(5V)}$ = 0	10
xVCC Propagation Delay and Rise Time With 1-µF Load, 5-V Switch	11
xVCC Propagation Delay and Fall Time With 1-µF Load, 5-V Switch	12
xVCC Propagation Delay and Rise Time With 150-µF Load, 5-V Switch	13
xVCC Propagation Delay and Fall Time With 150-µF Load, 5-V Switch	14
xVPP Propagation Delay and Rise Time With 1-µF Load, 12-V Switch	15
xVPP Propagation Delay and Fall Time With 1-µF Load, 12-V Switch	16
xVPP Propagation Delay and Rise Time With 150-µF Load, 12-V Switch	17
xVPP Propagation Delay and Fall Time With 150-µF Load, 12-V Switch	18



NOTE A. Data is clocked in on the positive leading edge of the clock. The latch should occur before the next positive leading edge of the clock. For definition of D0 to D8, see the control logic table.

Figure 2. Serial-Interface Timing

PARAMETER MEASUREMENT INFORMATION

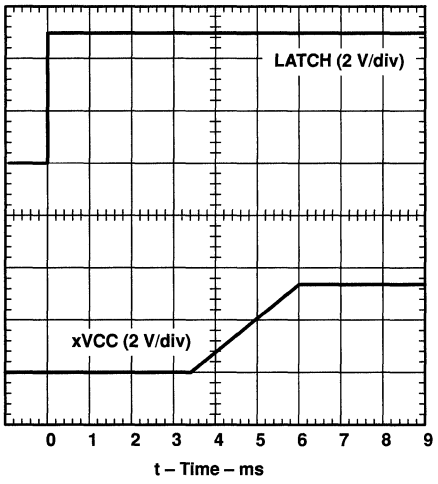


Figure 3. xVCC Propagation Delay and Rise Time With 1-μF Load, 3.3-V Switch, ($V_{I(5\ V)}$ = 5 V)

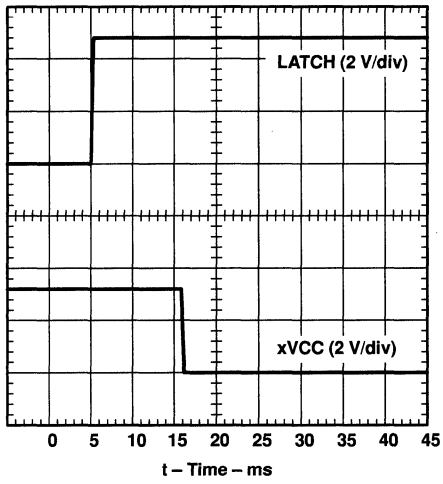


Figure 4. xVCC Propagation Delay and Fall Time With 1-μF Load, 3.3-V Switch, ($V_{I(5\ V)}$ = 5 V)

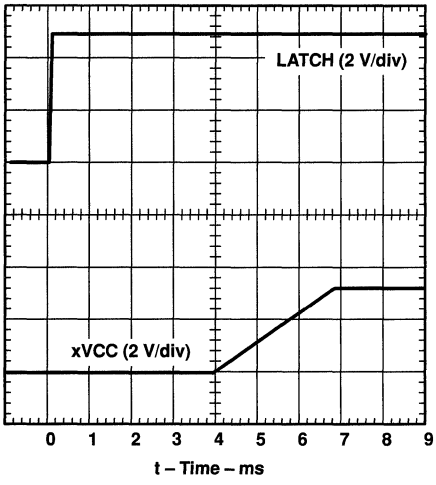


Figure 5. xVCC Propagation Delay and Rise Time With 150-μF Load, 3.3-V Switch, $V_{I(5\ V)}$ = 5 V

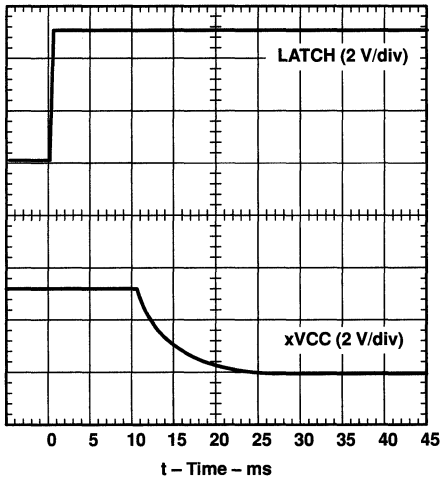


Figure 6. xVCC Propagation Delay and Fall Time With 150-μF Load, 3.3-V Switch, $V_{I(5\ V)}$ = 5 V

PARAMETER MEASUREMENT INFORMATION

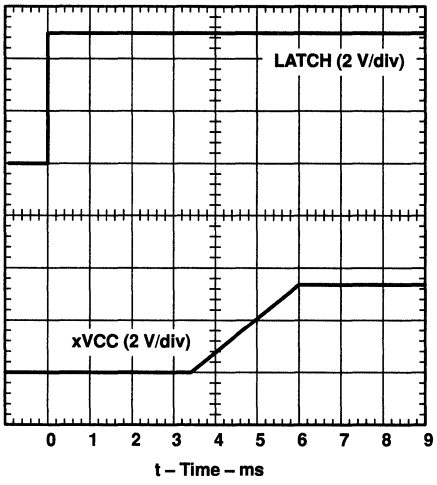


Figure 7. xVCC Propagation Delay and Rise Time With 1-μF Load, 3.3-V Switch, $V_{I(5\ V)} = 0$

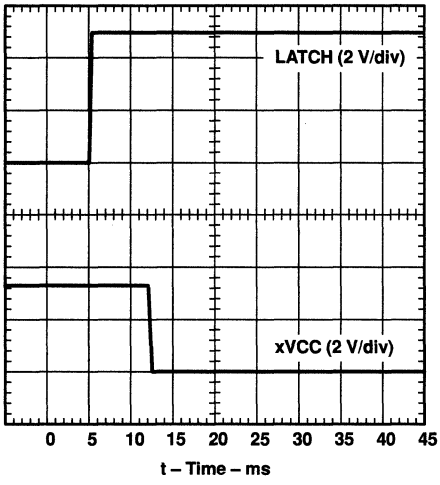


Figure 8. xVCC Propagation Delay and Fall Time With 1-μF Load, 3.3-V Switch, $V_{I(5\ V)} = 0$

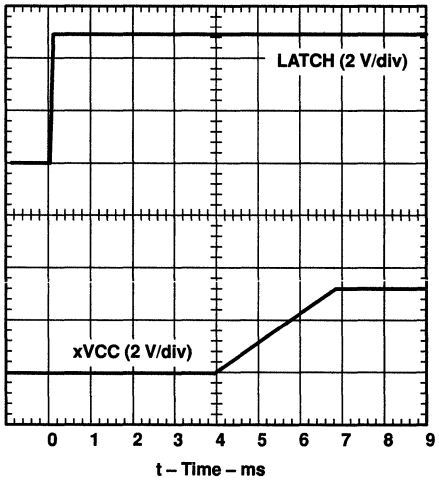


Figure 9. xVCC Propagation Delay and Rise Time With 150-μF Load, 3.3-V Switch, $V_{I(5\ V)} = 0$

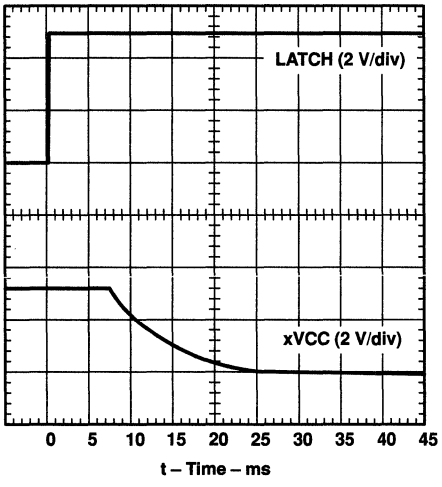


Figure 10. xVCC Propagation Delay and Fall Time With 150-μF Load, 3.3-V Switch, $V_{I(5\ V)} = 0$

PARAMETER MEASUREMENT INFORMATION

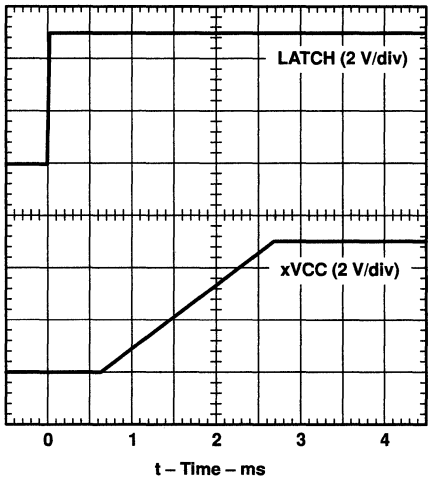


Figure 11. xVCC Propagation Delay and Rise Time With 1-μF Load, 5-V Switch

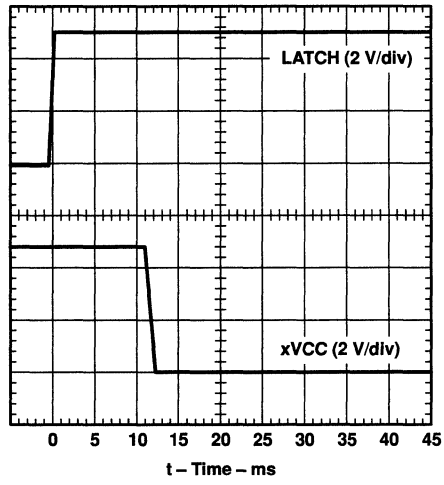


Figure 12. xVCC Propagation Delay and Fall Time With 1-μF Load, 5-V Switch

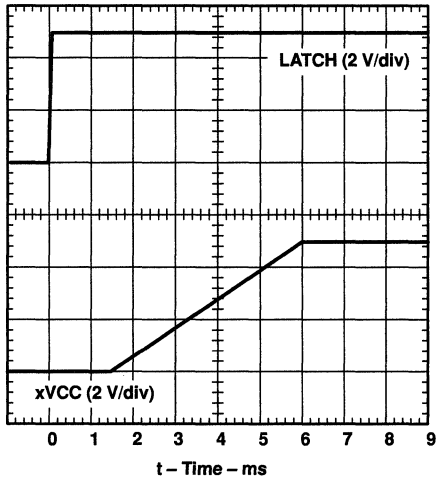


Figure 13. xVCC Propagation Delay and Rise Time With 150-μF Load, 5-V Switch

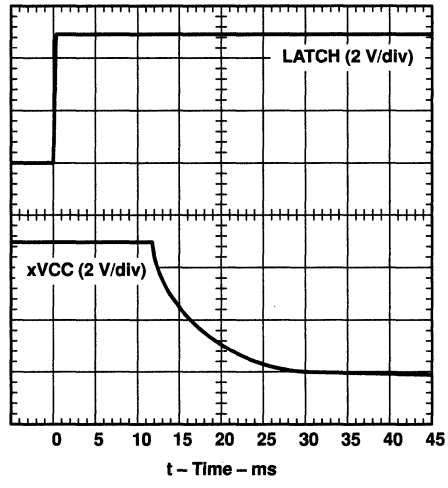


Figure 14. xVCC Propagation Delay and Fall Time With 150-μF Load, 5-V Switch

PARAMETER MEASUREMENT INFORMATION

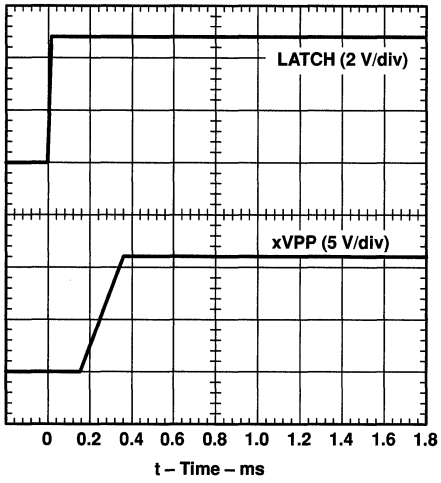


Figure 15. xVPP Propagation Delay and Rise Time With 1-μF Load, 12-V Switch

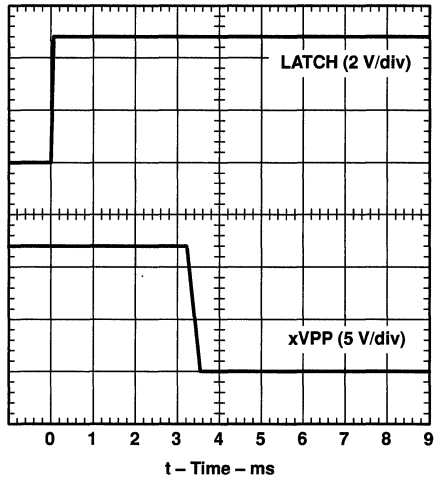


Figure 16. xVPP Propagation Delay and Fall Time With 1-μF Load, 12-V Switch

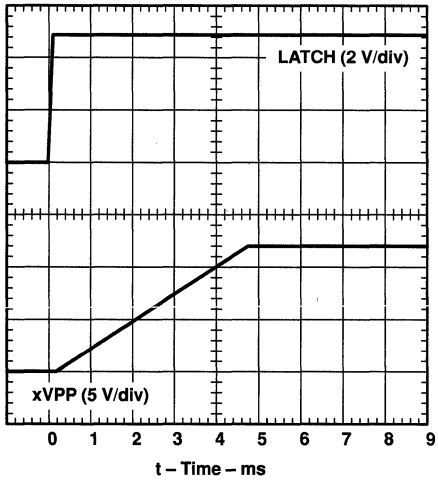


Figure 17. xVPP Propagation Delay and Rise Time With 150-μF Load, 12-V Switch

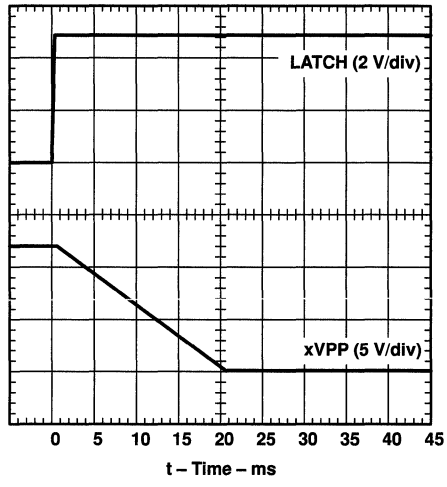


Figure 18. xVPP Propagation Delay and Fall Time With 150-μF Load, 12-V Switch

TYPICAL CHARACTERISTICS

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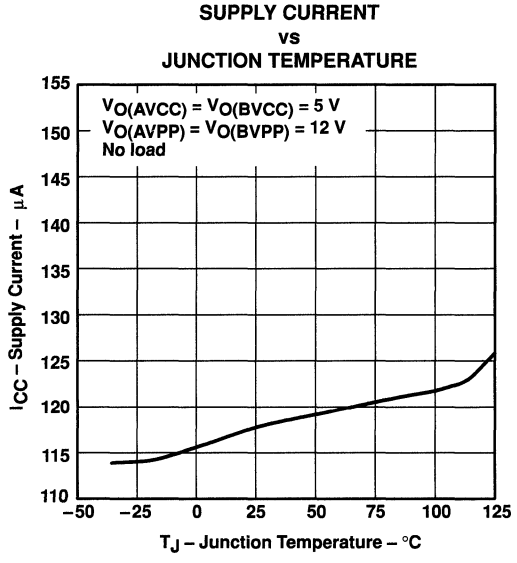

Figure 19

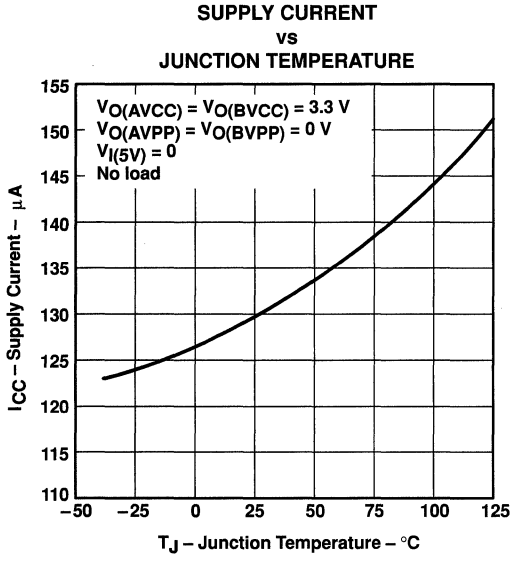

Figure 20

TYPICAL CHARACTERISTICS

3.3-V SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

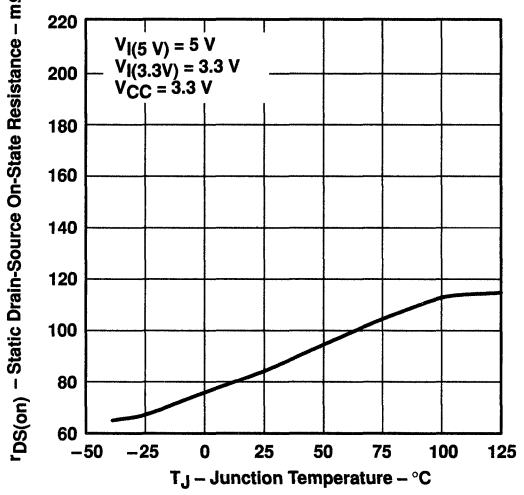

Figure 21

3.3-V SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

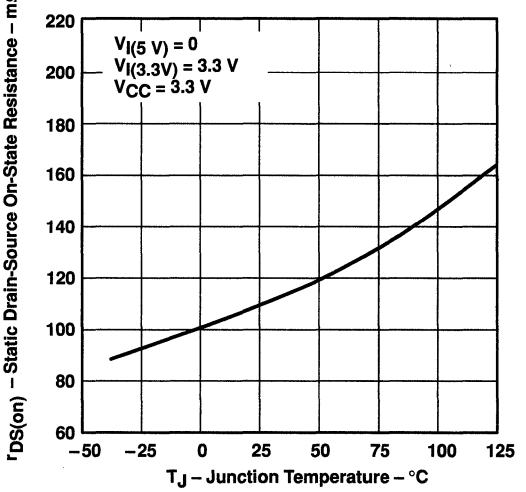

Figure 22

5-V SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

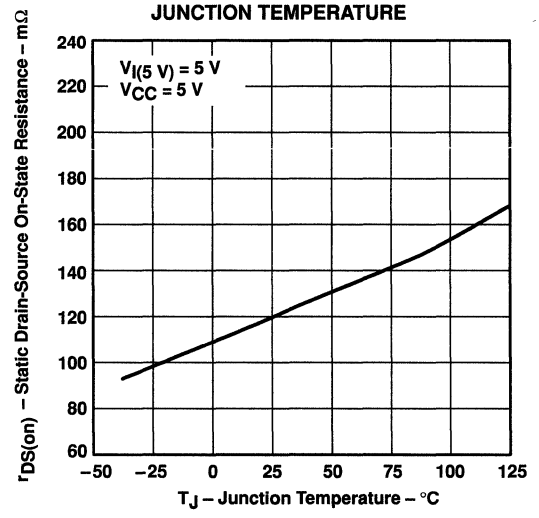

Figure 23

12-V SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

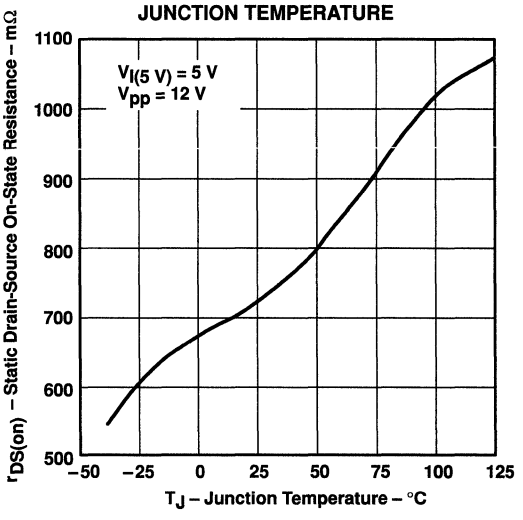

Figure 24

TYPICAL CHARACTERISTICS

5-V SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

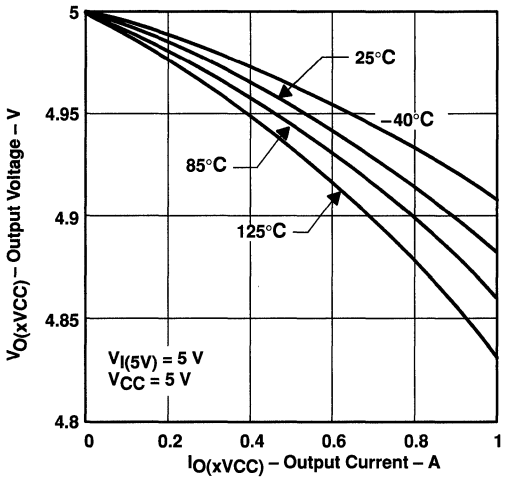

Figure 25

3.3-V SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

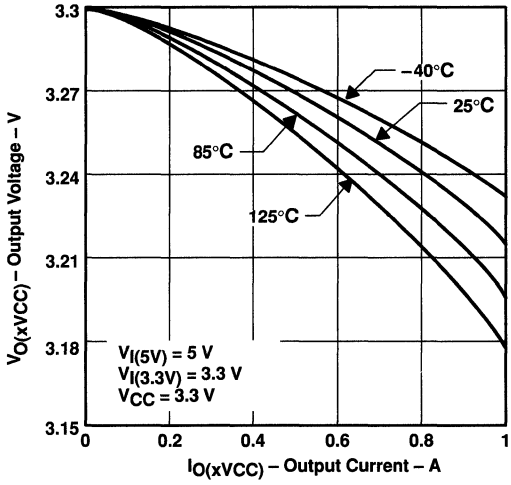

Figure 26

3.3-V SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

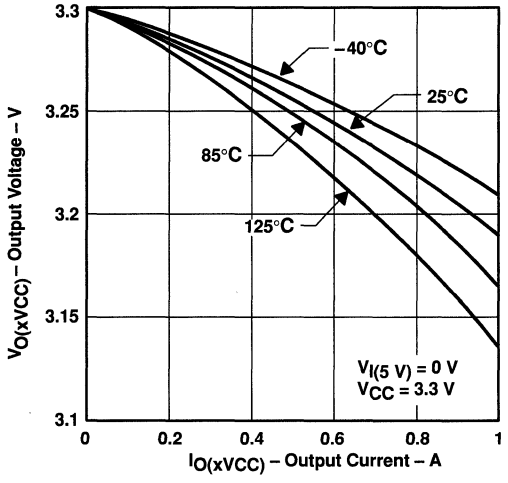

Figure 27

12-V SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

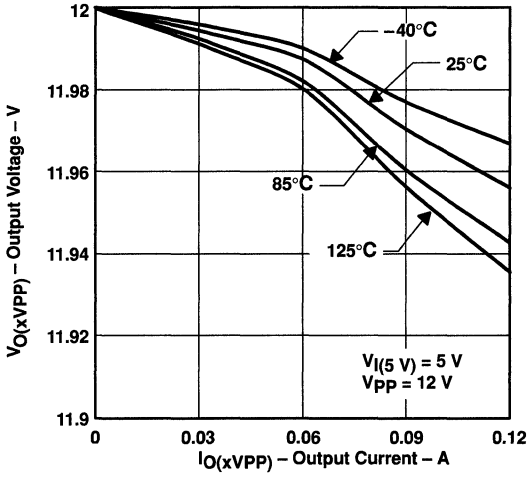

Figure 28

TYPICAL CHARACTERISTICS

5-V SWITCH
SHORT-CIRCUIT CURRENT
vs
JUNCTION TEMPERATURE

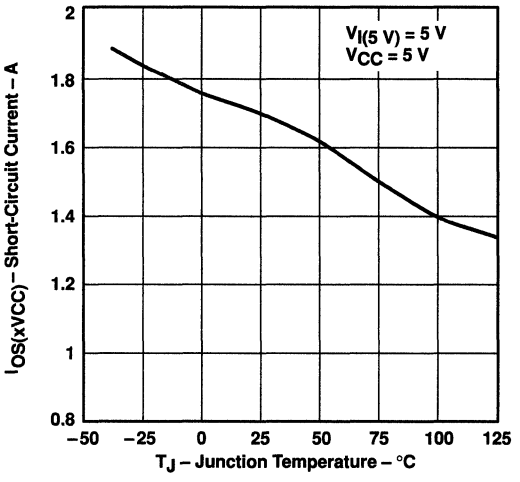

Figure 29

3.3-V SWITCH
SHORT-CIRCUIT CURRENT
vs
JUNCTION TEMPERATURE

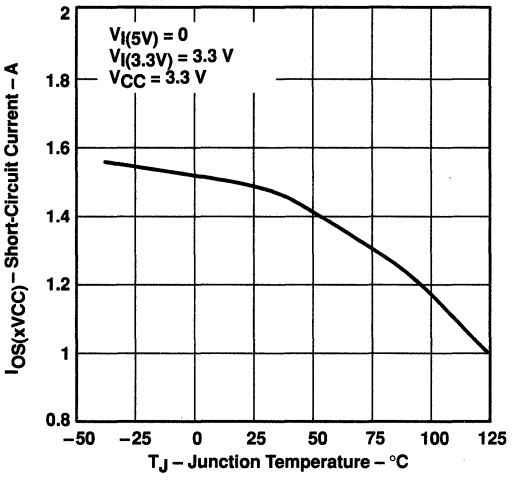

Figure 30

12-V SWITCH
SHORT-CIRCUIT CURRENT
vs
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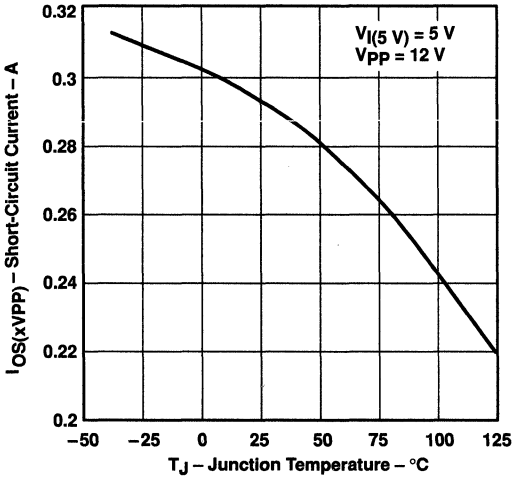


Figure 31

APPLICATION INFORMATION

overview

PC Cards were initially introduced as a means to add EEPROM (flash memory) to portable computers with limited on-board memory. The idea of add-in cards quickly took hold; modems, wireless LANs, Global Positioning Satellite System (GPS), multimedia, and hard-disk versions were soon available. As the number of PC Card applications grew, the engineering community quickly recognized the need for a standard to ensure compatibility across platforms. To this end, the PCMCIA was established, comprised of members from leading computer, software, PC Card, and semiconductor manufacturers. One key goal was to realize the "plug-and-play" concept. Cards and hosts from different vendors should be compatible — able to communicate with one another transparently.

PC Card power specification

System compatibility also means power compatibility. The most current set of specifications (PC Card Standard) set forth by the PCMCIA committee states that power is to be transferred between the host and the card through eight of the 68 terminals of the PC Card connector. This power interface consists of two V_{CC}, two V_{pp}, and four ground terminals. Multiple V_{CC} and ground terminals minimize connector-terminal and line resistance. The two V_{pp} terminals were originally specified as separate signals but are commonly tied together in the host to form a single node to minimize voltage losses. Card primary power is supplied through the V_{CC} terminals; flash-memory programming and erase voltage is supplied through the V_{pp} terminals.

designing for voltage regulation

The current PCMCIA specification for output-voltage regulation ($V_{O(reg)}$) of the 5-V output is 5% (250 mV). In a typical PC power-system design, the power supply has an output-voltage regulation ($V_{PS(reg)}$) of 2% (100 mV). Also, a voltage drop from the power supply to the PC Card will result from resistive losses (V_{PCB}) in the PCB traces and the PCMCIA connector. A typical design would limit the total of these resistive losses to less than 1% (50 mV) of the output voltage. Therefore, the allowable voltage drop (V_{DS}) for the TPS2206 would be the PCMCIA voltage regulation less the power supply regulation and less the PCB and connector resistive drops:

$$V_{DS} = V_{O(reg)} - V_{PS(reg)} - V_{PCB} \quad (1)$$

Typically, this would leave 100 mV for the allowable voltage drop across the TPS2206. The voltage drop is the output current multiplied by the switch resistance of the TPS2206. Therefore, the maximum output current that can be delivered to the PC Card in regulation is the allowable voltage drop across the TPS2206 divided by the output switch resistance.

$$I_O max = \frac{V_{DS}}{r_{DS(on)}} \quad (2)$$

The xVCC outputs have been designed to deliver 700 mA at 5 V within regulation over the operating temperature range. Current proposals for the PCMCIA specifications are to limit the power dissipated in the PCMCIA slot to 3 W. With an input voltage of 5 V, 700 mA continuous is the maximum current that can be delivered to the PC Card. The TPS2206 is capable of delivering up to 1 A continuously, but during worst-case conditions the output may not be within regulation. This is generally acceptable because the majority of PC Cards require less than 700 mA continuous. Some cards require higher peak currents (disk drives during initial platter spin-up), but it is generally acceptable for small voltage sags to occur during these peak currents.

The xVCC outputs have been designed to deliver 1 A continuously at 3.3 V within regulation over the operating temperature range. The PCMCIA specification for output voltage regulation of the 3.3-V output is 300 mV. Using the voltage drop percentages (2%) for power supply regulation and PCB resistive loss (1%), the allowable voltage drop for the 3.3 V switch is 200 mV.

The xVPP outputs have been designed to deliver 150 mA continuously at 12 V.

APPLICATION INFORMATION

overcurrent and over-temperature protection

PC Cards are inherently subject to damage that can result from mishandling. Host systems require protection against short-circuited cards that could lead to power supply or PCB-trace damage. Even systems robust enough to withstand a short circuit would still undergo rapid battery discharge into the damaged PC Card, resulting in the rather sudden and unacceptable loss of system power. Most hosts include fuses for protection. However, the reliability of fused systems is poor, as blown fuses require troubleshooting and repair, usually by the manufacturer.

The TPS2206 takes a two-pronged approach to overcurrent protection. First, instead of fuses, sense FETs monitor each of the power outputs. Excessive current generates an error signal that linearly limits the output current, preventing host damage or failure. Sense FETs, unlike sense resistors or polyfuses, have an added advantage in that they do not add to the series resistance of the switch and thus produce no additional voltage losses. Second, when an overcurrent condition is detected, the TPS2206 asserts a signal at $\overline{OC}$ that can be monitored by the microprocessor to initiate diagnostics and/or send the user a warning message. In the event that an overcurrent condition persists, causing the IC to exceed its maximum junction temperature, thermal-protection circuitry activates, shutting down all power outputs until the device cools to within a safe operating region.

12-V supply not required

Most PC Card switches use the externally supplied 12-V V_{pp} power for switch-gate drive and other chip functions, which requires that power be present at all times. The TPS2206 offers considerable power savings by using an internal charge pump to generate the required higher voltages from the 5-V or 3.3-V input; therefore, the external 12-V supply can be disabled except when needed for flash-memory functions, thereby extending battery lifetime. Do not ground the 12-V input if the 12-V input is not used. Additional power savings are realized by the TPS2206 during a software shutdown in which quiescent current drops to a maximum of 1 μA.

backward compatibility and 3.3-V low-voltage mode

The TPS2206 is backward compatible with the TPS2202 AND TPS2202A products, with the following considerations. Pin 25 (V_{DD} on TPS2202/TPS2202A) is a no connect because bias current is derived from either the 3.3-V input pin or the 5-V input pin. Also, the TPS2206 does not have the APWR_GOOD or BPWR_GOOD VPP reporting outputs. These are left as no connects.

The TPS2206 operates in 3.3-V low-voltage mode when 3.3 volts is the only available input voltage ($V_{I(5V)}$=0). This allows host and PC Cards to be operated in low-power 3.3-V-only modes such as sleep modes or pager modes. Note that in this operation mode, the TPS2206 derives its bias current from the 3.3-V input pin and only 3.3 V can be delivered to the PC Card. The 3.3-V switch resistance increases, but the added switch resistance should not be critical, because only a small amount of current is delivered in this mode. If 6% (198 mV) is allowed for the 3.3-V switch voltage drop, a 500 mΩ switch could deliver over 350 mA to the PC Card.

voltage transitioning requirement

PC Cards, like portables, are migrating from 5 V to 3.3 V to minimize power consumption, optimize board space, and increase logic speeds. The TPS2206 is designed to meet all combinations of power delivery as currently defined in the PCMCIA standard. The latest protocol accommodates mixed 3.3-V/5-V systems by first powering the card with 5 V, then polling it to determine its 3.3-V compatibility. The PCMCIA specification requires that the capacitors on 3.3-V-compatible cards be discharged to below 0.8 V before applying 3.3-V power. This ensures that sensitive 3.3-V circuitry is not subjected to any residual 5-V charge and functions as a power reset. The TPS2206 offers a selectable V_{CC} and V_{pp} ground state, in accordance with PCMCIA 3.3-V/5-V switching specifications, to fully discharge the card capacitors while switching between V_{CC} voltages.

APPLICATION INFORMATION

output ground switches

Several PCMCIA power-distribution switches on the market do not have an active-grounding FET switch. These devices do not meet the PC Card specification requiring a discharge of V_{CC} within 100 ms. PC Card resistance can not be relied on to provide a discharge path for voltages stored on PC Card capacitance because of possible high-impedance isolation by power-management schemes. A method commonly shown to alleviate this problem is to add to the switch output an external 100-kΩ resistor in parallel with the PC Card. Considering that this is the only discharge path to ground, a timing analysis shows that the RC time constant delays the required discharge time to more than 2 seconds. The only way to ensure timing compatibility with PC Card standards is to use a power-distribution switch that has an internal ground switch, like that of the TPS22xx family, or add an external ground FET to each of the output lines with the control logic necessary to select it.

In summary, the TPS2206 is a complete single-chip dual-slot PC Card power interface. It meets all currently defined PCMCIA specifications for power delivery in 5-V, 3.3-V, and mixed systems, and offers a serial control interface. The TPS2206 offers functionality, power savings, overcurrent and thermal protection, and fault reporting in one 30-pin SSOP surface-mount package for maximum value added to new portable designs.

power supply considerations

The TPS2206 has multiple pins for each of its 3.3-V, 5-V, and 12-V power inputs and for the switched V_{CC} outputs. Any individual pin can conduct the rated input or output current. Unless all pins are connected in parallel, the series resistance is significantly higher than that specified, resulting in increased voltage drops and lost power. Both 12-V inputs must be connected for proper V_{pp} switching; it is recommended that all input and output power pins be paralleled for optimum operation.

Although the TPS2206 is fairly immune to power input fluctuations and noise, it is generally considered good design practice to bypass power supplies typically with a 1-µF electrolytic or tantalum capacitor paralleled by a 0.047-µF to 0.1-µF ceramic capacitor. It is strongly recommended that the switched V_{CC} and V_{pp} outputs be bypassed with a 0.1-µF or larger capacitor; doing so improves the immunity of the TPS2206 to electrostatic discharge (ESD). Care should be taken to minimize the inductance of PCB traces between the TPS2206 and the load. High switching currents can produce large negative-voltage transients, which forward biases substrate diodes, resulting in unpredictable performance. Similary, no pin should be taken below −0.3 V.

RESET or $\overline{\text{RESET}}$ inputs

To ensure that cards are in a known state after power brownouts or system initialization, the PC Cards should be reset at the same time as the host by applying a low impedance to the V_{CC} and V_{pp} terminals. A low-impedance output state allows discharging of residual voltage remaining on PC Card filter capacitance, permitting the system (host and PC Cards) to be powered up concurrently. The RESET or $\overline{\text{RESET}}$ input closes internal switches S1, S4, S7, and S10 with all other switches left open (see TPS2206 control-logic table). The TPS2206 remains in the low-impedance output state until the signal is deasserted and further data is clocked in and latched. RESET or $\overline{\text{RESET}}$ is provided for direct compatibility with systems that use either an active-low or active-high reset voltage supervisor. The unused pin is internally pulled up or down and should be left unconnected.

APPLICATION INFORMATION

overcurrent and thermal protection

The TPS2206 uses sense FETs to check for overcurrent conditions in each of the V_{CC} and V_{pp} outputs. Unlike sense resistors or polyfuses, these FETs do not add to the series resistance of the switch; therefore, voltage and power losses are reduced. Overcurrent sensing is applied to each output separately. When an overcurrent condition is detected, only the power output affected is limited; all other power outputs continue to function normally. The $\overline{OC}$ indicator, normally a logic high, is a logic low when any overcurrent condition is detected, providing for initiation of system diagnostics and/or sending a warning message to the user.

During power up, the TPS2206 controls the rise time of the V_{CC} and V_{pp} outputs and limits the current into a faulty card or connector. If a short circuit is applied after power is established (e.g., hot insertion of a bad card), current is initially limited only by the impedance between the short and the power supply. In extreme cases, as much as 10 A to 15 A may flow into the short before the current limiting of the TPS2206 engages. If the V_{CC} or V_{pp} outputs are driven below ground, the TPS2206 may latch nondestructively in an off state. Cycling power will reestablish normal operation.

Overcurrent limiting for the V_{CC} outputs is designed to activate, if powered up, into a short in the range of 1 A to 2.2 A, typically at about 1.6 A. The V_{pp} outputs limit from 120 mA to 400 mA, typically around 280 mA. The protection circuitry acts by linearly limiting the current passing through the switch rather than initiating a full shutdown of the supply. Shutdown occurs only during thermal limiting.

Thermal limiting prevents destruction of the IC from overheating if the package power-dissipation ratings are exceeded. Thermal limiting disables all power outputs (both A and B slots) until the device has cooled.

calculating junction temperature

The switch resistance, $r_{DS(on)}$, is dependent on the junction temperature, T_J, of the die. The junction temperature is dependent on both $r_{DS(on)}$ and the current through the switch. To calculate T_J, first find $r_{DS(on)}$ from Figures 21, 22, 23, and 24 using an initial temperature estimate about 50°C above ambient. Then calculate the power dissipation for each switch, using the formula:

$$P_D = r_{DS(on)} \times I^2 \quad (3)$$

Next, sum the power dissipation and calculate the junction temperature:

$$T_J = \left(\Sigma P_D \times R_{\theta JA}\right) + T_A,\ R_{\theta JA} = 108°C/W \quad (4)$$

Compare the calculated junction temperature with the initial temperature estimate. If the temperatures are not within a few degrees of each other, recalculate using the calculated temperature as the initial estimate.

logic input and outputs

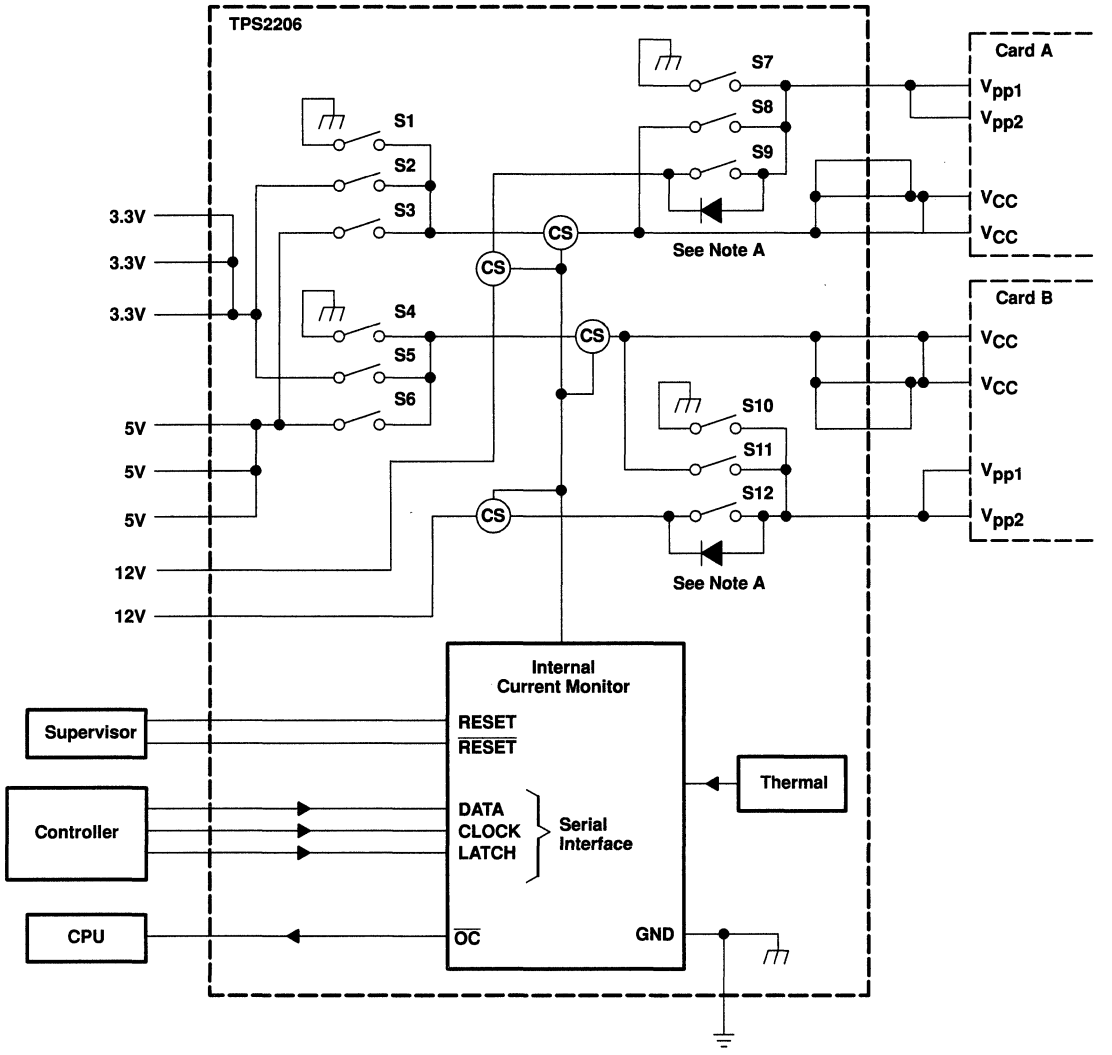
The serial interface consists of DATA, CLOCK, and LATCH leads. The data is clocked in on the positive leading edge of the clock (see Figure 2). The 9-bit (D0 through D8) serial data word is loaded during the positive edge of the latch signal. The latch signal should occur before the next positive leading edge of the clock.

The shutdown bit of the data word places all V_{CC} and V_{pp} outputs in a high-impedance state and reduces chip quiescent current to 1 μA to conserve battery power.

The TPS2206 serial interface is designed to be compatible with serial-interface PCMCIA controllers and current PCMCIA and Japan Electronic Industry Development Association (JEIDA) standards.

An overcurrent output ($\overline{OC}$) is provided to indicate an overcurrent condition in any of the V_{CC} or V_{pp} outputs as previously discussed.

APPLICATION INFORMATION



NOTE A. MOSFET switches S9 and S12 have a back-gate diode from the source to the drain. Unused switch inputs should never be grounded.

Figure 32. Internal Switching Matrix

APPLICATION INFORMATION

TPS2206 control logic

AVPP

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
D8 $\overline{SHDN}$	D0 A_VPP_PGM	D1 A_VPP_VCC	S7	S8	S9	VAVPP
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	VCC†
1	1	0	OPEN	OPEN	CLOSED	VPP(12 V)
1	1	1	OPEN	OPEN	OPEN	Hi-Z
0	X	X	OPEN	OPEN	OPEN	Hi-Z

BVPP

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
D8 $\overline{SHDN}$	D4 B_VPP_PGM	D5 B_VPP_VCC	S10	S11	S12	VBVPP
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	VCC‡
1	1	0	OPEN	OPEN	CLOSED	VPP(12 V)
1	1	1	OPEN	OPEN	OPEN	Hi-Z
0	X	X	OPEN	OPEN	OPEN	Hi-Z

AVCC

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
D8 $\overline{SHDN}$	D3 $\overline{A\_VCC3}$	D2 $\overline{A\_VCC5}$	S1	S2	S3	VAVCC
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	3.3 V
1	1	0	OPEN	OPEN	CLOSED	5 V
1	1	1	CLOSED	OPEN	OPEN	0 V
0	X	X	OPEN	OPEN	OPEN	Hi-Z

BVCC

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
D8 $\overline{SHDN}$	D6 $\overline{B\_VCC3}$	D7 $\overline{B\_VCC5}$	S4	S5	S6	VBVCC
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	3.3 V
1	1	0	OPEN	OPEN	CLOSED	5 V
1	1	1	CLOSED	OPEN	OPEN	0 V
0	X	X	OPEN	OPEN	OPEN	Hi-Z

† Output depends on AVCC
‡ Output depends on BVCC

ESD protection

All TPS2206 inputs and outputs incorporate ESD-protection circuitry designed to withstand a 2-kV human-body-model discharge as defined in MIL-STD-883C, Method 3015. The V_{CC} and V_{pp} outputs can be exposed to potentially higher discharges from the external environment through the PC Card connector. Bypassing the outputs with 0.1-µF capacitors protects the devices from discharges up to 10 kV.

APPLICATION INFORMATION

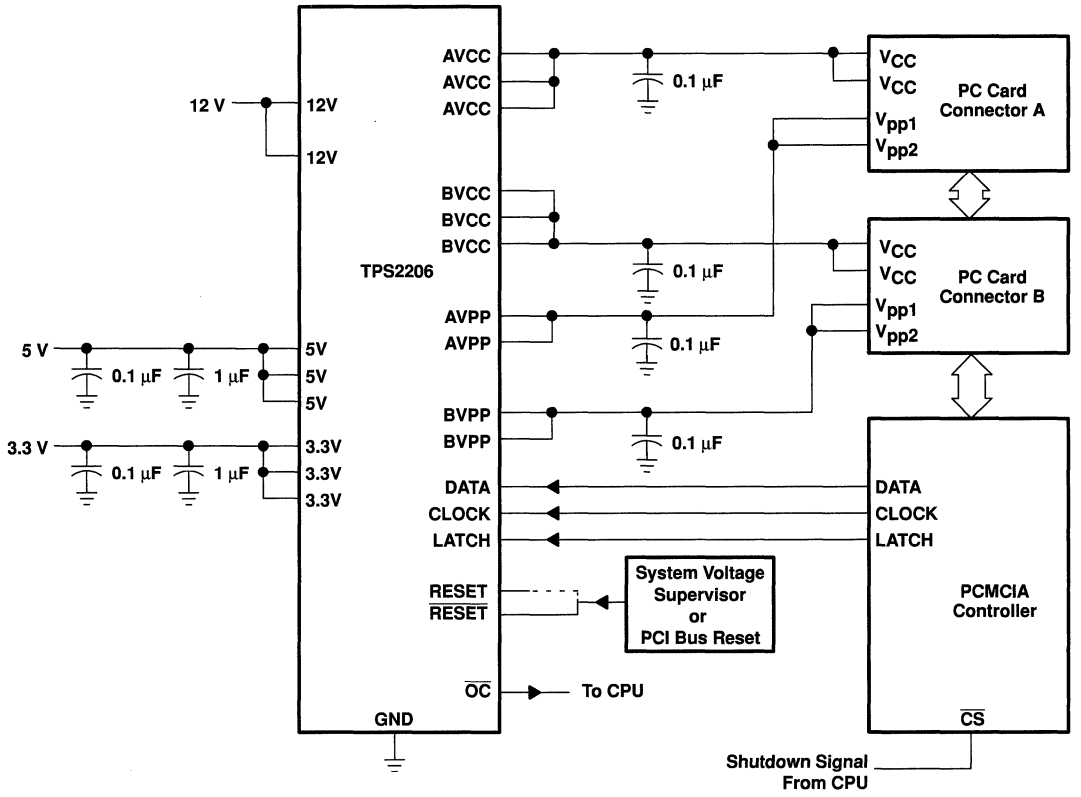


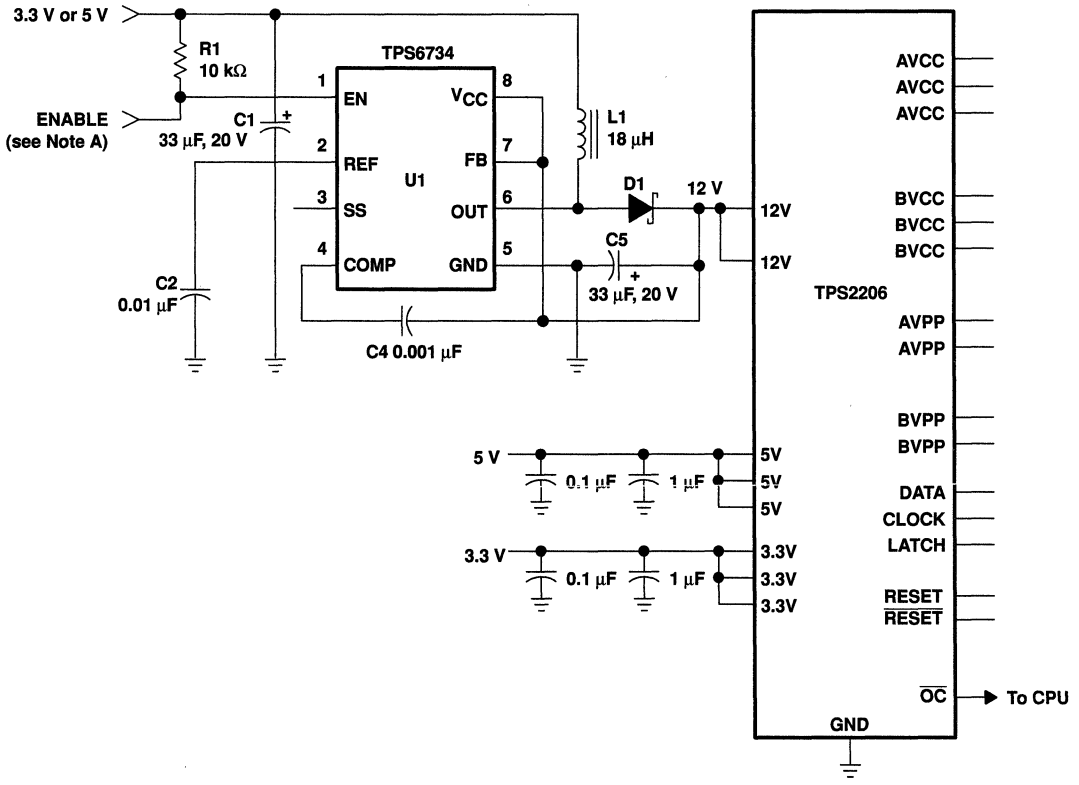
Figure 33. Detailed Interconnections and Capacitor Recommendations

APPLICATION INFORMATION

12-V flash memory supply

The TPS6734 is a fixed 12-V output boost converter capable of delivering 120 mA from inputs as low as 2.7 V. The device is pin-for-pin compatible with the MAX734 regulator and offers the following advantages: lower supply current, wider operating input-voltage range, and higher output currents. As shown in Figure 1, the only external components required are: an inductor, a Schottky rectifier, an output filter capacitor, an input filter capacitor, and a small capacitor for loop compensation. The entire converter occupies less than 0.7 in^2 of PCB space when implemented with surface-mount components. An enable input is provided to shut the converter down and reduce the supply current to 3 μA when 12 V is not needed.

The TPS6734 is a 170-kHz current-mode PWM (pulse-width modulation) controller with an n-channel MOSFET power switch. Gate drive for the switch is derived from the 12-V output after start-up to minimize the die area needed to realize the 0.7-Ω MOSFET and improve efficiency at input voltages below 5 V. Soft start is accomplished with the addition of one small capacitor. A 1.22-V reference (pin 2) is brought out for external use. For additional information, see the TPS6734 data sheet (SLVS127).



NOTE A. The enable terminal can be tied to a generall purpose I/O terminal on the PCMCIA controller or tied high.

Figure 34. TPS2206 with TPS6734 12-V, 120-mA Supply

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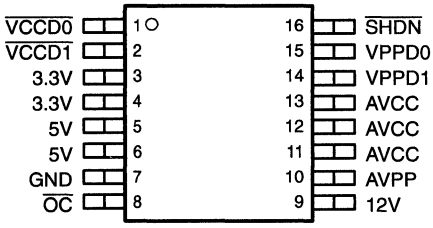
- **Fully Integrated V_{CC} and V_{pp} Switching for Single-Slot PC Card™ Interface**
- **Low $r_{DS(on)}$ (90-mΩ 5-V V_{CC} Switch and 3.3-V V_{CC} Switch)**
- **Compatible With Controllers From Cirrus, Ricoh, O_2Micro, Intel, and Texas Instruments**
- **3.3-V Low-Voltage Mode**
- **Meets PC Card Standards**
- **12-V Supply Can Be Disabled Except During 12-V Flash Programming**
- **Short-Circuit and Thermal Protection**
- **Space-Saving 16-Pin SSOP (DB)**
- **Compatible With 3.3-V, 5-V, and 12-V PC Cards**
- **Break-Before-Make Switching**

DB PACKAGE
(TOP VIEW)



description

The TPS2211 PC Card power-interface switch provides an integrated power-management solution for a single PC Card. All of the discrete power MOSFETs, a logic section, current limiting, and thermal protection for PC Card control are combined on a single integrated circuit, using the Texas Instruments LinBiCMOS™ process. The circuit allows the distribution of 3.3-V, 5-V, and/or 12-V card power, and is compatible with many PCMCIA controllers. The current-limiting feature eliminates the need for fuses, which reduces component count and improves reliability. Current-limit reporting can help the user isolate a system fault to the PC Card.

The TPS2211 features a 3.3-V low-voltage mode that allows for 3.3-V switching without the need for 5 V. Bias power can be derived from either the 3.3-V or 5-V inputs. This facilitates low-power system designs such as sleep mode and pager mode where only 3.3 V is available.

End equipment for the TPS2211 includes notebook computers, desktop computers, personal digital assistants (PDAs), digital cameras, and bar-code scanners.

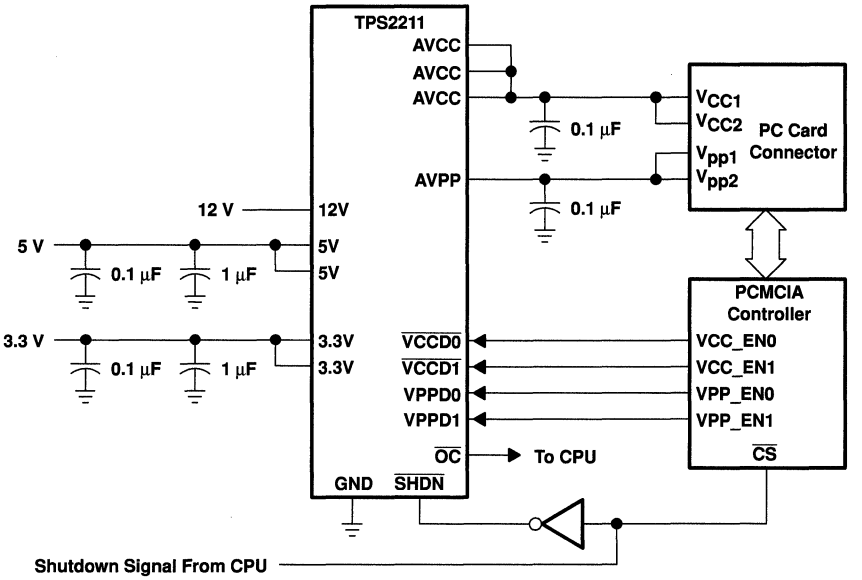
AVAILABLE OPTIONS

T_A	PACKAGED DEVICE	CHIP FORM (Y)
	SMALL OUTLINE (DB)	
–40°C to 85°C	TPS2211IDBLE	TPS2211Y

The DB package is only available left-end taped and reeled (indicated by the LE suffix on the device type, e.g. TPS2211IDBLE).

PC Card is a trademark of PCMCIA (Personal Computer Memory Card International Association).
LinBiCMOS is a trademark of Texas Instruments Incorporated.

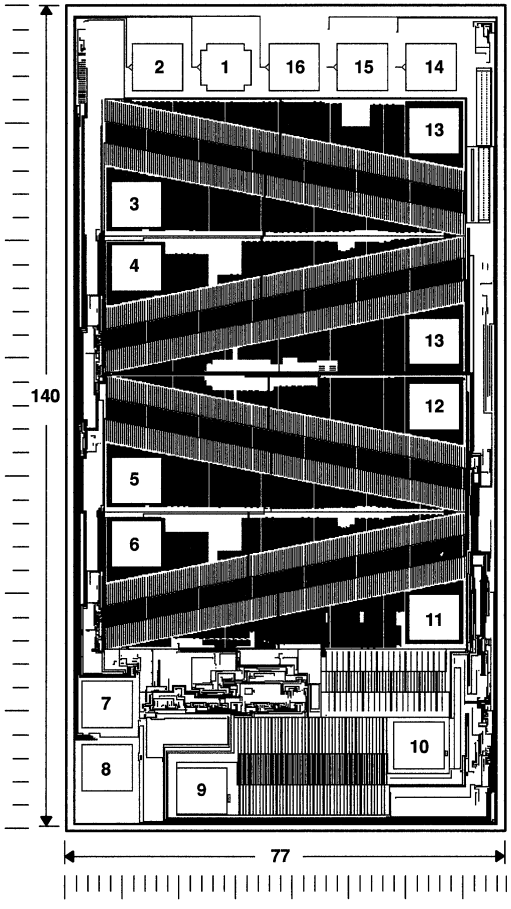
typical PC-card power-distribution application

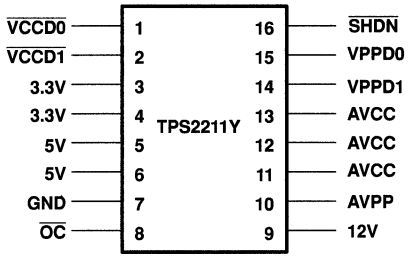


TPS2211Y chip information

This chip, when properly assembled, displays characteristics similar to those of the TPS2211. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
3.3V	3, 4	I	3.3-V V_{CC} input for card power and/or chip power if 5 V is not present
5V	5, 6	I	5-V V_{CC} input for card power and/or chip power
12V	9	I	12-V V_{pp} input card power
AVCC	11, 12, 13	O	Switched output that delivers 0 V, 3.3-V, 5-V, or high impedance to card
AVPP	10	O	Switched output that delivers 0 V 3.3-V, 5-V, 12-V, or high impedance to card
GND	7		Ground
$\overline{OC}$	8	O	Logic-level overcurrent reporting output that goes low when an overcurrent conditions exists
$\overline{SHDN}$	16	I	Logic input that shuts down the TPS2211 and sets all power outputs to high-impedance state
$\overline{VCCD0}$	1	I	Logic input that controls voltage of AVCC (see control-logic table)
$\overline{VCCD1}$	2	I	Logic input that controls voltage of AVCC (see control-logic table)
VPPD0	15	I	Logic input that controls voltage of AVPP (see control-logic table)
VPPD1	14	I	Logic input that controls voltage of AVPP (see control-logic table)

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Input voltage range for card power: $V_{I(5V)}$ ..... –0.3 V to 7 V
$V_{I(3.3V)}$ ..... –0.3 V to 7 V
$V_{I(12V)}$ ..... –0.3 V to 14 V
Logic input voltage ..... –0.3 V to 7 V
Continuous total power dissipation ..... See Dissipation Rating Table
Output current (each card): $I_{O(VCC)}$ ..... internally limited
$I_{O(VPP)}$ ..... internally limited
Operating virtual junction temperature range, T_J ..... –40°C to 150°C
Operating free-air temperature range, T_A ..... –40°C to 85°C
Storage temperature range, T_{stg} ..... –55°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DB	775 mW	6.2 mW/°C	496 mW	403 mW

These devices are mounted on an FR4 board with no special thermal considerations.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	$V_{I(5V)}$	0	5.25	V
	$V_{I(3.3V)}$	0	5.25	V
	$V_{I(12V)}$	0	13.5	V
Output current	$I_{O(AVCC)}$		1	A
	$I_{O(AVPP)}$		150	mA
Operating virtual junction temperature, T_J		–40	125	°C

electrical characteristics, T_A = –40°C to 85°C (unless otherwise noted)

power switch

PARAMETER			TEST CONDITIONS†	TPS2211 MIN	TPS2211 TYP	TPS2211 MAX	UNIT
	Switch resistance	5 V to AVCC	$V_{I(5V)}$ = 5 V		50	90	mΩ
		3.3 V to AVCC	$V_{I(5V)}$ = 5 V, $V_{I(3.3V)}$ = 3.3 V		48	90	
		3.3 V to AVCC	$V_{I(5V)}$ = 0 V, $V_{I(3.3V)}$ = 3.3 V		48	90	
		5 V to AVPP	T_J=25°C			6	Ω
		3.3 V to AVPP	T_J=25°C			6	
		12 V to AVPP	T_J=25°C			1	
$V_{O(AVPP)}$	Clamp low voltage		I_{pp} at 10 mA			0.8	V
$V_{O(AVCC)}$	Clamp low voltage		I_{CC} at 10 mA			0.8	V
I_{lkg}	Leakage current	I_{pp} high-impedance state	T_A = 25°C		1	10	µA
			T_A= 85°C			50	
		I_{CC} high-impedance state	T_A = 25°C		1	10	
			T_A=85°C			50	
I_I	Input current	$V_{I(5V)}$ = 5 V	$V_{O(AVCC)}$ = 5 V, $V_{O(AVPP)}$ = 12 V		40	150	µA
		$V_{I(5V)}$ = 0 V, $V_{I(3.3V)}$ = 3.3 V	$V_{O(AVCC)}$ = 3.3 V, $V_{O(AVPP)}$ = 12 V		40	150	
		Shutdown mode	$V_{O(AVCC)}$ = $V_{O(AVPP)}$ = Hi-Z			1	
I_{OS}	Short-circuit output-current limit	$I_{O(AVCC)}$	T_J = 85°C, output powered into a short to GND	1		2.2	A
		$I_{O(AVPP)}$		120		400	mA

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

logic section

PARAMETER	TEST CONDITIONS†	TPS2211 MIN	TPS2211 MAX	UNIT
Logic input current			1	µA
Logic input high level		2		V
Logic input low level			0.8	V
Logic output high level	$V_{I(5V)}$ = 5 V, I_O = 1 mA	$V_{I(5V)}$ – 0.4		V
	$V_{I(5V)}$ = 0 V, I_O = 1 mA, $V_{I(3.3V)}$ = 3.3 V	$V_{I(3.3V)}$ – 0.4		
Logic output low level	I_O = 1 mA		0.4	V

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics, T_A = 25°C (unless otherwise noted)

power switch

PARAMETER			TEST CONDITIONS†	TPS2211Y MIN	TPS2211Y TYP	TPS2211Y MAX	UNIT
	Switch resistance	5 V to AVCC	$V_{I(5V)}$ = 5 V		50		mΩ
		3.3 V to AVCC	$V_{I(5V)}$ = 5 V, $V_{I(3.3V)}$ = 3.3 V		48		
		3.3 V to AVCC	$V_{I(5V)}$ = 0 V, $V_{I(3.3V)}$ = 3.3 V		48		
		5 V to AVPP	T_J=25°C		4.3		Ω
		3.3 V to AVPP	T_J=25°C		4.3		
		12 V to AVPP	T_J=25°C		0.5		
$V_{O(AVPP)}$	Clamp low voltage		I_{pp} at 10 mA		0.28		V
$V_{O(AVCC)}$	Clamp low voltage		I_{pp} at 10 mA		0.28		V
I_{lkg}	Leakage current	I_{pp} high-impedance state			1		μA
		I_{CC} high-impedance state			1		
I_I	Input current	V_I = 5 V	$V_{O(AVCC)}$ = 5 V, $V_{O(AVPP)}$ = 12 V		42		μA
		$V_{I(5V)}$ = 5 V, $V_{I(3.3V)}$ = 3.3 V	$V_{O(AVCC)}$ = 3.3 V, $V_{O(AVPP)}$ = 12 V		42		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

switching characteristics‡

PARAMETER		TEST CONDITIONS§		TPS2211, TPS2211Y MIN	TPS2211, TPS2211Y TYP	TPS2211, TPS2211Y MAX	UNIT
t_r	Rise times, output	$V_{O(AVCC)}$			2.8		ms
		$V_{O(AVPP)}$			6.4		
t_f	Fall times, output	$V_{O(AVCC)}$			4.5		
		$V_{O(AVPP)}$			12		
t_{pd}	Propagation delay (see Figure1)	$V_{I(VPPD0)}$ to $V_{O(AVPP)}$	t_{on}		6.8		ms
			t_{off}		18		
		$V_{I(\overline{VCCD1})}$ to $V_{O(AVCC)}$ (3.3V)	t_{on}		4		
			t_{off}		17		
		$V_{I(\overline{VCCD0})}$ to $V_{O(AVCC)}$ (5V)	t_{on}		6.6		
			t_{off}		17		

‡ Switching Characteristics are with C_L = 150 μF.
§ Refer to Parameter Measurement Information

PARAMETER MEASUREMENT INFORMATION

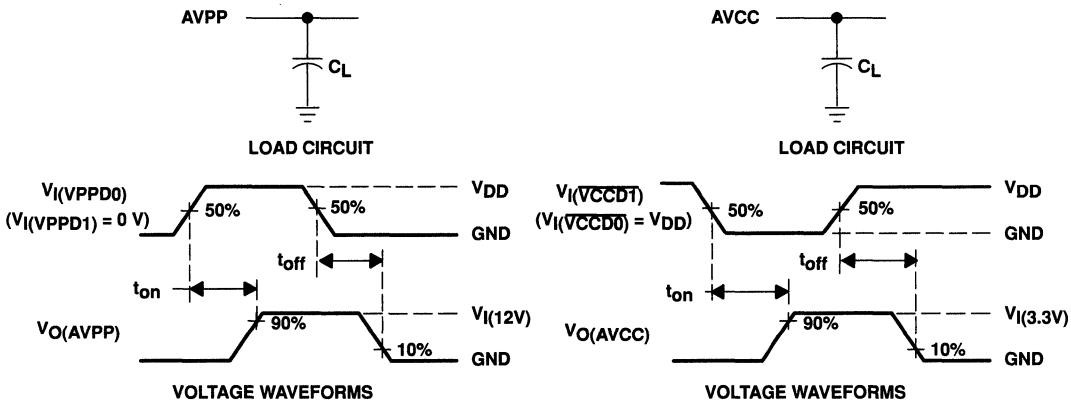


Figure 1. Test Circuits and Voltage Waveforms

Table of Timing Diagrams

	FIGURE
AVCC Propagation Delay and Rise Time With 1-μF Load, 3.3-V Switch	2
AVCC Propagation Delay and Fall Time With 1-μF Load, 3.3-V Switch	3
AVCC Propagation Delay and Rise Time With 150-μF Load, 3.3-V Switch	4
AVCC Propagation Delay and Fall Time With 150-μF Load, 3.3-V Switch	5
AVCC Propagation Delay and Rise Time With 1-μF Load, 5-V Switch	6
AVCC Propagation Delay and Fall Time With 1-μF Load, 5-V Switch	7
AVCC Propagation Delay and Rise Time With 150-μF Load, 5-V Switch	8
AVCC Propagation Delay and Fall Time With 150-μF Load, 5-V Switch	9
AVPP Propagation Delay and Rise Time With 1-μF Load, 12-V Switch	10
AVPP Propagation Delay and Fall Time With 1-μF Load, 12-V Switch	11
AVPP Propagation Delay and Rise Time With 150-μF Load, 12-V Switch	12
AVPP Propagation Delay and Fall Time With 150-μF Load, 12-V Switch	13

PARAMETER MEASUREMENT INFORMATION

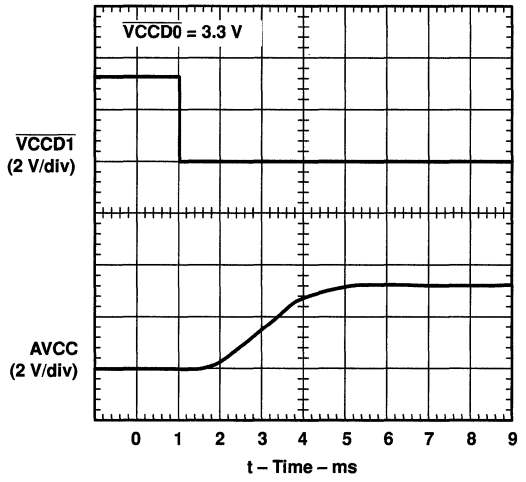


Figure 2. AVCC Propagation Delay and Rise Time With 1-μF Load, 3.3-V Switch

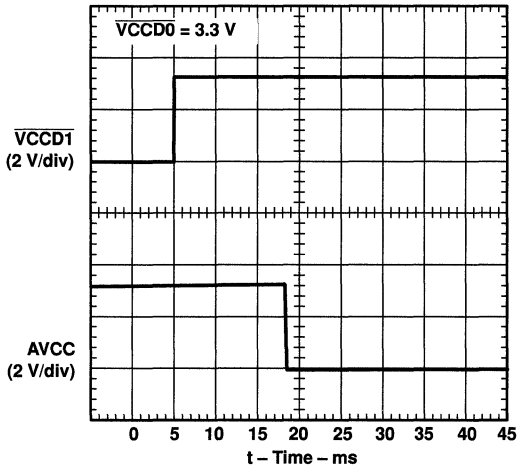


Figure 3. AVCC Propagation Delay and Fall Time With 1-μF Load, 3.3-V Switch

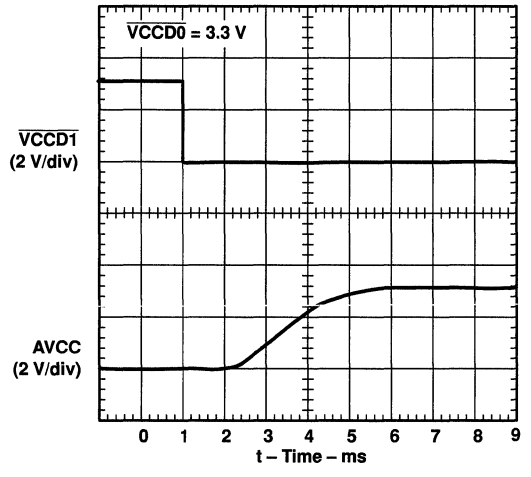


Figure 4. AVCC Propagation Delay and Rise Time With 150-μF Load, 3.3-V Switch

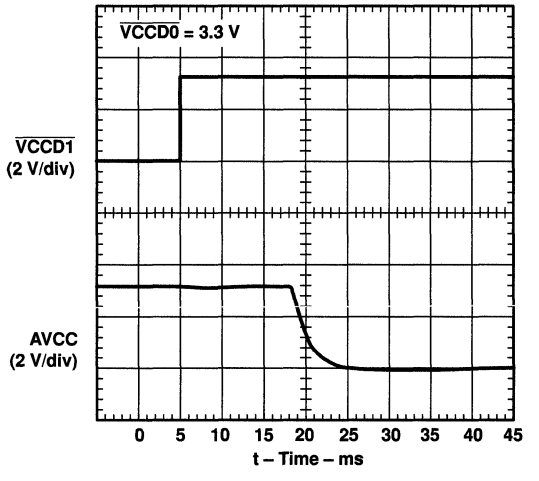


Figure 5. AVCC Propagation Delay and Fall Time With 150-μF Load, 3.3-V Switch

PARAMETER MEASUREMENT INFORMATION

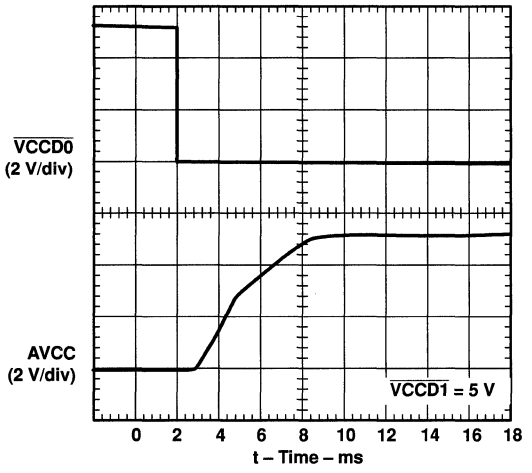


Figure 6. AVCC Propagation Delay and Rise Time With 1-μF Load, 5-V Switch

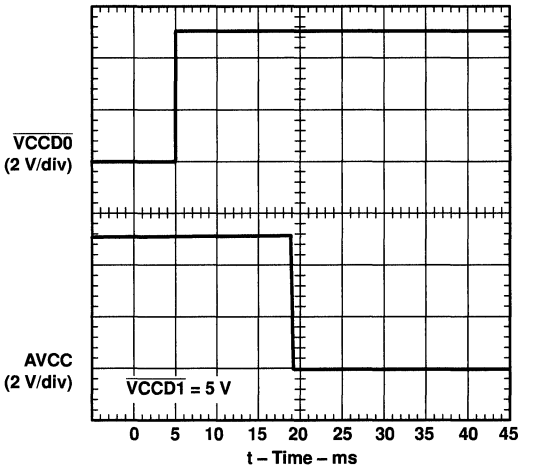


Figure 7. AVCC Propagation Delay and Fall Time With 1-μF Load, 5-V Switch

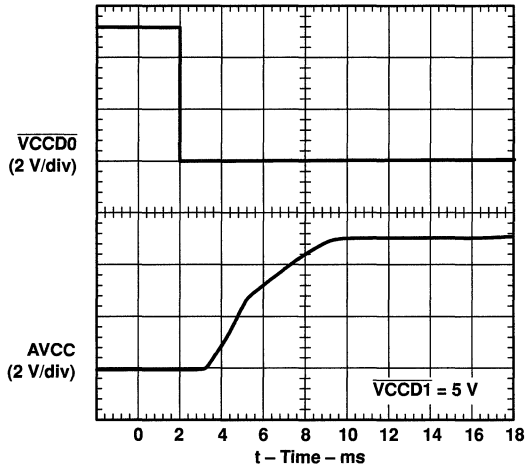


Figure 8. AVCC Propagation Delay and Rise Time With 150-μF Load, 5-V Switch

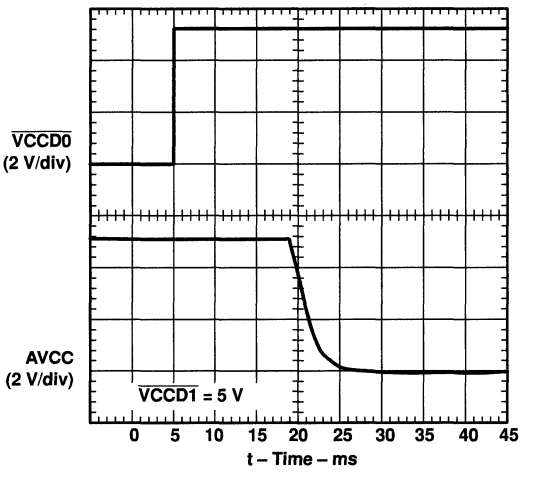


Figure 9. AVCC Propagation Delay and Fall Time With 150-μF Load, 5-V Switch

PARAMETER MEASUREMENT INFORMATION

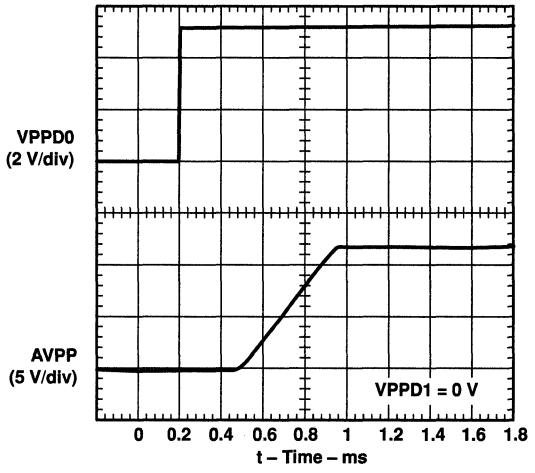


Figure 10. AVPP Propagation Delay and Rise Time With 1-μF Load, 12-V Switch

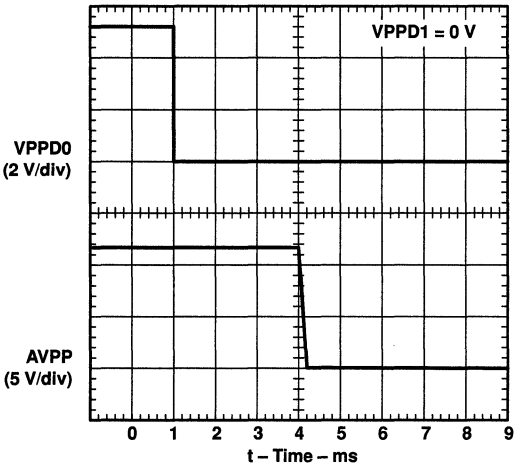


Figure 11. AVPP Propagation Delay and Fall Time With 1-μF Load, 12-V Switch

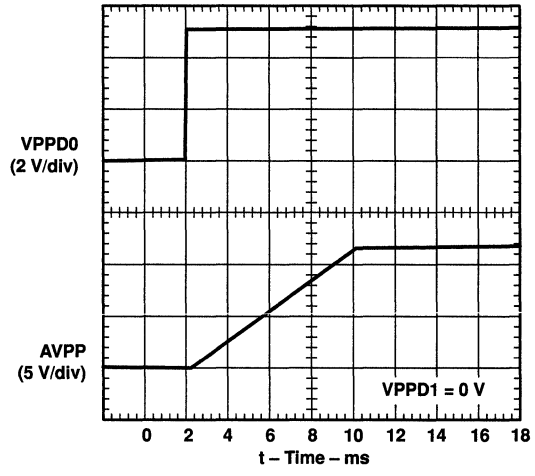


Figure 12. AVPP Propagation Delay and Rise Time With 150-μF Load, 12-V Switch

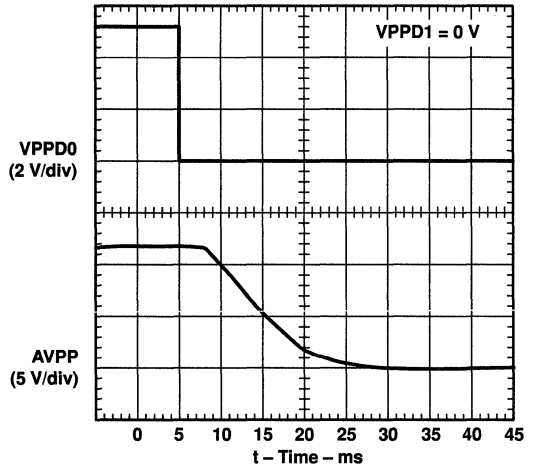


Figure 13. AVPP Propagation Delay and Fall Time With 150-μF Load, 12-V Switch

TYPICAL CHARACTERISTICS

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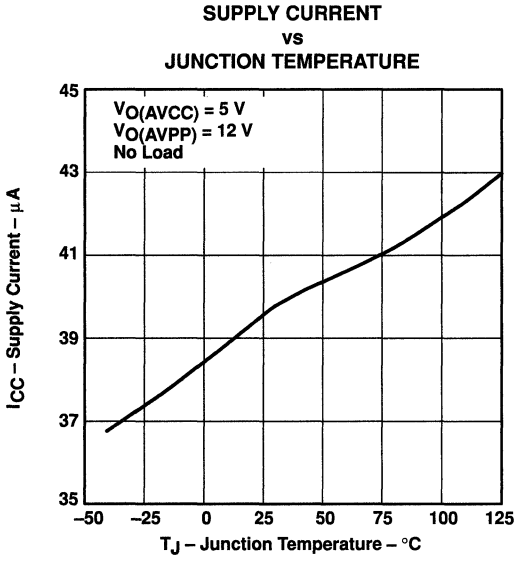


Figure 14

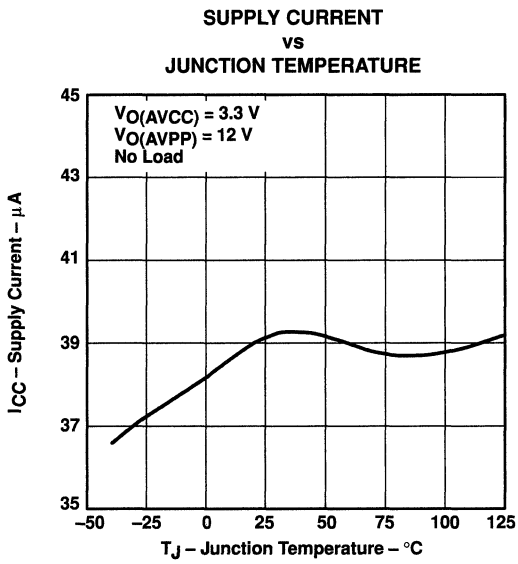


Figure 15

TYPICAL CHARACTERISTICS

5-V VCC SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

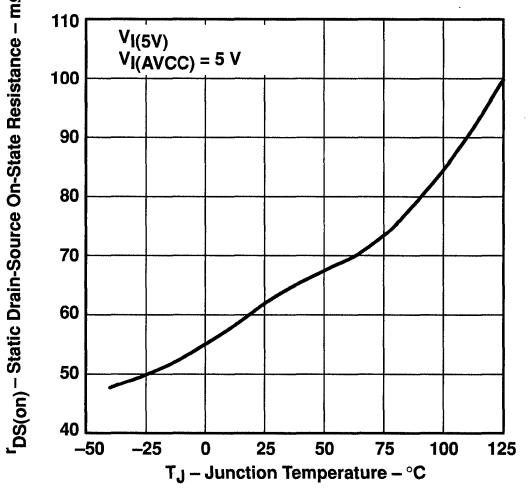


Figure 16

3.3-V VCC SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

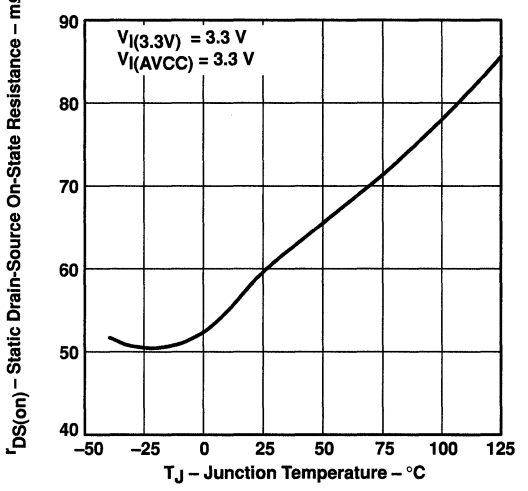


Figure 17

12-V VPP SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

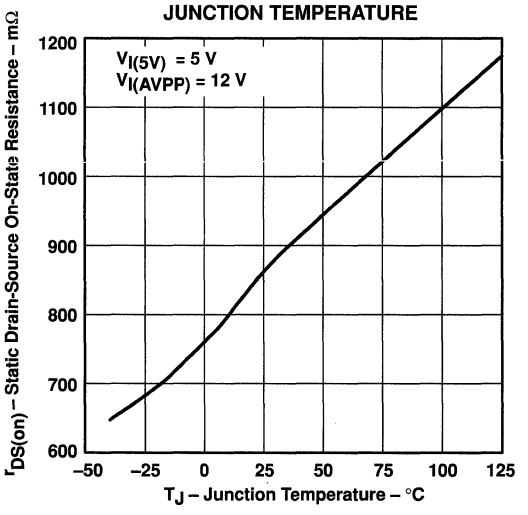


Figure 18

5-V VCC SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

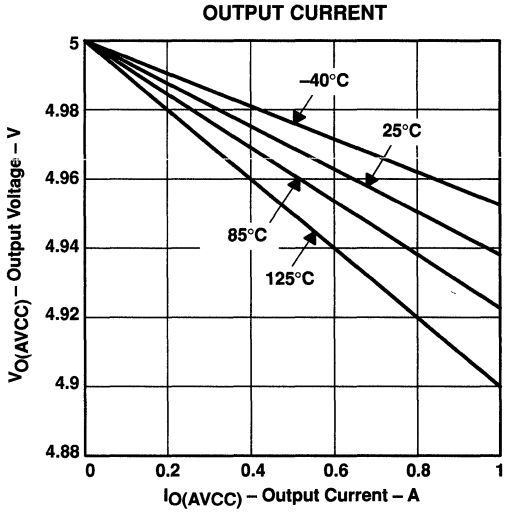


Figure 19

TYPICAL CHARACTERISTICS

3.3-V VCC SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

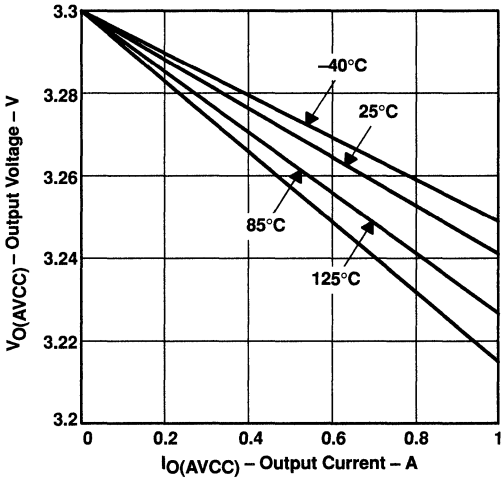


Figure 20

12-V VPP SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

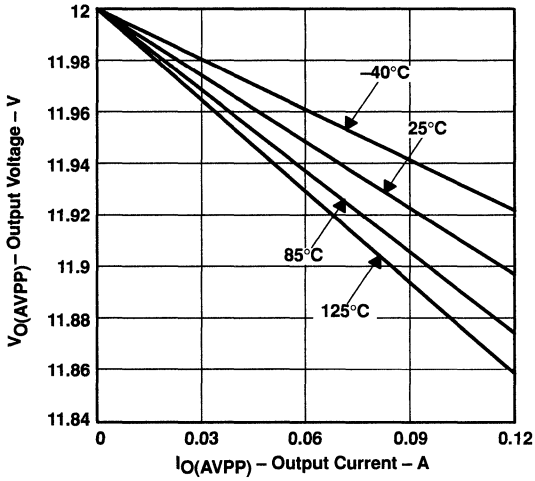


Figure 21

5-V VCC SWITCH
SHORT-CIRCUIT CURRENT
vs
JUNCTION TEMPERATURE

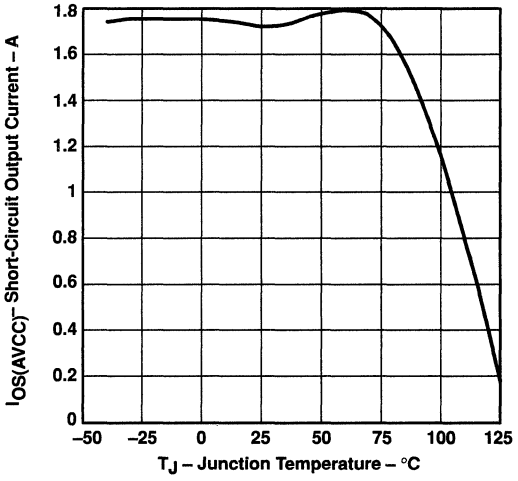


Figure 22

3.3-V VCC SWITCH
SHORT-CIRCUIT CURRENT
vs
JUNCTION TEMPERATURE

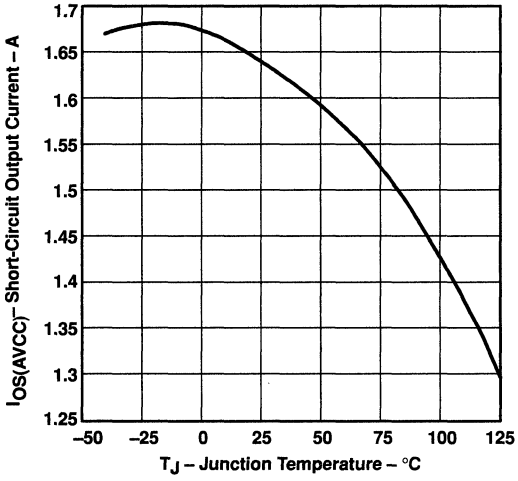


Figure 23

TYPICAL CHARACTERISTICS

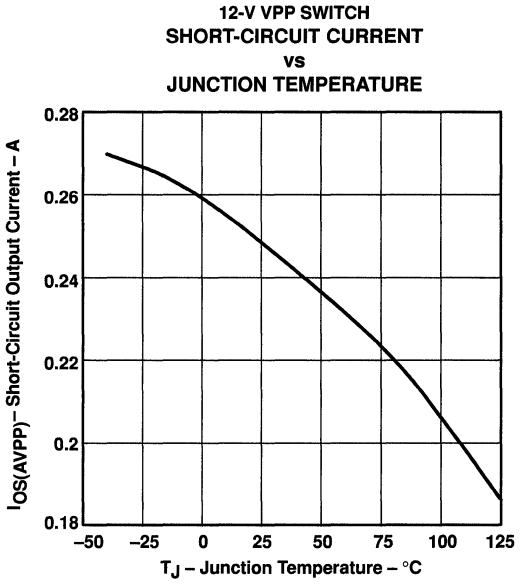


Figure 24

APPLICATION INFORMATION

overview

PC Cards were initially introduced as a means to add EEPROM (flash memory) to portable computers with limited onboard memory. The idea of add-in cards quickly took hold; modems, wireless LANs, GPS systems, multimedia, and hard-disk versions were soon available. As the number of PC Card applications grew, the engineering community quickly recognized the need for a standard to ensure compatibility across platforms. To this end, the PCMCIA (Personal Computer Memory Card International Association) was established, comprised of members from leading computer, software, PC Card, and semiconductor manufacturers. One key goal was to realize the *plug and play* concept, i.e. cards and hosts from different vendors should be compatible.

PC Card power specification

System compatibility also means power compatibility. The most current set of specifications (PC Card Standard) set forth by the PCMCIA committee states that power is to be transferred between the host and the card through eight of the 68 terminals of the PC Card connectors. This power interface consists of two V_{CC}, two V_{pp}, and four ground terminals. Multiple V_{CC} and ground terminals minimize connector-terminal and line resistance. The two V_{pp} terminals were originally specified as separate signals but are commonly tied together in the host to form a single node to minimize voltage losses. Card primary power is supplied through the V_{CC} terminals; flash-memory programming and erase voltage is supplied through the V_{pp} terminals.

APPLICATION INFORMATION

designing for voltage regulation

The current PCMCIA specification for output voltage regulation of the 5-V output is 5% (250 mV). In a typical PC power-system design, the power supply will have an output voltage regulation ($V_{PS(reg)}$) of 2% (100 mV). Also, a voltage drop from the power supply to the PC Card will result from resistive losses (V_{PCB}) in the PCB traces and the PCMCIA connector. A typical design would limit the total of these resistive losses to less than 1% (50 mV) of the output voltage. Therefore, the allowable voltage drop (V_{DS}) for the TPS2211 is the PCMCIA voltage regulation less the power supply regulation and less the PCB and connector resistive drops:

$$V_{DS} = V_{O(reg)} - V_{PS(reg)} - V_{PCB}$$

Typically, this would leave 100 mV for the allowable voltage drop across the TPS2211. The voltage drop is the output current multiplied by the switch resistance of the TPS2211. Therefore, the maximum output current that can be delivered to the PC Card in regulation is the allowable voltage drop across the TPS2211 divided by the output switch resistance.

$$I_O max = \frac{V_{DS}}{r_{DS(on)}}$$

The AVCC outputs deliver 1 A continuous at 5 V and 3.3 V within regulation over the operating temperature range. Using the same equations, the PCMCIA specification for output voltage regulation of the 3.3 V output is 300 mV. Using the voltage drop percentages for power supply regulation (2%) and PCB resistive loss (1%), the allowable voltage drop for the 3.3 V switch is 200 mV. The 12-V outputs (AVPP) of the TPS2211 can deliver 150 mA continuously.

overcurrent and overtemperature protection

PC Cards are inherently subject to damage from mishandling. Host systems require protection against short-circuited cards that could lead to power supply or PCB trace damage. Even systems sufficiently robust to withstand a short circuit would still undergo rapid battery discharge into the damaged PC Card, resulting in a sudden loss of system power. Most hosts include fuses for protection. The reliability of fused systems is poor and requires troubleshooting and repair, usually by the manufacturer, when fuses are blown.

The TPS2211 uses sense FETs to check for overcurrent conditions in each of the AVCC and AVPP outputs. Unlike sense resistors or polyfuses, these FETs do not add to the series resistance of the switch; therefore voltage and power losses are reduced. Overcurrent sensing is applied to each output separately. When an overcurrent condition is detected, only the power output affected is limited; all other power outputs continue to function normally. The $\overline{OC}$ indicator, normally a logic high, is a logic low when an overcurrent condition is detected providing for initiation of system diagnostics and/or sending a warning message to the user.

During power up, the TPS2211 controls the rise time of the AVCC and AVPP outputs and limits the current into a faulty card or connector. If a short circuit is applied after power is established (e.g., hot insertion of a bad card), current is initially limited only by the impedance between the short and the power supply. In extreme cases, as much as 10 A to 15 A may flow into the short before the current limiting of the TPS2211 engages. If the AVCC or AVPP outputs are driven below ground, the TPS2211 may latch nondestructively in an off state. Cycling power will reestablish normal operation.

Overcurrent limiting for the AVCC outputs is designed to activate if powered up into a short in the range of 1 A to 2.2 A, typically at about 1.6 A. The AVPP outputs limit from 120 mA to 400 mA, typically around 280 mA. The protection circuitry acts by linearly limiting the current passing through the switch rather than initiating a full shutdown of the supply. Shutdown occurs only during thermal limiting.

Thermal limiting prevents destruction of the IC from overheating if the package power dissipation ratings are exceeded. Thermal limiting disables power output until the device has cooled.

APPLICATION INFORMATION

12-V supply not required

Most PC Card switches use the externally supplied 12 V to power gate drive and other chip functions, which require that power be present at all times. The TPS2211 offers considerable power savings by using an internal charge pump to generate the required higher voltages from the 5-V input. Therefore, the external 12-V supply can be disabled except when needed for flash-memory functions, thereby extending battery lifetime. Do not ground the 12-V switch inputs when the 12-V input is not used. Additional power savings are realized by the TPS2211 during a software shutdown in which quiescent current drops to a maximum of 1 μA.

3.3-V low-voltage mode

The TPS2211 will operate in a 3.3-V low-voltage mode when 3.3 V is the only available input voltage ($V_{I(5V)} = 0$). This allows host and PC Cards to be operated in low-power 3.3-volts-only modes such as sleep or pager modes. Note that in these operation modes, the TPS2211 will derive its bias current from the 3.3-V input pin and only 3.3 V can be delivered to the PC Card.

voltage transitioning requirement

PC Cards are migrating from 5 V to 3.3 V to minimize power consumption, optimize board space, and increase logic speeds. The TPS2211 meets all combinations of power delivery as currently defined in the PCMCIA standard. The latest protocol accommodates mixed 3.3-V/5-V systems by first powering the card with 5 V, then polling it to determine its 3.3-V compatibility. The PCMCIA specification requires that the capacitors on 3.3-V compatible cards be discharged to below 0.8 V before applying 3.3-V power. This functions as a power reset and ensures that sensitive 3.3-V circuitry is not subjected to any residual 5-V charge. The TPS2211 offers a selectable V_{CC} and V_{pp} ground state, in accordance with PCMCIA 3.3-V/5-V switching specifications.

output ground switches

PC Card specification requires that V_{CC} be discharged within 100 ms. PC Card resistance can not be relied on to provide a discharge path for voltages stored on PC Card capacitance because of possible high-impedance isolation by power-management schemes.

power-supply considerations

The TPS2211 has multiple pins for each of its 3.3-V and 5-V power inputs and for the switched AVCC outputs. Any individual pin can conduct the rated input or output current. Unless all pins are connected in parallel, the series resistance is significantly higher than that specified, resulting in increased voltage drops and lost power. It is recommended that all input and output power pins be paralleled for optimum operation.

To increase the noise immunity of the TPS2211, the power supply inputs should be bypassed with a 1-μF electrolytic or tantalum capacitor paralleled by a 0.047-μF to 0.1-μF ceramic capacitor. It is strongly recommended that the switched outputs be bypassed with a 0.1-μF, or larger, ceramic capacitor; doing so improves the immunity of the TPS2211 to electrostatic discharge (ESD). Care should be taken to minimize the inductance of PCB traces between the TPS2211 and the load. High switching currents can produce large negative voltage transients, which forward biases substrate diodes, resulting in unpredictable performance. Similarly, no pin should be taken below –0.3 V.

APPLICATION INFORMATION

calculating junction temperature

The switch resistance, $r_{DS(on)}$, is dependent on the junction temperature, T_J, of the die and the current through the switch. To calculate T_J, first find $r_{DS(on)}$ from Figures 16 through 18 using an initial temperature estimate about 50°C above ambient. Then calculate the power dissipation for each switch, using the formula:

$$P_D = r_{DS(on)} \times I^2$$

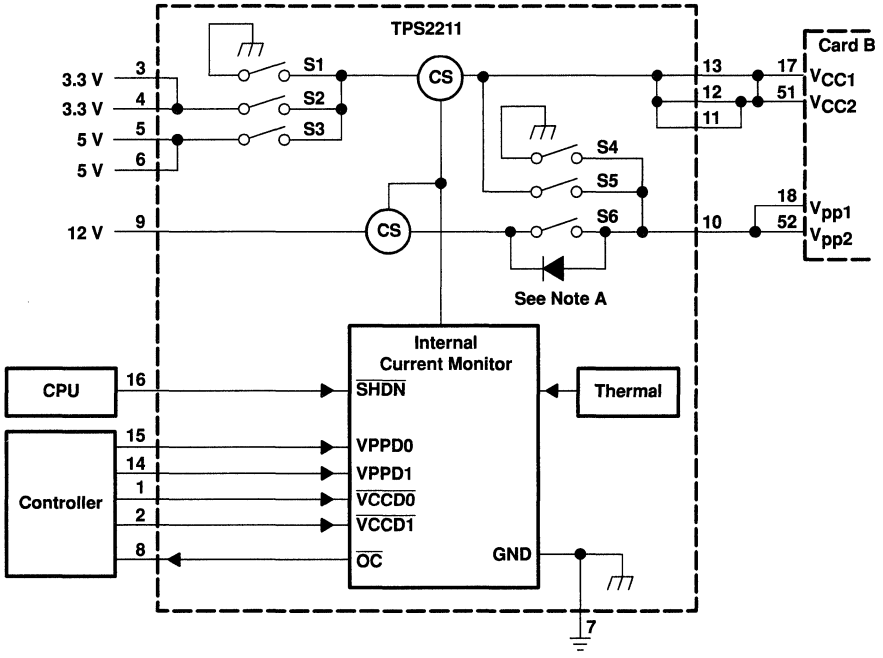
Next, sum the power dissipation and calculate the junction temperature:

$$T_J = \left(\sum P_D \times R_{\theta JA}\right) + T_A,\ R_{\theta JA} = 108°C/W$$

Compare the calculated junction temperature with the initial temperature estimate. If the temperatures are not within a few degrees of each other, recalculate using the calculated temperature as the initial estimate.

ESD protection

All TPS2211 inputs and outputs incorporate ESD-protection circuitry designed to withstand a 2-kV human-body-model discharge as defined in MIL-STD-883C, Method 3015. The AVCC and AVPP outputs can be exposed to potentially higher discharges from the external environment through the PC Card connector. Bypassing the outputs with 0.1-µF capacitors protects the devices from discharges up to 10 kV.



NOTE A. MOSFET switch S6 has a back-gate diode from the source to the drain. Unused switch inputs should never be grounded.

Figure 25. Internal Switching Matrix, TPS2211 control logic

APPLICATION INFORMATION

TPS2211 control logic

AVPP

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
$\overline{SHDN}$	VPPD0	VPPD1	S4	S5	S6	AVPP
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	AVCC†
1	1	0	OPEN	OPEN	CLOSED	VPP (12 V)
1	1	1	OPEN	OPEN	OPEN	Hi-Z
0	X	X	OPEN	OPEN	OPEN	Hi-Z

† Output depends on AVCC

AVCC

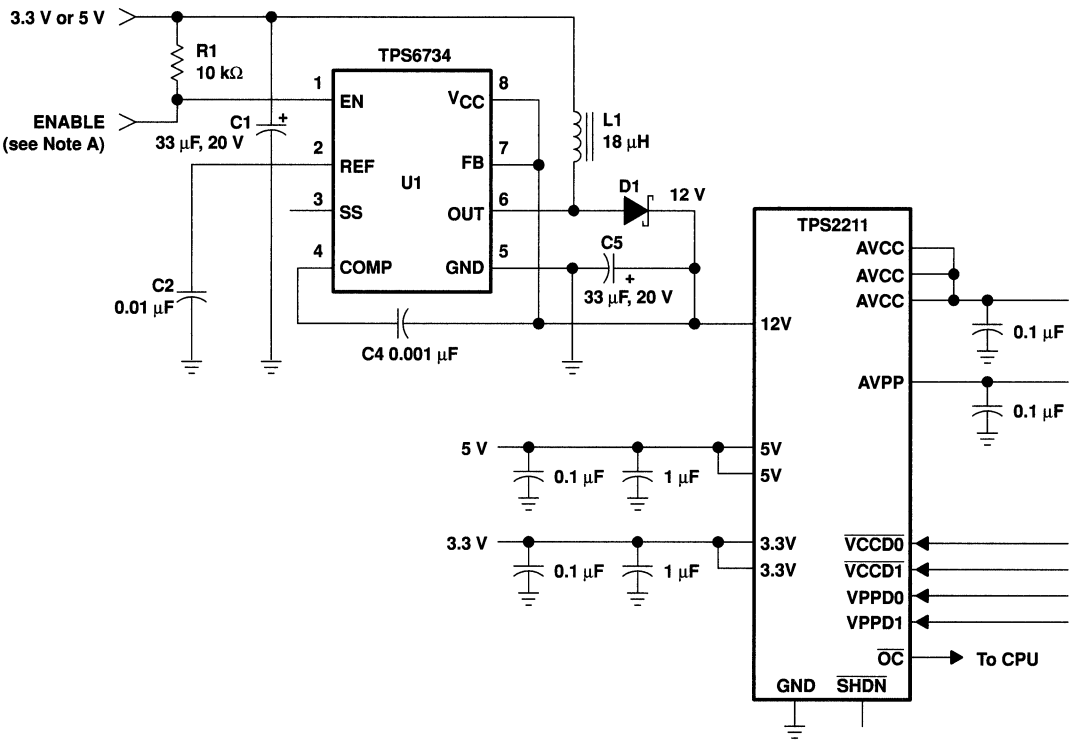
CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
$\overline{SHDN}$	$\overline{VCCD1}$	$\overline{VCCD0}$	S1	S2	S3	AVCC
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	3.3 V
1	1	0	OPEN	OPEN	CLOSED	5 V
1	1	1	CLOSED	OPEN	OPEN	0 V
0	X	X	OPEN	OPEN	OPEN	Hi-Z

12-V flash memory supply

The TPS6734 is a fixed 12-V output boost converter capable of delivering 120 mA from inputs as low as 2.7 V. The device is pin-for-pin compatible with the MAX734 regulator and offers the following advantages: lower supply current, wider operating input-voltage range, and higher output currents. As shown in Figure 1, the only external components required are: an inductor, a Schottky rectifier, an output filter capacitor, an input filter capacitor, and a small capacitor for loop compensation. The entire converter occupies less than 0.7 in^2 of PCB space when implemented with surface-mount components. An enable input is provided to shut the converter down and reduce the supply current to 3 μA when 12 V is not needed.

The TPS6734 is a 170-kHz current-mode PWM (pulse-width modulation) controller with an n-channel MOSFET power switch. Gate drive for the switch is derived from the 12-V output after start-up to minimize the die area needed to realize the 0.7-Ω MOSFET and improve efficiency at input voltages below 5 V. Soft start is accomplished with the addition of one small capacitor. A 1.22-V reference (pin 2) is brought out for external use. For additional information, see the TPS6734 data sheet (SLVS127).

APPLICATION INFORMATION

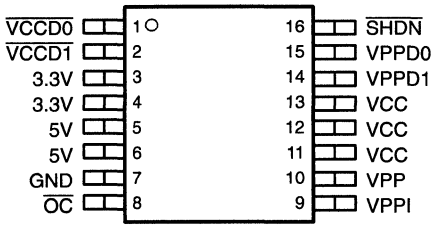


NOTE A. The enable terminal can be tied to a general-purpose I/O terminal on the PCMCIA controller or tied high.

Figure 26. TPS2211 with TPS6734 12-V, 120-mA Supply

- **Fully Integrated V_{CC} and V_{pp} Switching for Low Power Single-Slot PC Card™ Interface**
- **Low $r_{DS(on)}$ (160-mΩ V_{CC} Switches)**
- **Low Current Limit, 450 mA (V_{CC}) Typ**
- **3.3-V Low-Voltage Mode**
- **12-V Supply Can Be Disabled Except During 12-V Flash Programming**
- **Short-Circuit and Thermal Protection**
- **Space-Saving 16-Pin SSOP (DB)**
- **Compatible With 3.3-V, 5-V, and 12-V PC Cards**
- **Break-Before-Make Switching**
- **Typical Applications Include: PCMCIA PC Card Sockets in PDAs, PBXs, Bar Code Scanners, Compact Flash and Smart Cards**

DB PACKAGE
(TOP VIEW)



description

The TPS2212 PC Card power-interface switch provides an integrated power-management solution for a single low power PC Card. All of the discrete power MOSFETs, a logic section, current limiting, and thermal protection for PC Card control are combined on a single integrated circuit, using the Texas Instruments LinBiCMOS™ process. The circuit allows the distribution of 3.3-V, 5-V, and/or 12-V card power, and is compatible with many PCMCIA controllers. The current-limiting feature eliminates the need for fuses, which reduces component count and improves reliability. Current-limit reporting can help the user isolate a system fault to the PC Card.

The TPS2212 features a 3.3-V low-voltage mode that allows for 3.3-V switching without the need for 5 V. Bias power can be derived from either the 3.3-V or 5-V inputs. This facilitates low-power system designs such as sleep mode and pager mode, where only 3.3 V is available.

End equipment for the TPS2212 includes notebook computers, desktop computers, personal digital assistants (PDAs), digital cameras, and bar-code scanners. This device is well suited for those applications which need to limit the power provided to the PC card due to power supply constraints. In many applications, such as palm computers, the system cannot allocate more than 200 mA of current to a PC card slot. For these lower power applications, the TPS2212 provides the same advanced level of protection as the TPS2211 provides for higher power applications.

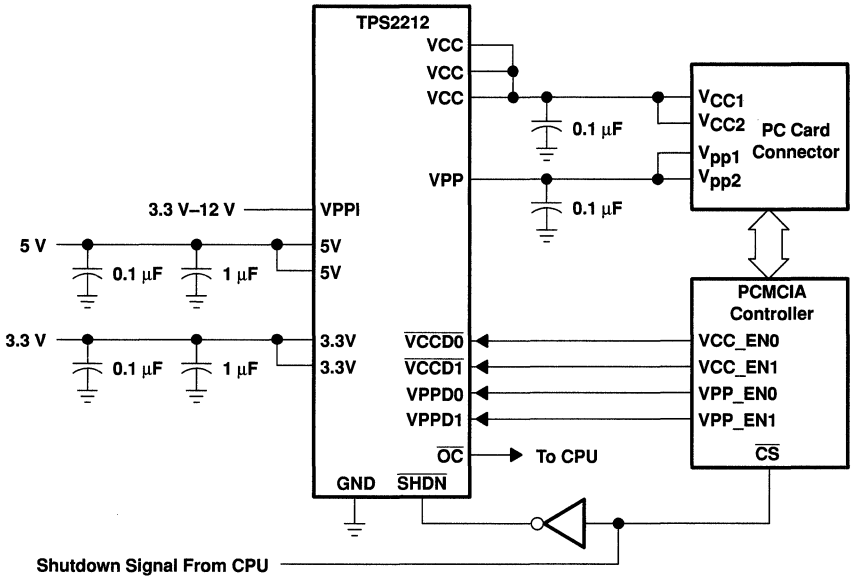
AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	SMALL OUTLINE (DB)
–40°C to 85°C	TPS2212IDBLE

The DB package is only available left-end taped and reeled (indicated by the LE suffix on the device type, e.g. TPS2212IDBLE).

PC Card is a trademark of PCMCIA (Personal Computer Memory Card International Association).
LinBiCMOS is a trademark of Texas Instruments Incorporated.

typical PC-card power-distribution application



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
3.3V	3, 4	I	3.3-V V_{CC} input for card power and/or chip power if 5 V is not present
5V	5, 6	I	5-V V_{CC} input for card power and/or chip power
VPPI	9	I	Main VPP input, typically 12 V, allows 3.3 V–12 V.
VCC	11, 12, 13	O	Switched output that delivers 0 V, 3.3-V, 5-V, or high impedance to card
VPP	10	O	Switched output that delivers 0 V 3.3-V, 5-V, VPPI (12V), or high impedance to card
GND	7		Ground
$\overline{OC}$	8	O	Logic-level overcurrent reporting output that goes low when an overcurrent conditions exists
$\overline{SHDN}$	16	I	Logic input that shuts down the TPS2212 and sets all power outputs to high-impedance state
$\overline{VCCD0}$	1	I	Logic input that controls voltage of VCC (see control-logic table)
$\overline{VCCD1}$	2	I	Logic input that controls voltage of VCC (see control-logic table)
VPPD0	15	I	Logic input that controls voltage of VPP (see control-logic table)
VPPD1	14	I	Logic input that controls voltage of VPP (see control-logic table)

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Input voltage range for card power: $V_{I(5V)}$ . . . . . –0.3 V to 7 V
$V_{I(3.3V)}$ . . . . . –0.3 V to 7 V
$V_{I(VPPI)}$ . . . . . –0.3 V to 14 V
Logic input voltage . . . . . –0.3 V to 7 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Output current (each card): $I_{O(VCC)}$ . . . . . internally limited
$I_{O(VPP)}$ . . . . . internally limited
Operating virtual junction temperature range, T_J . . . . . –40°C to 150°C
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –55°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DB	775 mW	6.2 mW/°C	496 mW	403 mW

These devices are mounted on an FR4 board with no special thermal considerations.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	$V_{I(5V)}$	0	5.25	V
	$V_{I(3.3V)}$	0	5.25	V
	$V_{I(VPPI)}$	0	13.5	V
Output Current	$I_{O(VCC)}$		250	mA
	$I_{O(VPP)}$		150	mA
Operating virtual junction temperature, T_J		–40	125	°C

electrical characteristics, T_A = –40°C to 85°C (unless otherwise noted)

power switch

PARAMETER			TEST CONDITIONS†	MIN	TYP	MAX	UNIT
	Switch resistance	5 V to VCC	$V_{I(5V)}$ = 5 V		160	210	mΩ
		3.3 V to VCC	$V_{I(5V)}$ = 5 V, $V_{I(3.3V)}$ = 3.3 V		160	210	
		3.3 V to VCC	$V_{I(5V)}$ = 0 V, $V_{I(3.3V)}$ = 3.3 V		160	210	
		5 V to VPP	T_J=25°C			6	Ω
		3.3 V to VPP	T_J=25°C			6	
		12 V to VPP	T_J=25°C			1	
$V_{O(VPP)}$	Clamp low voltage		I_{pp} at 10 mA			0.8	V
$V_{O(VCC)}$	Clamp low voltage		I_{CC} at 10 mA			0.8	V
I_{lkg}	Leakage current	I_{PP} high-impedance state	T_A = 25°C		1	10	µA
			T_A= 85°C			50	
		I_{CC} high-impedance state	T_A = 25°C		1	10	
			T_A=85°C			50	
I_I	Input current	$V_{I(5V)}$ = 5 V	$V_{O(VCC)}$ = 5 V, $V_{O(VPP)}$ = 12 V		40	150	µA
		$V_{I(5V)}$ = 0 V, $V_{I(3.3V)}$ = 3.3 V	$V_{O(VCC)}$ = 3.3 V, $V_{O(VPP)}$ = 12 V		40	150	
		Shutdown mode	$V_{O(VCC)}$ = $V_{O(VPP)}$ = Hi-Z			1	
I_{OS}	Short-circuit output-current limit	$I_{O(VCC)}$	T_J = 85°C, output powered into a short to GND	300		600	mA
		$I_{O(VPP)}$		120		400	mA

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

logic section

PARAMETER	TEST CONDITIONS†	MIN	MAX	UNIT
Logic input current			1	µA
Logic input high level		2		V
Logic input low level			0.8	V
Logic output high level	$V_{I(5V)}$ = 5 V, I_O = 1 mA	$V_{I(5V)}$ – 0.4		V
	$V_{I(5V)}$ = 0 V, I_O = 1 mA, $V_{I(3.3V)}$ = 3.3 V	$V_{I(3.3V)}$ – 0.4		
Logic output low level	I_O = 1 mA		0.4	V

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

switching characteristics‡

PARAMETER		TEST CONDITIONS§		MIN	TYP	MAX	UNIT
t_r	Rise times, output	$V_{O(VCC)}$			2.8		ms
		$V_{O(VPP)}$			6.4		
t_f	Fall times, output	$V_{O(VCC)}$			4.5		
		$V_{O(VPP)}$			12		
t_{pd}	Propagation delay (see Figure1)	$V_{I(VPPD0)}$ to $V_{O(VPP)}$	t_{on}		6.8		ms
			t_{off}		18		
		$V_{I(\overline{VCCD1})}$ to $V_{O(VCC)}$ (3.3V)	t_{on}		4		
			t_{off}		17		
		$V_{I(\overline{VCCD0})}$ to $V_{O(VCC)}$ (5V)	t_{on}		6.6		
			t_{off}		17		

‡ Switching Characteristics are with C_L = 150 µF.
§ Refer to Parameter Measurement Information

PARAMETER MEASUREMENT INFORMATION

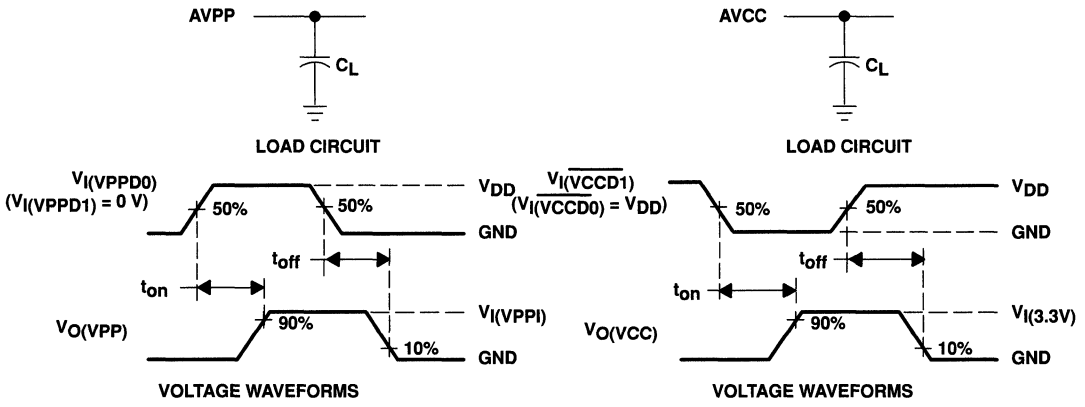


Figure 1. Test Circuits and Voltage Waveforms

Table of Timing Diagrams

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VCC Propagation Delay and Rise Time With 1-μF Load, 3.3-V Switch	2
VCC Propagation Delay and Fall Time With 1-μF Load, 3.3-V Switch	3
VCC Propagation Delay and Rise Time With 150-μF Load, 3.3-V Switch	4
VCC Propagation Delay and Fall Time With 150-μF Load, 3.3-V Switch	5
VCC Propagation Delay and Rise Time With 1-μF Load, 5-V Switch	6
VCC Propagation Delay and Fall Time With 1-μF Load, 5-V Switch	7
VCC Propagation Delay and Rise Time With 150-μF Load, 5-V Switch	8
VCC Propagation Delay and Fall Time With 150-μF Load, 5-V Switch	9
VPP Propagation Delay and Rise Time With 1-μF Load, 12-V Switch	10
VPP Propagation Delay and Fall Time With 1-μF Load, 12-V Switch	11
VPP Propagation Delay and Rise Time With 150-μF Load, 12-V Switch	12
VPP Propagation Delay and Fall Time With 150-μF Load, 12-V Switch	13

PARAMETER MEASUREMENT INFORMATION

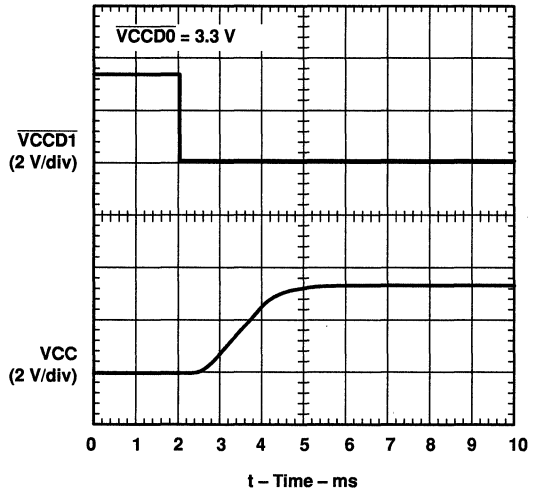


Figure 2. VCC Propagation Delay and Rise Time With 1-μF Load, 3.3-V Switch

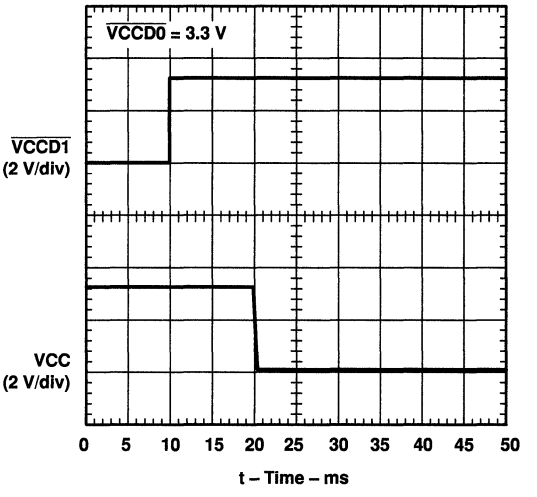


Figure 3. VCC Propagation Delay and Fall Time With 1-μF Load, 3.3-V Switch

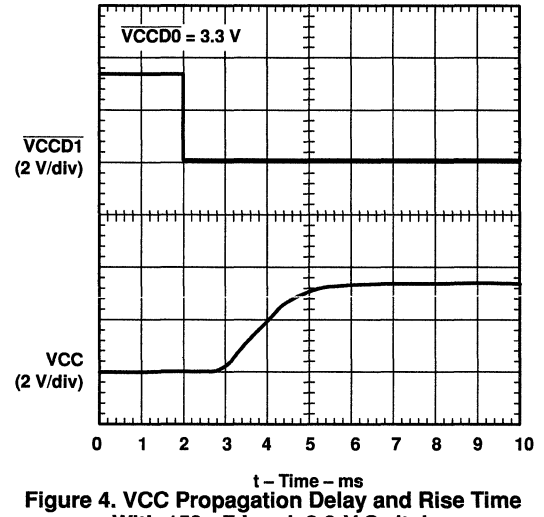


Figure 4. VCC Propagation Delay and Rise Time With 150-μF Load, 3.3-V Switch

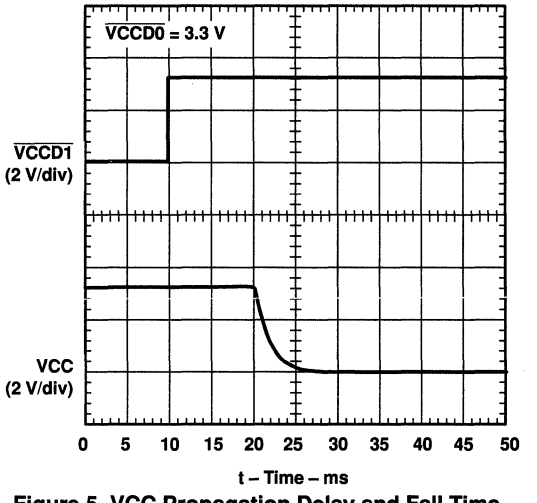


Figure 5. VCC Propagation Delay and Fall Time With 150-μF Load, 3.3-V Switch

PARAMETER MEASUREMENT INFORMATION

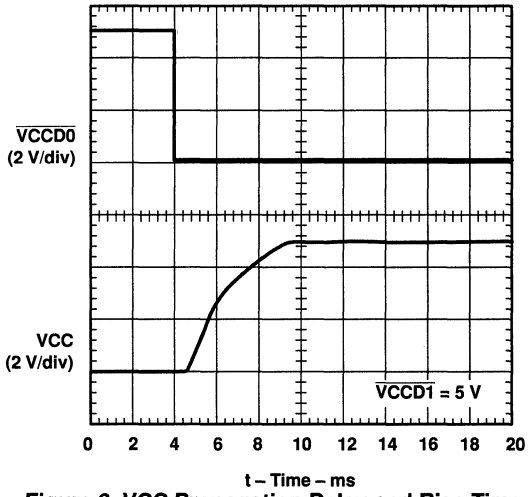


Figure 6. VCC Propagation Delay and Rise Time With 1-μF Load, 5-V Switch

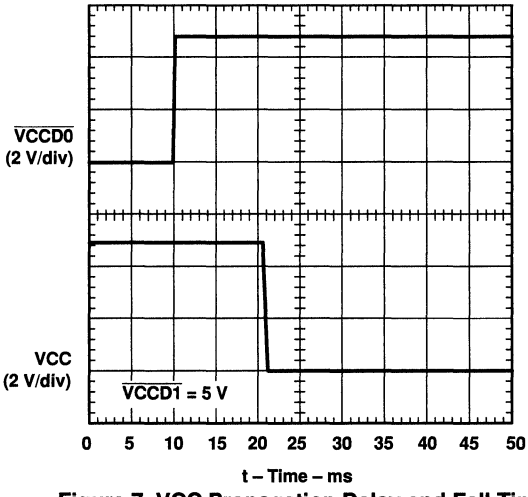


Figure 7. VCC Propagation Delay and Fall Time With 1-μF Load, 5-V Switch

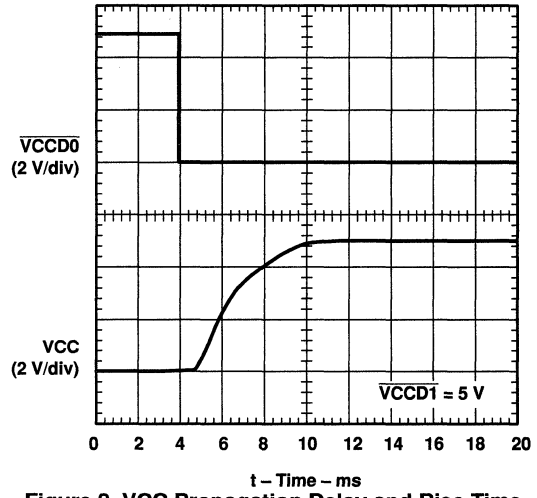


Figure 8. VCC Propagation Delay and Rise Time With 150-μF Load, 5-V Switch

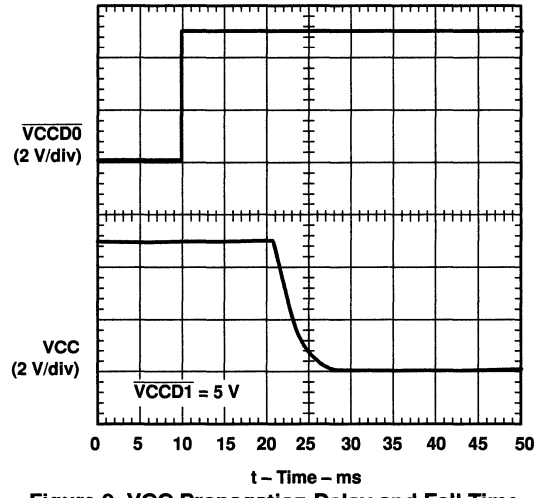


Figure 9. VCC Propagation Delay and Fall Time With 150-μF Load, 5-V Switch

PARAMETER MEASUREMENT INFORMATION

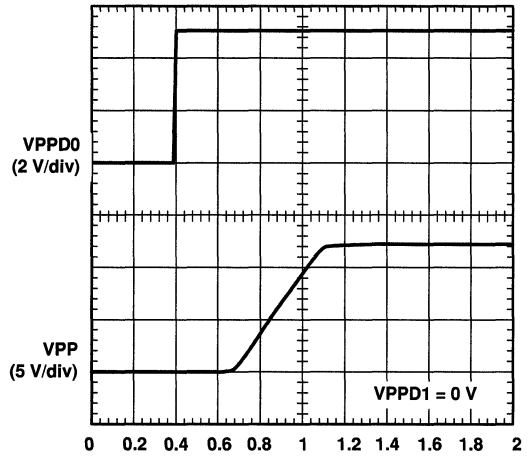


Figure 10. VPP Propagation Delay and Rise Time With 1-μF Load, 12-V Switch

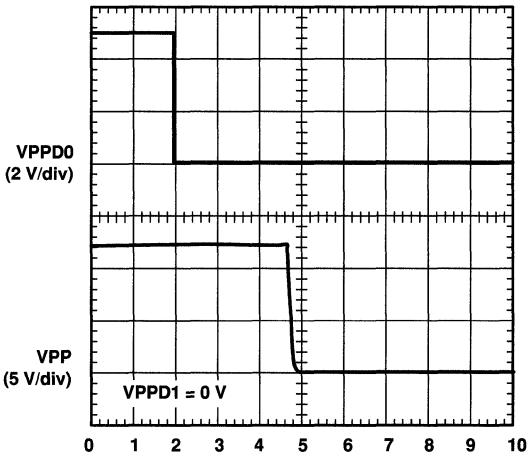


Figure 11. VPP Propagation Delay and Fall Time With 1-μF Load, 12-V Switch

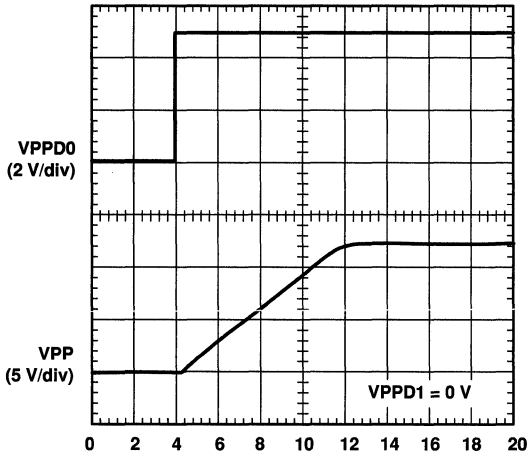


Figure 12. VPP Propagation Delay and Rise Time With 150-μF Load, 12-V Switch

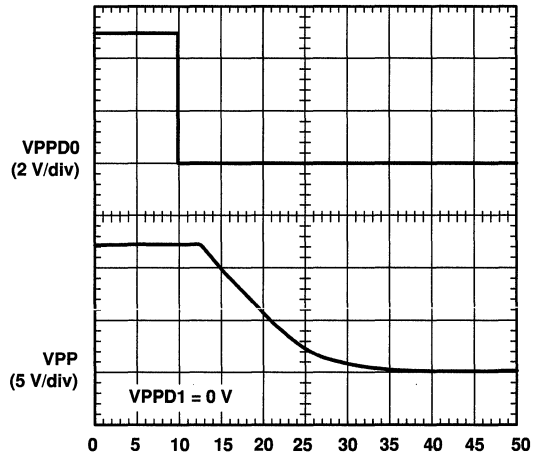


Figure 13. VPP Propagation Delay and Fall Time With 150-μF Load, 12-V Switch

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
$I_{CC(5V)}$	Supply current	vs Junction Temperature	14
$I_{CC(3.3V)}$	Supply current	vs Junction Temperature	15
$r_{DS(on)}$	Static drain-source on-state resistance, 5-V VCC switch	vs Junction Temperature	16
$r_{DS(on)}$	Static drain-source on-state resistance, 3.3-V VCC switch	vs Junction Temperature	17
$r_{DS(on)}$	Static drain-source on-state resistance, 12-V VPP switch	vs Junction Temperature	18
$V_{O(VCC)}$	Output voltage, 5-V VCC switch	vs Output current	19
$V_{O(VCC)}$	Output voltage, 3.3-V VCC switch	vs Output current	20
$V_{O(VPP)}$	Output voltage, 12-V VPP switch	vs Output current	21
$I_{OS(VCC)}$	Short-circuit current, 5-V VCC switch	vs Junction Temperature	22
$I_{OS(VCC)}$	Short-circuit current, 3.3-V VCC switch	vs Junction Temperature	23
$I_{OS(VPP)}$	Short-circuit current, 12-V VPP switch	vs Junction Temperature	24

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
JUNCTION TEMPERATURE

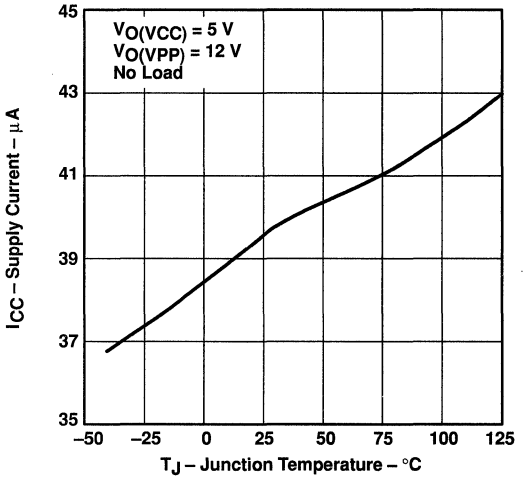


Figure 14

SUPPLY CURRENT
vs
JUNCTION TEMPERATURE

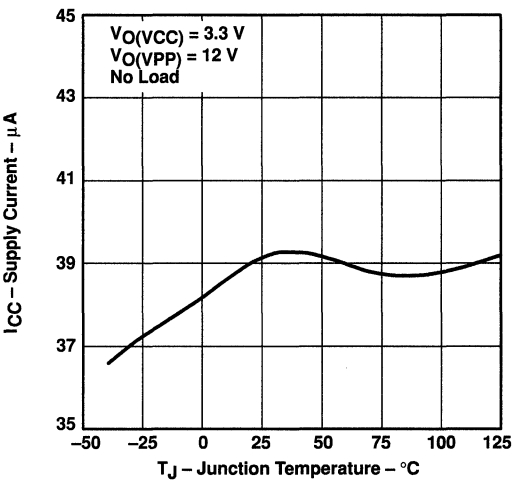


Figure 15

5–V VCC SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

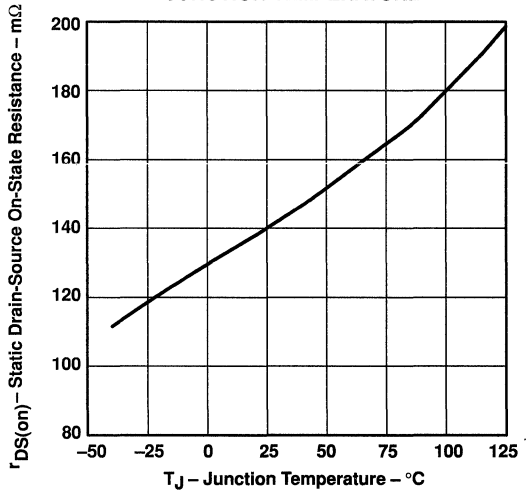


Figure 16

3.3–V VCC SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

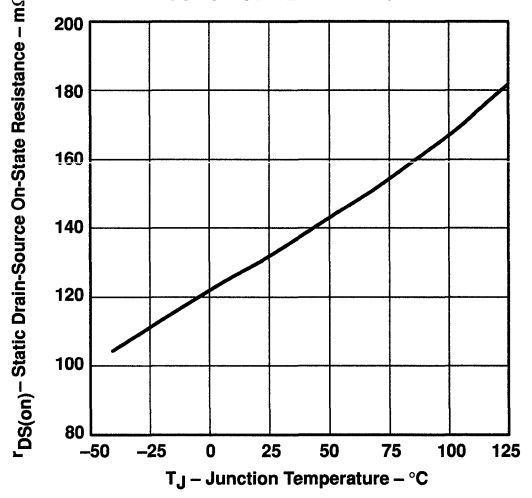


Figure 17

TYPICAL CHARACTERISTICS

12-V VPP SWITCH
STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

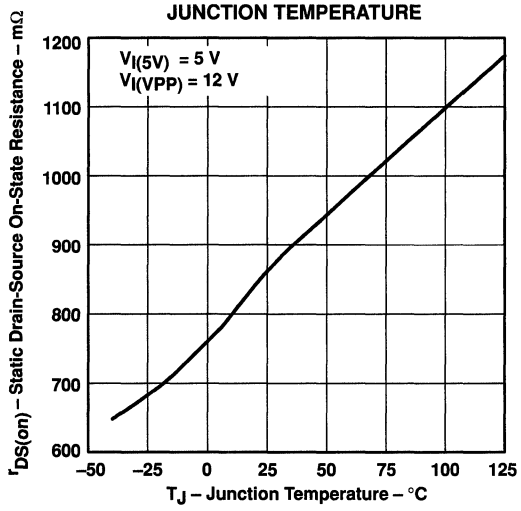


Figure 18

5-V VCC SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

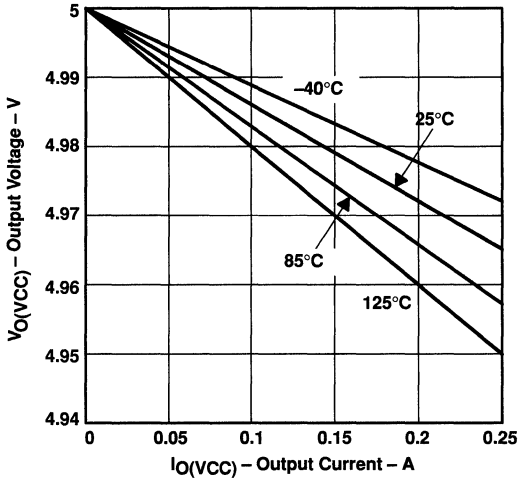


Figure 19

3.3-V VCC SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

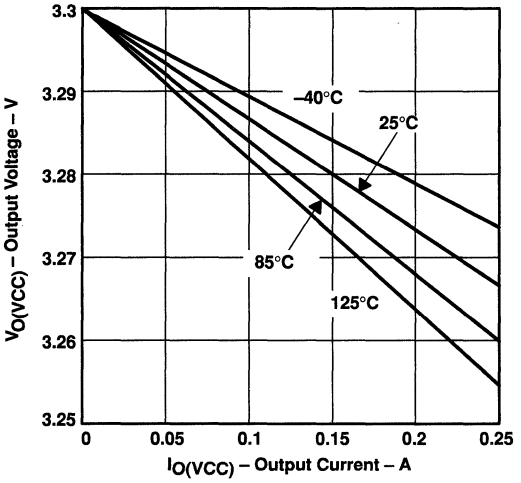


Figure 20

12-V VPP SWITCH
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

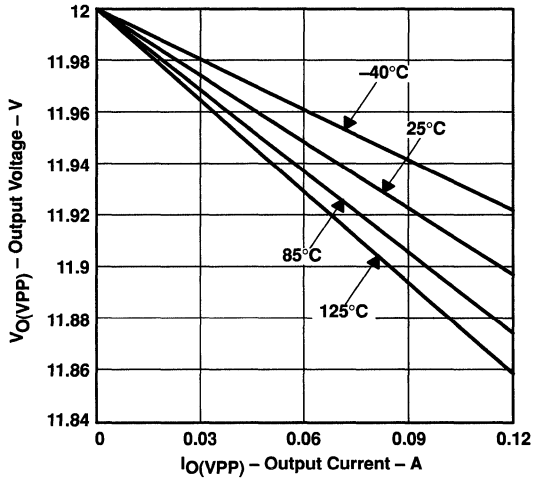


Figure 21

TYPICAL CHARACTERISTICS

5-V VCC SWITCH
SHORT-CIRCUIT CURRENT
vs
JUNCTION TEMPERATURE

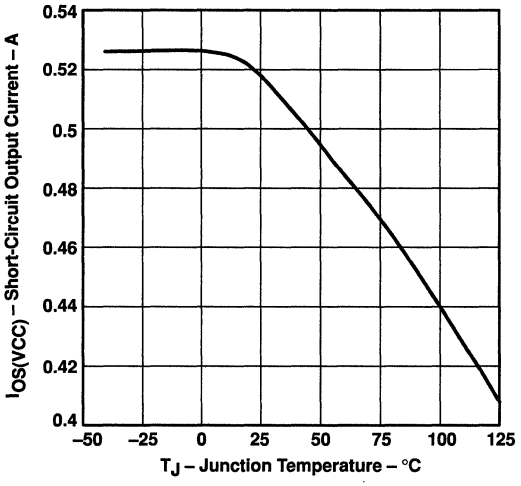


Figure 22

3.3-V VCC SWITCH
SHORT-CIRCUIT CURRENT
vs
JUNCTION TEMPERATURE

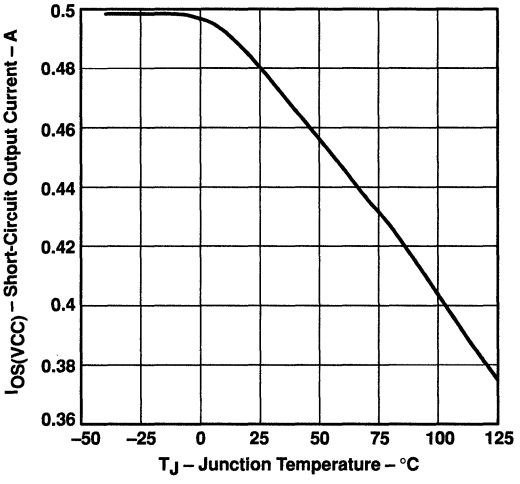


Figure 23

12-V VPP SWITCH
SHORT-CIRCUIT CURRENT
vs
JUNCTION TEMPERATURE

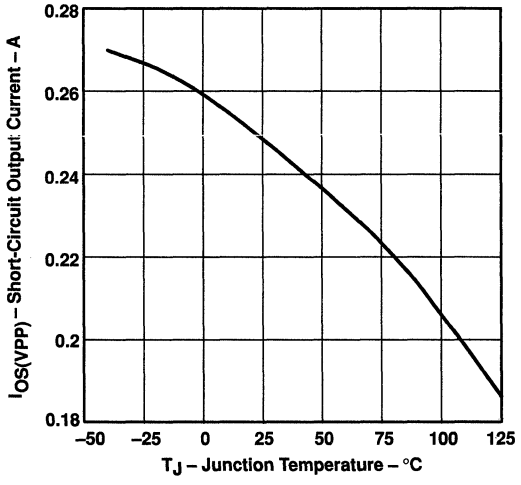


Figure 24

APPLICATION INFORMATION

overview

PC Cards were initially introduced as a means to add EEPROM (flash memory) to portable computers with limited on-board memory. The idea of add-in cards quickly took hold; modems, wireless LANs, GPS systems, multimedia, and hard-disk versions were soon available. As the number of PC Card applications grew, the engineering community quickly recognized the need for a standard to ensure compatibility across platforms. To this end, the PCMCIA (Personal Computer Memory Card International Association) was established, comprised of members from leading computer, software, PC Card, and semiconductor manufacturers. One key goal was to realize the *plug and play* concept, i.e. cards and hosts from different vendors should be compatible.

PC Card power specification

System compatibility also means power compatibility. The most current set of specifications (PC Card Standard) set forth by the PCMCIA committee states that power is to be transferred between the host and the card through eight of the 68 terminals of the PC Card connectors. This power interface consists of two VCC, two VPP, and four ground terminals. Multiple VCC and ground terminals minimize connector-terminal and line resistance. The two VPP terminals were originally specified as separate signals, but are commonly tied together in the host to form a single node to minimize voltage losses. Card primary power is supplied through the VCC terminals; flash-memory programming and erase voltage is supplied through the VPP terminals.

designing for voltage regulation

The current PCMCIA specification for output voltage regulation of the 5-V output is 5% (250 mV). In a typical PC power-system design, the power supply will have an output voltage regulation ($V_{PS(reg)}$) of 2% (100 mV). Also, a voltage drop from the power supply to the PC Card will result from resistive losses (V_{PCB}) in the PCB traces and the PCMCIA connector. A typical design would limit the total of these resistive losses to less than 1% (50 mV) of the output voltage. Therefore the allowable voltage drop (V_{DS}) for the TPS2212 is the PCMCIA voltage regulation less the power supply regulation and less the PCB and connector resistive drops:

$$V_{DS} = V_{O(reg)} - V_{PS(reg)} - V_{PCB}$$

Typically, this would leave 100 mV for the allowable voltage drop across the TPS2212. The voltage drop is the output current multiplied by the switch resistance of the TPS2212. Therefore, the maximum output current that can be delivered to the PC Card in regulation is the allowable voltage drop across the TPS2212 divided by the output switch resistance.

$$I_O max = \frac{V_{DS}}{r_{DS(on)}}$$

The VCC outputs deliver 250 mA continuous at 5 V and 3.3 V within regulation over the operating temperature range. Using the same equations, the PCMCIA specification for output voltage regulation of the 3.3 V output is 300 mV. Using the voltage drop percentages for power supply regulation (2%) and PCB resistive loss (1%), the allowable voltage drop for the 3.3 V switch is 200 mV. The 12-V outputs (VPP) of the TPS2212 can deliver 150 mA continuously.

APPLICATION INFORMATION

overcurrent and overtemperature protection

PC Cards are inherently subject to damage from mishandling. Host systems require protection against short-circuited cards that could lead to power supply or PCB trace damage. Even systems sufficiently robust to withstand a short circuit would still undergo rapid battery discharge into the damaged PC Card, resulting in a sudden loss of system power. Most hosts include fuses for protection. The reliability of fused systems is poor and requires troubleshooting and repair, usually by the manufacturer, when fuses are blown.

The TPS2212 uses sense FETs to check for overcurrent conditions in each of the VCC and VPP outputs. Unlike sense resistors or polyfuses, these FETs do not add to the series resistance of the switch; therefore voltage and power losses are reduced. Overcurrent sensing is applied to each output separately. When an overcurrent condition is detected, only the power output affected is limited; all other power outputs continue to function normally. The $\overline{OC}$ indicator, normally a logic high, is a logic low when an overcurrent condition is detected providing for initiation of system diagnostics and/or sending a warning message to the user.

During power up, the TPS2212 controls the rise time of the VCC and VPP outputs and limits the current into a faulty card or connector. If a short circuit is applied after power is established (e.g., hot insertion of a bad card), current is initially limited only by the impedance between the short and the power supply. In extreme cases, as much as 5 A to 10 A may flow into the short before the current limiting of the TPS2212 engages. If the VCC or VPP outputs are driven below ground, the TPS2212 may latch nondestructively in an off state. Cycling power will reestablish normal operation.

Overcurrent limiting for the VCC outputs is designed to activate if powered up into a short in the range of 300 mA to 600 mA, typically at about 450 mA. The VPP outputs limit from 120 mA to 400 mA, typically around 280 mA. The protection circuitry acts by linearly limiting the current passing through the switch rather than initiating a full shutdown of the supply. Shutdown occurs only during thermal limiting.

Thermal limiting prevents destruction of the IC from overheating if the package power dissipation ratings are exceeded. Thermal limiting disables power output until the device has cooled.

12-V supply not required

Most PC Card switches use the externally supplied 12 V to power gate drive and other chip functions, which requires that power be present at all times. The TPS2212 offers considerable power savings by using an internal charge pump to generate the required higher voltages from the 5-V input. Therefore, the external 12-V supply can be disabled except when needed for flash-memory functions, thereby extending battery lifetime. Do not ground the $\overline{VPPI}$ switch input when the VPPI input is not used. Additional power savings are realized by the TPS2212 during a software shutdown in which quiescent current drops to a maximum of 1 μA.

3.3-V low-voltage mode

The TPS2212 will operate in a 3.3-V low-voltage mode when 3.3 V is the only available input voltage ($V_{I(5V)} = 0$). This allows host and PC Cards to be operated in low-power 3.3-volts-only modes such as sleep or pager modes. Note that in these operation modes, the TPS2212 will derive its bias current from the 3.3-V input pin and only 3.3 V can be delivered to the PC Card.

APPLICATION INFORMATION

voltage transitioning requirement

PC Cards are migrating from 5 V to 3.3 V to minimize power consumption, optimize board space, and increase logic speeds. The TPS2212 meets all combinations of power delivery as currently defined in the PCMCIA standard. The latest protocol accommodates mixed 3.3-V/5-V systems by first powering the card with 5 V, then polling it to determine its 3.3-V compatibility. The PCMCIA specification requires that the capacitors on 3.3-V compatible cards be discharged to below 0.8 V before applying 3.3-V power. This functions as a power reset and ensures that sensitive 3.3-V circuitry is not subjected to any residual 5-V charge. The TPS2212 offers a selectable VCC and VPP ground state, in accordance with PCMCIA 3.3-V/5-V switching specifications.

output ground switches

PC Card specification requires that V_{CC} be discharged within 100 ms. PC Card resistance can not be relied on to provide a discharge path for voltages stored on PC Card capacitance because of possible high-impedance isolation by power-management schemes.

power supply considerations

The TPS2212 has multiple pins for each of its 3.3-V and 5-V power inputs and for the switched VCC outputs. Any individual pin can conduct the rated input or output current. Unless all pins are connected in parallel, the series resistance is significantly higher than that specified, resulting in increased voltage drops and lost power. It is recommended that all input and output power pins be paralleled for optimum operation.

To increase the noise immunity of the TPS2212, the power supply inputs should be bypassed with a 1-µF electrolytic or tantalum capacitor paralleled by a 0.047-µF to 0.1-µF ceramic capacitor. It is strongly recommended that the switched outputs be bypassed with a 0.1-µF, or larger, ceramic capacitor; doing so improves the immunity of the TPS2212 to electrostatic discharge (ESD). Care should be taken to minimize the inductance of PCB traces between the TPS2212 and the load. High switching currents can produce large negative voltage transients, which forward biases substrate diodes, resulting in unpredictable performance. Similarly, no pin should be taken below –0.3 V.

calculating junction temperature

The switch resistance, $r_{DS(on)}$, is dependent on the junction temperature, T_J, of the die and the current through the switch. To calculate T_J, first find $r_{DS(on)}$ from Figures 16 through 18 using an initial temperature estimate about 50°C above ambient. Then calculate the power dissipation for each switch, using the formula:

$$P_D = r_{DS(on)} \times I^2$$

Next, sum the power dissipation and calculate the junction temperature:

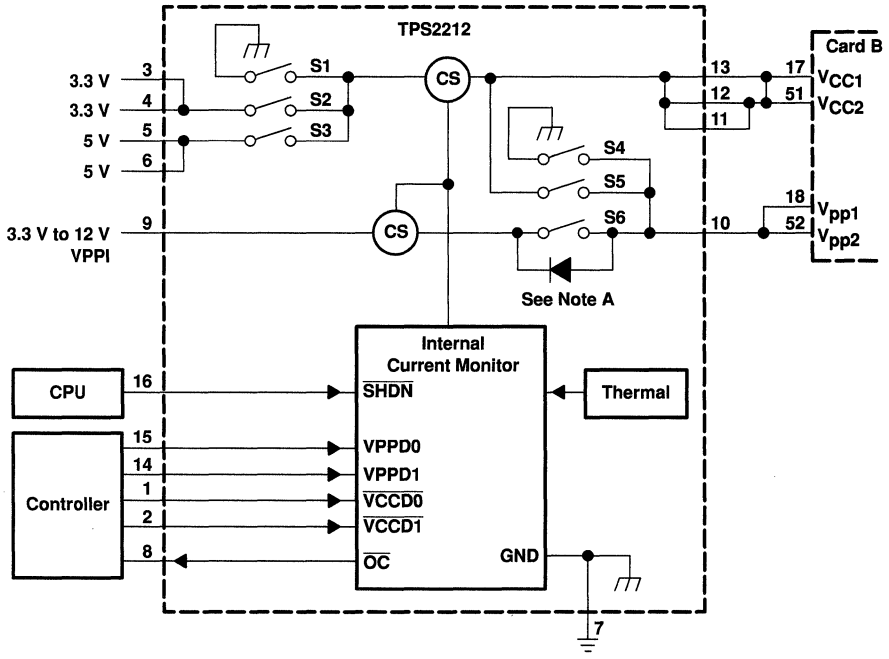
$$T_J = \left(\sum P_D \times R_{\theta JA}\right) + T_A,\ R_{\theta JA} = 108°C/W$$

Compare the calculated junction temperature with the initial temperature estimate. If the temperatures are not within a few degrees of each other, recalculate using the calculated temperature as the initial estimate.

APPLICATION INFORMATION

ESD protection

All TPS2212 inputs and outputs incorporate ESD-protection circuitry designed to withstand a 2-kV human-body-model discharge as defined in MIL-STD-883C, Method 3015. The VCC and VPP outputs can be exposed to potentially higher discharges from the external environment through the PC Card connector. Bypassing the outputs with 0.1-μF capacitors protects the devices from discharges up to 10 kV.



NOTE A. MOSFET switch S6 has a back-gate diode from the source to the drain. Unused switch inputs should never be grounded.

Figure 25. Internal Switching Matrix, TPS2212 Control Logic

APPLICATION INFORMATION

TPS2212 control logic

VPP

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
$\overline{SHDN}$	VPPD0	VPPD1	S4	S5	S6	VPP
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	VCC†
1	1	0	OPEN	OPEN	CLOSED	VPPI
1	1	1	OPEN	OPEN	OPEN	Hi-Z
0	X	X	OPEN	OPEN	OPEN	Hi-Z

† Output depends on AVCC

VCC

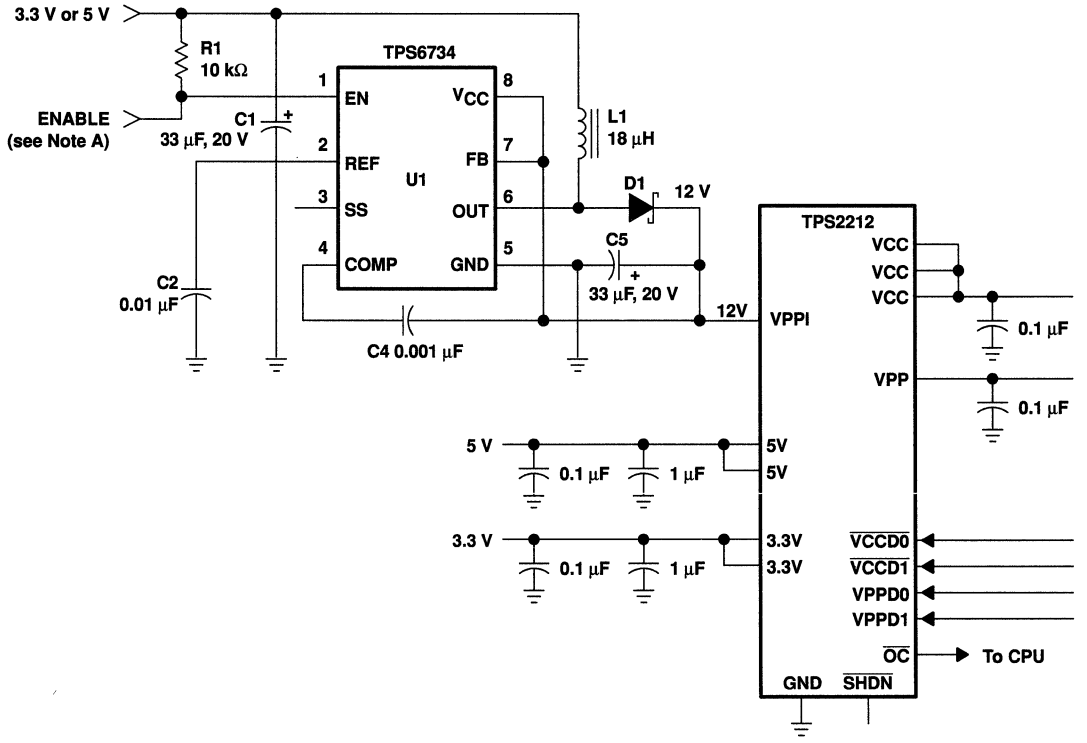
CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
$\overline{SHDN}$	$\overline{VCCD1}$	$\overline{VCCD0}$	S1	S2	S3	VCC
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	3.3 V
1	1	0	OPEN	OPEN	CLOSED	5 V
1	1	1	CLOSED	OPEN	OPEN	0 V
0	X	X	OPEN	OPEN	OPEN	Hi-Z

APPLICATION INFORMATION

12-V flash memory supply

The TPS6734 is a fixed 12-V output boost converter capable of delivering 120 mA from inputs as low as 2.7 V. The device is pin-for-pin compatible with the MAX734 regulator and offers the following advantages: lower supply current, wider operating input-voltage range, and higher output currents. As shown in Figure 26, the only external components required are: an inductor, a Schottky rectifier, an output filter capacitor, an input filter capacitor, and a small capacitor for loop compensation. The entire converter occupies less than 0.7 in^2 of PCB space when implemented with surface-mount components. An enable input is provided to shut the converter down and reduce the supply current to 3 μA when 12 V is not needed.

The TPS6734 is a 170-kHz current-mode PWM (pulse-width modulation) controller with an n-channel MOSFET power switch. Gate drive for the switch is derived from the 12-V output after start-up to minimize the die area needed to realize the 0.7-Ω MOSFET and improve efficiency at input voltages below 5 V. Soft start is accomplished with the addition of one small capacitor. A 1.22-V reference (pin 2) is brought out for external use. For additional information, see the TPS6734 data sheet (SLVS127).

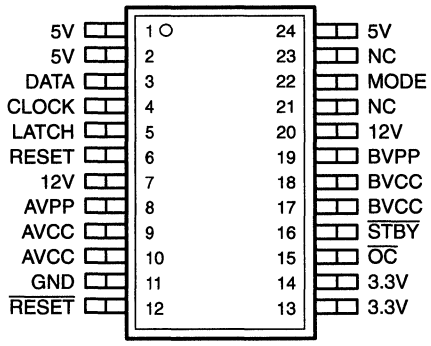


NOTE A. The enable terminal can be tied to a generall purpose I/O terminal on the PCMCIA controller or tied high.

Figure 26. TPS2212 with TPS6734 12-V, 120-mA Supply

- **Fully Integrated xVCC and xVPP Switching**
- **xVPP Programmed Independent of xVCC**
- **3.3-V, 5-V, and/or 12-V Power Distribution**
- **Low $r_{DS(on)}$ (60-mΩ xVCC Switch Typical)**
- **Short Circuit and Thermal Protection**
- **150-μA (Maximum) Quiescent Current**
- **Standby Mode: 50-mA Current Limit (Typ)**
- **12-V Supply Can Be Disabled**
- **3.3-V Low-Voltage Mode**
- **Meets PC Card™ Standards**
- **TTL-Logic Compatible Inputs**
- **Break-Before-Make Switching**
- **Internal Power-On Reset**

DB PACKAGE
(TOP VIEW)



† The TPS2214 is identical to the TPS2216 in all respects except packaging and pin assignments.
NC – No internal connection

description

The TPS2214 PC Card power-interface switch provides an integrated power-management solution for two PC Cards. All of the discrete power MOSFETs, a logic section, current limiting, and thermal protection for PC Card control are combined on a single integrated circuit. This device allows the distribution of 3.3-V, 5-V, and/or 12-V power to the card. The current-limiting feature eliminates the need for fuses. Current-limit reporting can help the user isolate a system fault.

The TPS2214 features a 3.3-V low-voltage mode that allows for 3.3-V switching without the need for 5-V power. This feature facilitates low-power system designs such as sleep modes where only 3.3 V is available. This device also has the ability to program the xVPP outputs independent of the xVCC outputs. A standby mode that changes all output-current limits to 50 mA (typical) has been incorporated.

End-equipment applications for the TPS2214 include: notebook computers, desktop computers, personal digital assistants (PDAs), digital cameras, and bar-code scanners.

AVAILABLE OPTIONS

T_J	PACKAGED DEVICES†
	PLASTIC SMALL OUTLINE (DB)
–40°C to 125°C	TPS2214DB(R)

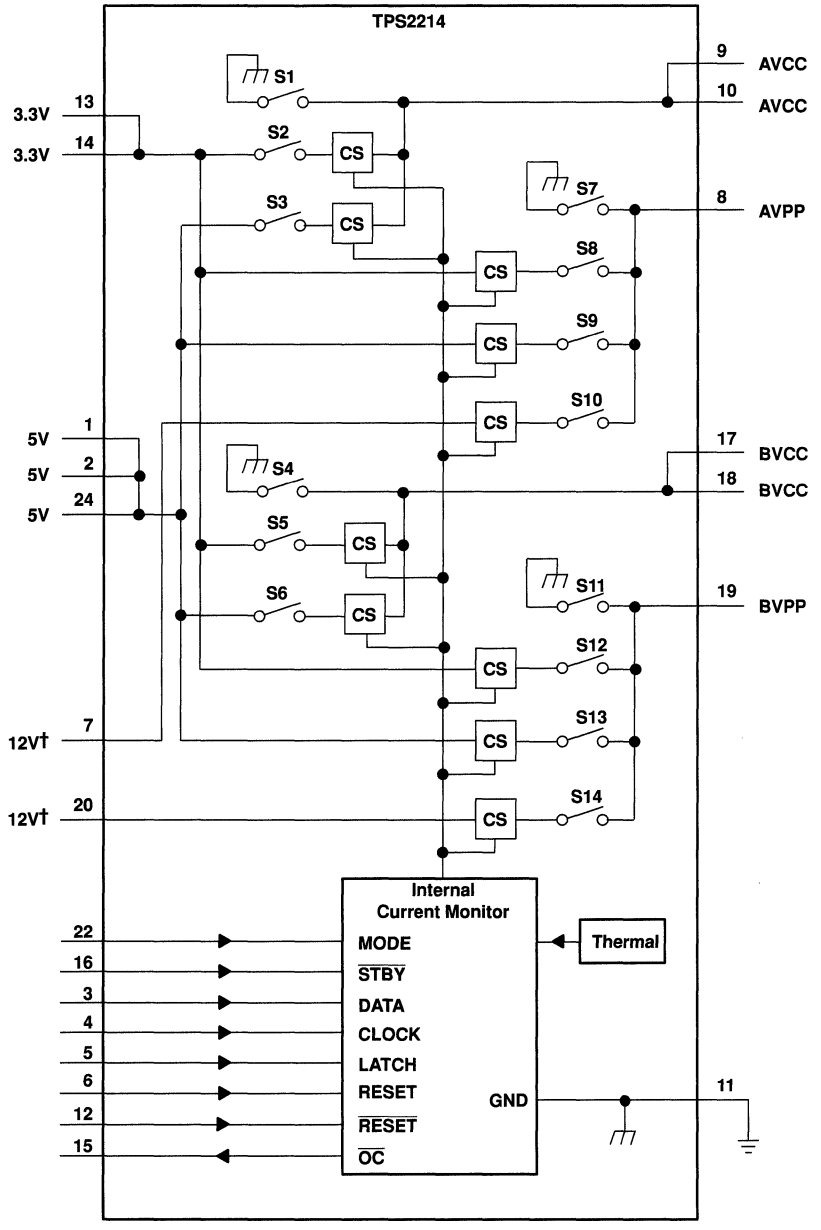
† The DB package is available in tubes and left-end taped and reeled. Add R suffix to device type (e.g., TPS2214DBR) for taped and reeled.

PC Card is a trademark of PCMCIA (Personal Computer Memory Card International Association).

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
3.3V	13,14	I	3.3-V input for card power and/or chip power if 5 V is not present
5V	1, 2, 24	I	5-V input for card power and/or chip power
12V	7, 20	I	12-V V_{pp} input card power
AVCC	9, 10	O	VCC output: 3.3-V, 5-V, GND or high impedance to card
AVPP	8	O	VPP output: 3.3-V, 5-V, 12-V, GND or high impedance to card
BVCC	17, 18	O	VCC output: 3.3-V, 5-V, GND or high impedance to card
BVPP	19	O	VPP output: 3.3-V, 5-V, 12-V, GND or high impedance to card
GND	11		Ground
MODE	22	I	TPS2206 operation when floating or pulled low; must be pulled high externally for TPS2214 operation. MODE is internally pulled low with a 150-kΩ pulldown resistor.
$\overline{OC}$	15	O	Logic-level output that goes low when an overcurrent or overtemperature condition exists.
RESET	6	I	Logic-level reset input active high. Do not connect if $\overline{RESET}$ pin is used. RESET is internally pulled low with a 150-kΩ pulldown resistor.
$\overline{RESET}$	12	I	Logic-level reset input active low. Do not connect if RESET pin is used. The pin is internally pulled high with a 150-kΩ pullup resistor.
$\overline{STBY}$	16	I	Logic-level active low input sets the TPS2214 to standby mode and sets all current limits to 50 mA. The pin is internally pulled high with a 150-kΩ pullup resistor.
CLOCK	4	I	Logic-level clock for serial data word
DATA	3	I	Logic-level serial data word
LATCH	5	I	Logic-level latch for serial data word
NC	21, 23		No internal connection

functional block diagram



† Both 12V pins must be connected together.

absolute maximum ratings over operating virtual free-air temperature (unless otherwise noted)†

Input voltage range for card power: $V_{I(3.3V)}$ ..... –0.3 V to 6 V
$V_{I(5V)}$ ..... –0.3 V to 6 V
$V_{I(12V)}$ ..... –0.3 V to 14 V
Logic input voltage ..... –0.3 V to 6 V
Output voltage range: $V_{O(xVCC)}$ ..... –0.3 V to 6 V
$V_{O(xVPP)}$ ..... –0.3 V to 14 V
Continuous total power dissipation ..... See Dissipation Rating Table
Output current: $I_{O(xVCC)}$ ..... Internally limited
$I_{O(xVPP)}$ ..... Internally limited
Operating virtual junction temperature range, T_J ..... –40°C to 125°C
Storage temperature range, T_{stg} ..... –55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DB	890 mW	8.90 mW/°C	489 mW	356 mW

‡ These devices are mounted on an JEDEC low-k board (2 oz. traces on surface), 1-W power applied.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	$V_{I(3.3V)}$	2.7	5.25	V
	$V_{I(5V)}$	2.7	5.25	V
	$V_{I(12V)}$	2.7	13.5	V
Output current, I_O	$I_{O(VCC)}$ at $T_A = 70°C$		1	A
	$I_{O(VPP)}$ at $T_A = 70°C$		200	mA
Clock frequency			2.5	MHz
Pulse duration	Data	200		ns
	Latch	250		
	Clock	100		
Data hold time§		100		ns
Data setup time§		100		ns
Latch delay time§		100		ns
Clock delay time§		250		ns
Operating virtual junction temperature, T_J		–40	125	°C

§ Refer to Figures 2 and 3.

electrical characteristics, T_J = 25°C, $V_{I(5V)}$ = 5 V, $V_{I(3.3V)}$ = 3.3 V, $V_{I(12V)}$ = 12 V, $\overline{STBY}$ floating, all outputs unloaded (unless otherwise noted)

power switch

PARAMETER			TEST CONDITIONS			MIN	TYP	MAX	UNIT
Switch resistance†	3.3 V to xVCC, with one switch on		T_J = 25°C,	I_O = 1 A			60	85	mΩ
			T_J = 125°C,	I_O = 1 A			90	120	
			T_J = 25°C,	$V_{I(5V)}$ = 0,	I_O = 1 A		65	85	
			T_J = 125°C,	$V_{I(5V)}$ = 0,	I_O = 1 A		90	130	
	5 V to xVCC, with one switch on		T_J = 25°C,	I_O = 1 A			60	85	
			T_J = 125°C,	I_O = 1 A			90	120	
	3.3 V to xVCC, with two switches on		T_J = 25°C,	I_O = 1 A each			65	105	
			T_J = 125°C,	I_O = 1 A each			95	140	
			T_J = 25°C,	$V_{I(5V)}$ = 0,	I_O = 1 A each		70	105	
			T_J = 125°C,	$V_{I(5V)}$ = 0,	I_O = 1 A each		100	140	
	5 V to xVCC, with two switches on		T_J = 25°C,	I_O = 1 A each			70	105	
			T_J = 125°C,	I_O = 1 A each			100	140	
	3.3 V/5 V/12 V to xVPP		T_J = 25°C,	I_O = 50 mA			0.7	1	Ω
			T_J = 125°C,	I_O = 50 mA			1.4	2.5	
	3.3 V/5 V to xVCC		T_J = 25°C,	$\overline{STBY}$ = low,	I_O = 30 mA		1.4	2	
			T_J = 125°C,	$\overline{STBY}$ = low,	I_O = 30 mA		2	3	
	3.3 V/5 V/12 V to xVPP		T_J = 25°C,	$\overline{STBY}$ = low,	I_O = 30 mA		5	7	
			T_J = 125°C,	$\overline{STBY}$ = low,	I_O = 30 mA		10	16	
Clamp low voltage	$V_{O(xVCC)}$		$I_{O(xVCC)}$ at 10 mA, After reset				0.275	0.8	V
	$V_{O(xVPP)}$		$I_{O(xVPP)}$ at 10 mA, After reset				0.275	0.8	
I_{lkg} Leakage current	$I_{O(xVCC)}$ High-impedance state		T_J = 25°C				1	10	µA
			T_J = 125°C				2	50	
	$I_{O(xVPP)}$ High-impedance state		T_J = 25°C				1	10	
			T_J = 125°C				2	50	
I_{OS} Short-circuit output current limit†	$I_{O(xVCC)}$		T_J = 85°C, output powered into a short to GND			1		2.2	A
	$I_{O(xVPP)}$					250		500	mA
	Standby mode $I_{O(xVCC)}$		T_J = 85°C, Output powered into a short to GND, $\overline{STBY}$ = 0 V			35	50	65	mA
	Standby mode $I_{O(xVPP)}$					30	50	60	
Current limit response time‡	xVCC switch		100-mΩ short circuit				100		µs
	xVPP switch						16		
I_I Input current§	Normal operation and in reset mode	$I_{I(3.3V)}$	$V_{O(xVCC)}$ = $V_{O(xVPP)}$ = 5 V				0.01	2	µA
		$I_{I(5V)}$					100	120	
		$I_{I(12V)}$					6	10	
		$I_{I(3.3V)}$	$V_{I(5V)}$ = 0, $V_{O(xVCC)}$ = 3.3 V, $V_{O(xVPP)}$ = 12 V				100	120	µA
		$I_{I(5V)}$					0		
		$I_{I(12V)}$					22	30	
	Shutdown mode	$I_{I(3.3V)}$	$V_{O(xVCC)}$ = Hi-Z, $V_{O(xVPP)}$ = Hi-Z					1	µA
		$I_{I(5V)}$						1	
		$I_{I(12V)}$						1	
Thermal shutdown‡	Trip point, T_J						155		°C
	Hysteresis						10		

† Pulse-testing techniques maintain junction temperature close to ambient temperature (250-µs-wide pulse, less than 0.5% duty cycle); thermal effects must be taken into account separately.
‡ Specified by design, not tested in production.
§ Input currents do not include logic input currents (presented in electrical characteristics for logic section); clock is inactive.
NOTE: $V_{I(3.3V)}$ or $V_{I(5V)}$ must be biased for switches to function.

logic section (CLOCK, DATA, LATCH, MODE, RESET, $\overline{\text{RESET}}$, $\overline{\text{STBY}}$, $\overline{\text{OC}}$)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic input current	$I_{I(RESET)}$ or $I_{I(\overline{RESET})}$†	$V_{I(RESET)}$ = 5 V or $V_{I(\overline{RESET})}$ = 0 V		30	50	μA
		$V_{I(RESET)}$ = 0 V or $V_{I(\overline{RESET})}$ = 5 V			1	
	$I_{I(MODE)}$†	$V_{I(MODE)}$ = 5 V		30	50	
		$V_{I(MODE)}$ = 0 V			1	
	$I_{I(\overline{STBY})}$†	$V_{I(\overline{STBY})}$ = 5 V			1	
		$V_{I(\overline{STBY})}$ = 0 V		30	50	
	$I_{I(CLOCK)}$ or $I_{I(DATA)}$ or $I_{I(LATCH)}$				1	
Logic input high level		$V_{I(5V)}$ = 5 V	2			V
		$V_{I(5V)}$ = 0 V	2			
Logic input low level					0.8	V
Logic output high level, $\overline{\text{OC}}$		$V_{I(5V)}$ = 5 V, I_O = 1 mA	$V_{I(5V)}$–0.4			V
		$V_{I(5V)}$ = 0 V, I_O = 1 mA	$V_{I(3.3V)}$–0.4			
Logic output low level, $\overline{\text{OC}}$		I_O = 1 mA			0.4	V

† RESET and MODE have internal 150-kΩ pulldown resistors; $\overline{\text{RESET}}$ and $\overline{\text{STBY}}$ have internal 150-kΩ pullup resistors.

switching characteristics

PARAMETER†		LOAD CONDITION†	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
t_r	Output rise times‡	$C_{L(xVCC)}$ = 0.1 µF, $C_{L(xVPP)}$ = 0.1 µF, $I_{O(xVCC)}$ = 0§, $I_{O(xVPP)}$ = 0§	$V_{O(xVCC)}$			1		ms
			$V_{O(xVPP)}$			0.8		
		$C_{L(xVCC)}$ = 150 µF, $C_{L(xVPP)}$ = 10 µF, $I_{O(xVCC)}$ = 1 A, $I_{O(xVPP)}$ = 50 mA	$V_{O(xVCC)}$			1.2		
			$V_{O(xVPP)}$			2.5		
t_f	Output fall times‡	$C_{L(xVCC)}$ = 0.1 µF, $C_{L(xVPP)}$ = 0.1 µF, $I_{O(xVCC)}$ = 0§, $I_{O(xVPP)}$ = 0§	$V_{O(xVCC)}$			0.01		ms
			$V_{O(xVPP)}$			0.01		
		$C_{L(xVCC)}$ = 150 µF, $C_{L(xVPP)}$ = 10 µF, $I_{O(xVCC)}$ = 1 A, $I_{O(xVPP)}$ = 50 mA	$V_{O(xVCC)}$			3		
			$V_{O(xVPP)}$			8		
t_{pd}	Propagation delay‡	$C_{L(xVCC)}$ = 0.1 µF, $C_{L(xVPP)}$ = 0.1 µF, $I_{O(xVCC)}$ = 0§, $I_{O(xVPP)}$ = 0§	Latch↑ to xVPP (12 V)	$t_{pd(on)}$		3		ms
				$t_{pd(off)}$		25		
			Latch↑ to xVPP (5 V)	$t_{pd(on)}$		0.6		
				$t_{pd(off)}$		8.5		
			Latch↑ to xVPP (3.3 V), $V_{I(5V)}$ = 5 V	$t_{pd(on)}$		0.6		
				$t_{pd(off)}$		9		
			Latch↑ to xVPP (3.3 V), $V_{I(5V)}$ = 0 V	$t_{pd(on)}$		1.4		
				$t_{pd(off)}$		9		
			Latch↑ to xVCC (5 V)	$t_{pd(on)}$		0.3		
				$t_{pd(off)}$		15		
			Latch↑ to xVCC (3.3 V), $V_{I(5V)}$ = 5 V	$t_{pd(on)}$		0.2		
				$t_{pd(off)}$		15		
			Latch↑ to xVCC (3.3 V), $V_{I(5V)}$ = 0 V	$t_{pd(on)}$		0.4		
				$t_{pd(off)}$		15		
		$C_{L(xVCC)}$ = 150 µF, $C_{L(xVPP)}$ = 10 µF, $I_{O(xVCC)}$ = 1 A, $I_{O(xVPP)}$ = 50 mA	Latch↑ to xVPP (12 V)	$t_{pd(on)}$		4.5		
				$t_{pd(off)}$		13		
			Latch↑ to xVPP (5 V)	$t_{pd(on)}$		3.3		
				$t_{pd(off)}$		8		
			Latch↑ to xVPP (3.3 V), $V_{I(5V)}$ = 5 V	$t_{pd(on)}$		3		
				$t_{pd(off)}$		9		
			Latch↑ to xVPP (3.3 V), $V_{I(5V)}$ = 0 V	$t_{pd(on)}$		3		
				$t_{pd(off)}$		9		
			Latch↑ to xVCC (5 V)	$t_{pd(on)}$		1		
				$t_{pd(off)}$		12		
			Latch↑ to xVCC (3.3 V), $V_{I(5V)}$ = 5 V	$t_{pd(on)}$		0.6		
				$t_{pd(off)}$		12		
			Latch↑ to xVCC (3.3 V), $V_{I(5V)}$ = 0 V	$t_{pd(on)}$		1		
				$t_{pd(off)}$		12		

† Refer to *Parameter Measurement Information*
‡ Specified by design: not tested in production.
§ No card inserted, assumes 0.1-µF recommended output capacitor (see Figure 34).

PARAMETER MEASUREMENT INFORMATION

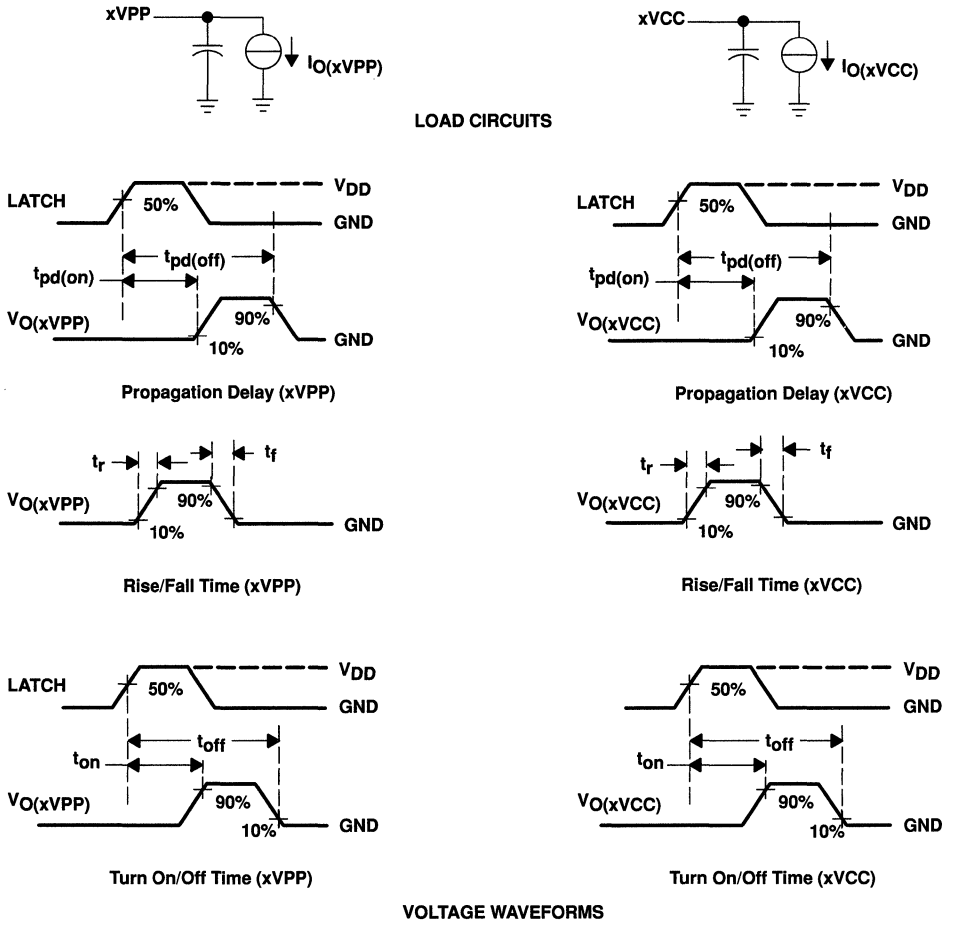
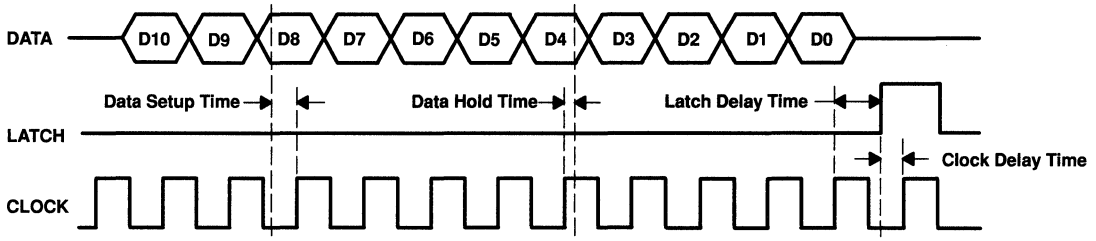


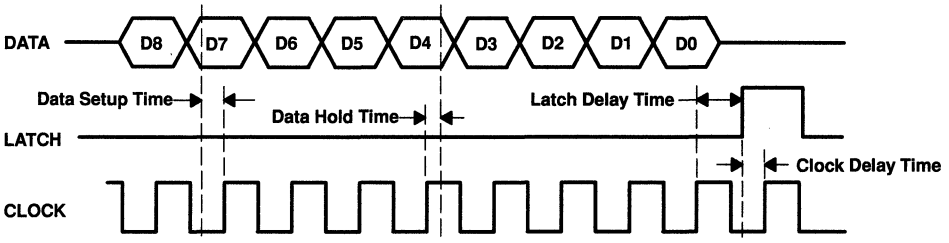
Figure 1. Test Circuits and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE: Data is clocked in on the positive edge of the clock. The positive edge of the latch signal should occur before the next positive edge of the clock. For definition of D0 to D10, see the control logic table.

Figure 2. Serial-Interface Timing for Independent xVPP Switching When MODE = 5 V or 3.3 V



NOTE: Data is clocked in on the positive edge of the clock. The positive edge of the latch signal should occur before the next positive edge of the clock. For definition of D0 to D8, see the control logic table.

Figure 3. Serial-Interface Timing When MODE = 0 V or Floating

Table of Timing Diagrams†

	FIGURE
Short-circuit current response, short applied to powered-on 5-V xVCC switch output	4
Short-circuit current response, short applied to powered-on 12-V xVPP switch output	5
$\overline{OC}$ response with ramped load on 5-V xVCC switch output	6
$\overline{OC}$ response with ramped load on 12-V xVPP switch output	7

† Timing tests are conducted at free-air temperature, $V_{I(5V)}$ = 5 V, $V_{I(3.3V)}$ = 3.3 V, $V_{I(12V)}$ = 12 V, C_L = 0.1 µF on each output, $\overline{STBY}$ floating.

PARAMETER MEASUREMENT INFORMATION

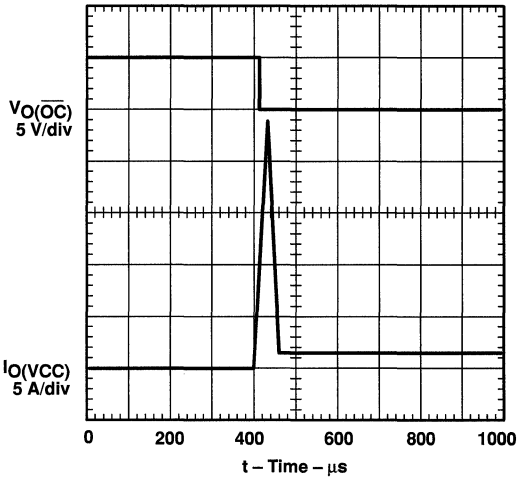


Figure 4. Short-Circuit Response, Short Applied to Powered-On 5-V xVCC-Switch Output

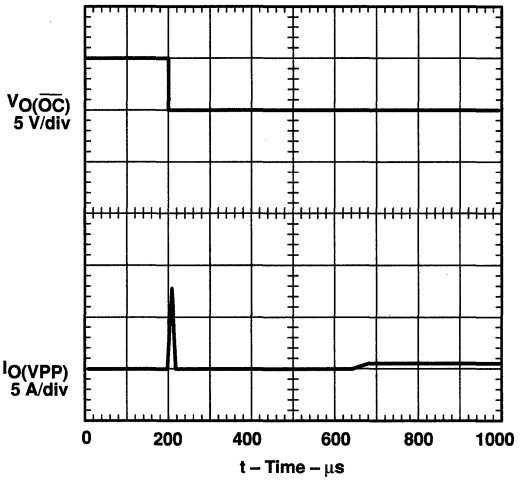


Figure 5. Short-Circuit Response, Short Applied to Powered-On 12-V xVPP-Switch Output

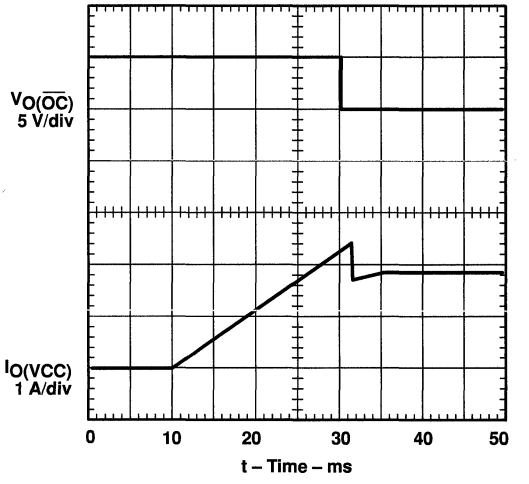


Figure 6. $\overline{OC}$ Response With Ramped Load on 5-V xVCC-Switch Output

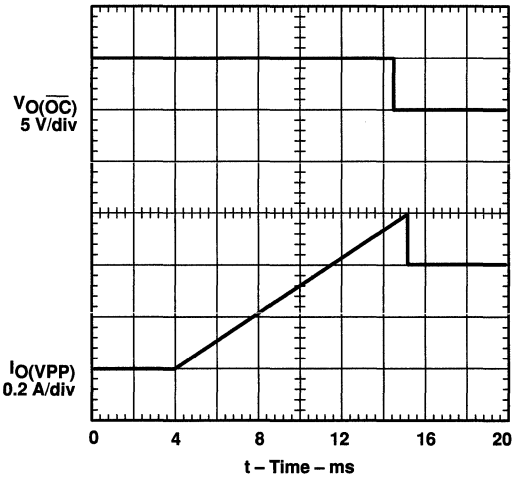


Figure 7. $\overline{OC}$ Response With Ramped Load on 12-V xVPP-Switch Output

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
$t_{pd(on)}$	Turnon propagation delay time, 3.3-V xVCC switch	vs Load capacitance	8
$t_{pd(off)}$	Turnoff propagation delay time, 3.3-V xVCC switch	vs Load capacitance	9
$t_{pd(on)}$	Turnon propagation delay time, 5-V xVCC switch	vs Load capacitance	10
$t_{pd(off)}$	Turnoff propagation delay time, 5-V xVCC switch	vs Load capacitance	11
$t_{pd(on)}$	Turnon propagation delay time, 12-V xVPP switch	vs Load capacitance	12
$t_{pd(off)}$	Turnoff propagation delay time, 12-V xVPP switch	vs Load capacitance	13
t_r	Rise time, 3.3-V xVCC switch	vs Load capacitance	14
t_f	Fall time, 3.3-V xVCC switch	vs Load capacitance	15
t_r	Rise time, 5-V xVCC switch	vs Load capacitance	16
t_f	Fall time, 5-V xVCC switch	vs Load capacitance	17
t_r	Rise time, 12-V xVPP switch	vs Load capacitance	18
t_f	Fall time, 12-V xVPP switch	vs Load capacitance	19
I_I	Input current at $V_{O(xVCC)} = V_{O(xVPP)}$ =3.3 V	vs Junction temperature	20
	Input current at $V_{O(xVCC)} = V_{O(xVPP)}$ =5 V	vs Junction temperature	21
	Input current at $V_{O(xVCC)}$ = 5 V, $V_{O(xVPP)}$ =12 V	vs Junction temperature	22
$r_{DS(on)}$	Static drain-source on-state resistance, 3.3-V xVCC switch ($V_{I(5V)}$=0)	vs Junction temperature	23
	Static drain-source on-state resistance, 3.3-V xVCC switch	vs Junction temperature	24
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$V_{IO(xVCC)}$	dc input-to-output voltage (drop), 3.3-V xVCC switch ($V_{I(5V)}$=0)	vs Load current	27
	dc input-to-output voltage (drop), 3.3-V xVCC switch	vs Load current	28
	dc input-to-output voltage (drop), 5-V xVCC switch	vs Load current	29
$V_{IO(xVPP)}$	dc input-to-output voltage (drop), 12-V xVPP switch	vs Load current	30
I_{OS}	Short-circuit current limit, 3.3-V xVCC switch	vs Junction temperature	31
	Short-circuit current limit, 5-V xVCC switch	vs Junction temperature	32
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NOTE: Electrical characteristics tests are conducted at $V_{I(5V)}$ = 5 V, $V_{I(3.3V)}$ = 3.3 V, $V_{I(12V)}$ = 12 V, C_L = 0.1 µF on each output, $\overline{STBY}$ floating (unless otherwise noted on Figures).

TYPICAL CHARACTERISTICS

TURNON PROPAGATION DELAY TIME,
3.3-V xVCC SWITCH
vs
LOAD CAPACITANCE

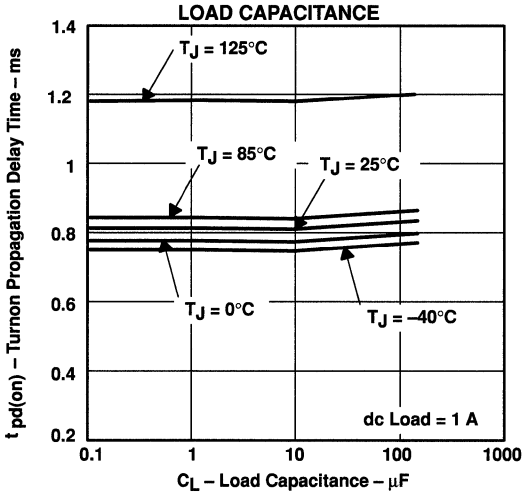


Figure 8

TURNOFF PROPAGATION DELAY TIME,
3.3-V xVCC SWITCH
vs
LOAD CAPACITANCE

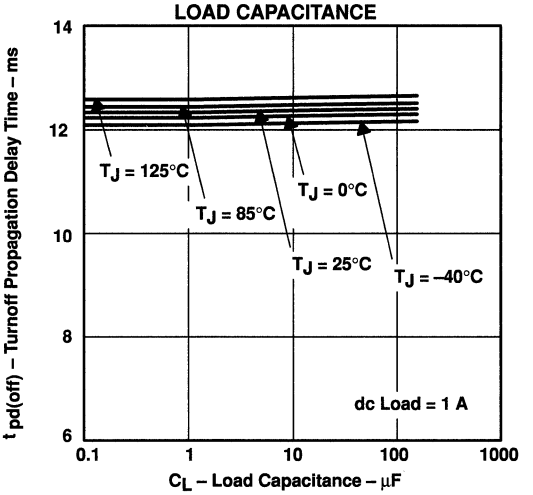


Figure 9

TURNON PROPAGATION DELAY TIME,
5-V xVCC SWITCH
vs
LOAD CAPACITANCE

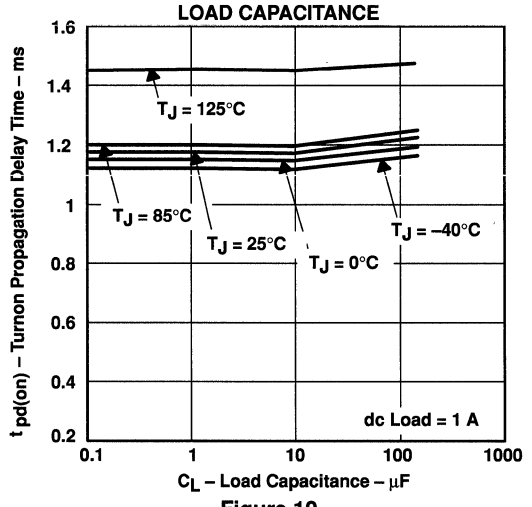


Figure 10

TURNOFF PROPAGATION DELAY TIME,
5-V xVCC SWITCH
vs
LOAD CAPACITANCE

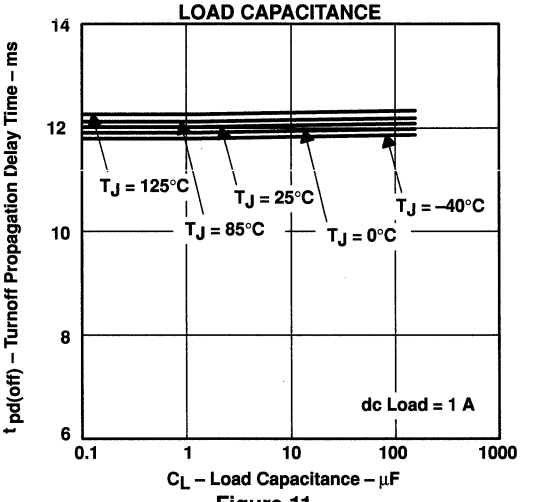


Figure 11

TYPICAL CHARACTERISTICS

TURNON PROPAGATION DELAY TIME,
12-V xVPP SWITCH
vs
LOAD CAPACITANCE

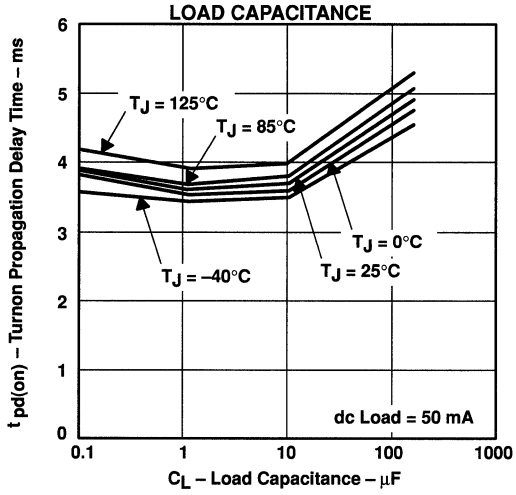


Figure 12

TURNOFF PROPAGATION DELAY TIME dc,
12-V xVPP SWITCH
vs
LOAD CAPACITANCE

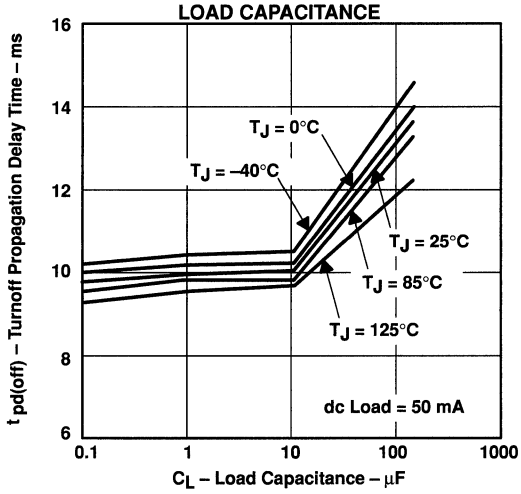


Figure 13

RISE TIME, 3.3-V xVCC SWITCH
vs
LOAD CAPACITANCE

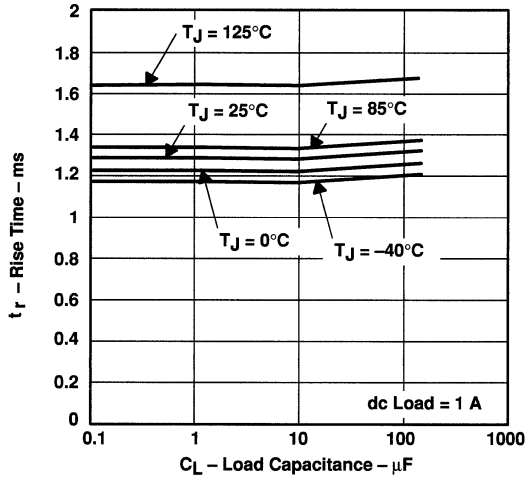


Figure 14

FALL TIME, 3.3-V xVCC SWITCH
vs
LOAD CAPACITANCE

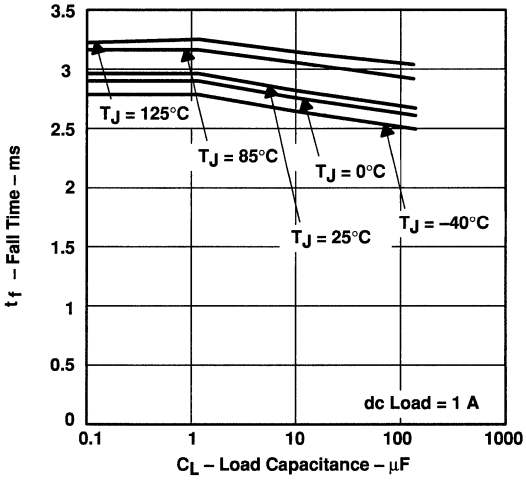


Figure 15

TYPICAL CHARACTERISTICS

RISE TIME, 5-V xVCC SWITCH
vs
LOAD CAPACITANCE

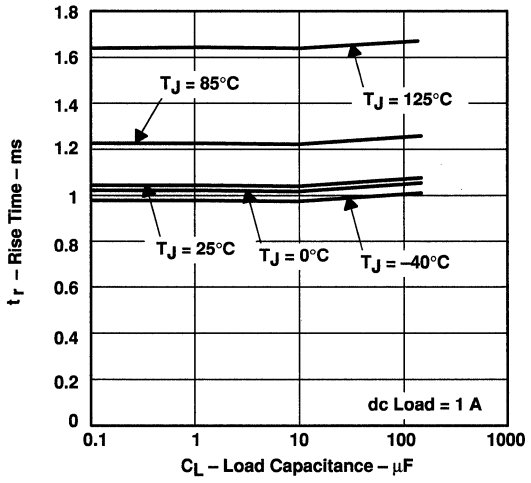


Figure 16

FALL TIME, 5-V xVCC SWITCH
vs
LOAD CAPACITANCE

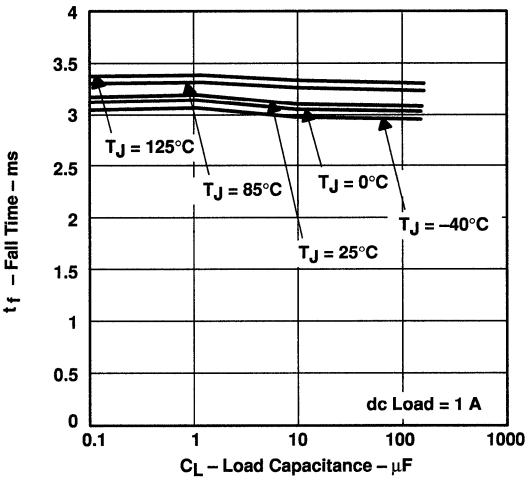


Figure 17

RISE TIME, 12-V xVPP SWITCH
vs
LOAD CAPACITANCE

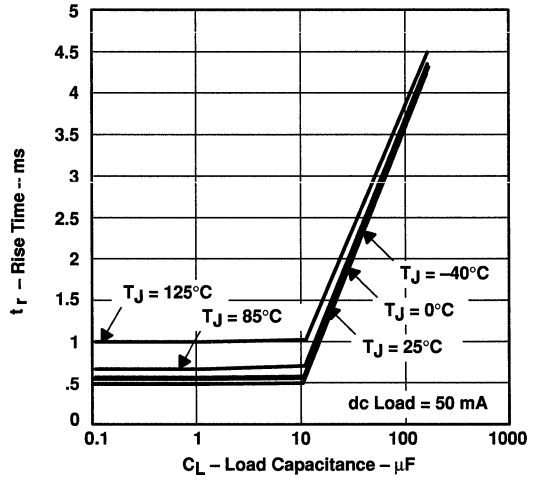


Figure 18

FALL TIME, 12-V xVPP SWITCH
vs
LOAD CAPACITANCE

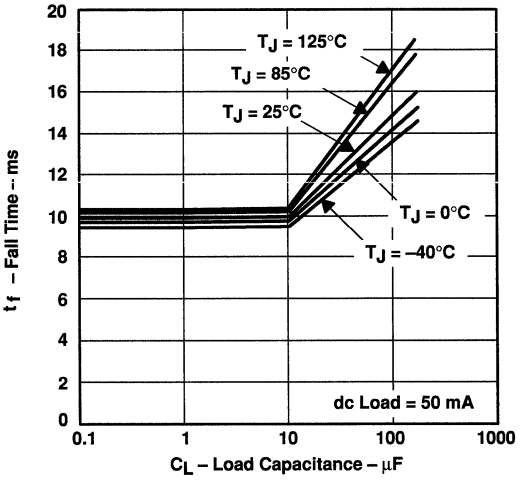


Figure 19

TYPICAL CHARACTERISTICS

INPUT CURRENT AT $V_{O(xVCC)} = V_{O(xVPP)} = 3.3$ V
vs
JUNCTION TEMPERATURE

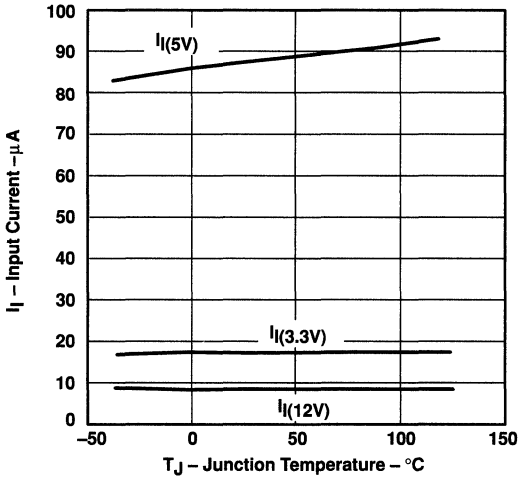


Figure 20

INPUT CURRENT AT $V_{O(xVCC)} = V_{O(xVPP)} = 5$ V
vs
JUNCTION TEMPERATURE

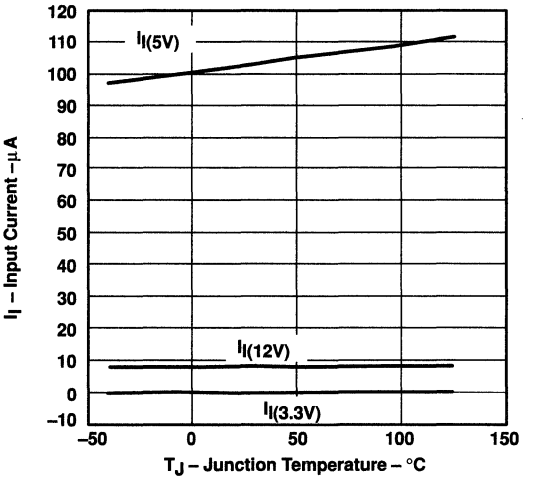


Figure 21

INPUT CURRENT AT $V_{O(xVCC)} = 5$ V, $V_{O(xVPP)} = 12$ V
vs
JUNCTION TEMPERATURE

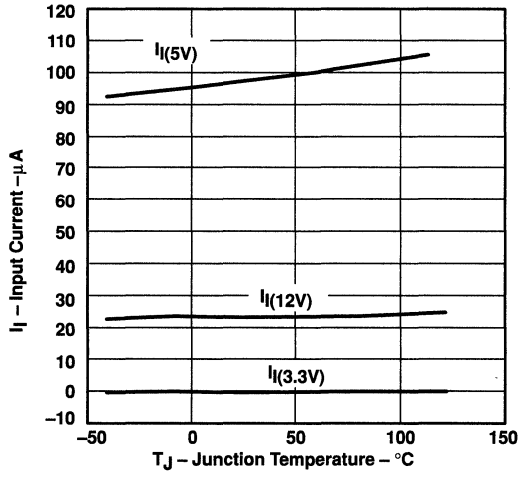


Figure 22

STATIC DRAIN-SOURCE ON-STATE RESISTANCE,
3.3-V xVCC SWITCH
vs
JUNCTION TEMPERATURE

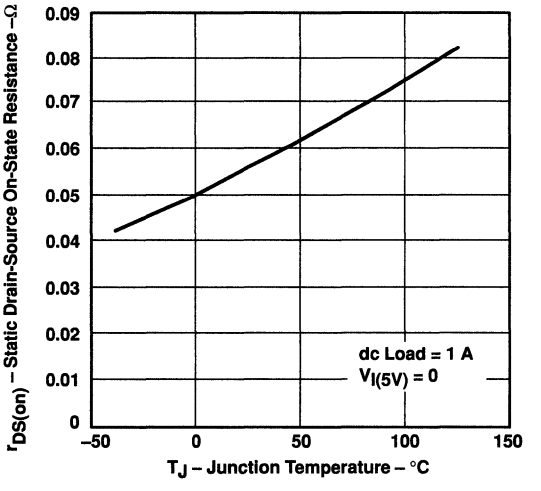


Figure 23

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE,
3.3-V xVCC SWITCH
vs
JUNCTION TEMPERATURE

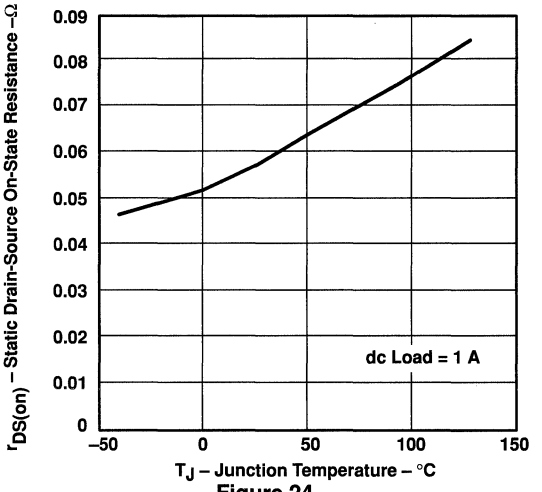


Figure 24

STATIC DRAIN-SOURCE ON-STATE RESISTANCE,
5-V xVCC SWITCH
vs
JUNCTION TEMPERATURE

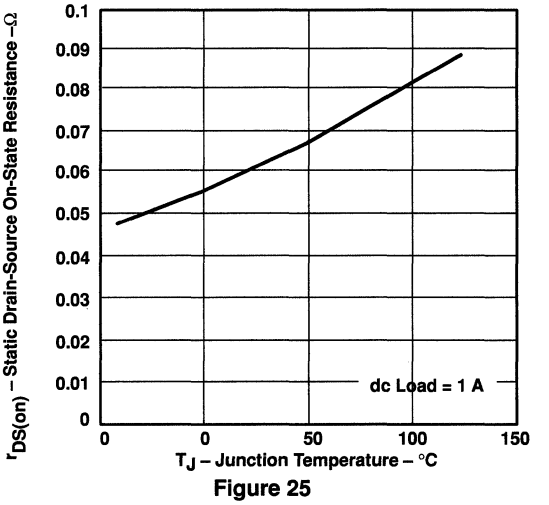


Figure 25

STATIC DRAIN-SOURCE ON-STATE RESISTANCE,
12-V xVPP SWITCH
vs
JUNCTION TEMPERATURE

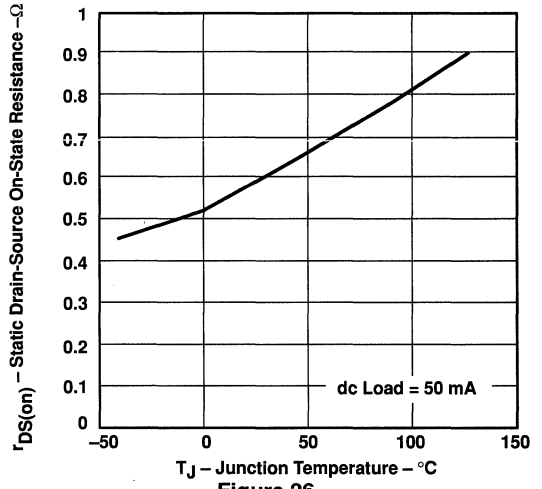


Figure 26

dc INPUT-TO-OUTPUT VOLTAGE (DROP),
3.3-V xVCC SWITCH
vs
LOAD CURRENT

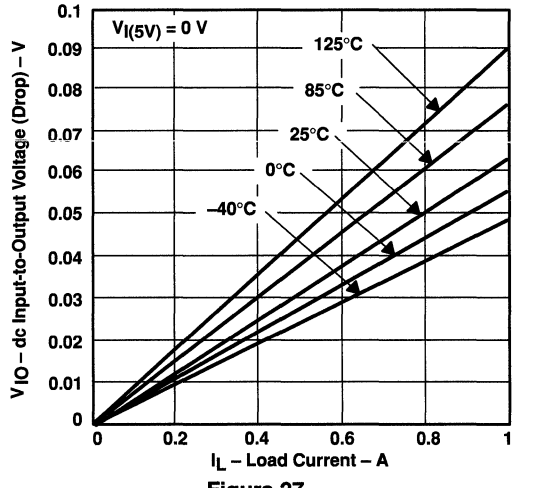


Figure 27

TYPICAL CHARACTERISTICS

dc INPUT-TO-OUTPUT VOLTAGE (DROP),
3.3-V xVCC SWITCH
vs
LOAD CURRENT

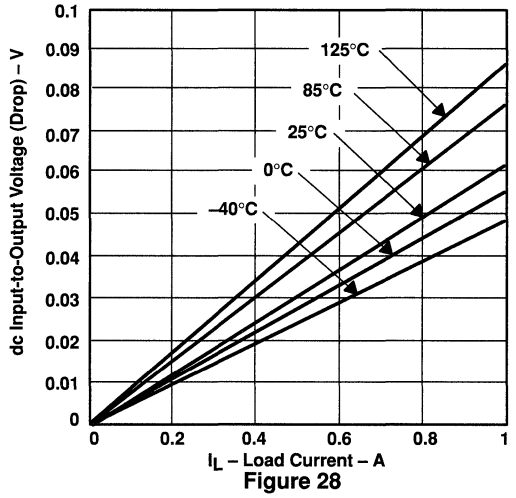


Figure 28

dc INPUT-TO-OUTPUT VOLTAGE (DROP),
5-V xVCC SWITCH
vs
LOAD CURRENT

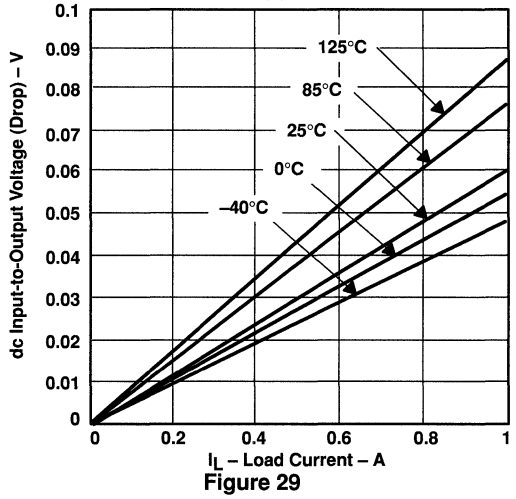


Figure 29

dc INPUT-TO-OUTPUT VOLTAGE (DROP),
12-V xVPP SWITCH
vs
LOAD CURRENT

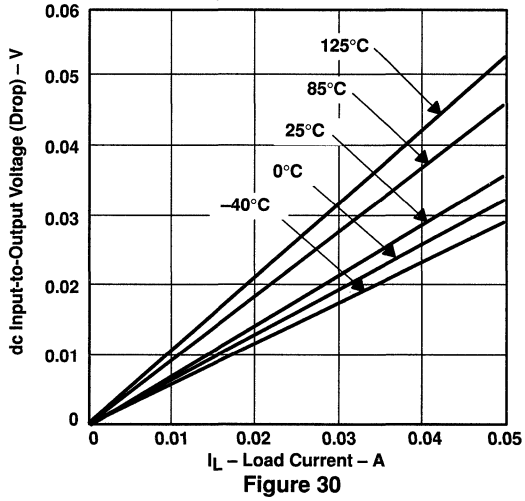


Figure 30

SHORT-CIRCUIT CURRENT LIMIT,
3.3-V xVCC SWITCH
vs
JUNCTION TEMPERATURE

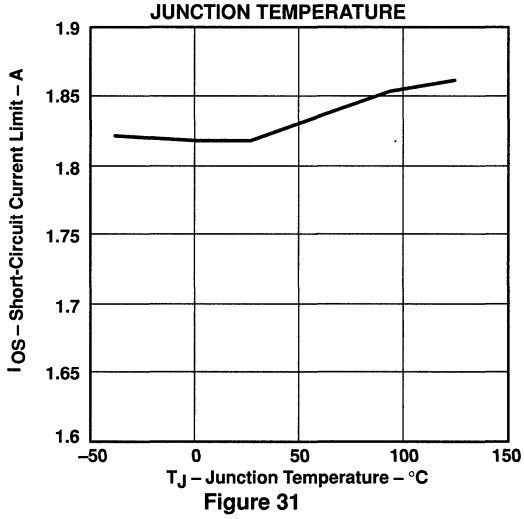


Figure 31

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT CURRENT LIMIT, 5-V xVCC SWITCH vs JUNCTION TEMPERATURE

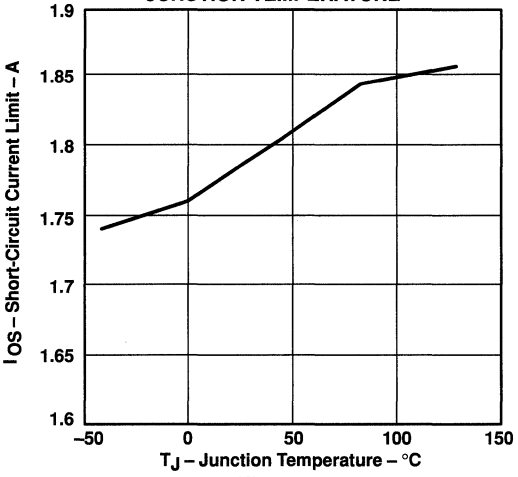


Figure 32

SHORT-CIRCUIT CURRENT LIMIT, 12-V xVPP SWITCH vs JUNCTION TEMPERATURE

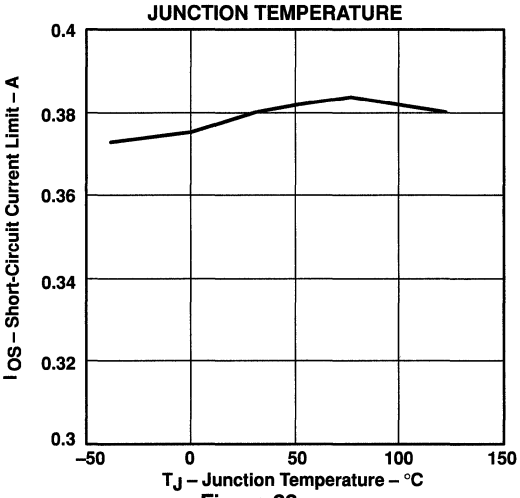


Figure 33

APPLICATION INFORMATION

overview

PC Cards were initially introduced as a means to add EEPROM (flash memory) to portable computers with limited onboard memory. The idea of add-in cards quickly took hold; modems, wireless LANs, Global Positioning Satellite System (GPS), multimedia, and hard-disk versions were soon available. As the number of PC Card applications grew, the engineering community quickly recognized the need for a standard to ensure compatibility across platforms. To this end, the PCMCIA (Personal Computer Memory Card International Association), comprising members from leading computer, software, PC Card, and semiconductor manufacturers, was established. One key goal was to realize the plug-and-play concept. Cards and hosts from different vendors should be compatible or able to communicate with one another transparently.

PC Card power specification

System compatibility also means power compatibility. The most current set of specifications (PC Card Standard) set forth by the PCMCIA committee states that power is to be transferred between the host and the card through eight of the 68 terminals of the PC Card connector. This power interface consists of two V_{CC}, two V_{pp}, and four ground terminals. Multiple V_{CC} and ground terminals minimize connector terminal and line resistance. The two V_{pp} terminals were originally specified as separate signals, but are commonly tied together in the host to form a single node to minimize voltage losses. Card primary power is supplied through the V_{CC} terminals; flash-memory programming and erase voltage is supplied through the V_{pp} terminals.

APPLICATION INFORMATION

designing for voltage regulation

The current PCMCIA specification for output voltage regulation, $V_{O(reg)}$, of the 5-V output is 5% (250 mV). In a typical PC power-system design, the power supply has an output-voltage regulation, $V_{PS(reg)}$, of 2% (100 mV). Also, a voltage drop from the power supply to the PC Card will result from resistive losses, V_{PCB}, in the PCB traces and the PCMCIA connector. A typical design would limit the total of these resistive losses to less than 1% (50 mV) of the output voltage. Therefore, the allowable voltage drop, V_{DS}, for the TPS2214 would be the PCMCIA voltage regulation less the power supply regulation and less the PCB and connector resistive drops:

$$V_{DS} = V_{O(reg)} - V_{PS(reg)} - V_{PCB}$$

Typically, this would leave 100 mV for the allowable voltage drop across the 5-V switch. The specification for output voltage regulation of the 3.3-V output is 300 mV; so, using the same equation by deducting the voltage drop percentages (2%) for power-supply regulation and PCB resistive loss (1%), the allowable voltage drop for the 3.3-V switch is 200 mV. The voltage drop is the output current multiplied by the switch resistance of the TPS2214. Therefore, the maximum output current, I_O max, that can be delivered to the PC Card in regulation is the allowable voltage drop across the IC, divided by the output-switch resistance.

$$I_O\text{max} = \frac{V_{DS}}{r_{DS(on)}}$$

The xVCC outputs can deliver 1 A continuously at 5 V and 3.3 V within regulation over the operating temperature range. The xVPP outputs of the IC can deliver 200 mA continuously.

overcurrent and overtemperature protection

PC Cards are inherently subject to damage that can result from mishandling. Host systems require protection against short-circuited cards that could lead to power-supply or PCB trace damage. Even systems robust enough to withstand a short circuit would still undergo rapid battery discharge into the damaged PC Card, resulting in the rather sudden and unacceptable loss of system power. Most hosts include fuses for protection. However, the reliability of fused systems is poor, as blown fuses require troubleshooting and repair, usually by the manufacturer.

The TPS2214 takes a two-pronged approach to overcurrent protection, which is designed to activate if an output is shorted or when an overcurrent condition is present when switches are powered up. First, instead of fuses, sense FETs monitor each of the xVCC and xVPP power outputs. Unlike sense resistors or polyfuses, these FETs do not add to the series resistance of the switch; therefore voltage and power losses are reduced. Overcurrent sensing is applied to each output separately. Excessive current generates an error signal that limits the output current of only the affected output, preventing damage to the host. Each xVCC output overcurrent limits from 1 A to 2.2 A, typically around 1.6 A; the xVPP outputs limit from 250 mA to 500 mA, typically around 375 mA.

Second, when an overcurrent condition is detected, the TPS2214 asserts an active low $\overline{OC}$ signal that can be monitored by the microprocessor or controller to initiate diagnostics and/or send the user a warning message. In the event that an overcurrent condition persists, causing the IC to exceed its maximum junction temperature, thermal-protection circuitry activates. This shuts down all power outputs until the device cools to within a safe operating region, which is ensured by a thermal shutdown hysteresis.

APPLICATION INFORMATION

12-V supply not required

Many PC Card switches use the externally supplied 12 V to power gate drive and other chip functions; this requires that power be present at all times. The TPS2214 offers considerable power savings by using an internal charge pump to generate the required higher gate drive voltages from the 5-V or 3.3-V power supplies. Therefore, the external 12-V supply can be disabled except when needed for flash-memory functions, thereby extending battery lifetime. Additional power savings are realized by the IC during shutdown mode, in which quiescent current drops to a maximum of 1 µA.

3.3-V low-voltage mode

The TPS2214 will operate in 3.3-V low-voltage mode when 3.3 V is the only available input voltage ($V_{I(5V)}$ = 0, $V_{I(12V)}$ = 0). This feature allows host and PC Cards to be operated in low-power 3.3-V-only modes such as sleep modes. Note that in this operation mode, the IC will derive its bias current from the 3.3-V input pin and can only provide 3.3 V to the outputs.

voltage transitioning requirement

PC Cards are migrating from 5 V to 3.3 V to minimize power consumption, optimize board space, and increase logic speeds. The TPS2214 meets all combinations of power delivery as currently defined in the PCMCIA standard. The latest protocol accommodates mixed 3.3-V/5-V systems by first powering the card with 5 V, then polling it to determine its 3.3-V compatibility. The PCMCIA specification requires that the capacitors on 3.3-V-compatible cards be discharged to below 0.8 V before applying 3.3-V power. This action ensures that sensitive 3.3-V circuitry is not subjected to any residual 5-V charge and functions as a power reset. PC Card specification requires that V_{CC} be discharged within 100 ms. PC Card resistance can not be relied on to provide a discharge path for voltages stored on PC Card capacitance because of possible high-impedance isolation by power-management schemes. The TPS2214 includes discharge transistors on all xVCC and xVPP outputs to meet the specification requirement.

shutdown mode

In the shutdown mode, which can be controlled by bit D8 of the input serial DATA word, each of the xVCC and xVPP outputs is forced to a high-impedance state. In this mode, the chip quiescent current is limited to 1 µA or less to conserve battery power.

standby mode

The TPS2214 can be put in standby mode by pulling $\overline{\text{STBY}}$ low to conserve power during low-power operation. In this mode, all of the power outputs (xVCC and xVPP) will have a nominal current limit of 50 mA. $\overline{\text{STBY}}$ has an internal 150-kΩ pullup resistor. The output-switch status of the device must be set, allowing the output capacitors to charge, prior to enabling the standby mode. Changing the setting of the output switches with the device in standby mode may cause an overcurrent response to be generated.

mode

The mode pin programs the switches in either TPS2214 or TPS2206 mode. An internal 150-kΩ pulldown resistor is connected to the pin. Floating or pulling the mode pin low sets the switches in TPS2206 mode; pulling the mode pin high sets the switches in TPS2214 mode. In TPS2206 mode, xVPP outputs are dependent on xVCC outputs. In TPS2214 mode, xVPP is programmed independent of xVCC. Refer to TPS2214 control-logic tables for more information.

APPLICATION INFORMATION

power supply considerations

The TPS2214 has multiple pins for each of its 3.3-V and 5-V power inputs and for the switched xVCC outputs. Any individual pin can conduct the rated input or output current. Unless all pins are connected in parallel, the series resistance is higher than that specified, resulting in increased voltage drops and less power. It is recommended that all input and output power pins be paralleled for optimum operation. Because the two 12-V pins are not internally connected, they must be tied together externally.

To increase the noise immunity of the TPS2214, the power-supply inputs should be bypassed with a 1-µF electrolytic or tantalum capacitor paralleled by a 0.047-µF to 0.1-µF ceramic capacitor. It is strongly recommended that the switched outputs be bypassed with a 0.1-µF (or larger) ceramic capacitor; doing so improves the immunity of the IC to electrostatic discharge (ESD). Care should be taken to minimize the inductance of PCB traces between the IC and the load. High switching currents can produce large negative voltage transients, which forward biases substrate diodes, resulting in unpredictable performance. Similarly, no pin should be taken, or allowed to fall, below –0.3 V.

RESET and $\overline{\text{RESET}}$ inputs

To ensure that cards are in a known state after power brownouts or system initialization, the PC Cards should be reset at the same time as the host by applying low impedance paths from xVCC and xVPP terminals to ground. A low-impedance output state allows discharging of residual voltage remaining on PC Card filter capacitance, permitting the system (host and PC Cards) to be powered up concurrently. The active-high RESET or active low $\overline{\text{RESET}}$ input will close internal switches S1, S4, S7, and S11 with all other switches left open. The TPS2214 remains in the low-impedance output state until the signal is deasserted and further data is clocked in and latched. The input serial data can not be latched during Reset mode. RESET and $\overline{\text{RESET}}$ are provided for direct compatibility with systems that use either an active-low or active-high reset voltage supervisor. The RESET pin has an internal 150-kΩ pulldown resistor and the $\overline{\text{RESET}}$ pin has an internal 150-kΩ pullup resistor. The device will be reset automatically when powered up.

calculating junction temperature

The switch resistance, $r_{DS(on)}$, is dependent on the junction temperature, T_J, of the die. The junction temperature is dependent on both $r_{DS(on)}$ and the current through the switch. To calculate T_J, first find $r_{DS(on)}$ from Figures 23 through 26, using an initial temperature estimate about 50°C above ambient. Then calculate the power dissipation for each switch, using the formula:

$$P_D = r_{DS(on)} \times I^2$$

Next, sum the power dissipation of all switches and calculate the junction temperature:

$$T_J = \left(\sum P_D \times R_{\theta JA}\right) + T_A$$

Where:

$R_{\theta JA}$ is the inverse of the derating factor given in the dissipation rating table.

Compare the calculated junction temperature with the initial temperature estimate. If the temperatures are not within a few degrees of each other, recalculate using the calculated temperature as the initial estimate.

logic inputs and outputs

The serial interface consists of DATA, CLOCK, and LATCH leads. The data is clocked in on the positive edge of the clock (see Figures 2 and 3). The 11-bit (D0–D10) serial data word is loaded during the positive edge of the latch signal. The positive edge of the latch signal should occur before the next positive edge of the clock occurs.

APPLICATION INFORMATION

logic inputs and outputs (continued)

The TPS2214 serial interfaces are compatible with serial-interface PCMCIA controllers and current PCMCIA and Japan Electronic Industry Development Association (JEIDA) standards.

An overcurrent output ($\overline{OC}$) is provided to indicate an overcurrent or overtemperature condition in any of the xVCC and xVPP outputs as previously discussed.

TPS2214 control logic

TPS2214 mode (MODE pulled high)

xVPP

	AVPP CONTROL SIGNALS			OUTPUT V_AVPP	BVPP CONTROL SIGNALS				OUTPUT V_BVPP
D8 ($\overline{SHDN}$)	D0	D1	D9		D8 ($\overline{SHDN}$)	D4	D5	D10	
1	0	0	X	0 V	1	0	0	X	0 V
1	0	1	0	3.3 V	1	0	1	0	3.3 V
1	0	1	1	5 V	1	0	1	1	5 V
1	1	0	X	12 V	1	1	0	X	12 V
1	1	1	X	Hi-Z	1	1	1	X	Hi-Z
0	X	X	X	Hi-Z	0	X	X	X	Hi-Z

xVCC

	AVCC CONTROL SIGNALS		OUTPUT V_AVCC	BVCC CONTROL SIGNALS			OUTPUT V_BVCC
D8 ($\overline{SHDN}$)	D3	D2		D8 ($\overline{SHDN}$)	D6	D7	
1	0	0	0 V	1	0	0	0 V
1	0	1	3.3 V	1	0	1	3.3 V
1	1	0	5 V	1	1	0	5 V
1	1	1	0 V	1	1	1	0 V
0	X	X	Hi-Z	0	X	X	Hi-Z

TPS2206 mode (MODE floating or pulled low)

xVPP

	AVPP CONTROL SIGNALS		OUTPUT V_AVPP	BVPP CONTROL SIGNALS			OUTPUT V_BVPP
D8 ($\overline{SHDN}$)	D0	D1		D8 ($\overline{SHDN}$)	D4	D5	
1	0	0	0 V	1	0	0	0 V
1	0	1	V_AVCC	1	0	1	V_BVCC
1	1	0	12 V	1	1	0	12 V
1	1	1	Hi-Z	1	1	1	Hi-Z
0	X	X	Hi-Z	0	X	X	Hi-Z

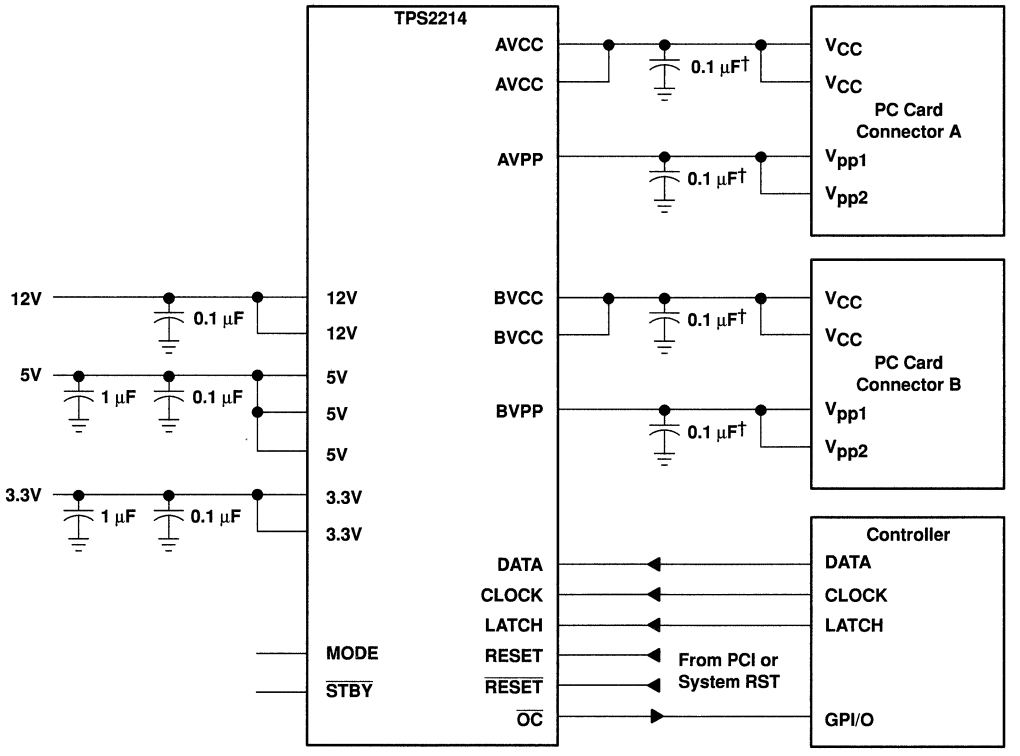
xVCC

	AVCC CONTROL SIGNALS		OUTPUT V_AVCC	BVCC CONTROL SIGNALS			OUTPUT V_BVCC
D8 ($\overline{SHDN}$)	D3	D2		D8 ($\overline{SHDN}$)	D6	D7	
1	0	0	0 V	1	0	0	0 V
1	0	1	3.3 V	1	0	1	3.3 V
1	1	0	5 V	1	1	0	5 V
1	1	1	0 V	1	1	1	0 V
0	X	X	Hi-Z	0	X	X	Hi-Z

APPLICATION INFORMATION

ESD protections (see Figure 34)

All TPS2214 inputs and outputs incorporate ESD-protection circuitry designed to withstand a 2-kV human-body-model discharge as defined in MIL-STD-883C, Method 3015. The xVCC and xVPP outputs can be exposed to potentially higher discharges from the external environment through the PC Card connector. Bypassing the outputs with 0.1-μF capacitors protects the devices from discharges up to 10 kV.



† Maximum recommended output capacitance for xVCC is 220 μF and for xVPP is 10 μF without $\overline{OC}$ glitch when switches are powered on.

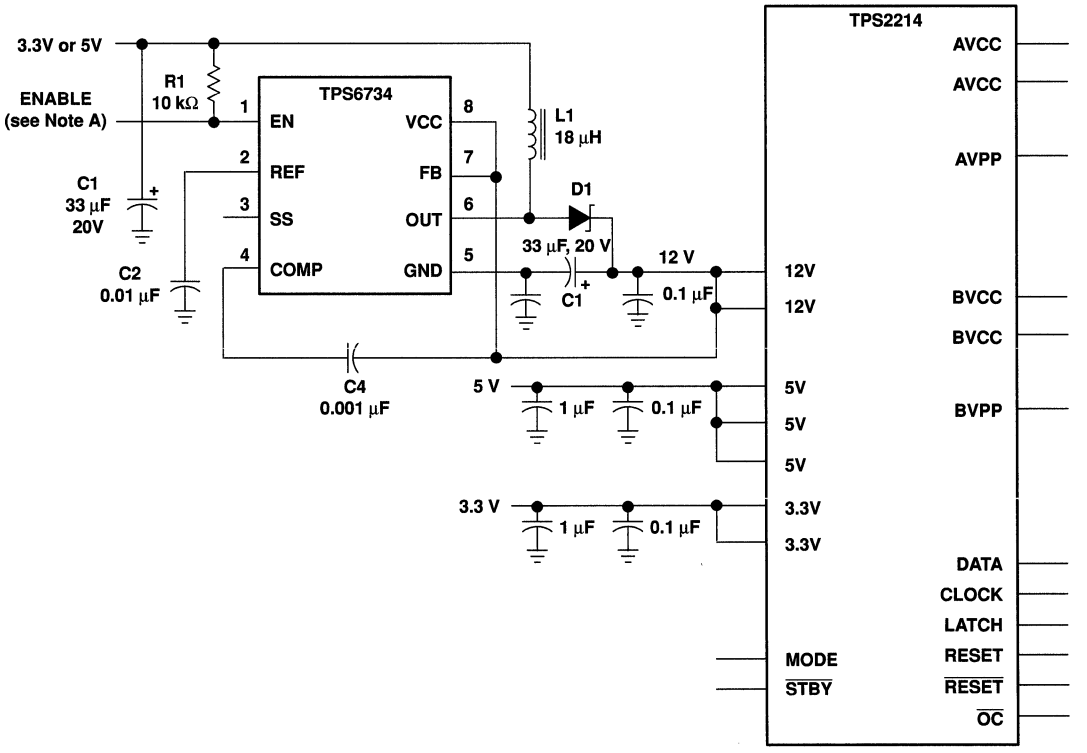
Figure 34. Detailed Interconnections and Capacitor Recommendations

APPLICATION INFORMATION

12-V flash memory supply

The TPS6734 is a fixed 12-V output boost converter capable of delivering 120 mA from inputs as low as 2.7 V. The device is pin-for-pin compatible with the MAX734 regulator and offers the following advantages: lower supply current, wider operating input-voltage range, and higher output currents. As shown in Figure 35, the only external components required are: an inductor, a Schottky rectifier, an output filter capacitor, an input filter capacitor, and a small capacitor for loop compensation. The entire converter occupies less than 0.7 in^2 of PCB space when implemented with surface-mount components. An enable input is provided to shut the converter down and reduce the supply current to 3 μA when 12 V is not needed.

The TPS6734 is a 170-kHz current-mode PWM (pulse-width modulation) controller with an n-channel MOSFET power switch. Gate drive for the switch is derived from the 12-V output after start-up to minimize the die area needed to realize the 0.7-Ω MOSFET and improve efficiency at input voltages below 5 V. Soft start is accomplished with the addition of one small capacitor. A 1.22-V reference (pin 2) is brought out for external use. For additional information, see the TPS6734 data sheet (SLVS127).

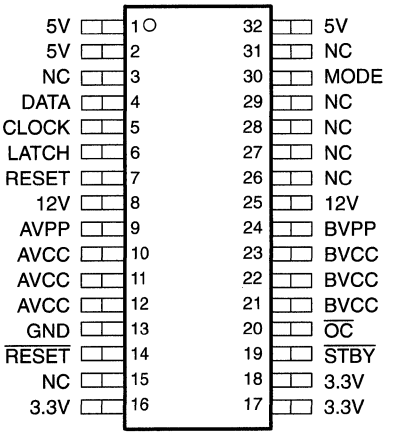


NOTE A. The enable terminal can be tied to a general-purpose I/O terminal on the PCMCIA controller or tied high.

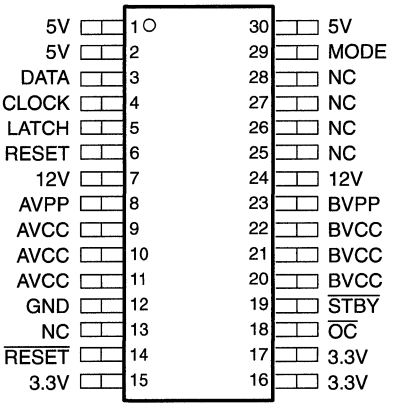
Figure 35. TPS2214 with TPS6734 12-V, 120-mA Supply

- **Fully Integrated xVCC and xVPP Switching**
- **xVPP Programmed Independent of xVCC**
- **3.3-V, 5-V, and/or 12-V Power Distribution**
- **Low $r_{DS(on)}$ (60-mΩ xVCC Switch Typical)**
- **Short Circuit and Thermal Protection**
- **150-μA (maximum) Quiescent Current**
- **Standby Mode: 50-mA Current Limit (Typ)**
- **12-V Supply Can Be Disabled**
- **3.3-V Low-Voltage Mode**
- **Meets PC Card™ Standards**
- **TTL-Logic Compatible Inputs**
- **Available in 30-Pin SSOP (DB) and 32-Pin TSSOP (DAP) Packages**
- **Break-Before-Make Switching**
- **Internal Power-On Reset**

DAP PACKAGE†
(TOP VIEW)



DB PACKAGE†
(TOP VIEW)



† The TPS2216 is identical to the TPS2214 in all respects except packaging and pin assignments.

NC – No internal connection

description

The TPS2216 PC Card power-interface switch provides an integrated power-management solution for two PC Cards. All of the discrete power MOSFETs, a logic section, current limiting, and thermal protection for PC Card control are combined on a single integrated circuit. This device allows the distribution of 3.3-V, 5-V, and/or 12-V power to the card. The current-limiting feature eliminates the need for fuses. Current-limit reporting can help the user isolate a system fault.

The TPS2216 features a 3.3-V low-voltage mode that allows for 3.3-V switching without the need for 5-V power. This feature facilitates low-power system designs such as sleep modes where only 3.3 V is available. This device also has the ability to program the xVPP outputs independent of the xVCC outputs. A standby mode that changes all output-current limits to 50 mA (typical) has been incorporated.

End-equipment applications for the TPS2216 include: notebook computers, desktop computers, personal digital assistants (PDAs), digital cameras, and bar-code scanners.

The TPS2216 is backward-compatible with the TPS2202A and TPS2206.

PC Card is a trademark of PCMCIA (Personal Computer Memory Card International Association).

AVAILABLE OPTIONS

T_J	PACKAGED DEVICES†	
	PLASTIC SMALL OUTLINE (DB)	PowerPAD PLASTIC SMALL OUTLINE™ (DAP)
–40°C to 125°C	TPS2216DB(R)	TPS2216DAP(R)

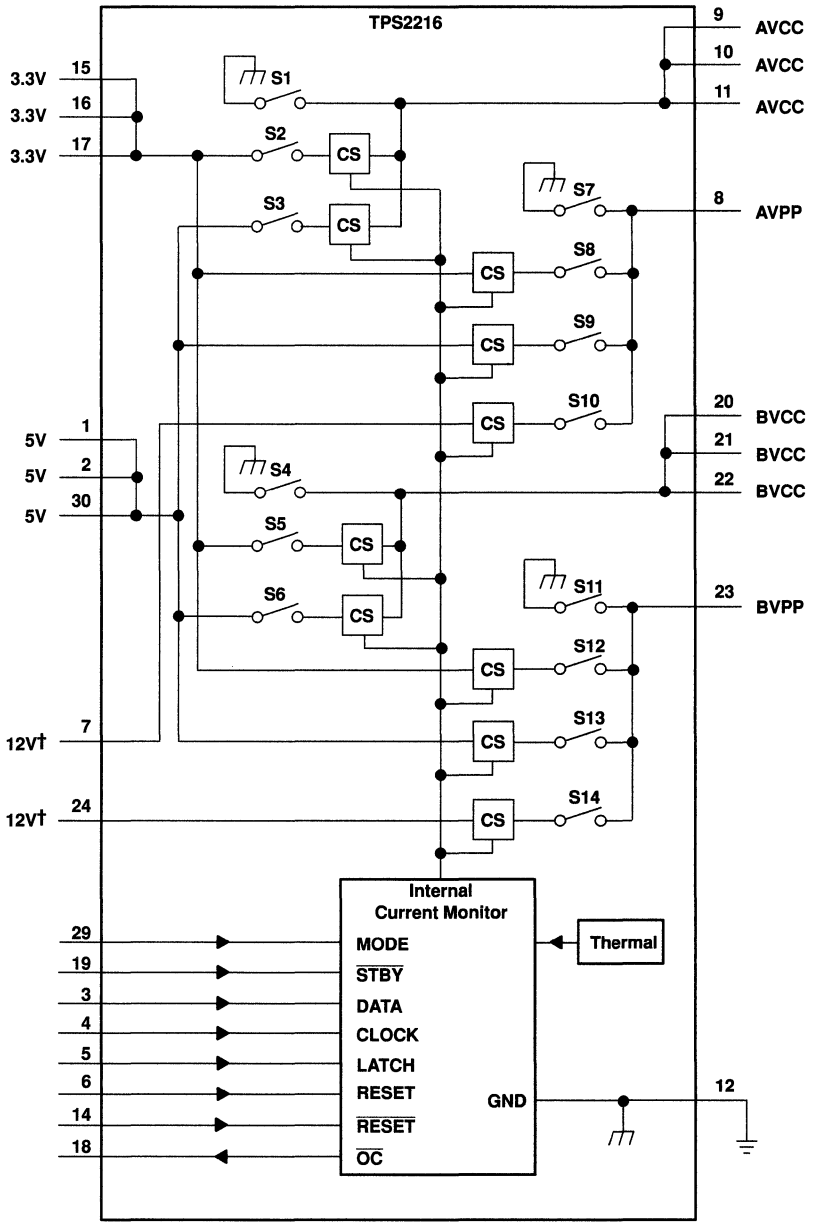
† The DB and DAP packages are available in tubes and left-end taped and reeled. Add R suffix to device type (e.g., TPS2216DBR) for taped and reeled.

Terminal Functions

TERMINAL NAME	TERMINAL NO. DB	TERMINAL NO. DAP	I/O	DESCRIPTION
3.3V	15, 16, 17	16, 17, 18	I	3.3-V input for card power and/or chip power if 5 V is not present
5V	1, 2, 30	1, 2, 32	I	5-V input for card power and/or chip power
12V	7, 24	8, 25	I	12-V V_{pp} input card power
AVCC	9, 10, 11	10, 11, 12	O	VCC output: 3.3-V, 5-V, GND or high impedance to card
AVPP	8	9	O	VPP output: 3.3-V, 5-V, 12-V, GND or high impedance to card
BVCC	20, 21, 22	21, 22, 23	O	VCC output: 3.3-V, 5-V, GND or high impedance to card
BVPP	23	24	O	VPP output: 3.3-V, 5-V, 12-V, GND or high impedance to card
GND	12	13		Ground
MODE	29	30	I	TPS2206 operation when floating or pulled low; must be pulled high externally for TPS2216 operation. MODE is internally pulled low with a 150-kΩ pulldown resistor.
$\overline{OC}$	18	20	O	Logic-level output that goes low when an overcurrent or overtemperature condition exists.
RESET	6	7	I	Logic-level reset input active high. Do not connect if $\overline{RESET}$ pin is used. RESET is internally pulled low with a 150-kΩ pulldown resistor.
$\overline{RESET}$	14	14	I	Logic-level reset input active low. Do not connect if RESET pin is used. The pin is internally pulled high with a 150-kΩ pullup resistor.
$\overline{STBY}$	19	19	I	Logic-level active low input sets the TPS2216 to standby mode and sets all current limits to 50 mA. The pin is internally pulled high with a 150-kΩ pullup resistor.
CLOCK	4	5	I	Logic-level clock for serial data word
DATA	3	4	I	Logic-level serial data word
LATCH	5	6	I	Logic-level latch for serial data word
NC	13, 25, 26, 27, 28	3, 15, 26, 27, 28, 29, 31		No internal connection

PowerPAD is a trademark of Texas Instruments Incorporated.

functional block diagram (pin numbers refer to DB package)



† Both 12V pins must be connected together.

absolute maximum ratings over operating virtual free-air temperature (unless otherwise noted)†

Input voltage range for card power: $V_{I(3.3V)}$ ..... –0.3 V to 6 V
$V_{I(5V)}$ ..... –0.3 V to 6 V
$V_{I(12V)}$ ..... –0.3 V to 14 V
Logic input voltage ..... –0.3 V to 6 V
Output voltage range: $V_{O(xVCC)}$ ..... –0.3 V to 6 V
$V_{O(xVPP)}$ ..... –0.3 V to 14 V
Continuous total power dissipation ..... See Dissipation Rating Table
Output current: $I_{O(xVCC)}$ ..... Internally limited
$I_{O(xVPP)}$ ..... Internally limited
Operating virtual junction temperature range, T_J ..... –40°C to 125°C
Storage temperature range, T_{stg} ..... –55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DB	1095 mW	10.99 mW/°C	602 mW	438 mW
DAP	4255 mW	42.55 mW/°C	2340 mW	1702 mW

‡ These devices are mounted on an JEDEC low-k board (2 oz. traces on surface), 1-W power applied.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	$V_{I(3.3V)}$	2.7	5.25	V
	$V_{I(5V)}$	2.7	5.25	V
	$V_{I(12V)}$	2.7	13.5	V
Output current, I_O	$I_{O(VCC)}$ at $T_A = 70°C$		1	A
	$I_{O(VPP)}$ at $T_A = 70°C$		200	mA
Clock frequency			2.5	MHz
Pulse duration	Data	200		ns
	Latch	250		
	Clock	100		
Data hold time§		100		ns
Data setup time§		100		ns
Latch delay time§		100		ns
Clock delay time§		250		ns
Operating virtual junction temperature, T_J		–40	125	°C

§ Refer to Figures 2 and 3.

electrical characteristics, T_J = 25°C, $V_{I(5V)}$ = 5 V, $V_{I(3.3V)}$ = 3.3 V, $V_{I(12V)}$ = 12 V, $\overline{STBY}$ floating, all outputs unloaded (unless otherwise noted)

power switch

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Switch resistance†	3.3 V to xVCC, with one switch on		T_J = 25°C, I_O = 1 A		60	85	mΩ
			T_J = 125°C, I_O = 1 A		90	120	
			T_J = 25°C, $V_{I(5V)}$ = 0, I_O = 1 A		65	85	
			T_J = 125°C, $V_{I(5V)}$ = 0, I_O = 1 A		90	130	
	5 V to xVCC, with one switch on		T_J = 25°C, I_O = 1 A		60	85	
			T_J = 125°C, I_O = 1 A		90	120	
	3.3 V to xVCC, with two switches on		T_J = 25°C, I_O = 1 A each		65	105	
			T_J = 125°C, I_O = 1 A each		95	140	
			T_J = 25°C, $V_{I(5V)}$ = 0, I_O = 1 A each		70	105	
			T_J = 125°C, $V_{I(5V)}$ = 0, I_O = 1 A each		100	140	
	5 V to xVCC, with two switches on		T_J = 25°C, I_O = 1 A each		70	105	
			T_J = 125°C, I_O = 1 A each		100	140	
	3.3 V/5 V/12 V to xVPP		T_J = 25°C, I_O = 50 mA		0.7	1	Ω
			T_J = 125°C, I_O = 50 mA		1.4	2.5	
	3.3 V/5 V to xVCC		T_J = 25°C, $\overline{STBY}$ = low, I_O = 30 mA		1.4	2	
			T_J = 125°C, $\overline{STBY}$ = low, I_O = 30 mA		2	3	
	3.3 V/5 V/12 V to xVPP		T_J = 25°C, $\overline{STBY}$ = low, I_O = 30 mA		5	7	
			T_J = 125°C, $\overline{STBY}$ = low, I_O = 30 mA		10	16	
Clamp low voltage	$V_{O(xVCC)}$		$I_{O(xVCC)}$ at 10 mA, After reset		0.275	0.8	V
	$V_{O(xVPP)}$		$I_{O(xVPP)}$ at 10 mA, After reset		0.275	0.8	
I_{lkg} Leakage current	$I_{O(xVCC)}$ High-impedance state		T_J = 25°C		1	10	µA
			T_J = 125°C		2	50	
	$I_{O(xVPP)}$ High-impedance state		T_J = 25°C		1	10	
			T_J = 125°C		2	50	
I_{OS} Short-circuit output current limit†	$I_{O(xVCC)}$		T_J = 85°C, output powered into a short to GND	1		2.2	A
	$I_{O(xVPP)}$			250		500	mA
	Standby mode $I_{O(xVCC)}$		T_J = 85°C, Output powered into a short to GND, $\overline{STBY}$ = 0 V	35	50	65	mA
	Standby mode $I_{O(xVPP)}$			30	50	60	
Current limit response time‡	xVCC switch		100-mΩ short circuit		100		µs
	xVPP switch				16		
I_I Input current§	Normal operation and in reset mode	$I_{I(3.3V)}$	$V_{O(xVCC)}$ = $V_{O(xVPP)}$ = 5 V		0.01	2	µA
		$I_{I(5V)}$			100	120	
		$I_{I(12V)}$			6	10	
		$I_{I(3.3V)}$	$V_{I(5V)}$ = 0, $V_{O(xVCC)}$ = 3.3 V, $V_{O(xVPP)}$ = 12 V		100	120	µA
		$I_{I(5V)}$			0		
		$I_{I(12V)}$			22	30	
	Shutdown mode	$I_{I(3.3V)}$	$V_{O(xVCC)}$ = Hi-Z, $V_{O(xVPP)}$ = Hi-Z			1	µA
		$I_{I(5V)}$				1	
		$I_{I(12V)}$				1	
Thermal shutdown‡	Trip point, T_J				155		°C
	Hysteresis				10		

† Pulse-testing techniques maintain junction temperature close to ambient temperature (250-µs-wide pulse, less than 0.5% duty cycle); thermal effects must be taken into account separately.
‡ Specified by design, not tested in production.
§ Input currents do not include logic input currents (presented in electrical characteristics for logic section); clock is inactive.
NOTE: $V_{I(3.3V)}$ or $V_{I(5V)}$ must be biased for switches to function.

logic section (CLOCK, DATA, LATCH, MODE, RESET, $\overline{\text{RESET}}$, $\overline{\text{STBY}}$, $\overline{\text{OC}}$)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic input current	$I_{I(RESET)}$ or $I_{I(\overline{RESET})}$†	$V_{I(RESET)}$ = 5 V or $V_{I(\overline{RESET})}$ = 0 V		30	50	µA
		$V_{I(RESET)}$ = 0 V or $V_{I(\overline{RESET})}$ = 5 V			1	
	$I_{I(MODE)}$†	$V_{I(MODE)}$ = 5 V		30	50	
		$V_{I(MODE)}$ = 0 V			1	
	$I_{I(\overline{STBY})}$†	$V_{I(\overline{STBY})}$ = 5 V			1	
		$V_{I(\overline{STBY})}$ = 0 V		30	50	
	$I_{I(CLOCK)}$ or $I_{I(DATA)}$ or $I_{I(LATCH)}$				1	
Logic input high level		$V_{I(5V)}$ = 5 V	2			V
		$V_{I(5V)}$ = 0 V	2			
Logic input low level					0.8	V
Logic output high level, $\overline{\text{OC}}$		$V_{I(5V)}$ = 5 V, I_O = 1 mA	$V_{I(5V)}$–0.4			V
		$V_{I(5V)}$ = 0 V, I_O = 1 mA	$V_{I(3.3V)}$–0.4			
Logic output low level, $\overline{\text{OC}}$		I_O = 1 mA			0.4	V

† RESET and MODE have internal 150-kΩ pulldown resistors; $\overline{\text{RESET}}$ and $\overline{\text{STBY}}$ have internal 150-kΩ pullup resistors.

switching characteristics

PARAMETER†		LOAD CONDITION†	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
t_r	Output rise times‡	$C_{L(xVCC)}$ = 0.1 µF, $C_{L(xVPP)}$ = 0.1 µF, $I_{O(xVCC)}$ = 0§, $I_{O(xVPP)}$ = 0§	$V_{O(xVCC)}$			1		ms
			$V_{O(xVPP)}$			0.8		
		$C_{L(xVCC)}$ = 150 µF, $C_{L(xVPP)}$ = 10 µF, $I_{O(xVCC)}$ = 1 A, $I_{O(xVPP)}$ = 50 mA	$V_{O(xVCC)}$			1.2		
			$V_{O(xVPP)}$			2.5		
t_f	Output fall times‡	$C_{L(xVCC)}$ = 0.1 µF, $C_{L(xVPP)}$ = 0.1 µF, $I_{O(xVCC)}$ = 0§, $I_{O(xVPP)}$ = 0§	$V_{O(xVCC)}$			0.01		ms
			$V_{O(xVPP)}$			0.01		
		$C_{L(xVCC)}$ = 150 µF, $C_{L(xVPP)}$ = 10 µF, $I_{O(xVCC)}$ = 1 A, $I_{O(xVPP)}$ = 50 mA	$V_{O(xVCC)}$			3		
			$V_{O(xVPP)}$			8		
t_{pd}	Propagation delay‡	$C_{L(xVCC)}$ = 0.1 µF, $C_{L(xVPP)}$ = 0.1 µF, $I_{O(xVCC)}$ = 0§, $I_{O(xVPP)}$ = 0§	Latch↑ to xVPP (12 V)	$t_{pd(on)}$		3		ms
				$t_{pd(off)}$		25		
			Latch↑ to xVPP (5 V)	$t_{pd(on)}$		0.6		
				$t_{pd(off)}$		8.5		
			Latch↑ to xVPP (3.3 V), $V_{I(5V)}$ = 5 V	$t_{pd(on)}$		0.6		
				$t_{pd(off)}$		9		
			Latch↑ to xVPP (3.3 V), $V_{I(5V)}$ = 0 V	$t_{pd(on)}$		1.4		
				$t_{pd(off)}$		9		
			Latch↑ to xVCC (5 V)	$t_{pd(on)}$		0.3		
				$t_{pd(off)}$		15		
			Latch↑ to xVCC (3.3 V), $V_{I(5V)}$ = 5 V	$t_{pd(on)}$		0.2		
				$t_{pd(off)}$		15		
			Latch↑ to xVCC (3.3 V), $V_{I(5V)}$ = 0 V	$t_{pd(on)}$		0.4		
				$t_{pd(off)}$		15		
		$C_{L(xVCC)}$ = 150 µF, $C_{L(xVPP)}$ = 10 µF, $I_{O(xVCC)}$ = 1 A, $I_{O(xVPP)}$ = 50 mA	Latch↑ to xVPP (12 V)	$t_{pd(on)}$		4.5		
				$t_{pd(off)}$		13		
			Latch↑ to xVPP (5 V)	$t_{pd(on)}$		3.3		
				$t_{pd(off)}$		8		
			Latch↑ to xVPP (3.3 V), $V_{I(5V)}$ = 5 V	$t_{pd(on)}$		3		
				$t_{pd(off)}$		9		
			Latch↑ to xVPP (3.3 V), $V_{I(5V)}$ = 0 V	$t_{pd(on)}$		3		
				$t_{pd(off)}$		9		
			Latch↑ to xVCC (5 V)	$t_{pd(on)}$		1		
				$t_{pd(off)}$		12		
			Latch↑ to xVCC (3.3 V), $V_{I(5V)}$ = 5 V	$t_{pd(on)}$		0.6		
				$t_{pd(off)}$		12		
			Latch↑ to xVCC (3.3 V), $V_{I(5V)}$ = 0 V	$t_{pd(on)}$		1		
				$t_{pd(off)}$		12		

† Refer to *Parameter Measurement Information*
‡ Specified by design: not tested in production.
§ No card inserted, assumes 0.1-µF recommended output capacitor (see Figure 34).

PARAMETER MEASUREMENT INFORMATION

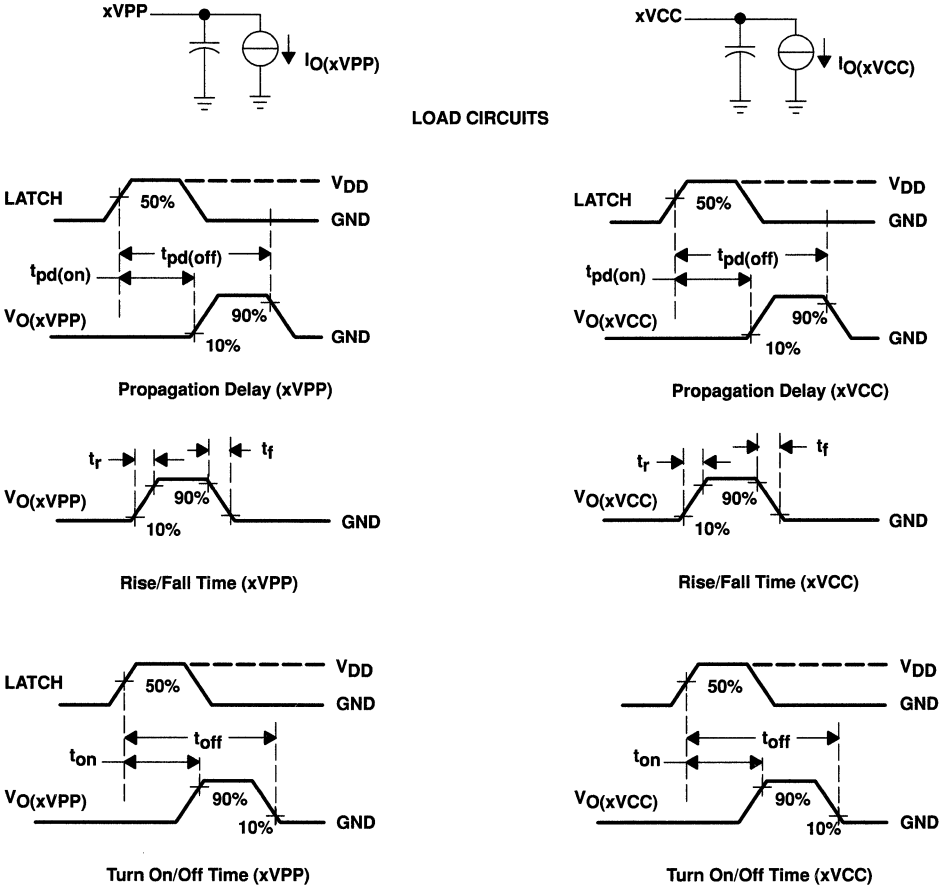
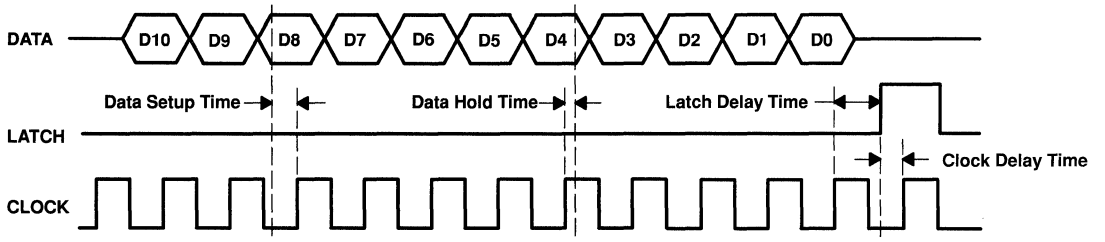


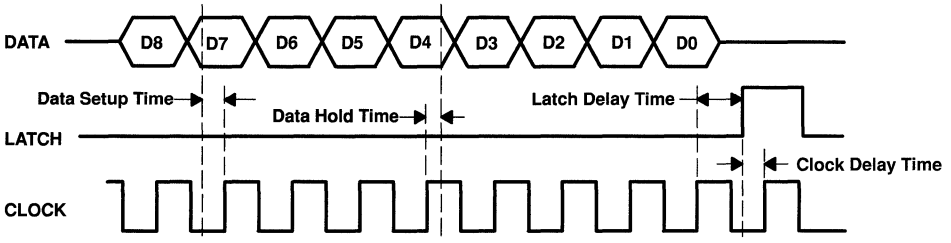
Figure 1. Test Circuits and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE: Data is clocked in on the positive edge of the clock. The positive edge of the latch signal should occur before the next positive edge of the clock. For definition of D0 to D10, see the control logic table.

Figure 2. Serial-Interface Timing for Independent xVPP Switching When MODE = 5 V or 3.3 V



NOTE: Data is clocked in on the positive edge of the clock. The positive edge of the latch signal should occur before the next positive edge of the clock. For definition of D0 to D8, see the control logic table.

Figure 3. Serial-Interface Timing When MODE = 0 V or Floating

Table of Timing Diagrams†

	FIGURE
Short-circuit current response, short applied to powered-on 5-V xVCC switch output	4
Short-circuit current response, short applied to powered-on 12-V xVPP switch output	5
$\overline{OC}$ response with ramped load on 5-V xVCC switch output	6
$\overline{OC}$ response with ramped load on 12-V xVPP switch output	7

† Timing tests are conducted at free-air temperature, $V_{I(5V)}$ = 5 V, $V_{I(3.3V)}$ = 3.3 V, $V_{I(12V)}$ = 12 V, C_L = 0.1 µF on each output, $\overline{STBY}$ floating.

PARAMETER MEASUREMENT INFORMATION

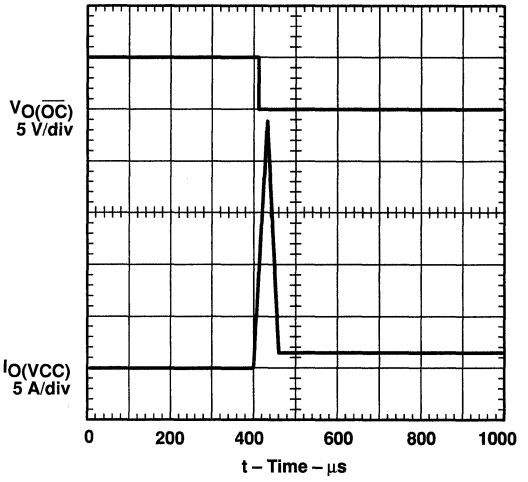


Figure 4. Short-Circuit Response, Short Applied to Powered-on 5-V xVCC-Switch Output

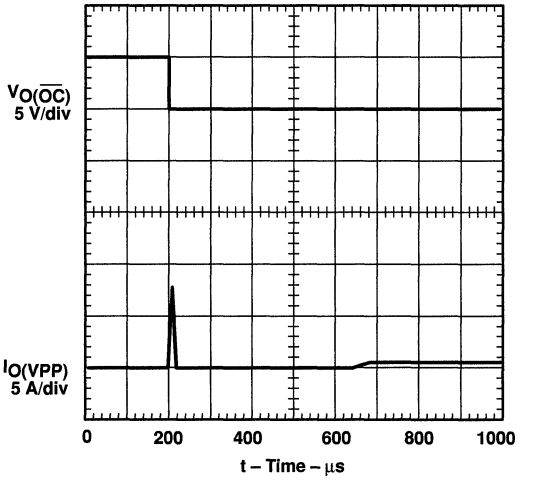


Figure 5. Short-Circuit Response, Short Applied to Powered-on 12-V xVPP-Switch Output

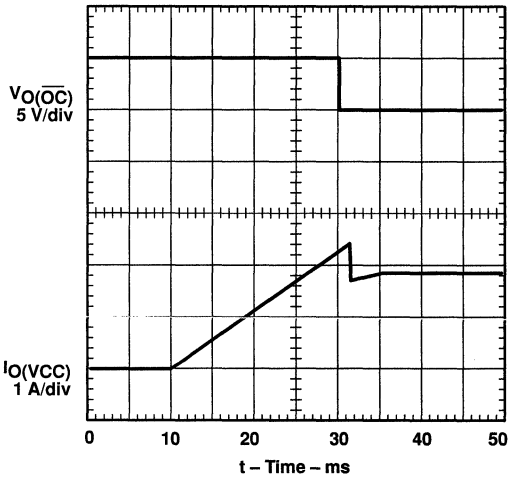


Figure 6. $\overline{OC}$ Response With Ramped Load on 5-V xVCC-Switch Output

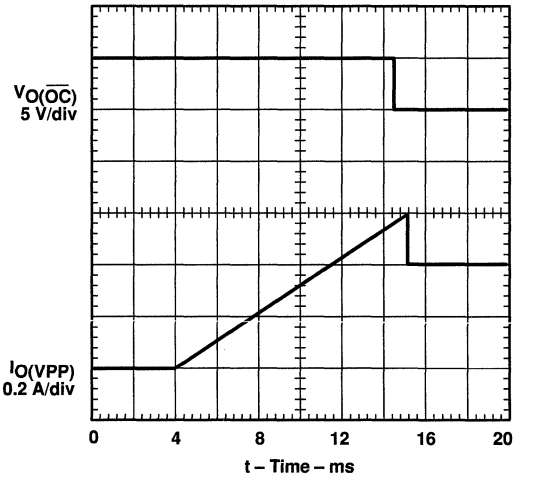


Figure 7. $\overline{OC}$ Response With Ramped Load on 12-V xVPP-Switch Output

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
$t_{pd(on)}$	Turnon propagation delay time, 3.3-V xVCC switch	vs Load capacitance	8
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$t_{pd(off)}$	Turnoff propagation delay time, 5-V xVCC switch	vs Load capacitance	11
$t_{pd(on)}$	Turnon propagation delay time, 12-V xVPP switch	vs Load capacitance	12
$t_{pd(off)}$	Turnoff propagation delay time, 12-V xVPP switch	vs Load capacitance	13
t_r	Rise time, 3.3-V xVCC switch	vs Load capacitance	14
t_f	Fall time, 3.3-V xVCC switch	vs Load capacitance	15
t_r	Rise time, 5-V xVCC switch	vs Load capacitance	16
t_f	Fall time, 5-V xVCC switch	vs Load capacitance	17
t_r	Rise time, 12-V xVPP switch	vs Load capacitance	18
t_f	Fall time, 12-V xVPP switch	vs Load capacitance	19
I_I	Input current at $V_{O(xVCC)} = V_{O(xVPP)}$ =3.3 V	vs Junction temperature	20
	Input current at $V_{O(xVCC)} = V_{O(xVPP)}$ =5 V	vs Junction temperature	21
	Input current at $V_{O(xVCC)}$ = 5 V, $V_{O(xVPP)}$ =12 V	vs Junction temperature	22
$r_{DS(on)}$	Static drain-source on-state resistance, 3.3-V xVCC switch ($V_{I(5V)}$=0)	vs Junction temperature	23
	Static drain-source on-state resistance, 3.3-V xVCC switch	vs Junction temperature	24
	Static drain-source on-state resistance, 5-V xVCC switch	vs Junction temperature	25
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$V_{IO(xVCC)}$	DC input-to-output voltage (drop), 3.3-V xVCC switch ($V_{I(5V)}$=0)	vs Load current	27
	DC input-to-output voltage (drop), 3.3-V xVCC switch	vs Load current	28
	DC input-to-output voltage (drop), 5-V xVCC switch	vs Load current	29
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I_{OS}	Short-circuit current limit, 3.3-V xVCC switch	vs Junction temperature	31
	Short-circuit current limit, 5-V xVCC switch	vs Junction temperature	32
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NOTE: Electrical characteristics tests are conducted at $V_{I(5V)}$ = 5 V, $V_{I(3.3V)}$ = 3.3 V, $V_{I(12V)}$ = 12 V, C_L = 0.1 µF on each output, $\overline{STBY}$ floating (unless otherwise noted on Figures).

TYPICAL CHARACTERISTICS

TURNON PROPAGATION DELAY TIME,
3.3-V xVCC SWITCH
vs
LOAD CAPACITANCE

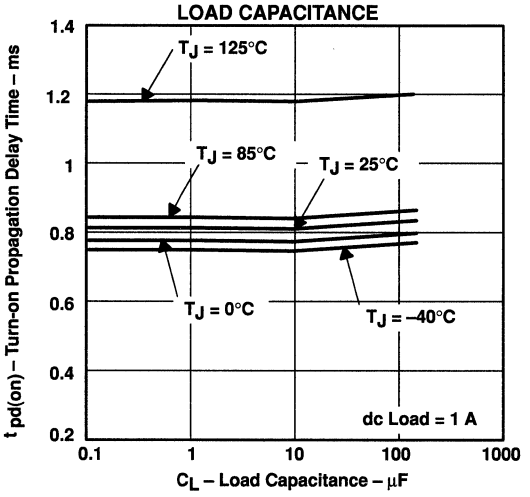


Figure 8

TURNOFF PROPAGATION DELAY TIME,
3.3-V xVCC SWITCH
vs
LOAD CAPACITANCE

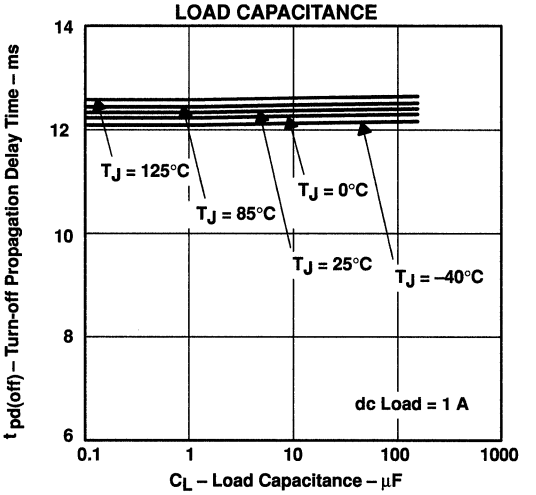


Figure 9

TURNON PROPAGATION DELAY TIME,
5-V xVCC SWITCH
vs
LOAD CAPACITANCE

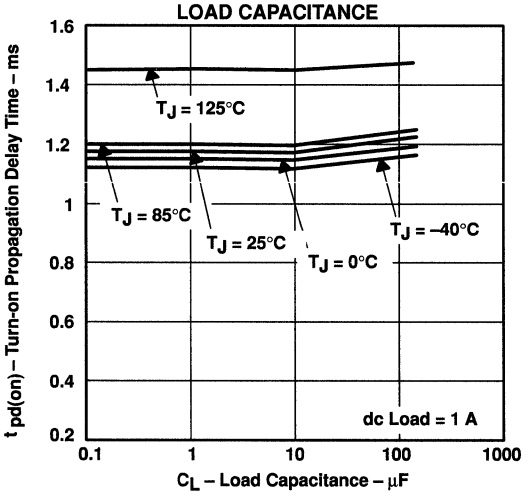


Figure 10

TURNOFF PROPAGATION DELAY TIME,
5-V xVCC SWITCH
vs
LOAD CAPACITANCE

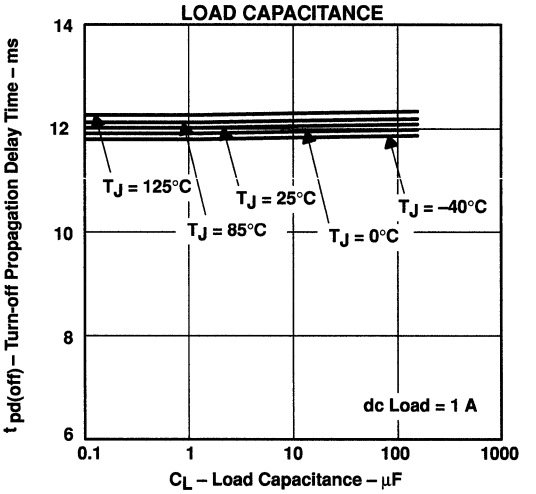


Figure 11

TYPICAL CHARACTERISTICS

TURNON PROPAGATION DELAY TIME,
12-V xVPP SWITCH
vs
LOAD CAPACITANCE

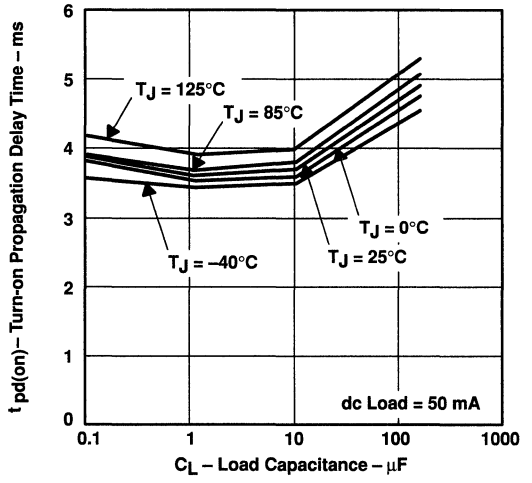


Figure 12

TURNOFF PROPAGATION DELAY TIME dc,
12-V xVPP SWITCH
vs
LOAD CAPACITANCE

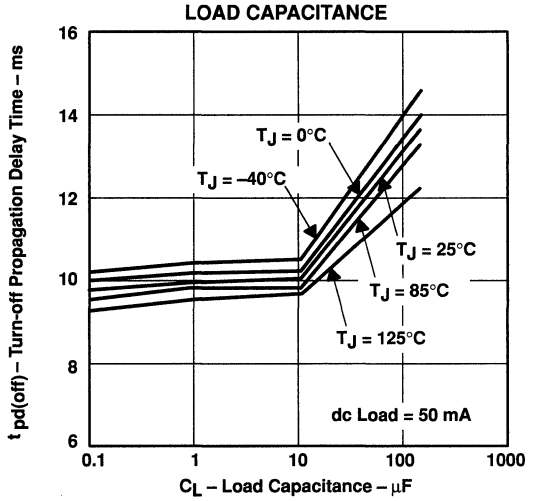


Figure 13

RISE TIME, 3.3-V xVCC SWITCH
vs
LOAD CAPACITANCE

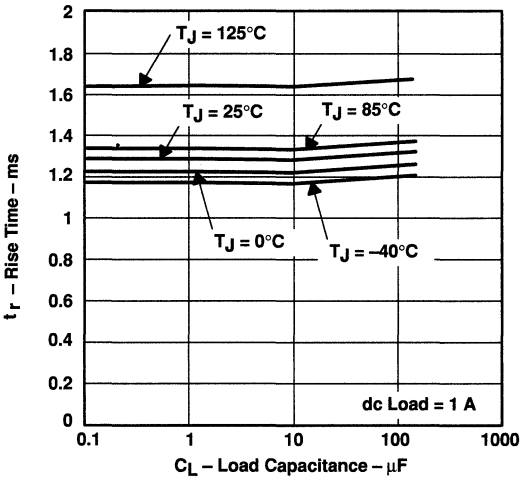


Figure 14

FALL TIME, 3.3-V xVCC SWITCH
vs
LOAD CAPACITANCE

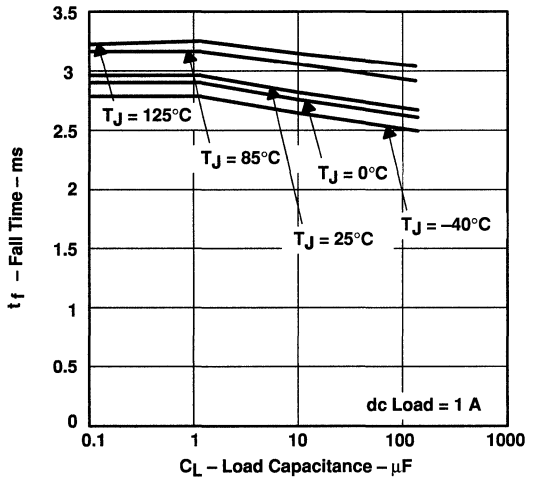


Figure 15

TYPICAL CHARACTERISTICS

RISE TIME, 5-V xVCC SWITCH
vs
LOAD CAPACITANCE

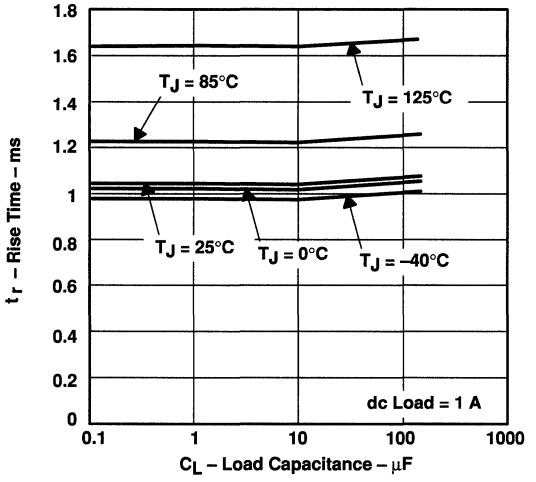


Figure 16

FALL TIME, 5-V xVCC SWITCH
vs
LOAD CAPACITANCE

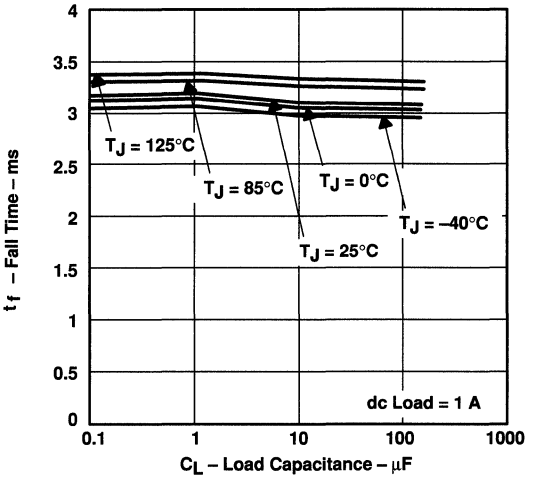


Figure 17

RISE TIME, 12-V xVPP SWITCH
vs
LOAD CAPACITANCE

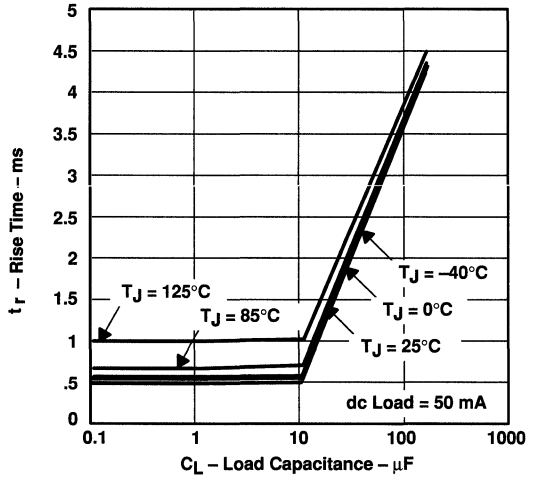


Figure 18

FALL TIME, 12-V xVPP SWITCH
vs
LOAD CAPACITANCE

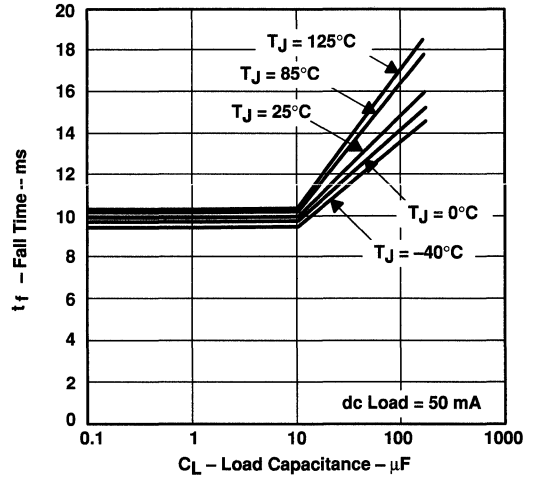


Figure 19

TYPICAL CHARACTERISTICS

INPUT CURRENT AT $V_{I(xVCC)} = V_{I(xVPP)} = 3.3$ V
vs
JUNCTION TEMPERATURE

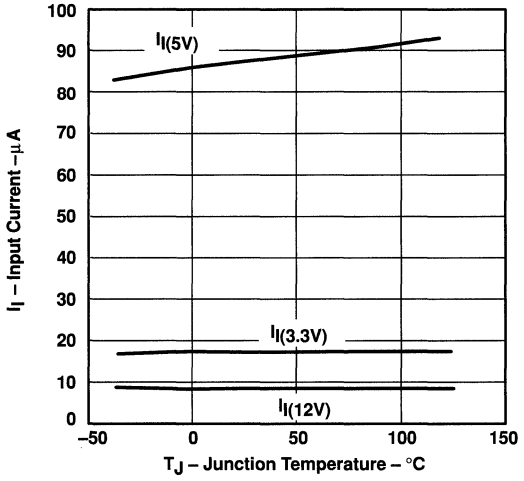


Figure 20

INPUT CURRENT AT $V_{I(xVCC)} = V_{I(xVPP)} = 5$ V
vs
JUNCTION TEMPERATURE

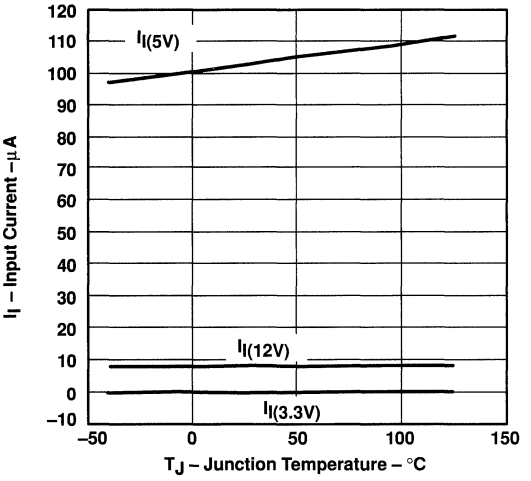


Figure 21

INPUT CURRENT AT $V_{I(xVCC)} = 5$ V, $V_{I(xVPP)} = 12$ V
vs
JUNCTION TEMPERATURE

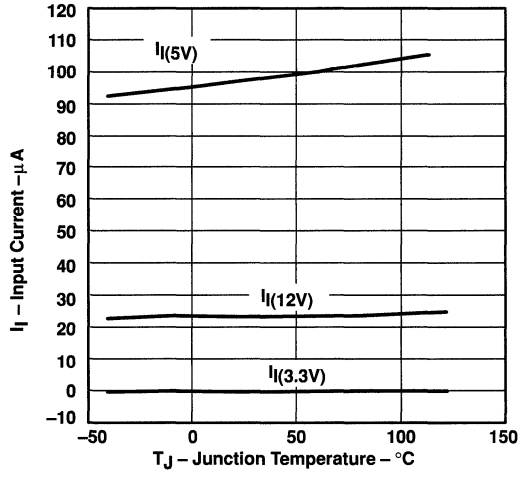


Figure 22

STATIC DRAIN-SOURCE ON-STATE RESISTANCE,
3.3-V xVCC SWITCH
vs
JUNCTION TEMPERATURE

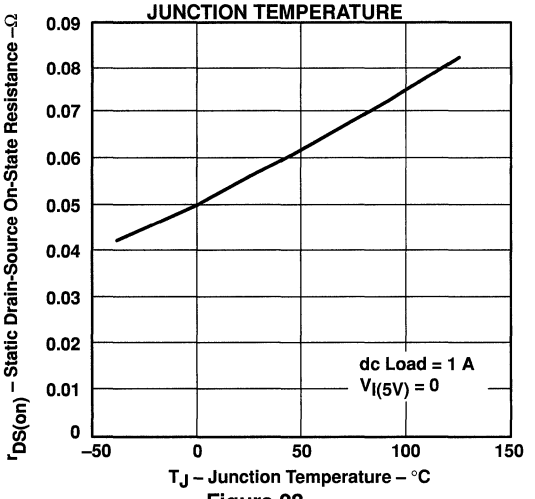


Figure 23

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE,
3.3-V xVCC SWITCH
vs
JUNCTION TEMPERATURE

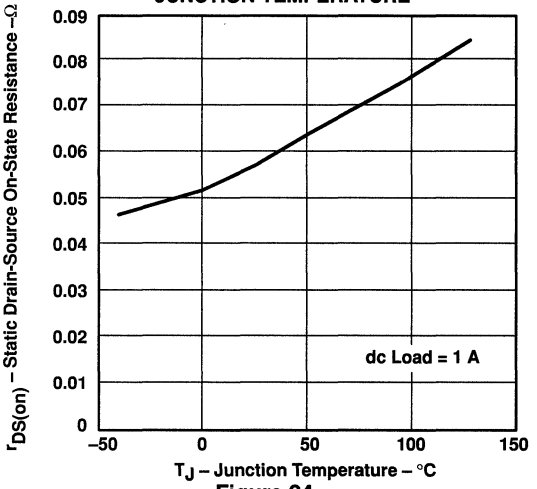


Figure 24

STATIC DRAIN-SOURCE ON-STATE RESISTANCE,
5-V xVCC SWITCH
vs
JUNCTION TEMPERATURE

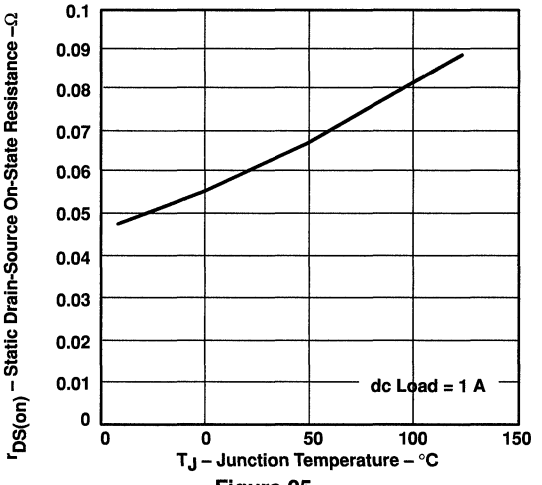


Figure 25

STATIC DRAIN-SOURCE ON-STATE RESISTANCE,
12-V xVPP SWITCH
vs
JUNCTION TEMPERATURE

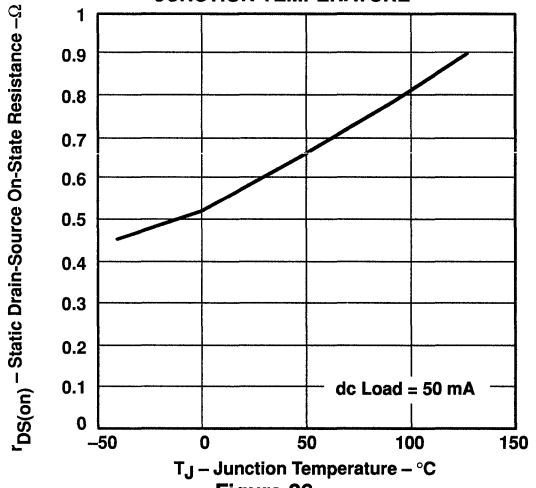


Figure 26

DC INPUT-TO-OUTPUT VOLTAGE (DROP),
3.3-V xVCC SWITCH
vs
LOAD CURRENT

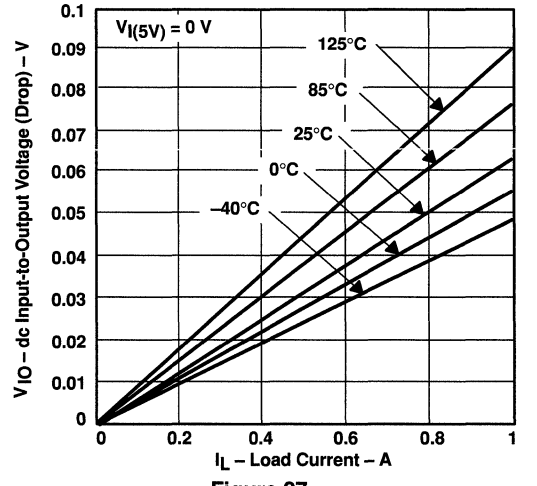


Figure 27

TYPICAL CHARACTERISTICS

DC INPUT-TO-OUTPUT VOLTAGE (DROP),
3.3-V xVCC SWITCH
vs
LOAD CURRENT

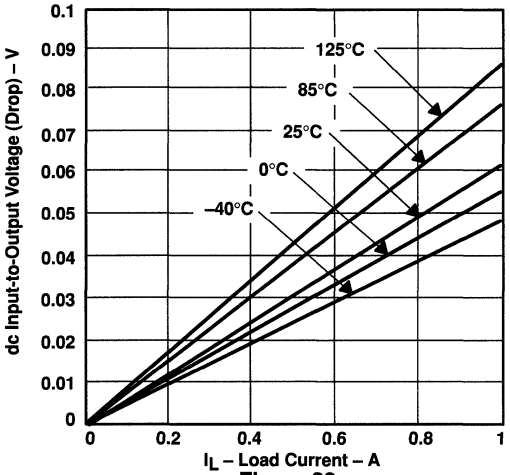


Figure 28

DC INPUT-TO-OUTPUT VOLTAGE (DROP),
5-V xVCC SWITCH
vs
LOAD CURRENT

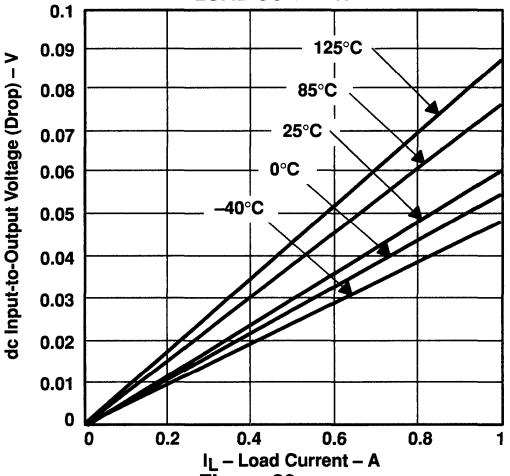


Figure 29

DC INPUT-TO-OUTPUT VOLTAGE (DROP),
12-V xVPP SWITCH
vs
LOAD CURRENT

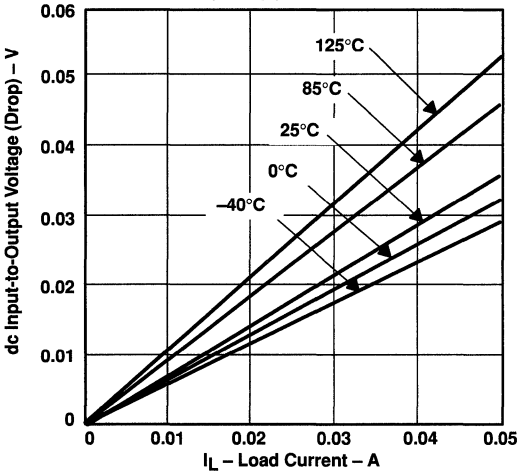


Figure 30

SHORT-CIRCUIT CURRENT LIMIT,
3.3-V xVCC SWITCH
vs
JUNCTION TEMPERATURE

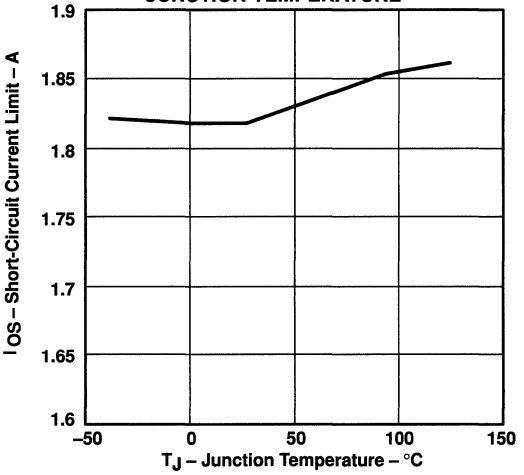


Figure 31

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT CURRENT LIMIT, 5-V xVCC SWITCH vs JUNCTION TEMPERATURE

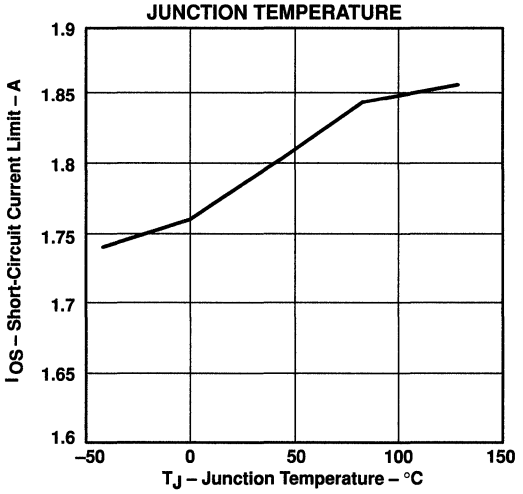


Figure 32

SHORT-CIRCUIT CURRENT LIMIT, 12-V xVPP SWITCH vs JUNCTION TEMPERATURE

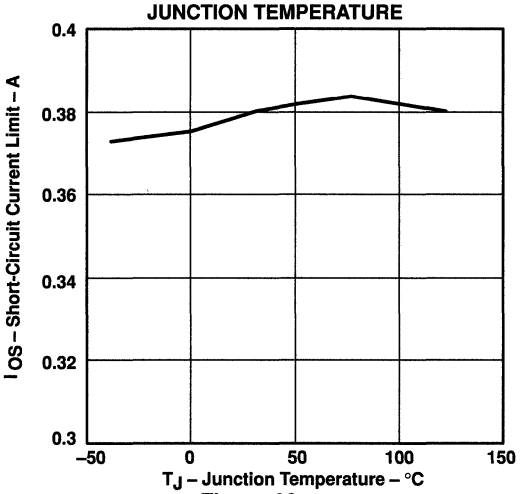


Figure 33

APPLICATION INFORMATION

overview

PC Cards were initially introduced as a means to add EEPROM (flash memory) to portable computers with limited onboard memory. The idea of add-in cards quickly took hold; modems, wireless LANs, Global Positioning Satellite System (GPS), multimedia, and hard-disk versions were soon available. As the number of PC Card applications grew, the engineering community quickly recognized the need for a standard to ensure compatibility across platforms. To this end, the PCMCIA (Personal Computer Memory Card International Association), comprising members from leading computer, software, PC Card, and semiconductor manufacturers, was established. One key goal was to realize the plug-and-play concept. Cards and hosts from different vendors should be compatible or able to communicate with one another transparently.

PC Card power specification

System compatibility also means power compatibility. The most current set of specifications (PC Card Standard) set forth by the PCMCIA committee states that power is to be transferred between the host and the card through eight of the 68 terminals of the PC Card connector. This power interface consists of two V_{CC}, two V_{pp}, and four ground terminals. Multiple V_{CC} and ground terminals minimize connector terminal and line resistance. The two V_{pp} terminals were originally specified as separate signals, but are commonly tied together in the host to form a single node to minimize voltage losses. Card primary power is supplied through the V_{CC} terminals; flash-memory programming and erase voltage is supplied through the V_{pp} terminals.

APPLICATION INFORMATION

designing for voltage regulation

The current PCMCIA specification for output voltage regulation, $V_{O(reg)}$, of the 5-V output is 5% (250 mV). In a typical PC power-system design, the power supply has an output-voltage regulation, $V_{PS(reg)}$, of 2% (100 mV). Also, a voltage drop from the power supply to the PC Card will result from resistive losses, V_{PCB}, in the PCB traces and the PCMCIA connector. A typical design would limit the total of these resistive losses to less than 1% (50 mV) of the output voltage. Therefore, the allowable voltage drop, V_{DS}, for the TPS2216 would be the PCMCIA voltage regulation less the power supply regulation and less the PCB and connector resistive drops:

$$V_{DS} = V_{O(reg)} - V_{PS(reg)} - V_{PCB}$$

Typically, this would leave 100 mV for the allowable voltage drop across the 5-V switch. The specification for output voltage regulation of the 3.3-V output is 300 mV; so, using the same equation by deducting the voltage drop percentages (2%) for power-supply regulation and PCB resistive loss (1%), the allowable voltage drop for the 3.3-V switch is 200 mV. The voltage drop is the output current multiplied by the switch resistance of the TPS2216. Therefore, the maximum output current, I_O max, that can be delivered to the PC Card in regulation is the allowable voltage drop across the IC, divided by the output-switch resistance.

$$I_O max = \frac{V_{DS}}{r_{DS(on)}}$$

The xVCC outputs can deliver 1 A continuously at 5 V and 3.3 V within regulation over the operating temperature range. The xVPP outputs of the IC can deliver 200 mA continuously.

overcurrent and overtemperature protection

PC Cards are inherently subject to damage that can result from mishandling. Host systems require protection against short-circuited cards that could lead to power-supply or PCB trace damage. Even systems robust enough to withstand a short circuit would still undergo rapid battery discharge into the damaged PC Card, resulting in the rather sudden and unacceptable loss of system power. Most hosts include fuses for protection. However, the reliability of fused systems is poor, as blown fuses require troubleshooting and repair, usually by the manufacturer.

The TPS2216 takes a two-pronged approach to overcurrent protection, which is designed to activate if an output is shorted or when an overcurrent condition is present when switches are powered up. First, instead of fuses, sense FETs monitor each of the xVCC and xVPP power outputs. Unlike sense resistors or polyfuses, these FETs do not add to the series resistance of the switch; therefore voltage and power losses are reduced. Overcurrent sensing is applied to each output separately. Excessive current generates an error signal that limits the output current of only the affected output, preventing damage to the host. Each xVCC output overcurrent limits from 1 A to 2.2 A, typically around 1.6 A; the xVPP outputs limit from 250 mA to 500 mA, typically around 375 mA.

Second, when an overcurrent condition is detected, the TPS2216 asserts an active low $\overline{OC}$ signal that can be monitored by the microprocessor or controller to initiate diagnostics and/or send the user a warning message. In the event that an overcurrent condition persists, causing the IC to exceed its maximum junction temperature, thermal-protection circuitry activates. This shuts down all power outputs until the device cools to within a safe operating region, which is ensured by a thermal shutdown hysteresis.

APPLICATION INFORMATION

12-V supply not required

Many PC Card switches use the externally supplied 12 V to power gate drive and other chip functions; this requires that power be present at all times. The TPS2216 offers considerable power savings by using an internal charge pump to generate the required higher gate drive voltages from the 5-V or 3.3-V power supplies. Therefore, the external 12-V supply can be disabled except when needed for flash-memory functions, thereby extending battery lifetime. Additional power savings are realized by the IC during shutdown mode, in which quiescent current drops to a maximum of 1 µA.

3.3-V low-voltage mode

The TPS2216 will operate in 3.3-V low-voltage mode when 3.3 V is the only available input voltage ($V_{I(5V)}$ = 0, $V_{I(12V)}$ = 0). This feature allows host and PC Cards to be operated in low-power 3.3-V-only modes such as sleep modes. Note that in this operation mode, the IC will derive its bias current from the 3.3-V input pin and can only provide 3.3 V to the outputs.

voltage transitioning requirement

PC Cards are migrating from 5 V to 3.3 V to minimize power consumption, optimize board space, and increase logic speeds. The TPS2216 meets all combinations of power delivery as currently defined in the PCMCIA standard. The latest protocol accommodates mixed 3.3-V/5-V systems by first powering the card with 5 V, then polling it to determine its 3.3-V compatibility. The PCMCIA specification requires that the capacitors on 3.3-V-compatible cards be discharged to below 0.8 V before applying 3.3-V power. This action ensures that sensitive 3.3-V circuitry is not subjected to any residual 5-V charge and functions as a power reset. PC Card specification requires that V_{CC} be discharged within 100 ms. PC Card resistance can not be relied on to provide a discharge path for voltages stored on PC Card capacitance because of possible high-impedance isolation by power-management schemes. The TPS2216 includes discharge transistors on all xVCC and xVPP outputs to meet the specification requirement.

shutdown mode

In the shutdown mode, which can be controlled by bit D8 of the input serial DATA word, each of the xVCC and xVPP outputs is forced to a high-impedance state. In this mode, the chip quiescent current is limited to 1 µA or less to conserve battery power.

standby mode

The TPS2216 can be put in standby mode by pulling $\overline{\text{STBY}}$ low to conserve power during low-power operation. In this mode, all of the power outputs (xVCC and xVPP) will have a nominal current limit of 50 mA. $\overline{\text{STBY}}$ has an internal 150-kΩ pullup resistor. The output-switch status of the device must be set, allowing the output capacitors to charge, prior to enabling the standby mode. Changing the setting of the output switches with the device in standby mode may cause an overcurrent response to be generated.

mode

The mode pin programs the switches in either TPS2216 or TPS2206 mode. An internal 150-kΩ pulldown resistor is connected to the pin. Floating or pulling the mode pin low sets the switches in TPS2206 mode; pulling the mode pin high sets the switches in TPS2216 mode. In TPS2206 mode, xVPP outputs are dependent on xVCC outputs. In TPS2216 mode, xVPP is programmed independent of xVCC. Refer to TPS2216 control-logic tables for more information.

APPLICATION INFORMATION

power supply considerations

The TPS2216 has multiple pins for each of its 3.3-V and 5-V power inputs and for the switched xVCC outputs. Any individual pin can conduct the rated input or output current. Unless all pins are connected in parallel, the series resistance is higher than that specified, resulting in increased voltage drops and less power. It is recommended that all input and output power pins be paralleled for optimum operation. Because the two 12-V pins are not internally connected, they must be tied together externally.

To increase the noise immunity of the TPS2216, the power-supply inputs should be bypassed with a 1-μF electrolytic or tantalum capacitor paralleled by a 0.047-μF to 0.1-μF ceramic capacitor. It is strongly recommended that the switched outputs be bypassed with a 0.1-μF (or larger) ceramic capacitor; doing so improves the immunity of the IC to electrostatic discharge (ESD). Care should be taken to minimize the inductance of PCB traces between the IC and the load. High switching currents can produce large negative voltage transients, which forward biases substrate diodes, resulting in unpredictable performance. Similarly, no pin should be taken, or allowed to fall, below –0.3 V.

RESET and $\overline{\text{RESET}}$ inputs

To ensure that cards are in a known state after power brownouts or system initialization, the PC Cards should be reset at the same time as the host by applying low impedance paths from xVCC and xVPP terminals to ground. A low-impedance output state allows discharging of residual voltage remaining on PC Card filter capacitance, permitting the system (host and PC Cards) to be powered up concurrently. The active-high RESET or active low $\overline{\text{RESET}}$ input will close internal switches S1, S4, S7, and S11 with all other switches left open. The TPS2216 remains in the low-impedance output state until the signal is deasserted and further data is clocked in and latched. The input serial data can not be latched during Reset mode. RESET and $\overline{\text{RESET}}$ are provided for direct compatibility with systems that use either an active-low or active-high reset voltage supervisor. The RESET pin has an internal 150-kΩ pulldown resistor and the $\overline{\text{RESET}}$ pin has an internal 150-kΩ pullup resistor. The device will be reset automatically when powered up.

calculating junction temperature

The switch resistance, $r_{DS(on)}$, is dependent on the junction temperature, T_J, of the die. The junction temperature is dependent on both $r_{DS(on)}$ and the current through the switch. To calculate T_J, first find $r_{DS(on)}$ from Figures 23 through 26, using an initial temperature estimate about 50°C above ambient. Then calculate the power dissipation for each switch, using the formula:

$$P_D = r_{DS(on)} \times I^2$$

Next, sum the power dissipation of all switches and calculate the junction temperature:

$$T_J = \left(\sum P_D \times R_{\theta JA}\right) + T_A$$

Where:

$R_{\theta JA}$ is the inverse of the derating factor given in the dissipation rating table.

Compare the calculated junction temperature with the initial temperature estimate. If the temperatures are not within a few degrees of each other, recalculate using the calculated temperature as the initial estimate.

logic inputs and outputs

The serial interface consists of DATA, CLOCK, and LATCH leads. The data is clocked in on the positive edge of the clock (see Figures 2 and 3). The 11-bit (D0–D10) serial data word is loaded during the positive edge of the latch signal. The positive edge of the latch signal should occur before the next positive edge of the clock occurs.

APPLICATION INFORMATION

logic inputs and outputs (continued)

The TPS2216 serial interfaces are compatible with serial-interface PCMCIA controllers and current PCMCIA and Japan Electronic Industry Development Association (JEIDA) standards.

An overcurrent output ($\overline{OC}$) is provided to indicate an overcurrent or overtemperature condition in any of the xVCC and xVPP outputs as previously discussed.

TPS2216 control logic

TPS2216 mode (MODE pulled high)

xVPP

	AVPP CONTROL SIGNALS			OUTPUT V_AVPP	BVPP CONTROL SIGNALS				OUTPUT V_BVPP
D8 ($\overline{SHDN}$)	D0	D1	D9		D8 ($\overline{SHDN}$)	D4	D5	D10	
1	0	0	X	0 V	1	0	0	X	0 V
1	0	1	0	3.3 V	1	0	1	0	3.3 V
1	0	1	1	5 V	1	0	1	1	5 V
1	1	0	X	12 V	1	1	0	X	12 V
1	1	1	X	Hi-Z	1	1	1	X	Hi-Z
0	X	X	X	Hi-Z	0	X	X	X	Hi-Z

xVCC

	AVCC CONTROL SIGNALS		OUTPUT V_AVCC	BVCC CONTROL SIGNALS			OUTPUT V_BVCC
D8 ($\overline{SHDN}$)	D3	D2		D8 ($\overline{SHDN}$)	D6	D7	
1	0	0	0 V	1	0	0	0 V
1	0	1	3.3 V	1	0	1	3.3 V
1	1	0	5 V	1	1	0	5 V
1	1	1	0 V	1	1	1	0 V
0	X	X	Hi-Z	0	X	X	Hi-Z

TPS2206 mode (MODE floating or pulled low)

xVPP

	AVPP CONTROL SIGNALS		OUTPUT V_AVPP	BVPP CONTROL SIGNALS			OUTPUT V_BVPP
D8 ($\overline{SHDN}$)	D0	D1		D8 ($\overline{SHDN}$)	D4	D5	
1	0	0	0 V	1	0	0	0 V
1	0	1	V_AVCC	1	0	1	V_BVCC
1	1	0	12 V	1	1	0	12 V
1	1	1	Hi-Z	1	1	1	Hi-Z
0	X	X	Hi-Z	0	X	X	Hi-Z

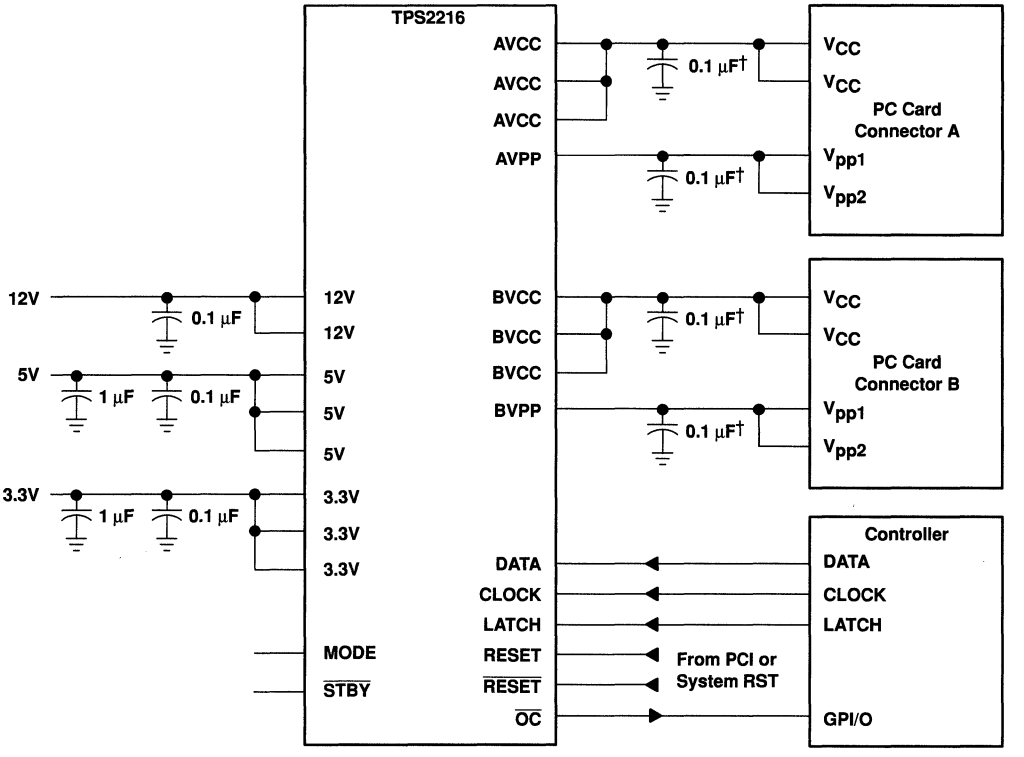
xVCC

	AVCC CONTROL SIGNALS		OUTPUT V_AVCC	BVCC CONTROL SIGNALS			OUTPUT V_BVCC
D8 ($\overline{SHDN}$)	D3	D2		D8 ($\overline{SHDN}$)	D6	D7	
1	0	0	0 V	1	0	0	0 V
1	0	1	3.3 V	1	0	1	3.3 V
1	1	0	5 V	1	1	0	5 V
1	1	1	0 V	1	1	1	0 V
0	X	X	Hi-Z	0	X	X	Hi-Z

APPLICATION INFORMATION

ESD protections (see Figure 34)

All TPS2216 inputs and outputs incorporate ESD-protection circuitry designed to withstand a 2-kV human-body-model discharge as defined in MIL-STD-883C, Method 3015. The xVCC and xVPP outputs can be exposed to potentially higher discharges from the external environment through the PC Card connector. Bypassing the outputs with 0.1-μF capacitors protects the devices from discharges up to 10 kV.



† Maximum recommended output capacitance for xVCC is 220 μF and for xVPP is 10 μF without $\overline{OC}$ glitch when switches are powered on.

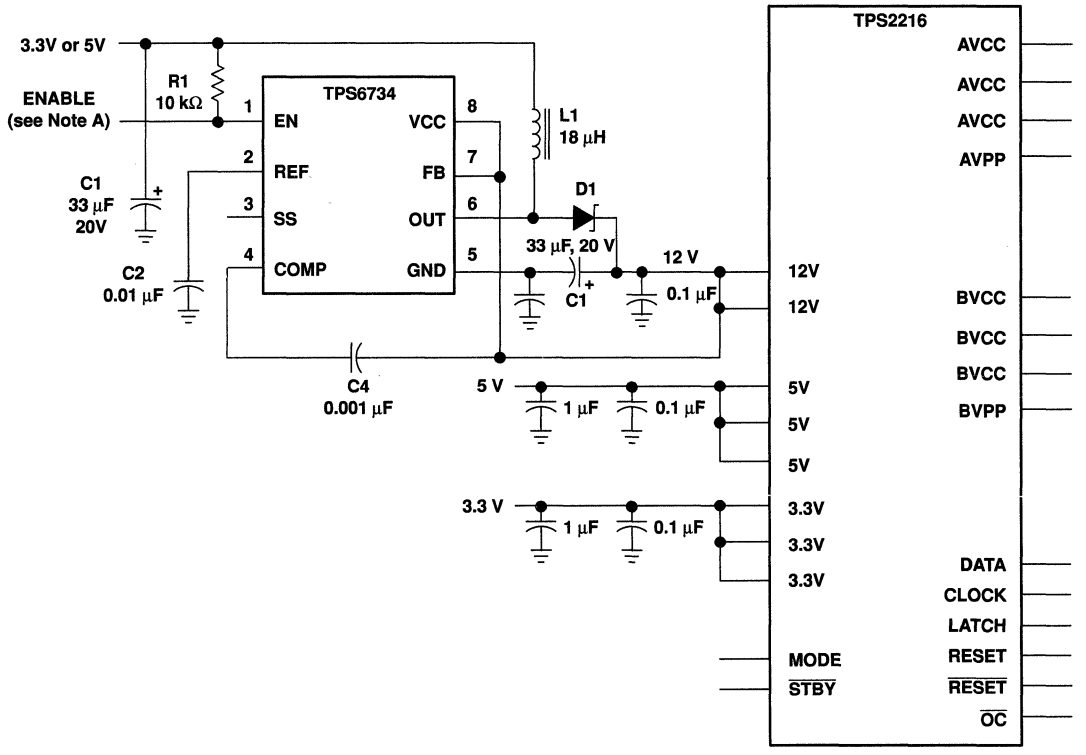
Figure 34. Detailed Interconnections and Capacitor Recommendations

APPLICATION INFORMATION

12-V flash memory supply

The TPS6734 is a fixed 12-V output boost converter capable of delivering 120 mA from inputs as low as 2.7 V. The device is pin-for-pin compatible with the MAX734 regulator and offers the following advantages: lower supply current, wider operating input-voltage range, and higher output currents. As shown in Figure 35, the only external components required are: an inductor, a Schottky rectifier, an output filter capacitor, an input filter capacitor, and a small capacitor for loop compensation. The entire converter occupies less than 0.7 in^2 of PCB space when implemented with surface-mount components. An enable input is provided to shut the converter down and reduce the supply current to 3 μA when 12 V is not needed.

The TPS6734 is a 170-kHz current-mode PWM (pulse-width modulation) controller with an n-channel MOSFET power switch. Gate drive for the switch is derived from the 12-V output after start-up to minimize the die area needed to realize the 0.7-Ω MOSFET and improve efficiency at input voltages below 5 V. Soft start is accomplished with the addition of one small capacitor. A 1.22-V reference (pin 2) is brought out for external use. For additional information, see the TPS6734 data sheet (SLVS127).



NOTE A. The enable terminal can be tied to a general-purpose I/O terminal on the PCMCIA controller or tied high.

Figure 35. TPS2216 with TPS6734 12-V, 120-mA Supply

- Drive Capability and Output Counts
  - 80 mA (Current Sink) × 16 Bits
  - 120 mA (Current Sink) × 8 Bits
- Constant Current Output Range
  - 5 mA to 80 mA/10 mA to 120 mA (Selectable by MODE Terminal) (Current Value Setting for All Output Terminals Using External Resistor and Internal Brightness Control Register)
- Constant Current Accuracy
  - ±4% (Maximum Error Between Bits)
- Voltage Applied to Constant Current Output Terminals
  - Minimum 0.4 V (Output Current 5 mA to 40 mA
  - Minimum 0.7 V (Output Current 40 mA to 80 mA
- 256 Gray Scale Display
  - Pulse Width Control 256 Steps
- Brightness Adjustment
  - Output Current Adjustment for 32 Steps (Adjustment for Brightness Deviation Between LEDs)
  - 8 Steps Brightness Control by 8 Times Speed Gray Scale Control Clock (Brightness Adjustment for Panel)
- Voltage Monitor
  - Monitor Voltage on Constant Current Output Terminals (Detect LED Disconnection and Short Circuit)
- Output Signal Check
  - Check Output Signal When Protection Circuit is Operating
- Data Output Timing Selectable
  - Select Data Output Timing for Shift Register Relative to Clock
- Data Input
  - Clock Synchronized 8 Bit Parallel Input (Schmitt Triggered Input)
- Data Output
  - Clock Synchronized 8 Bit Parallel Output (3-State Output)
- Input Signal Level: CMOS Level
- Power Supply Voltage: 4.5 V to 5.5 V
- Maximum Output Voltage: 17 V (Max)
- Data Transfer Rate: 15 MHz (Max)
- Gray Scale Clock Frequency: 8 MHz (Max)
- Operating Free-Air Temperature Range
  - –20°C to 85°C
- Protection
  - WDT Function (Turn Output Off When Scan Signal Stopped)
  - TSD Function (Turn Output Off When Junction Temperature Exceeds Limit)
- Package: 100 Pin HTQFP (P_D = 4.7 W, T_A = 25°C

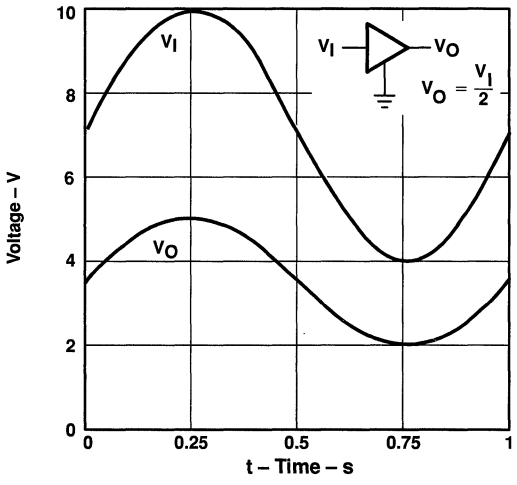
PRODUCT PREVIEW

description

The TLC5904 is a constant current driver incorporating shift register, data latch, constant current circuitry with current value adjustable, and 256 gray scale display using pulse width control. The output current can be selected as maximum 80 mA with 16 bits or 120 mA with 8 bit, and the current value of constant current output can be set by one external register. After this device is mounted on PCB, the brightness deviation between LEDs (ICs) can be adjusted by external data input, and the brightness control for panel can be accomplished by brightness adjustment circuitry. Also, the device incorporates the voltage monitor circuitry used for LED failure detection to monitor constant current output. Moreover, the device incorporates WDT (watch-dog timer) circuitry, which turns constant current output off when scan signal stopped at dynamic scanning operation, and thermal shutdown (TSD) circuitry, which turns constant current output off when the junction temperature exceeds the limit.

- 1/2 V_I Virtual Ground for Analog Systems
- Self-Contained 3-terminal TO-226AA Package
- Micropower Operation . . . 170 μA Typ, V_I = 5 V
- Wide V_I Range . . . 4 V to 40 V
- High Output-Current Capability
  - Source . . . 20 mA Typ
  - Sink . . . 20 mA Typ
- Excellent Output Regulation
  - −45 μV Typ at I_O = 0 to −10 mA
  - +15 μV Typ at I_O = 0 to +10 mA
- Low-Impedance Output . . . 0.0075 Ω Typ
- Noise Reduction Pin (D, JG, and P Packages Only)

INPUT/OUTPUT TRANSFER CHARACTERISTICS



description

In signal-conditioning applications utilizing a single power source, a reference voltage equal to one-half the supply voltage is required for termination of all analog signal grounds. Texas Instruments presents a precision virtual ground whose output voltage is always equal to one-half the input voltage, the TLE2426 "rail splitter."

The unique combination of a high-performance, micropower operational amplifier and a precision-trimmed divider on a single silicon chip results in a precise V_O/V_I ratio of 0.5 while sinking and sourcing current. The TLE2426 provides a low-impedance output with 20 mA of sink and source capability while drawing less than 280 μA of supply current over the full input range of 4 V to 40 V. A designer need not pay the price in terms of board space for a conventional signal ground consisting of resistors, capacitors, operational amplifiers, and voltage references. The performance and precision of the TLE2426 is available in an easy-to-use, space saving, 3-terminal LP package. For increased performance, the optional 8-pin packages provide a noise-reduction pin. With the addition of an external capacitor (C_{NR}), peak-to-peak noise is reduced while line ripple rejection is improved.

Initial output tolerance for a single 5-V or 12-V system is better than 1% with 3.6% over the full 40-V input range. Ripple rejection exceeds 12 bits of accuracy. Whether the application is for a data acquisition front end, analog signal termination, or simply a precision voltage reference, the TLE2426 eliminates a major source of system error.

AVAILABLE OPTIONS

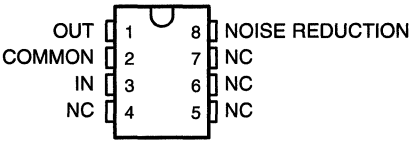
PACKAGED DEVICES					CHIP FORM (Y)
T_A	SMALL OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC (LP)	PLASTIC DIP (P)	
0°C to 70°C	TLE2426CD	—	TLE2426CLP	TLE2426CP	TLE2426Y
−40°C to 85°C	TLE2426ID	—	TLE2426ILP	TLE2426IP	
−55°C to 125°C	TLE2426MD	TLE2426MJG	TLE2426MLP	TLE2426MP	

The D and LP packages are available taped and reeled in the commercial temperature range only. Add R suffix to the device type (e. g., TLC2426CDR). Chips are tested at 25°C.

description (continued)

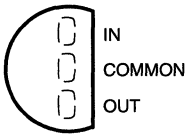
The C-suffix devices are characterized for operation from 0°C to 70°C. The I suffix devices are characterized for operation from –40°C to 85°C. The M suffix devices are characterized over the full military temperature range of –55°C to 125°C.

D, JG, OR P PACKAGE
(TOP VIEW)



NC – No internal connection

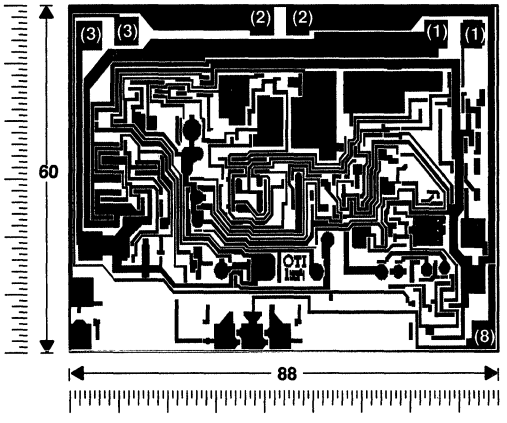
LP PACKAGE
(TOP VIEW)

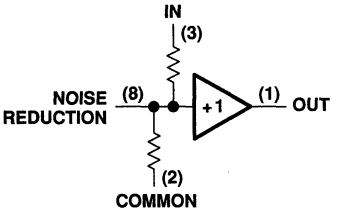


TLE2426Y chip information

This chip, properly assembled, displays characteristics similar to the TLE2426C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 MILS TYPICAL

BONDING PADS:
4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

NOTE A. Both bonding pads numbered 1, both numbered 2, and both numbered 3, must be bonded out to the corresponding functions pin.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Continuous input voltage, V_I ..... 40 V
Continuous filter trap voltage ..... 40 V
Output current, I_O ..... ±80 mA
Duration of short-circuit current at (or below) 25°C (see Note 1) ..... unlimited
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix ..... 0°C to 70°C
I suffix ..... −40°C to 85°C
M suffix ..... −55°C to 125°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or LP package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mV	5.8 mW/°C	464 mW	377 mW	145 mW
JG	1050 mV	8.4 mW/°C	672 mW	546 mW	210 mW
LP	775 mV	6.2 mW/°C	496 mW	403 mW	155 mW
P	1000 mV	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

	C SUFFIX		I SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Input voltage, V_I	4	40	4	40	4	40	V
Operating free-air temperature, T_A	0	70	−40	85	−55	125	°C

electrical characteristics at specified free-air temperature, V_I = 5 V, I_O = 0 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	TLE2426C			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 4 V		25°C	1.98	2	2.02	V
	V_I = 5 V			2.48	2.5	2.52	
	V_I = 40 V			19.8	20	20.2	
	V_I = 5 V		Full range	2.475		2.525	
Temperature coefficient of output voltage			Full range		25		ppm/°C
Supply current	No load	V_I = 5 V	25°C		170	300	μA
		V_I = 4 to 40 V	Full range			400	
Output voltage regulation (sourcing current)‡	I_O = 0 to –10 mA		25°C		–45	±160	μV
			Full range			±250	
	I_O = 0 to –20 mA		25°C		–150	±450	
Output voltage regulation (sinking current)‡	I_O = 0 to 10 mA		25°C		15	±160	μV
			Full range			±250	
	I_O = 0 to 20 mA		25°C		65	±235	
Output impedance			25°C		7.5	22.5	mΩ
Noise-reduction impedance			25°C		110		kΩ
Short-circuit current	Sinking current,	V_O = 5 V	25°C		26		mA
	Sourcing current,	V_O = 0			–47		
Output noise voltage, rms	f = 10 Hz to 10 kHz	C_{NR} = 0	25°C		120		μV
		C_{NR} = 1 μF			30		
Output voltage current step response	V_O to 0.1%, I_O = ±10 mA	C_L = 0	25°C		290		μs
		C_L = 100 pF			275		
	V_O to 0.01%, I_O = ±10 mA	C_L = 0	25°C		400		
		C_L = 100 pF			390		
Step response	V_I = 0 to 5 V, V_O to 0.1%	C_L = 100 pF	25°C		20		μs
	V_I = 0 to 5 V, V_O to 0.01%				160		

† Full range is 0°C to 70°C.
‡ The listed values are not production tested.

electrical characteristics at specified free-air temperature, V_I = 12 V, I_O = 0 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	TLE2426C			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 4 V		25°C	1.98	2	2.02	V
	V_I = 12 V			5.95	6	6.05	
	V_I = 40 V			19.8	20	20.2	
	V_I = 12 V		Full range	5.945		6.055	
Temperature coefficient of output voltage			Full range		35		ppm/°C
Supply current	No load	V_I = 12 V	25°C		195	300	μA
		V_I = 4 to 40 V	Full range			400	
Output voltage regulation (sourcing current)‡	I_O = 0 to −10 mA		25°C		−45	±160	μV
			Full range			±250	
	I_O = 0 to −20 mA		25°C		−150	±450	
Output voltage regulation (sinking current)‡	I_O = 0 to 10 mA		25°C		15	±160	μV
			Full range			±250	
	I_O = 0 to 20 mA		25°C		65	±235	
Output impedance			25°C		7.5	22.5	mΩ
Noise-reduction impedance			25°C		110		kΩ
Short-circuit current	Sinking current,	V_O = 12 V	25°C		31		mA
	Sourcing current,	V_O = 0			−70		
Output noise voltage, rms	f = 10 Hz to 10 kHz	C_{NR} = 0	25°C		120		μV
		C_{NR} = 1 μF			30		
Output voltage current step response	V_O to 0.1%, I_O = ±10 mA	C_L = 0	25°C		290		μs
		C_L = 100 pF			275		
	V_O to 0.01%, I_O = ±10 mA	C_L = 0	25°C		400		
		C_L = 100 pF			390		
Step response	V_I = 0 to 12 V, V_O to 0.1%	C_L = 100 pF	25°C		20		μs
	V_I = 0 to 12 V, V_O to 0.01%				120		

† Full range is 0°C to 70°C.
‡ The listed values are not production tested.

electrical characteristics at specified free-air temperature, V_I = 5 V, I_O = 0 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	TLE2426I			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 4 V		25°C	1.98	2	2.02	V
	V_I = 5 V			2.48	2.5	2.52	
	V_I = 40 V			19.8	20	20.2	
	V_I = 5 V		Full range	2.47		2.53	
Temperature coefficient of output voltage			Full range		25		ppm/°C
Supply current	No load	V_I = 5 V	25°C		170	300	µA
		V_I = 4 to 40 V	Full range			400	
Output voltage regulation (sourcing current)‡	I_O = 0 to –10 mA		25°C		–45	±160	µV
			Full range			±250	
	I_O = 0 to –20 mA		25°C		–150	±450	
Output voltage regulation (sinking current)‡	I_O = 0 to 10 mA		25°C		15	±160	µV
	I_O = 0 to 8 mA		Full range			±250	
	I_O = 0 to 20 mA		25°C		65	±235	
Output impedance			25°C		7.5	22.5	mΩ
Noise-reduction impedance			25°C		110		kΩ
Short-circuit current	Sinking current,	V_O = 5 V	25°C		26		mA
	Sourcing current,	V_O = 0			–47		
Output noise voltage, rms	f = 10 Hz to 10 kHz	C_{NR} = 0	25°C		120		µV
		C_{NR} = 1 µF			30		
Output voltage current step response	V_O to 0.1%, I_O = ±10 mA	C_L = 0	25°C		290		µs
		C_L = 100 pF			275		
	V_O to 0.01%, I_O = ±10 mA	C_L = 0	25°C		400		
		C_L = 100 pF			390		
Step response	V_I = 0 to 5 V, V_O to 0.1%	C_L = 100 pF	25°C		20		µs
	V_I = 0 to 5 V, V_O to 0.01%				160		

† Full range is –40°C to 85°C.
‡ The listed values are not production tested.

electrical characteristics at specified free-air temperature, V_I = 12 V, I_O = 0 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	TLE2426I			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 4 V		25°C	1.98	2	2.02	V
	V_I = 12 V			5.95	6	6.05	
	V_I = 40 V			19.8	20	20.2	
	V_I = 12 V		Full range	5.935		6.065	
Temperature coefficient of output voltage			Full range		35		ppm/°C
Supply current	No load	V_I = 12 V	25°C		195	300	µA
		V_I = 4 to 40 V	Full range			400	
Output voltage regulation (sourcing current)‡	I_O = 0 to –10 mA		25°C		–45	±160	µV
			Full range			±250	
	I_O = 0 to –20 mA		25°C		–150	±450	
Output voltage regulation (sinking current)‡	I_O = 0 to 10 mA		25°C		15	±160	µV
	I_O = 0 to 8 mA		Full range			±250	
	I_O = 0 to 20 mA		25°C		65	±235	
Output impedance			25°C		7.5	22.5	mΩ
Noise-reduction impedance			25°C		110		kΩ
Short-circuit current	Sinking current,	V_O = 12 V	25°C		31		mA
	Sourcing current,	V_O = 0			–70		
Output noise voltage, rms	f = 10 Hz to 10 kHz	C_{NR} = 0	25°C		120		µV
		C_{NR} = 1 µF			30		
Output voltage current step response	V_O to 0.1%, I_O = ±10 mA	C_L = 0	25°C		290		µs
		C_L = 100 pF			275		
	V_O to 0.01%, I_O = ±10 mA	C_L = 0	25°C		400		
		C_L = 100 pF			390		
Step response	V_I = 0 to 12 V, V_O to 0.1%	C_L = 100 pF	25°C		20		µs
	V_I = 0 to 12 V, V_O to 0.01%				120		

† Full range is –40°C to 85°C.
‡ The listed values are not production tested.

electrical characteristics at specified free-air temperature, V_I = 5 V, I_O = 0 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	TLE2426M			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 4 V		25°C	1.98	2	2.02	V
	V_I = 5 V			2.48	2.5	2.52	
	V_I = 40 V			19.8	20	20.2	
	V_I = 5 V		Full range	2.465		2.535	
Temperature coefficient of output voltage			Full range		25		ppm/°C
Supply current	No load	V_I = 5 V	25°C		170	300	μA
		V_I = 4 to 40 V	Full range			400	
Output voltage regulation (sourcing current)‡	I_O = 0 to –10 mA		25°C		–45	±160	μV
			Full range			±250	
	I_O = 0 to –20 mA		25°C		–150	±450	
Output voltage regulation (sinking current)‡	I_O = 0 to 10 mA		25°C		15	±160	μV
	I_O = 0 to 3 mA		Full range			±250	
	I_O = 0 to 20 mA		25°C		65	±235	
Output impedance			25°C		7.5	22.5	mΩ
Noise-reduction impedance			25°C		110		kΩ
Short-circuit current	Sinking current,	V_O = 5 V	25°C		26		mA
	Sourcing current,	V_O = 0			–47		
Output noise voltage, rms	f = 10 Hz to 10 kHz	C_{NR} = 0	25°C		120		μV
		C_{NR} = 1 μF			30		
Output voltage current step response	V_O to 0.1%, I_O = ±10 mA	C_L = 0	25°C		290		μs
		C_L = 100 pF			275		
	V_O to 0.01%, I_O = ±10 mA	C_L = 0	25°C		400		
		C_L = 100 pF			390		
Step response	V_I = 0 to 5 V, V_O to 0.1%	C_L = 100 pF	25°C		20		μs
	V_I = 0 to 5 V, V_O to 0.01%				120		

† Full range is –55°C to 125°C.
‡ The listed values are not production tested.

electrical characteristics at specified free-air temperature, V_I = 12 V, I_O = 0 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A†	TLE2426M			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 4 V		25°C	1.98	2	2.02	V
	V_I = 12 V			5.95	6	6.05	
	V_I = 40 V			19.8	20	20.2	
	V_I = 12 V		Full range	5.925		6.075	
Temperature coefficient of output voltage			Full range		35		ppm/°C
Supply current	No load	V_I = 12 V	25°C		195	250	μA
		V_I = 4 to 40 V	Full range			350	
Output voltage regulation (sourcing current)‡	I_O = 0 to −10 mA		25°C		−45	±160	μV
			Full range			±250	
	I_O = 0 to −20 mA		25°C		−150	±450	
Output voltage regulation (sinking current)‡	I_O = 0 to 10 mA		25°C		15	±160	μV
	I_O = 0 to 8 mA		Full range			±250	
	I_O = 0 to 20 mA		25°C		65	±235	
Output impedance			25°C		7.5	22.5	mΩ
Noise-reduction impedance			25°C		110		kΩ
Short-circuit current	Sinking current,	V_O = 12 V	25°C		31		mA
	Sourcing current,	V_O = 0			−70		
Output noise voltage, rms	f = 10 Hz to 10 kHz	C_{NR} = 0	25°C		120		μV
		C_{NR} = 1 μF			30		
Output voltage current step response	V_O to 0.1%, I_O = ±10 mA	C_L = 0	25°C		290		μs
		C_L = 100 pF			275		
	V_O to 0.01%, I_O = ±10 mA	C_L = 0	25°C		400		
		C_L = 100 pF			390		
Step response	V_I = 0 to 12 V, V_O to 0.1%	C_L = 100 pF	25°C		12		μs
	V_I = 0 to 12 V, V_O to 0.01%				120		

† Full range is −55°C to 125°C.
‡ The listed values are not production tested.

electrical characteristics at specified free-air temperature, V_I = 5 V, I_O = 0, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TLE2426Y			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 5 V			2.5		V
Supply current	No load			170		µA
Output voltage regulation (sourcing current)†	I_O = 0 to −10 mA			−45		µV
	I_O = 0 to −20 mA			−150		
Output voltage regulation (sinking current)†	I_O = 0 to 10 mA			15		µV
	I_O = 0 to 20 mA			65		
Output impedance				7.5		mΩ
Noise-reduction impedance				110		kΩ
Short-circuit current	Sinking current,	V_O = 5 V		26		mA
	Sourcing current,	V_O = 0		−47		
Output noise voltage, rms	f = 10 Hz to 10 kHz	C_{NR} = 0		120		µV
		C_{NR} = 1 µF		30		
Output voltage current step response	V_O to 0.1%, I_O = ±10 mA	C_L = 0		290		µs
		C_L = 100 pF		275		
	V_O to 0.01%, I_O = ±10 mA	C_L = 0		400		
		C_L = 100 pF		390		
Step response	V_I = 0 to 5 V, V_O to 0.1%	C_L = 100 pF		20		µs
	V_I = 0 to 5 V, V_O to 0.01%			160		

† The listed values are not production tested.

electrical characteristics at specified free-air temperature, V_I = 12 V, I_O = 0, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TLE2426Y			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 12 V			6		V
Supply current	No load			195		µA
Output voltage regulation (sourcing current)†	I_O = 0 to −10 mA			−45		µV
	I_O = 0 to −20 mA			−150		
Output voltage regulation (sinking current)†	I_O = 0 to 3 mA			15		µV
	I_O = 0 to 20 mA			65		
Output impedance				7.5		mΩ
Noise-reduction impedance				110		kΩ
Short-circuit current	Sinking current,	V_O = 12 V		31		mA
	Sourcing current,	V_O = 0		−70		
Output noise voltage, rms	f = 10 Hz to 10 kHZ	C_{NR} = 0		120		µV
		C_{NR} = 1 µF		30		
Output voltage current, step response	V_O to 0.1%, I_O = ±10 mA	C_L = 0		290		µs
		C_L = 100 pF		275		
	V_O to 0.01%, I_O = ±10 mA	C_L = 0		400		
		C_L = 100 pF		390		
Step response	V_I = 0 to 12 V, V_O to 0.1%	C_L = 100 pF		12		µs
	V_I = 0 to 12 V, V_O to 0.01%			120		

† The listed values are not production tested.

TYPICAL CHARACTERISTICS

Table Of Graphs

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Output voltage	Distribution	1,2
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Output voltage error	vs Input voltage	4
Input bias current	vs Input voltage	5
	vs Free-air temperature	6
Output voltage regulation	vs Output current	7
Output impedance	vs Frequency	8
Short-circuit output current	vs Input voltage	9,10
	vs Free-air temperature	11,12
Ripple rejection	vs Frequency	13
Spectral noise voltage density	vs Frequency	14
Output voltage response to output current step	vs Time	15
Output voltage power-up response	vs Time	16
Output current	vs Load capacitance	17

TYPICAL CHARACTERISTICS†

DISTRIBUTION
OF
OUTPUT VOLTAGE

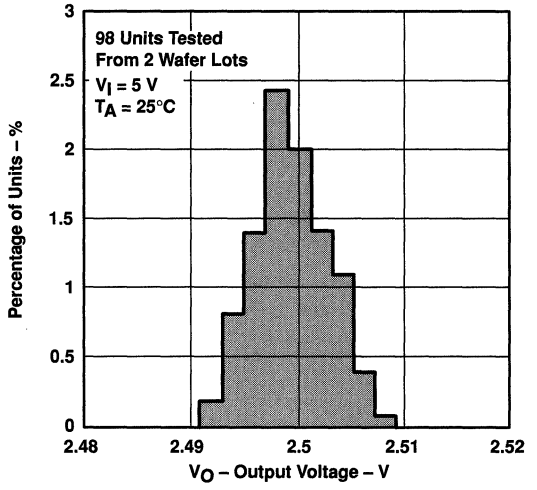


Figure 1

DISTRIBUTION
OF
OUTPUT VOLTAGE

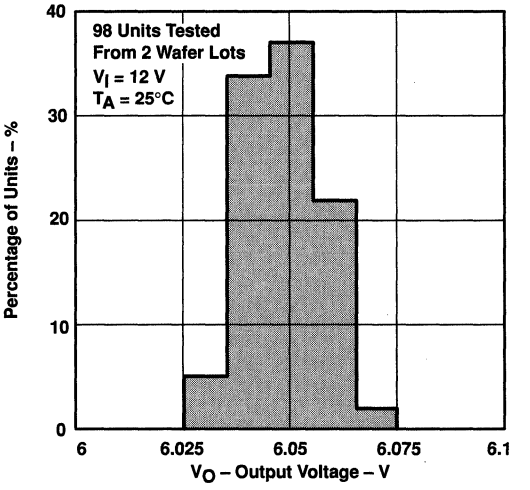


Figure 2

OUTPUT VOLTAGE CHANGE
vs
FREE-AIR TEMPERATURE

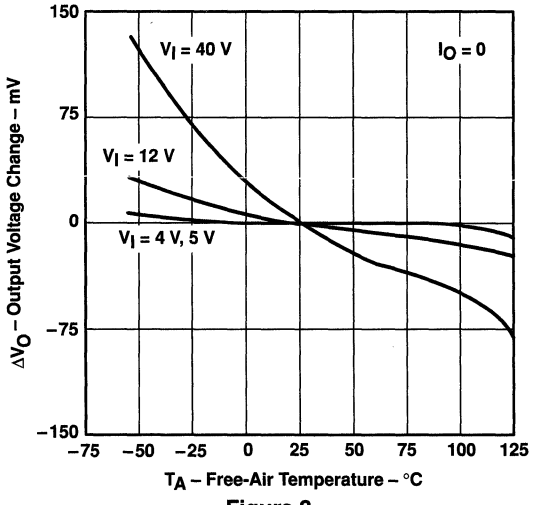


Figure 3

OUTPUT VOLTAGE ERROR
vs
INPUT VOLTAGE

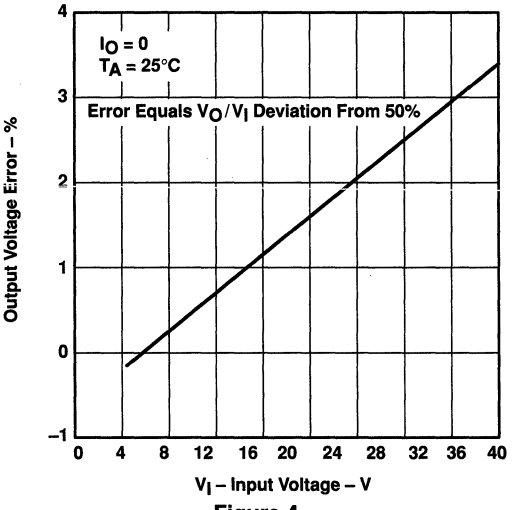


Figure 4

† Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
INPUT VOLTAGE

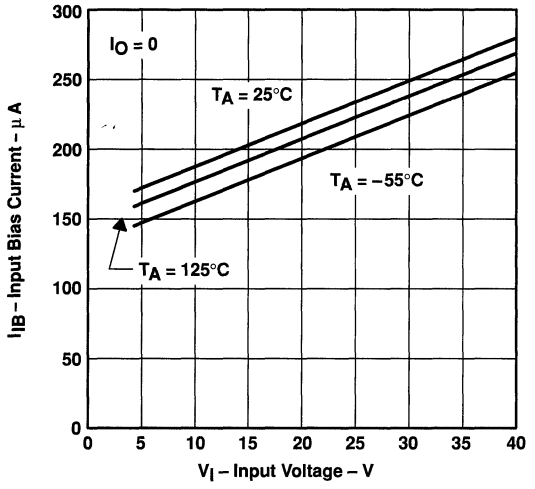


Figure 5

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

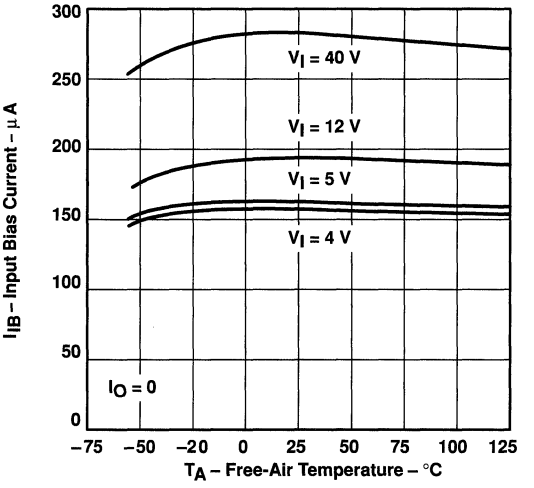


Figure 6

OUTPUT VOLTAGE REGULATION
vs
OUTPUT CURRENT

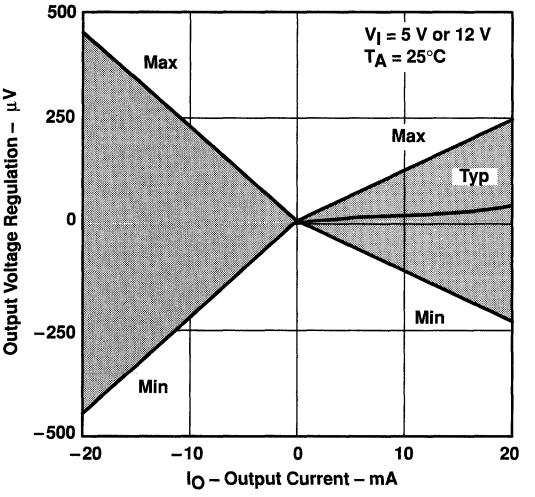


Figure 7

OUTPUT IMPEDANCE
vs
FREQUENCY

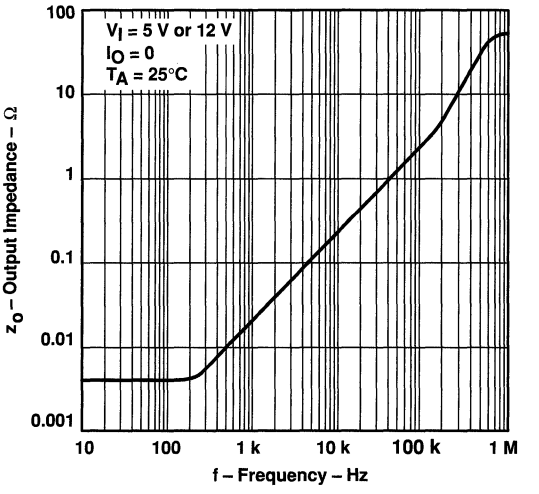


Figure 8

† Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT
vs
INPUT VOLTAGE

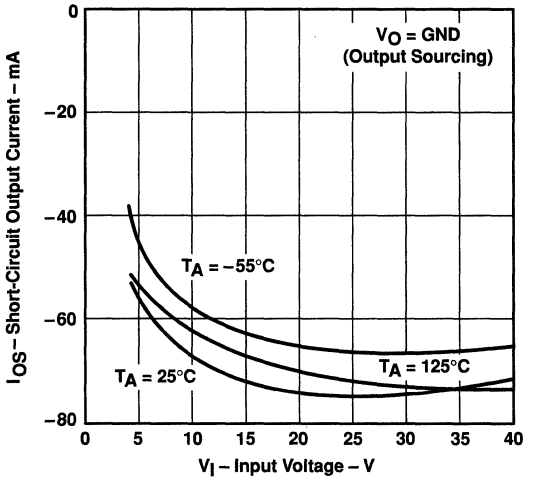


Figure 9

SHORT-CIRCUIT OUTPUT CURRENT
vs
INPUT VOLTAGE

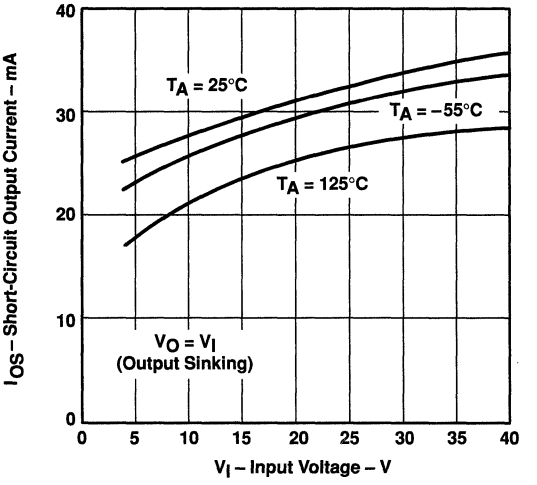


Figure 10

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

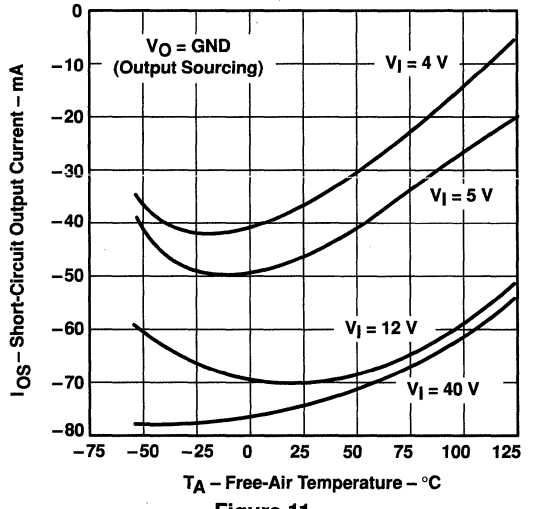


Figure 11

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

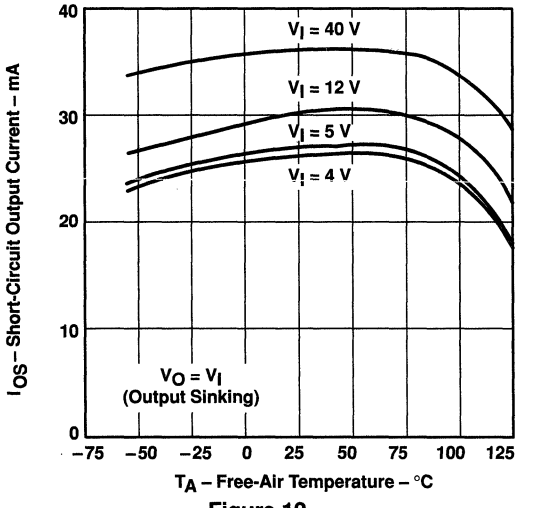


Figure 12

† Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

RIPPLE REJECTION
vs
FREQUENCY

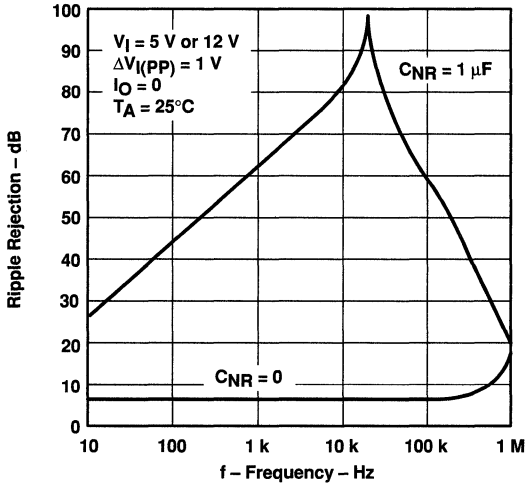


Figure 13

SPECTRAL NOISE VOLTAGE DENSITY
vs
FREQUENCY

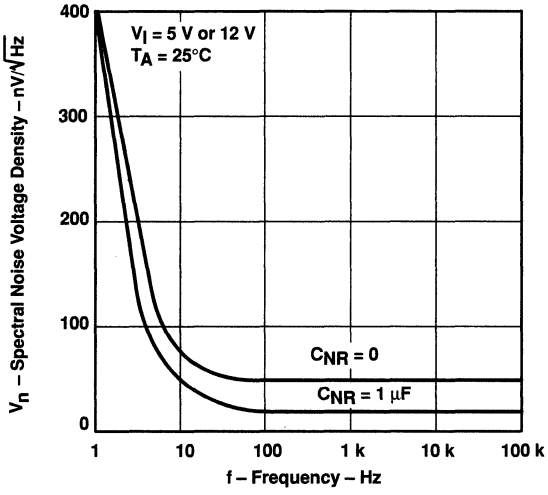


Figure 14

OUTPUT VOLTAGE RESPONSE
TO OUTPUT CURRENT STEP

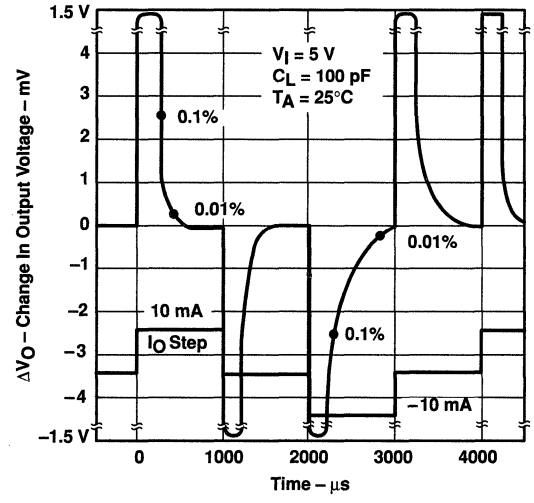


Figure 15

OUTPUT VOLTAGE POWER-UP RESPONSE

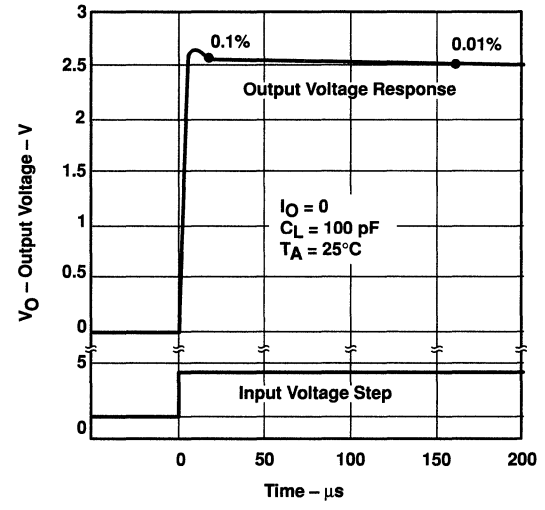


Figure 16

TYPICAL CHARACTERISTICS

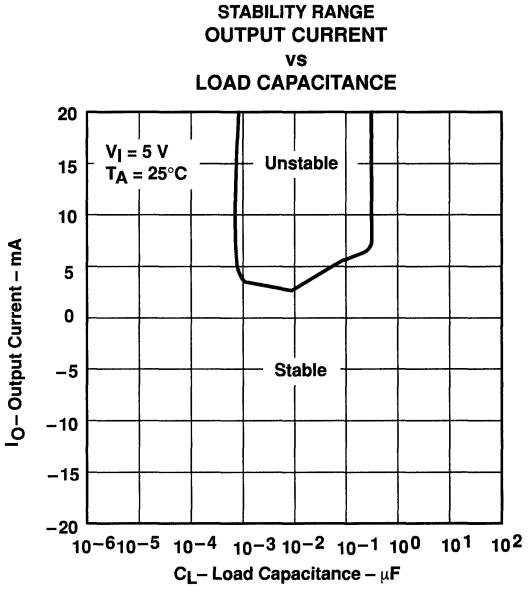


Figure 17

MACROMODEL INFORMATION

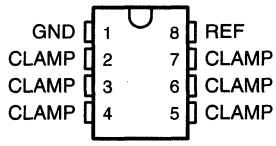
```
*   TLE2426 OPERATIONAL AMPLIFIER "MACROMODEL" SUBCIRCUIT
*   CREATED USING PARTS RELEASE 4.03 0N 08/21/90 AT 13:51
*   REV (N/A)     SUPPLY VOLTAGE: 5 V
*   CONNECTIONS:      FILTER
                      |   INPUT
*                     |   |   COMMON
*                     |   |   |   OUTPUT
*                     |   |   |   |
.SUBCKT TLE2426       1   3   4   5
```

```
    C1     11  12  21.66E-12
    C2      6   7  30.00E-12
    C3     87   0  10.64E-9
    CPSR   85  86  15.9E-9
    DCM+   81  82  DX
    DCM-   83  81  DX
    DC      5  53  DX
    DE     54   5  DX
    DLP    90  91  DX
    DLN    92  90  DX
    DP      4   3  DX
    ECMR   84  99  (2,99) 1
    EGND   99   0  POLY(2)   (3,0) (4,0)   0   .5  .5
    EPSR   85   0  POLY(1)   (3,4)  -16.22E-6 3.24E-6
    ENSE   89   2  POLY(1)   (88,0) 120E-61
    FB      7  99  POLY(6)   VB  VC  VE  VLP VLN VPSR 0 74.8E6 -10E6  10E6   10E6   -10E6  74E6
    GA      6   0  11  12  320.4E-6
    GCM     0   6  10  99  1.013E-9
    GPSR   85  86  (85,86)   100E-6
    GRC1    4  11  (4,11) 3.204E-4
    GRC2    4  12  (4,12) 3.204E-4
    GRE1   13  10  (13,10)   1.038E-3
    GRE2   14  10  (14,10)   1.038E-3
    HLIM   90   0  VLIM   1K
    HCMR   80   1  POLY(2)   VCM+   VCM-   0   1E2    1E2
    IRP     3   4  146E-6
    IEE     3  10  DC  24.05E-6
    IIO     2   0  .2E-9
    I1     88   0  1E-21
    Q1     11  89  13  QX
    Q2     12  80  14  QX
    R2      6   9  100.0E3
    RCM    84  81  1K
    REE    10  99   8.316E6
    RN1    87   0   2.55E8
    RN2    87  88  11.67E3
    RO1     8   5  63
    RO2     7  99  62
    VCM+   82  99  1.0
    VCM-   83  99  -2.3
    VB      9   0  DC  0
    VC      3  53  DC  1.400
    VE     54   4  DC  1.400
    VLIM    7   8  DC  0
    VLP    91   0  DC  30
    VLN     0  92  DC  30
    VPSR    0  86  DC  0
    RFB     5   2  1K
    RIN1    3   1  220K
    RIN2    1   4  220K
.MODEL DX  D(IS=800.OE-18)
.MODEL QX  PNP(IS=800.OE-18 BF=480)
.ENDS
```

SLAS078C – SEPTEMBER 1993 – REVISED JULY 1999

- **Protects Against Latch-Up**
- **25-mA Current Sink in Active State**
- **Less Than 1-mW Dissipation in Standby Condition**
- **Ideal for Applications in Environments Where Large Transient Spikes Occur**
- **Stable Operation for All Values of Capacitive Load**
- **No Output Overshoot**

D OR P PACKAGE
(TOP VIEW)



description

The TL7726 consists of six identical clamping circuits that monitor an input voltage with respect to a reference value, REF. For an input voltage (V_I) in the range of GND to < REF, the clamping circuits present a very high impedance to ground, drawing current of less than 10 μA. The clamping circuits are active for V_I < GND or V_I > REF when they have a very low impedance and can sink up to 25 mA.

These characteristics make the TL7726 ideal as protection devices for CMOS semiconductor devices in environments where there are large positive or negative transients to protect analog-to-digital converters in automotive or industrial systems. The use of clamping circuits provides a safeguard against potential latch-up.

The TL7726C is characterized for operation over the temperature range of 0°C to 70°C. The TL7726I is characterized for operation over the temperature range of –40°C to 85°C. The TL7726Q is characterized for operation over the temperature range of –40°C to 125°C.

AVAILABLE OPTIONS

T_A	SOIC (D)	PLASTIC DIP (P)
0°C to 70°C	TL7726CD	TL7726CP
–40°C to 85°C	TL7726ID	TL7726IP
–40°C to 125°C	TL7726QD	TL7726QP

The D package is available taped and reeled. Add the suffix R to the device type (i.e., TL7726CDR).

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Reference voltage, V_{ref} ..... 6 V
Clamping current, I_{IK} ..... ±50 mA
Junction temperature, T_J ..... 150°C
Package thermal impedance, θ_{JA} (see Notes 1 and 2): D package ..... 97°C/W
P package ..... 127°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C
Storage temperature range, T_{stg} ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
Reference voltage, V_{ref}		4.5	5.5	V
Input clamping current, I_{IK}	$V_I \geq V_{ref}$		25	mA
	$V_I \leq$ GND	−25		
Operating free-air temperature range, T_A	TL7726C	0	70	°C
	TL7726I	−40	85	
	TL7726Q	−40	125	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

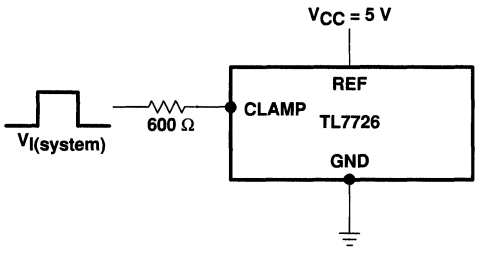
PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IK+}	Positive clamp voltage	I_I = 20 mA	V_{ref}		V_{ref}+200	mV
V_{IK-}	Negative clamp voltage	I_I = 20 mA	−200		0	mV
I_Z	Reference current	V_{ref} = 5 V		25	60	µA
I_I	Input current	V_{ref} − 50 mV ≤ V_I ≤ V_{ref}			10	µA
		GND ≤ V_I ≤ 50 mV	−10			
		50 mV ≤ V_I ≤ V_{ref} − 50 mV	−1		1	

‡ All typical values are at T_A = 25°C.

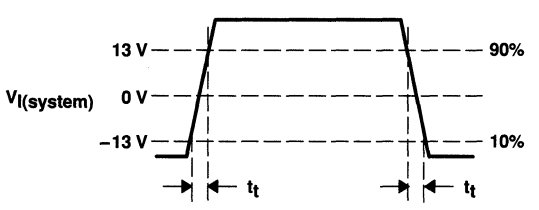
switching characteristics specified at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_s	Settling time	V_I(system) = ±13 V, R_l = 600 Ω, t_t < 1 µs, Measured at 10% to 90%, See Figure 1		30	µs

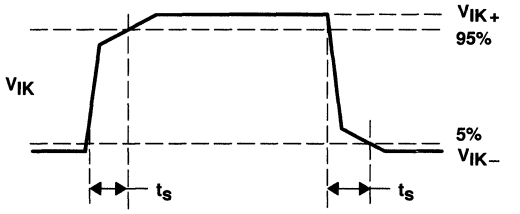
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



INPUT WAVEFORM



CLAMP WAVEFORM

Figure 1. Switching Characteristics

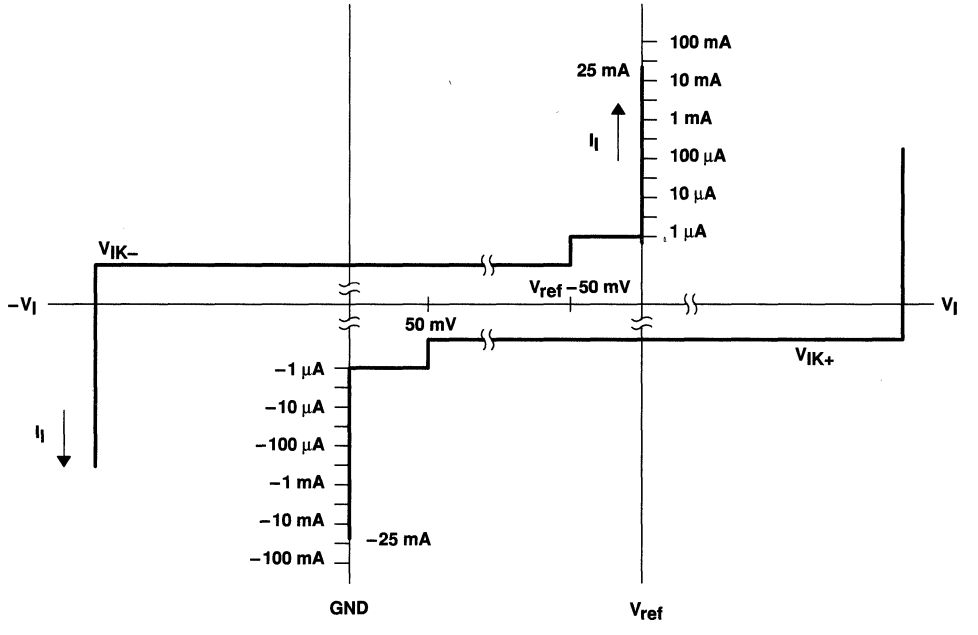
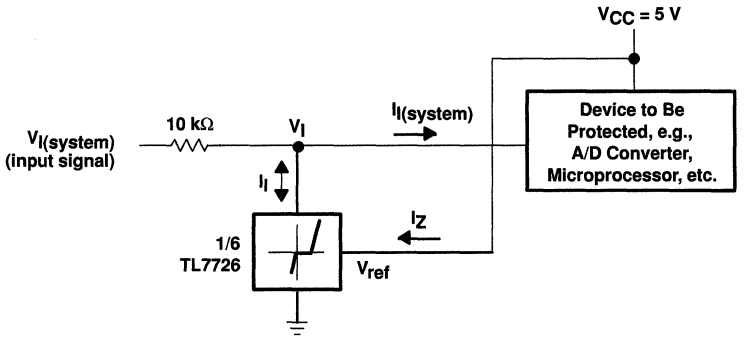


Figure 2. Tolerance Band for Clamping Circuit

APPLICATION INFORMATION



Example: If $I_I >> I_{I(system)}$, i.e., $V_{I(system)} > V_{ref}$ + 200 mV
where:

$I_{I(system)}$ = Input current to the device being protected
$V_{I(system)}$ = Input voltage to the device being protected

then the maximum input voltage

$V_{I(system)max} = V_{ref} + I_I max(10k\Omega)$
$= 5\ V + 25\ mA(10k\Omega)$
$= 5\ V + 250\ V$
$= 255\ V$

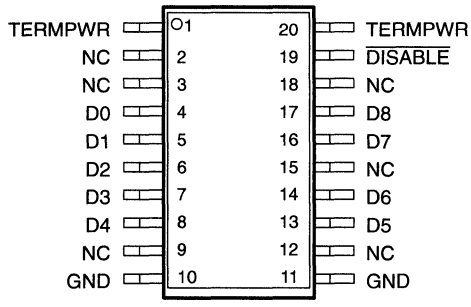
Figure 3. Typical Application

SLVS072C – DECEMBER 1992 – REVISED OCTOBER 1995

available features

- **Fully Integrated 9-Channel SCSI Termination**
- **No External Components Required**
- **Maximum Allowed Current Applied at First High-Level Step**
- **6-pF Typical Power-Down Output Capacitance**
- **Wide V_{term}† (Termination Voltage) Operating Range, 3.5 V to 5.5 V**
- **TTL-Compatible Disable Feature**
- **Compatible With Active Negation**
- **Thermal Regulation**

PW PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TL2218-285 is a current-mode 9-channel monolithic terminator specially designed for single-ended small-computer-systems-interface (SCSI) bus termination. A user-controlled disable function is provided to reduce standby power. No impedance-matching resistors or other external components are required for its operation as a complete terminator.

The device operates over a wide termination-voltage (V_{term}†) range of 3.5 V to 5.5 V, offering an extra 0.5 V of operating range when compared to the minimum termination voltage of 4 V required by other integrated active terminators. The TL2218-285 functions as a current-sourcing terminator and supplies a constant output current of 23 mA into each asserted line. When a line is deasserted, the device senses the rising voltage level and begins to function as a voltage source, supplying a fixed output voltage of 2.85 V. The TL2218-285 features compatibility with active negation drivers and has a typical sink current capability of 20 mA.

The TL2218-285 is able to ensure that maximum current is applied at the first high-level step. This performance means that the device should provide a first high-level step exceeding 2 V even at a 10-MHz rate. Therefore, noise margins are improved considerably above those provided by resistive terminators.

A key difference between the TL2218-285 current-mode terminator and a Boulay terminator is that the TL2218-285 does not incorporate a low dropout regulator to set the output voltage to 2.85 V. In contrast with the Boulay termination concept, the accuracy of the 2.85 V is not critical with the current-mode method used in the TL2218-285 because this voltage does not determine the driver current. Therefore, the primary device specifications are not the same as with a voltage regulator but are more concerned with output current.

The $\overline{\text{DISABLE}}$ terminal is TTL compatible and must be taken low to shut down the outputs. The device is normally active, even when $\overline{\text{DISABLE}}$ is left floating. In the disable mode, only the device startup circuits remain active, thereby reducing the supply current to just 500 µA. Output capacitance in the shutdown mode is typically 6 pF.

The TL2218-285 has on-board thermal regulation and current limiting, thus eliminating the need for external protection circuitry. A thermal regulation circuit that is designed to provide current limiting, rather than an actual thermal shutdown, is included in the individual channels of the TL2218-285. When a system fault occurs that leads to excessive power dissipation by the terminator, the thermal regulation circuit causes a reduction in the asserted-line output current sufficient to maintain operation. This feature allows the bus to remain active during a fault condition, which permits data transfer immediately upon removal of the fault. A terminator with thermal shutdown does not allow for data transfer until sufficient cooling has occurred. Another advantage offered by the TL2218-285 is a design that does not require costly laser trimming in the manufacturing process.

The TL2218-285 is characterized for operation over the virtual junction temperature range of 0°C to 125°C.

† This symbol is not presently listed within EIA/JEDEC standards for letter symbols.

AVAILABLE OPTIONS

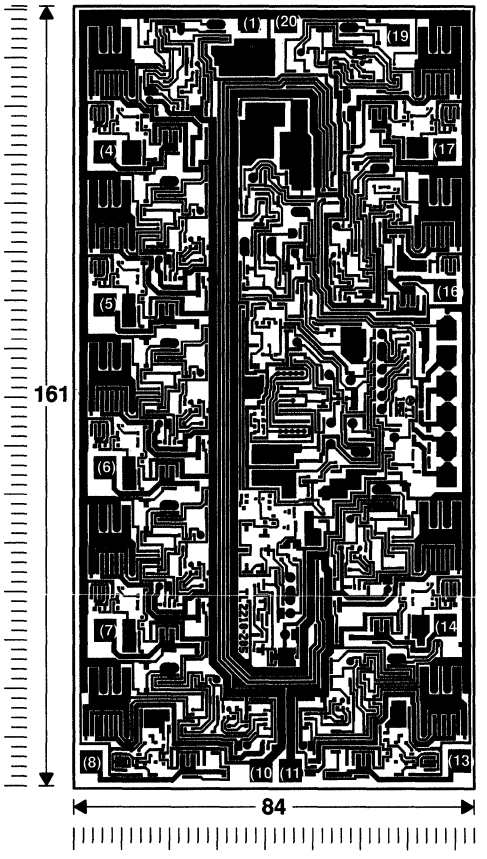
T_J	SURFACE MOUNT (PW)†	CHIP FORM (Y)
0°C to 125°C	TL2218-285PWLE	TL2218-285Y

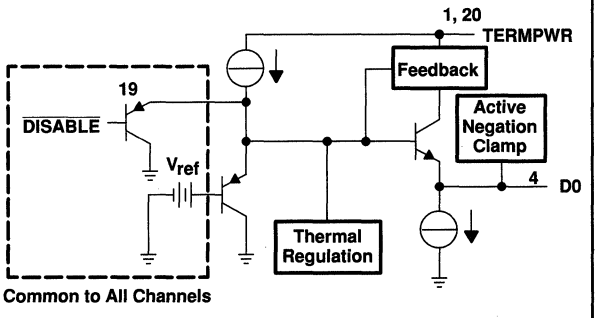
† The PW package is only available left-end taped and reeled.

TL2218-285Y chip information

This chip, when properly assembled, displays characteristics similar to the TL2218-285. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 11 MILS TYPICAL

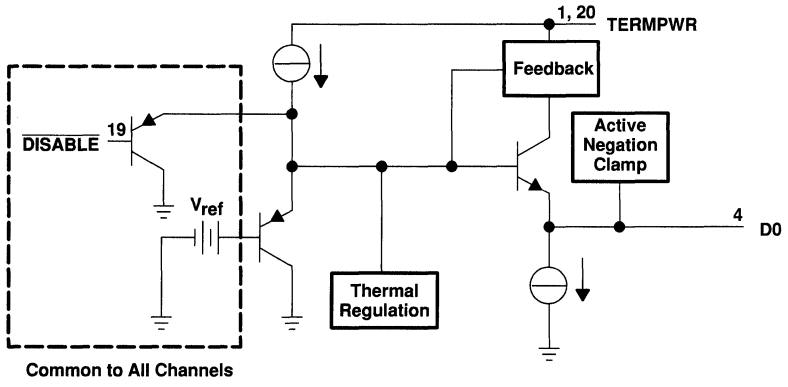
BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

functional block diagram (each channel)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted) (see Figures 1, 2, and 3)†

Continuous termination voltage	10 V
Continuous output voltage range	0 V to 5.5 V
Continuous disable voltage range	0 V to 5.5 V
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	–55°C to 150°C
Storage temperature range, T_{stg}	–60°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING AT	T ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T = 25°C	T = 70°C POWER RATING	T = 85°C POWER RATING	T = 125°C POWER RATING
PW	T_A	828 mW	6.62 mW/°C	530 mW	430 mW	166 mW
	T_C	4032 mW	32.2 mW/°C	2583 mW	2100 mW	812 mW
	T_L‡	2475 mW	19.8 mW/°C	1584 mW	1287 mW	495 mW

‡ $R_{\theta JL}$ is the thermal resistance between the junction and device lead. To determine the virtual junction temperature (T_J) relative to the device lead temperature, the following calculations should be used: $T_J = P_D \times R_{\theta JL} + T_L$, where P_D is the internal power dissipation of the device and T_L is the device lead temperature at the point of contact to the printed wiring board. $R_{\theta JL}$ is 50.5°C/W.

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

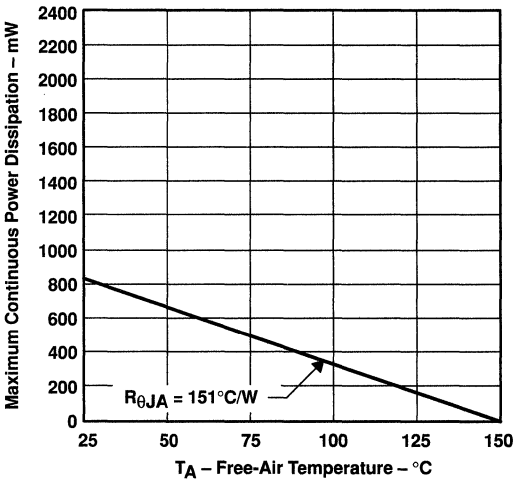


Figure 1

CASE TEMPERATURE
DISSIPATION DERATING CURVE

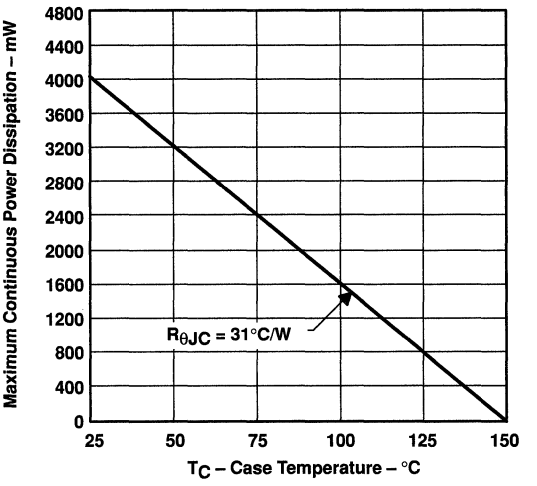


Figure 2

LEAD TEMPERATURE
DISSIPATION DERATING CURVE

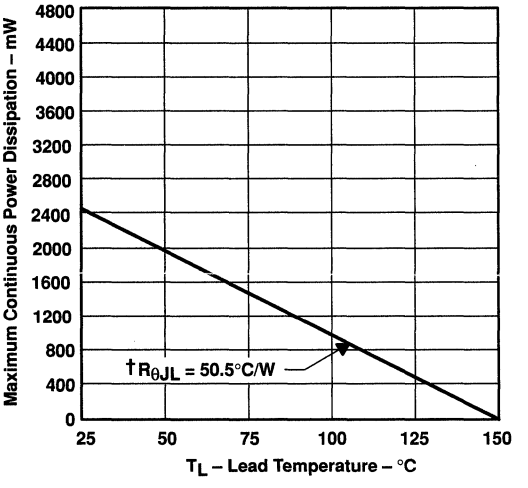


Figure 3

† $R_{\theta JL}$ is the thermal resistance between the junction and device lead. To determine the virtual junction temperature (T_J) relative to the device lead temperature, the following calculations should be used: $T_J = P_D \times R_{\theta JL} + T_L$, where P_D is the internal power dissipation of the device, and T_L is the device lead temperature at the point of contact to the printed wiring board. $R_{\theta JL}$ is 50.5°C/W.

recommended operating conditions

	MIN	MAX	UNIT
Termination voltage	3.5	5.5	V
High-level disable input voltage, V_{IH}	2	V_{term}	V
Low-level disable input voltage, V_{IL}	0	0.8	V
Operating virtual junction temperature, T_J	0	125	°C

electrical characteristics, V_{term} = 4.75 V, V_O = 0.5 V, T_J = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output high voltage		2.5	2.85		V
TERMPWR supply current	All data lines open		9		mA
	All data lines = 0.5 V		228		
	$\overline{\text{DISABLE}}$ = 0 V		500		µA
Output current		−20.5	−23	−24	mA
Disable input current (see Note 1)	$\overline{\text{DISABLE}}$ = 4.75 V			1	µA
	$\overline{\text{DISABLE}}$ = 0 V			600	
Output leakage current	$\overline{\text{DISABLE}}$ = 0 V		100		nA
Output capacitance, device disabled	V_O = 0 V, 1 MHz		6		pF
Termination sink current, total	V_O = 4 V		20		mA

NOTE 1: When $\overline{\text{DISABLE}}$ is open or high, the terminator is active.

THERMAL INFORMATION

The need for smaller surface-mount packages for use on compact printed-wiring boards (PWB) causes an increasingly difficult problem in the area of thermal dissipation. In order to provide the systems designer with a better approximation of the junction temperature rise in the thin-shrink small-outline package (TSSOP), the junction-to-lead thermal resistance ($R_{\theta JL}$) is provided along with the more typical values of junction-to-ambient and junction-to-case thermal resistances, $R_{\theta JA}$ and $R_{\theta JC}$.

$R_{\theta JL}$ is used to calculate the device junction temperature rise measured from the leads of the unit. Consequently, the junction temperature is dependent upon the board temperature at the leads, $R_{\theta JL}$, and the internal power dissipation of the device. The board temperature is contingent upon several variables, including device packing density, thickness, material, area, and number of interconnects. The $R_{\theta JL}$ value depends on the number of leads connecting to the die-mount pad, the lead-frame alloy, area of the die, mount material, and mold compound. Since the power level at which the TSSOP can be used is highly dependent upon both the temperature rise of the PWB and the device itself, the systems designer can maximize this level by optimizing the circuit board. The junction temperature of the device can be calculated using the equation $T_J = (P_D \times R_{\theta JL}) + T_L$ where T_J = junction temperature, P_D = power dissipation, $R_{\theta JL}$ = junction-to-lead thermal resistance, and T_L = board temperature at the leads of the unit.

The values of thermal resistance for the TL2218-285 PW are as follows:

Thermal Resistance	Typical Junction Rise
$R_{\theta JA}$	151°C/W
$R_{\theta JC}$	31 °C/W
$R_{\theta JL}$	50.5°C/W

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_O	Output current	vs Input voltage	4
V_O	Output voltage	vs Input voltage	5
I_O	Output current	vs Junction temperature	6
V_O	Output voltage	vs Junction temperature	7

TYPICAL CHARACTERISTICS

OUTPUT CURRENT
vs
INPUT VOLTAGE

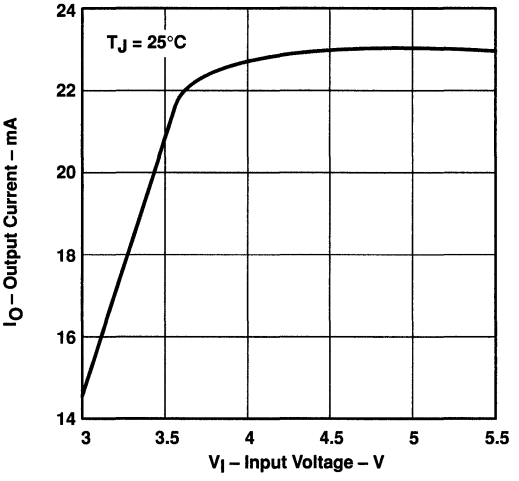


Figure 4

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

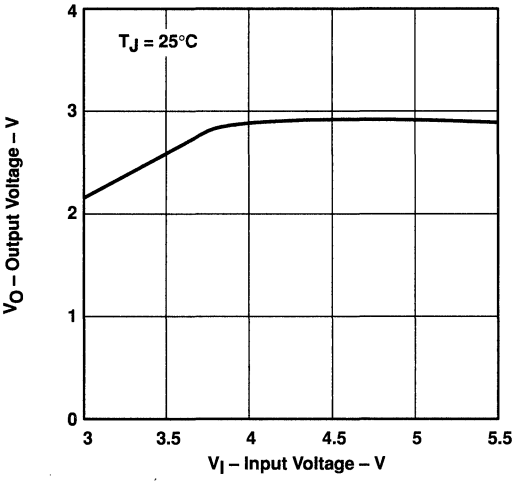


Figure 5

OUTPUT CURRENT
vs
JUNCTION TEMPERATURE

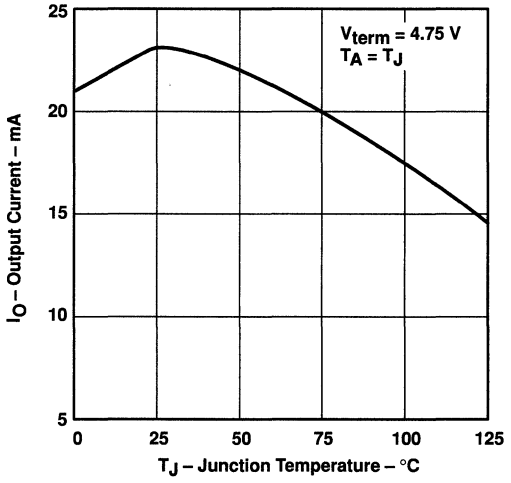


Figure 6

OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

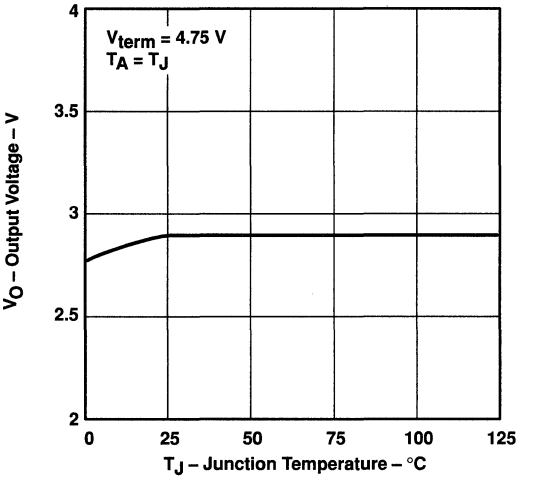
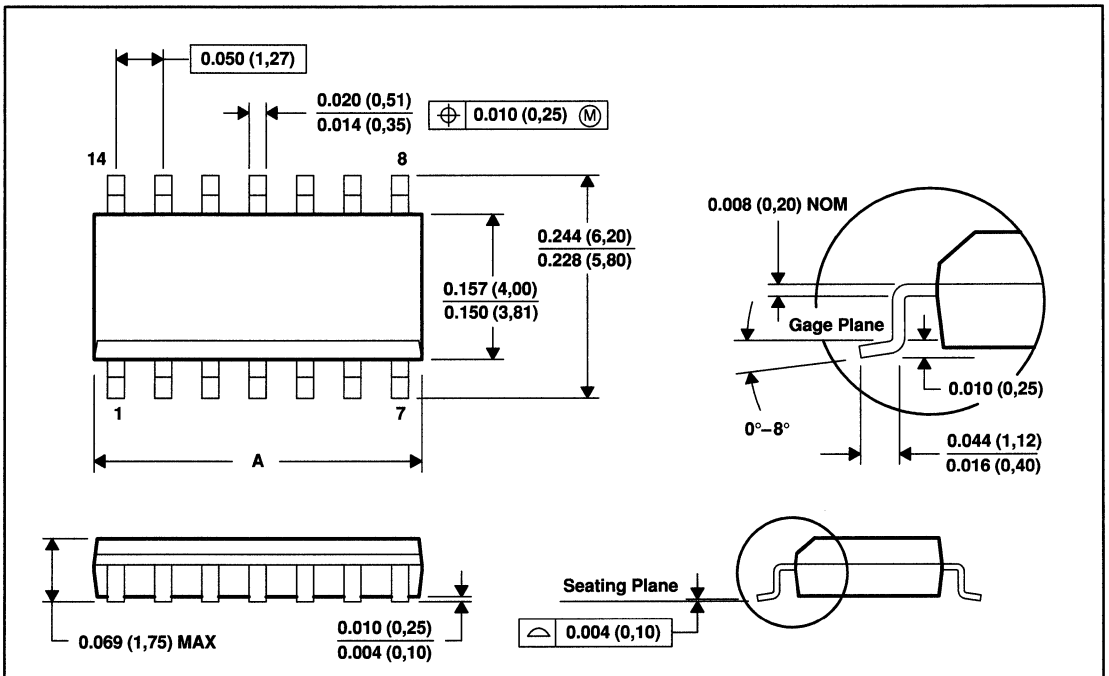


Figure 7

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

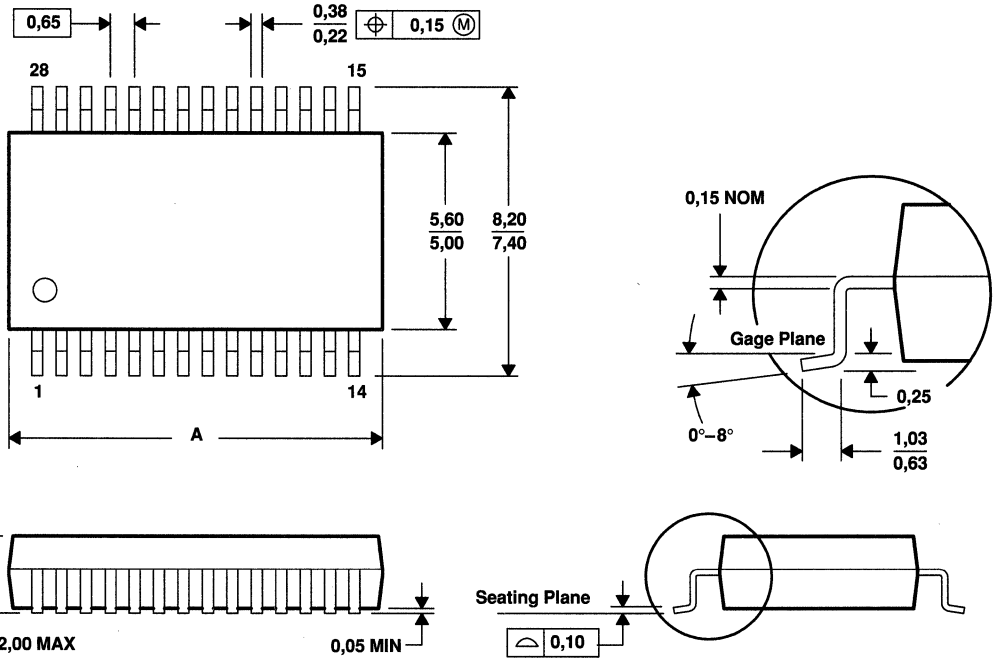
4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL INFORMATION

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

28 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28	30	38
A MAX	3,30	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	2,70	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 / C 10/95

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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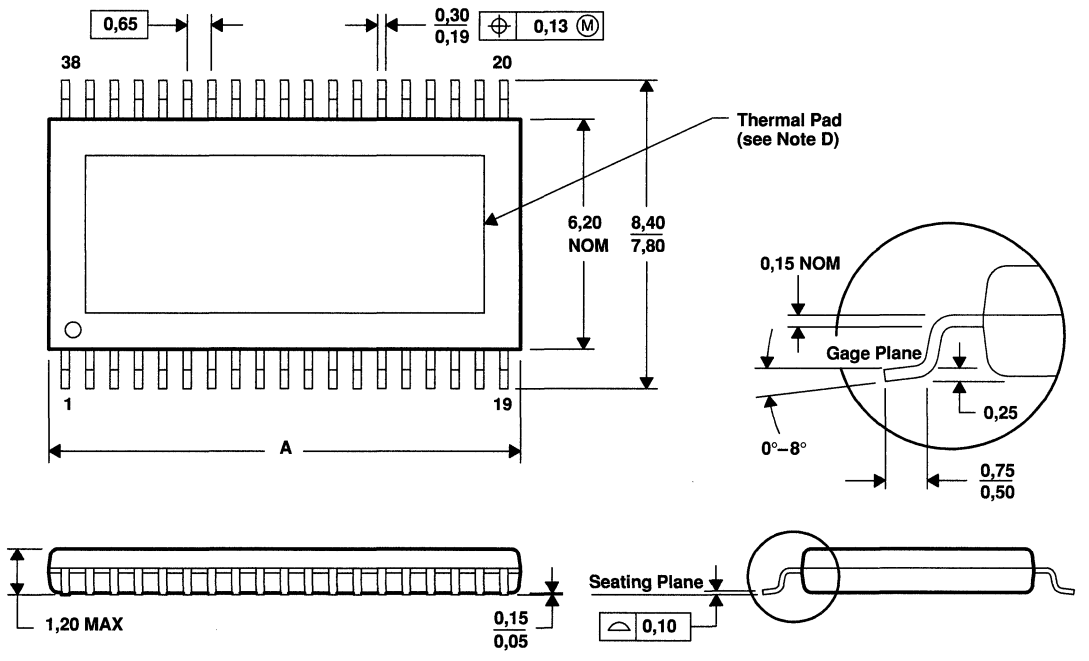
MECHANICAL INFORMATION

DAP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**

38 PINS SHOWN



DIM \ PINS **	28	30	32	38
A MAX	9,80	11,10	11,10	12,60
A MIN	9,60	10,90	10,90	12,40

4073257/A 07/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

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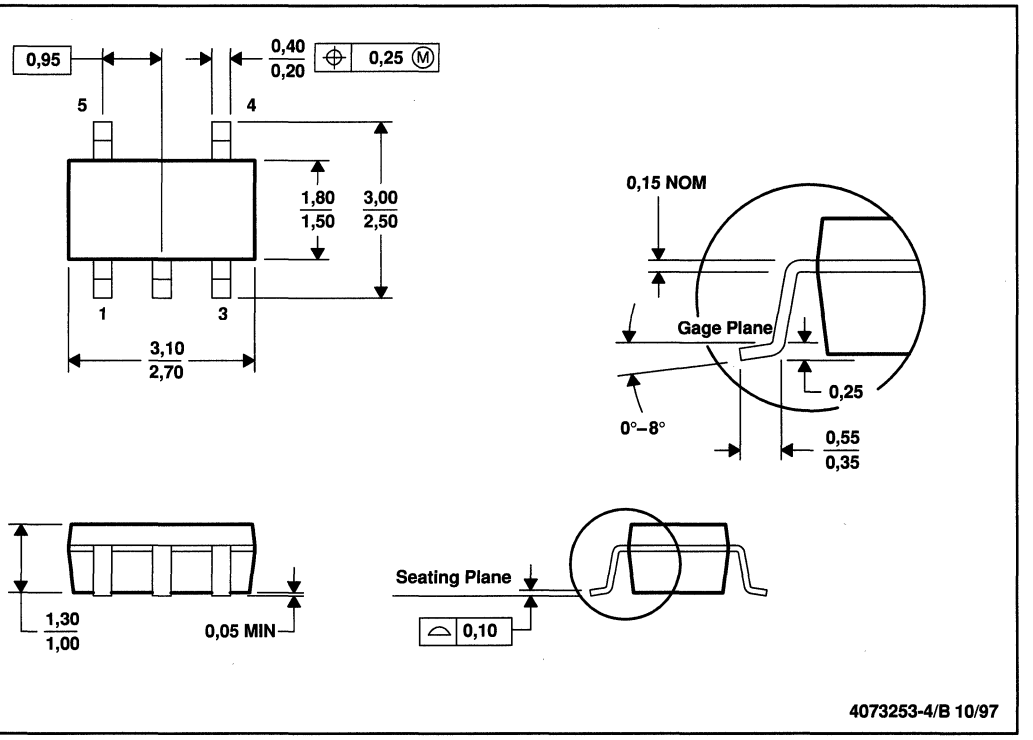
MECHANICAL INFORMATION

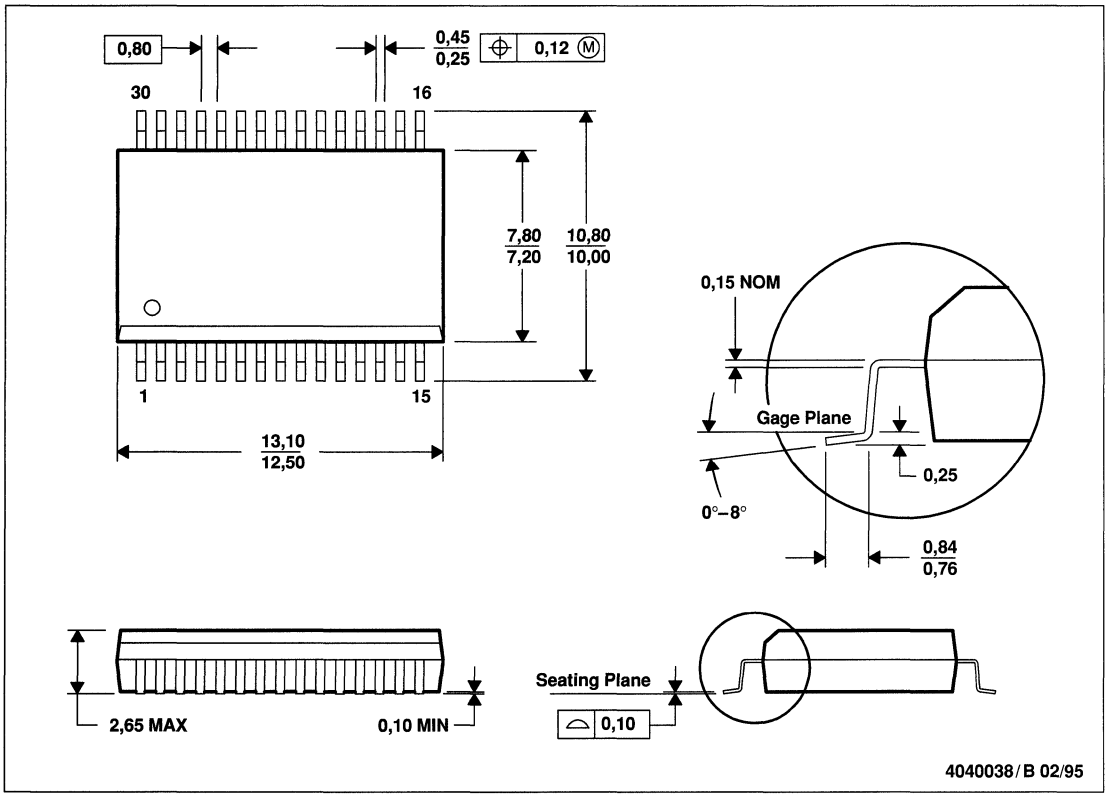
DBV (R-PDSO-G5) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

MECHANICAL INFORMATION

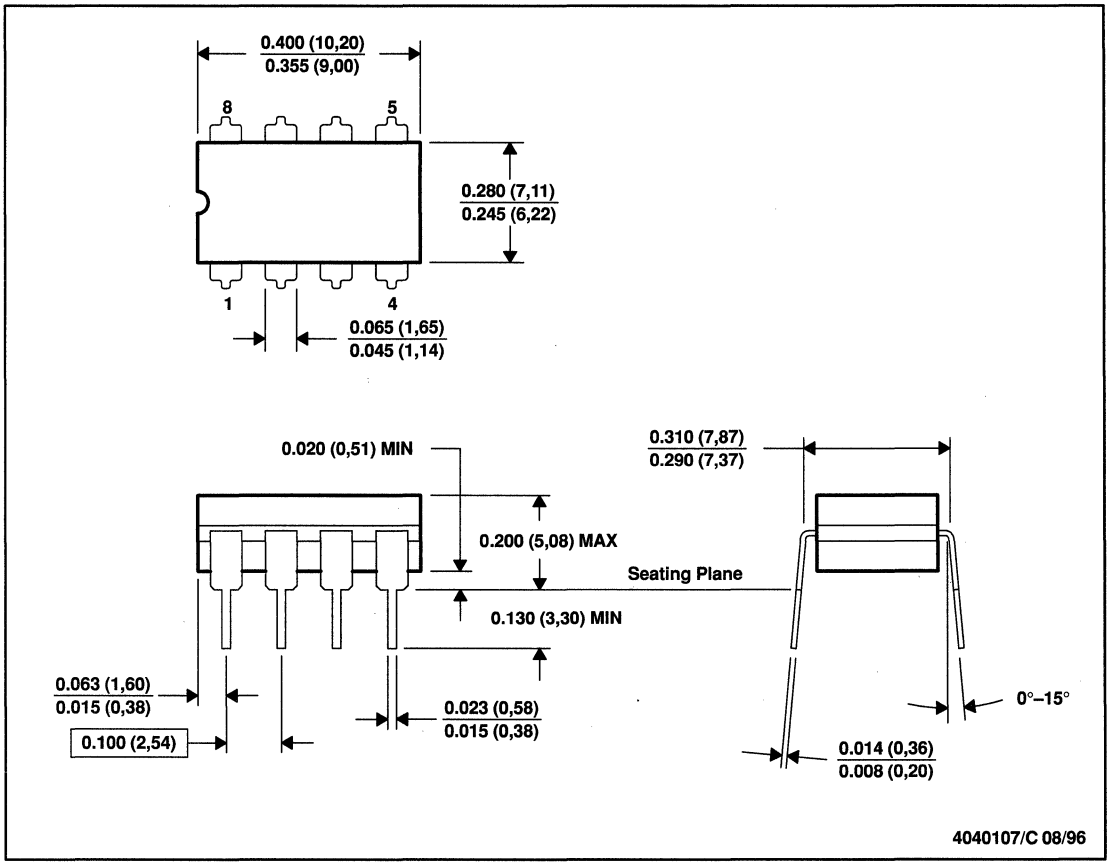
DF (R-PDSO-G30) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

MECHANICAL INFORMATION

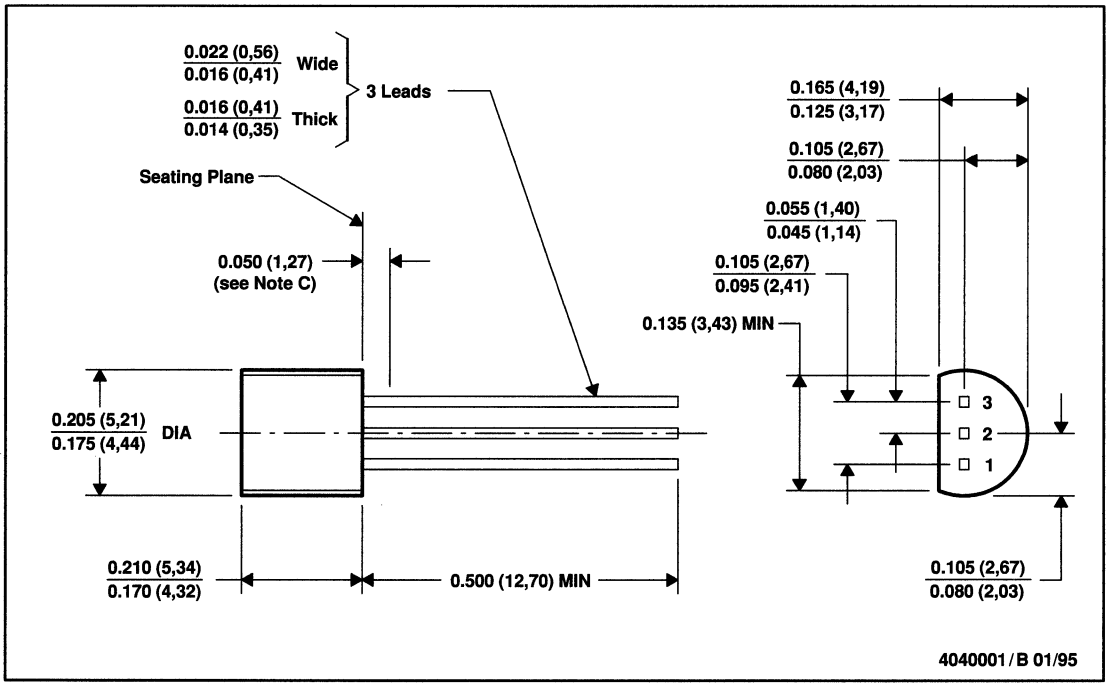
JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL-STD-1835 GDIP1-T8

MECHANICAL INFORMATION

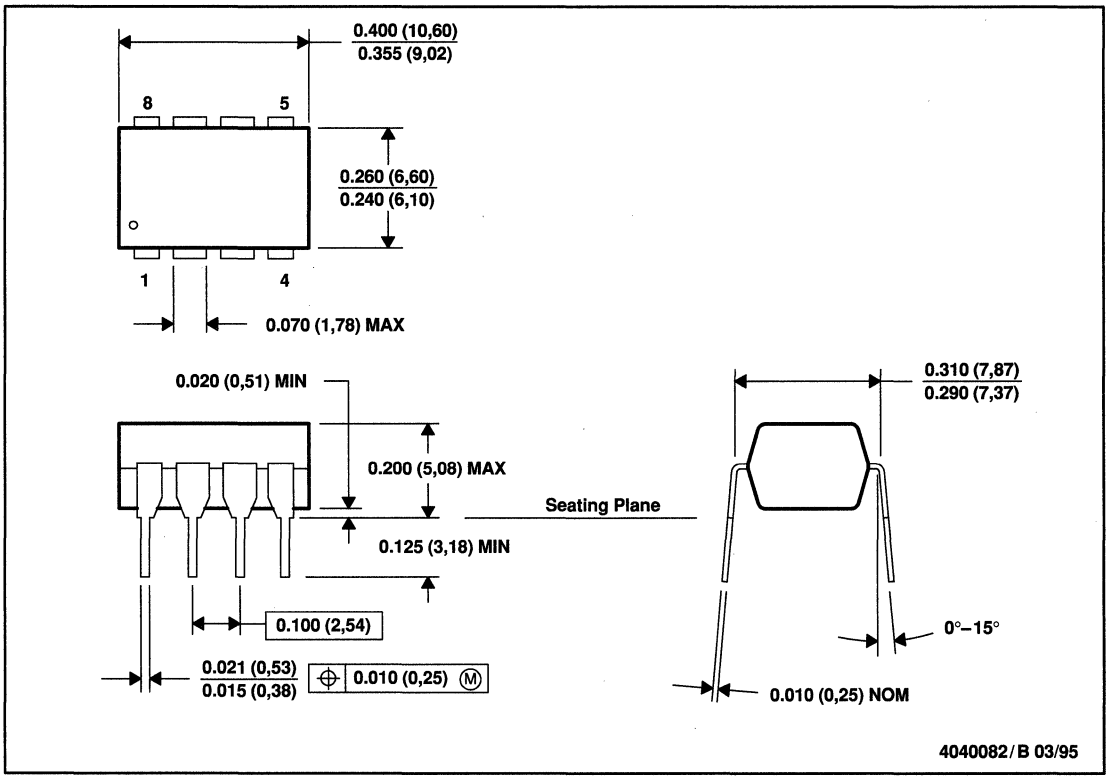
LP (O-PBCY-W3) **PLASTIC CYLINDRICAL PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead dimensions are not controlled within this area.
D. Falls within JEDEC TO-226AA (TO-226AA replaces TO-92)

MECHANICAL INFORMATION

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE PACKAGE**

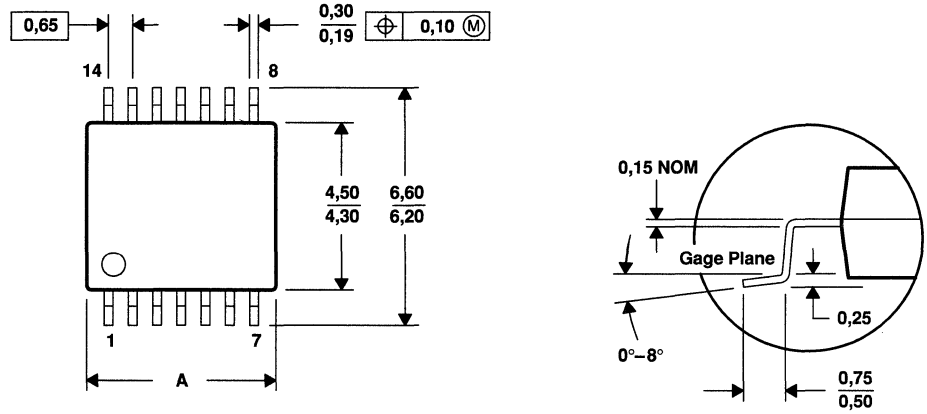


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

MECHANICAL INFORMATION

PW (R-PDSO-G)** PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

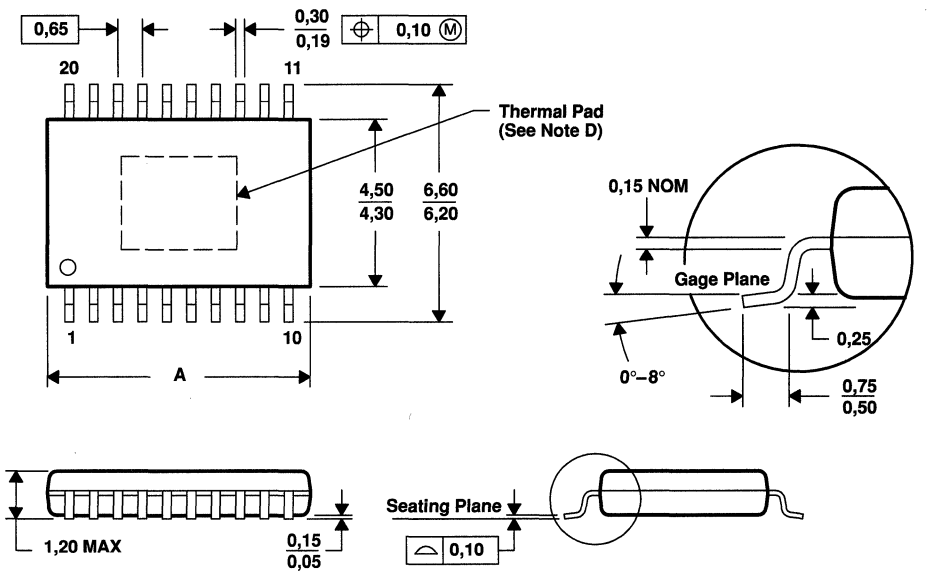
4040064/E 08/96

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

MECHANICAL INFORMATION

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE**

20 PINS SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/F 10/98

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

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